

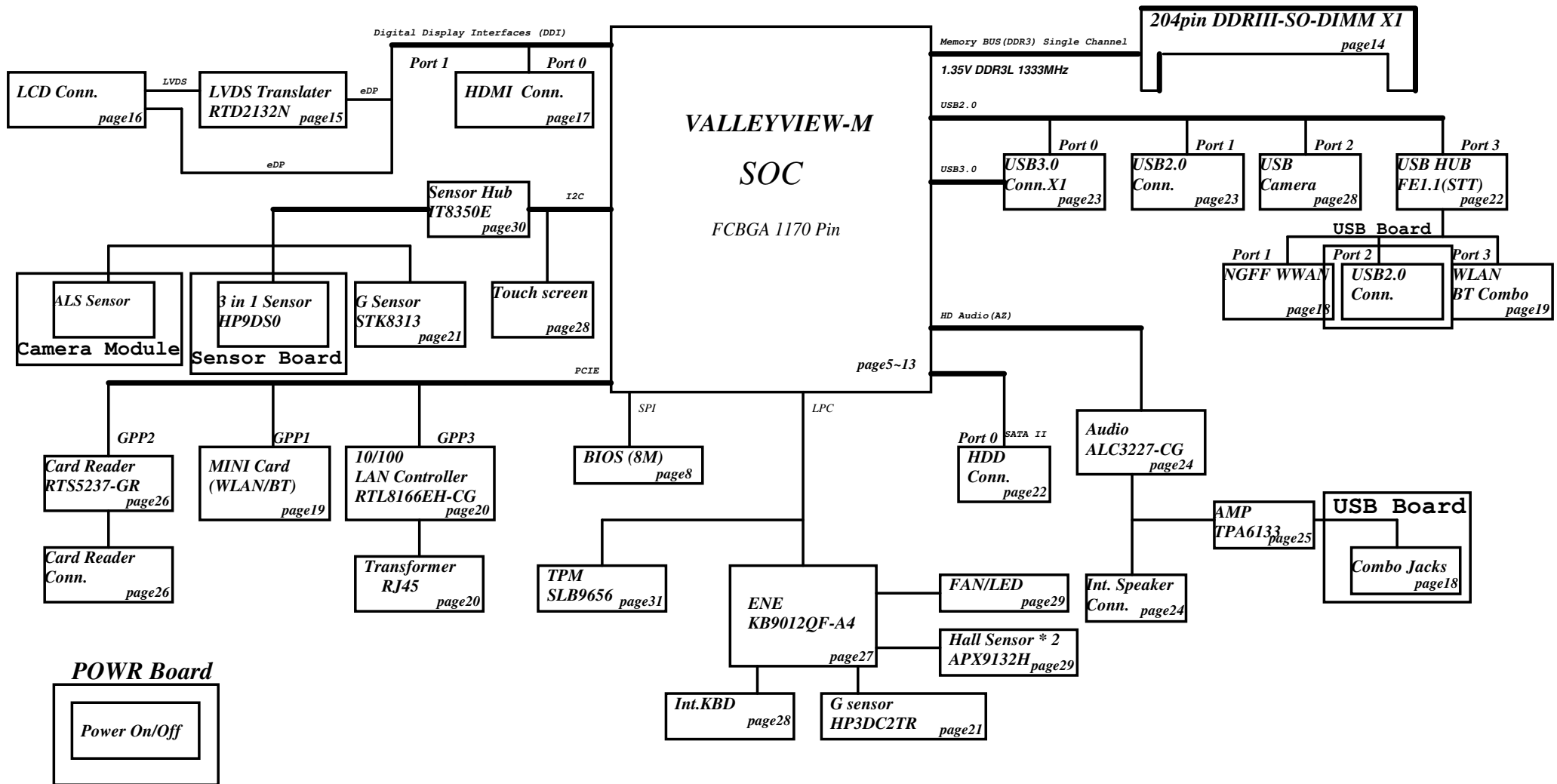
Compal Confidential

ZPT10 UMA M/B LA-B151P Schematics Document

Intel Bay Trail M

2014-01-14
Rev:1.0

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Voltage Rails

Power Plane	Description	S0	S3	S4/S5
VIN	19V Adapter power supply	ON	ON	ON
BATT+	12V Battery power supply	ON	ON	ON
B+	AC or battery power rail for power circuit. (19V/12V)	ON	ON	ON
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.0VALW	+1.0v Always power rail	ON	ON	ON
+1.2VALW	+1.2v Always power rail	ON	ON	ON
+1.8VALW	+1.8v Always power rail	ON	ON	ON
+3VALW	+3.3v Always power rail	ON	ON	ON
+5VALW	+5.0v Always power rail	ON	ON	ON
+1.35V	+1.35V power rail for DDR3L	ON	ON	OFF
+SOC_VCC	Core voltage for SOC	ON	OFF	OFF
+SOC_VNN	GFX voltage for SOC	ON	OFF	OFF
+0.675VS	+0.675V power rail for DDR3L Terminator	ON	OFF	OFF
+1.0VS	+1.0v system power rail	ON	OFF	OFF
+1.05VS	+1.05v system power rail	ON	OFF	OFF
+1.35VS	+1.35v system power rail	ON	OFF	OFF
+1.5VS	+1.5v system power rail	ON	OFF	OFF
+1.8VS	+1.8v system power rail	ON	OFF	OFF
+3VS	+3.3v system power rail	ON	OFF	OFF
+5VS	+5.0v system power rail	ON	OFF	OFF
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 1%			
Ra/Rc/Re	100K +/- 1%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0.300V
1	12K+/- 1%	0.307V	0.354V	0.360V
2	15K+/- 1%	0.423V	0.430V	0.438V
3	20K+/- 1%	0.541V	0.550V	0.559V
4	27K+/- 1%	0.691V	0.702V	0.713V
5	33K+/- 1%	0.807V	0.819V	0.831V
6	43K+/- 1%	0.978V	0.992V	1.006V
7	56K+/- 1%	1.169V	1.185V	1.200V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	

BOM Option Table

BTO Item	BOM Structure
Unpop	@
Connector	CONN@
EMI requirement	EMI@
ESD requirement	ESD@
EMI requirement unpop	@EMI@
ESD requirement unpop	@ESD@
For Debug	DB@
For LVDS Panel	LVDS@
For eDP Panel	eDP@
RF requirement	RF@
PIR Item 64	
RF requirement unpop	@RF@
For TPM	TPM@

EC SM Bus1 address

Device	Address	
Accelerometer	52 01010010	U25
Charger		
Battery		
Home Key	60 01100000	

SOC SM Bus address

Sensor Hub address

Device	Address		Device	Address	
ChannelA	A0 10100000	JDIMM1	Accelerometer	22 00100010	U2101
Thermal Sensor	4D 01001101	UC3	MP09250	68 01101000	U2(SenSor/B)

DAX

PCB
Part Number = DA600149000
PCB 150 LA-B151P REV0 M/B 3

ZZZ1

HDMI
Part Number = RO0000003HM
PCB 102 LA-B151P REV0 M/B 3
45@

PIR Item 50

USOC1 N3520@

CPU
Part Number = SA00007E940
S IC FH8065301616103 SR1SE B3 2.17G BGA

USOC1 N2820@

CPU
Part Number = SA00007EK30
S IC FH8065301616603 SR1SG B3 2.13G BGA

BOM config

PCB P/N	
4319S432L01	EMI@/ESD@/LVDS@/DB@/RF@/N3520@
4319S432L02	EMI@/ESD@/LVDS@/DB@/RF@/N2820@

43 level BOM table

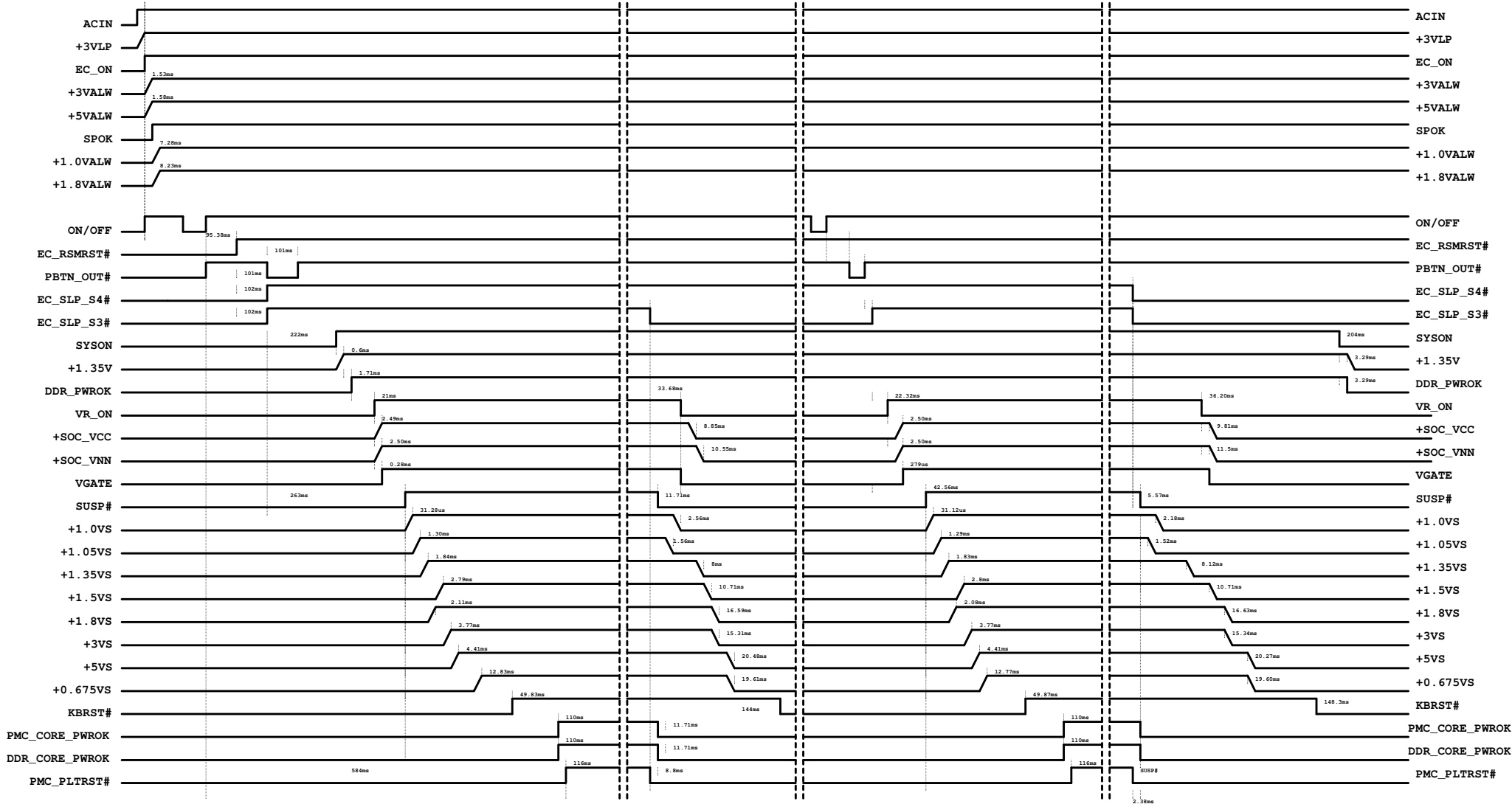
43 Level	Description	BOM Structure
4319S432L01	SMT MB AB151 ZPT10 N3510 4.5W HDMI R1	
4319S432L02	SMT MB AB151 ZPT10 N2810 4.5W HDMI R1	

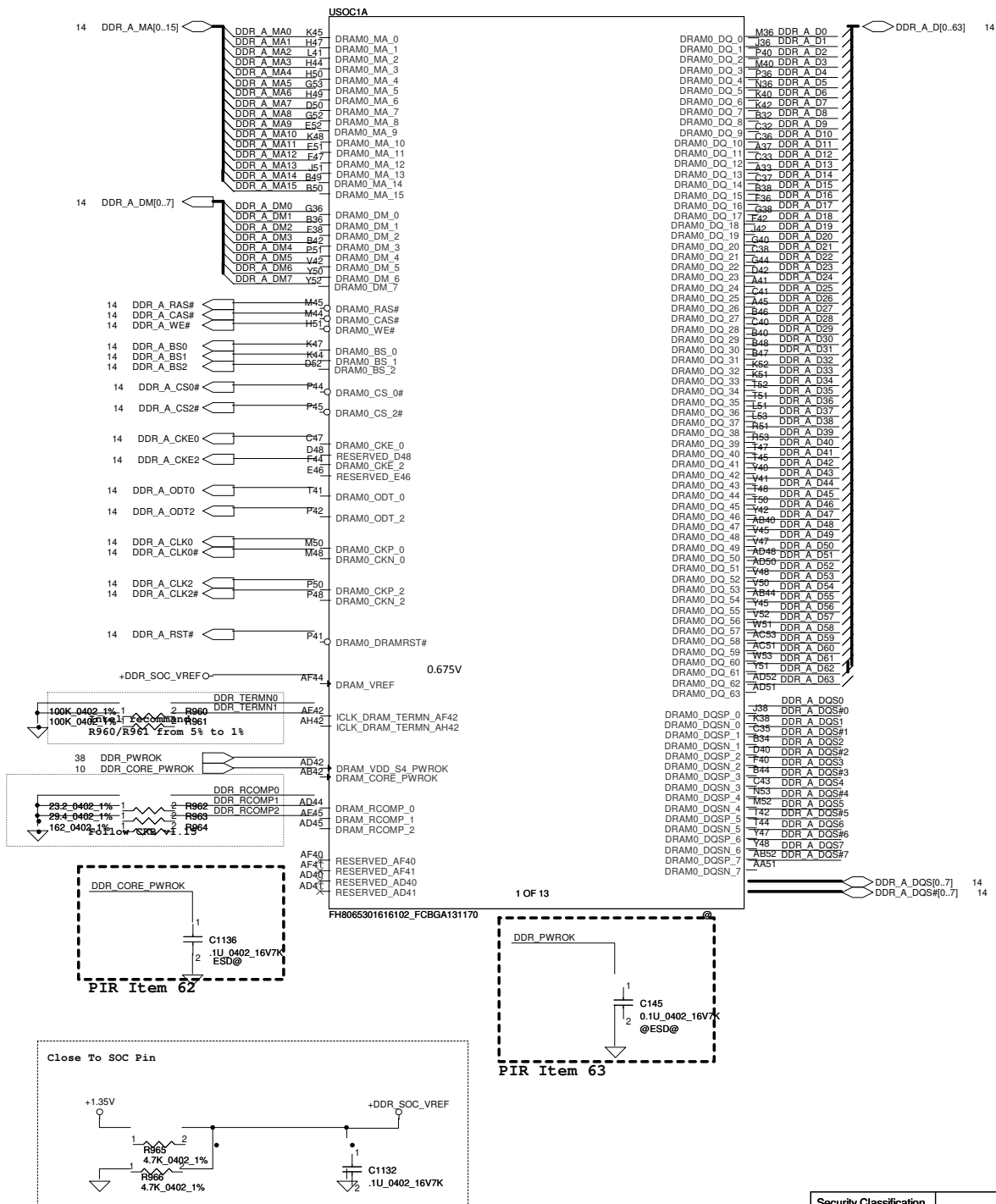
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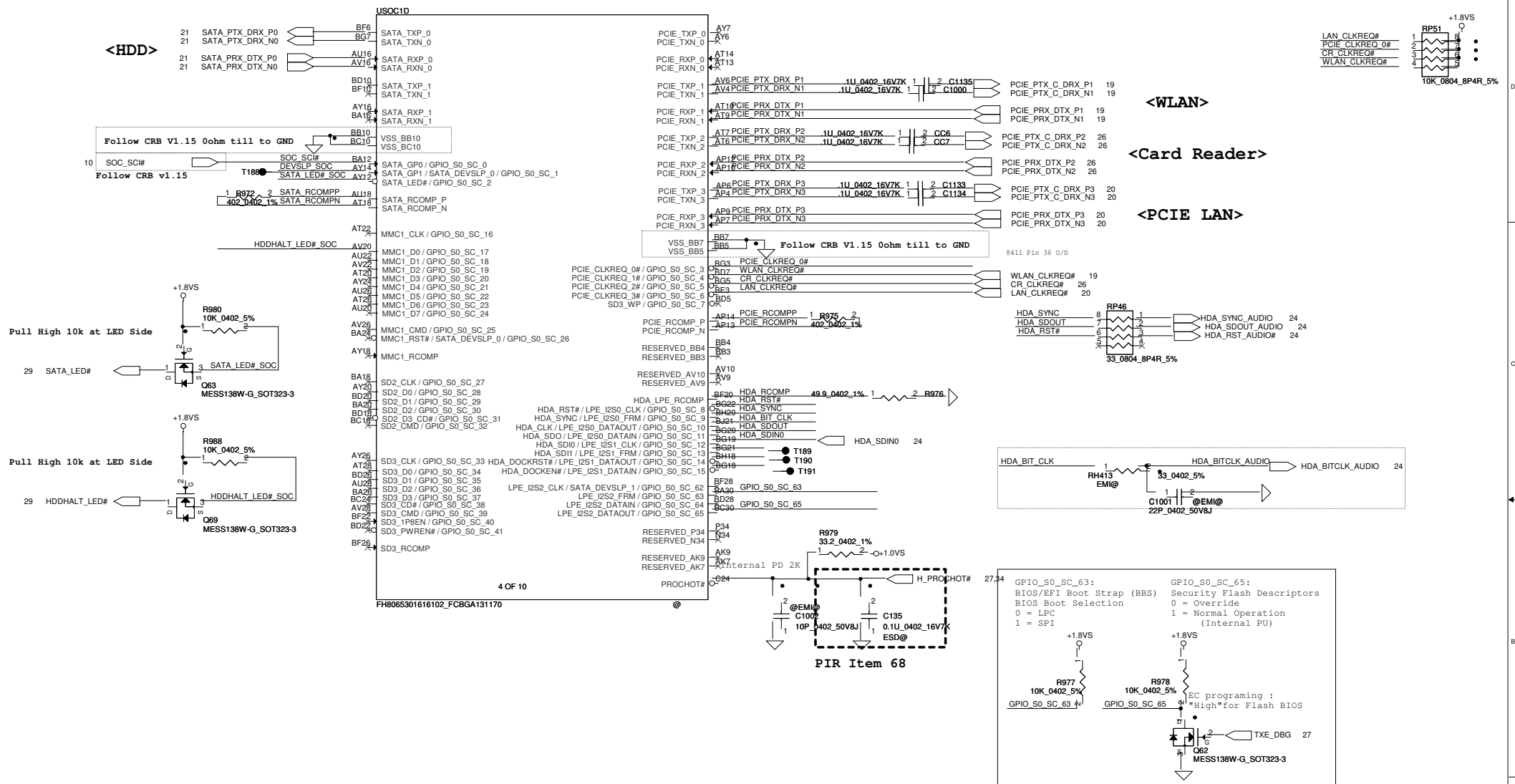
S0->S3

S3->S0

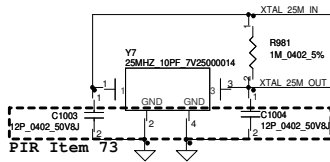
S0->S5







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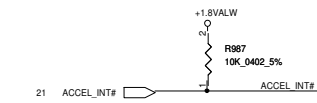
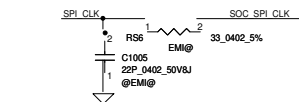
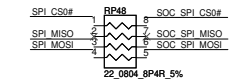
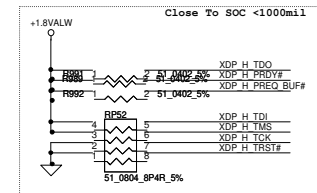


Intel recommend:
C1003/C1004 from 10P to 22P

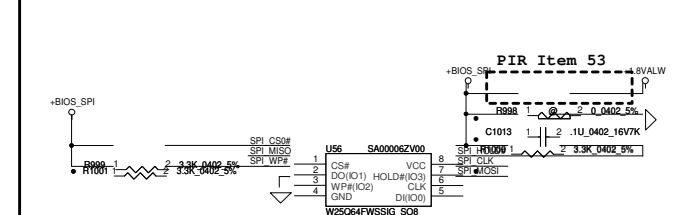
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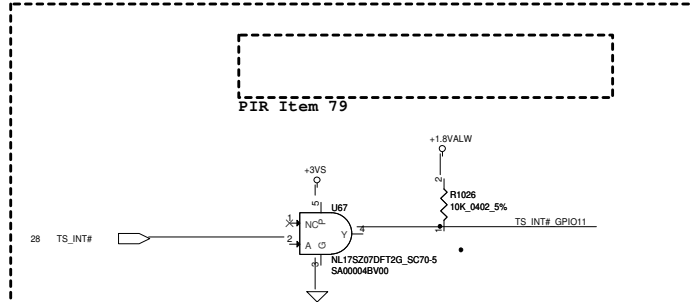
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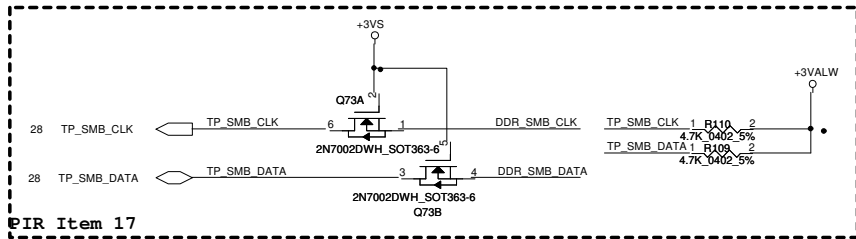
SPI ROM



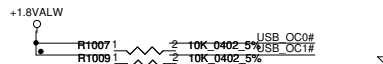
PIR Item 42



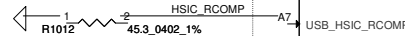
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<Camera>
<USB Hub>

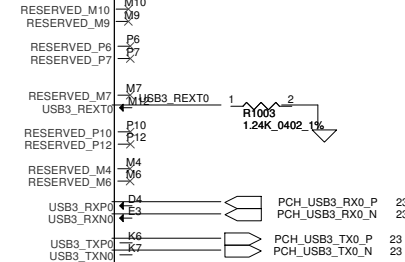
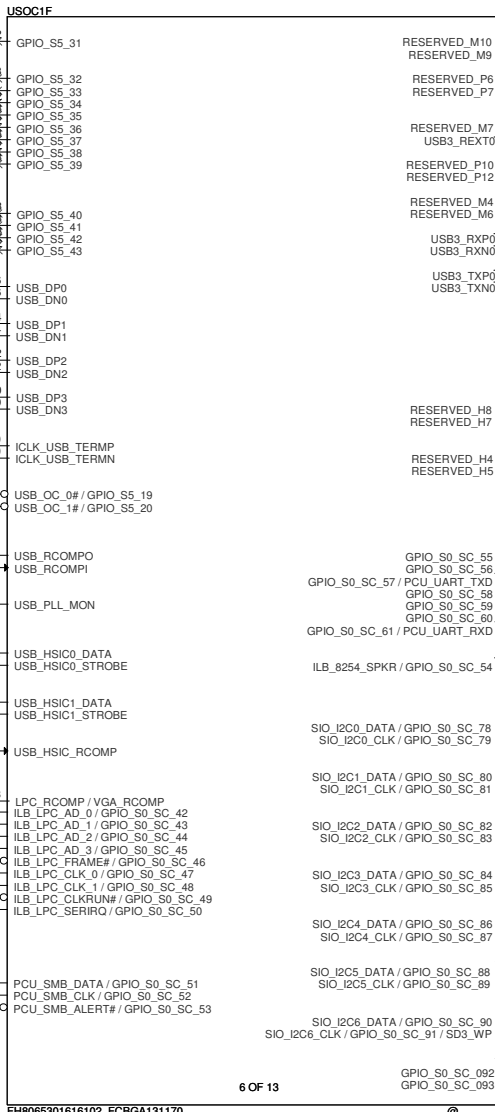
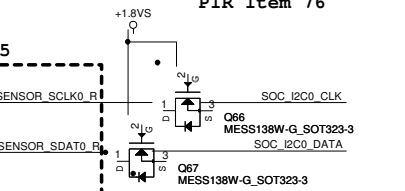
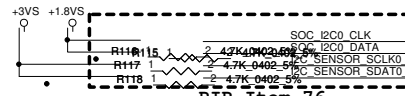
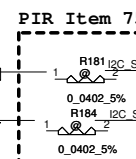
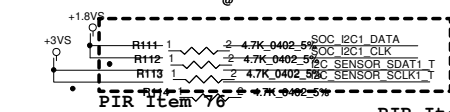
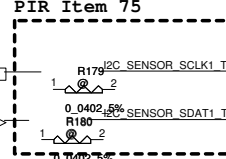
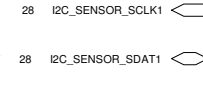
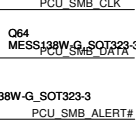
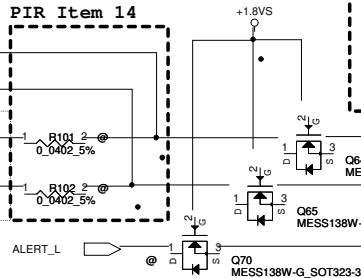
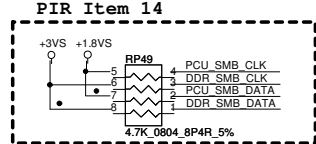
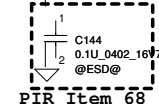
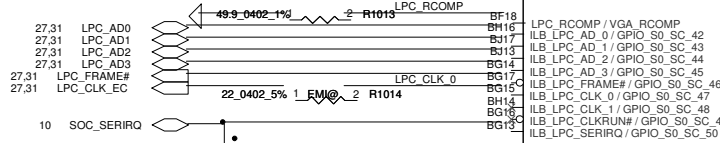
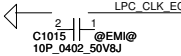


NOTE: Ref checklist rev1.0 p.25
USB_HSIC_RCOMP must NOT float if they are not being used.



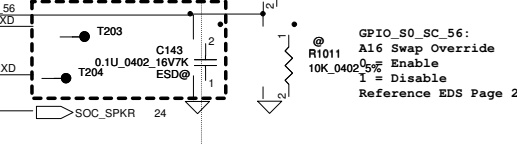
ILB LPC_CLK_0 : Output of 25Mhz,
Need Check with EC

ILB LPC_CLK_1 is for CLK_0 feedback.(Input)
Set to Output for Normal Usage



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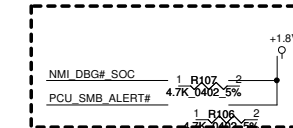
PIR Item 68



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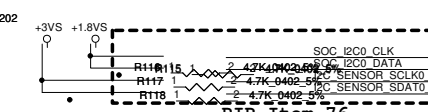
PIR Item 14



PIR Item 37

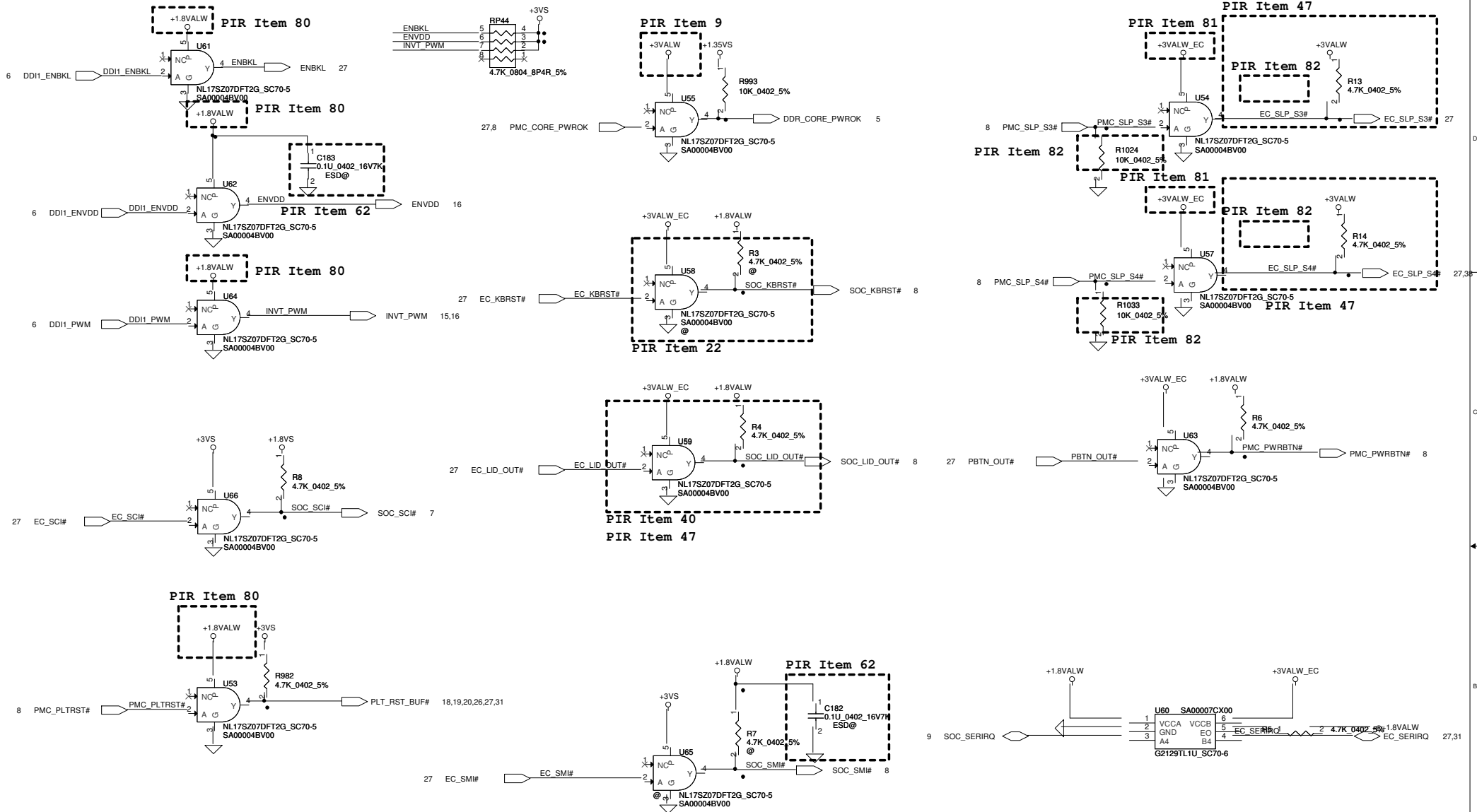


PDA (Platform Debug Assistant) Test Points

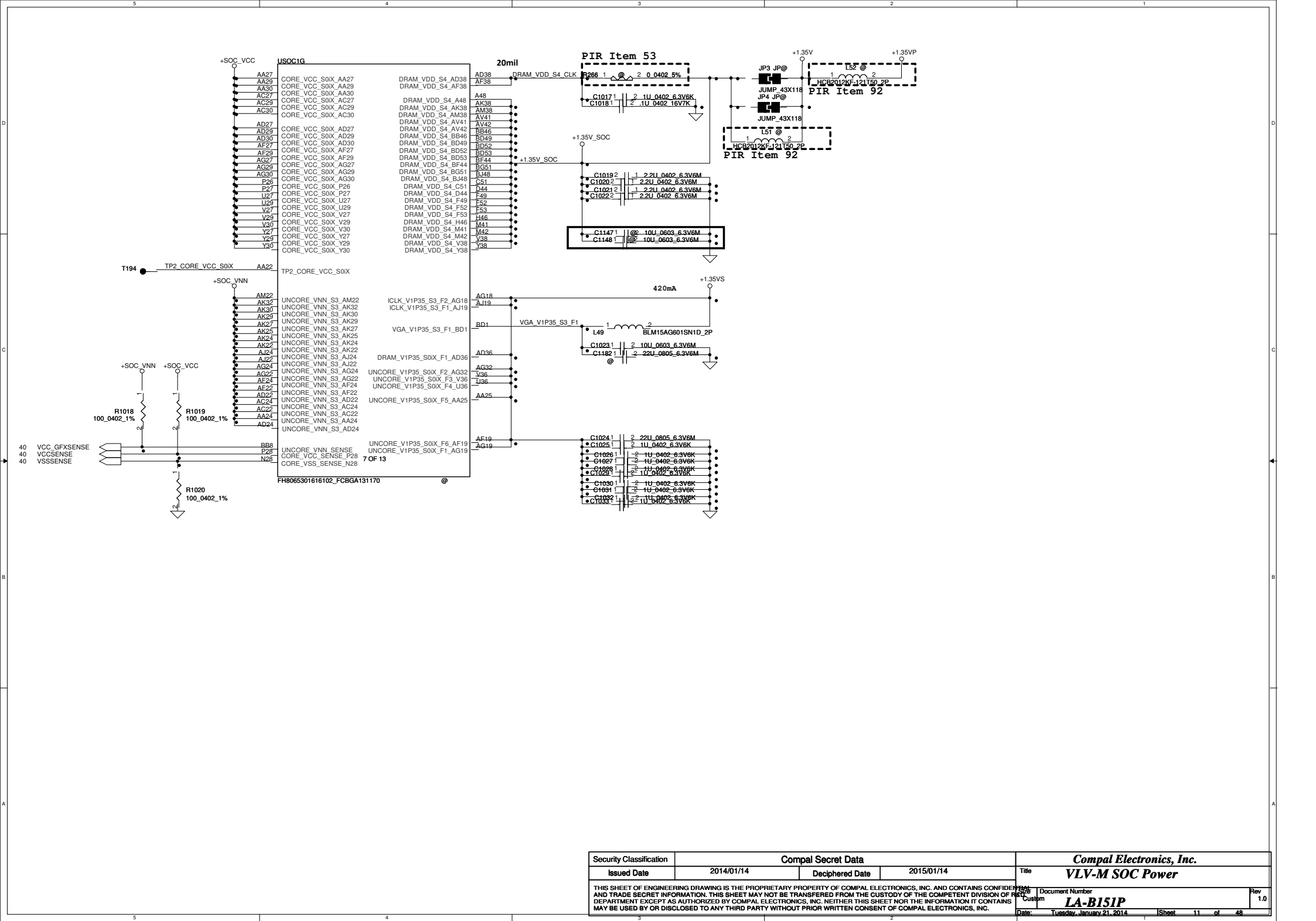


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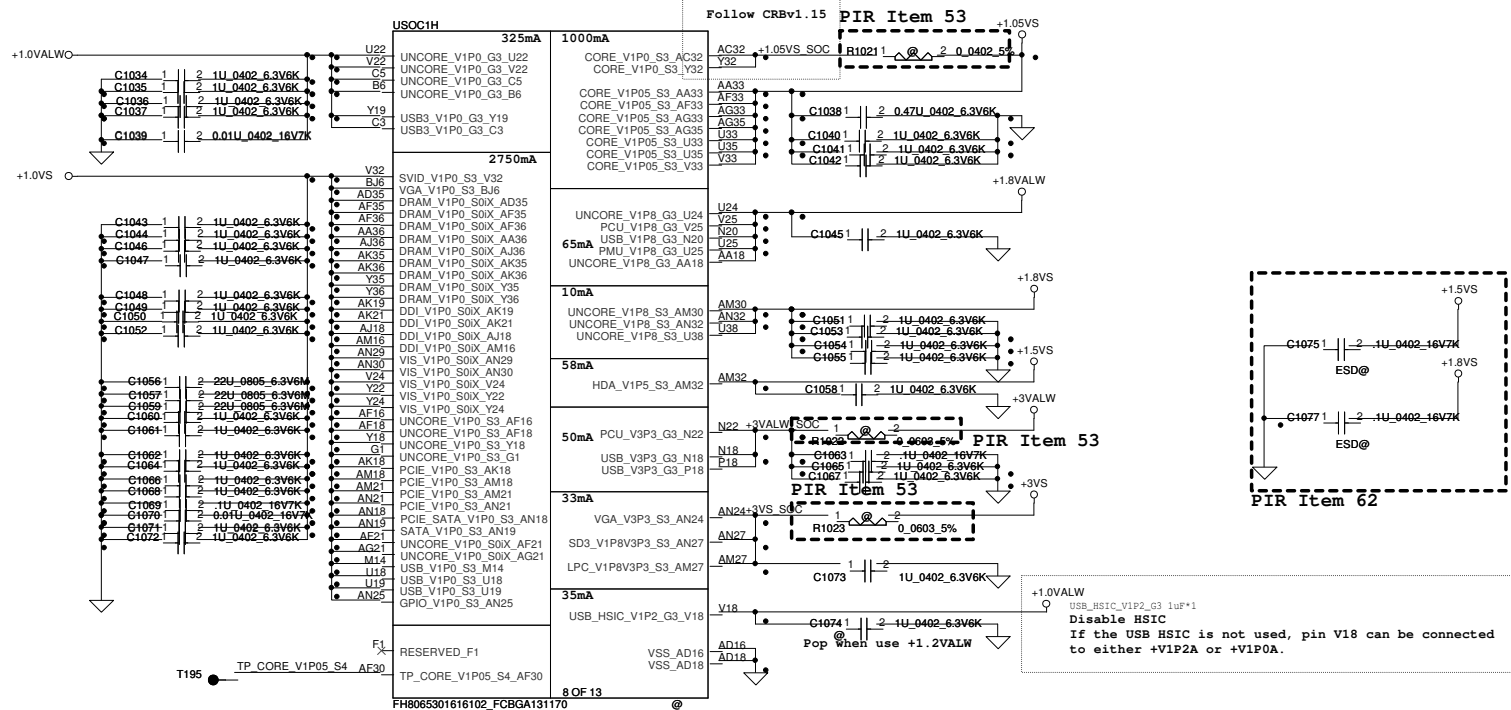
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Compal Electronics, Inc. VLV-M SOC USB/LPC/SMBus				Sheet 9 of 48

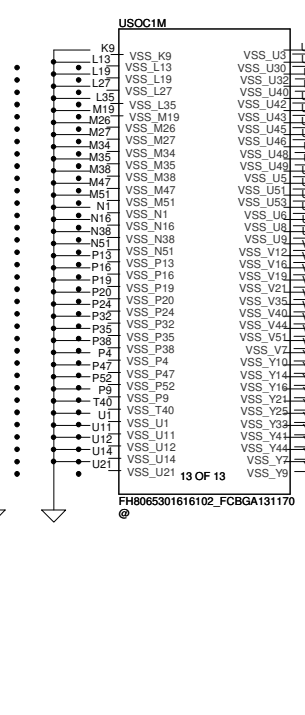
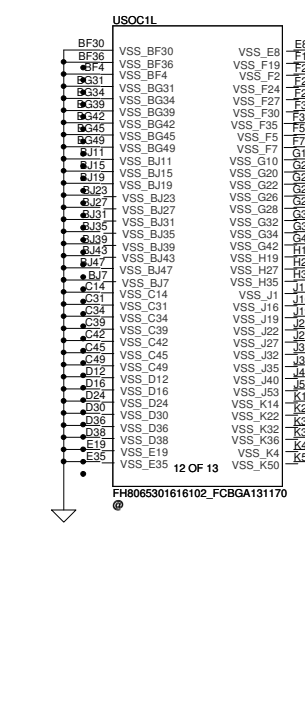
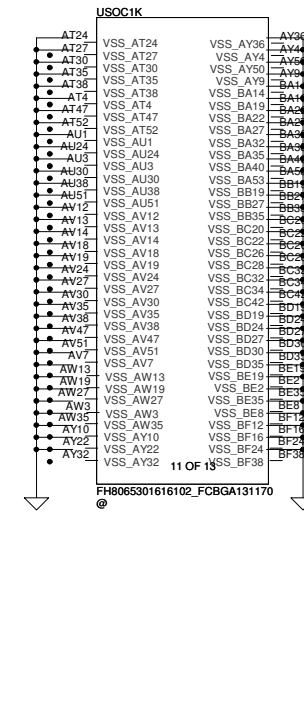
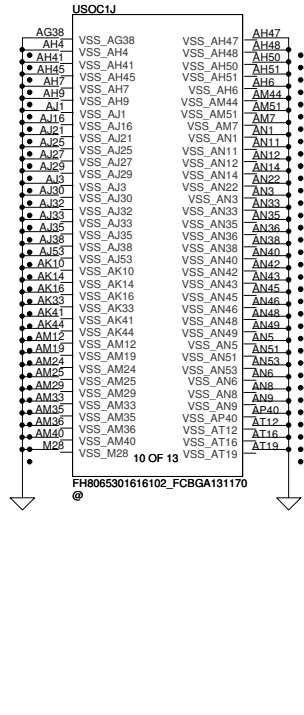
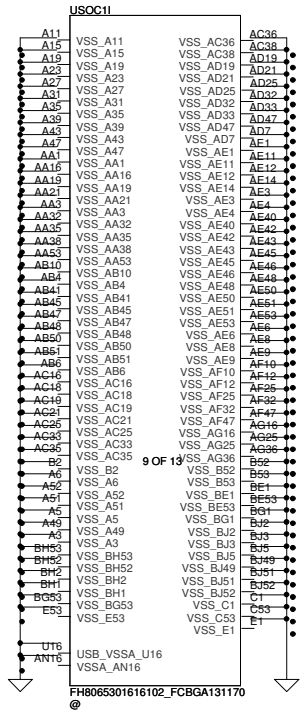


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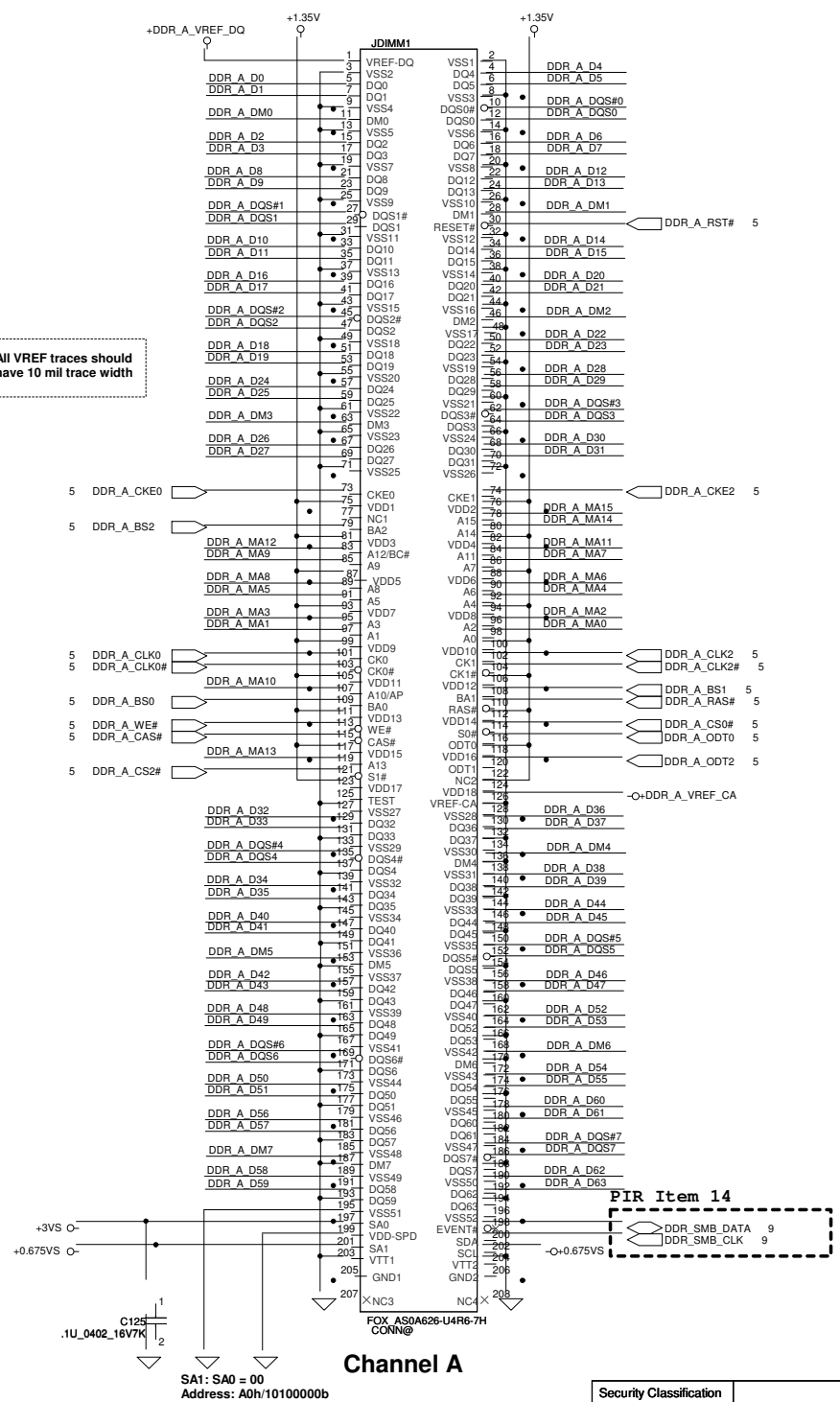


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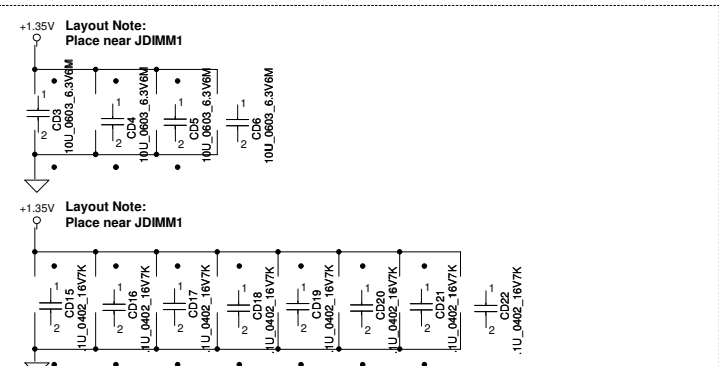
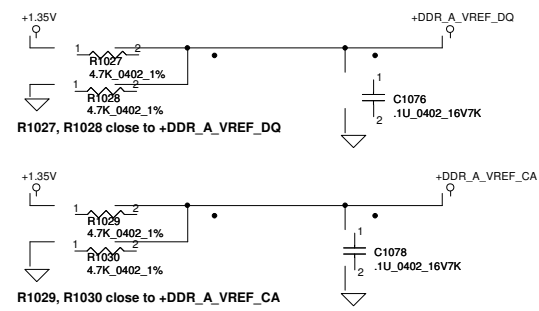


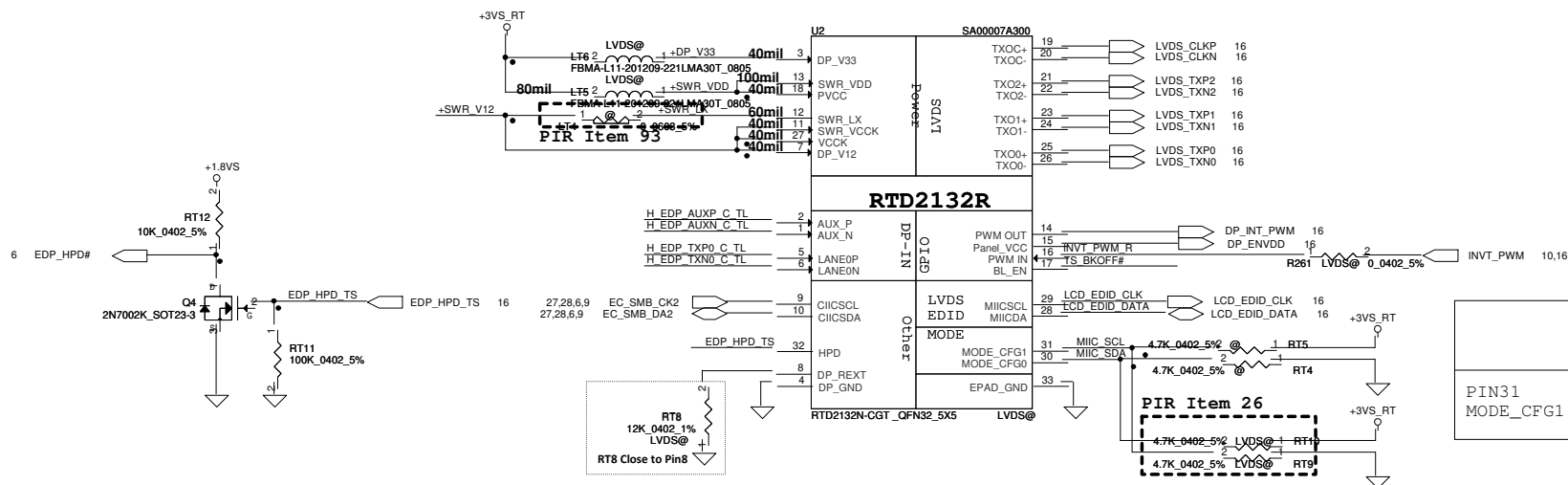
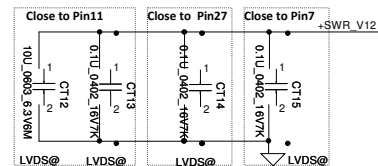
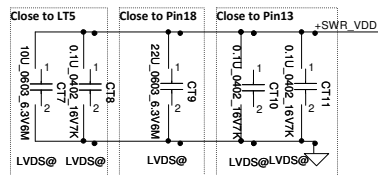
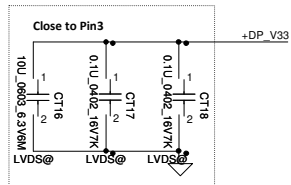
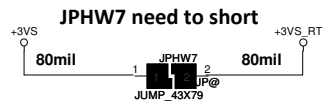
All VREF traces should have 10 mil trace width



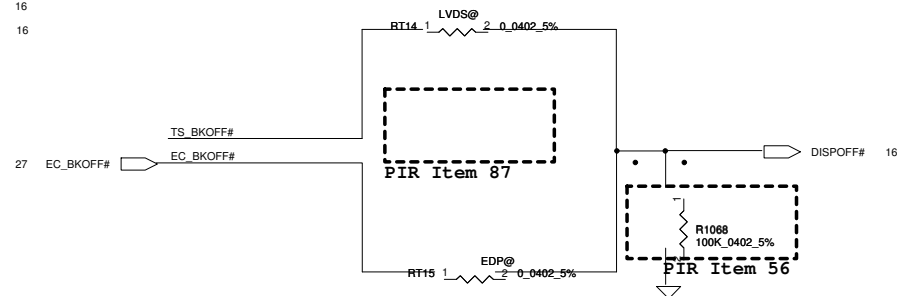
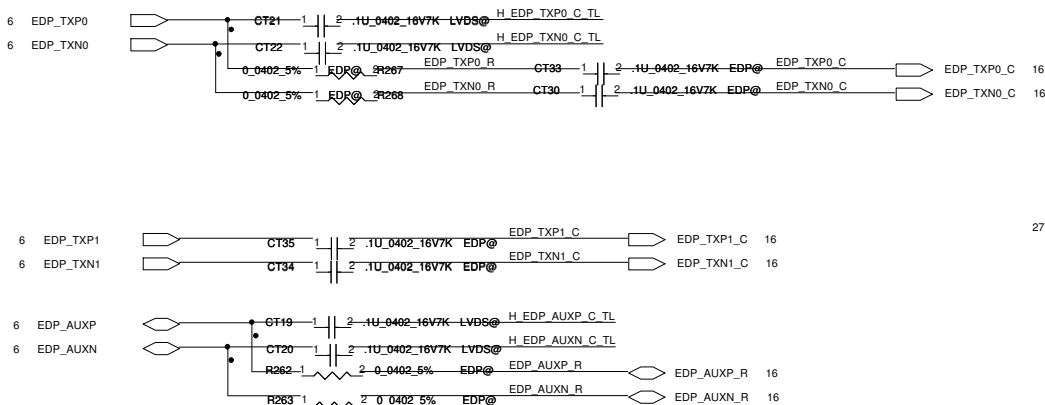
- DDR_A_DQS[0..7] 5
- DDR_A_DQS[0..7] 5
- DDR_A_D[0..63] 5
- DDR_A_MA[0..15] 5
- DDR_A_DM[0..7] 5

Signal voltage level = 0.675 V
PLACE TWO 4.7K RESISTORS CLOSE TO DIMMS ON DIMM_VREF_CA / DIMM_VREF_DQ
Decoupling caps are needed; one 0.1 uF placed close to VREF pins of each DDR3 SODIMM.

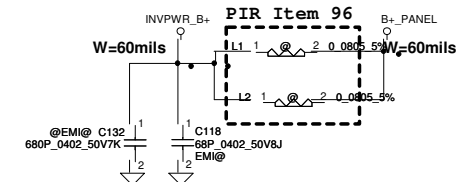
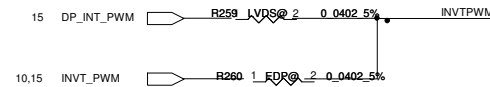
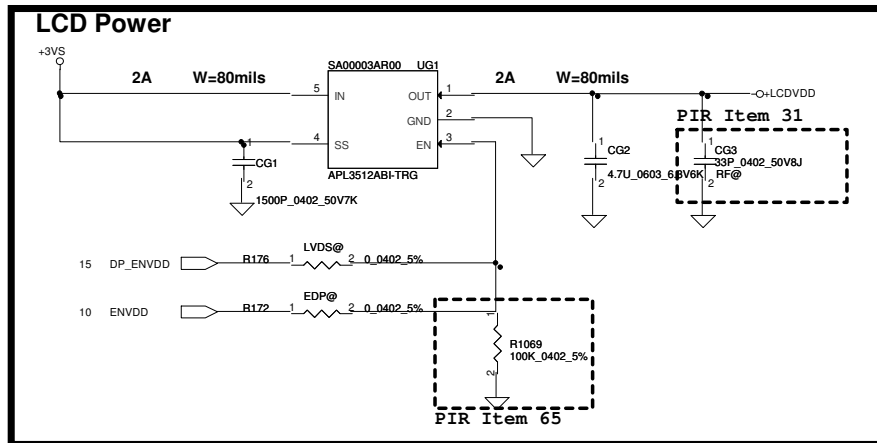




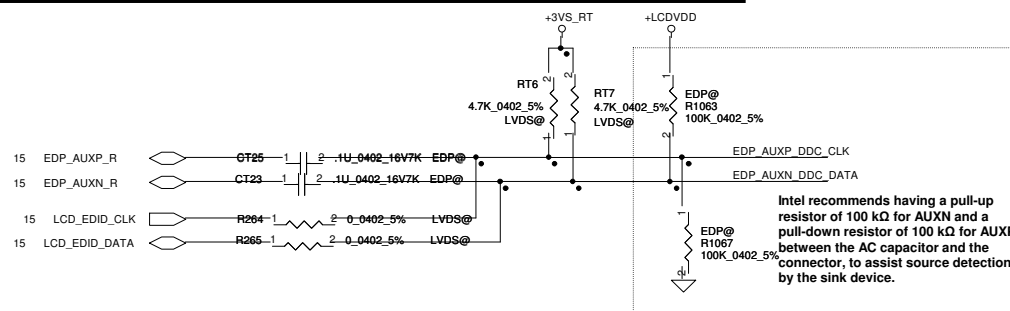
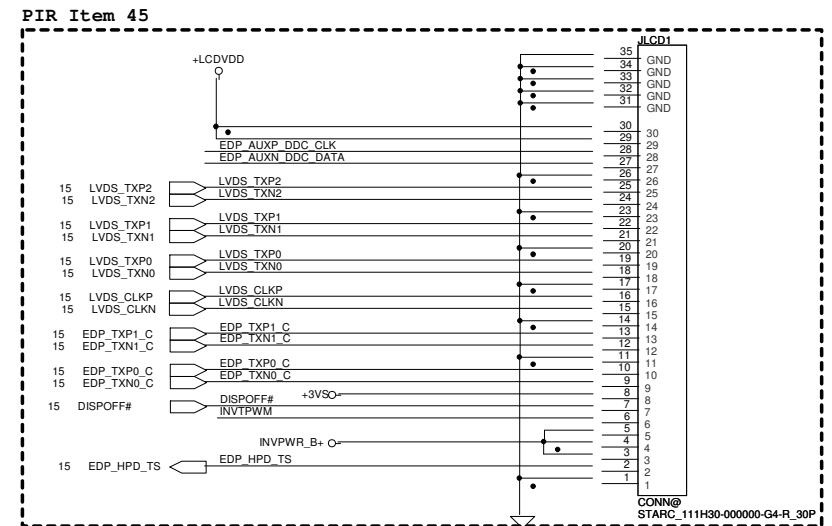
		PIN30 MODE_CFG0	
		0	1
PIN31 MODE_CFG1	0	X	EP Mode
	1	ROM	EEPROM



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LCD PANEL Conn.



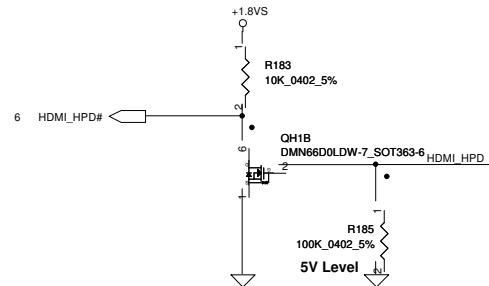
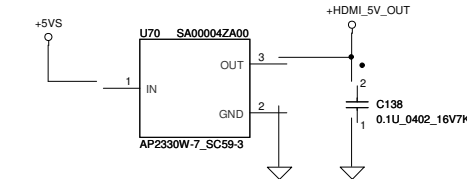
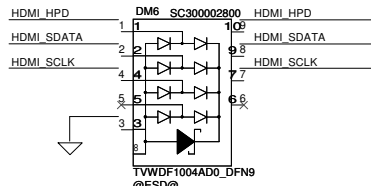
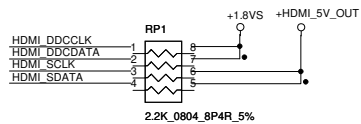
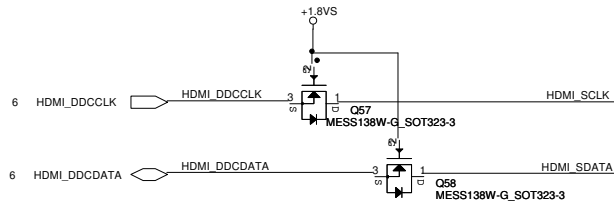
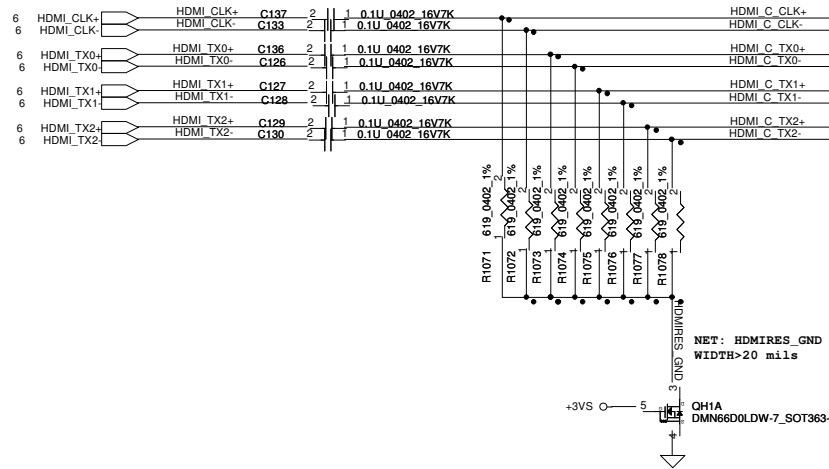
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/01/14	Deciphered Date	2015/01/14	Title
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CLK

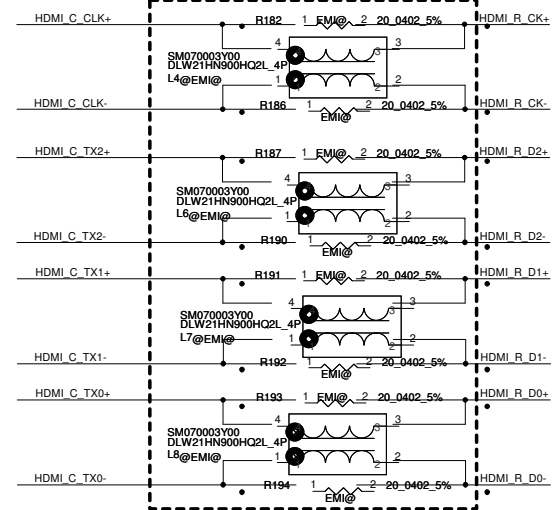
Data0

Data1

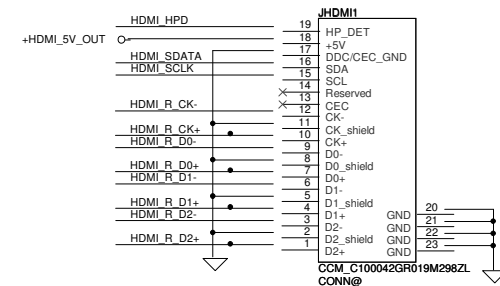
Data2



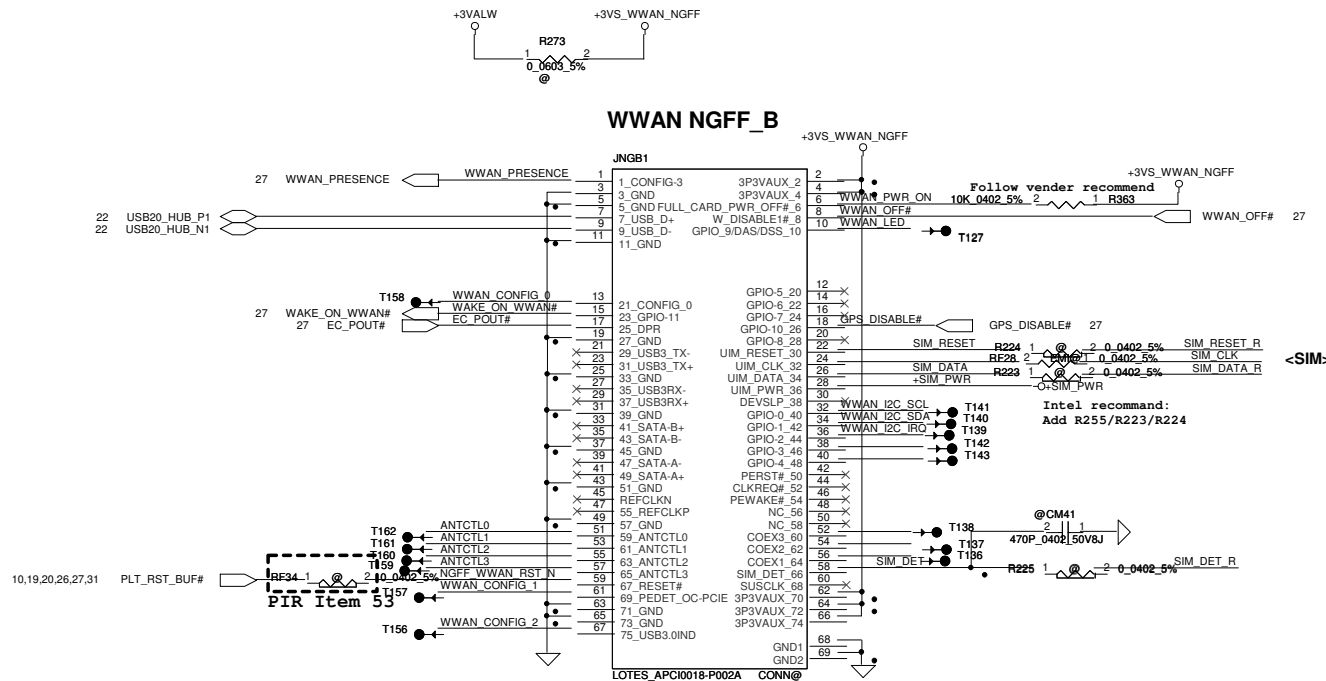
PIR Item 98



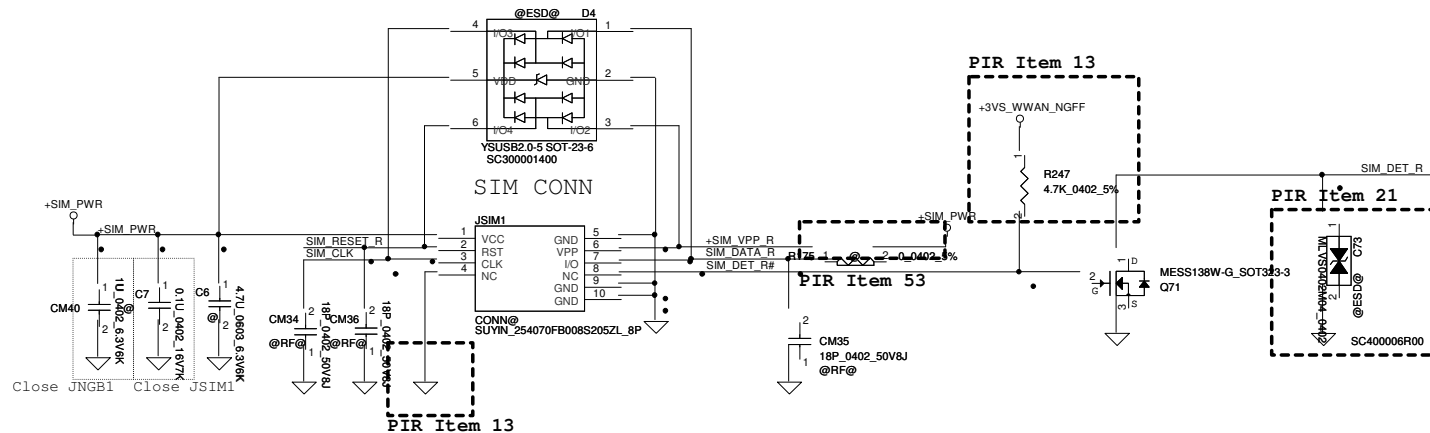
HDMI Conn.



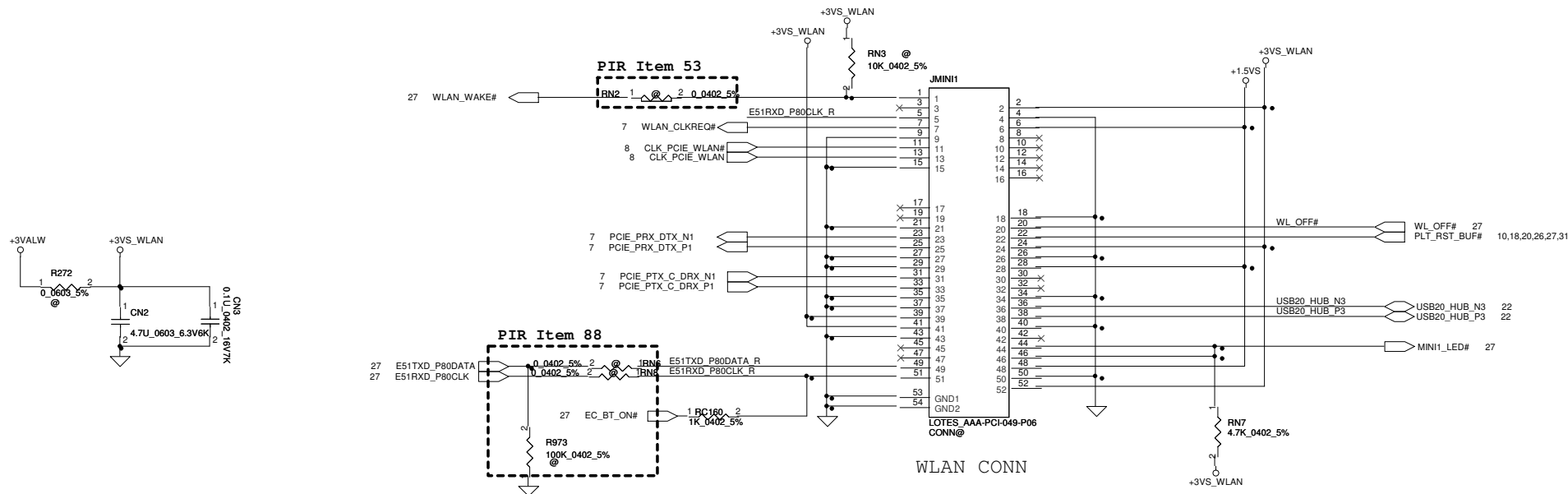
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/01/14	Deciphered Date	2015/01/14	Title
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Customer				Document Number
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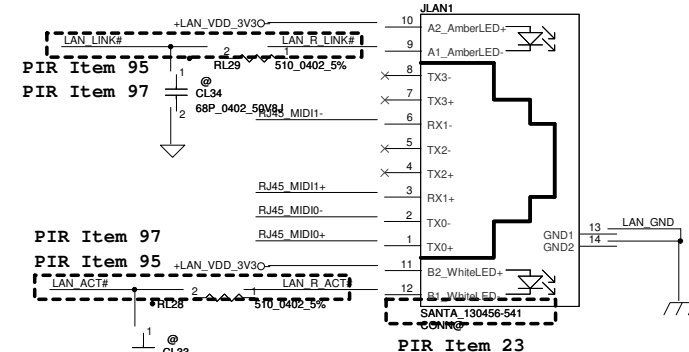
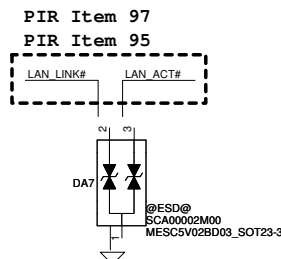
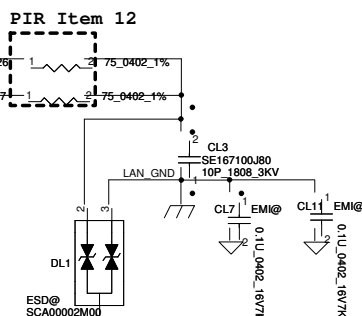
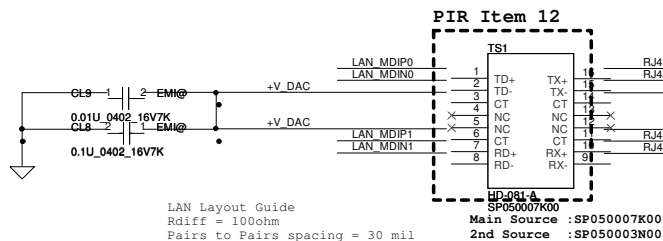
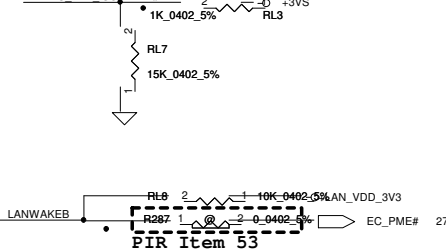
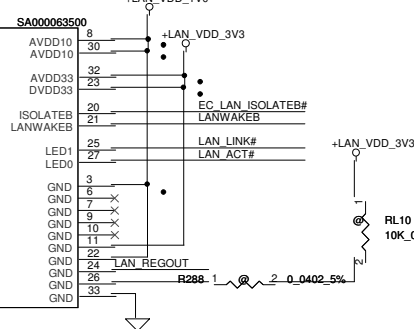
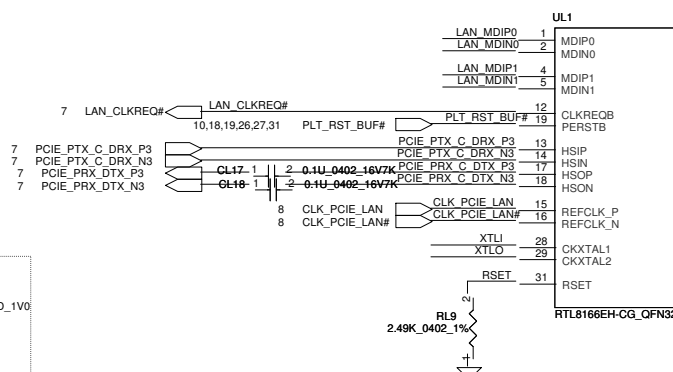
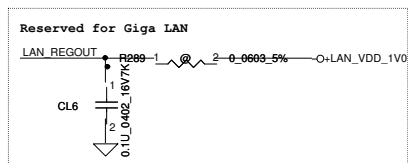
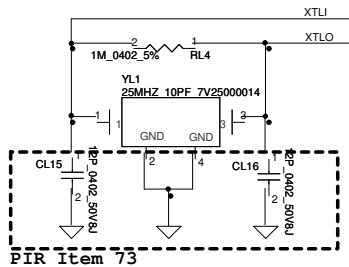
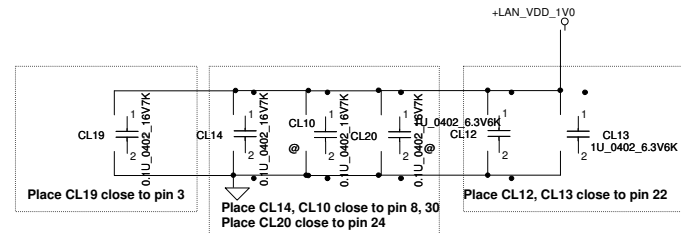
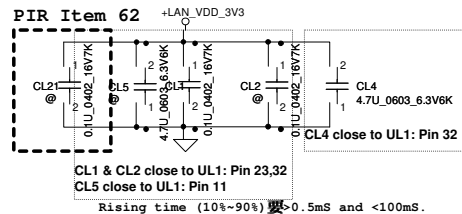
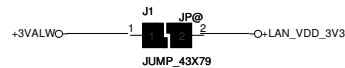
WWAN_PWREN_EC	WWAN_OFF#/GPS_DISABLE#
H: WWAN powers on.	H: WWAN function enabled by software
L: WWAN powers off.	L: WWAN function turned off by software
POUT	SIM_DET
H: No TX power backoff	H: SIM is present
L: TX power backoff.	L: SIM is absent



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				LA-B151P	1.0
				Date	Rev
				Tuesday, January 21, 2014	1.0
				Sheet	19 of 48

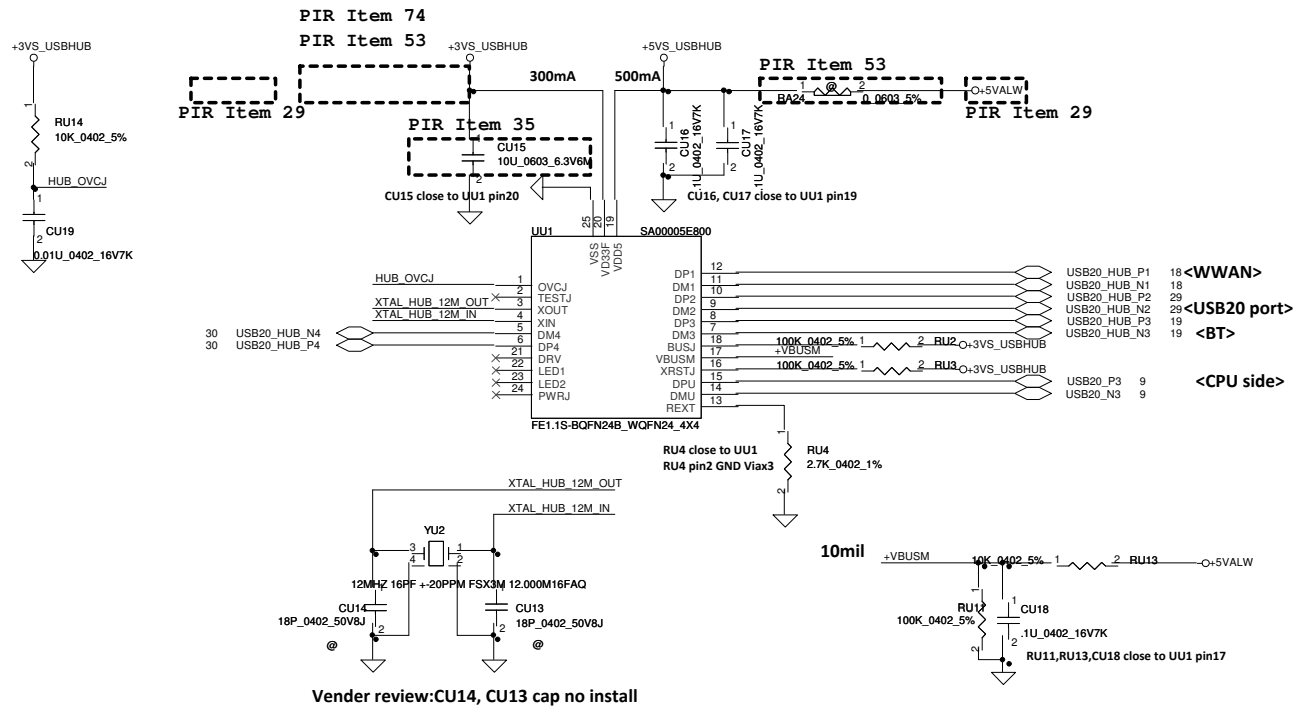


LAN Connector

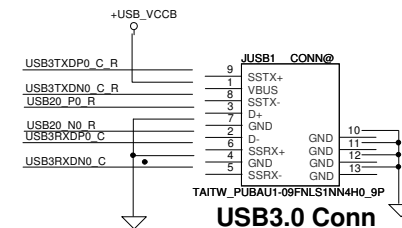
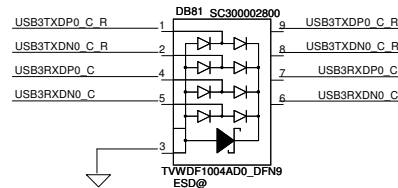
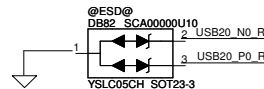
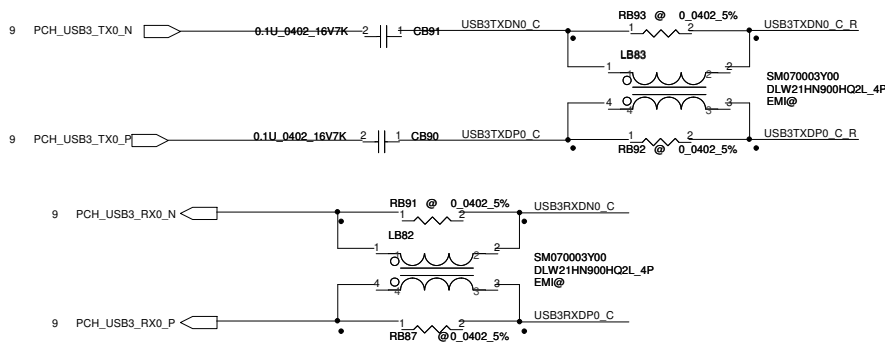
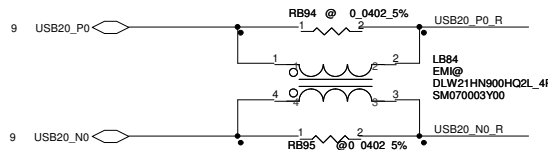
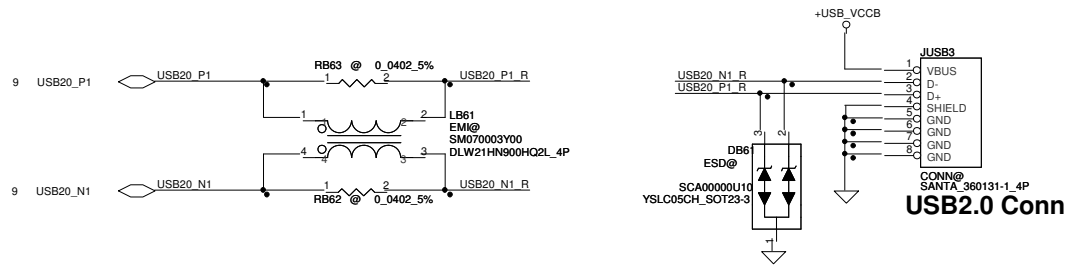
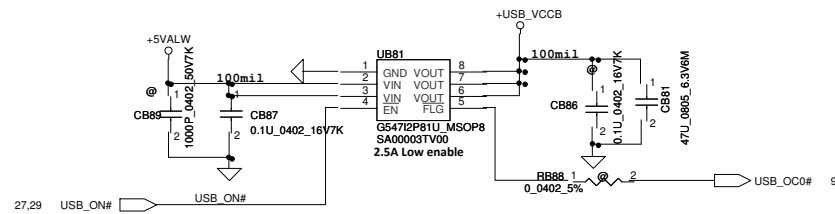
LAN Layout Guide
Rdiff = 100ohm
Pairs to Pairs spacing = 30 mil

Main Source : SP050007K00
2nd Source : SP050003N00

Security Classification	Compal Secret Data		Title	
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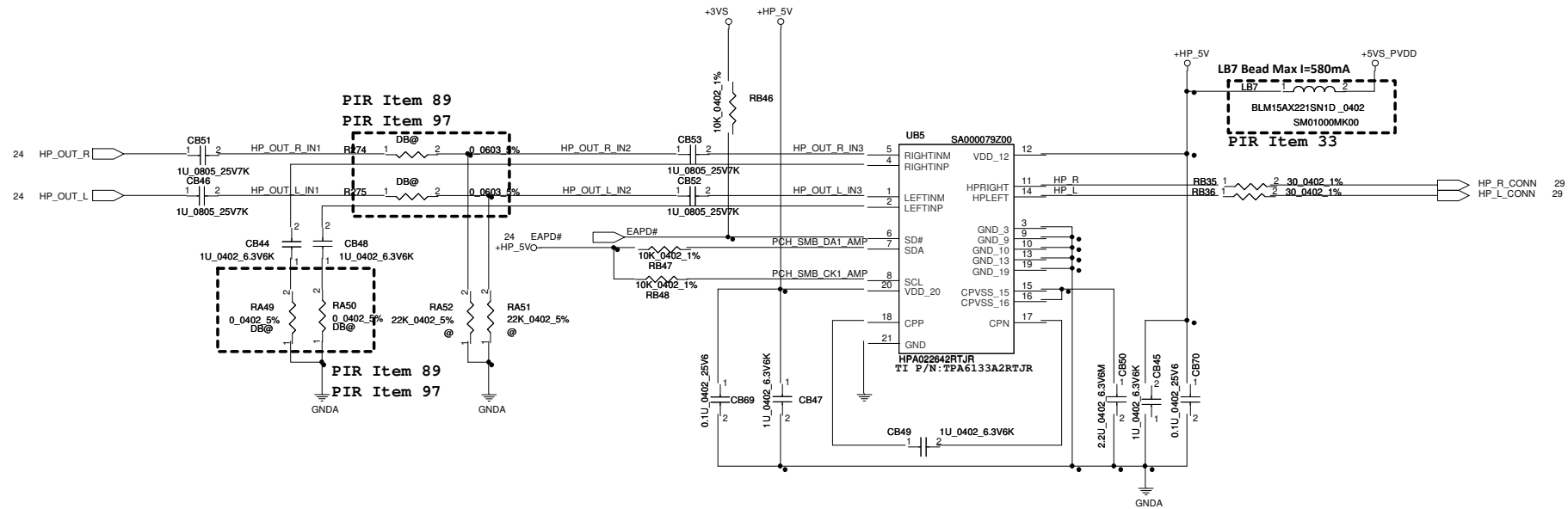


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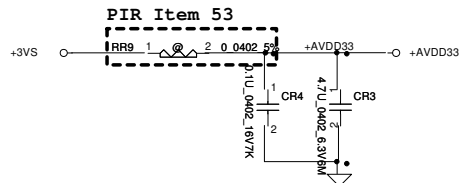
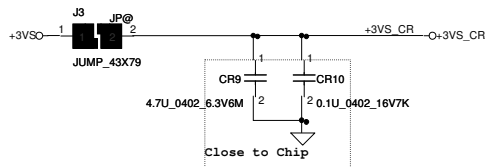


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				Document Number	Rev
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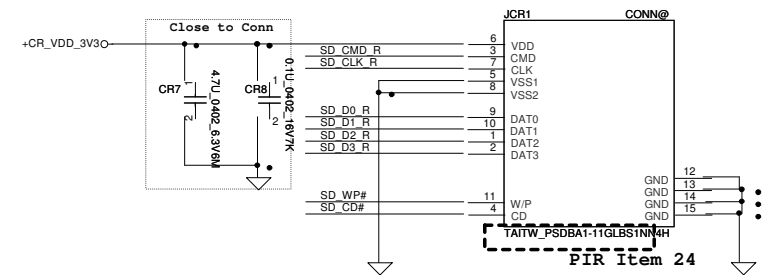
PIR Item 41: Modify circuit for baets



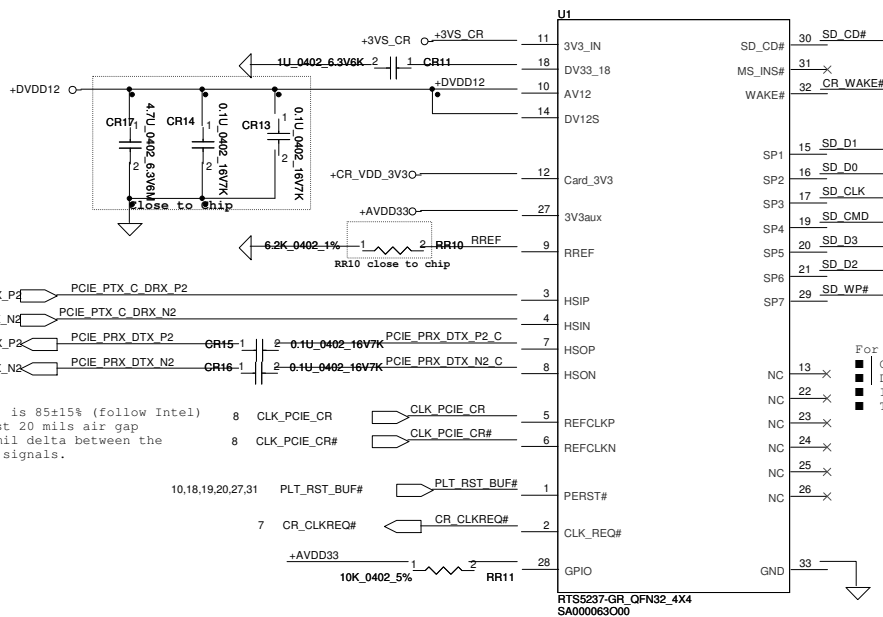
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/01/14	Deciphered Date	2015/01/14	Title	Audio HP Amp
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Card Reader Connector



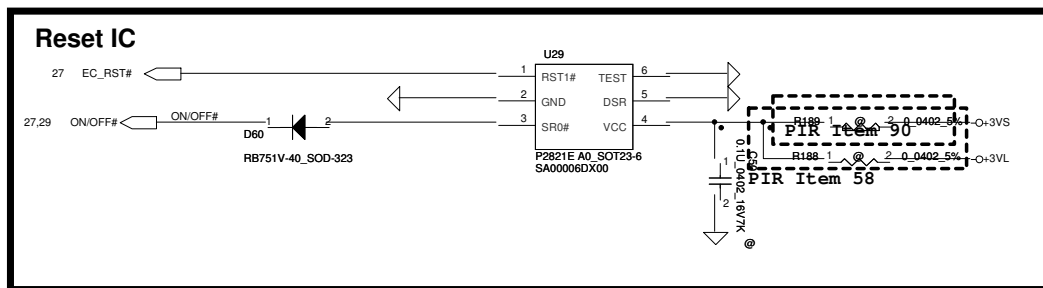
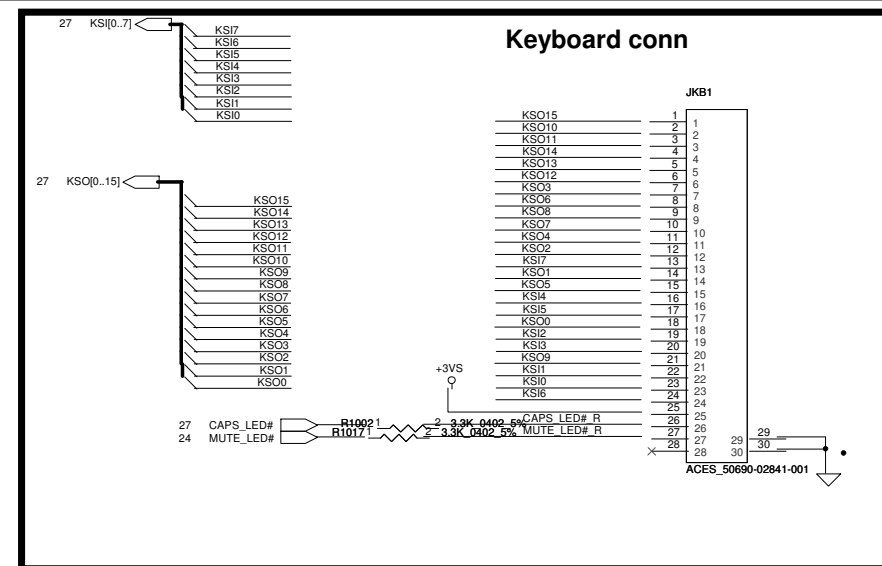
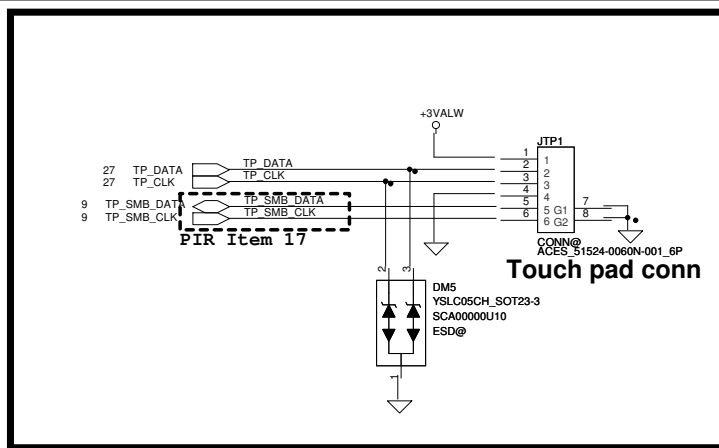
- Complete D3V3 power plane partition under RTS5227 chip and Socket in Power Layer
- Pin 11(3V3_IN) / pin 12 (CARD_3V3) trace width is 40 mils (minimum).
- Pin 27(3V3aux) trace width is 30 mils (minimum).
- Pin 10(AV12), pin 14(DV12S), pin 18 (DV33_18) trace width is 20 mils (minimum).
- Pin 9 (RREF) trace width is 12 mils (minimum).



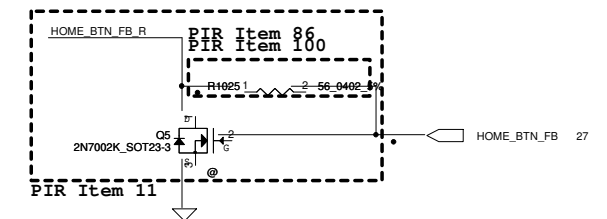
- For pin3 to pin8 :
1. impedance(Zdiff) is 85±15% (follow Intel)
 2. Maintain at least 20 mils air gap
 3. No more than 5-mil delta between the lengths of the two signals.

- For pin15 to pin21 :
- CLK - DATA | trace length ≤ 100 mils
 - DATA.x - DATA.y | trace length ≤ 100 mils
 - It is recommended that use a guard ground to isolate SD_CLK trace
 - These traces of characteristic impedance are 50±15%.

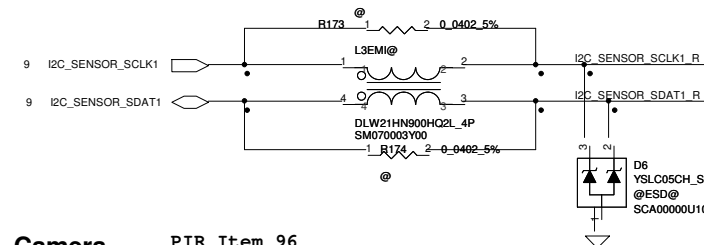
	Protect Contact		Detect Contact
	Disable	Enable	
Card Uninsertion	Open	Open	Open
Card Insertion	Close	Open	Close



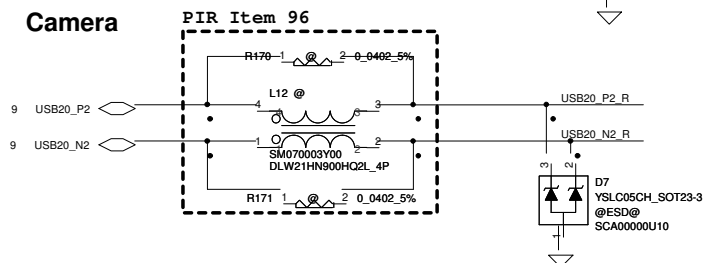
PIR Item 44
PIR Item 78



Touch Screen

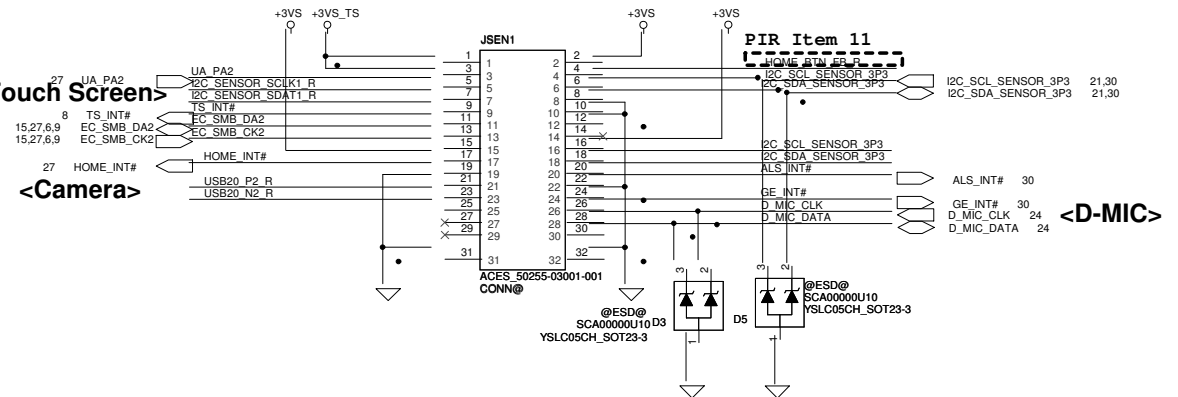


Camera



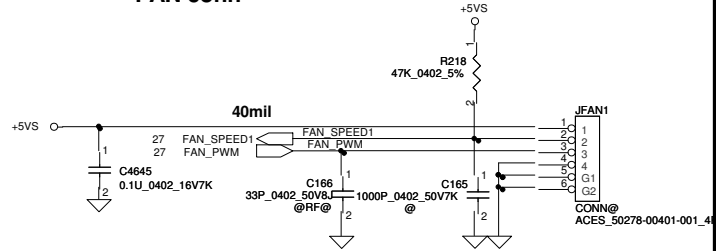
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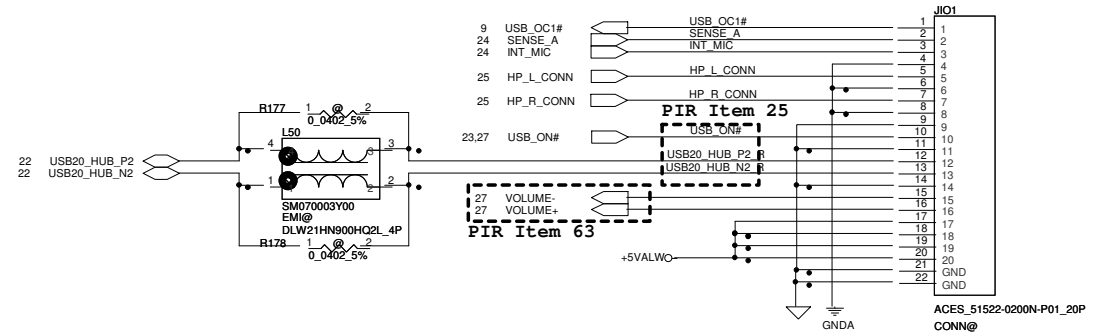


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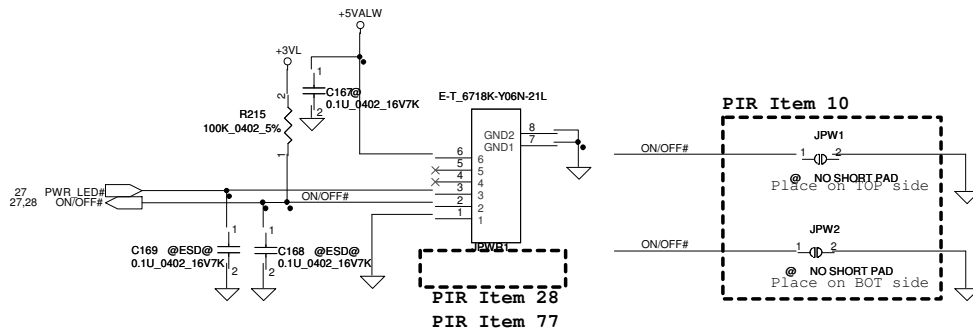
FAN conn



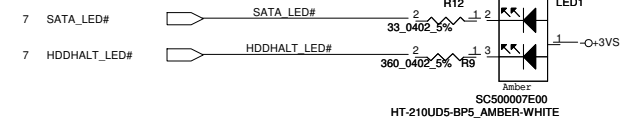
Audio Jack/USB IO Connector



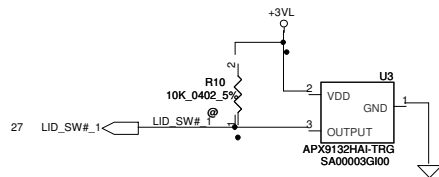
Power Button Conn



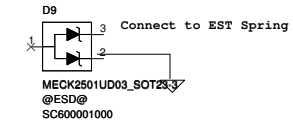
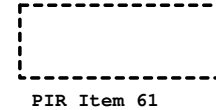
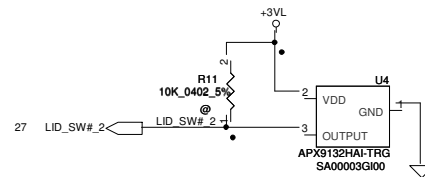
LED



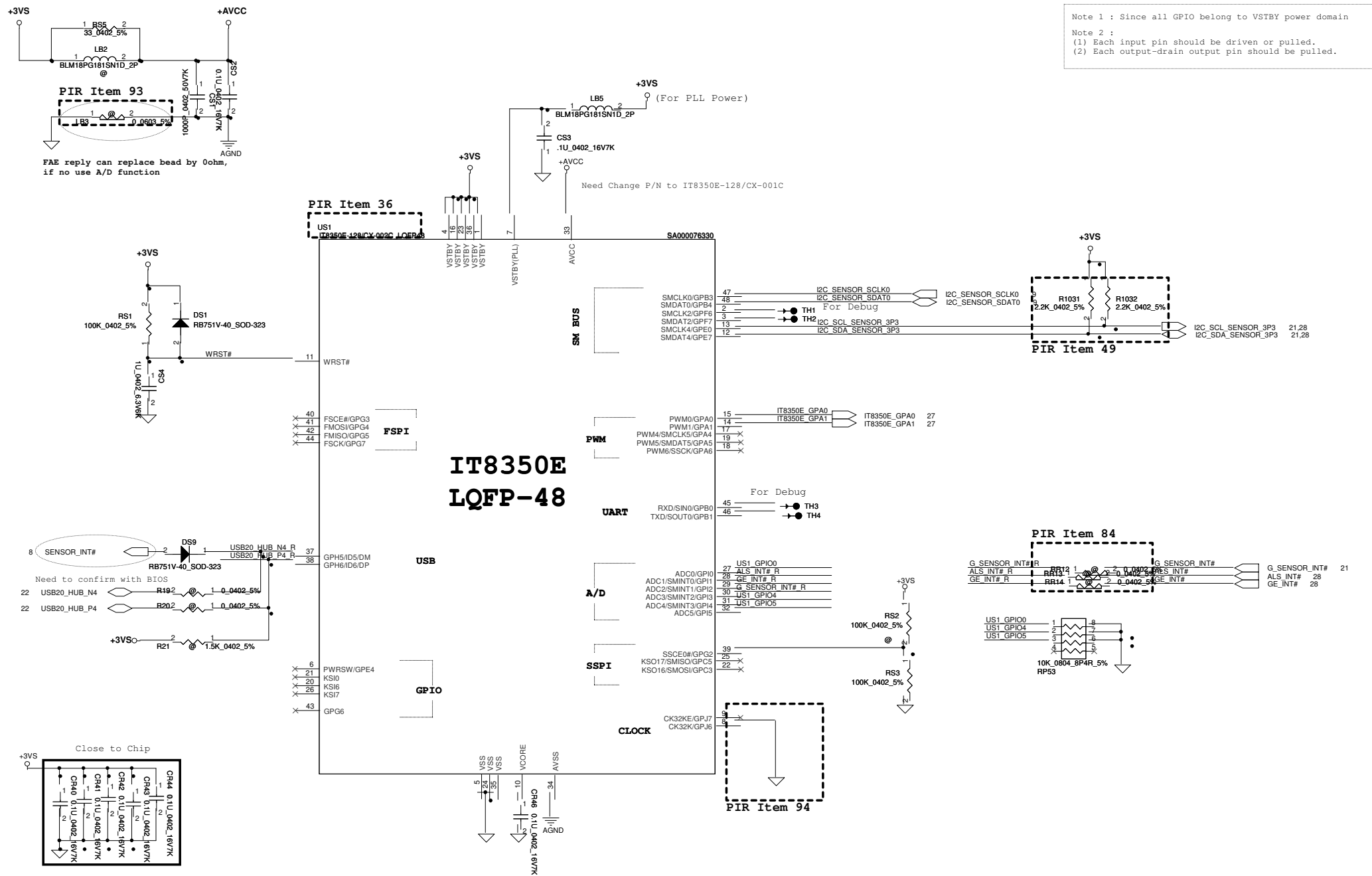
LID Switch(BOT)



LID Switch(TOP)

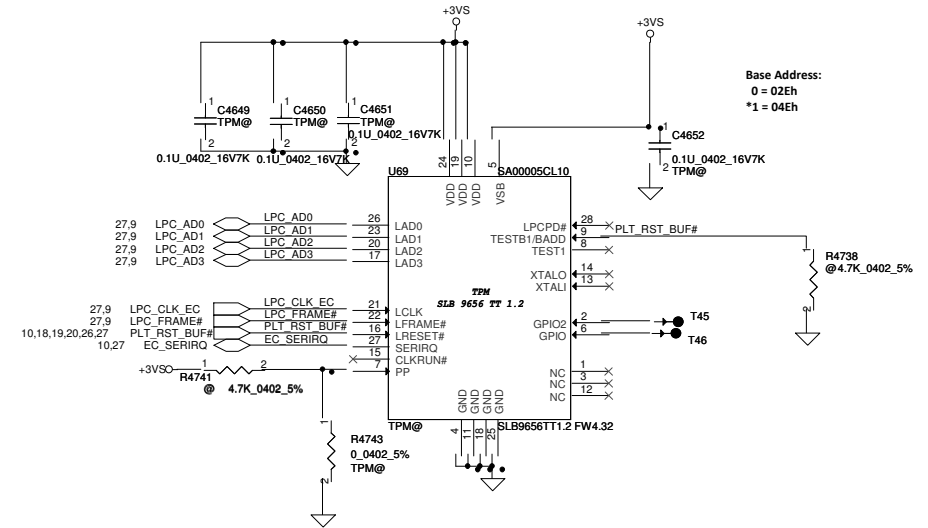


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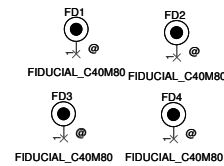
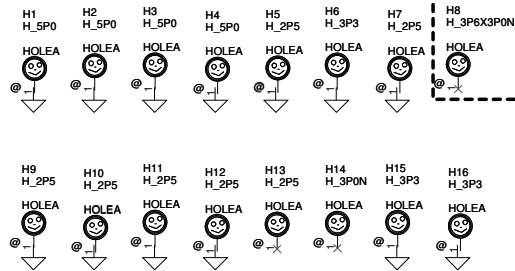
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		Deciphered Date		Sensro Hub-IT8350E-128-BX	
2014/01/14		2015/01/14		Title	
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TPM1.2 PIR43: Remove co-layout circuit of SLB9635TT1.2

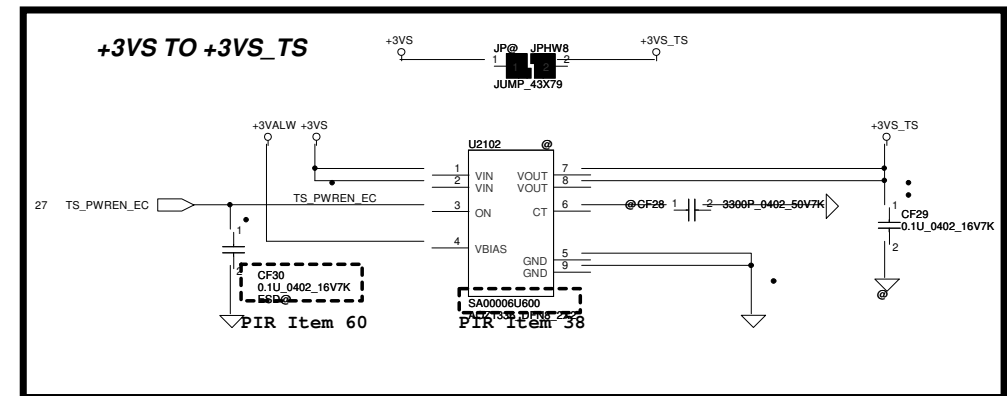
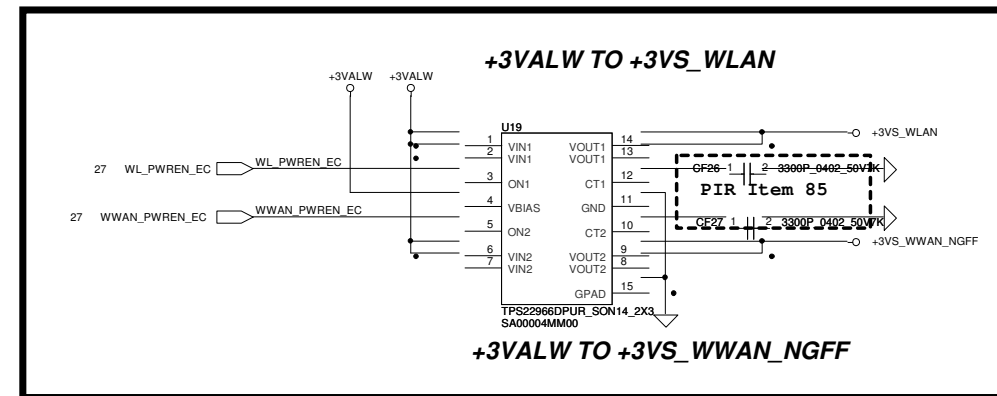
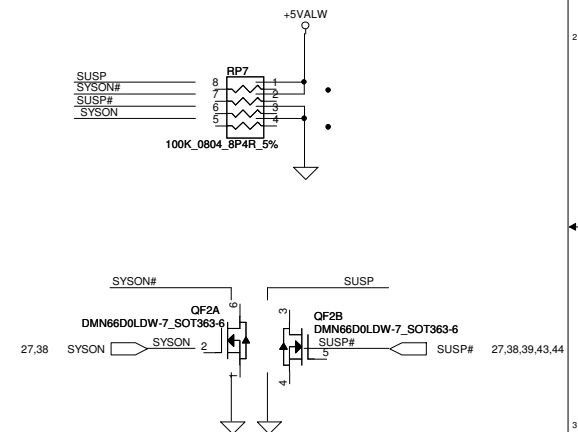
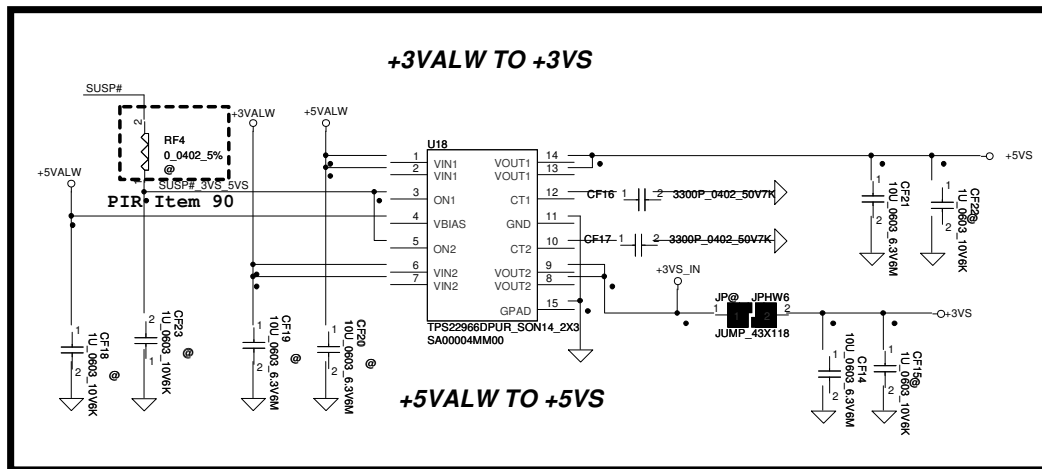
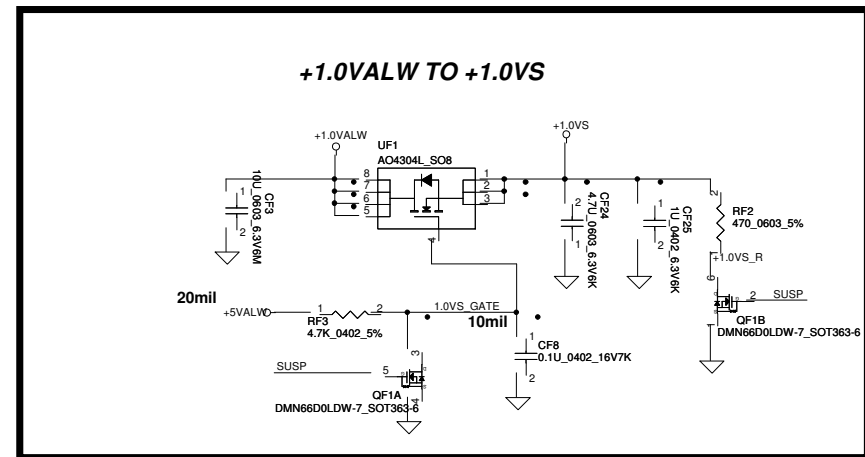
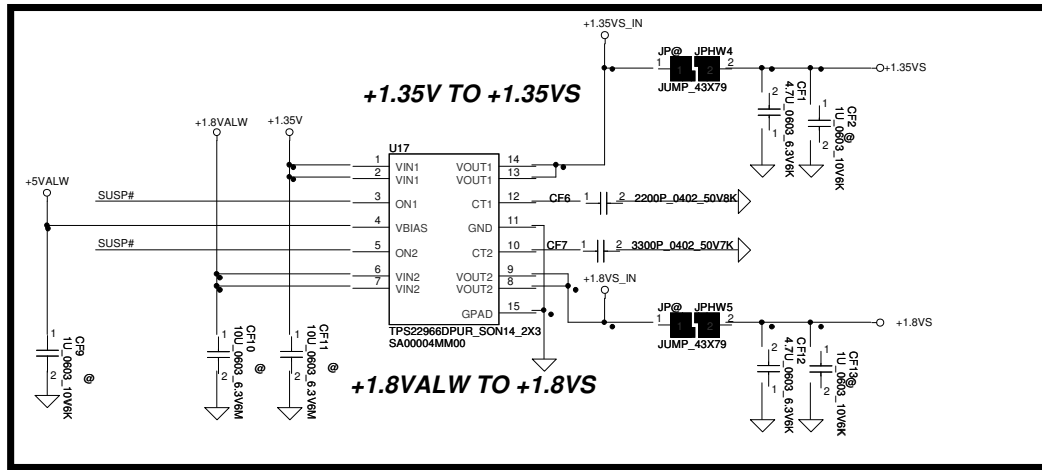


Base Address:
0 = 02Eh
*1 = 04Eh

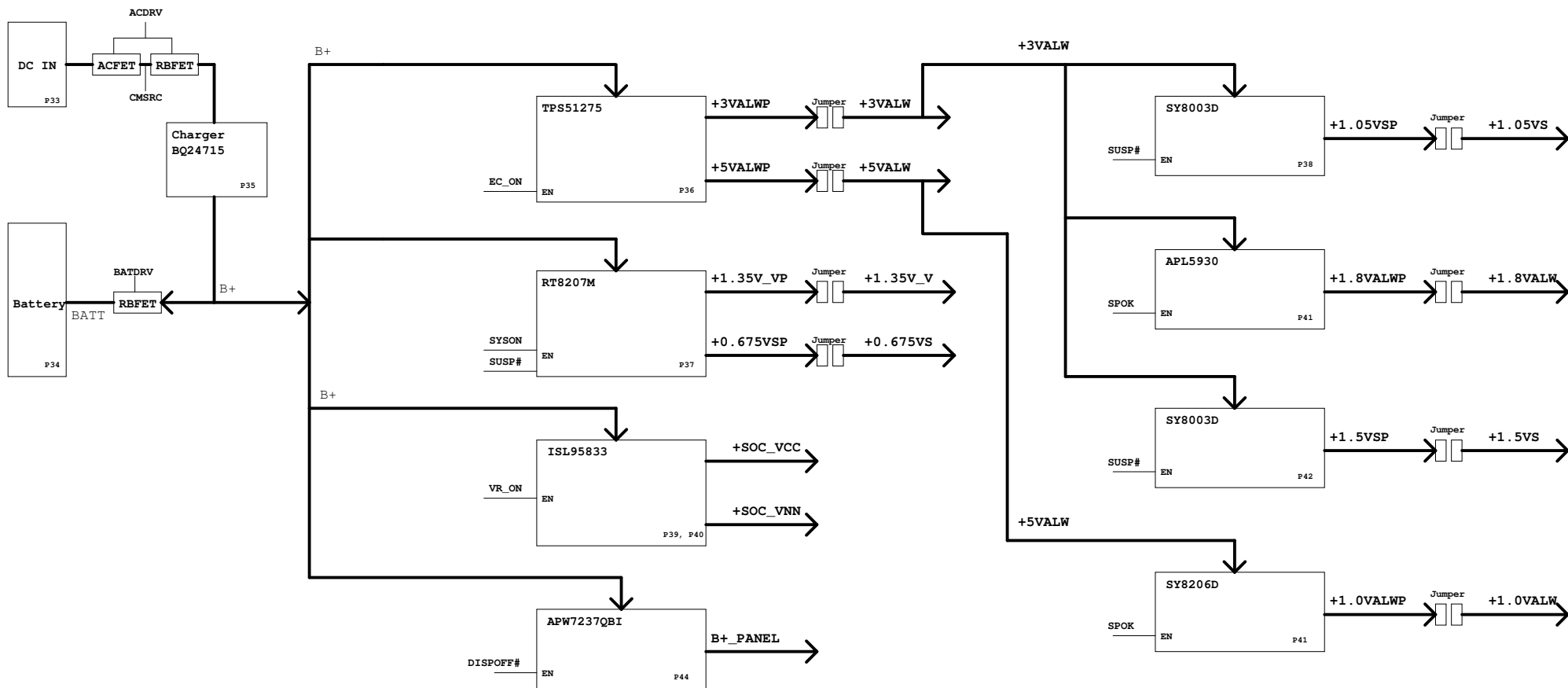
PIR Item 54



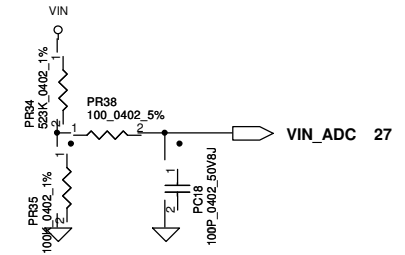
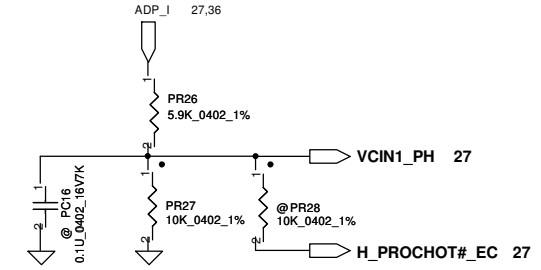
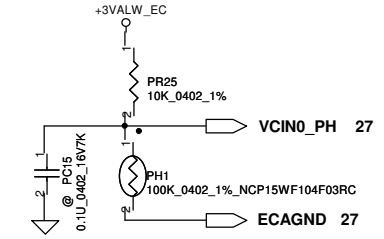
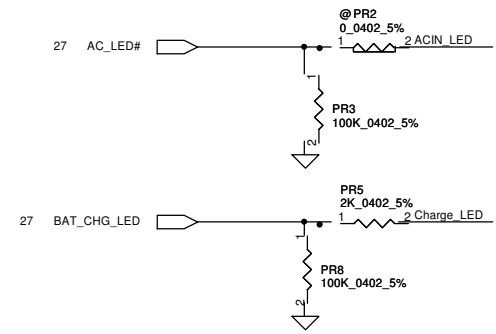
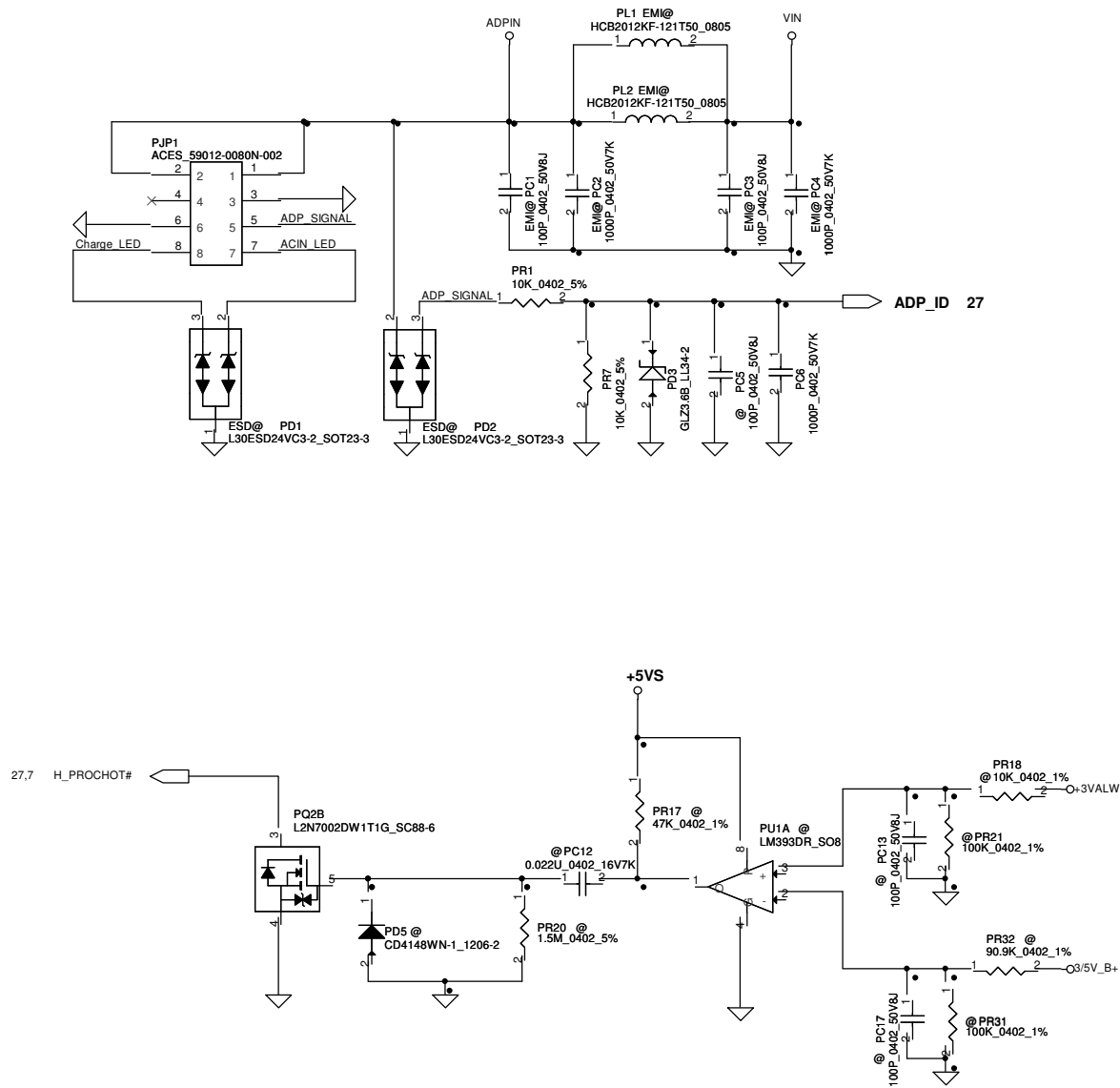
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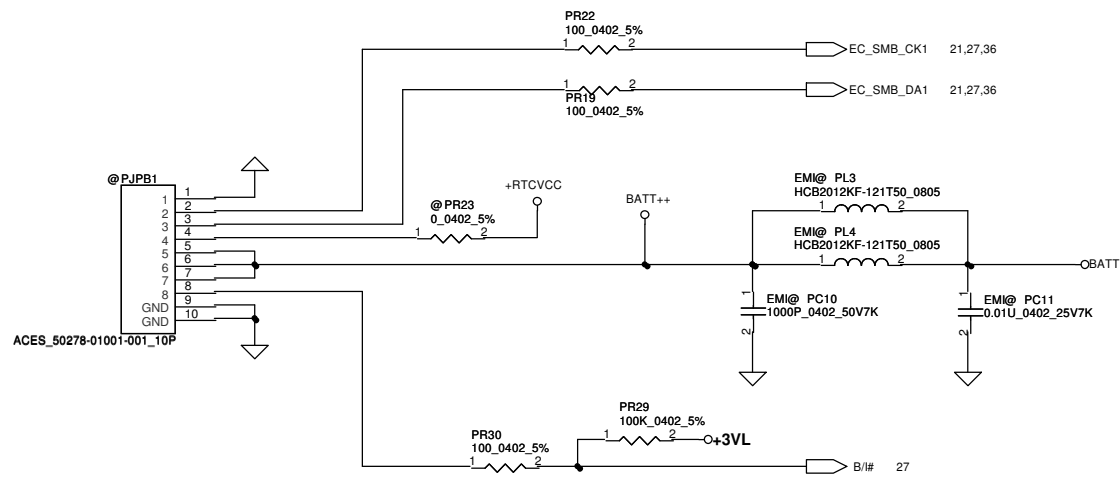
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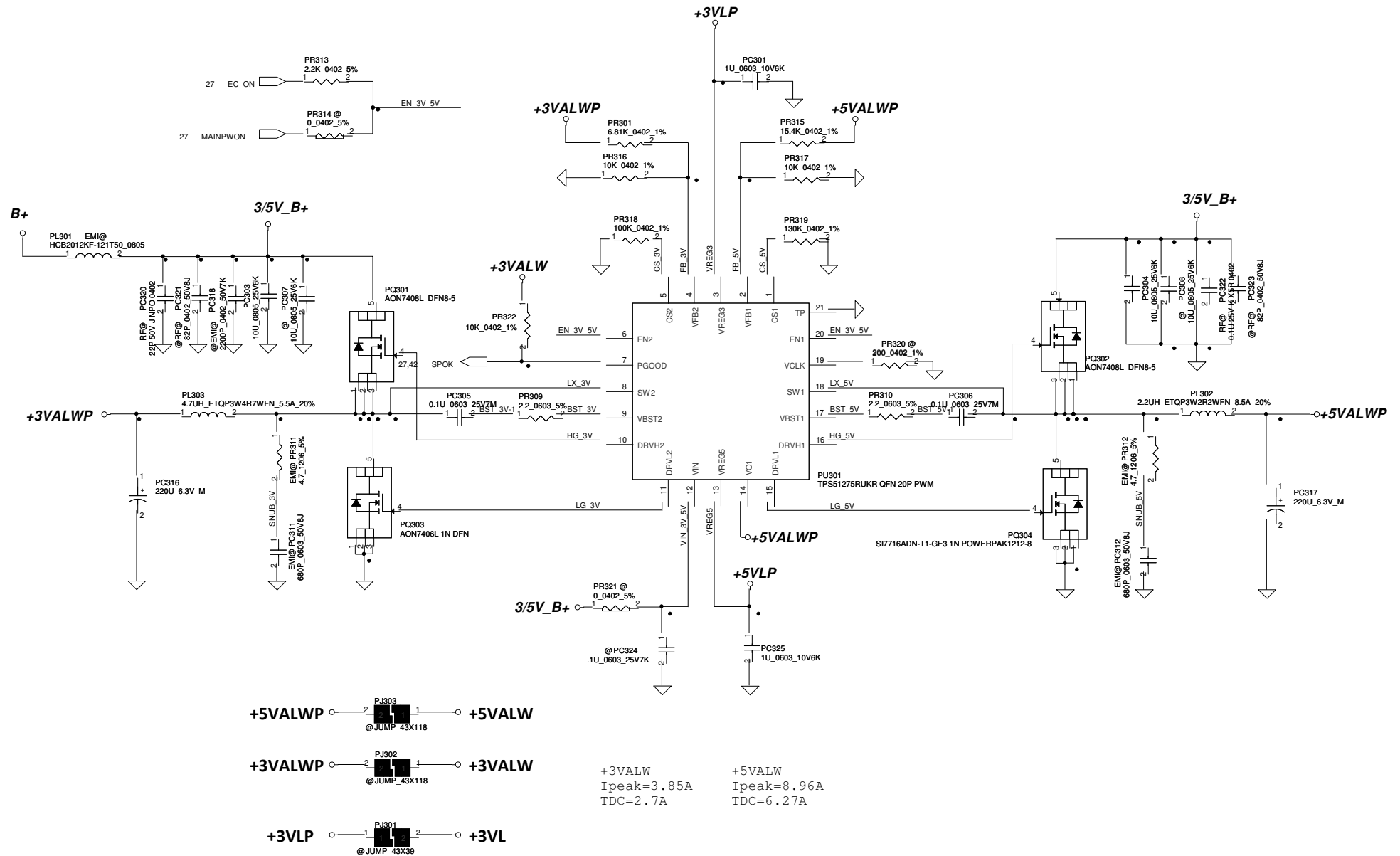
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/01/14	Deciphered Date	2015/01/14	Title	Power Block Diagram
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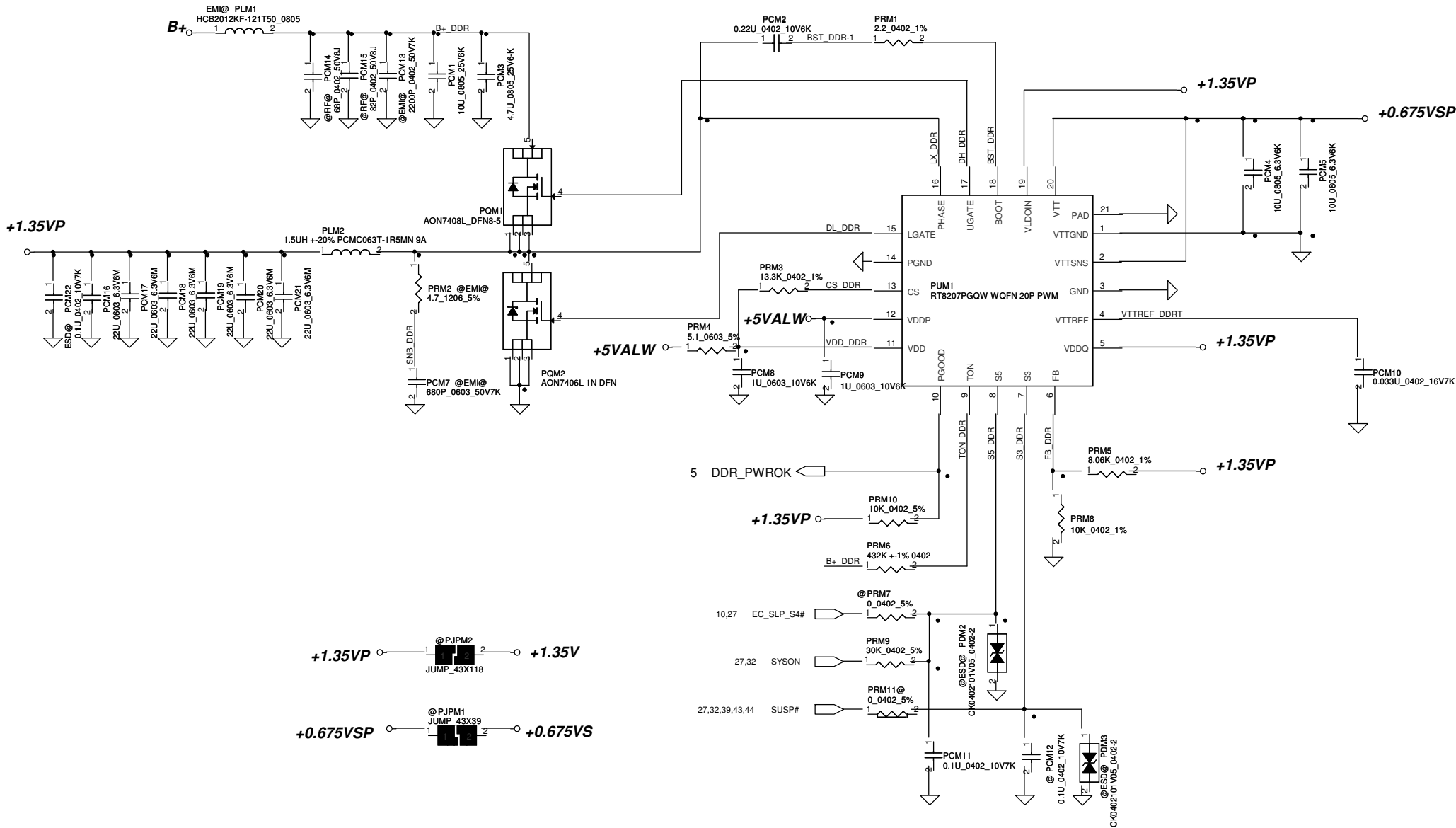


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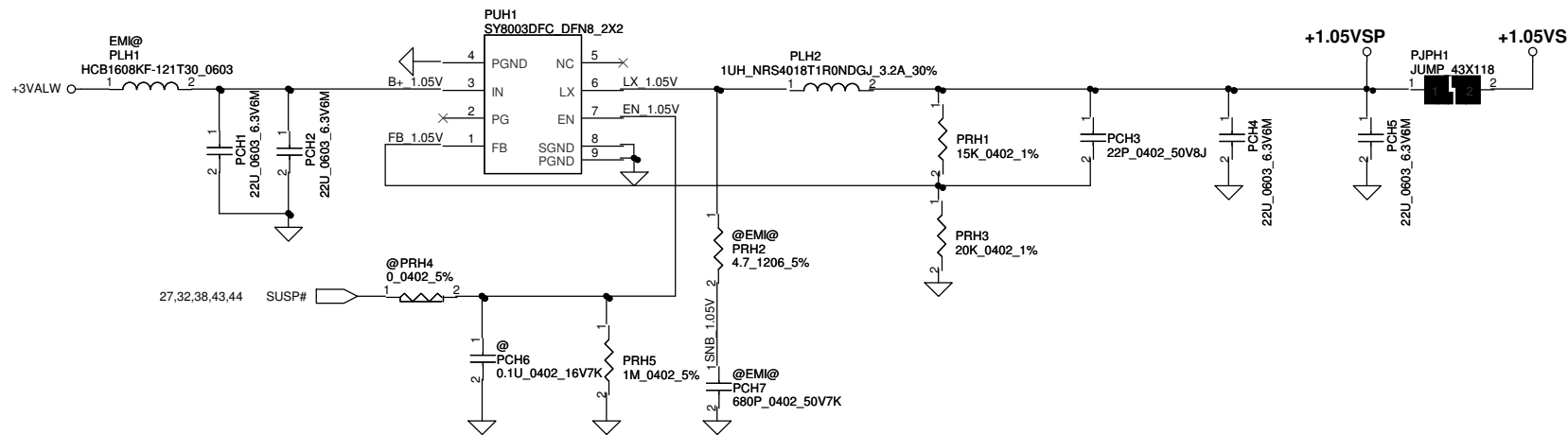


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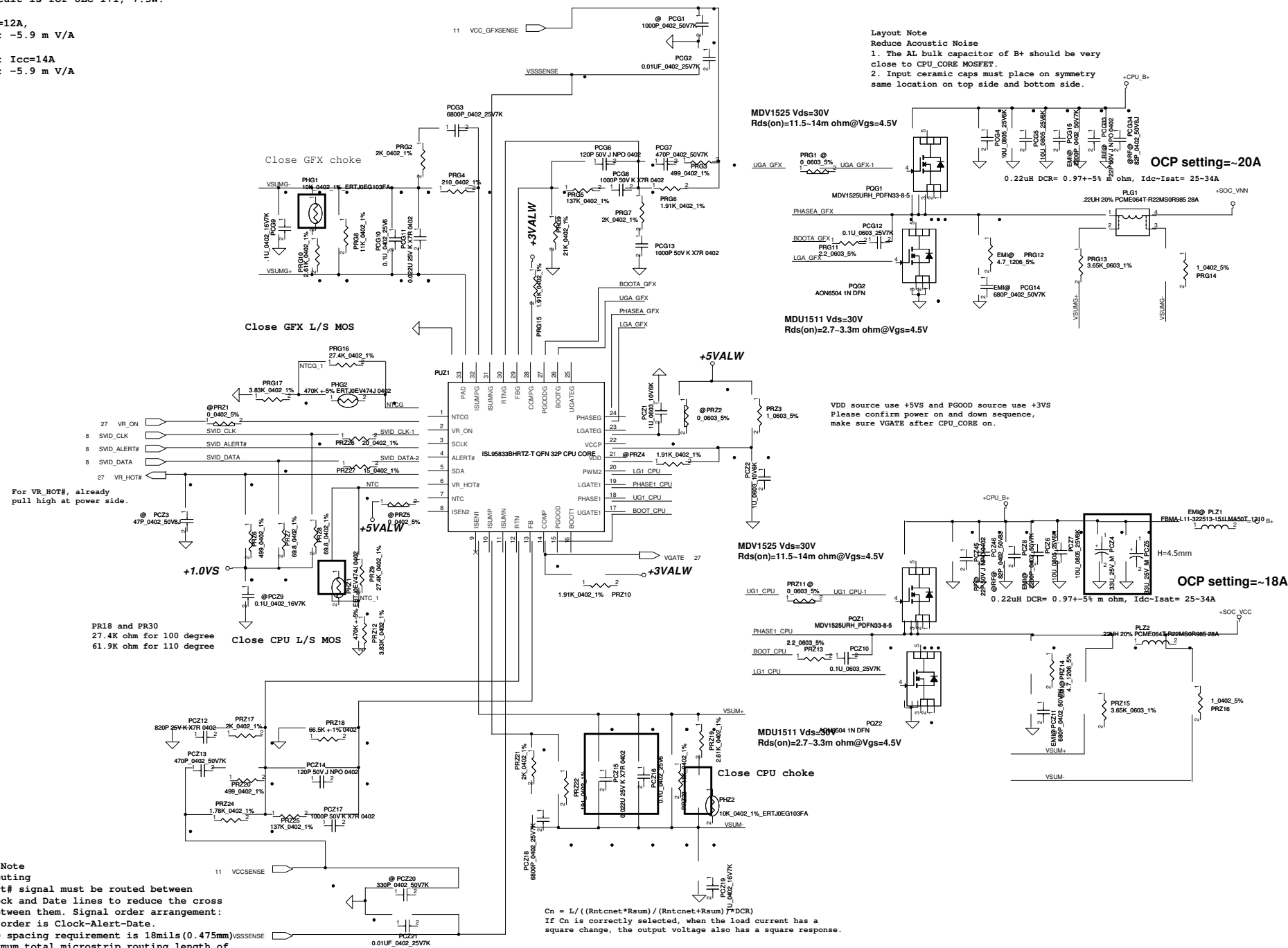
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/01/14	Deciphered Date	2015/01/14	Title	1.35V/0.675VS
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This circuit is for ULC 1+1, 7.5W.

GFX (GT2): $I_{cc}=14A$
Loadline: -5.9 m V/A



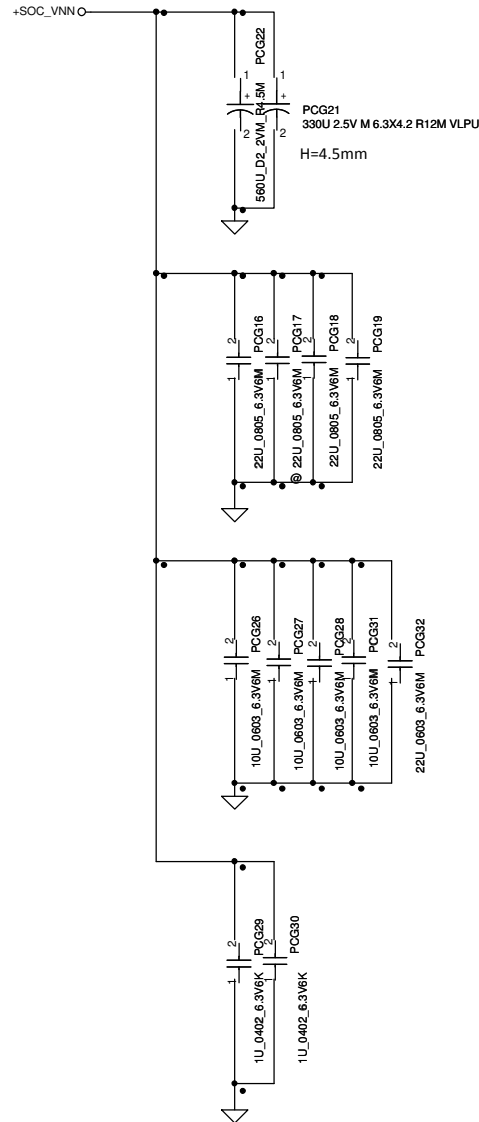
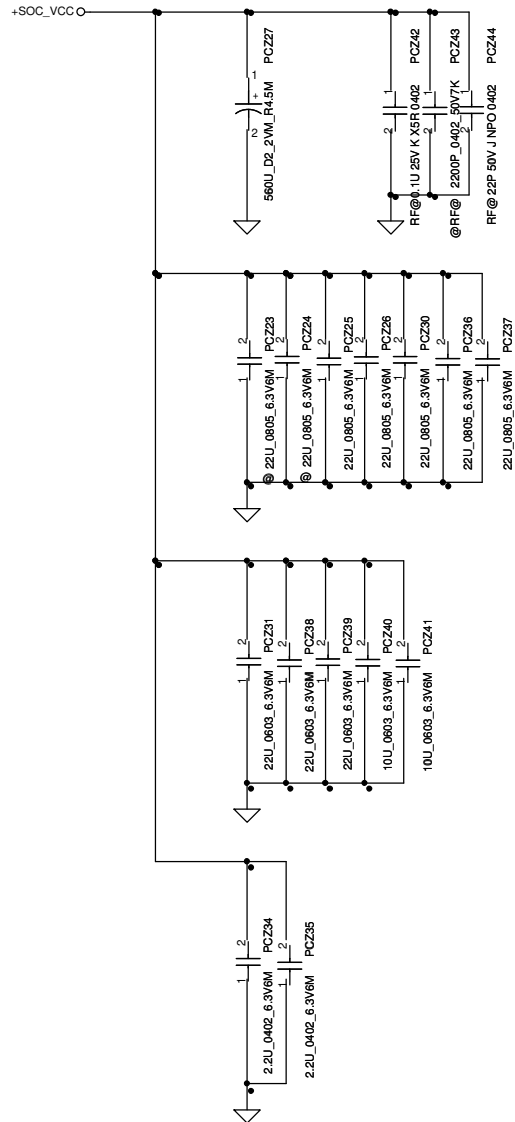
SVID routing

1. Alert# signal must be routed between the Clock and Data lines to reduce the cross talk between them. Signal order arrangement: mobile order is Clock-Alert-Data.
2. SVID spacing requirement is 18mils(0.475mm)  VSSENSE
3. Maximum total microstrip routing length of each SVID signal must not exceed 600mils(152.4mm) .
4. The SVID bus must be ground reference. It cannot be referenced to input (Vbat or 12V) power plans as they can couple noise into the SVID bus as power states change.
5. Avoid routing under noisy circuit, e.g. switch node , Gate driver, B+, Vin, high speed signal.
6. When SVID signal changes Layer, GND return path may be changed also. We need add GND via for GND reference.

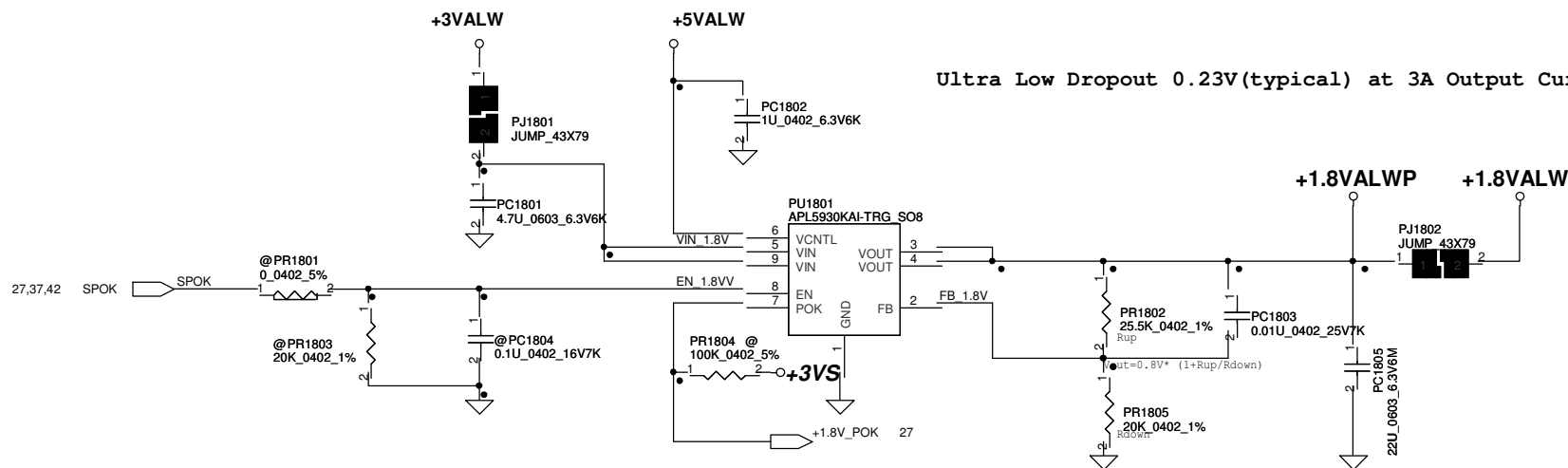
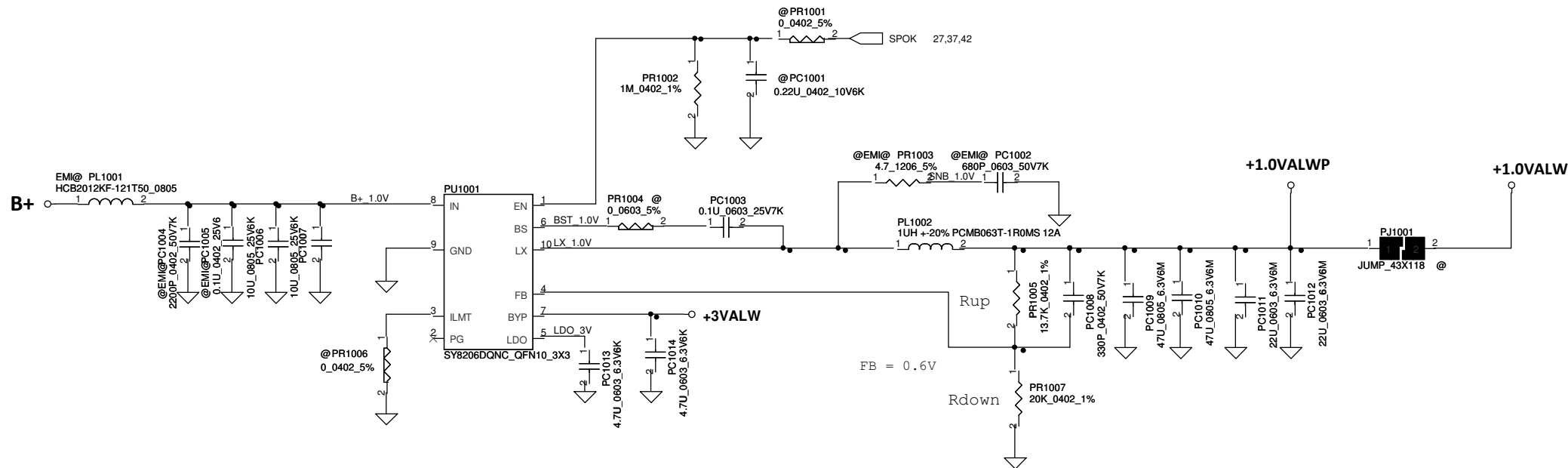
$$C_n = L / ((R_{ntcnet} * R_{sum}) / (R_{ntcnet} + R_{sum}))^{1/3} DCR$$

If C_n is correctly selected, when the load current has a square change, the output voltage also has a square response

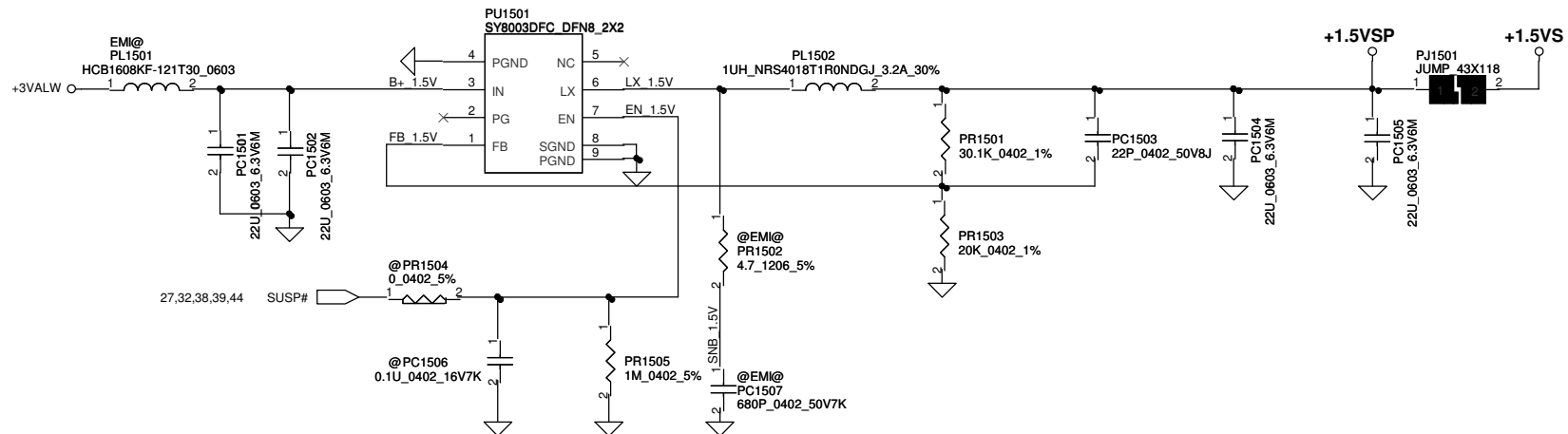
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Issued Date	2014/01/14	Deciphered Date	2015/01/14	SOC VCC/SOC VNN	
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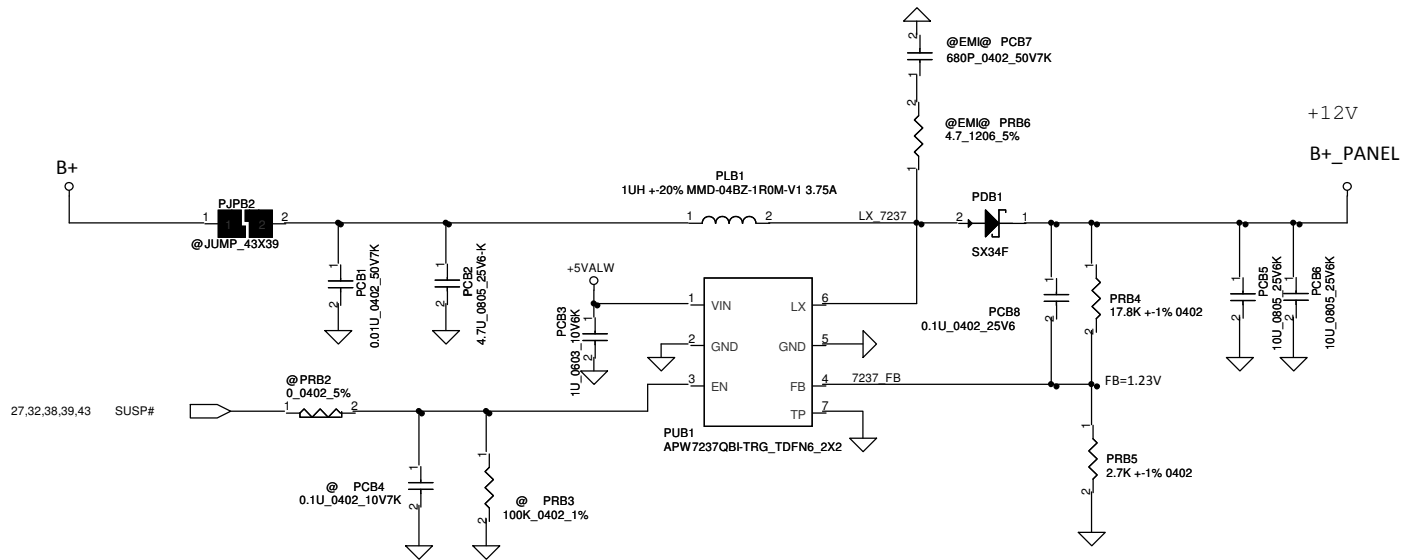
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Issued Date	2014/01/14	Deciphered Date	2015/01/14	Title	PROCESSOR DECOUPLING
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Version change list (P.I.R. List)

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		ME update screw hold	0.11	P31	Change H8 to H_3P0 from H_2P5	10/15	
2		ESD Request	0.11	P24	Change CA36/CA37 to SC400006R00	10/15	
3		Vendor suggestion	0.11	P15	Change LT4 to 0603	10/16	
4		EMI Request	0.11	P24	Change RA10/LA1 to EMI@	10/16	
5		Vendor suggestion	0.11	P30	Add R21 for debug	10/16	
6		For BIOS debug	0.11	P9 P27	Add D2/NMI_DBG#/NMI_DBG#_SOC	10/16	
7		Change to cost down version	0.11	P15	Change U2 to SA00007A300	10/16	
8		EMI Request	0.11	P17,P23 P28,P29	Change L3/L4/L6/L7/L8/L50/ L12/LB84/LB83/LB82 to SM070003Y00	10/16	
9		HW Design Change	0.11	P10	Change power of U55 to +3VALW_EC	10/18	
10		For Debug	0.11	P29	Add JPW1/JPW2	10/18	
11		HW Design Change	0.11	P28	Add R1025/Q5 for LED/Vibrator	10/21	
12		HW Design Change	0.11	P20	Change TS1 to 10/100 Transformer (SP050007K00)	10/21	
13		HW Design Change	0.11	P18	Change JSIM1.4 to GND/ Remove R246/ Change R247.1 to +3VS_WWAN_NGFF	10/21	
14		HW Design Change	0.11	P09	Add DDR_SMB_CLK/DDR_SMB_DATA for DDR Add R101/R102 for isolate SM Bus Add R106/R107 & Change RP49 pin assign	10/21	
15		HW Design Change	0.11	P06	Reserve R108	10/21	
16		Customer Spec Change	0.11	P24	Change Audio Codec to ALC3227	10/22	
17		Customer Requirement	0.11	P09 P28	Add Q73/R110/R109 for TP Add TP_SMB_DATA/TP_SMB_CLK for TP	10/22	
18		HW Design Change	0.11	P21	Change U25.14 to +3VALW_GSEN from +3V_GSEN	10/22	
19		EMI Request	0.11	P24	Add LA1	10/23	
20		EMC Request	0.11	P24	Remove DA12/DA13/DA8/CA66/CA64 Remove CA67/CA65/DA9/CA46/CA50	10/23	
21		ESD Request	0.11	P18	Add C73	10/23	
22		HW Design Change	0.11	P10	Change U58/R3 to @ for S3 autowake issue	10/23	
23		ME Request	0.11	P20	Change footprint of JLAN1 for ME connector modify	10/23	
24		ME Request	0.11	P26	Change footprint of JCR1 for ME connector modify	10/23	
25		EMI Request	0.12	0.29	Shifter JIO1 Pin assign USB20_HUB_P2_R change to Pin 12 USB20_HUB_N2_R change to Pin 13 USB_ON# change to Pin10	10/24	

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
26		EMI Request	0.12	P15	Add RT9/RT10 for translator mode control	10/24	
27		Power Request	0.12	P27	Change WL_OFF# to EC Pin 68 Add VIN_ADC to EC Pin75	10/24	
28		ME Request	0.12	P29	Change JPWR1 to E-T_6710K-Y06M-31L	10/25	
29		Customer Requirement	0.12	P22	Change power of U01 from +3/5VS to +3/5VALW	10/25	
30		HW Design Change	0.12	P22	Change power of RU13 from +5VS to +5VALW	10/26	
31		RF Request	0.12	P16	Change CG3 to 33PF	10/26	
32		RF Request	0.12	P21	Add C151 for +5VS_HDD	10/26	
33		HW Design Change	0.12	P24 P25	Change package of QA4 to SOT323-3 Change package of LB7 to 0402	10/28	
34		HW Design Change	0.12	P24	Change QA5 to SB000008E10	10/28	
35		HW Design Change	0.21	P22	Change footprint of CU15 to 0603	11/21	
36		Vender update firmware	0.21	P30	Change US1 to SA000076330 IT8350E-128/CX-002C	11/21	
37		HW Design Change	0.21	P09	Rotate D2 direction	11/21	
38		HW Design Change	0.21	P32	Change U2102 to SA00006U600 A0Z1336	11/21	
39		HW Design Change	0.21	P27	Change R244/R245 to @	11/21	
40		HW Design Change	0.21	P10	Change U59/R4 to @	11/21	
41		Vender recommend	0.21	P24 P25	Modify audio code and Amp. circuit	11/21	
42		HW Design Change	0.21	P08	Change TS_INT# to GPIO_S0_SC_94/GPIO_S5_11 Add D10/U67/R1024/R1026 for leakage	11/22	
43		HW Design Change	0.21	P31	Remove co-layout circuit of SLB9635TT1.2	11/22	
44		RF Request	0.21	P28	Change POUT to JPSEN1	11/22	
45		ME Request	0.21	P16	Rotate JLCD1 direction	11/22	
46		HW Design Change	0.21	P09	Swap pin assign of RP54 for layout	11/22	
47		BIOS Request	0.21	P10	Change U59/R4 to mount	11/25	
48		HW Design Change	0.21	P24	Change LA10 to HCB2012VF-601T20 Change LA8 to PBX160808T-601Y-N	11/26	
49		Vender recommend	0.21	P30	Add R1031/R1032	11/26	
50		Parts update revision	0.21	P03	Change N3520@ CPU P/N to SA00007E940 Change N2820@ CPU P/N to SA00007EK30	11/27	

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
51		HW Design Change	0.21	P24	Change RA41/RA42/RA43/RA44 to SM010008A00	11/27	
52		HW Design Change	0.21	P27	Change R214 to 15K for PV	11/27	
53		HW Design Change	0.21	P8,P11 P12,P18 P19,P20 P21,P22 P26,P27	Change Footprint to Short Pad R266/R998/R1022/R1023/R1021/RF34/RN2/R287 RH411/RH412/R227/RA35/RA24/RA25/RR9/R482 L9/R222/R175	11/27	
54		ME Request	0.21	P31	Change H8 size	11/27	
55		HW Design Change	0.21	P27	Change R244/R245 to mount	11/28	
56		HW Design Change	0.21	P10	Add R13/R14 Change R1/R2 to @	11/28	
57		HW Design Change	0.21	P15	Change R1068 to mount	11/28	
58		HW Design Change	0.21	P28	Add R188/R189	11/28	
59		Thermal Request	0.21	P06	Add Q8 for thermal remote detect	11/28	
60		ESD Request	0.21	P29	Add C168/C169	11/28	
61		ESD Request	0.21	P29	Remove D8 for layout space	11/28	
62		ESD Request	0.21	P32,P27	Add CF30/CF31	11/28	
63		HW Design Change	0.21	P27,P29	Exchange net name: VOLUME+/VOLUME-	11/28	
64		HW Design Change	0.21	P03	Remove 9635@/9656@ from BOM option table	11/28	
65		HW Design Change	0.21	P16	Add R1069 for panel sequence	11/29	
66		HW Design Change	0.21	P27	Change L9 to 0603	12/01	
67		HW Design Change	0.3	P24	Change DA5 to BAT54AW-L_SOT323 for layout space	12/01	
68		ESD Request	0.3	P27	Add C134/C139/C140/C141/C142/ Add C143/C144/C145	12/02	
69		HW Design Change	0.3	P08	Add R1070 for RTC power consumption	12/02	
70		HW Design Change	0.3	P27	Add R230 for pull up HOME_INT# to +3VS	12/03	
71		ESD Request	0.3	P27	Add C147	12/03	
72		HW Design Change	0.3	P21	Add RH414 Change power source of U25 to +3VL	12/03	
73		Vender recommend	0.3	P08,P20	Change C1009,C1010 to 18P Change C1003,C1004 to 12P Change CL15,CL16 to 12P	12/12	
74		HW Design Change	0.31	P22	Remove RA25	12/23	
75		HW Design Change	0.31	P09	Add R179,R180,R181,R184 for reserve	12/23	

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
76		HW Design Change	0.31	P09	Change RP54,RP50 to R111~R118 for debug	12/23	
77		ME Request	1.0	P29	Change JPWR1 to 6718K-Y06N-21L	01/07	
78		Customer Change Spec	1.0	P27,P28	Remove JPSEN1/POUT	01/07	
79		HW Design Change	1.0	P08	Remove R1024/D10 Change R1026/U67 to mount	01/08	
80		HW Design Change	1.0	P10	Change power source of U53 to +1.8VALW Change power source of U61 to +1.8VALW Change power source of U62 to +1.8VALW Change power source of U64 to +1.8VALW	01/08	
81		HW Design Change	1.0	P10	Change power source of U54 to +3VALW_EC Change power source of U57 to +3VALW_EC	01/08	
82		HW Design Change	1.0	P10	Remove R1/R2 Add R1024/R1033	01/08	
83		HW Design Change	1.0	P09	Change R181/R180/R179/R184 to R_SHORT	01/08	
84		HW Design Change	1.0	P30	Change RR12/RR13/RR14 to R_SHORT	01/08	
85		HW Design Change	1.0	P32	Change CF26/CF27 to 3300PF	01/08	
86		HW Design Change	1.0	P28	Change R1025 to 120 ohm	01/08	
87		HW Design Change	1.0	P15	Remove UT3, CT24 for layout space	01/08	
88		HW Design Change	1.0	P19	Change RN6/RN8/R973 to @	01/08	
89		HW Design Change	1.0	P24,P25	Change RA38 to R_SHORT Change RA50/RA49/R274/R275 to R_SHORT	01/08	
90		HW Design Change	1.0	P27,P28 P32	Change R299/R189/RF4 to R_SHORT	01/08	
91		HW Design Change	1.0	P08	Swap RTC_RST#/RTC_TEST#	01/08	
92		HW Design Change	1.0	P11	Reserve L51/L52 for 1.35V	01/09	
93		HW Design Change	1.0	P15,P30	Change LT4/LB3 to R_SHORT	01/09	
94		HW Design Change	1.0	P30	Remove CH19/Y3/CH18 Connect Pin9 of US1 to GND	01/09	
95		HW Design Change	1.0	P20	Swap LAN_LINK#/LAN_ACT#	01/10	
96		EMI Request	1.0	P16,P28	Change L1/L2/R170/R171 to R_SHORT	01/10	
97		HW Design Change	1.0	P25,P20	Change RA50/RA49/R274/R275 to 0 ohm Swap LAN_LINK#/LAN_ACT#	01/13	
98		EMI Request	1.0	P17	Change L4/L6/L7/L8 to @ Change R182/R186/R187/R190 to mount(20ohm) Change R191/R192/R193/R194 to mount(20ohm)	01/13	
99		EMI Request	1.0	P26	Change CR12 to @ Change RR4/RR6/RR7/RR16/RR17 to mount	01/13	
100		ID Request	1.0	P28	Change R1025 to 56ohm	01/14	

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Issued Date	2014/01/14	Deciphered Date	2015/01/14	Title	HW PIR
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