Compal Confidential

Broadwell M/B Schematics Document

Intel ULV Processor with DDRIIIL

Date : 2015/01/31

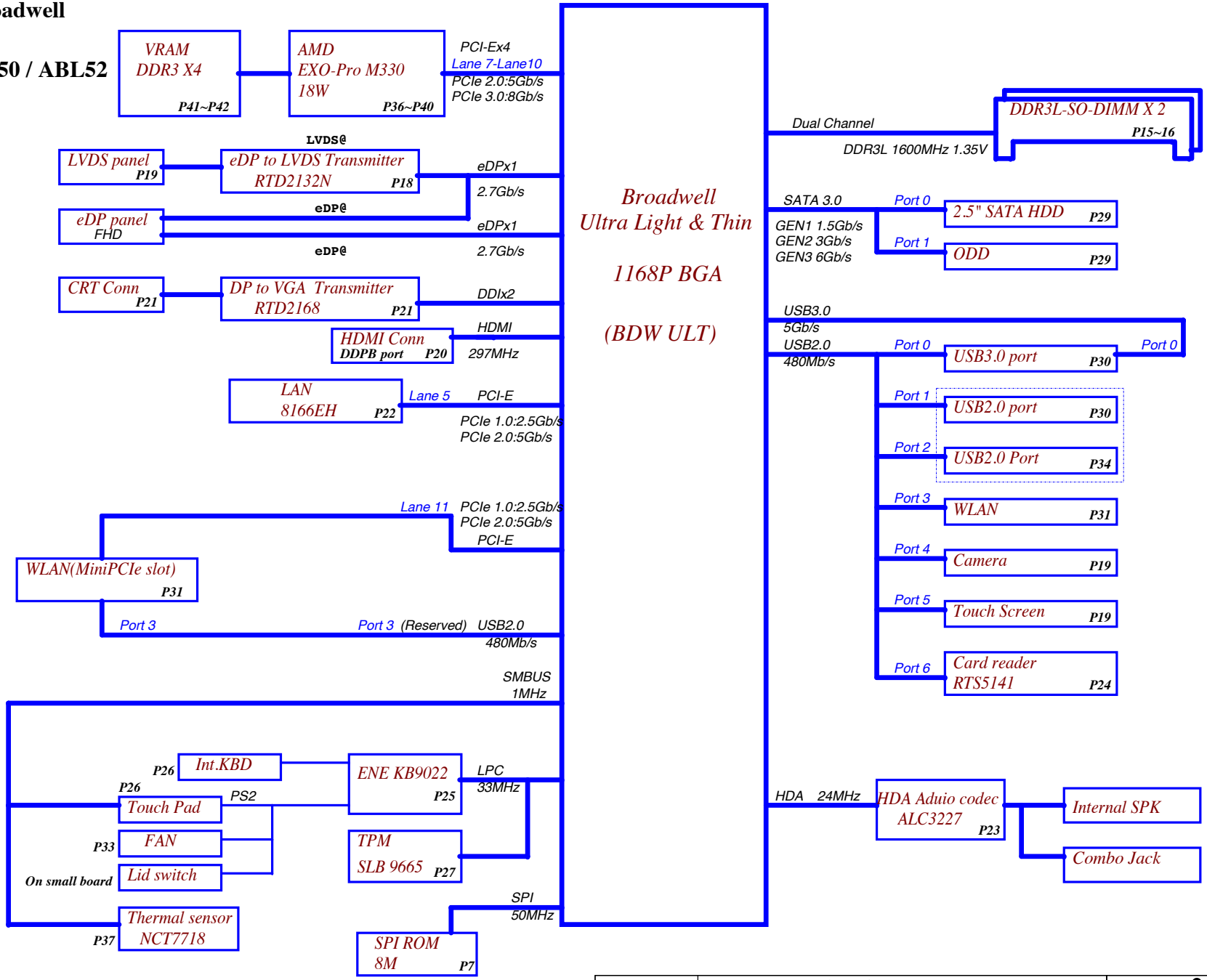
Version 0.3

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.		
Title: Cover Page		
Size: B	Document Number: LA-C701P	Rev: 0.1
Date: Saturday, January 31, 2015	Sheet 1 of 61	

Compal Confidential
Model Name : Broadwell

File Name : AHL50 / ABL52
LA-C701P



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Compal Electronics, Inc.

Title: Block Diagrams

Size	Document Number	Rev
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Power rail	Control (EC)	Source (CPU)
+RTCVCC	X	X
VIN	X	X
BATT+	X	X
B+	X	X
+VL	X	X
+3VL	X	X
+5VALW	EC_ON	X
+3VALW	EC_ON	X
+3VALW_EC	EC_ON	X
+3V_PCH	PCH_PWR_EN	X
+1.35V_VDDQ	SYSON	PM_SLP_S5#/PM_SLP_S4#
+5VS	SUSP#	PM_SLP_S3#
+3VS	SUSP#	PM_SLP_S3#
+1.5VS	SUSP#	PM_SLP_S3#
+1.05VS	SUSP#	PM_SLP_S3#
+0.6V_0.675VS	SUSP#	
+VCC_CORE	X	VR12.5_VR_ON

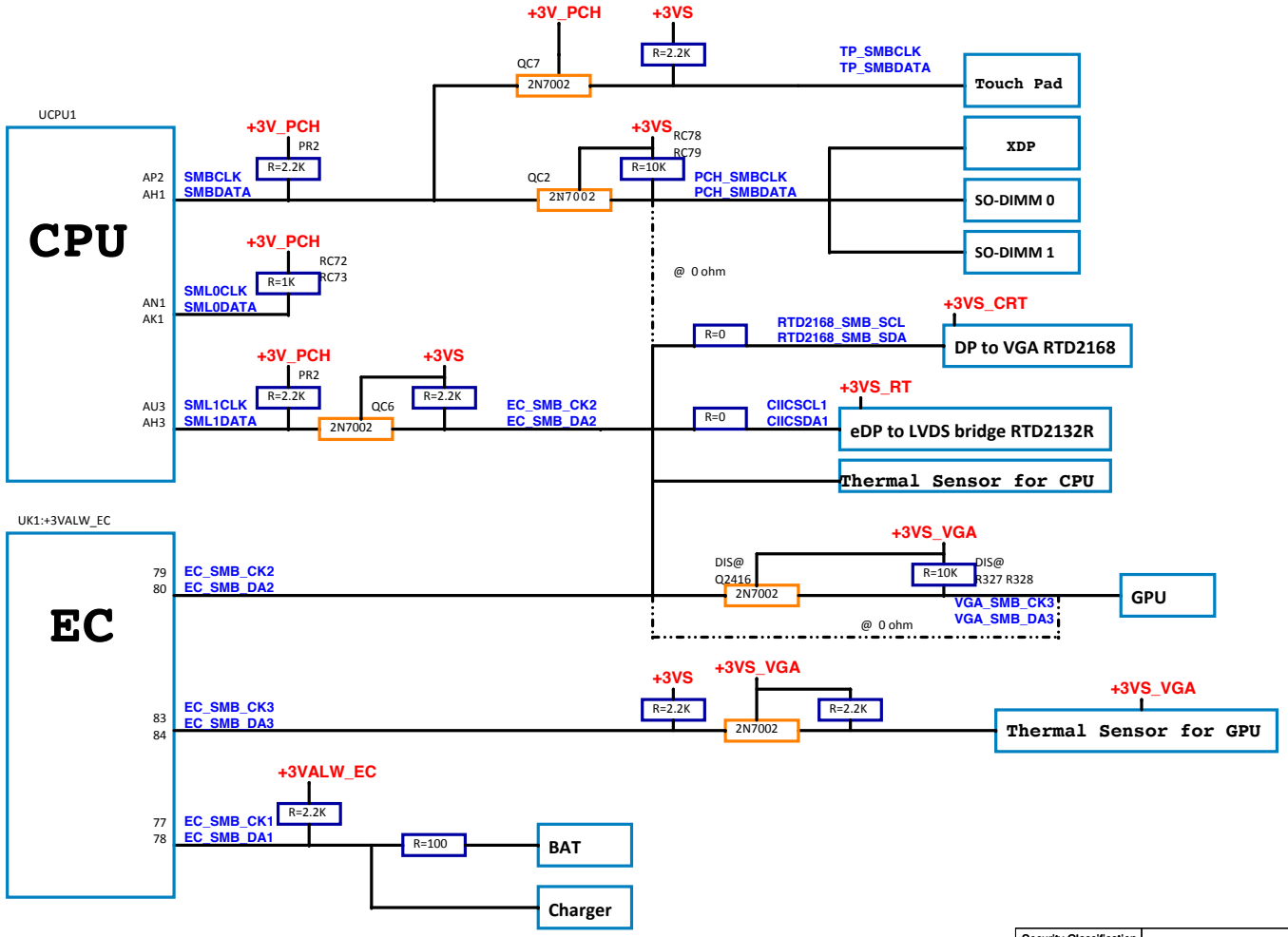
@ is NO SMT part (empty)

@EMI@,@ESD@,@RF@ : Reserve , don't pop.

RF@ : RF team request, must add.
EMI@ : EMI team request, must add.
ESD@ : ESD team request, must add.

SPI@ : SPI ROM request
LVDS@ : Support LVDS panel.
eDP@ : Support eDP panel

DIS@ : for AMD EXO
UMA@ : for UMA only
TP@ : TP SMBus
XTAL@ : for HSW SMT in DB phase only
GCLK@ : Support GCLK
GCLKUMA@ : UMA
GCLKDIS@: DIS
8111@ : for LAN giga
8166@ : for LAN 10/100



<USB2.0 port>

USB2.0 port	DESTINATION	
	UMA	Dis
0	USB 2.0/3.0(left side)	USB 2.0/3.0(left side)
1	USB 2.0(left side)	USB 2.0(left side)
2	USB 2.0(right side)	USB 2.0(right side)
3	WLAN/BT	WLAN/BT
4	Camera	Camera
5	Touch screen	Touch screen
6	Card reader	Card reader
7	X	X

<PCI-E,SATA,USB3.0>

Lane#	USB3.0	DESTINATION	
		UMA	Dis
0		USB3.0	USB3.0
1			

Lane#	PCIE	DESTINATION	
		UMA	Dis
0			
1			
2			
3		LAN	LAN

Lane#	SATA	DESTINATION	
		UMA	Dis
0		HDD	HDD
1		ODD	ODD
2		WLAN	WLAN

Lane#	PEG	DESTINATION	
		UMA	Dis
0			GPU
1			
2			
3			

Lane#	PCIE REQ	DESTINATION	
		UMA	Dis
0		LAN	LAN
1		X	X
2		WLAN	WLAN
3		X	GPU
4		PU	PU
5		PU	PU

Board ID control

15"	DB	SI	PV	MV
UMA RK4	0 ohm	15K ohm	27K ohm	43K ohm
DIS RK4	12k ohm	20k ohm	33k ohm	56k ohm

Thermal Sensor
CPU internal : PECI protocal
PCH internal : 0x90
GPU internal : 0x82
CPU external : 0x98
GPU external : 0x98

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Title: Notes List

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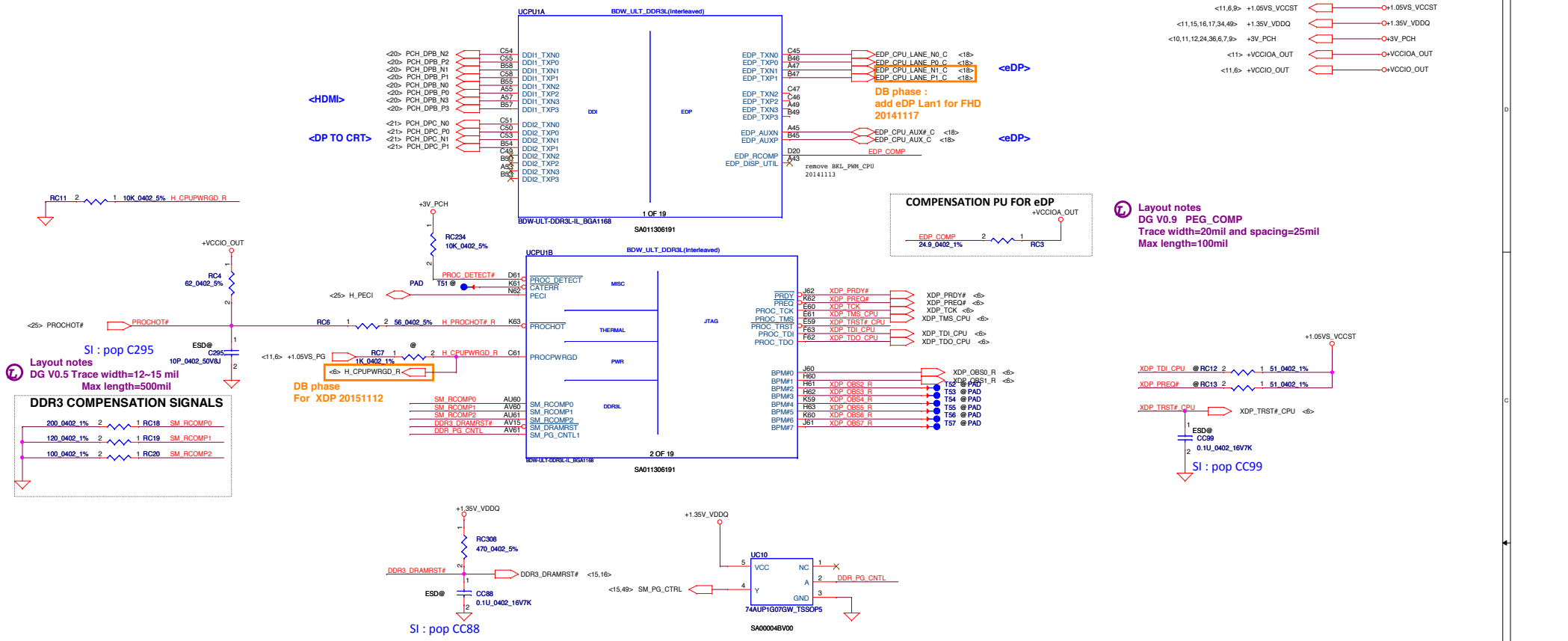

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Compal Electronics, Inc.

Title: DDI,MISC,XDP

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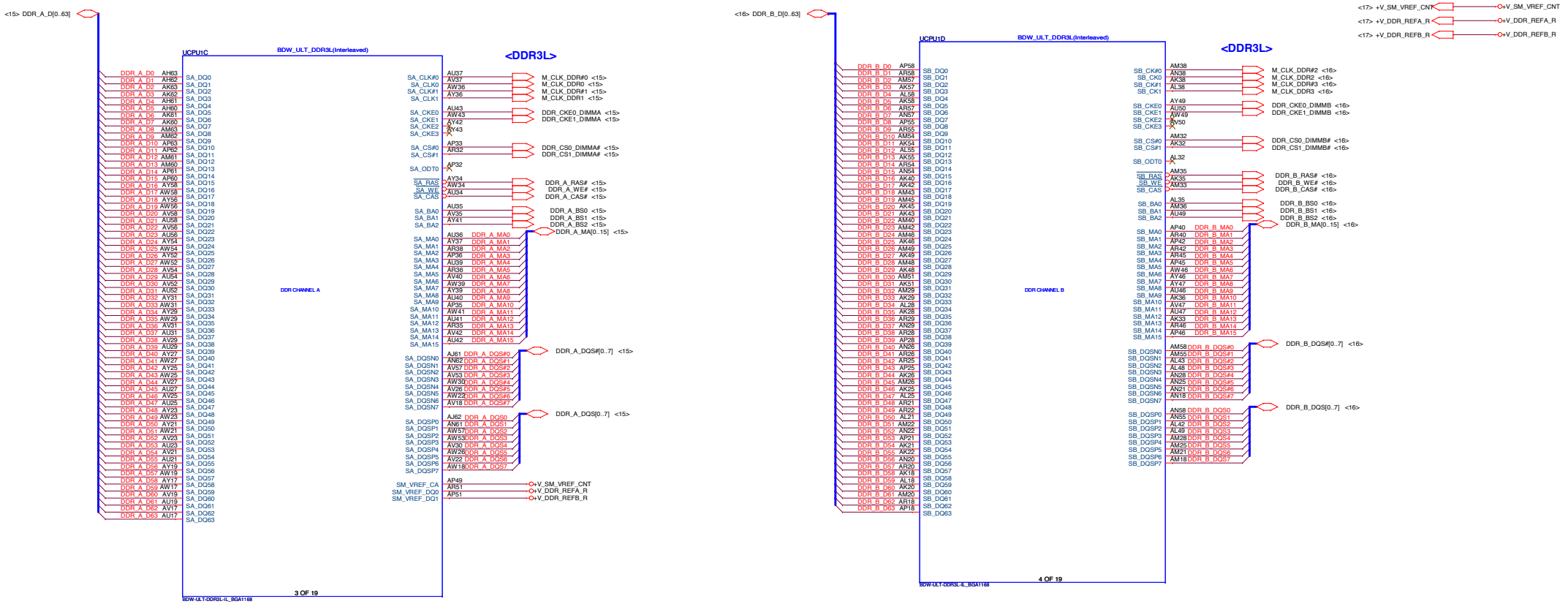

Interleaved Memory

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.			
Title: DDRIII			
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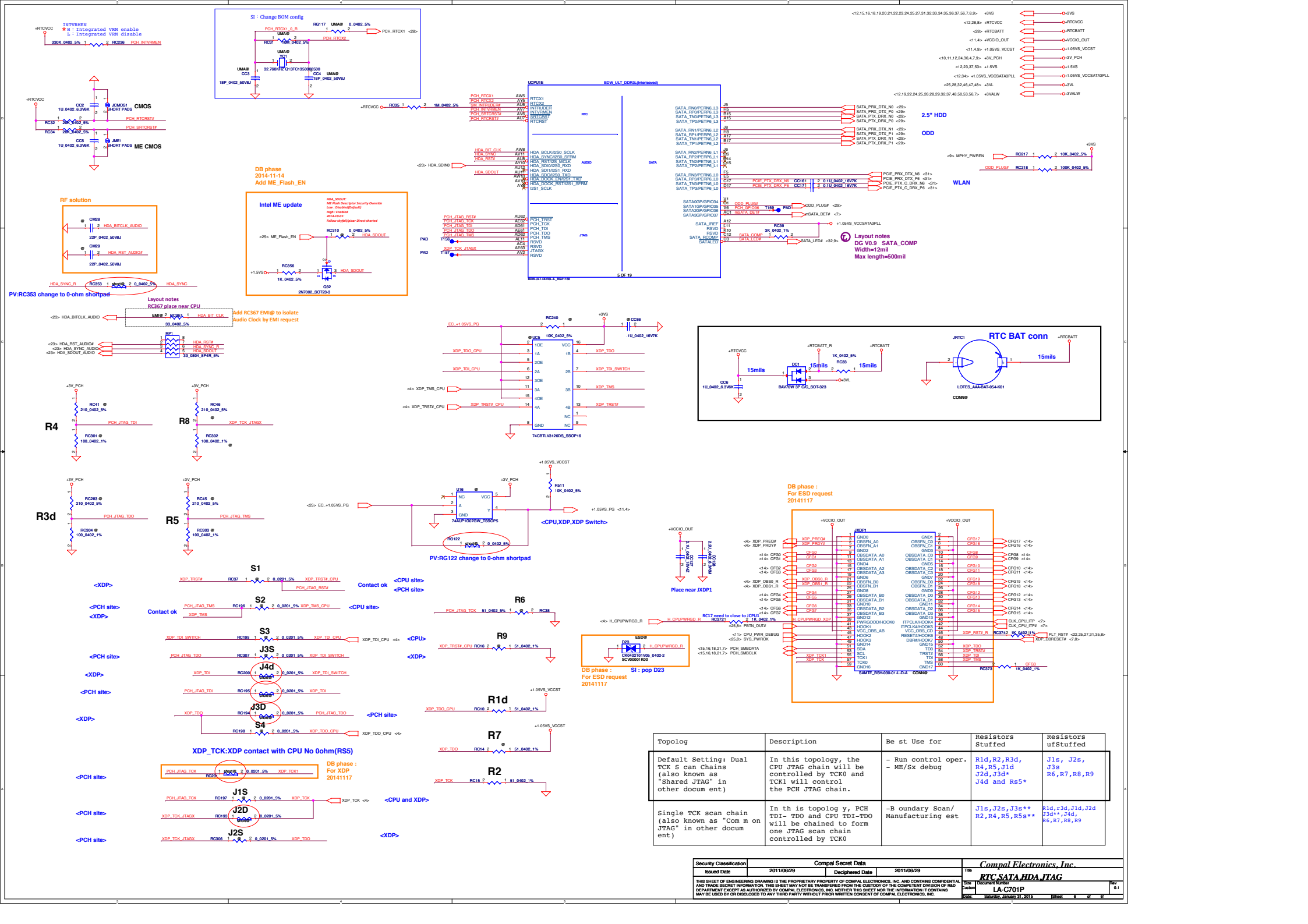

Topolog	Description	Be st Use for	Resistors Stuffed	Resistors ufStuffed
Default Setting: Dual TCK S can Chains (also known as "Shared JTAG" in other docum ent)	In this topology, the CPU JTAG chain will be controlled by TCK0 and TCK1 will control the PCH JTAG chain.	- Run control oper. - ME/Sx debug	R1d,R2,R3d, R4,R5,J1d J2d,J3d* J4d and Rs5*	J1s, J2s, J3s R6,R7,R8,R9
Single TCK scan chain (also known as "Com m on JTAG" in other docum ent)	In th is topolog y, PCH TDI- TDO and CPU TDI-TDO will be chained to form one JTAG scan chain controlled by TCK0	-B oundary Scan/ Manufacturing est	J1s,J2s,J3s** R2,R4,R5,R5s**	R1d,r3d,J1d,J2d J3d**,J4d, R6,R7,R8,R9

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Compal Electronics, Inc.			
Title	RTC,SATA,HDA,JTAG		
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PV phase :
Add pull-up at PCIECLKREQ1#
20150125

SI phase :
Modify CLK request channel
20141214

PCIE LAN
WLAN
GPU

UCPU1F — BDW_ULT_DDR3L(Interleaved) — CLOCK SIGNALS — 6 OF 19 — BDW-ULT-DDR3L-IL_BGA1168

UCPU1G — BDW_ULT_DDR3L(Interleaved) — LPC SPI SMBUS C-LINK — 7 OF 19 — BDW-ULT-DDR3L-IL_BGA1168

<EC>
<XDP CLK >

SI : Change BOM config

RF solution

Layout notes
avoid stub trace too long

Layout notes
RC368 place near CPU
RC369 place near EC
RC56 place near SPI ROM

SPI ROM (8MByte)

EON	SA000046400	S IC FL 64M EN25Q64-104HIP SOP 8P
MXIC	SA00006N100	S IC FL 64M MX25L6473EM2I-10G SOP 8P
WINBOND	SA000039A30	S IC FL 64M W25Q64FVSSIQ SOIC 8P SPI ROM
Micron	SA00005L100	S IC FL 64M N25Q064A13ESEC0F SO8W 8P

CPU THERMAL SENSOR

SI : add CPU thermal sensor 12/23

Address: 1001100xb NCT7718W
(x is R/W bit)

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: CLK,SPI,SMB,LPC

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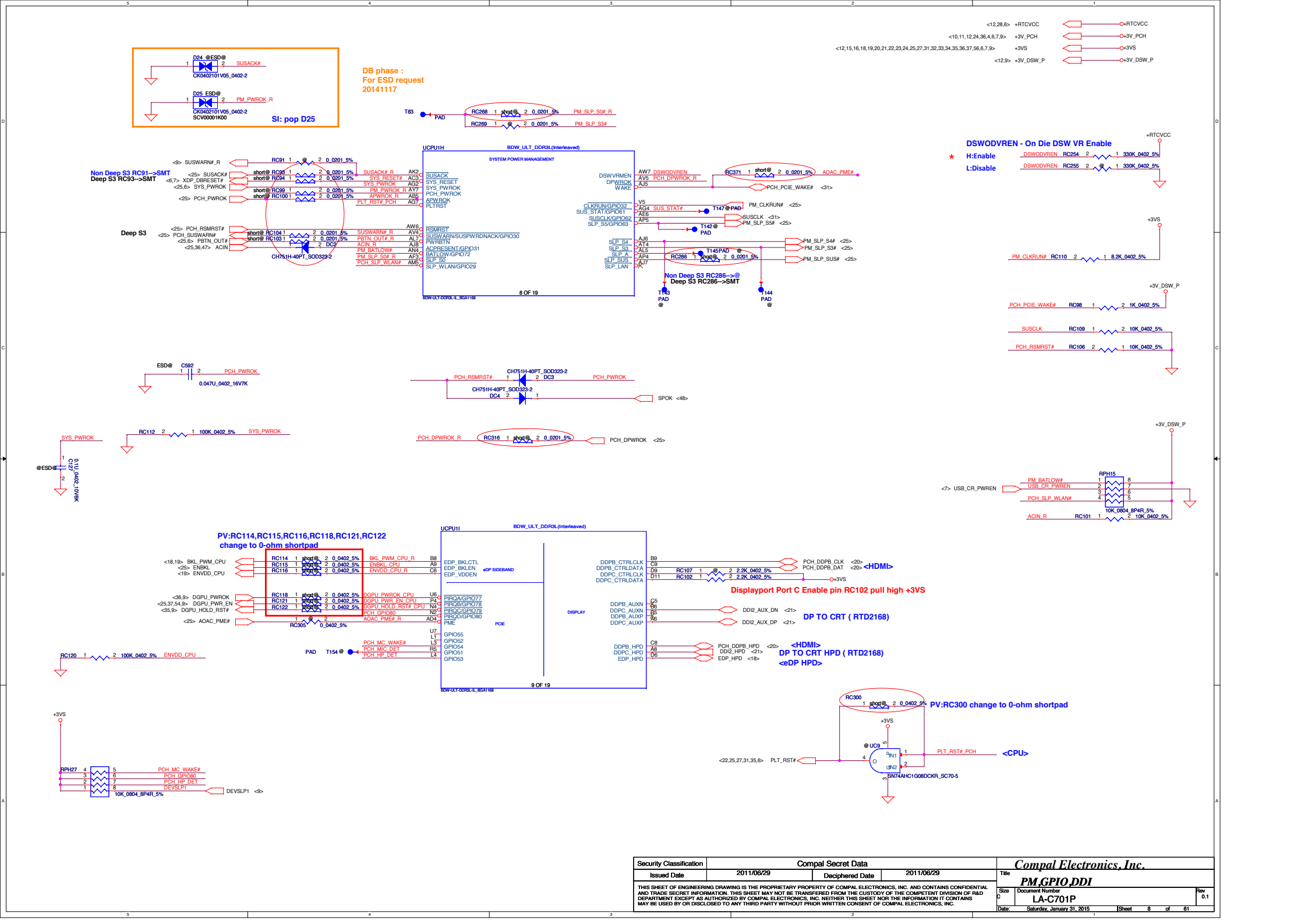

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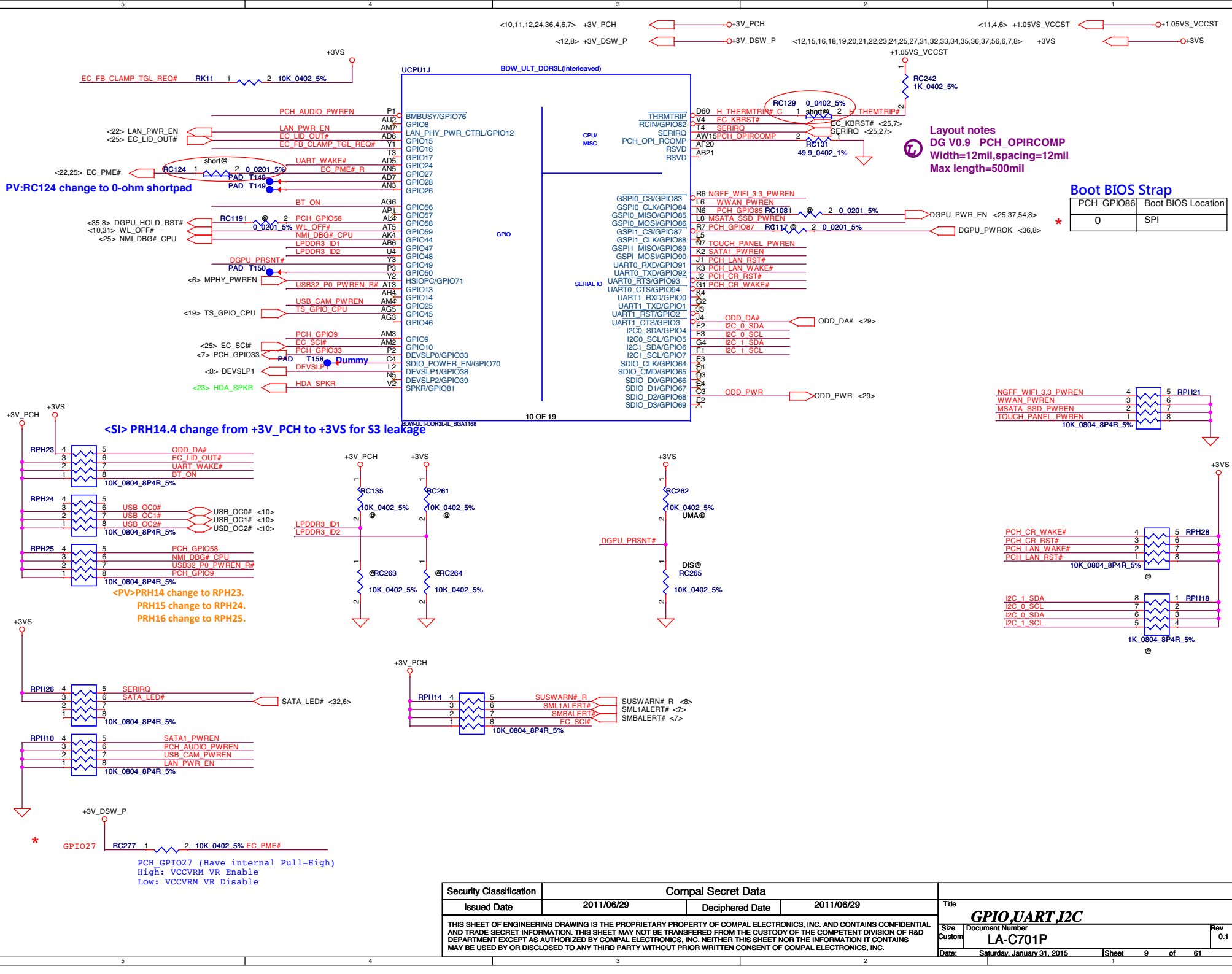
Title	PM,GPIO,DDI		
Size	Document Number		Rev
C	LA-C701P		0.1
Date:	Saturday, January 31, 2015	Sheet	8 of 61


UCPU1J
BDW_ULT_DDR3L(Interleaved)
BDW-ULT-DDR3L-IL_BGA1168
10 OF 19
PV:RC124 change to 0-ohm shortpad
<SI> PRH14.4 change from +3V_PCH to +3VS for S3 leakage
<PV>PRH14 change to RPH23.
PRH15 change to RPH24.
PRH16 change to RPH25.
PCH_GPIO27 (Have internal Pull-High)
High: VCCVRM VR Enable
Low: VCCVRM VR Disable
Layout notes
DG V0.9 PCH_OPIRCOMP
Width=12mil,spacing=12mil
Max length=500mil
Boot BIOS Strap
PCH_GPIO86 | Boot BIOS Location
0 | SPI
Security Classification | Compal Secret Data
Issued Date | 2011/06/29 | Deciphered Date | 2011/06/29
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Title
GPIO,UART,I2C
Size Custom
Document Number
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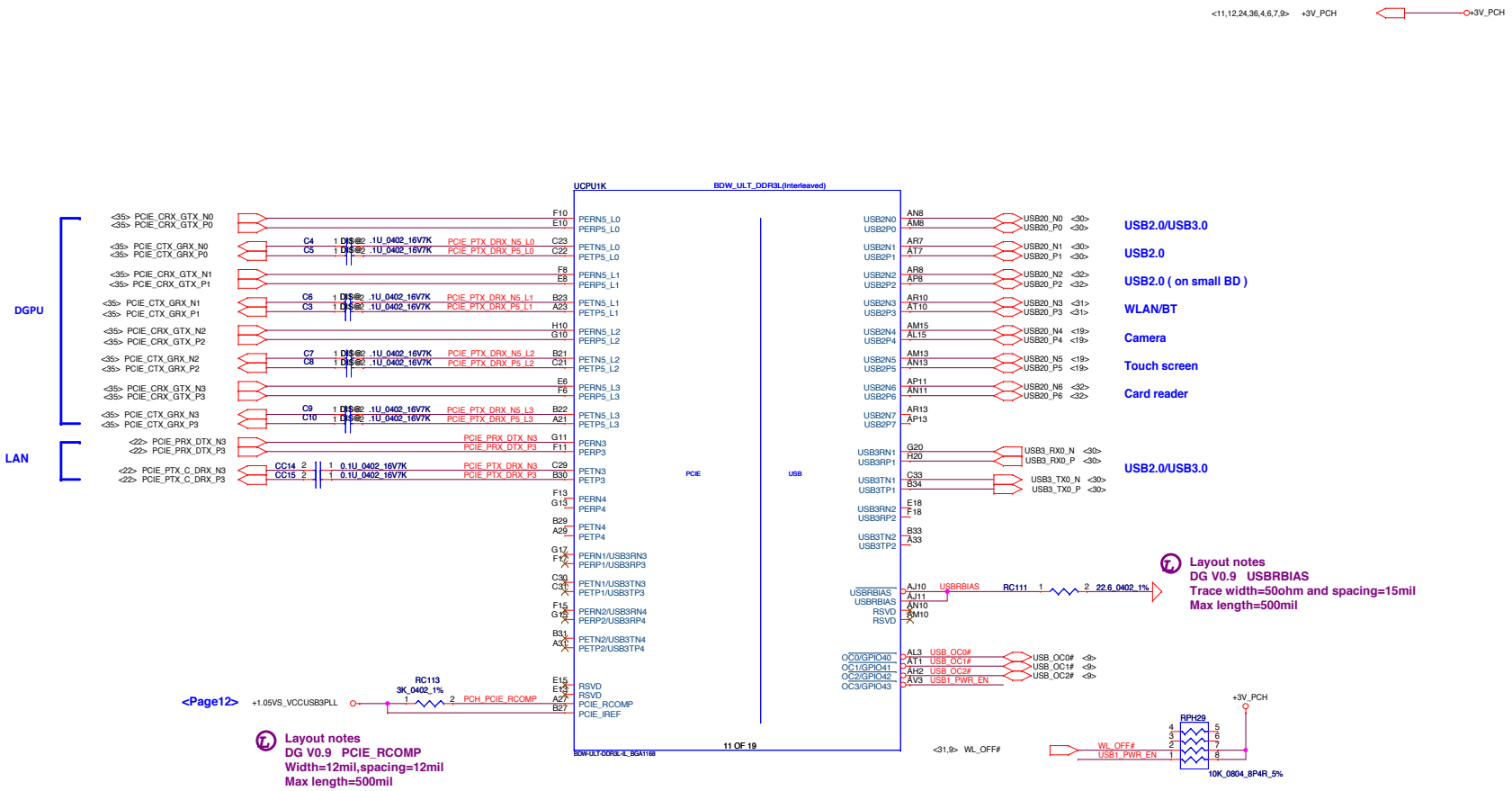

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Title	PCIE,USB		
Size: C	Document Number: LA-C701P		Rev: 0.1
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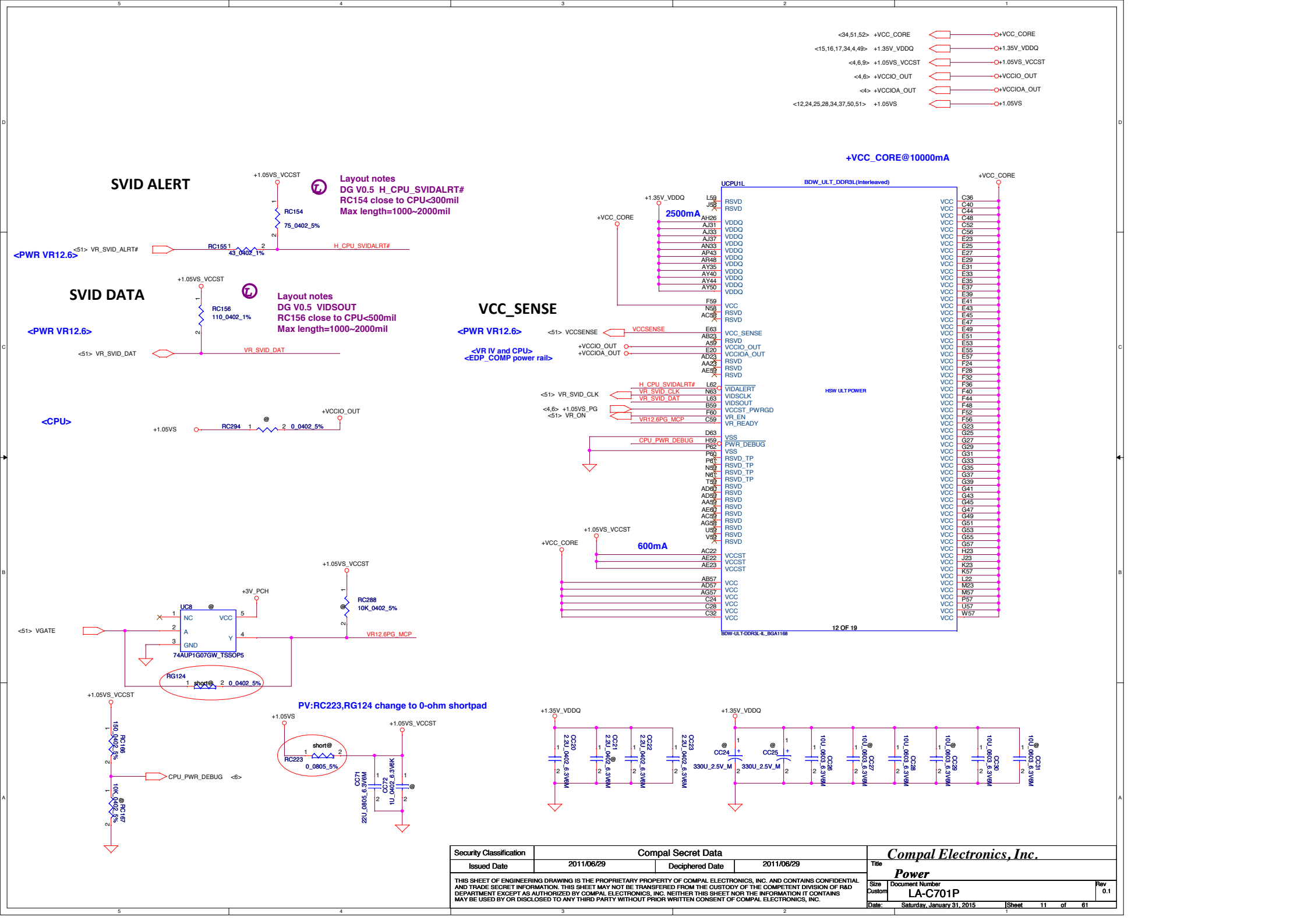

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Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: Power

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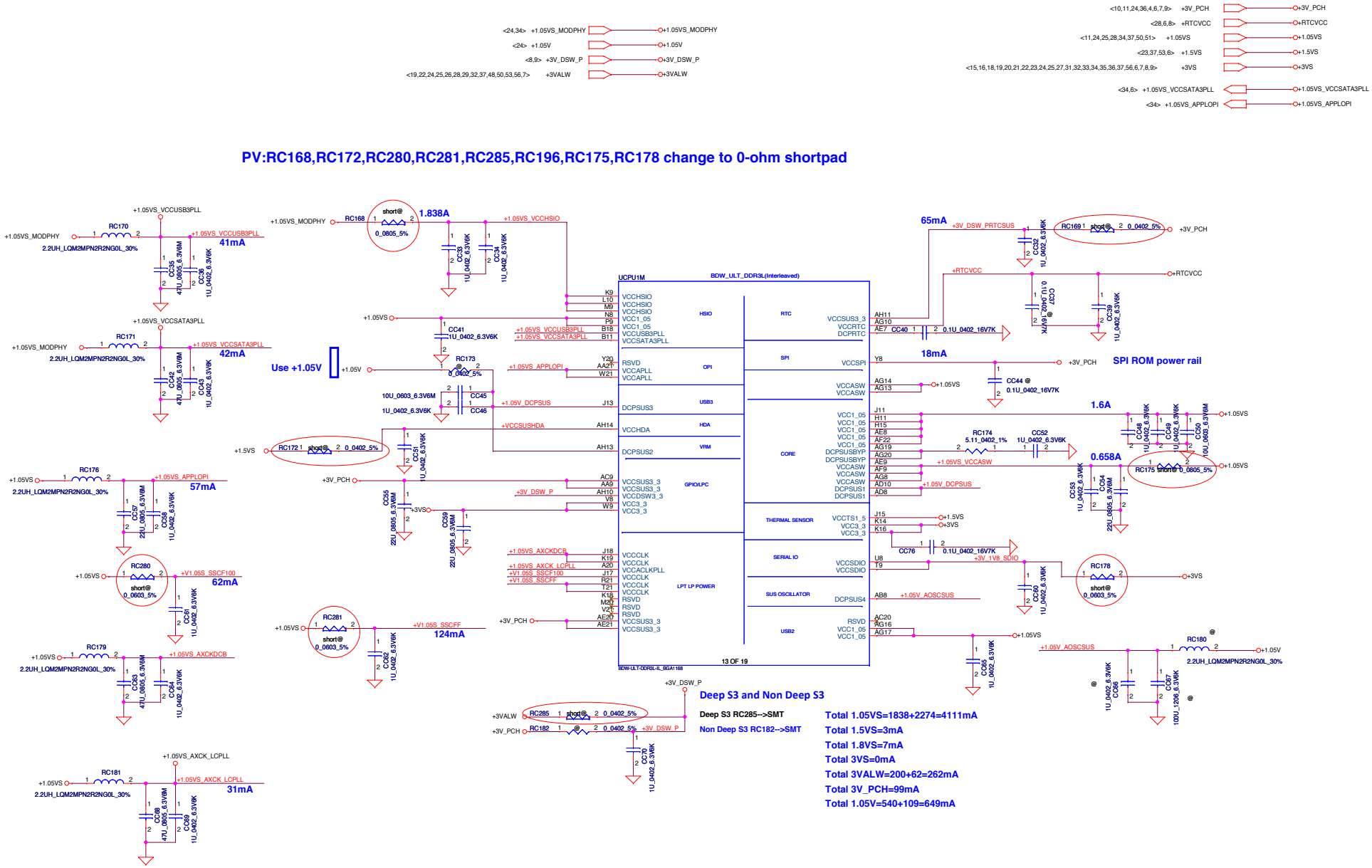

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Title	Power		
Size	Document Number		Rev
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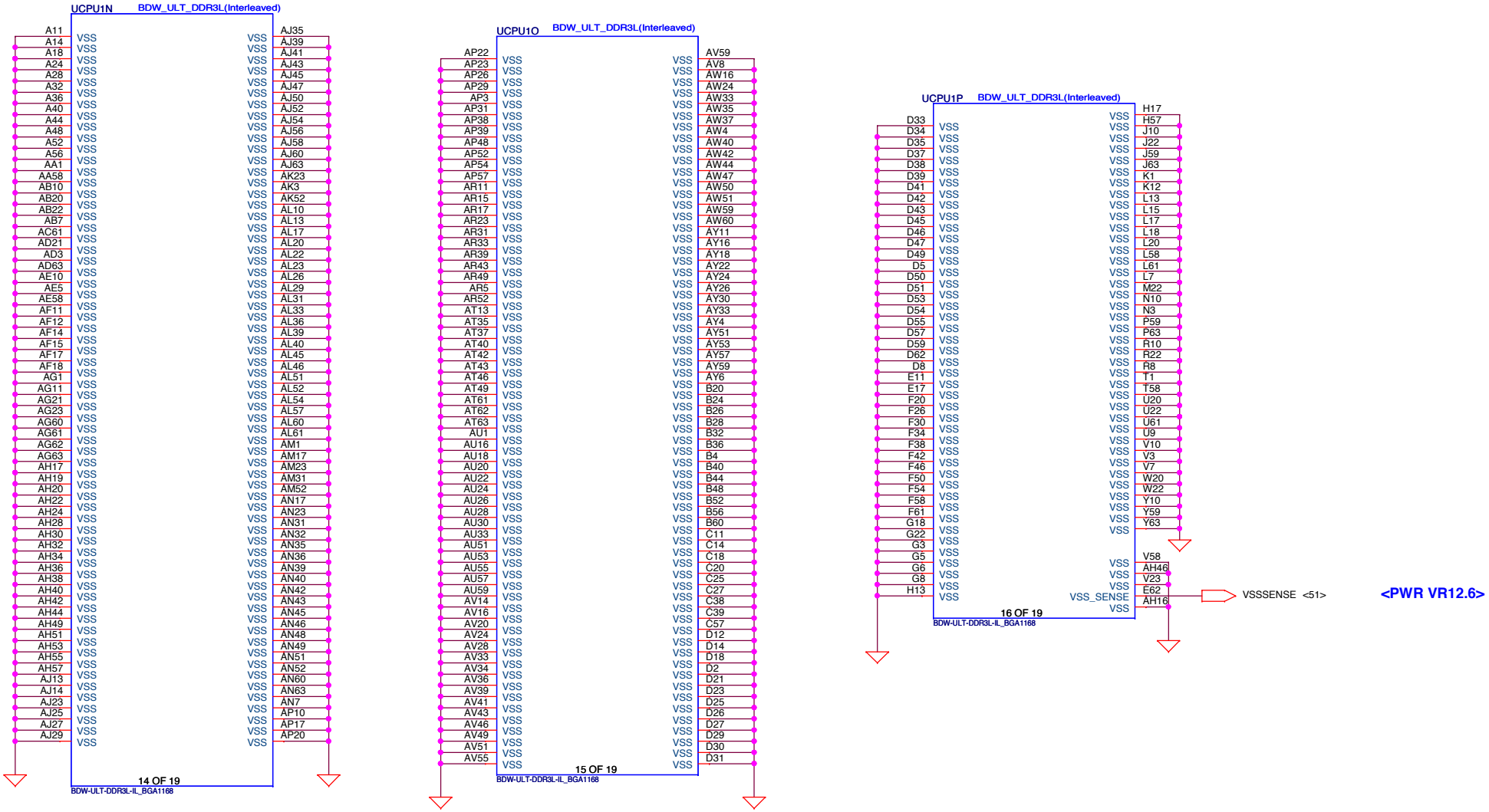

Security Classification	Compal Secret Data		
Issued Date	2010/05/27	Deciphered Date	2011/05/11

Compal Electronics, Inc.

Title	GND/VSSSEN	
Size	Document Number: LA-C701P	Rev: 0.1
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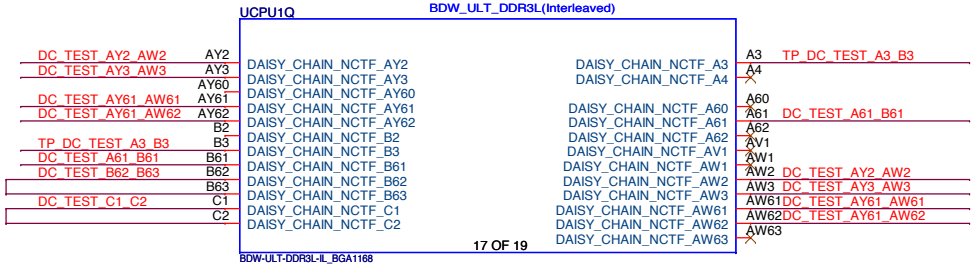
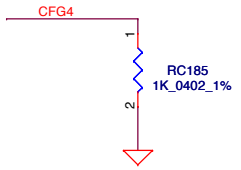
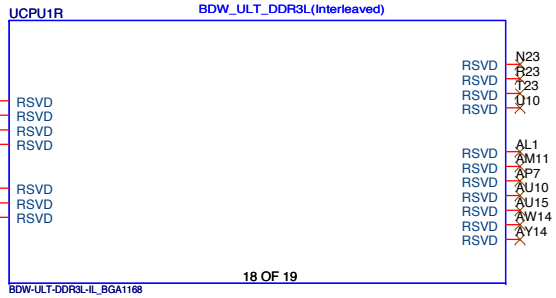
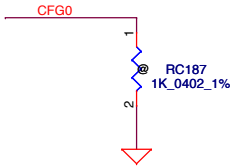
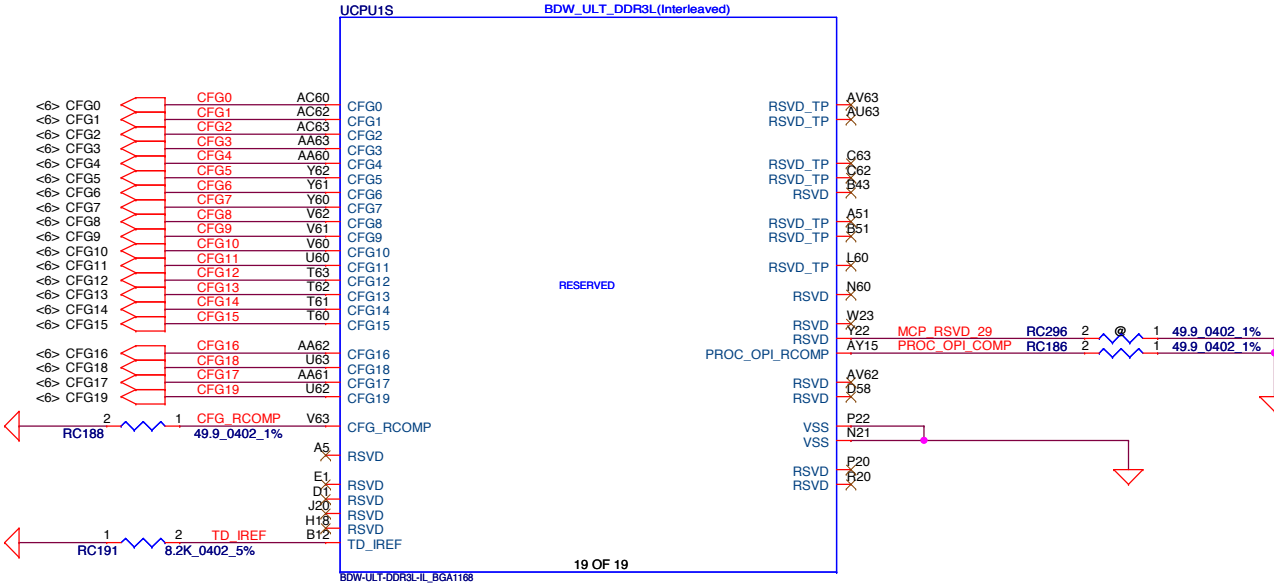




Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port







Layout notes
DG V0.9 PROC_OPI_COMP
Width=12mil,spacing=12mil
Max length=500mil

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Issued Date	2011/06/29	Deciphered Date	2011/06/29

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Title: RSVD/CFG

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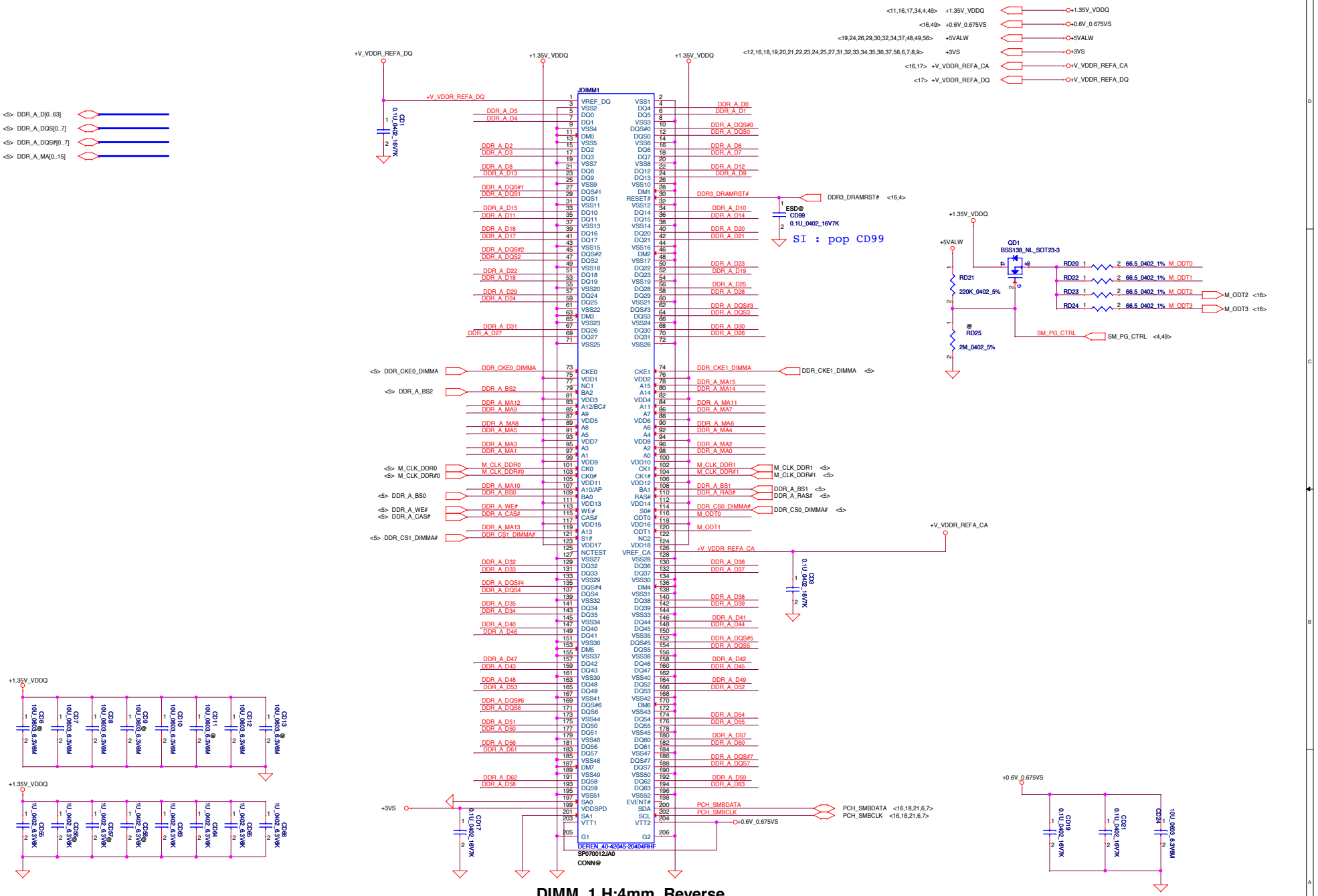

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Title	DDR3L DIMM0		
Size	Document Number		Rev
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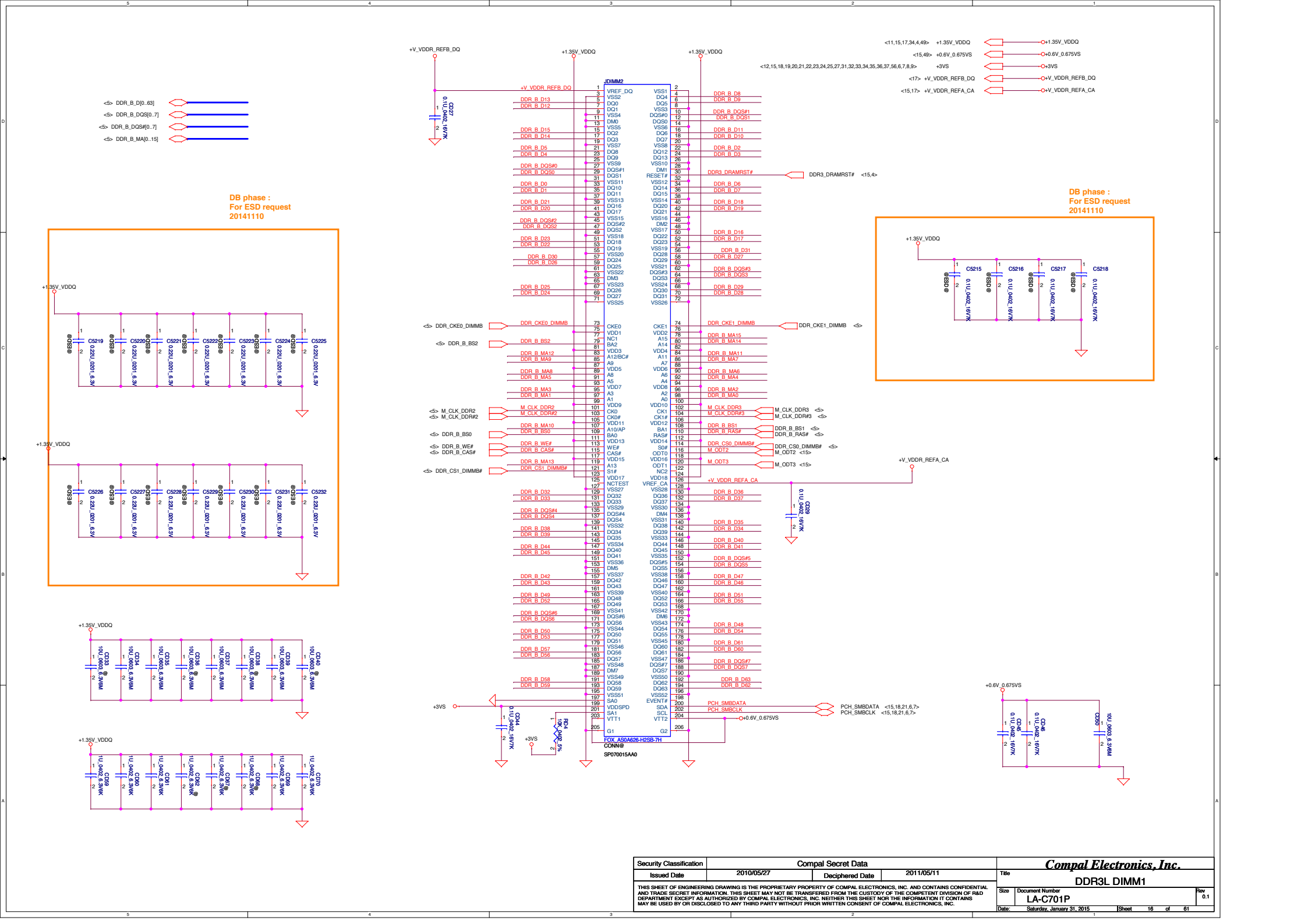
DB phase :
For ESD request
20141110
DB phase :
For ESD request
20141110
JDIMM2
CONN@
SP070015AA0
FOX_AS0A626-H2SB-7H
Security Classification
Compal Secret Data
Issued Date
2010/05/27
Deciphered Date
2011/05/11
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Title
DDR3L DIMM1
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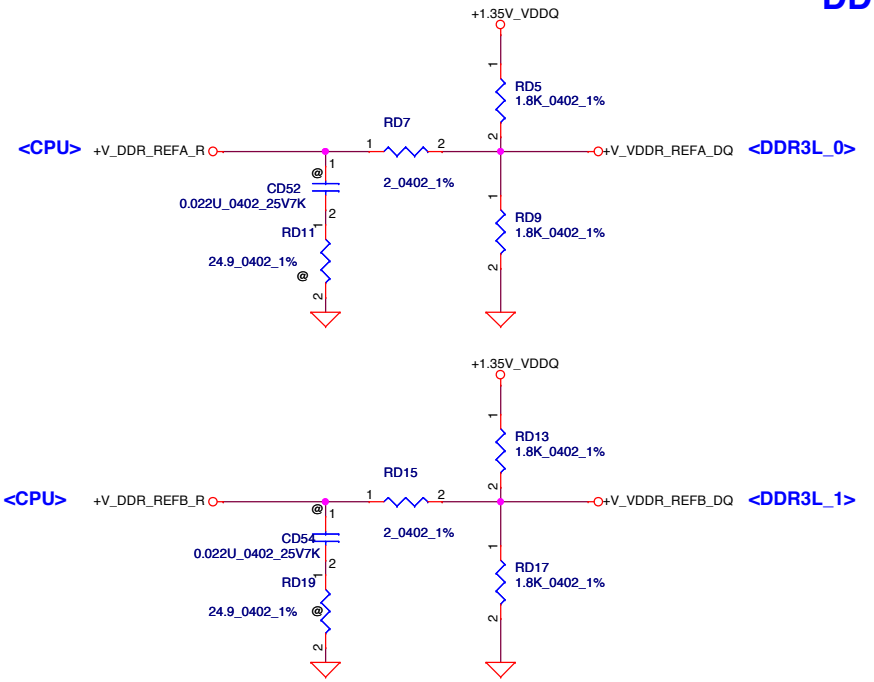
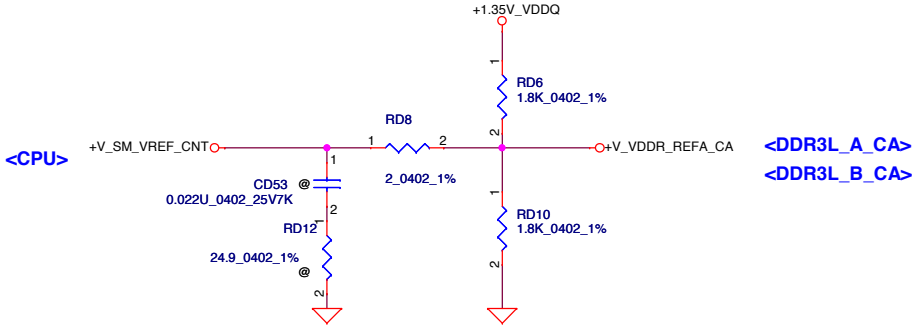
<11,15,16,34,4,49> +1.35V_VDDQ → +1.35V_VDDQ
<15,16> +V_VDDR_REFA_CA → +V_VDDR_REFA_CA
<5> +V_SM_VREF_CNT → +V_SM_VREF_CNT
<5> +V_DDR_REFA_R → +V_DDR_REFA_R
<15> +V_VDDR_REFA_DQ → +V_VDDR_REFA_DQ
<16> +V_VDDR_REFB_DQ → +V_VDDR_REFB_DQ

DDR3L VREF





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Compal Electronics, Inc.

Title: DDR3L VREF

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JPHW3 need to short

+3VS 80mil @ JPHW3 80mil +3VS_RT

JUMP_43X79

Layout notes
CT16~CT18 Close to Pin3

+DP_V33

10U_0603_6.3V6M CT16 0.1U_0402_16V4Z CT17 0.1U_0402_16V4Z CT18

LVDS@ LVDS@ LVDS@

Layout notes
Close to LT5 Pin18 Pin13

+SWR_VDD

10U_0603_6.3V6M CT77 0.1U_0402_16V4Z CT78 22U_0603_6.3V6M CT79 0.1U_0402_16V4Z CT10 0.1U_0402_16V4Z CT11

LVDS@ LVDS@ LVDS@ LVDS@ LVDS@

Layout notes
Close to Pin11 Pin27 Pin7

+SWR_V12

10U_0603_6.3V6M CT12 0.1U_0402_16V4Z CT13 0.1U_0402_16V4Z CT14 0.1U_0402_16V4Z CT15

LVDS@ LVDS@ LVDS@ LVDS@

<12,15,16,19,20,21,22,23,24,25,27,31,32,33,34,35,36,37,56,6,7,8,9> +3VS +3VS

<19,34> +LCDVDD +LCDVDD

※ROM only mode : PIN 30 4.7k pull low, Pin 31 4.7k pull high.
EP mode : PIN 30 4.7k pull high, Pin 31 4.7k pull low.
EEPROM : PIN 30 4.7k pull high, Pin 31 4.7k pull high.
〈 ※Default mode 〉

+3VS_RT 2132S@ RT2 4.7K_0402_5% MIIC_SDA PIN30

+3VS_RT LVDS@ RT3 4.7K_0402_5% MIIC_SCL 2132S@ RT5 4.7K_0402_5% LVDS@ RT4 4.7K_0402_5% PIN31

SWR / LDO Mode select

	LDO	SWR
2132S	Do not support	mount LT7
2132N	Use 0 ohm	mount LT7

※ If use 2132N, please select LDO mode as default.

+3VS_RT LVDS@ LT6 FBMA-L11-201209-221LMA30T_0805 +DP_V33 40mil 3

80mil LVDS@ LT5 FBMA-L11-201209-221LMA30T_0805 +SWR_VDD 100mil 13 40mil 18

+SWR_V12 LT7 @ 0_1206_5% +SWR_LX 40mil 12 40mil 11 40mil 27 40mil 7

<SI> LT7 change to 0 ohm short pad
use LDO mode translator only

UT1 RTD2132S

Power: DP_V33, SWR_VDD, PVCC, SWR_LX, SWR_VCCK, VCCK, DP_V12

LVDS: TXEC+/TXEC- LVDS_CLKP/LVDS_CLKN; TXE2+/TXE2- LVDS_TXP2/LVDS_TXN2; TXE1+/TXE1- LVDS_TXP1/LVDS_TXN1; TXE0+/TXE0- LVDS_TXP0/LVDS_TXN0

<CONN>

LVDS_CLKP <19> LVDS_CLKN <19>

LVDS_TXP0 <19> LVDS_TXN0 <19>

DP-IN: AUX_P/AUX_N EDP_CPU_AUX/EDP_CPU_AUX#; LANE0P/LANE0N EDP_CPU_LANE_P0/EDP_CPU_LANE_N0

GPIO: GPIO(PWM OUT) DP_INT_PWM; GPIO(Panel_VCC) +DP_ENVDD; GPIO(PWM IN) BKL_PWM_CPU; GPIO(BL_EN) TS_BKOFF#

DP_INT_PWM <19> +DP_ENVDD <19> BKL_PWM_CPU <19,8>

<CONN> <CPU>

Other: CIICSCL1/CIICSDA1; HPD; DP_REXT; DP_GND; GND

LVDS EDID: MIICSCL1/MIICSDA1 LCD_EDID_CLK/LCD_EDID_DATA

ROM: MIICSCL0/MIICSDA0 MIIC_SCL/MIIC_SDA

RTD2132N-CG QFN32
SA00007A300

<CPU CTRL>

<8> EDP_HPD EDP_HPD LVDS@ RT192 1K_0402_1% RT11 100K_0402_5% RT8 12K_0402_1% LVDS@

Layout notes
RT8 close to pin8

LCD_EDID_CLK RT6 LVDS@ 4.7K_0402_5% +3VS_RT

LCD_EDID_DATA RT7 LVDS@ 4.7K_0402_5%

	PIN15
2132S	TL_ENVDD
2132R	+LCD_VDD *

* Version R internal Power Switch, can output 1A, Rds(on)=0.2 ohm

PIN16	Accept voltage input (high level)
2132S	3.3V
2132R	1.5~3.3V

* Version R has internal level shifter, remove level shifter circuit on AMD platform

RTD2132 SMBus revrse to PCH

<21,25,36,7> EC_SMB_CK2 RT193 0_0201_5% CIICSCL1
<21,25,36,7> EC_SMB_DA2 RT194 0_0201_5% CIICSDA1
<15,16,21,6,7> PCH_SMBCLK RT195 0_0201_5%
<15,16,21,6,7> PCH_SMBDATA RT196 0_0201_5%

Layout notes
CC97~CC102 must closed to connector

<CPU>

<4> EDP_CPU_AUX_C CC102 .1U_0402_16V7K EDP_CPU_AUX
<4> EDP_CPU_AUX#_C CC101 .1U_0402_16V7K EDP_CPU_AUX#
<4> EDP_CPU_LANE_P0_C CC98 .1U_0402_16V7K EDP_CPU_LANE_P0
<4> EDP_CPU_LANE_N0_C CC97 .1U_0402_16V7K EDP_CPU_LANE_N0
<4> EDP_CPU_LANE_P1_C CC103 .1U_0402_16V7K EDP_CPU_LANE_P1 eDP@
<4> EDP_CPU_LANE_N1_C CC100 .1U_0402_16V7K EDP_CPU_LANE_N1 eDP@

DB phase :
add eDP Lan1 for FHD
20141117

+DP_ENVDD RT9 0_0805_5% LVDS@ +LCDVDD

CT23 4.7U_0603_6.3V6K LVDS@ RT10 100K_0402_5% LVDS@

Layout notes
RT9 close to pin15
RT10 CT23 close to CONN
+DP_ENVDD 80mil trace width

EDP_HPD RT34 eDP@ 0_0201_5% EDP_HPD_PANEL EDP_HPD_PANEL <19>

Delete BKL_PWM_CPU and DP_INT_PWM
20141113

Different between 2132S and 2132R

2132S	2132R
1. Support SWR mode	1. Support LDO mode and SWR mode 2. Internal ROM 3. Support LCD_VDD(internal Power switch) 4. Integrates Level shifter

<CPU by PASS eDP>

0_0804_8P4R_5%

EDP_CPU_LANE_N0 EDP_CPU_LANE_P0 EDP_CPU_AUX EDP_CPU_AUX# RP6 eDP@ SD309000080

2

<eDP to connector>

RP9 eDP@ SD309000080

EDP_AUX EDP_AUX# EDP_LANE_N0 EDP_LANE_P0 LCD_CLK LCD_DATA LVDS_TXN2_LN0 LVDS_TXP2_LP0

LCD_CLK <19> LCD_DATA <19> LVDS_TXN2_LN0 <19> LVDS_TXP2_LP0 <19>

0_0804_8P4R_5%

4

Layout notes
RP6 RP9 RP10 must closed to connector

<RTS2132>
<EC CTRL>

<25> EC_BKOFF# EC_BKOFF# TS_BKOFF# UT3 TC7SH08FUF_SSOP5 LVDS@ RT12 100K_0402_5% LVDS@

RT14 @ 0_0402_5% CT24 @ 0.1U_0402_16V7K +3VS

RT15 eDP@ 0_0402_5%

EC_TS_BKOFF# <19>

<LVDS Panel>

PD 100K on LVDS page

EDP_CPU_LANE_P1 RT16 eDP@ 0_0402_5% LVDS_TXP1_LP1 LVDS_TXP1_LP1 <19>

EDP_CPU_LANE_N1 RT17 eDP@ 0_0402_5% LVDS_TXN1_LN1 LVDS_TXN1_LN1 <19>

LVDS_TXP1 RT18 LVDS@ 0_0402_5% LVDS_TXP1_LP1

LVDS_TXN1 RT19 LVDS@ 0_0402_5% LVDS_TXN1_LN1

DB phase :
add eDP Lan1 for FHD
20141117

Layout notes
RT16~RT19 must closed to connector

<LVDS to connector>

0_0804_8P4R_5%

LCD_EDID_CLK LCD_EDID_DATA LVDS_TXN2 LVDS_TXP2 LCD_CLK LCD_DATA LVDS_TXN2_LN0 LVDS_TXP2_LP0 RP10 LVDS@ SD309000080

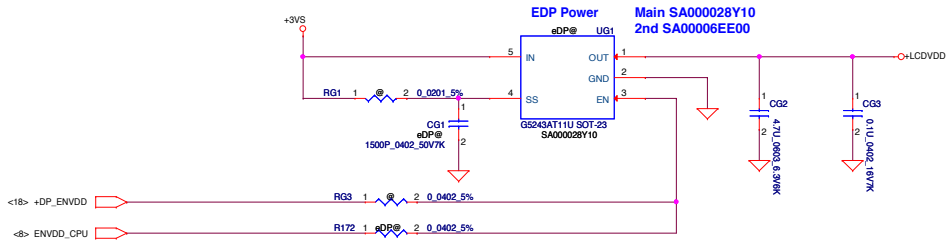
Security Classification	Compal Secret Data		
Issued Date	2013/3/1	Deciphered Date	2015/3/1

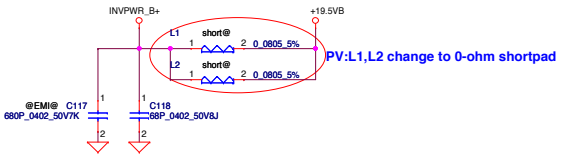
Compal Electronics, Inc.

Title: LVDS Translator-RTD2132N

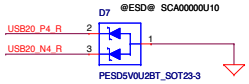
Size: Document Number: LA-C701P Rev: 0.1

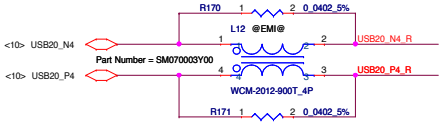
Date: Saturday, January 31, 2015 Sheet 18 of 61

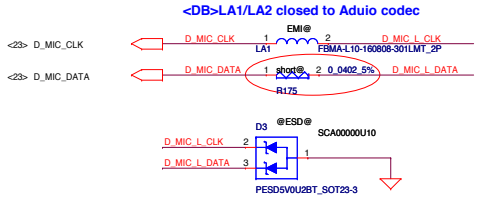




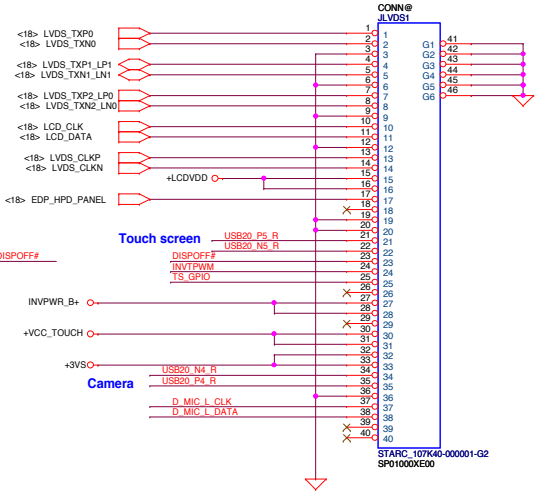
Camera



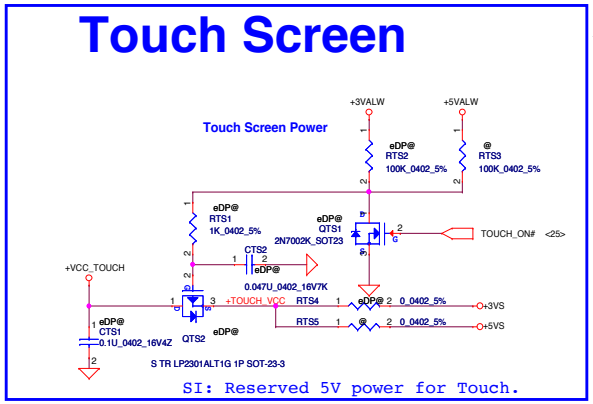


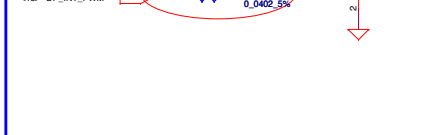


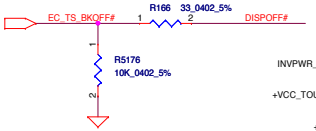
LCD/LED PANEL Conn.

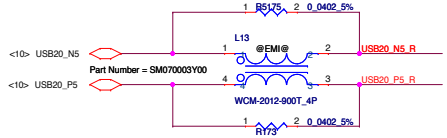


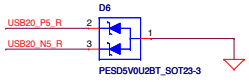
Touch Screen











Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

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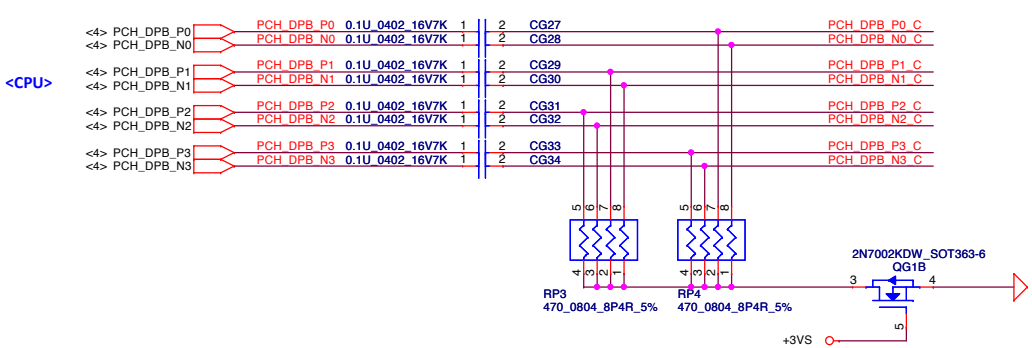
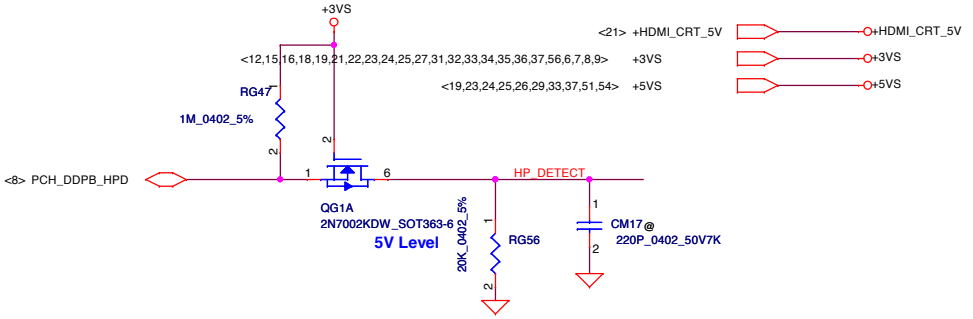
Compal Electronics, Inc.

Title: **LVDS Connector**

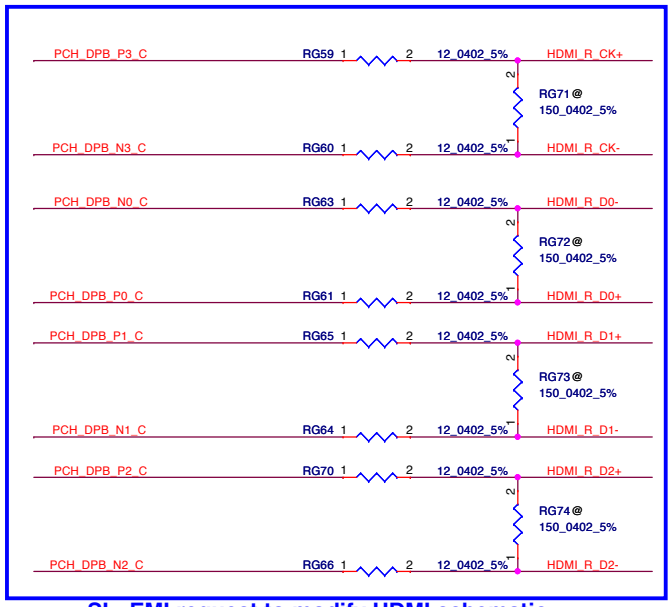
Size	Document Number	Rev
	LA-C701P	0.1

Date: Saturday, January 31, 2015 Sheet 19 of 61

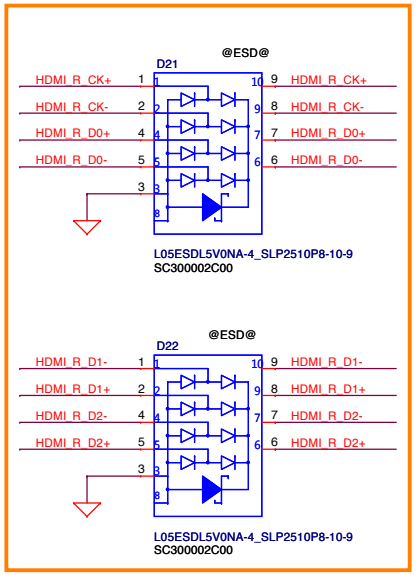


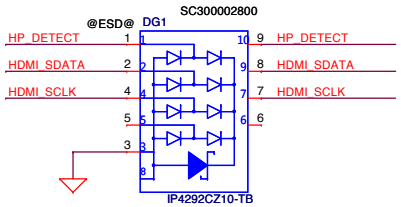


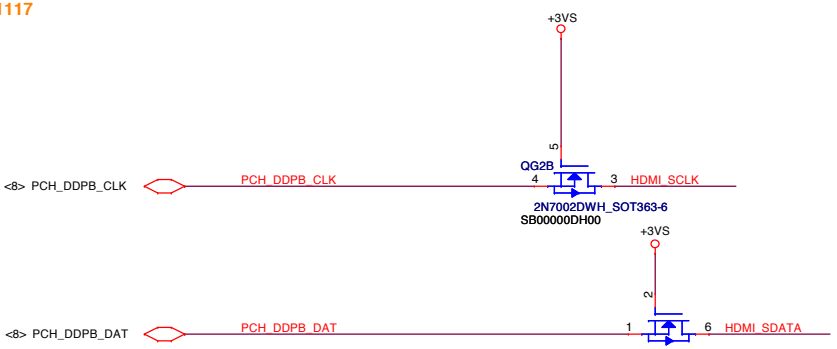
DB phase :
For ESD request
20141117

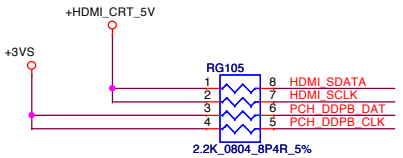


SI : EMI request to modify HDMI schematic.

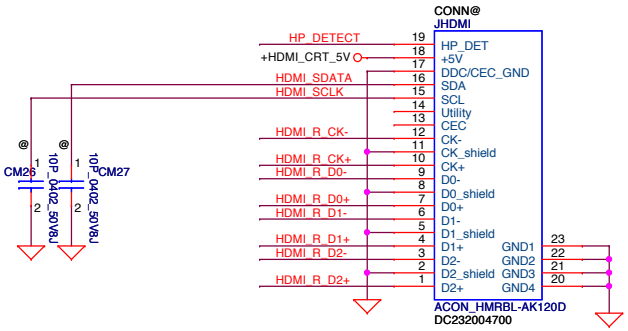






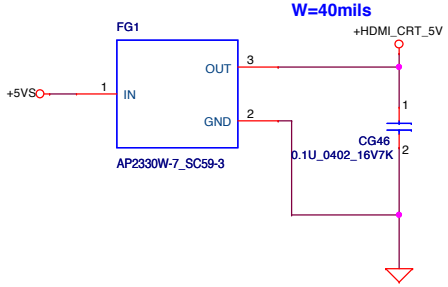


HDMI Conn.



Layout notes
40 mils

W=40mils



Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

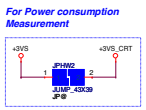
Compal Electronics, Inc.

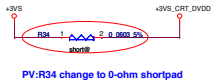
Title: **HDMI Conn/Level shift**

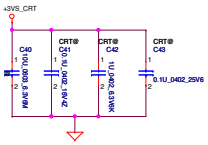
Size	Document Number	Rev
	LA-C701P	0.1

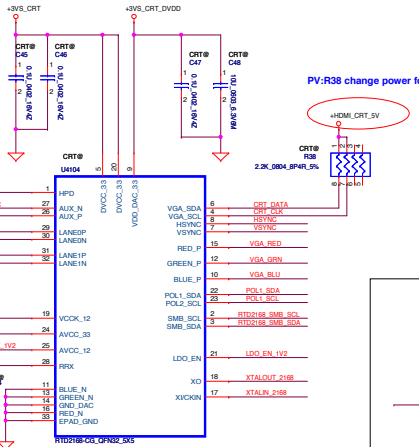
Date: Saturday, January 31, 2015 Sheet 20 of 61

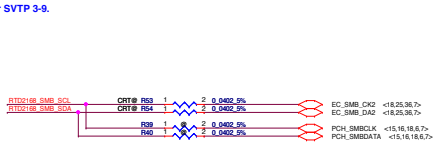
DP to CRT converter

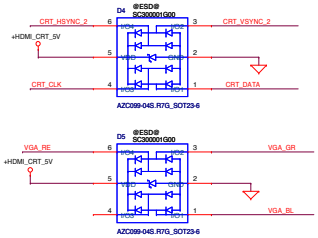




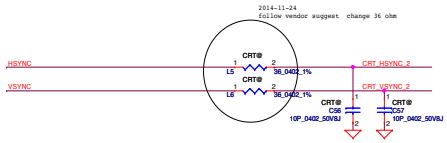




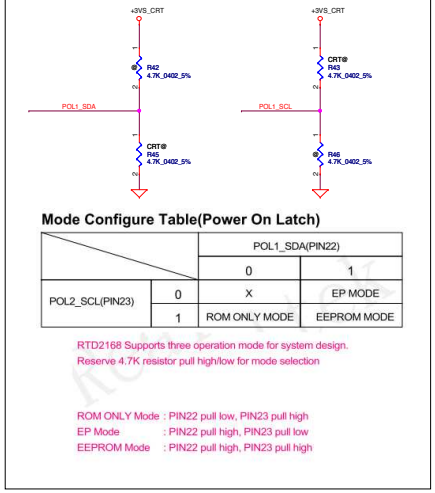




PV : Remove Buffer. 2015-01-27



Layout notes
R61,R62,R58,R59 close to RTD2168
R55,R57,R60,R56 close to CONN

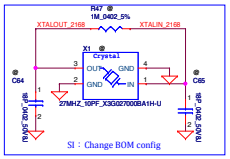


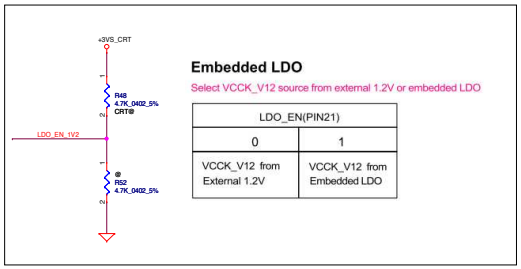
Mode Configure Table(Power On Latch)

		POL1_SDA(PIN22)	
		0	1
POL2_SCL(PIN23)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

RTD2168 Supports three operation mode for system design.
Reserve 4.7K resistor pull high/low for mode selection

ROM ONLY Mode : PIN22 pull low, PIN23 pull high
EP Mode : PIN22 pull high, PIN23 pull low
EEPROM Mode : PIN22 pull high, PIN23 pull high

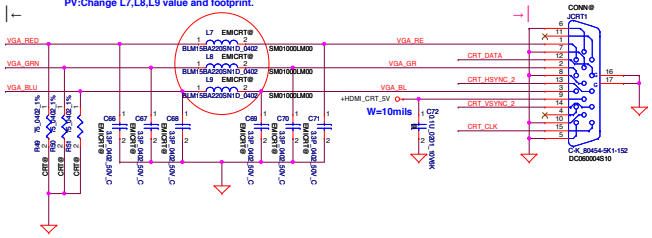




50 impedance

CRT Connector

PV:Change L7,L8,L9 value and footprint.



Security Classification	Compal Secret Data		
Issued Date	2014/02/18	Deciphered Date	2015/02/20

Compal Electronics, Inc.			
Title	DP to CRT RTD2168		
Size	Document Number		Rev
Custom	LA-C701P		0.1
Date: Saturday, January 31, 2015	Sheet 21 of 61		

JPHW1 need to short

+LAN_VDD_3V3 Rising time need>0.5mS and <100mS

Main SA000028Y10
2nd SA00006EE00
3rd SA00003AR00

SI phase :
change net name form +LAN_VDD_3V3 to +VDDREG
20141213

RTL8166EH (LDO mode)

	LDO mode	Switcing mode
LL1	@	@
CL2	@	@
LL2	@	SMT
CL3	@	SMT

RTL8166EH (LDO mode):
Pin3,22,24 is NC , Internal LDO output is Pin30.
Pin30 supply 1.05V to Pin8.

Layout notes
LL2, CL3, CL4 for Switcing mode
CL8 & CL18 close LL2
CL3,CL4 close LL2 pin2

Layout notes
Place CL5~CL6 close UL1 Pin 3 , 8
Place CL7 CL9 close UL1 Pin 22
Place CL8 CL11 close UL1 Pin 30

DB phase :
follow vender suggest reserve PU 10K to LAN_3V
20141117

Layout notes
CL15 & CL16 close to UL1: Pin 11,32
CL13 close to UL1: Pin 11
CL14 close to UL1: Pin 32

Layout notes
CL17 & CL18 close to UL1: Pin 23
Remove for NOT using SWR mode.

DB phase :
Reserve PU 10K by LAN vendor suggest
in CPU page
20141112

PV phase :
LL3,RL13 change to 0-ohm shortpad.
20150125

SI phase :
Need to pop LL3 for LAN 1V regout
20141213

SI：Change BOM config

Layout notes
+VDDREG=40mil
+LAN_VDD_3V3=40mil
+LAN_REGOUT=60mil

Layout notes
CR10,CR11 close UL1 Pin17,18

(SA000063500) 8166GSH 10/100 LDO mode
(SA000084T00) 8111HSH Giga switch mode

DB phase :
For ESD request
20141117

SP050005L00 Footprint

(SP050003P00) 10/100
(SP050006800) Giga

RJ-45 CONN.

Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

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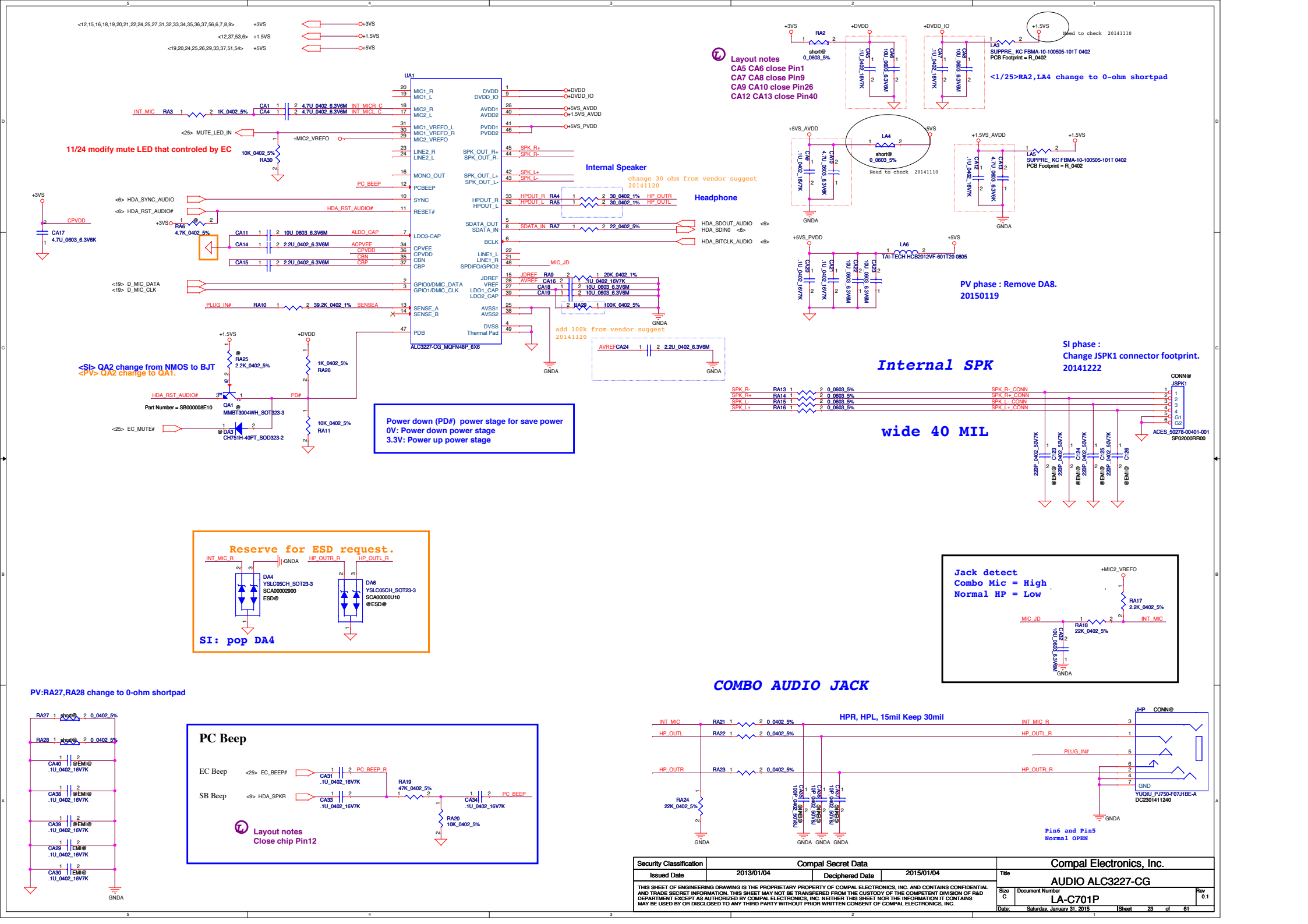
Compal Electronics, Inc.

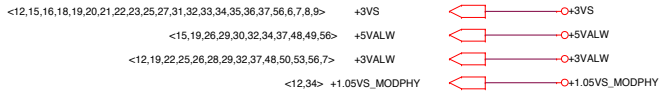
Title: LAN 8166G-EH 10/100

Size | Document Number: LA-C701P | Rev: 0.1

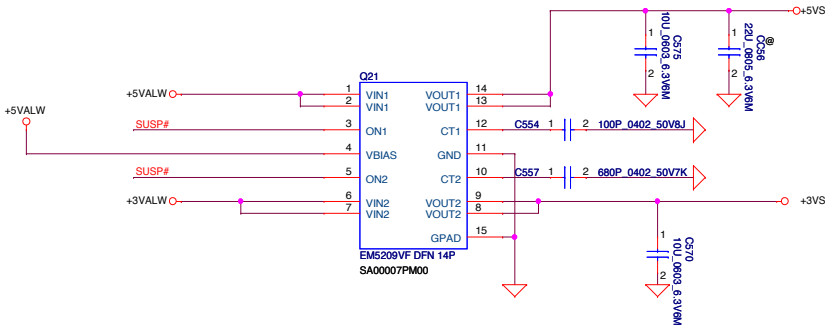
Date: Monday, February 02, 2015 | Sheet 22 of 61



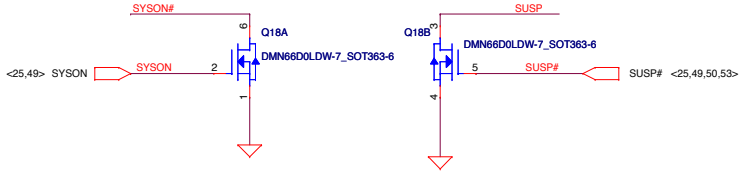
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/01/04	Deciphered Date	2015/01/04
Title	AUDIO ALC3227-CG		
Size C	Document Number LA-C701P		Rev 0.1
Date: Saturday, January 31, 2015	Sheet 23 of 61		

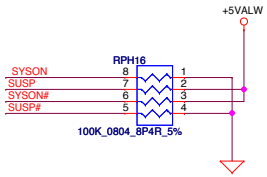


+5VALW TO +5VS

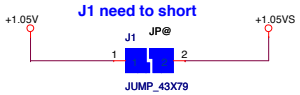


+3VALW TO +3VS

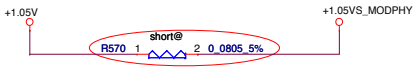




+1.05V TO +1.05VS

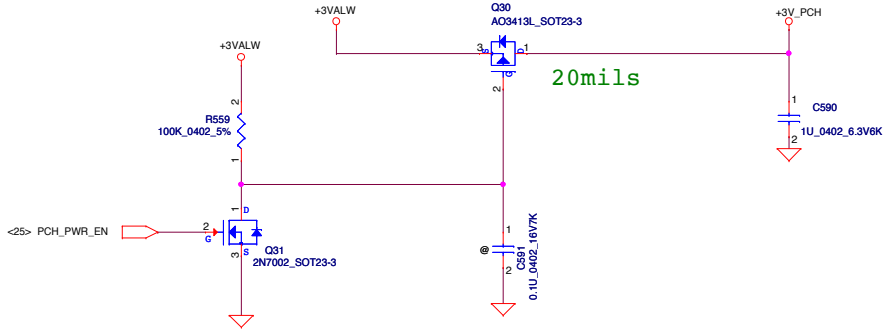


+1.05V TO +V1.05DX_MODPHY



PV:R570 change to 0-ohm shortpad

+3VALW TO +3V_PCH



Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
Custom	LA-C701P	0.1

Date: Saturday, January 31, 2015 | Sheet 24 of 61

15"	DB	SI	PV	MV
UMA RK4	0 ohm	15K ohm	27K ohm	43K ohm
DIS RK4	12k ohm	20k ohm	33k ohm	56k ohm

Board ID control

<DB>RK4 change to 12K ==>for 15" DIS

<DB>RK4 change to 0 ===>for 15" UMA

PV:RK1,RK3 change to 0-ohm shortpad

PV:R5178,RK8 change to 0-ohm shortpad

SI:EC_MUTE# change from 83 to 72.

SI:Add EC_SMB_CK3/DA3 for GPU.

SI:USB_ON# change from 84 to 86.

PV:RK22,RK9 change to 0-ohm shortpad

PV:RK6,RK15,RK16 change to 0-ohm shortpad

DB phase : 20141117

SI : Add RK27 for leakage of light

20mil

<PWR>

UK1 KB9022QD_LQFP128_14X14

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

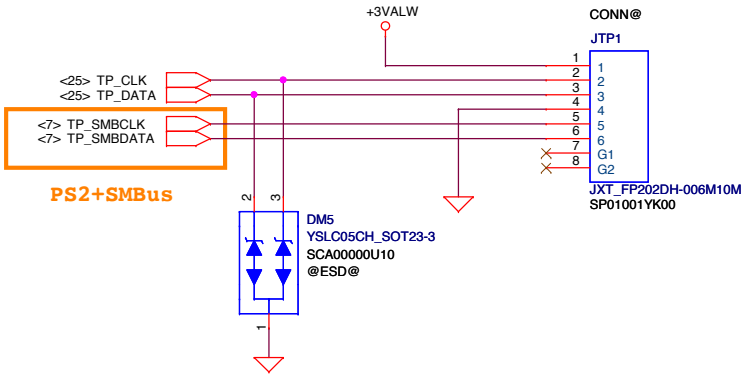
Compal Electronics, Inc.

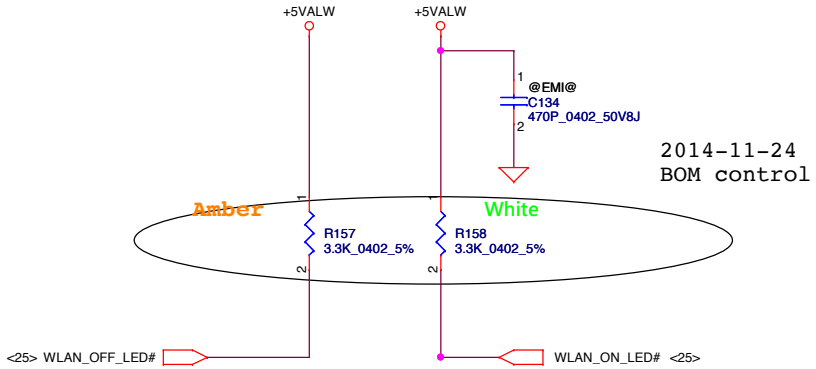
Title: EC ENE-KB9022

Size: Custom | Document Number: LA-C701P | Rev: 0.1

Date: Saturday, January 31, 2015 | Sheet 25 of 61

TP Button BD Connector

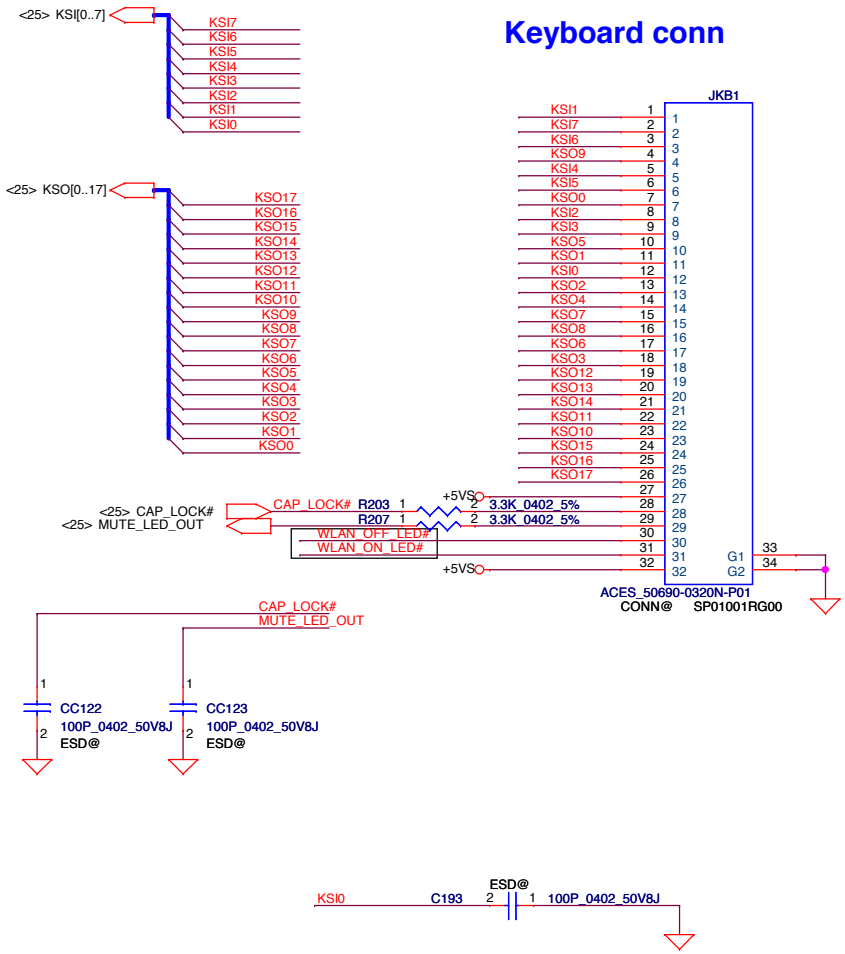




2014-11-24
BOM control

<12,19,22,24,25,28,29,32,37,48,50,53,56,7> +3VALW
<15,19,24,29,30,32,34,37,48,49,56> +5VALW

Keyboard conn



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/02/26	Deciphered Date	2015/07/08

Title	KB/TP		
Size B	Document Number LA-C701P		Rev 0.1
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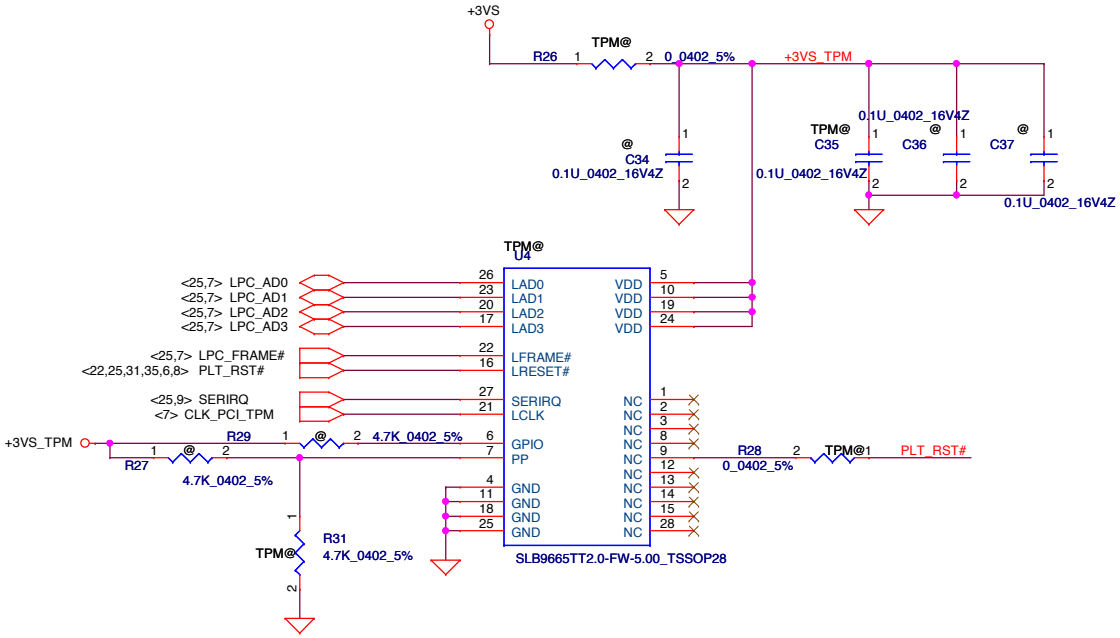
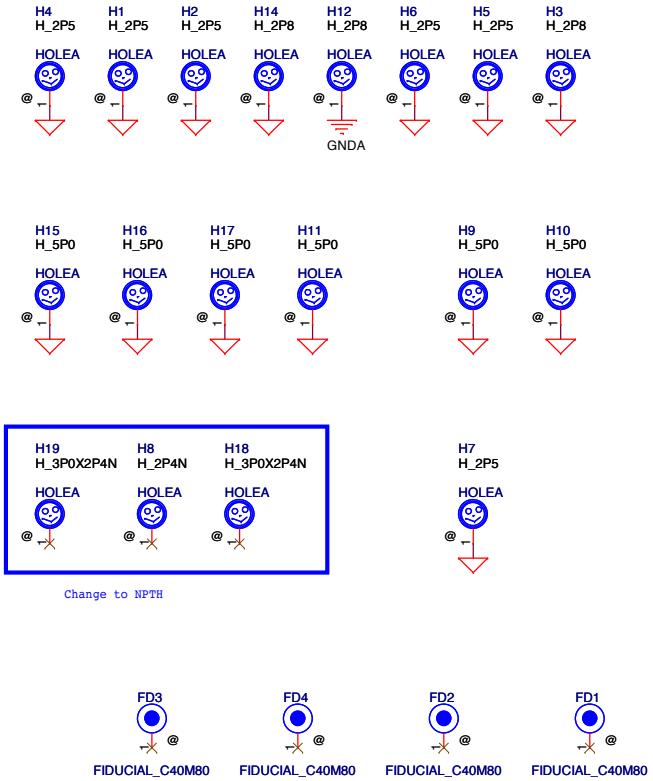
TPM2.0



SLB9665 (SA00007XU00)-->TPM2.0
SLB9660 (SA00007AB00) -->TPM1.2

Screw Hole



Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: **TPM/Screw**

Size	Document Number	Rev
	LA-C701P	0.1

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BOM control

Platform	Silego P/N	Compal PN	25MHz(A)	32.768KHz	24MHz(B)	27MHz	8MHz	Remark
Intel ULT UMA	SLG3NB3455VTR	SA00008IQ00	1	1	1	X	X	@
Intel ULT Dis	SLG3NB3456VTR	SA00008J800	1	1	1	1	X	DIS@

Base on A32 32.768KHz use 10ppm, G-CLK 25MHz X'TAL use 10ppm.

<36,37,38,56> +1.8VS_VGA → +1.8VS_VGA
<11,12,24,25,34,37,50,51> +1.05VS → +1.05VS
<22> +LAN_VDD_3V3 → +LAN_VDD_3V3
<25,32,46,47,48,6> +3VL → +3VL
<12,19,22,24,25,26,29,32,37,48,50,53,56,7> +3VALW → +3VALW
<6> +RTCBATT → +RTCBATT
<12,6,8> +RTCVCC → +RTCVCC

20141120 vendor recommend
1. AMD GPU power rail should be 1.8V, please modify +3VS_VGA to AMD GPU power rail.
2. CG47, CG48, CG49, CG50 and CG51 must placed close to UGCLK1.11, UGCLK1.3, UGCLK1.8, UGCLK1.15 and UGCLK1.2.
3. Please place RG114, RG109, RG111 and RG113 close to UGCLK1 for Impedance matching.
4. Modify RG114 Symbol from @ to GCLK@.
5. Change RG109 value from 33ohm to 10ohm.
6. We recommend to add RGxxx and RGyyy for isolated 32.768k and 24M clock tail.
7. We recommend to add CGxx, it is reserved for EMI.
8. We recommend to change CG54 Symbol from GCLK@ to @.

Depop if GCLK with UMA

+1.8VS_VGA: DIS@ CG47 0.1U_0402_10V7K
+1.05VS: DIS@ CG48 0.1U_0402_10V7K
+LAN_VDD_3V3: DIS@ CG49 0.1U_0402_10V7K
+3VL: DIS@ CG50 0.1U_0402_10V7K
+3VALW: DIS@ CG51 0.1U_0402_10V7K

Layout notes
CG47 Close UGCLK1.11
CG48 Close UGCLK1.13
CG49 Close UGCLK1.8
CG50 Close UGCLK1.15
CG41 Close UGCLK1.2

SI phase 20141225
Change YG1 PN to SJ10000FO00

S CRYSTAL 25MHZ 12PF +-10PPM RP25000099
SJ10000FO00
YG1 DIS@ (GND, OUT, IN, GND)
CLK_X2
CLK_X1
DIS@ CG59 12P_0402_50V8J
DIS@ CG58 15P_0402_50V8J

<SI> Change CG59 to 12pf , CG58 to 15pf recommend by vender

+RTCBATT
RG106 DIS@ 330_0402_5%
CG52 22U_0805_6.3V6M DIS@
+RTCVCC
RG107 @ 0_0402_5%
CG53 2.2U_0603_6.3V6K DIS@

DIS@ UGCLK1
VBAT, VDD_RTC_OUT, +V3.3A, VDD, 32kHz, VDDIO_27M, 27MHz, VDDIO_25M_A, 25MHz_A, VDDIO_25M_B, 25MHz_B, XTAL_IN, XTAL_OUT, GND1, GND2, GND3, GND4
GCLK_VRTC, RTC_VOUT
+3VL, +3VALW, +1.8VS_VGA, +LAN_VDD_3V3, +1.05VS, CLK_X1, CLK_X2

S IC SLG3NB3456VTR TQFN 16P CRYSTAL
SA00006J800

@ UGCLK1
SA00008IQ00
S IC SLG3NB3455VTR TQFN 16P CRYSTAL

20141120
add RG115 RG116 isolated GreenCLKtail from vendor suggest

PCH_RTCX1_R → DIS@ RG114 0_0402_5% → PCH_RTCX1_R_R → DIS@ RG115 0_0402_5% → PCH_RTCX1 <6>
VGA_X1_R → DIS@ RG109 10_0402_5% → XTALIN_R → DIS@ RG110 0_0402_5% → XTALIN <36>
LAN_X1_R → DIS@ RG111 33_0402_5% → XTLI_R → DIS@ RG112 0_0402_5% → XTLO_R <22>
PCH_X1_R → DIS@ RG113 0_0402_5% → PCH_X1_R_R → DIS@ RG116 0_0402_5% → CPU_XTAL24_IN <7>
CG54 5P_0402_50V8C @

<CPU> YC1 P6
<GPU> Y6 P37
<LAN> YL1 P22
<CPU> YC2 P7

Layout notes
Please place RG114, RG109, RG111 and RG113 close to UGCLK1 for Impedance matching.

Change RG109 to 10 ohm recommend by vender

Layout notes
For isolated GreenCLK tail
RG110 close to Y6 (27M for GPU)
RG112 close to YL1 (25M for LAN)
RG115 close to YC1 (32.768k for CPU)
RG116 close to YC2 (24M for CPU)

VGA_X1_R → CG57 5P_0402_50V8C @

Layout notes
Place CG57 between UGCLK1 and RG109
Reserve CG55 for vendor Place between UGCLK1 and RG113

PCH_X1_R → CG55 5P_0402_50V8C @

Security Classification	Compal Secret Data		
Issued Date	2013/06/10	Deciphered Date	2014/07/01

Compal Electronics, Inc.
Title: GCLK
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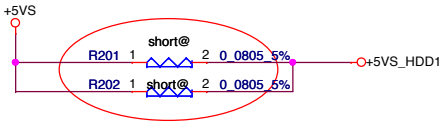
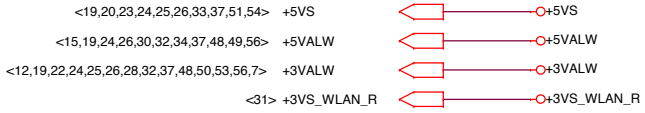
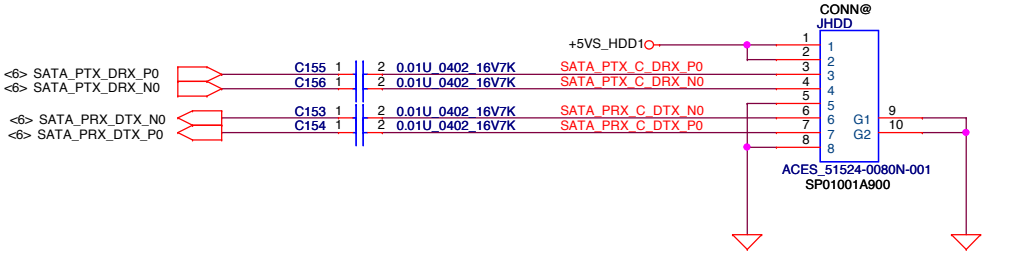
2.5" SATA HDD



HDD power on sub board.

PV : Change R201,R202 to 0-ohm shortpad.
20150125

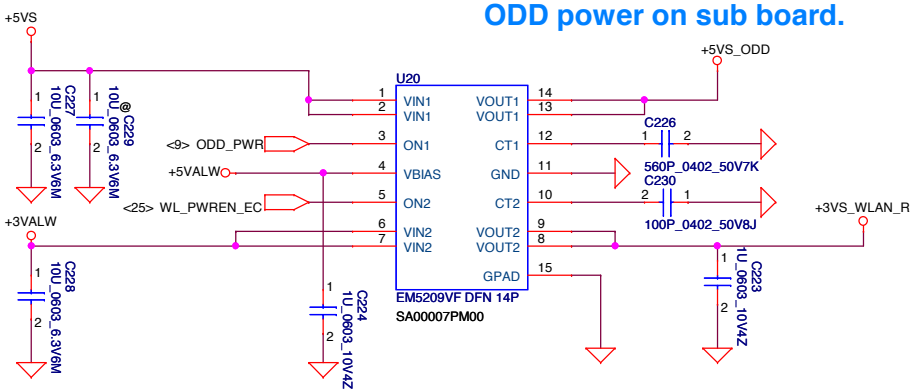


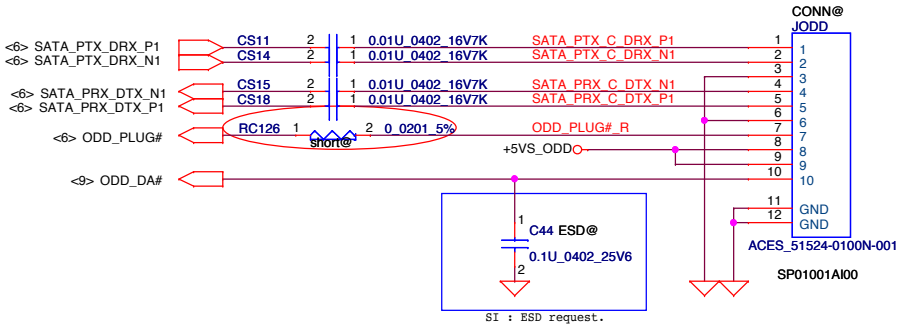


SI : Change HDD pin define.
Follow Cocoa. 12/25

2.5" SATA ODD

ODD power on sub board.





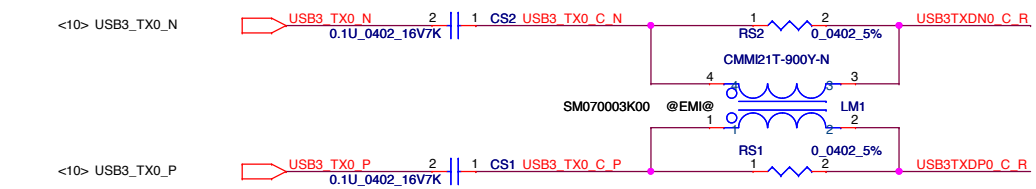
Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

Compal Electronics, Inc.

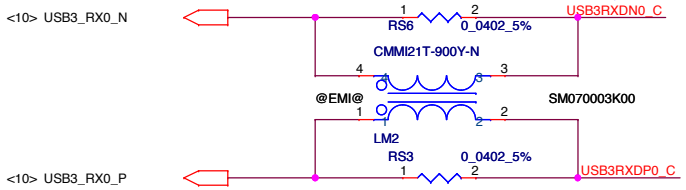
Title: HDD/ODD Conn

Size: B | Document Number: LA-C701P | Rev: 0.1

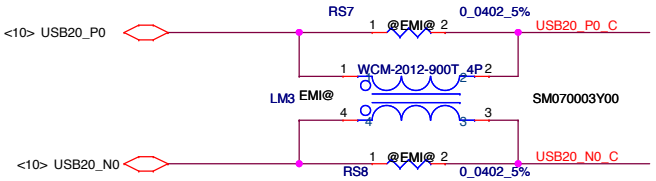
Date: Saturday, January 31, 2015 | Sheet 29 of 61

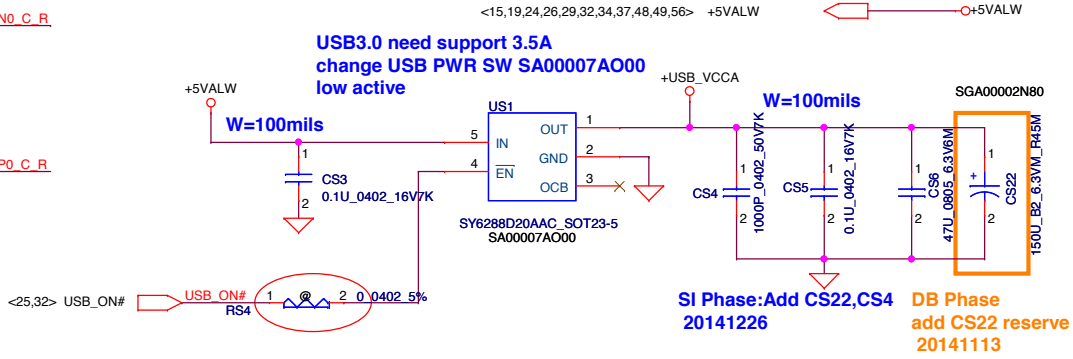


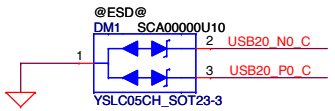
LM1,LM2 2nd : SM070003K00



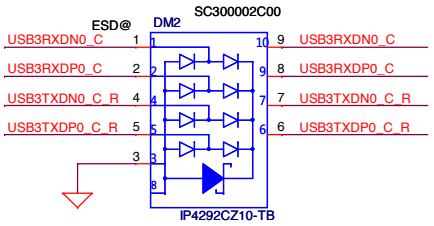
LM3 2nd : SM070002J00



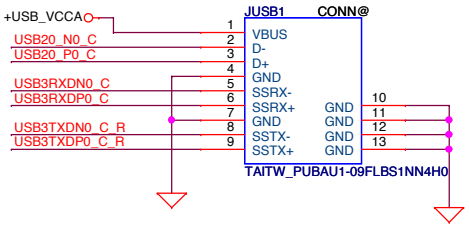




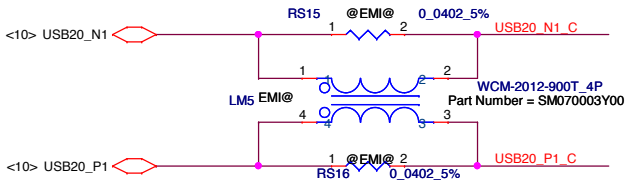
USB2.0/USB3.0 port 1



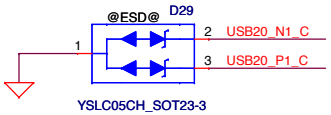
SI : pop DM2.

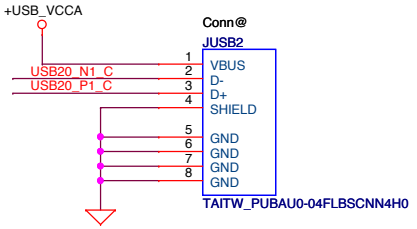


USB2.0 port x 1



LM5 2nd : SM070002J00





Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: USB 3.0/2.0 conn

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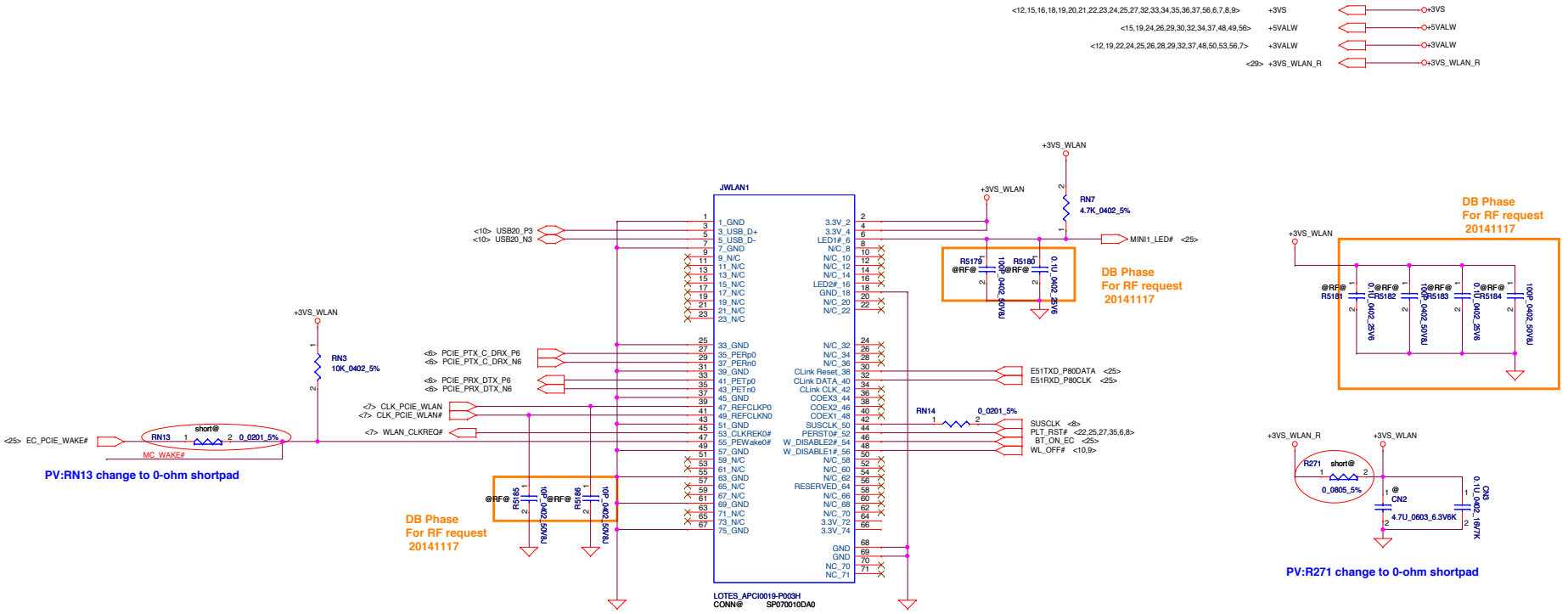
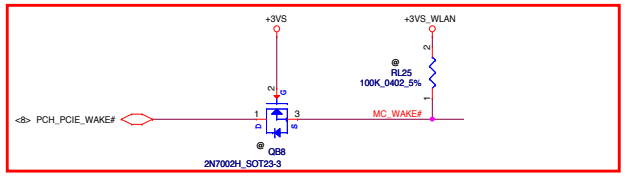


NGFF and WLAN



Unpop QB4 and RL23 for not support OBFF

Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: WLAN-BT

Size	Document Number	Rev
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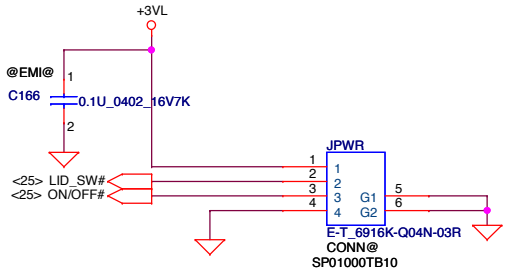
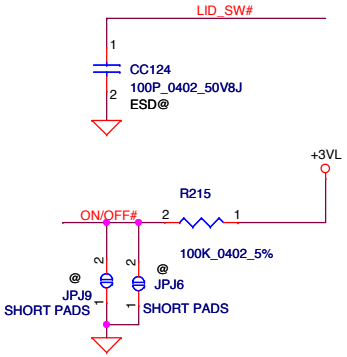
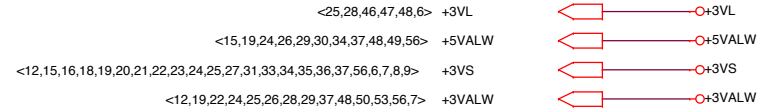
Powert Button Connector



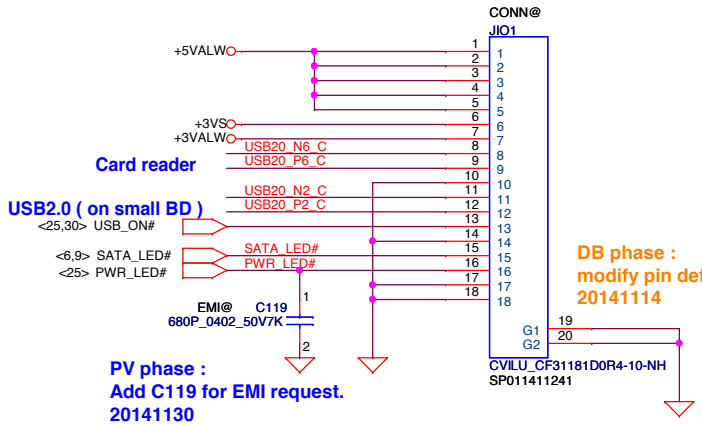


Layout notes
JPJ9 place Top layer,
JPJ6 place Bottom layer



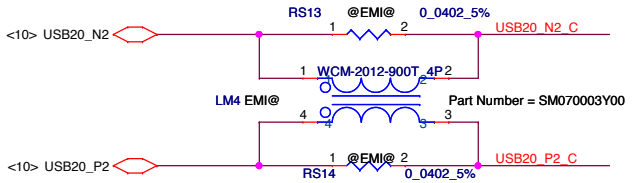
IO BD Connector (USB2.0,Card reader,HDD & PWR LED)

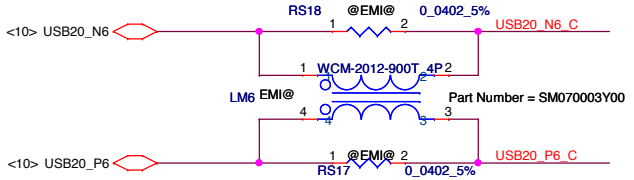
11/26 change CONN.



PV phase :
Add C119 for EMI request.
20141130

DB phase :
modify pin define
20141114





Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title	IO CON	
Size B	Document Number LA-C701P	Rev 0.1
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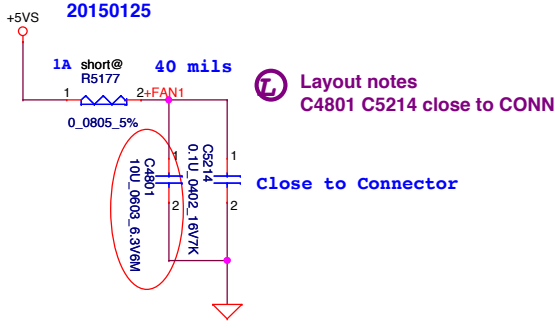
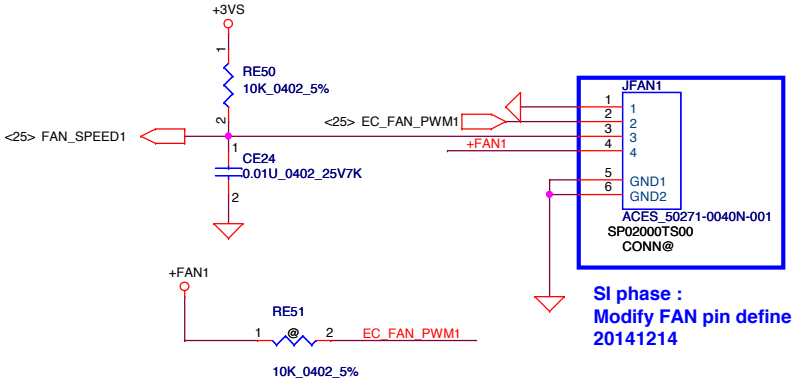
<12,15,16,18,19,20,21,22,23,24,25,27,31,32,34,35,36,37,56,6,7,8,9> +3VS

<19,20,23,24,25,26,29,37,51,54> +5VS

PV phase :
R5177 change to 0-ohm shortpad.
20150125





SI phase :
Modify FAN pin define
20141214

Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: FAN

Size	Document Number	Rev
B	LA-C701P	0.1

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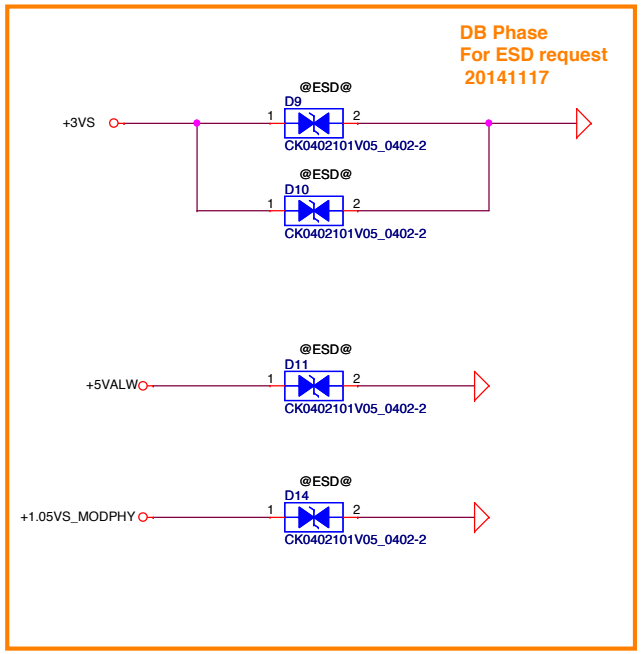
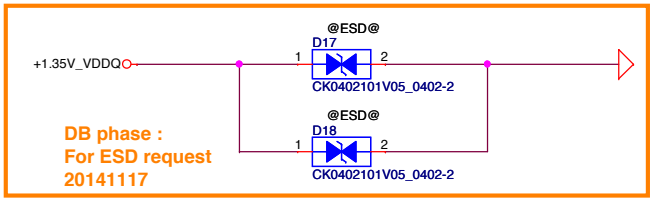
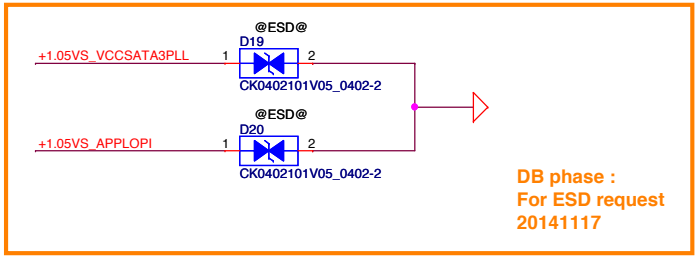
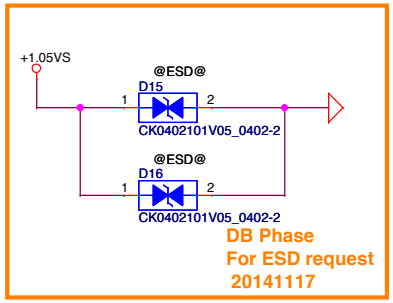
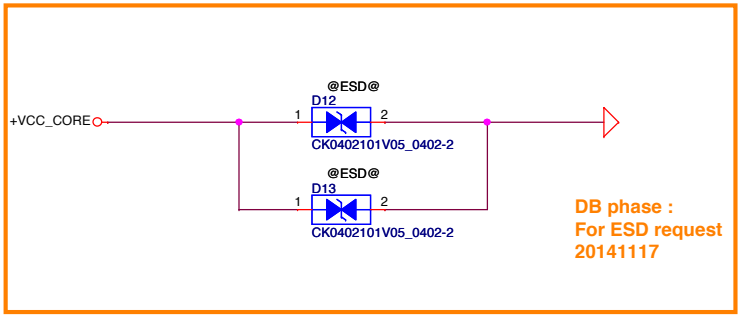
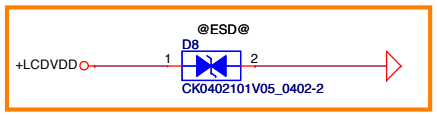












Security Classification	Compal Secret Data		
Issued Date	2013/3/1	Deciphered Date	2015/3/1

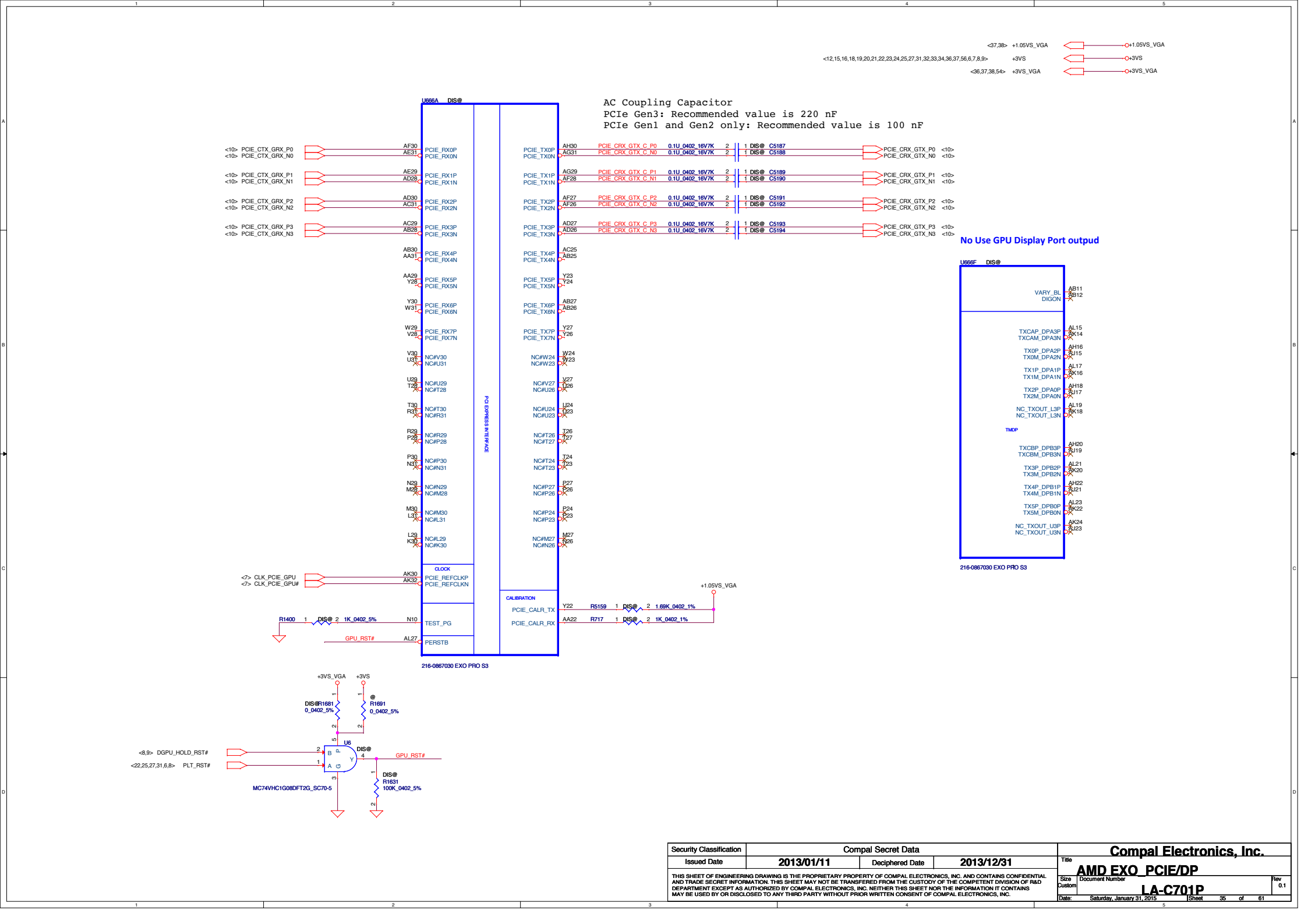
vinafix

Compal Electronics, Inc.

Title: *ESD RSVD*

Size: | Document Number: LA-C701P | Rev: 0.1

Date: Saturday, January 31, 2015 | Sheet 34 of 61


AC Coupling Capacitor
PCIe Gen3: Recommended value is 220 nF
PCIe Gen1 and Gen2 only: Recommended value is 100 nF
No Use GPU Display Port outpud
U666A DIS@
U666F DIS@
216-0867030 EXO PRO S3
PCI EXPRESS INTERFACE
CLOCK
CALIBRATION
TMDP
MC74VHC1G08DFT2G_SC70-5
+1.05VS_VGA
+3VS
+3VS_VGA
PCIE_CRX_GTX_C_P0
PCIE_CRX_GTX_C_N0
PCIE_CRX_GTX_C_P1
PCIE_CRX_GTX_C_N1
PCIE_CRX_GTX_C_P2
PCIE_CRX_GTX_C_N2
PCIE_CRX_GTX_C_P3
PCIE_CRX_GTX_C_N3
0.1U_0402_16V7K
C5187
C5188
C5189
C5190
C5191
C5192
C5193
C5194
R1400 1K_0402_5%
R5159 1.69K_0402_1%
R717 1K_0402_1%
R1681 0_0402_5%
R1691 0_0402_5%
R1631 100K_0402_5%
GPU_RST#
DGPU_HOLD_RST#
PLT_RST#
CLK_PCIE_GPU
CLK_PCIE_GPU#
Security Classification
Compal Secret Data
Issued Date
2013/01/11
Deciphered Date
2013/12/31
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Compal Electronics, Inc.
Title
AMD EXO_PCIE/DP
Size Custom
Document Number
LA-C701P
Rev 0.1
Date: Saturday, January 31, 2015
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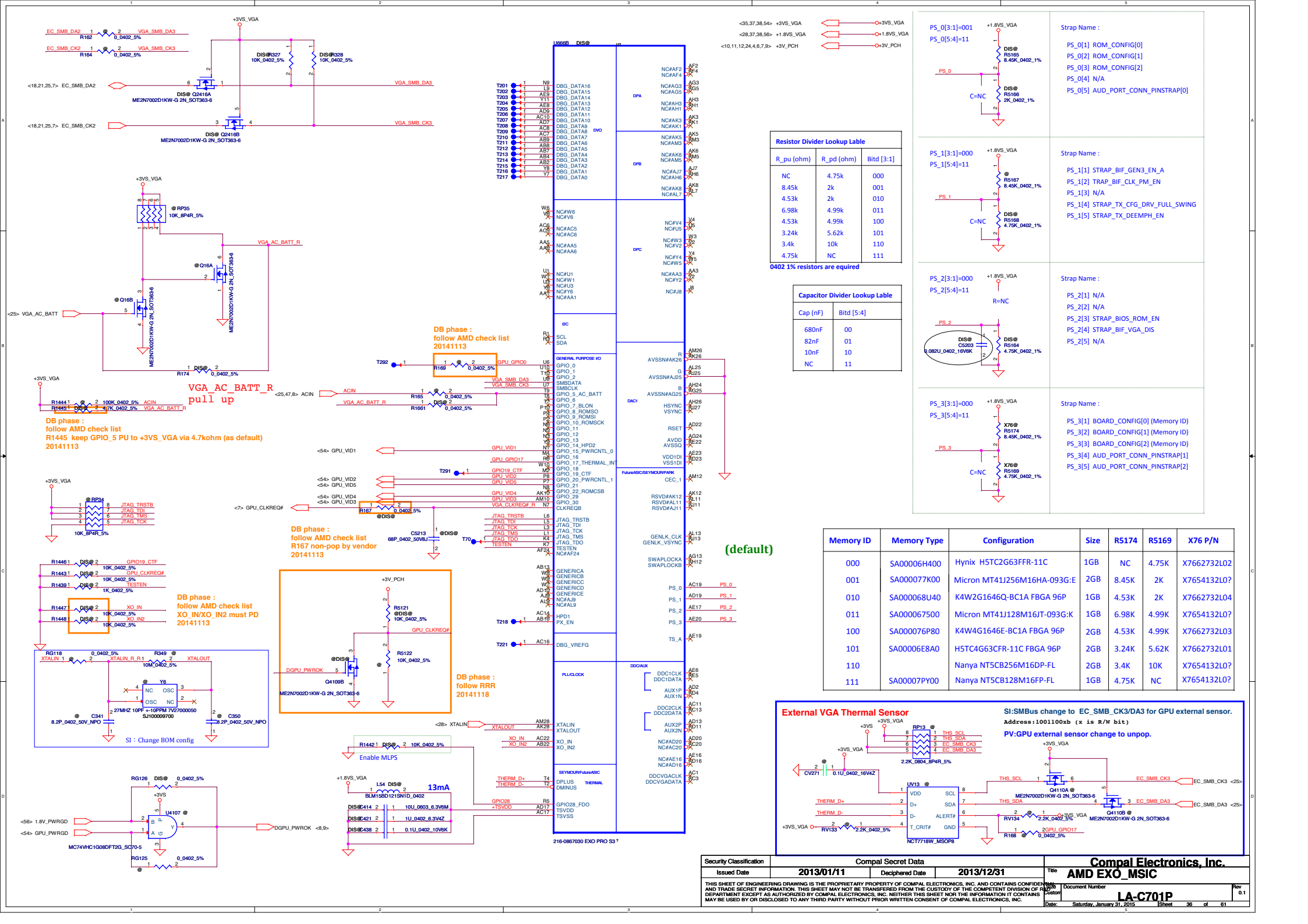

Memory ID	Memory Type	Configuration	Size	R5174	R5169	X76 P/N
000	SA00006H400	Hynix H5TC2G63FFR-11C	1GB	NC	4.75K	X7662732L02
001	SA000077K00	Micron MT41J256M16HA-093G:E	2GB	8.45K	2K	X7654132L0?
010	SA000068U40	K4W2G1646Q-BC1A FBGA 96P	1GB	4.53K	2K	X7662732L04
011	SA000067500	Micron MT41J128M16JT-093G:K	1GB	6.98K	4.99K	X7654132L0?
100	SA000076P80	K4W4G1646E-BC1A FBGA 96P	2GB	4.53K	4.99K	X7662732L03
101	SA00006E8A0	H5TC4G63CFR-11C FBGA 96P	2GB	3.24K	5.62K	X7662732L01
110		Nanya NT5CB256M16DP-FL	2GB	3.4K	10K	X7654132L0?
111	SA00007PY00	Nanya NT5CB128M16FP-FL	1GB	4.75K	NC	X7654132L0?

Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

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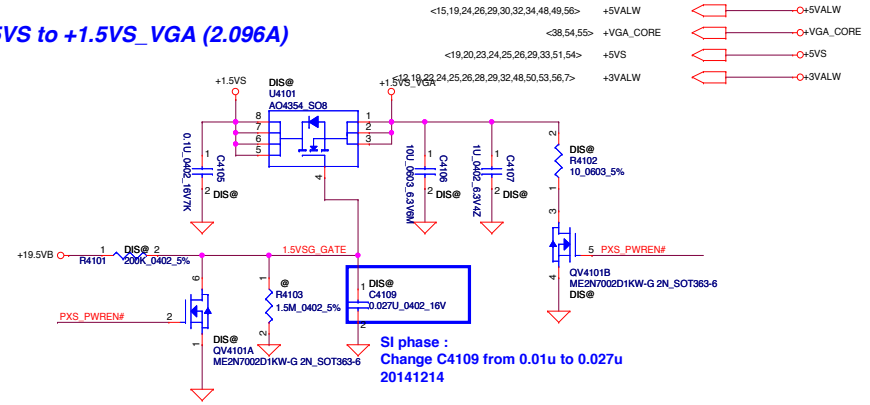
Compal Electronics, Inc.

Title: AMD EXO_MSIC

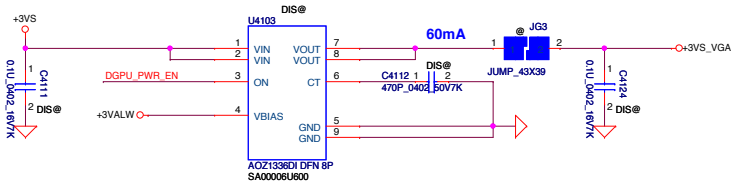
Size: B | Document Number: LA-C701P | Rev: 0.1

Date: Saturday, January 31, 2015 | Sheet 36 of 61

+1.5VS to +1.5VS_VGA (2.096A)

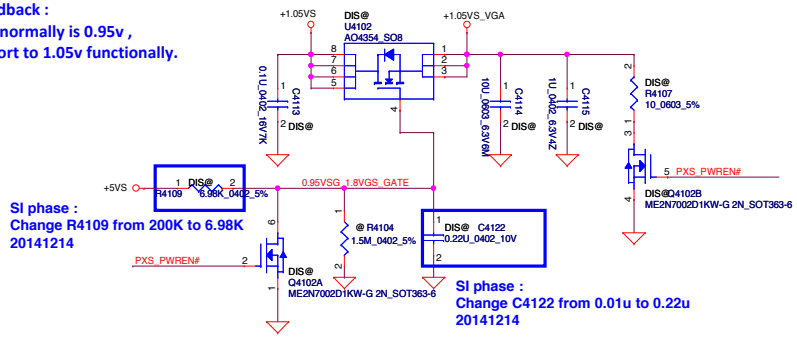


+3VS to +3VS_VGA (25mA)



+1.05VS to +1.05VS_VGA (2A)

AMD feedback :
Exo ASIC normally is 0.95v ,
can support to 1.05v functionally.



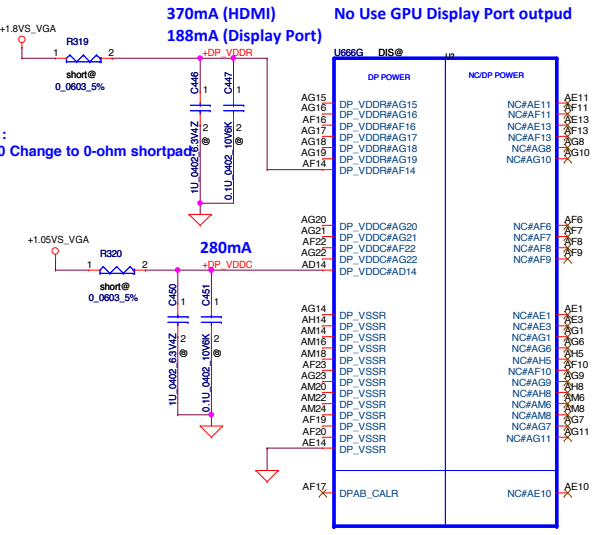
<56> 0.95VSG_1.8VGS_GATE

<15,19,24,26,29,30,32,34,48,49,56> +5VALW
<38,54,55> +VGA_CORE
<19,20,23,24,25,26,29,33,51,54> +5VS
<12,19,22,24,25,26,28,29,32,48,50,53,56,7> +3VALW

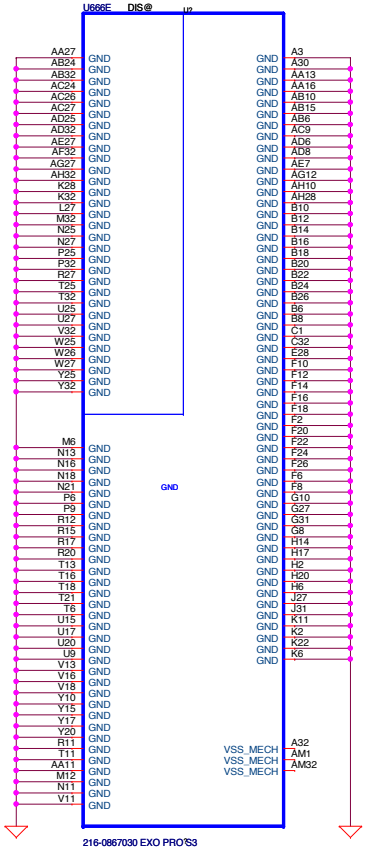
<12,23,53,6> +1.5VS
<38,39,40,41> +1.5VS_VGA
<12,15,16,18,19,20,21,22,23,24,25,27,31,32,33,34,35,36,56,6,7,8,9> +3VS
<35,36,38,54> +3VS_VGA

<11,12,24,25,28,34,50,51> +1.05VS
<35,38> +1.05VS_VGA
<19,47,48,49,51,53,54> +19.5VB

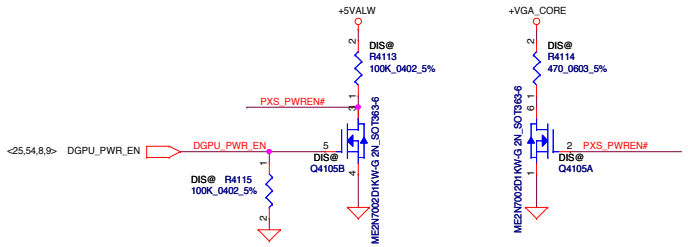
370mA (HDMI) / 188mA (Display Port) — No Use GPU Display Port outpud



PV phase :
R319,R320 Change to 0-ohm shortpads
20150125



+1.05VS_VGA (2A)



Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

Compal Electronics, Inc.

Title: AMD EXO_Power/GND

Size: Custom | Document Number: LA-C701P | Rev: 0.1

Date: Saturday, January 31, 2015 | Sheet 37 of 61

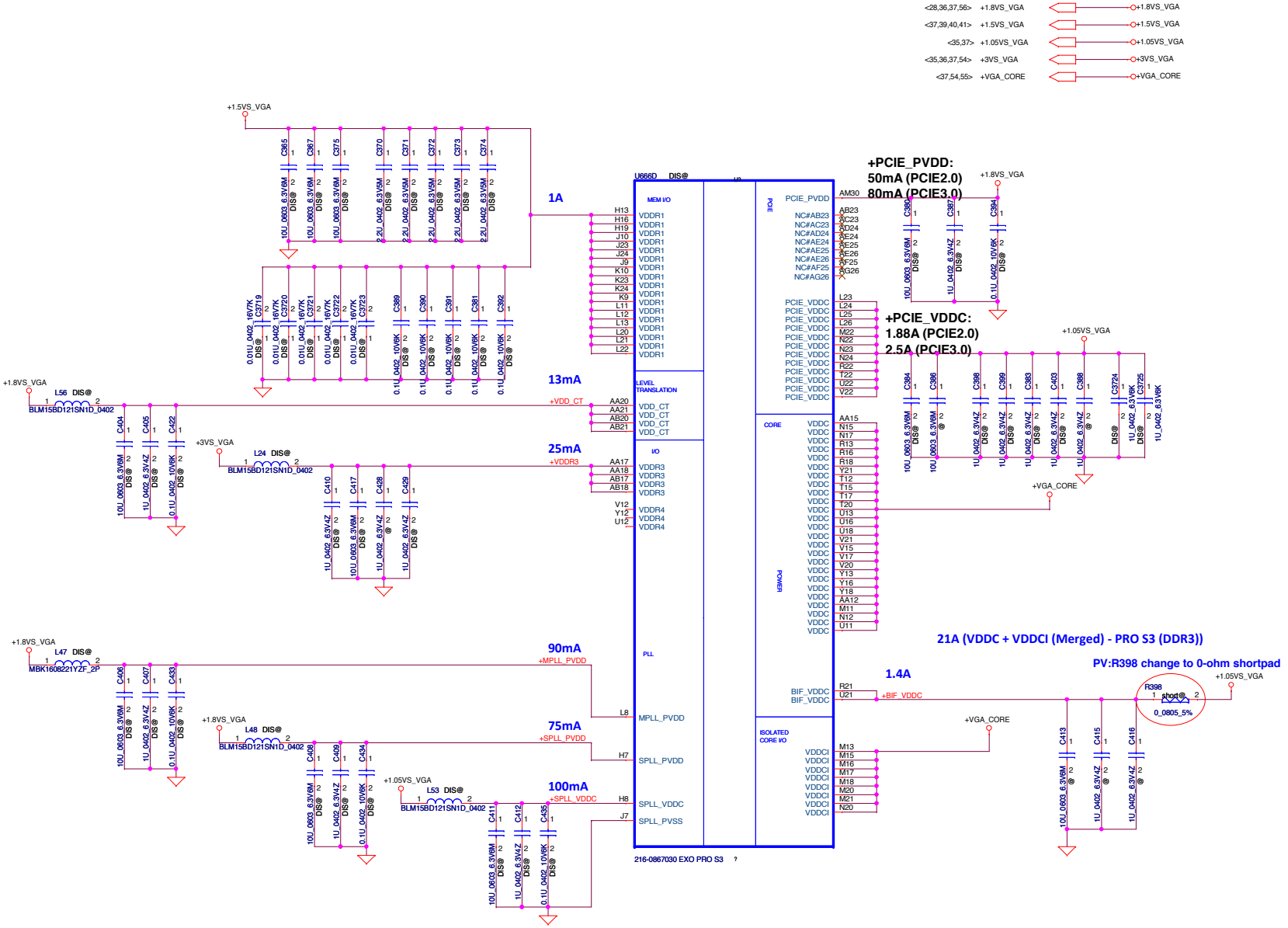
+VGA_CORE		10uF	1uF	0.1uF
VDDC	TBD	5 (1@)	10 (2@)	0
VDDCI	3.5A	1	3	0

+0.95VS_VGA		10uF	1uF	0.1uF
PCIE_VDDC	2.5A	2 (1@)	5 (1@)	0
BIF_VDDC	1.4A	0	0	0
SPLL_VDDC	100mA	1	1	1

+1.5VS_VGA		10uF	1uF	0.1uF
VDDR1	1.5A	3	5	5

+1.8VS_VGA		10uF	1uF	0.1uF
PCIE_PVDD	100mA	1	1	1
MPLL_PVDD	130mA	1	1	1
SPLL_PVDD	75mA	1	1	1
VDDR4	(300mA)	0	0	0
VDD_CT	13mA	1	1	1
+TSVDD	13mA	1	1	1
+DP_VDDR		0	0	0
+DP_VDDC		0	0	0

+3VS_VGA		10uF	1uF	0.1uF
VDDR3	25mA	0	2 (1@)	1



Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

Compal Electronics, Inc.

Title: AMD EXO_Power

Size: Custom | Document Number: LA-C701P | Rev: 0.1

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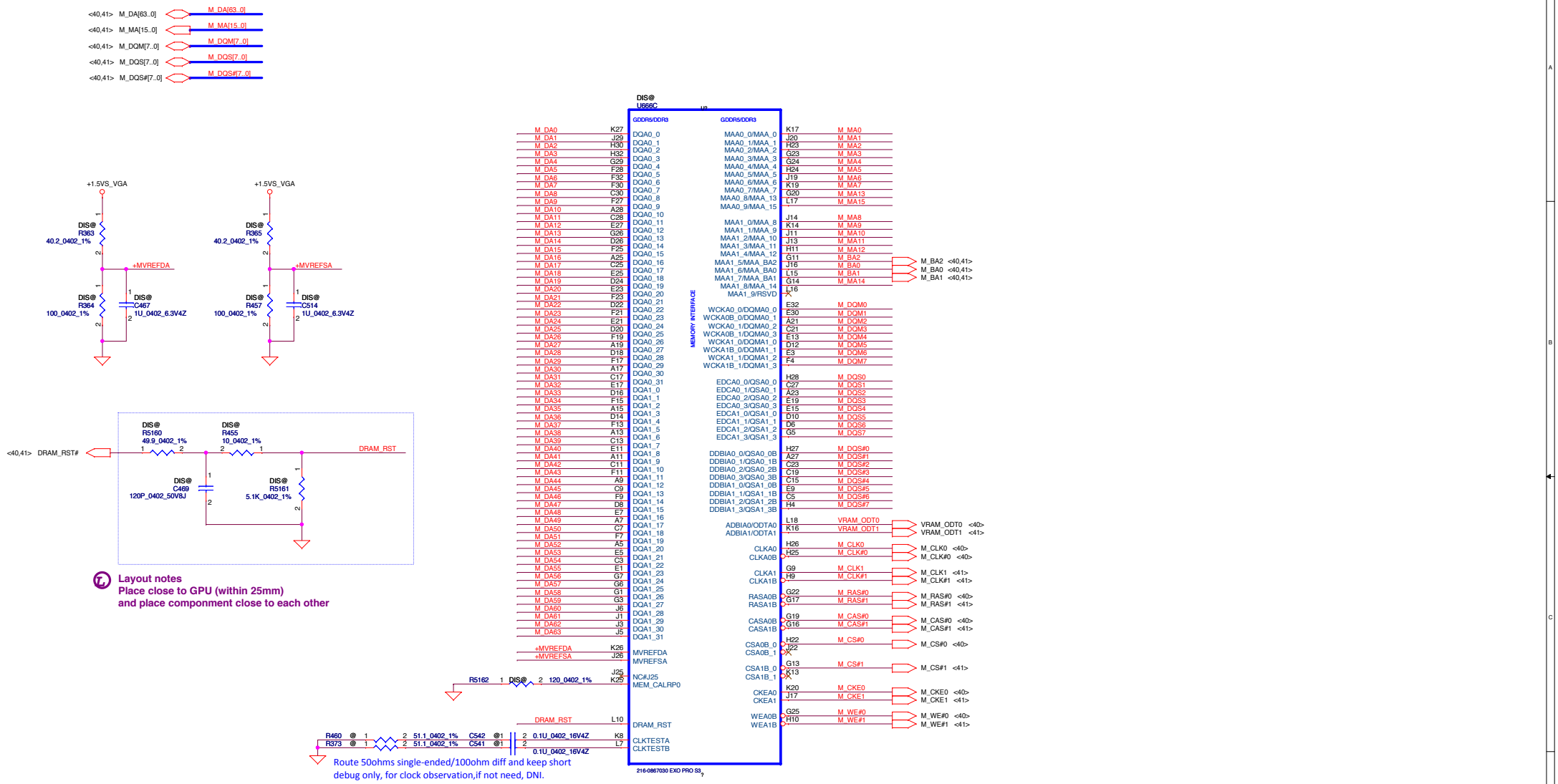

Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

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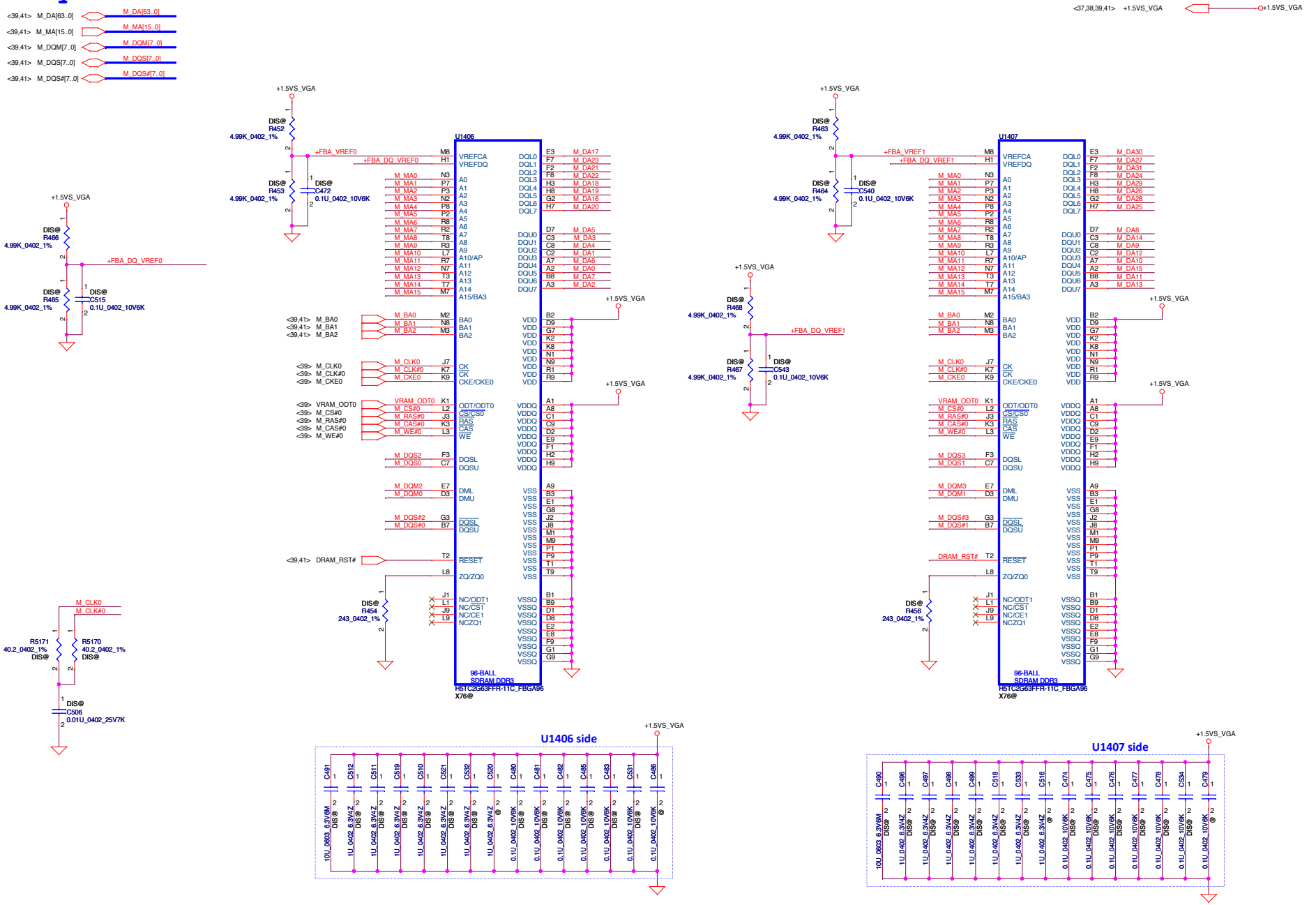
Compal Electronics, Inc.

Title	AMD EXO_MEM	
Size: Custom	Document Number: LA-C701P	Rev: 0.1
Date: Saturday, January 31, 2015	Sheet 39 of 61	

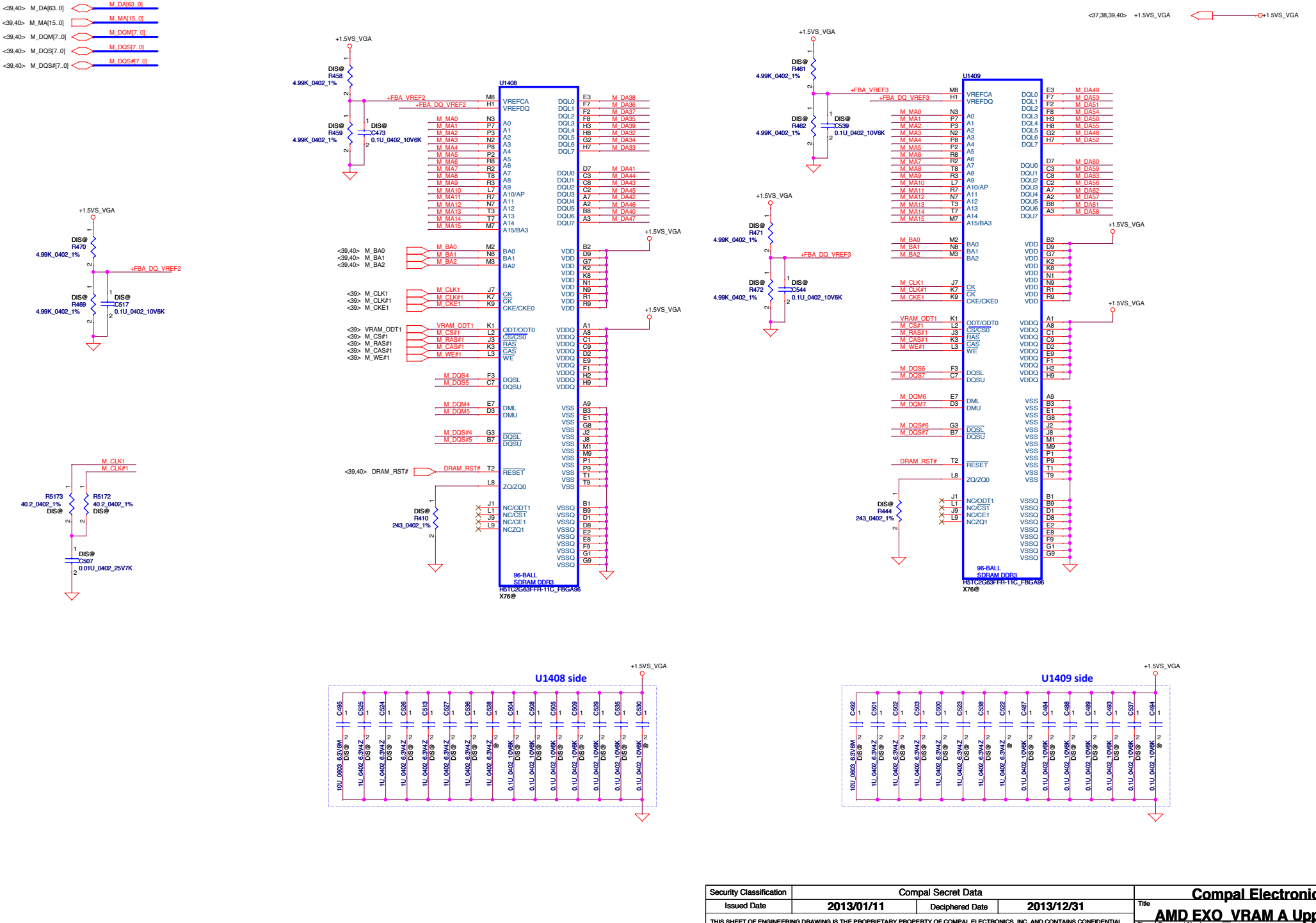
Memory Partition A - Lower 32 bits



Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

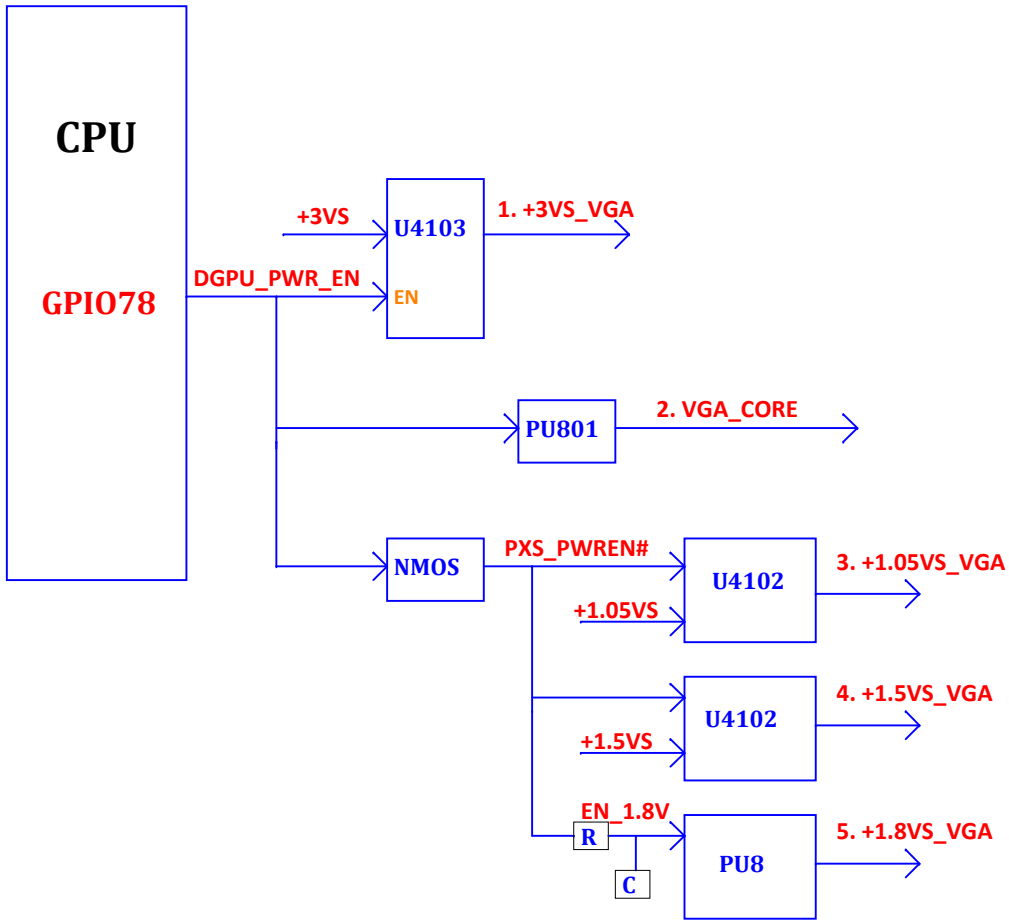
Compal Electronics, Inc.	
Title	AMD EXO_VRAM A Lower
Size: Custom	Document Number: LA-C701P
Rev	0.1
Date: Saturday, January 31, 2015	Sheet 40 of 61

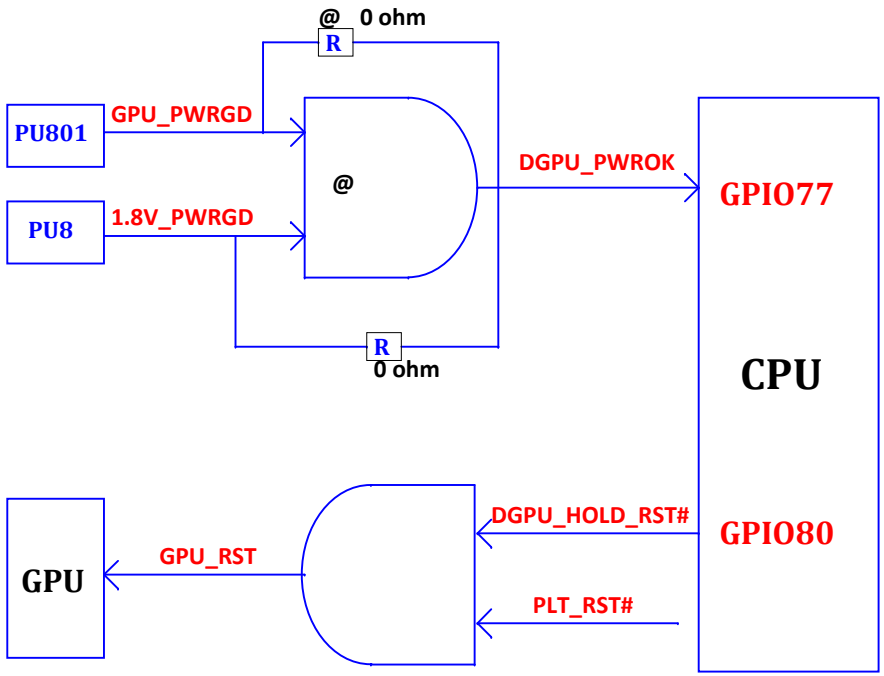
Memory Partition A - Upper 32 bits



Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

Compal Electronics, Inc.			
Title	AMD EXO_VRAM A Upper		
Size Custom	Document Number LA-C701P		Rev 0.1
Date: Saturday, January 31, 2015	Sheet 41 of 61		





Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: RSVD
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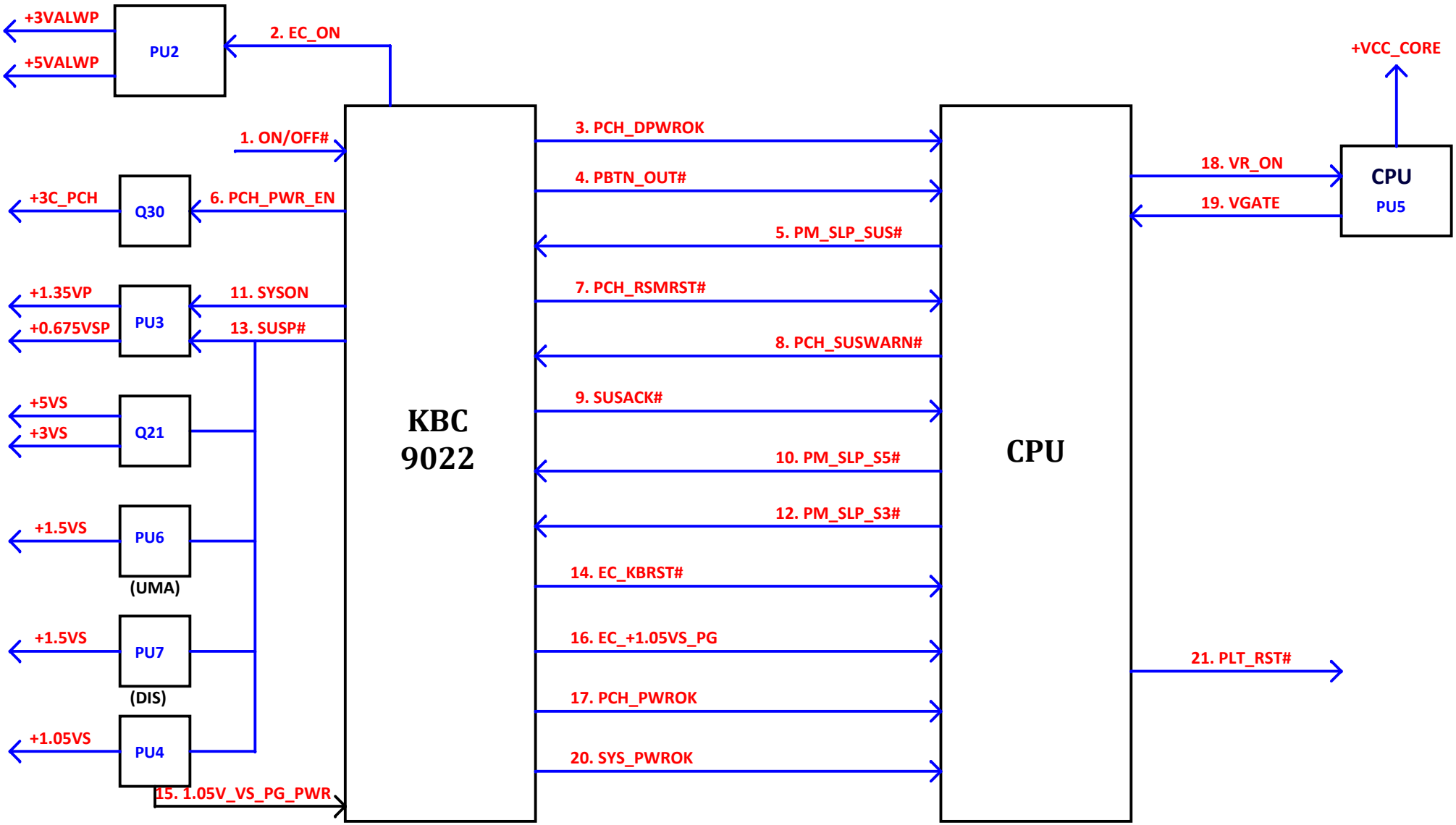
			Date: Saturday, January 31, 2015; Sheet 42 of 61



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: POWER SEQUENCE
Size: D	Document Number: LA-C701P		Rev: 0.1
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DB build CPU type

UCPU1
2.4G@
i7-5500U BDW
SA000089A00

UCPU1
2.0G@
i3-5005U BDW
SA000083E50

UCPU1
1.7G@
i3 4005U
SA000072Q80

ZZZ004
HY1@
1G Hynix
X7662732L02

ZZZ004
HY2@
2G Hynix
X7662732L01

ZZZ
DAX
DA6001DO000

ZZZ004
SAM2@
2G SAMSUNG
X7662732L03

ZZZ004
SAM1@
1G SAMSUNG
X7662732L04

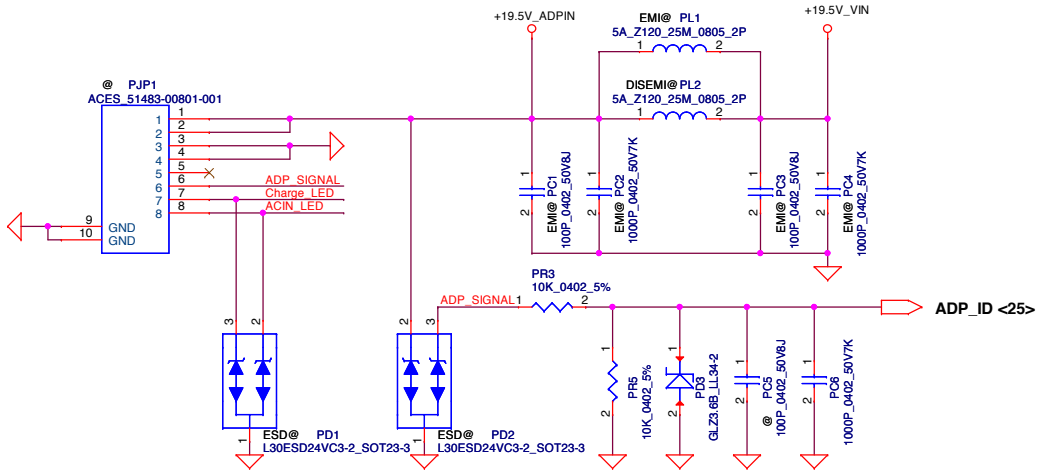
Security Classification	Compal Secret Data		
Issued Date	2013/3/1	Deciphered Date	2015/3/1

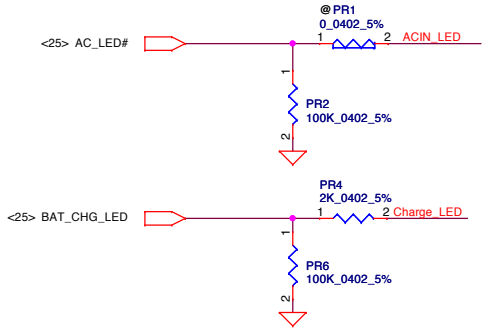
Compal Electronics, Inc.

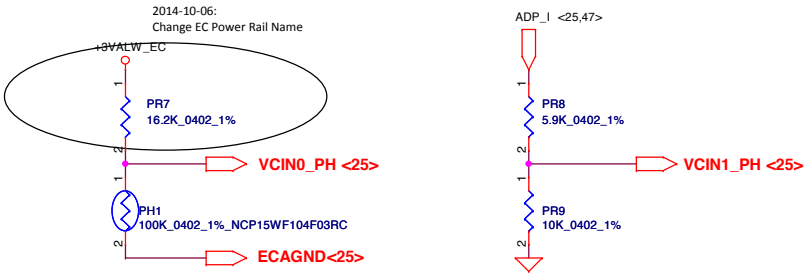
Title: ***BOM control***

Size | Document Number: **LA-C701P** | Rev: 0.1

Date: Saturday, January 31, 2015 | Sheet 44 of 61







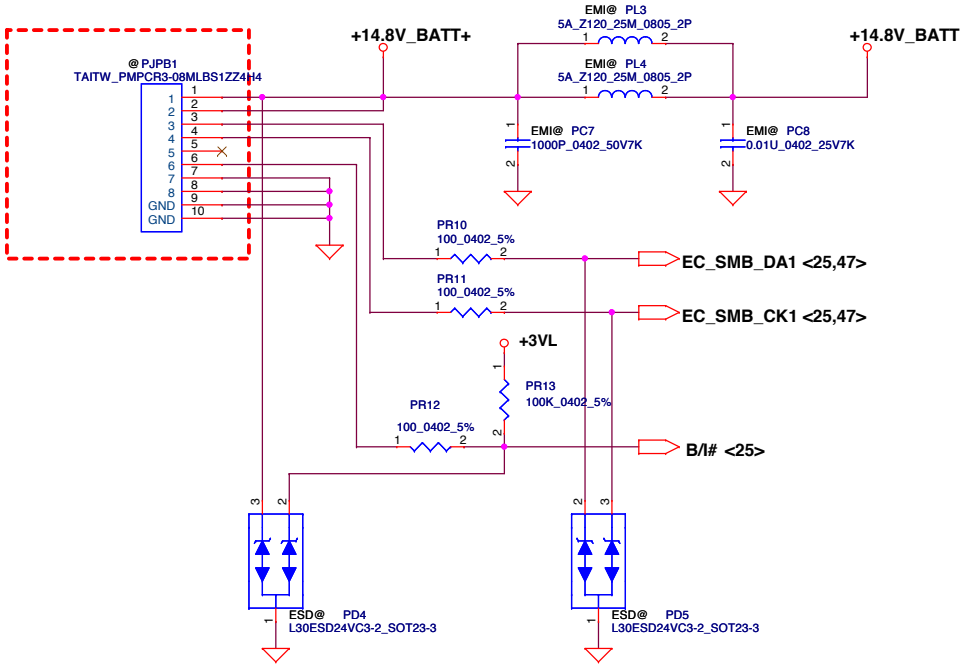
Security Classification	Compal Secret Data		
Issued Date	2014/10/09	Deciphered Date	2017/10/09

Compal Electronics, Inc.

Title: ***DC Conn***

Size | Document Number: **LA-C701P** | Rev: 0.1

Date: Saturday, January 31, 2015 | Sheet 45 of 60



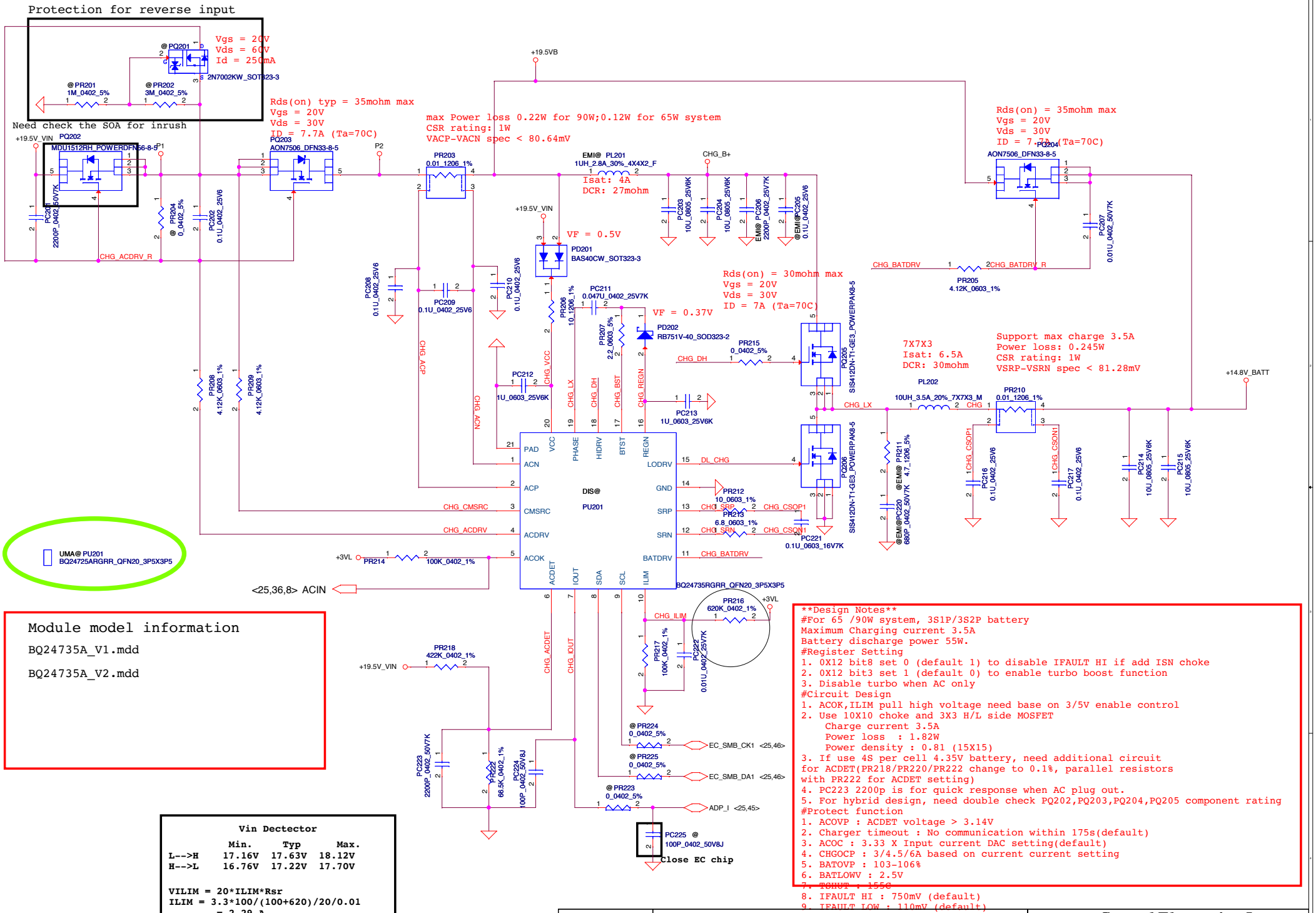
Security Classification	Compal Secret Data		
Issued Date	2014/10/09	Deciphered Date	2017/10/09

Compal Electronics, Inc.

Title: ***BATT Conn***

Size | Document Number: **LA-C701P** | Rev: 0.1

Date: Saturday, January 31, 2015 | Sheet 46 of 60



Module model information

BQ24735A_V1.mdd

BQ24735A_V2.mdd

Vin Dectector

	Min.	Typ	Max.
L-->H	17.16V	17.63V	18.12V
H-->L	16.76V	17.22V	17.70V

VILIM = 20*ILIM*Rsr
ILIM = 3.3*100/(100+620)/20/0.01
= 2.29 A

Design Notes
#For 65 /90W system, 3S1P/3S2P battery
Maximum Charging current 3.5A
Battery discharge power 55W.
#Register Setting
1. 0X12 bit8 set 0 (default 1) to disable IFAULT HI if add ISN choke
2. 0X12 bit3 set 1 (default 0) to enable turbo boost function
3. Disable turbo when AC only
#Circuit Design
1. ACOK,ILIM pull high voltage need base on 3/5V enable control
2. Use 10X10 choke and 3X3 H/L side MOSFET
Charge current 3.5A
Power loss : 1.82W
Power density : 0.81 (15X15)
3. If use 4S per cell 4.35V battery, need additional circuit for ACDET(PR218/PR220/PR222 change to 0.1%, parallel resistors with PR222 for ACDET setting)
4. PC223 2200p is for quick response when AC plug out.
5. For hybrid design, need double check PQ202,PQ203,PQ204,PQ205 component rating
#Protect function
1. ACOVP : ACDET voltage > 3.14V
2. Charger timeout : No communication within 175s(default)
3. ACOC : 3.33 X Input current DAC setting(default)
4. CHGOCP : 3/4.5/6A based on current current setting
5. BATOVP : 103-106%
6. BATLOWV : 2.5V
7. TSHUT : 155C
8. IFAULT HI : 750mV (default)
9. IFAULT LOW : 110mV (default)

Security Classification	Compal Secret Data		
Issued Date	2014/07/02	Deciphered Date	2012/07/02

Compal Electronics, Inc.

Title: **PWR-CHARGER**

Size | Document Number: Common Circuit | Rev: 0.1

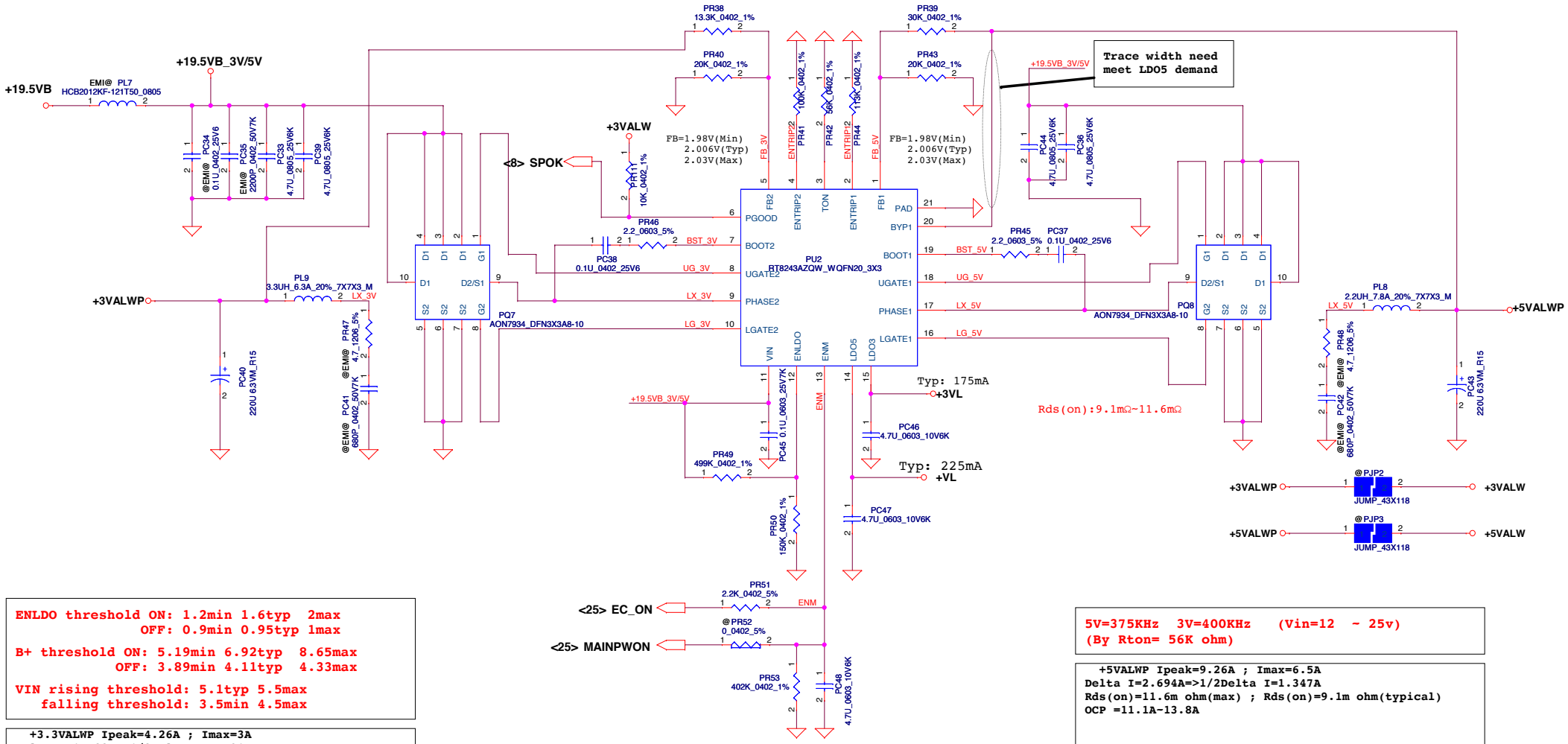
Date: Saturday, January 31, 2015 | Sheet 47 of 60

Module model information

RT8243A_V1.mdd

ENLDO (V)	ENM (V)	ENTRIP1 (V)	ENTRIP2 (V)	LDO5	LDO3	+5VALW	+3VALW
Low	Low	X	X	Off	Off	Off	Off
">1.6V" =>High	Low	X	X	On	On	Off	Off
">1.6V" =>High	">2.3V" =>High	Off	Off	On	On	Off	Off
">1.6V" =>High	">2.3V" =>High	Off	On	On	On	Off	On
">1.6V" =>High	">2.3V" =>High	On	On	On	On	On	On
">1.6V" =>High	">2.3V" =>High	On	Off	On	On	On	Off

ENTRIPx adjustment range: 0.5V~3V,
floating or over 4.5V will shutdown channel.



ENLDO threshold ON: 1.2min 1.6typ 2max
OFF: 0.9min 0.95typ 1max

B+ threshold ON: 5.19min 6.92typ 8.65max
OFF: 3.89min 4.11typ 4.33max

VIN rising threshold: 5.1typ 5.5max
falling threshold: 3.5min 4.5max

+3.3VALWP Ipeak=4.26A ; Imax=3A
Delta I=1.583A=>1/2Delta I=0.7915A
Rds(on)=11.6m ohm(max) ; Rds(on)=9.1m ohm(typical)
OCP = 9.41A~11.8A

TDC:4.31A Fsw:375KHz
H-MOS PD:0.3736W ΔT:12℃
L-MOS PD:0.2713W ΔT:7.9℃
Choke PD:1.5158W ΔT:24℃
OVP margin for Vos:8% @ 330uF cap, 6% @ 220uF

5V=375KHz 3V=400KHz (Vin=12 ~ 25v)
(By Rton= 56K ohm)

+5VALWP Ipeak=9.26A ; Imax=6.5A
Delta I=2.694A=>1/2Delta I=1.347A
Rds(on)=11.6m ohm(max) ; Rds(on)=9.1m ohm(typical)
OCP =11.1A~13.8A

TDC:4.9A Fsw:321KHz
H-MOS PD:0.4173W ΔT:13.4℃
L-MOS PD:0.3442W ΔT:10℃
Choke PD:1.9613W ΔT:30℃
OVP margin for Vos:9% @ 330uF cap, 8% @ 220uF

Security Classification	Compal Secret Data		
Issued Date	2012/07/10	Deciphered Date	2013/07/10

Compal Electronics, Inc.

Title: 3VALW/5VALW

Size: Custom | Document Number: LA-C701P | Rev: 0.1

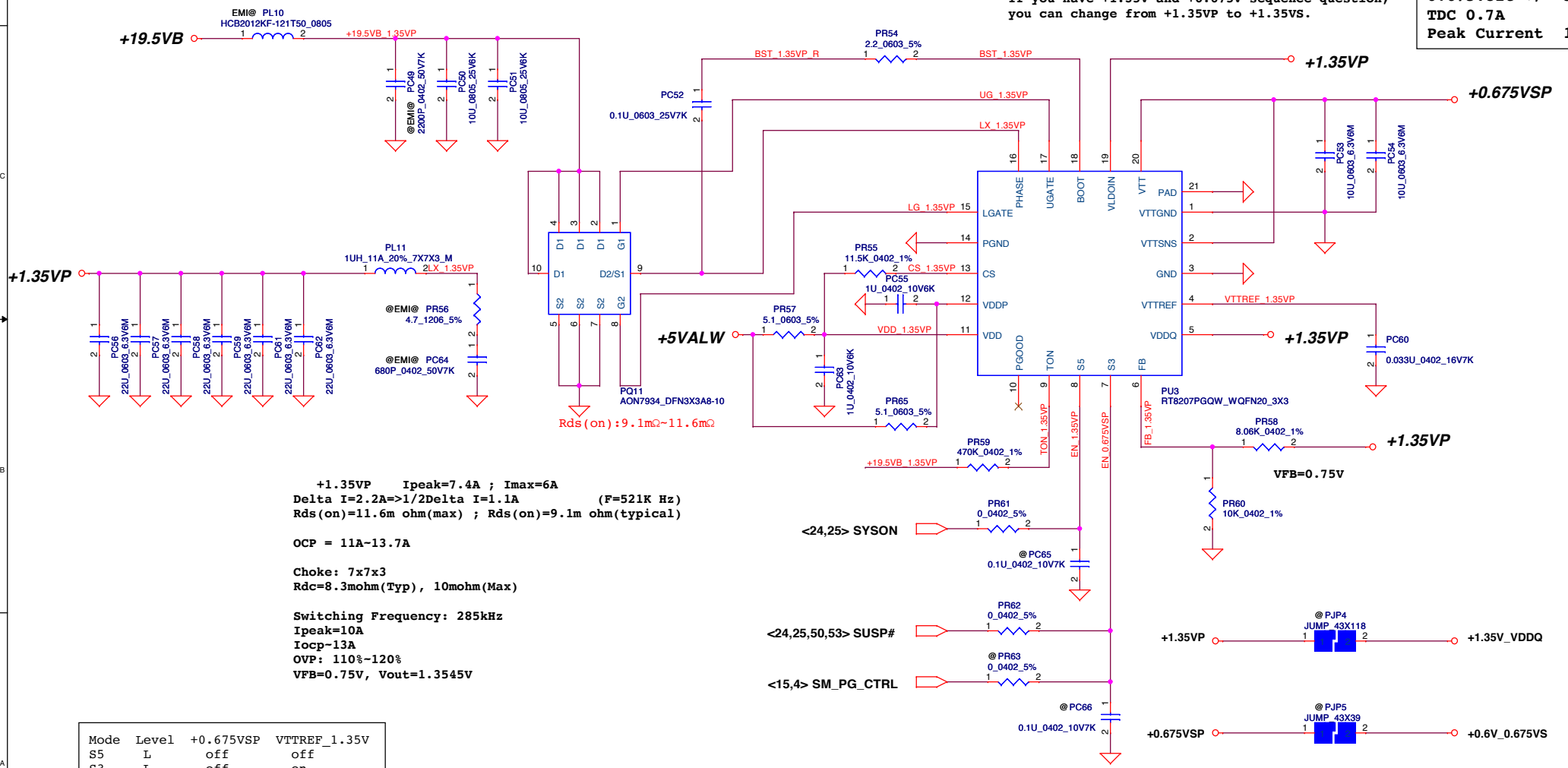
Date: Saturday, January 31, 2015 | Sheet 48 of 60

Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer

Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question,
you can change from +1.35VP to +1.35VS.

0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A



+1.35VP Ipeak=7.4A ; Imax=6A
Delta I=2.2A=>1/2Delta I=1.1A (F=521K Hz)
Rds(on)=11.6m ohm(max) ; Rds(on)=9.1m ohm(typical)

OCP = 11A~13.7A

Choke: 7x7x3
Rdc=8.3mohm(Typ), 10mohm(Max)

Switching Frequency: 285kHz
Ipeak=10A
Iocp~13A
OVP: 110%~120%
VFB=0.75V, Vout=1.3545V

Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2012/12/31

Compal Electronics, Inc.

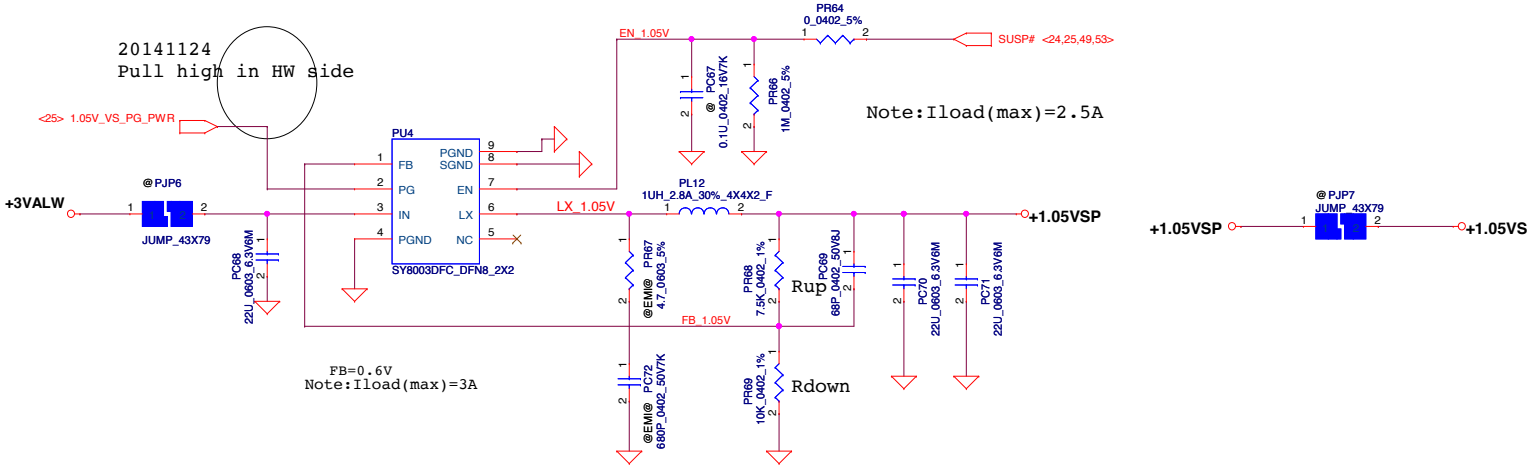
Title: RT8207P

Size: Custom | Document Number | Rev: 0.1

Date: Saturday, January 31, 2015 | Sheet 49 of 60

Module model information

SY8003_V2.mdd



Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

Vout=0.6V* (1+Rup/Rdown)

Security Classification	Compal Secret Data		
Issued Date	2011/06/13	Deciphered Date	2012/06/13

Title	SY8003		
Size: Custom	Document Number		Rev: 0.1
Date: Saturday, January 31, 2015	Sheet 50 of 60		

Module model information:
ISL95813_V1A for IC module
ISL95813_V1B for SW module

Base on BDW PDDG Rev_0_73			
Location	15W TDC 14A MAX 32A OCP 39A Loadline=-2.0mv/A	28W TDC 19A MAX 40A OCP 48A Loadline=-2.0mv/A	Note
PR89	287 Ohm	348 Ohm	OCP
PR85	1.27kOhm	1.58kOhm	Droop
PC88	0.033uF	0.01uF	RC Match
PR72	90.9kOhm	113kOhm	PROG1
PR75	95.3kOhm	95.3kOhm	IMON
PC83	0.1uF (0402)	0.1uF (0402)	RC Filter

H-side MOS: MDV1525URH
Rds(on):
<10.1mohm@Vgs=10V
<14.0mohm@Vgs=4.5V
Id :24A@Vgs=10V

L-side MOS: MDU1511RH
Rds(on):
<2.4mohm@Vgs=10V
<3.3mohm@Vgs=4.5V
Id :100A@Vgs=10V

Choke: 0.15UH (Size:7*7*4)
Rdc=0.66mohm +-7%
Heat Rating Current=36A

+1.05VS
Follow intel guideline
PR70 130_0402_1%
PR71 54.9_0402_1%
PC73 1U_0402_6.3V6K

Note:
VR_SVID_ALRT# Pull high on HW side

<11> VR_SVID_DAT
<11> VR_SVID_ALRT#
<11> VR_SVID_CLK
<11> VR_ON
<11> VGATE
<25> VR_HOT#
<11> VCCSENSE
<13> VSSSENSE

PR73 1.5K_0402_1%
PC79 1000P_0402_50V7K
PR75 95.3K_0402_1%
PH2 470K_0402_5%_B25/50 4700K
PR79 3.83K_0402_1%
PR80 27.4K_0402_1%
PC81 47P_0402_50V8J

Note:
VR_HOT# Pull high on HW side

Over temperature protection:
OTP Setting: 100C active
Pin5 (NTC) voltage <0.88V, Protect
Pin5 (NTC) voltage >0.92v, recovery

PU5
ISL95813HRZ-T_QFN20_3X4
PAD, VR_ON, PGOOD, IMON, VR_HOT#, NTC, COMP, FB, RTN, ISUMN, ISUMP, SCLK, ALERT#, SDA, PRGM1, LGATE, PHASE, UGATE, BOOT, VCC, PRGM2

PR72 90.9K_0402_1%

Note:
PR72=90.9K
=>Icc(max)=33A
fsw=700KHz

PR74 0_0603_5%
PR77 2.2_0603_5%
PC80 0.22U_0603_16V7K
PR81 124K_0402_1%
PC83 0.1U_0402_25V6

Note:
PR81=124K
=>Slew rate=53mV/us
Vboot = 1.7V

PQ12 MDV1525URH_PDFN33-8-5
PQ13 MDU1511RH_POWERDFN56-8-5

CPU_B+
PC74 10U_0805_25V6K
PC75 10U_0805_25V6K
PC76 0.1U_0402_25V6
PC77 220P_0402_50V7K
PC78 100U_25V_M
PC118 100U_25V_M
EMI@ PL13 5A_Z120_25M_0805_2P
EMI@ PL19 5A_Z120_25M_0805_2P
+19.5VB

PL14 0.15UH_29A_+-20%_7X7X4_M
+VCC_CORE
@EMI@ PR76 4.7_1206_5%
@EMI@ PC82 680P_0603_50V7K
PR78 3.65K_0603_1%

+5VS

PR82 5.9K_0402_1%
PC84 33P_0402_50V8J
PC85 6800P_0402_25V7K
PR83 @ 2K_0402_1%
PR84 @ 10_0402_1%
PC86 @ 330P_0402_50V7K
PC87 @ 390P_0402_50V7K
PR85 1.27K_0402_1%
Droop

PR86 @ 4.99M_0402_1%
RC Match
PC88 0.033U_0402_25V7K
PC89 0.1U_0402_16V4Z
PR87 2.61K_0402_1%
PR88 11K_0402_1%
PH3 10K_0402_5%_B25/50 4250K

OCP Setting
PR89 287_0402_1%

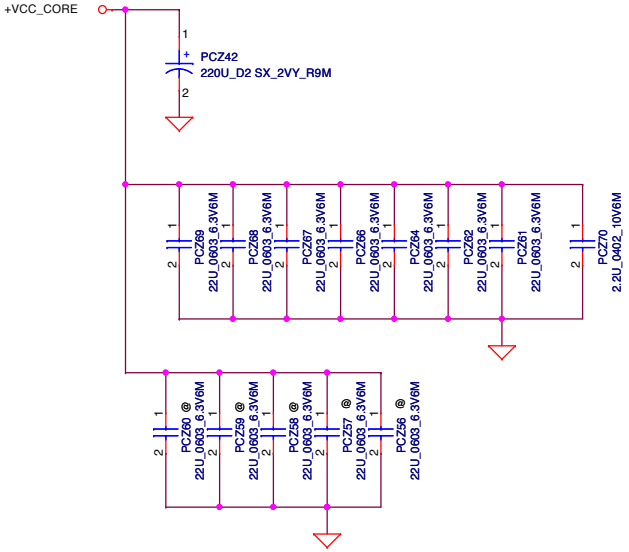
@PC90 330P_0402_50V7K
@PC91 0.082U_0402_16V7K
PC92 0.01U_0402_50V7K

@PC93 4700P_0402_25V7K
@PR90 1.5K_0402_1%

20150107
change PC88 PN
from SE000006OM8 to SE000006O00

Local sense put on HW site

123
Title: ISL95813 for BDW-Y&U(15W/28W) CPU
Size: Document Number: LA-C701P
Rev:
Date: Saturday, January 31, 2015 Sheet 51 of 60



BDW-U 15W
220uF × 1
22uF × 7
2.2uF × 1

Compal Electronics, Inc.

Title: ***PROCESSOR DECOUPLING***

Size | Document Number: **LA-C701P** | Rev: 0.1

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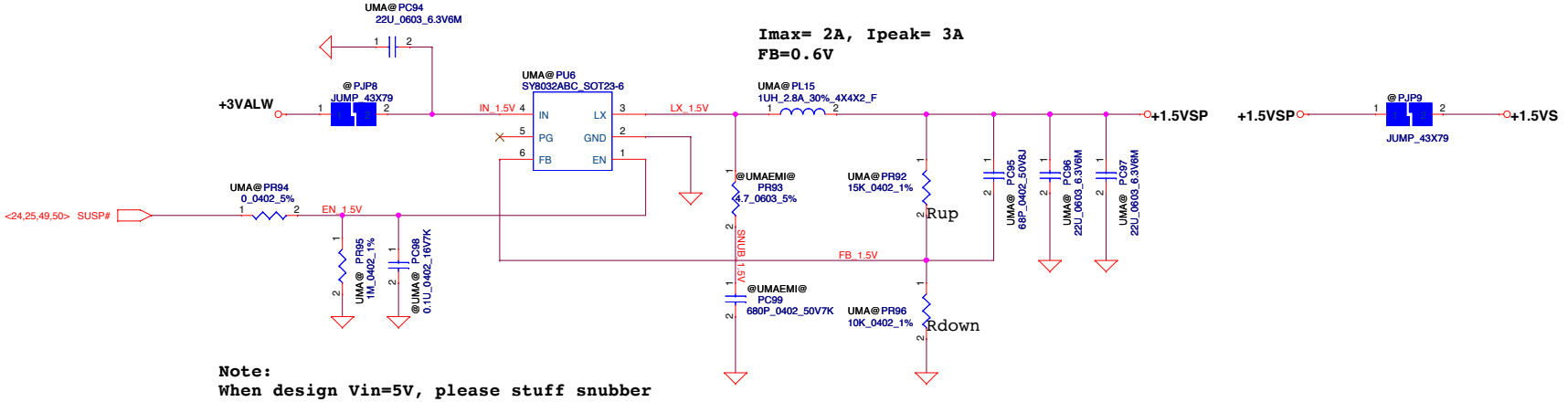
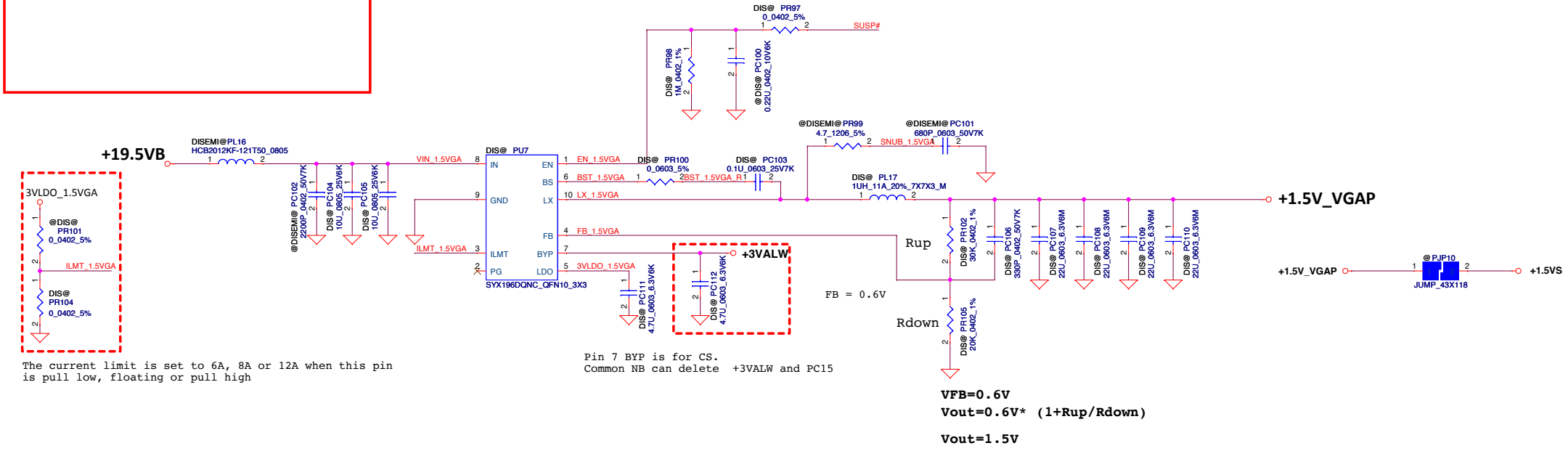


Module model information

SYX196D_V3.mdd

EN pin don't floating
If have pull down resistor at HW side, pls delete PR702



The current limit is set to 6A, 8A or 12A when this pin is pull low, floating or pull high

Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC15

VFB=0.6V
Vout=0.6V* (1+Rup/Rdown)

Vout=1.5V

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/09/09	Deciphered Date	2016/09/30

Title	+1.5VS		
Size	Document Number		Rev
	LA-C701P		0.1
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GPI021	GPI029	GPI030	GPI020	GPI015	
VID5	VID4	VID3	VID2	VID1	VDDC
0	1	1	1	0	1.150V
1	0	0	0	0	1.100V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V

Vboot(merge)

	AMD MARS series			LP: DDR3 Pro/XT/XTX: GDDR5	AMD SUN series		UL: DDR3 Pro/XT/XTX: GDDR5	Description
GPU	MARS XTX	MARS XT	MARS PRO	MARS LP	SUN UL	SUN PRO	SUN XT	NA
VDDC	0.775~1.175V	0.775~1.125V	0.775~1.050V	0.775~1.000V	0.775~1.125V	0.800~1.075V	0.800~1.150V	NA
TDC	32A (TDC)	25A (TDC)	21A (TDC)	17A (TDC)	16A (TDC)	19A (TDC)	25A (TDC)	NA
EDC	48A	37.5A	31.5A	26A	24A	28.5A	37.5A	NA
OCP	57.6A	45A	37.8A	31.2A	28.8A	34.2A	45A	NA
Vboot	0.85V	0.85V	0.85V	0.85V	0.9V	0.9V	0.9V	NA
Load line	1mohm	1mohm	1mohm	----------	----------	----------	1mohm	NA
Ri PR860	1.13K Ohm	887 Ohm	750 Ohm	----------	----------	----------	887 Ohm	for OCP and LoadLine Setting
Rdroop PR842	1.43K Ohm	1.13K Ohm	953 Ohm	----------	----------	----------	1.13K Ohm	for LoadLine Setting
PR844	187K Ohm	147K Ohm	124K Ohm	----------	----------	----------	147K Ohm	for Compensation
PR847	51.1K Ohm	51.1K Ohm	51.1K Ohm	----------	----------	----------	51.1K Ohm	for Positive offset

H-side MOS:MDU1516
Rds(on):
9mohm@Vgs=10V
7.8~9mohm@Vgs=4.5V
Id :11A@Ta=25 degC

L-side MOS:UDU1511
Rds(on):
2.4mohm@Vgs=10V
2.7~3.3mohm@Vgs=4.5V
Id :24A@Ta=25 degC

Choke: 0.22uH (Size:7*7*4)
Rdc=0.98mohm +-5%
Heat Rating Current=28A
Saturation Current=28A

Remark:

1. PWM3 (Pin24) tie to 5V & CLK# (Pin40) external pull high
   => 2 phase CPU VR config
   PWM3 (Pin24) tie to 5V & CLK# (Pin40) tie to GND or floating
   => 2 phase GPU VR config

2. When 2 Phase GPU config
   a. DPSLPVR (Pin39)=0 PSI# (Pin2)=0
      =>1 phase CCM operation mode
   b. DPSLPVR (Pin39)=0 PSI# (Pin2)=1
      =>2 phase CCM operation mode
   c. DPSLPVR (Pin39)=1 PSI# (Pin2)=0 or 1
      =>1 phase DE operation mode

3. Rbias=147K =>overshoot reduction function disable
   Rbias=47K =>overshoot reduction function enable

4. Thermal throttling:
   Protect: (6.98K+Rth)*60uA=1.2V
   => Rth=13.02K
   =>Tp=110C (+-3C)
   Recovery:(6.98K+Rth)*56uA=1.24V
   => Rth=15.16K
   => Tr=105C (+-3C)

PR837=6.98K	PR837=1.5K
protect T 110C +-3	protect T 100C +-3
Recovery T 105C +-3	Recovery T 96C +-3

5. Switching frequency set :
   Rfset(kohm)=[period(us)-0.29]*2.65
   =5.9Kohm
   fsw=1/period(us)=400KHZ

20150129
unpop PC801 for lose dGPU issue

Remark: MARS LP/ SUN UL/ SUN PRO
don't use this 2-phase solution

Module model information:
ISL62883C_V1A for IC
ISL62883C_V1B for SW Choke/MOS on BTN
ISL62883C_V2B for SW Choke on BTN, MOS on TOP

Layout Note:
PH801 should place near phase1 H-side MOS

PR813 Pop:
for Loadline disable
PR813 @:
for Loadline enable and LL=1mohm

TDC 28A
Peak Current = 37.5A
OCP Current = 45A
Load line=1.1mohm

Transient response :
Rntcnet=(Rntcs+Rntc)*Rp/(Rntcs+Rntc+Rp)
Cn=L*(Rntcnet+Rsum/N)/[Rntcnet*DCR*(Rsum/N)]
N is the number of phases

Rdroop=Io*LL/Idroop

Layout Note:
PH802 should place near Phase1 Choke

Security Classification	Compal Secret Data		
Issued Date	2013/01/03	Deciphered Date	2013/01/03

Compal Electronics, Inc.

Title: ISL62883C

Size: | Document Number: | Rev: 0.1

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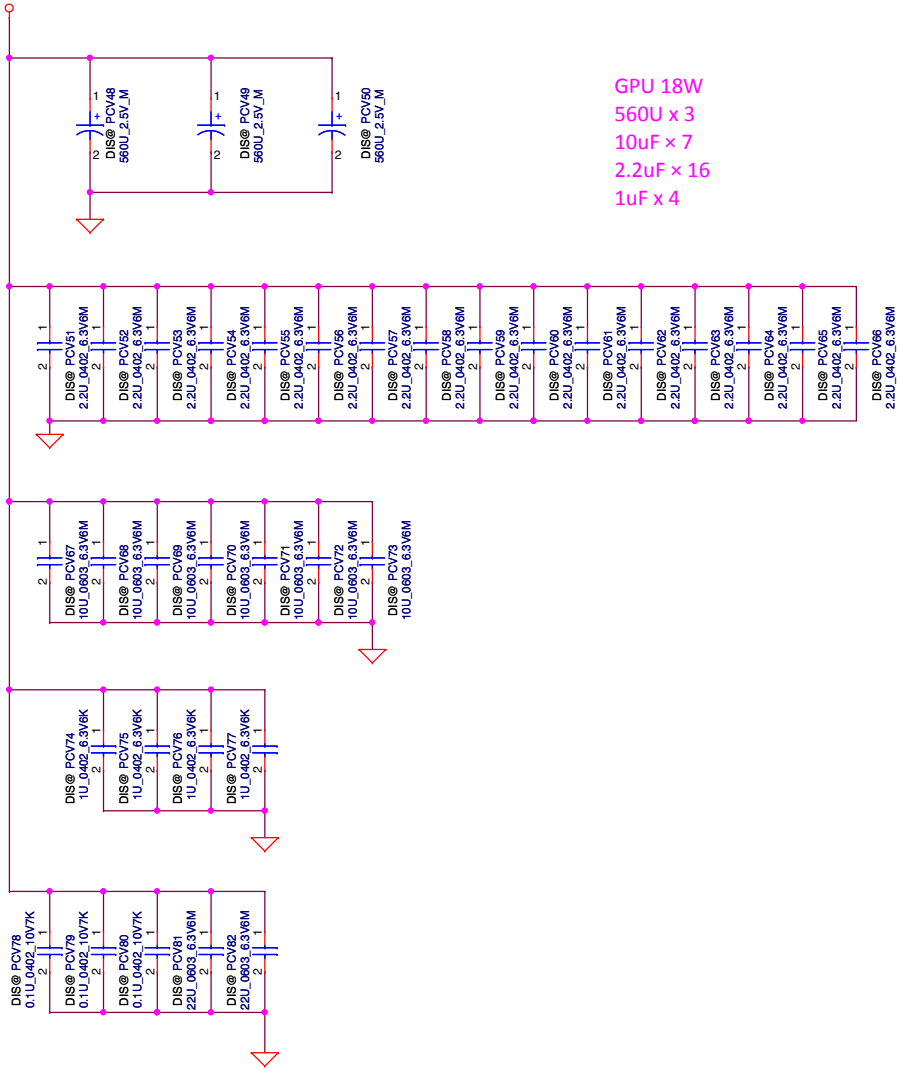
+VGA_CORE



GPU 18W
560U x 3
10uF x 7
2.2uF x 16
1uF x 4

Compal Electronics, Inc.

Title: *VGA CHIP DECOUPLING*

Size	Document Number	Rev
	LA-C701P	0.1

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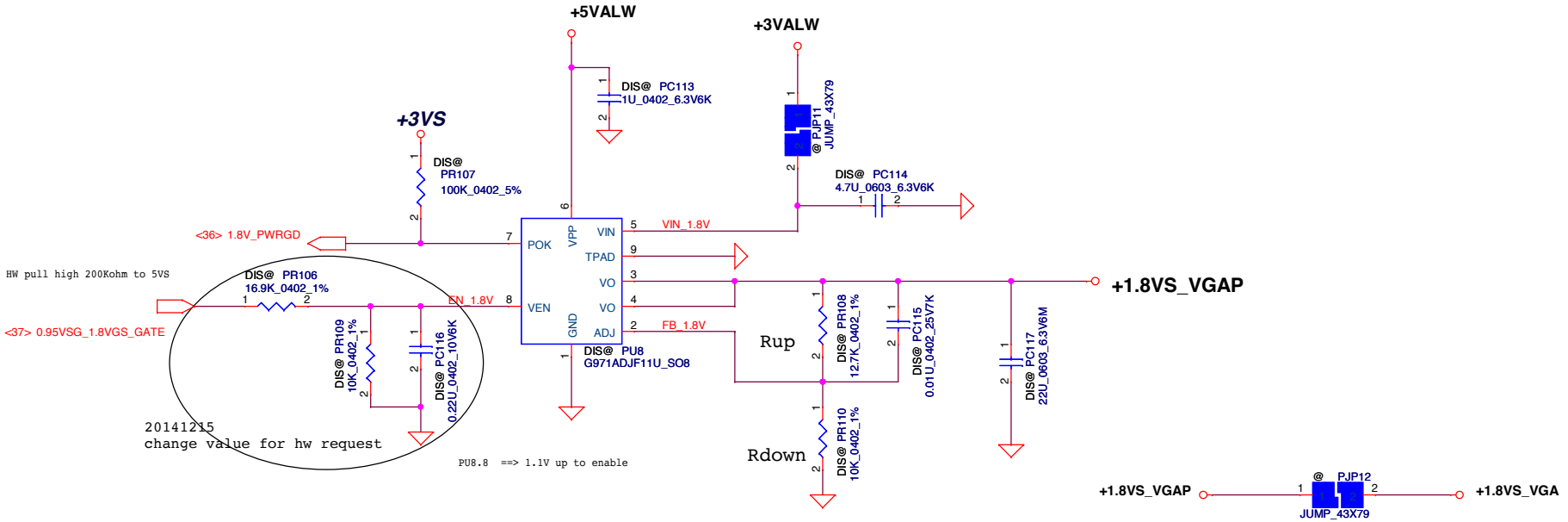


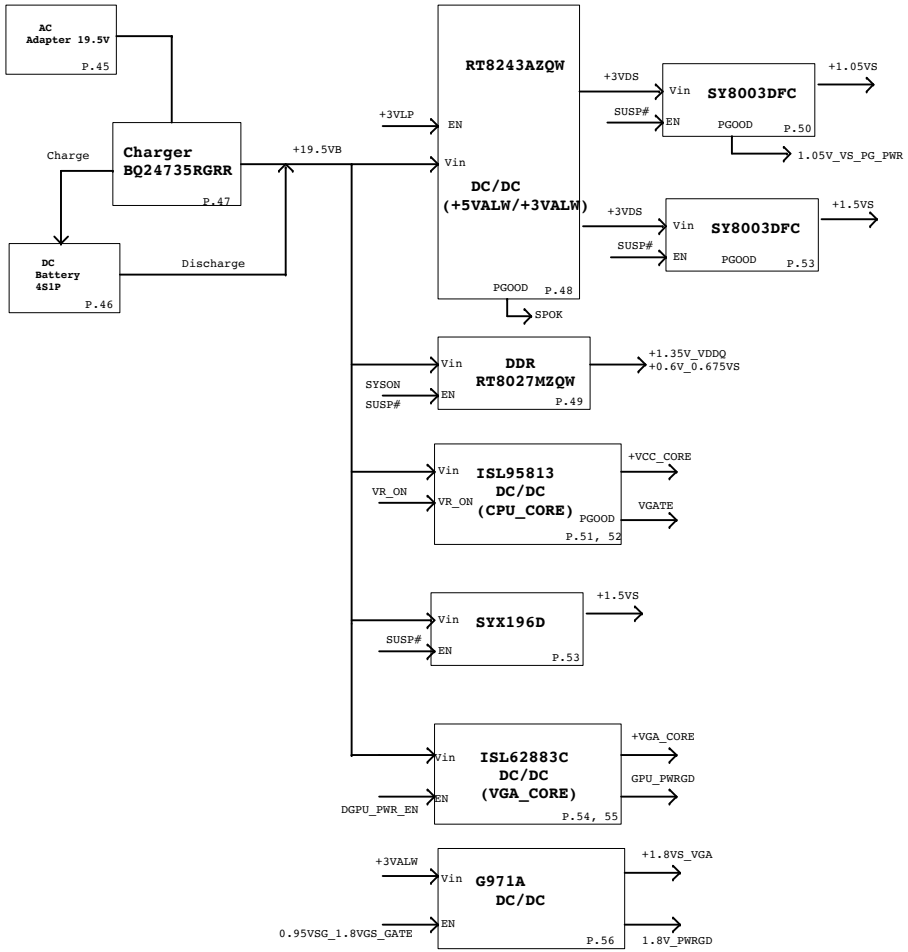
Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2016/09/30

Compal Electronics, Inc.

Title: *+1.8VS_VGA*

Size: B | Document Number: LA-C701P | Rev: 0.1

Date: | Sheet 56 of 60



Security Classification	Compal Secret Data		
Issued Date	2012/04/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.

Title: *Power Block Diagram*

Size	Document Number	Rev
	LA-C701P	0.1

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Version change list (P.I.R. List)

Item	Date	Fixed Issue	Reason for change	Modify List	Phase
1	change size		use common part for 7x7	change PL202 size from 10x10 to 7x7	SI
2	change part		no need 0ohm	PR224 and PR225 change from 0ohm to short pad	SI
3	change part		HW request	Change R, C value PR106 100k => 16.9k PR109 47k => 10k PC116 0.1U => 0.22U	SI
4	change part		Change PN	PC88 from SE0000060M8 to SE000006000	PV
5	20150129		for lose dGPU issue	unmount PC801	PV

Compal Electronics, Inc.		
Title: PIR List		
Size: B	Document Number: LA-C701P	Rev: 0.1
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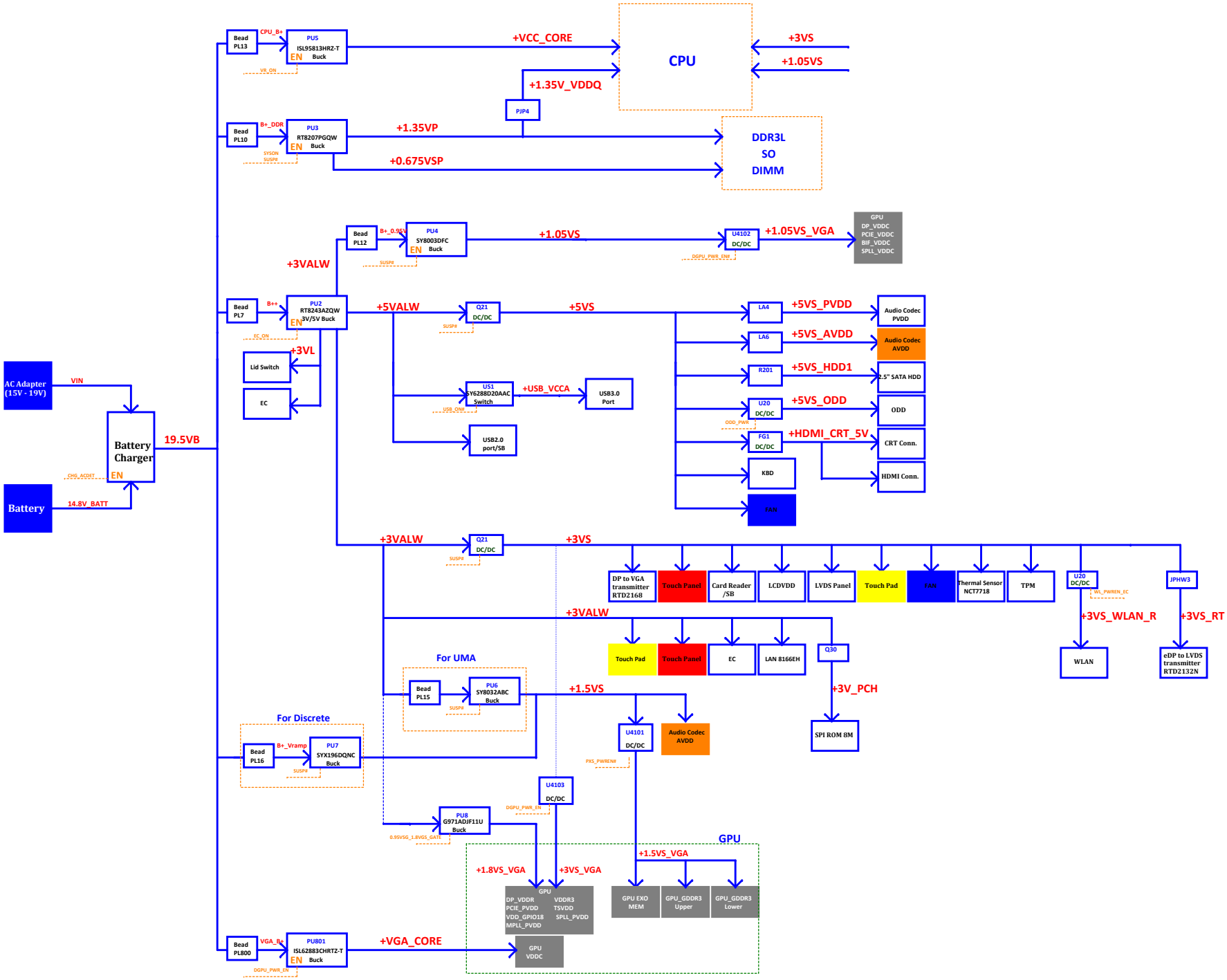

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/01/11	Declassified Date	2015/04/22
			System Power Tree
			LA-C701P

Version change list (P.I.R. List)

Item	Date	Fixed Issue	Reason for change	Modify List	Phase
1	2014-11-25		A32 request	[A32] Reserve XDP circuit	DB
2	2014-11-25		A32 request	[A32] Reserve SMBUS from CPU to TP module	DB
3	2014-11-25	BDW CPU ESD issue	BDW CPU ESD issue solution	[Compal] Reserve Capx19 & Varistor x13 for BDW CPU ESD issue	DB
4	2014-11-25	[HP] Reserve XDP circuit	A32 request	[A32] eDP to VGA solution Sanrio--ITE IT6513 Candy--RTD2168	DB
5	2014-11-25		A32 request	[A32] KBC solution solution Sanrio--ENE KBC9012 Candy--ENE KBC9022	DB
6	2014-11-25		reduce component	[Compal] Remove WLAN LED circuit ,use KBC GPIO	DB
7	2014-11-25		A32 request	[A32] reserve TPM 1.2 & 2.0 TPM 1.2--SLB9665 TPM2.0--SLB9660	DB
8	2014-11-25		reduce component	[Compal] ODD load switch Sanrio use single load switch Candy use dual load switch	DB
9	2014-11-25		A32 request	[A32l] Change WLAN connector Sanrio--mini card Candy--M.2 Conn	DB
10	2014-11-25		reduce component	[Compal] Sanrio use power switch for Fan control , Candy use PWM control from KBC	DB
11	2014-11-25		A32 request	[A32] Card reader solution Sanrio--RTS5239 Candy--RTS5141	DB
12	2014-11-25		A32 request	[A32] GPU solution Sanrio--Nvidia N15V-GM (17W) Candy--AMD Exo pro (18W)	DB
13	2014-11-25		reduce component	[Compal] +3VS to +3VS_VGA from dual load switch to single load switch +1.8VS_VGA power direct support	DB
14	2014-12-14		For LAN 1V regout	[Compal] Pop LL3	SI
15	2014-12-14		For fine turn DGPU power sequence	[Compal] Change C4122 value from 0,01u to 0.22u	SI
16	2014-12-14		For fine turn DGPU power sequence	[Compal] Change R4109 value from 200K to 6.98K	SI
17	2014-12-14		For fine turn DGPU power sequence	[Compal] Change C4109 value from 0,01u to 0.027u	SI
18	2014-12-14		Modify WLAN PCIE CLK request channel	[Compal] Modify WLAN CLK request channel from 2 to 5.	SI

Compal Electronics, Inc.

Title: HW PIR List

Size: B | Document Number: LA-C701P | Rev: 0.1

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Version change list (P.I.R. List)

Item	Date	Fixed Issue	Reason for change	Modify List	Phase
19	2014-12-14		Modify DGPU PCIE CLK request channel	[Compal] Modify DGPU CLK request channel from 3 to 4.	SI
20	2014-12-14		Modify LAN PCIE CLK request channel	[Compal] Modify LAN CLK request channel from 0 to 2.	SI
21	2014-12-23		HP request add thermal sensor for CPU PCB.	[Compal]Add CPU external Thermal sensor at EC_SMB_CK2/DA2.	SI
22	2014-12-23		CPU and GPU thermal sensor can't on the same bus.	GPU thermal sensor change to EC_SMB_CK3/DA3	SI
23	2014-12-23		Modify EC co-lay pin117 & 124.		SI
24	2014-12-24		EMI request to change HDMI schematic.		SI
25	2014-12-25		Reserved +5VS Touch power.		SI
26	2015-01-26		BIOS request.	Add pull-up at PCIECLKREQ1#	PV
27	2015-01-27		SVTP 3-9 fail.	R38 power change to +HDMI_CRT_5V , L7,L8,L9 change P/N.	PV
28	2015-01-27		SVTP 3-9 fail.	Remove Hsync,Vsync Buffer footprint.	PV
29	2015-01-28		Reserved for test.	Reserved 0 ohm on ODD_PLUG# , between CPU and ODD.	PV
210	2015-01-30		EMI request	Add 680p at PWR_LED#	

Compal Electronics, Inc.		
Title: HW PIR List		
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