Compal Confidential

Model Name : A4WAB
File Name : LA-C341P

Compal Confidential

M/B Schematics Document

Intel Broadwell ULT (Broadwell + Wildcat point)

Nvidia N16S-GT / N16V-GM

2015-03-18

REV:1.0

Security Classification	Compal Secret Data		
Issued Date	2014/09/16	Deciphered Date	2014/05/24

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VGA

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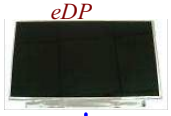
DP to VGA
RTD2168
page 30

eDP



page 28

HDMI Conn.

page 29

DP x 2 lanes

HDMI x 4 lanes

DDI

eDP

Intel Broadwell ULT

Broadwell ULT
Processor

OPI

Wildcat point
PCH

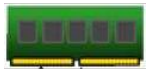
1168pin BGA
page 06~16

Fan Control
page 40

Memory BUS
Dual Channel

1.35V DDR3L 1333/1600

204pin DDR3L-SO-DIMM X1
BANK 0, 1, 2, 3
page 17



204pin DDR3L-SO-DIMM X1
BANK 4, 5, 6, 7
page 18

USB 3.0
conn x2
USB port 0, 1

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USB 2.0
conn x1
USB/B (port 2)

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CMOS
Camera
USB port 6

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Touch
Screen
I2C (PORT0)
USB (port 5)
page 28

USBx8
48MHz

HD Audio
3.3V 24MHz

HDA Codec
ALC255
page 35

Int. Speaker
page 35

Int. MIC
page 35

Universal Jack
USB/B
page 36

SPI

SPI ROM x1
page 7

PCIe 2.0
5GT/s
port 4

PCIe 2.0 x4
5GT/s
port 5

Flexible IO

PCIe 2.0
5GT/s
port 3

port 0

port 1

Nvidia N16S-GT / N16V-GM
with DDR3 x4 or 8
page 19~27

NGFF Card
WLAN
USB port 4
page 34

LAN(GbE)/ Card Reader
Realtek 8411B
page 29

SATA HDD
Conn.

page 36

SATA CDROM
Conn.

page 36

Card Reader
2 in 1 (SD)

page 33

RJ45 conn.

page 33

LPC BUS
CLK=24MHz

ENE
KB9022
page 38

Touch Pad
PS2 / I2C

page 39

Int.KBD

page 39

RTC CKT.
page 8

Power On/Off CKT.
page 39

DC/DC Interface CKT.
page 41

Power Circuit DC/DC
page 42~53

Sub Board

LS-C341P
USB/B
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Title: Block Diagrams

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+0.675VS	+0.675VS power rail for DDR3L terminator	ON	OFF	OFF
+1.05VS_VTT	+1.05V power rail for CPU	ON	OFF	OFF
+1.05VSDGPU	+1.05VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.35V	+1.35V power rail for DDR3L	ON	ON	OFF
+1.5VSDGPU	+1.5VSDGPU power rail for GPU	ON	OFF	OFF
+1.5VS	+1.5V power rail for CPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VLP	B+ to +3VLP power rail for suspend power	ON	ON	ON
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+3VSDGPU	+3VS to +3VSDGPU power rail for GPU	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VS	+5VALW to +5VS power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	12K +/- 5%	0.347 V	0.354 V	0.360 V
2	15K +/- 5%	0.423 V	0.430 V	0.438 V
3	20K +/- 5%	0.541 V	0.550 V	0.559 V
4	27K +/- 5%	0.691 V	0.702 V	0.713 V
5	33K +/- 5%	0.807 V	0.819 V	0.831 V
6	43K +/- 5%	0.978 V	0.992 V	1.006 V
7	56K +/- 5%	1.169 V	1.185 V	1.200 V
8	75K +/- 5%	1.398 V	1.414 V	1.430 V
9	100K +/- 5%	1.634 V	1.650 V	1.667 V
10	130K +/- 5%	1.849 V	1.865 V	1.881 V
11	160K +/- 5%	2.015 V	2.031 V	2.046 V
12	200K +/- 5%	2.185 V	2.200 V	2.215 V
13	240K +/- 5%	2.316 V	2.329 V	2.343 V

USB Port Table

USB 2.0	Port	3 External USB Port
EHCI1	0	USB Port (3.0 left front)
	1	USB Port (3.0 left back)
	2	USB Port(Right 2.0)
	3	
	4	Mini Card (WLAN+BT)
	5	Touch Screen
	6	Camera
	7	
USB 3.0	Port	
XHCI	0	USB Port (3.0 left front)
	1	USB Port (3.0 Left back)
	2	
	3	

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	1.0
6	
7	

BTO Option Table

BTO Item	BOM Structure
Unpop	@
Connector	CONN@
UMA Component	UMA@
GPU	VGA@
On Board HDD	HDD1@
Wire HDD	HDD2@
EMI Component	EMI@
EMI Reserve	XEMI@
ESD Component	ESD@
ESD Reserve	XESD@
TPM Module	TPM@
VRAM Selection	X76@
DGPU_IDEN	VGL@, VGM@, SGT@
CPU_IDEN	HW@, BW@
GC6 2.0	GC6@
non GC6	NGC6@
EA40	1DMIC@
VA50	2DMIC@
Power BTN for debug	DB@
For 15" V3 series	V3@
G-Sensor	GSEN@

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Title: Notes List

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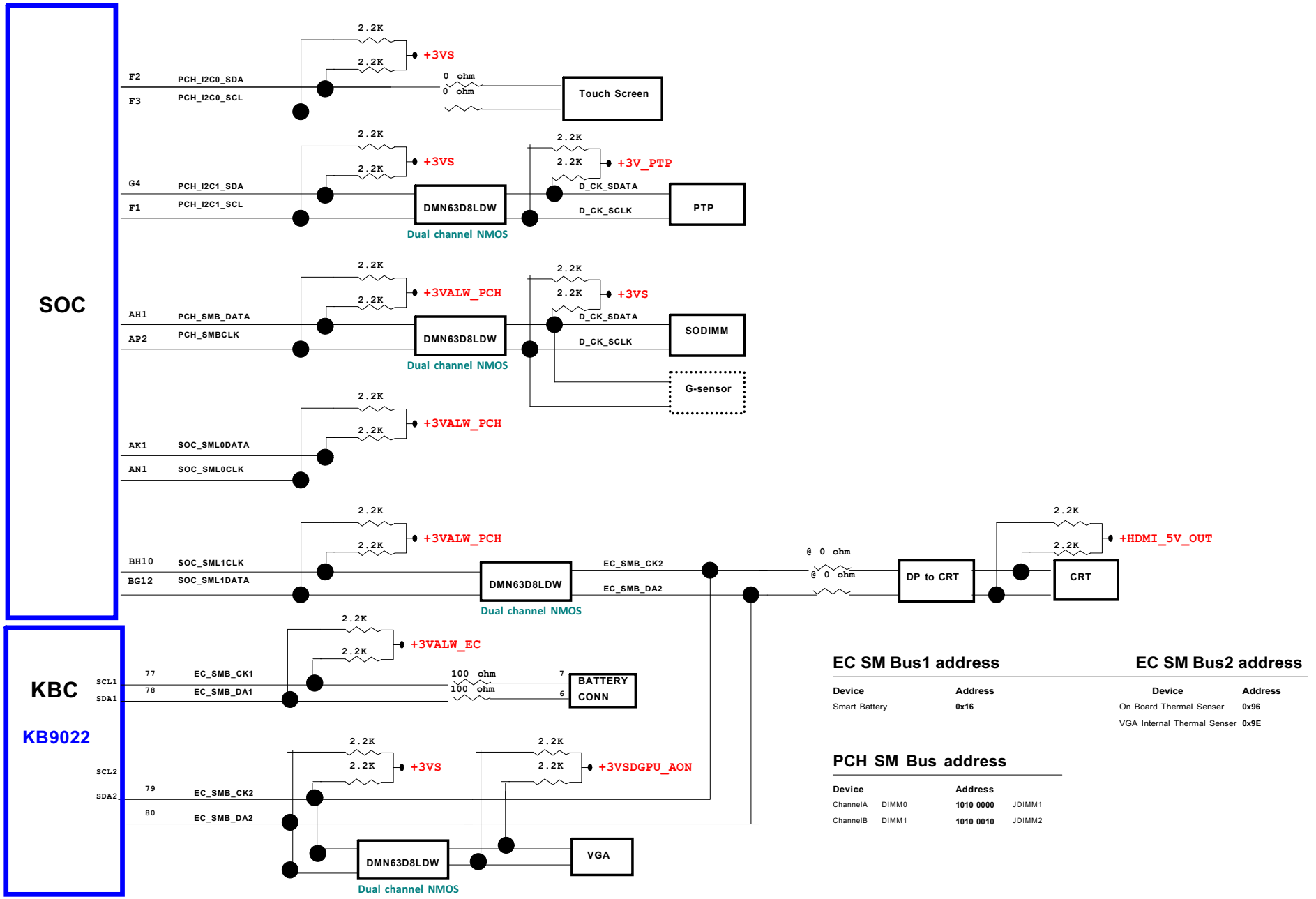

EC SM Bus1 address

Device	Address
Smart Battery	0x16

EC SM Bus2 address

Device	Address
On Board Thermal Senser	0x96
VGA Internal Thermal Senser	0x9E

PCH SM Bus address

Device		Address	
ChannelA	DIMM0	1010 0000	JDIMM1
ChannelB	DIMM1	1010 0010	JDIMM2

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Title: SMB/I2C

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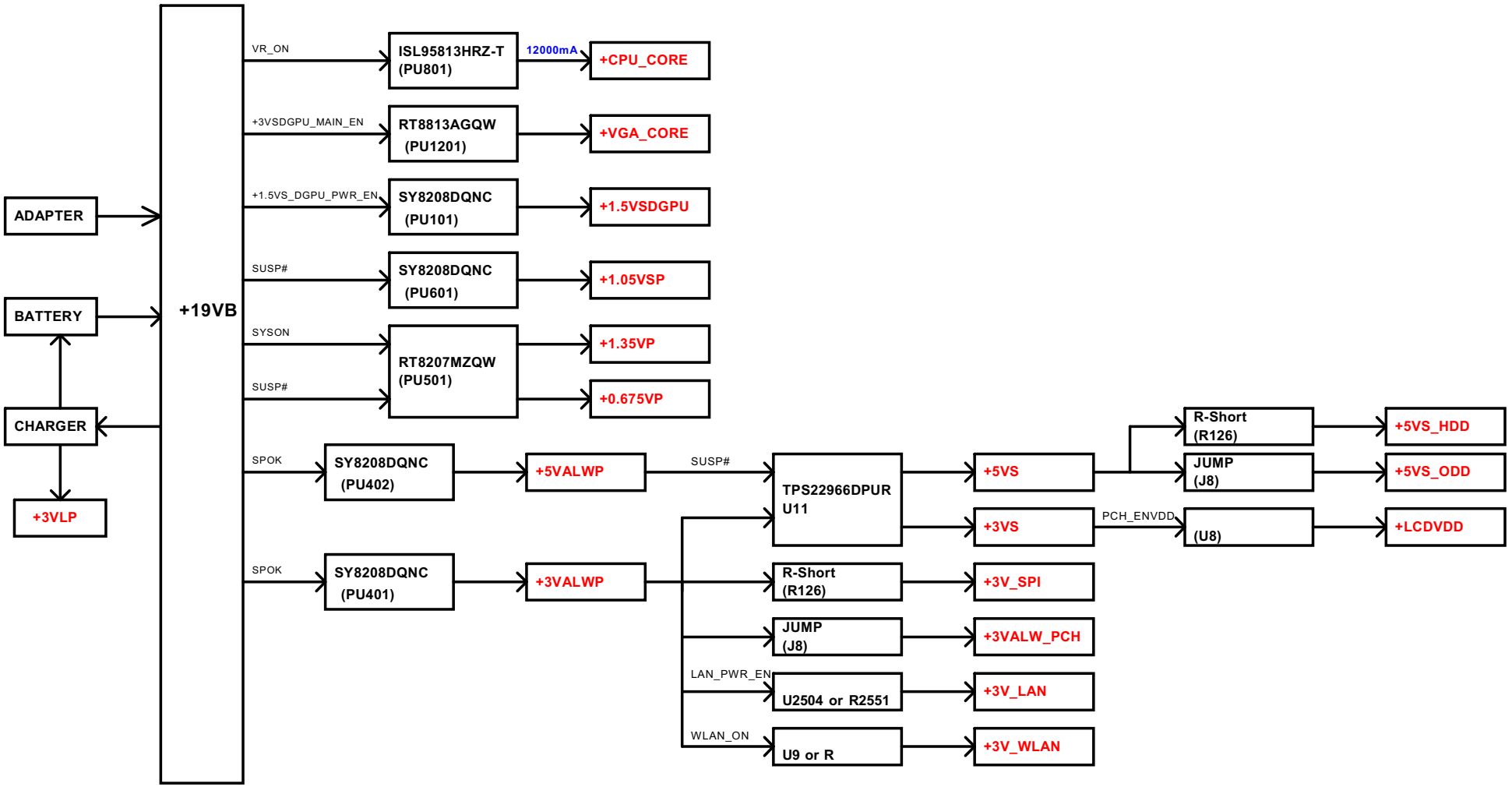

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Title: Power Rail			
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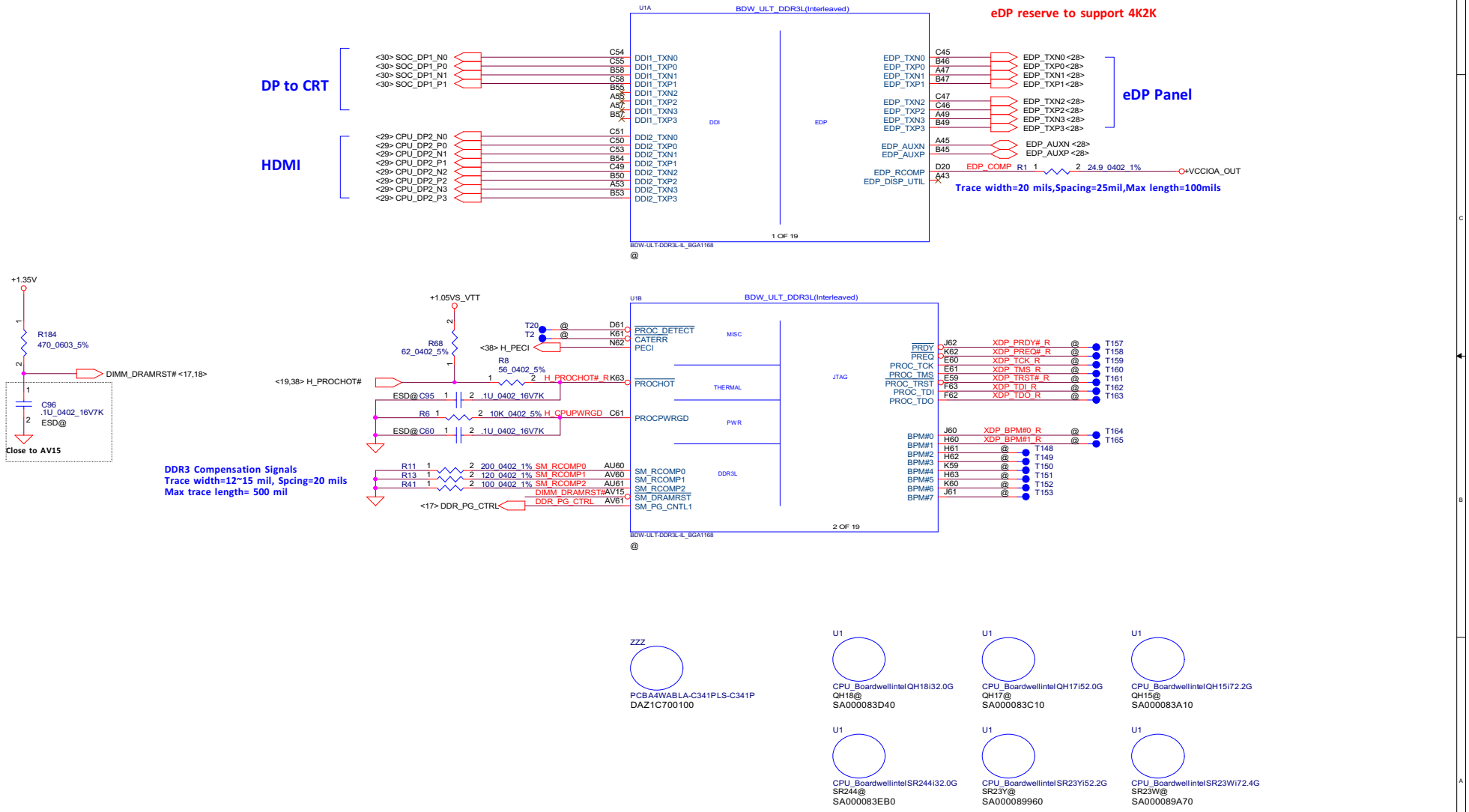

Security Classification	Compal Secret Data		
Issued Date	2014/09/16	Deciphered Date	2014/05/24

Compal Electronics, Inc.			
Title: BDW MCP(1/11) DDI,MSIC,XDP			
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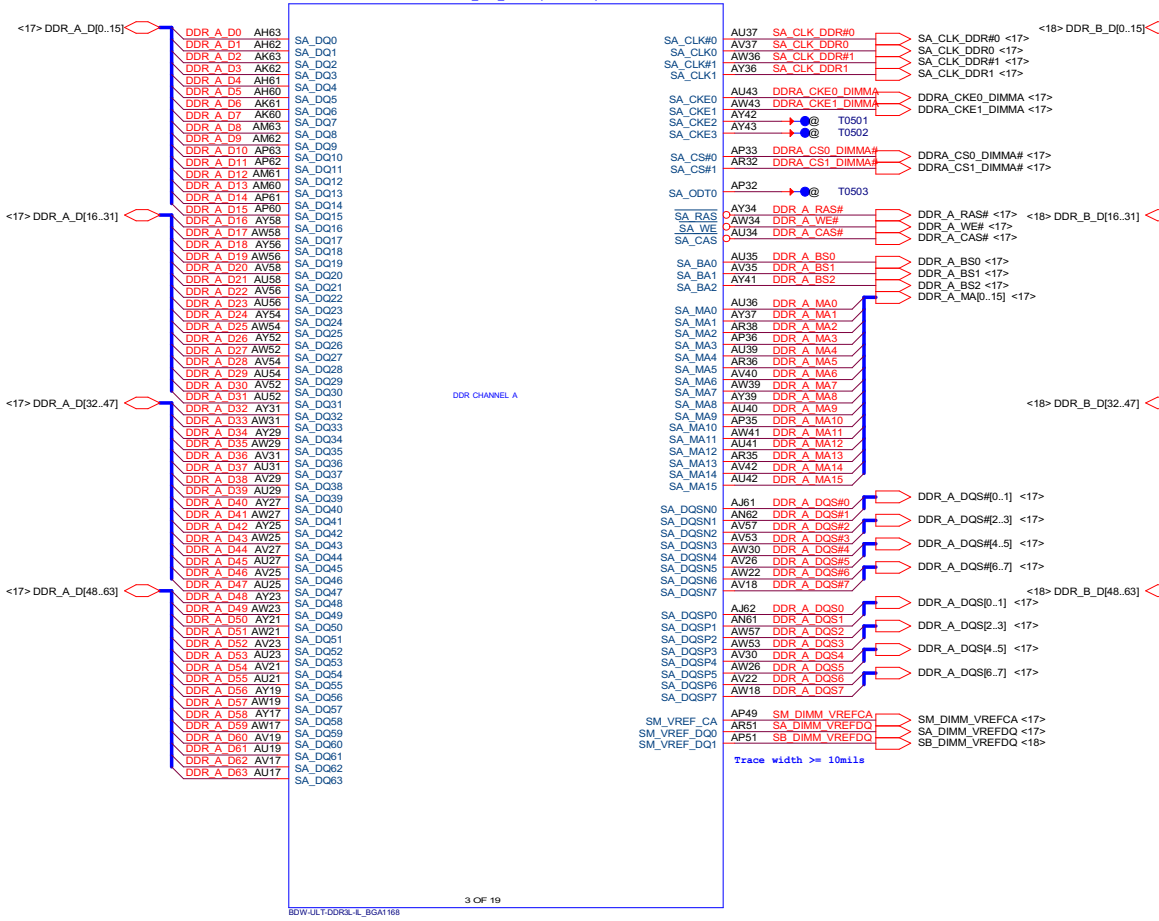
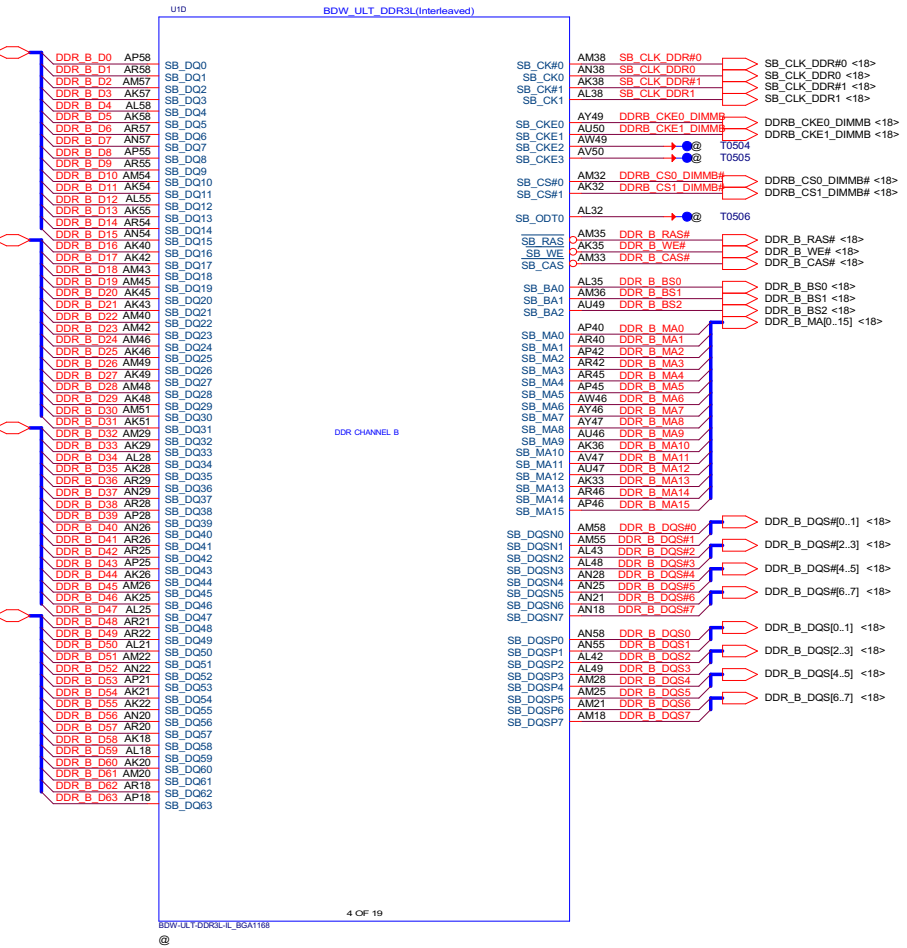
DDR interleave routing



DDR interleave routing



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Compal Electronics, Inc.	
Title	BDW MCP(2/11) DDRIII
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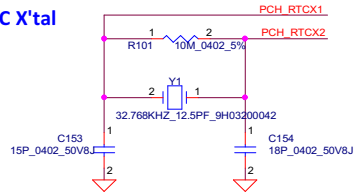
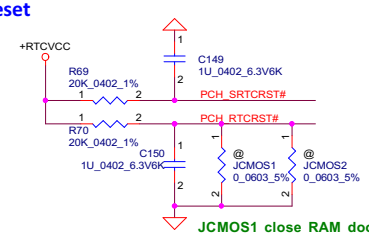
RTC X'tal



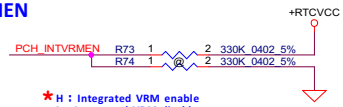
For BDW,
Crystal change to SJ10000LV00 (ESR=50k Ohm)

RTC Reset



JCMOS1 close RAM door

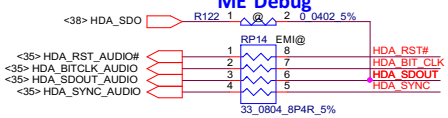
INTVRMEN



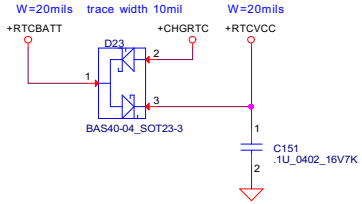
★H : Integrated VRM enable
L : Integrated VRM disable

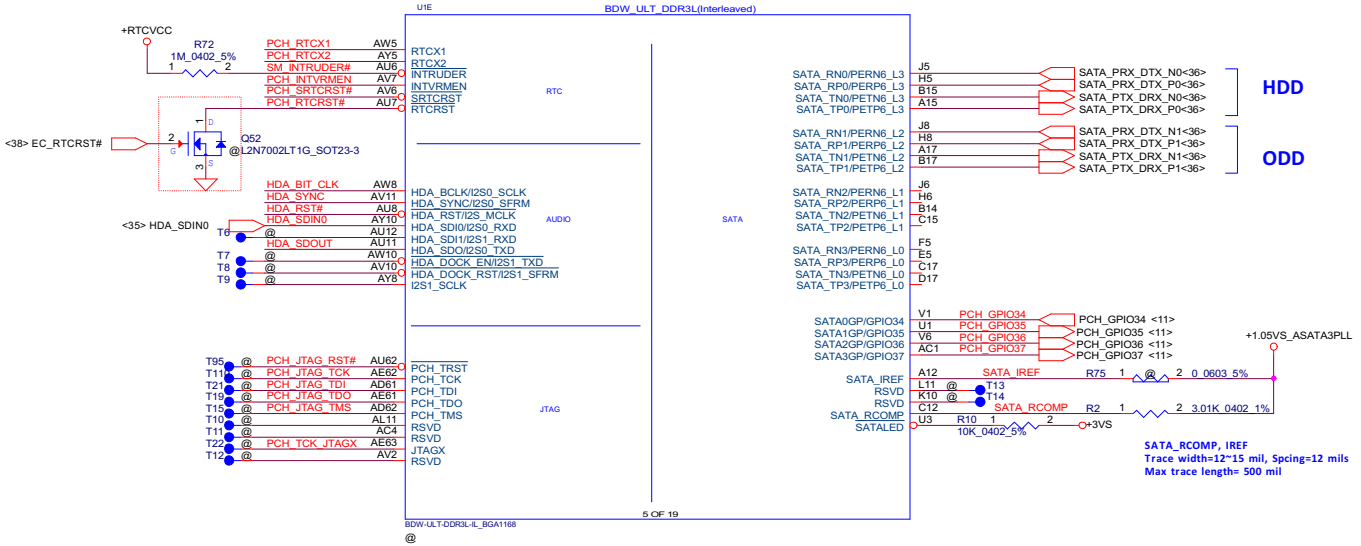
HDA for AUDIO

ME Debug



RTC Battery





SATA_RCOMP, IREF
Trace width=12~15 mil, Spcing=12 mils
Max trace length= 500 mil

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Title: BDW MCP(3/11) RTC,SATA,XDP

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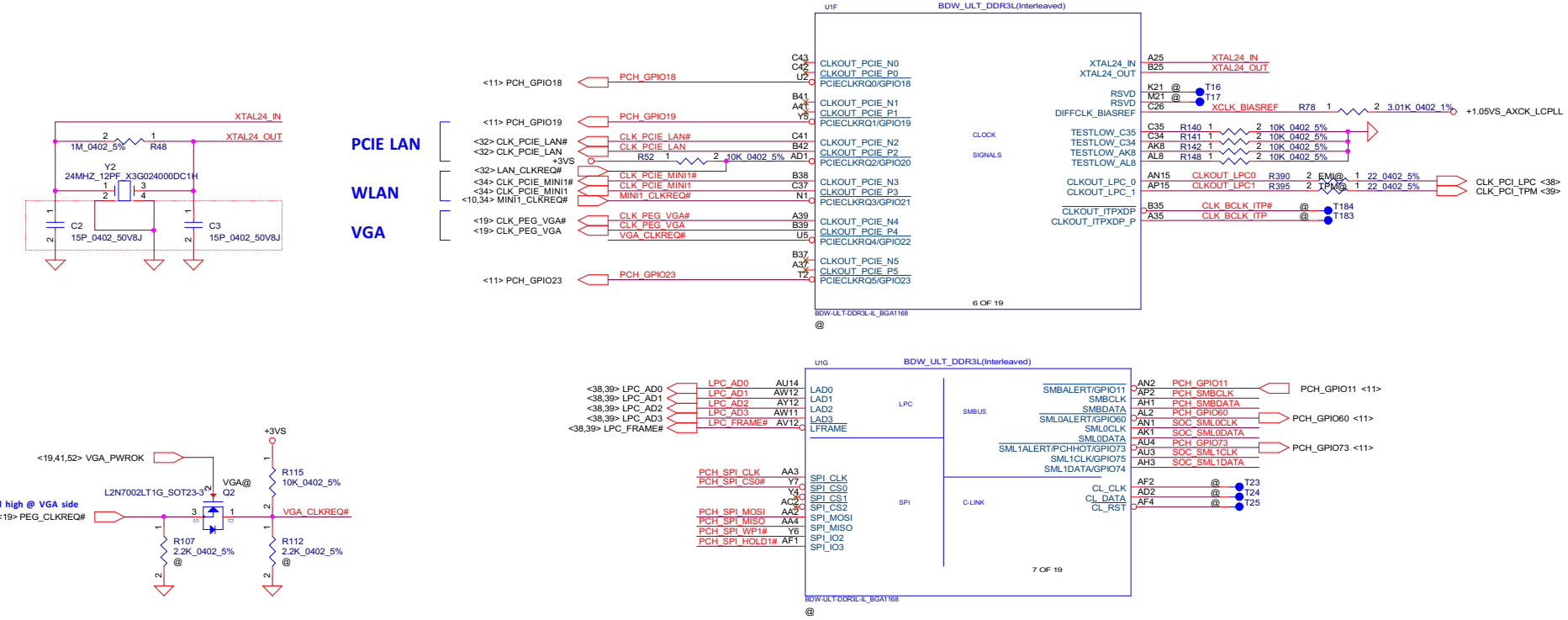
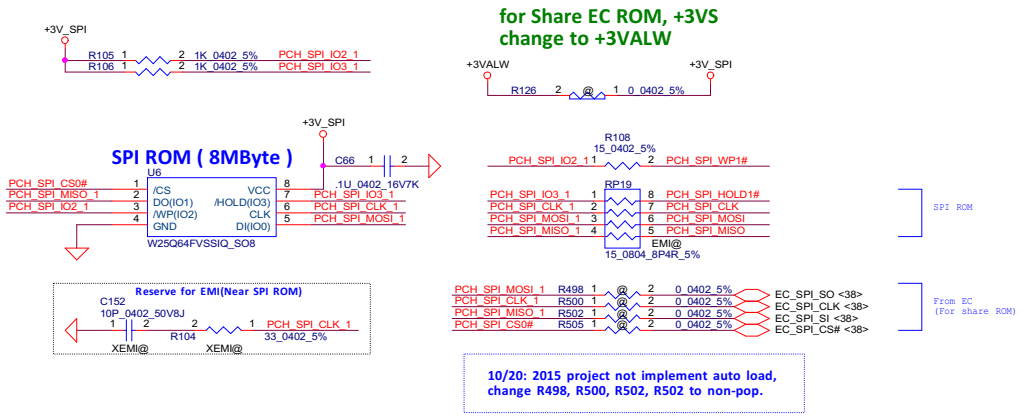
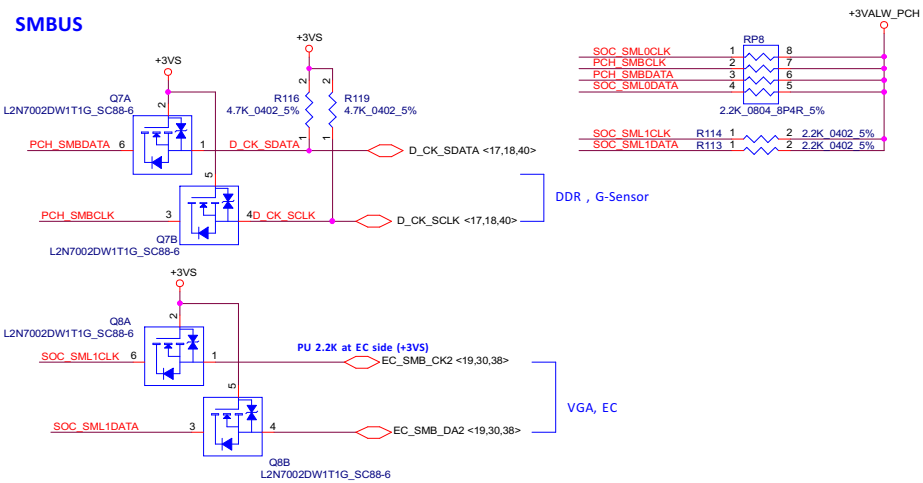


SPI ROM



SMBUS



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Compal Electronics, Inc.	
Title	BDW MCP(4/11) CLK,SPI,SMBUS
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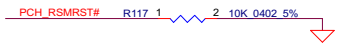
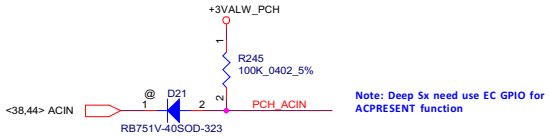
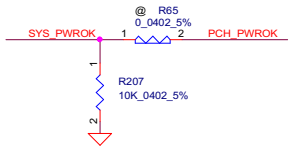
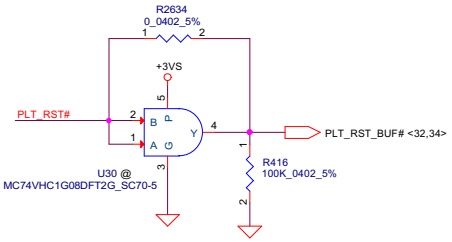
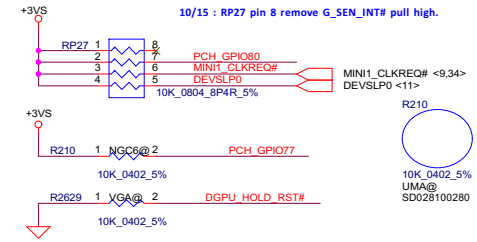
System Power Management

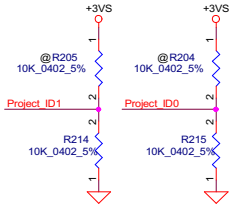




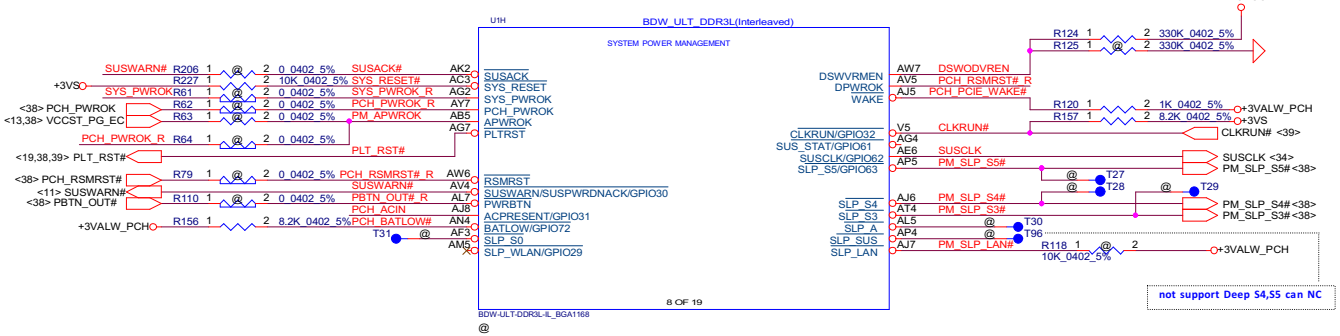


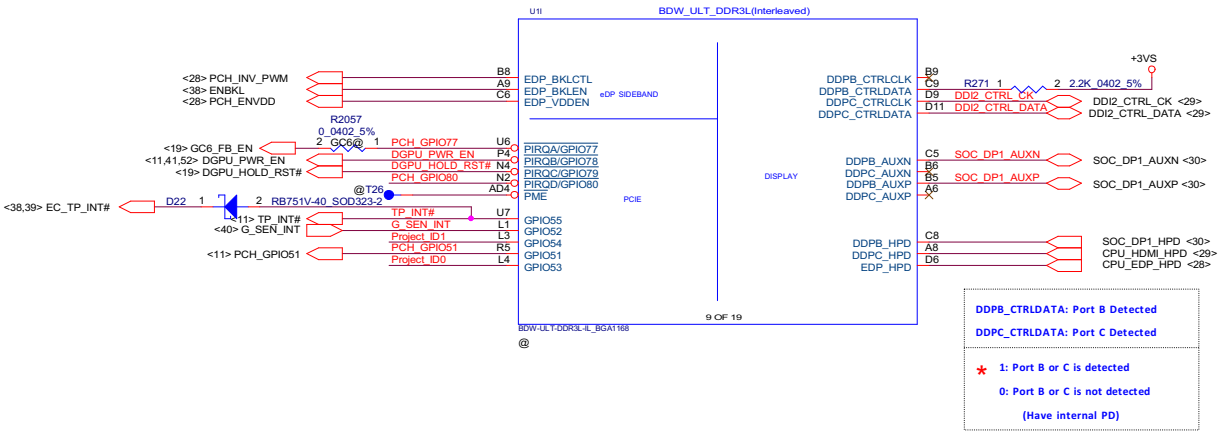






Project ID	Project_ID1 GPIO54	Project_ID0 GPIO53
*A4WAB	0	0
Reserved	0	1
Reserved	1	0
Reserved	1	1





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Title	BDW MCP(5/11) PM,GPIO,DDI		
Size	DocumentNumber		Rev
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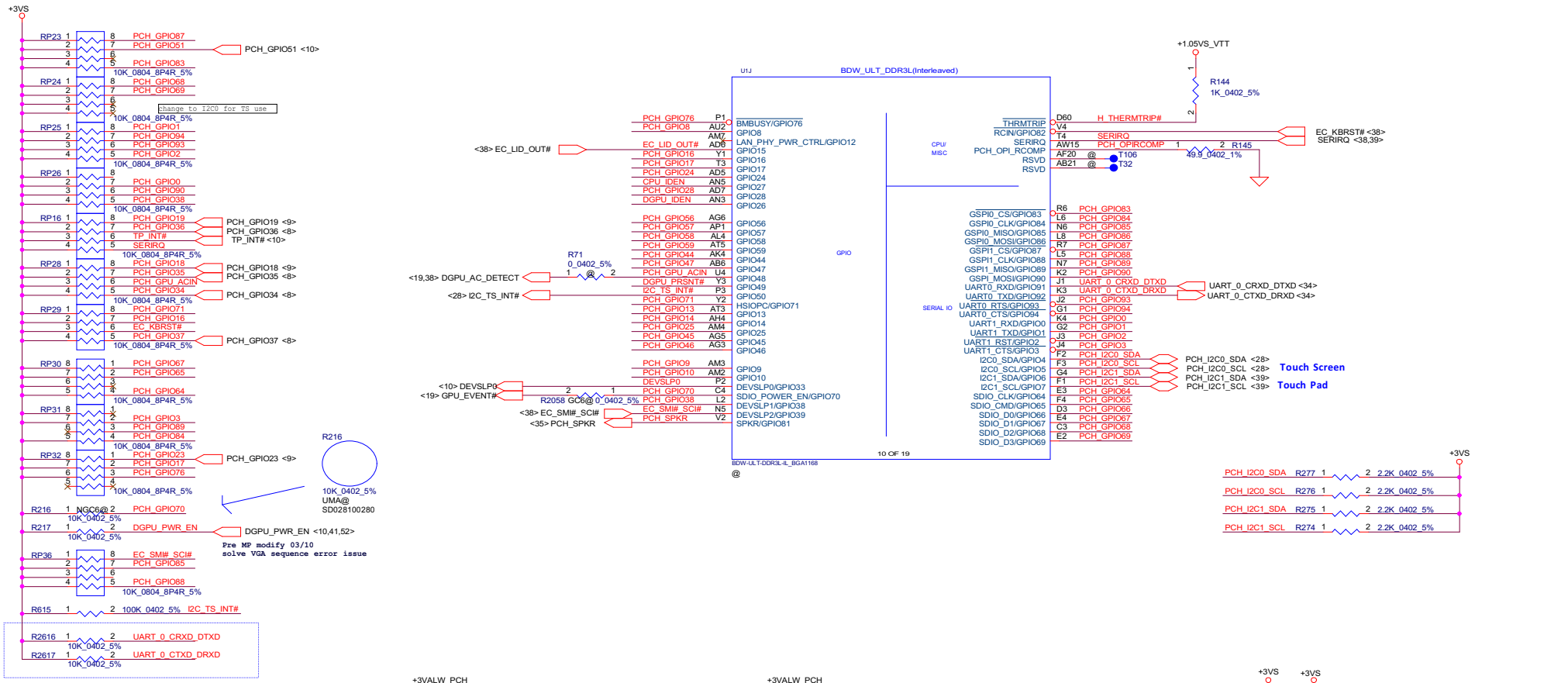

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Compal Electronics, Inc.

Title: BDW MCP(6/11) GPIO,LPIO

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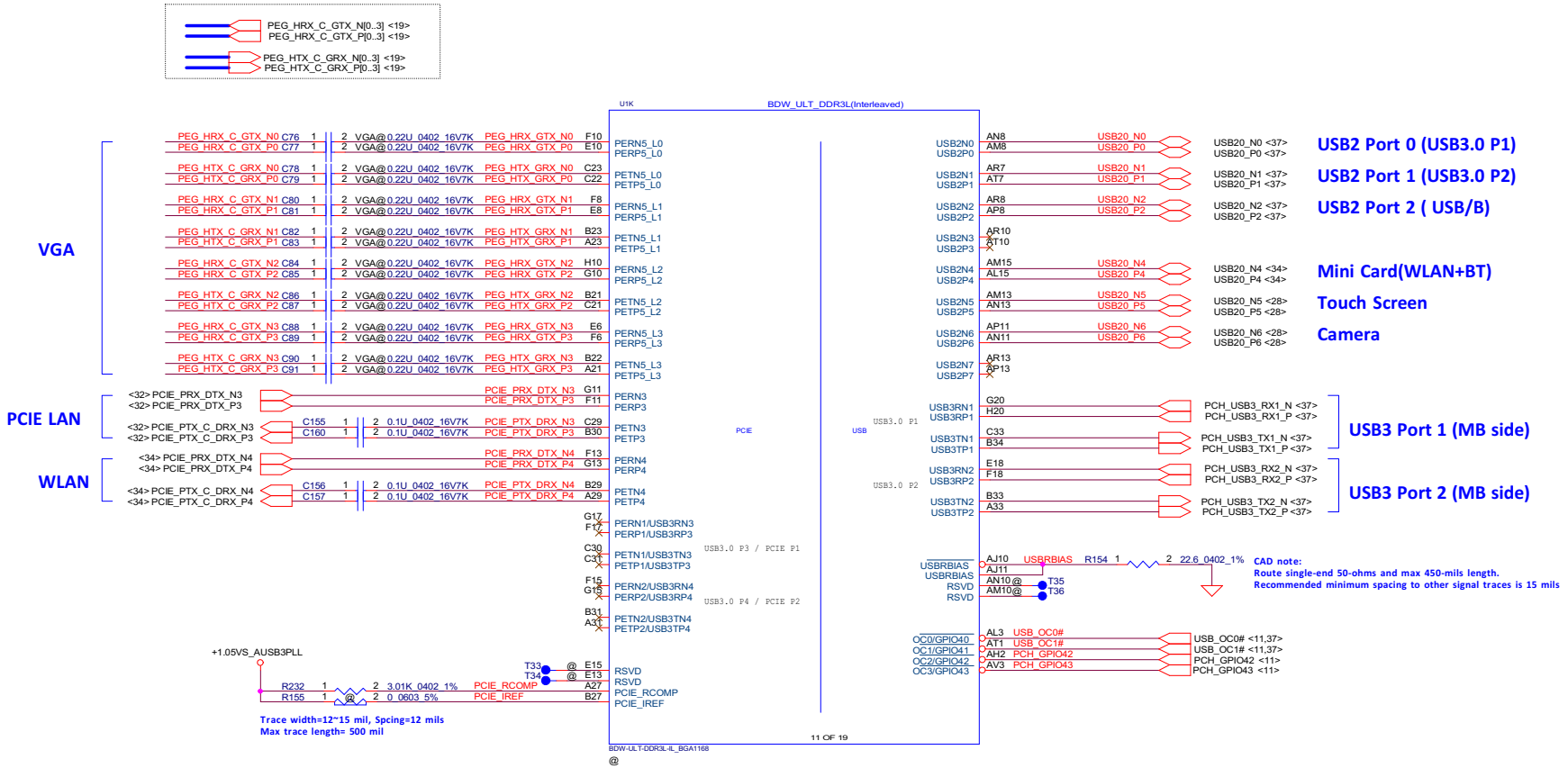

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Compal Electronics, Inc.			
Title	BDW MCP(7/11) PCIE,USB		
Size	Custom	DocumentNumber	A4WAB M/B LA-C341P
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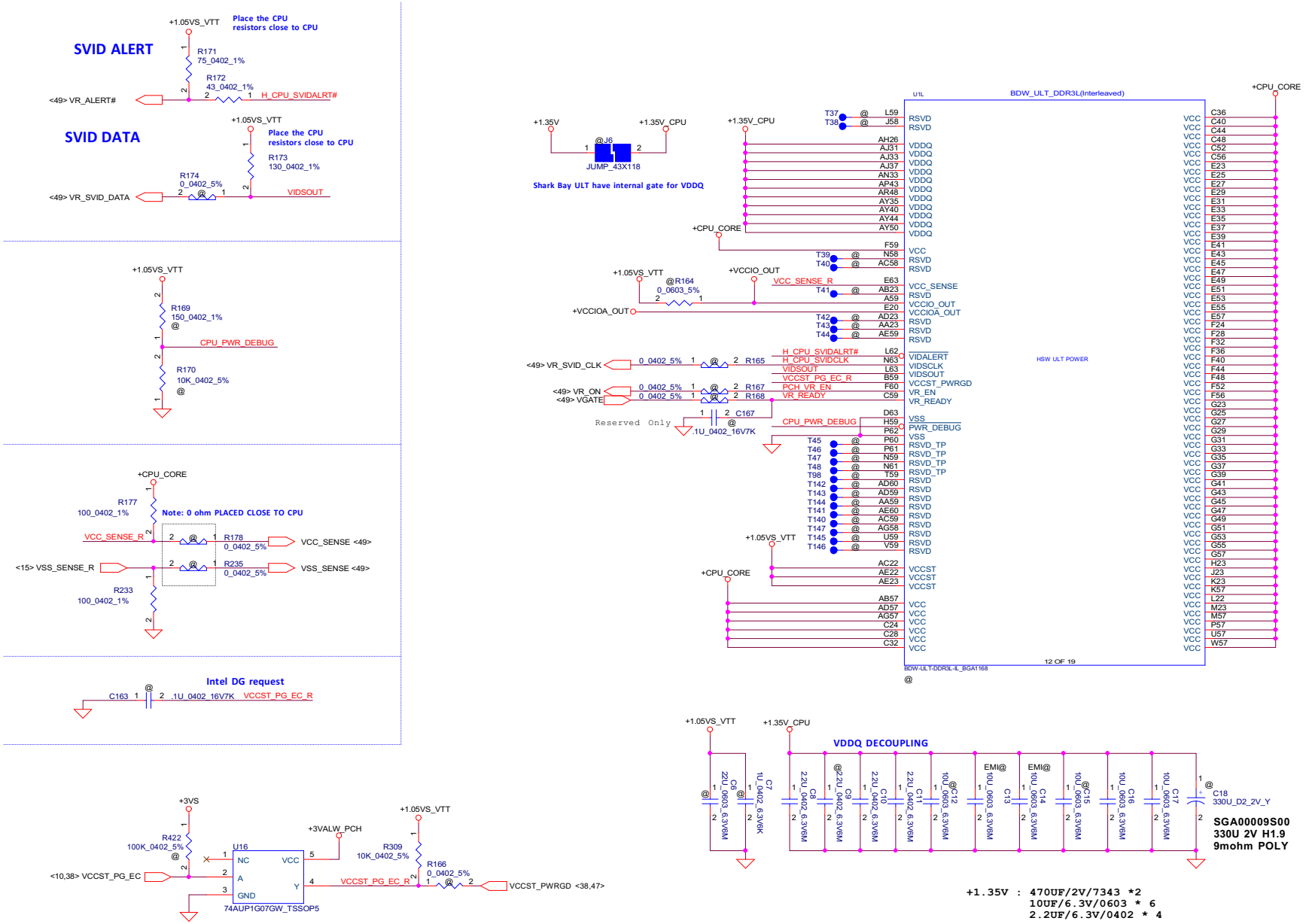

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Compal Electronics, Inc.	
Title	BDW MCP(8/11) Power
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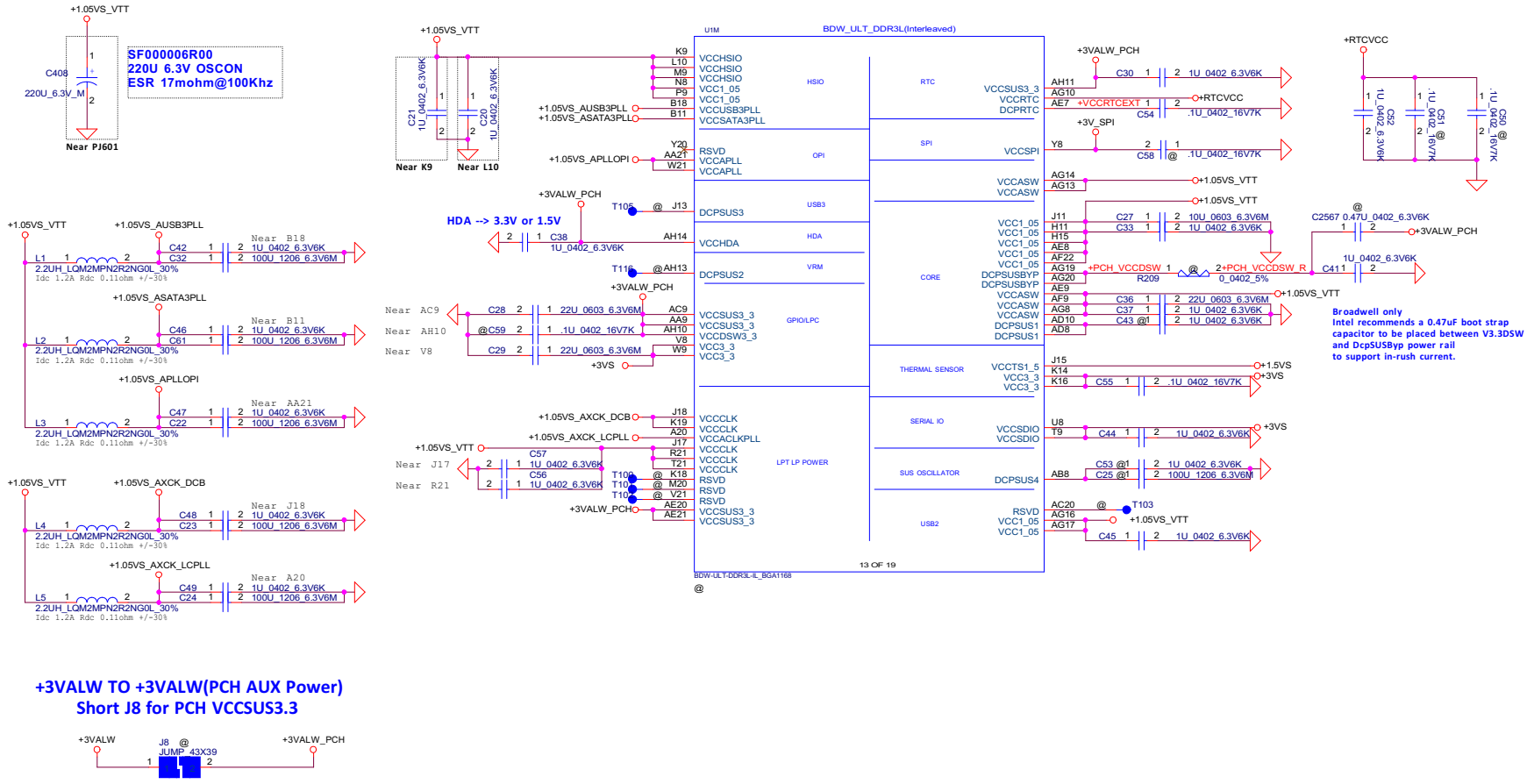

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Compal Electronics, Inc.			
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Size: Custom	DocumentNumber: A4WAB M/B LA-C341P		Rev: 0.2
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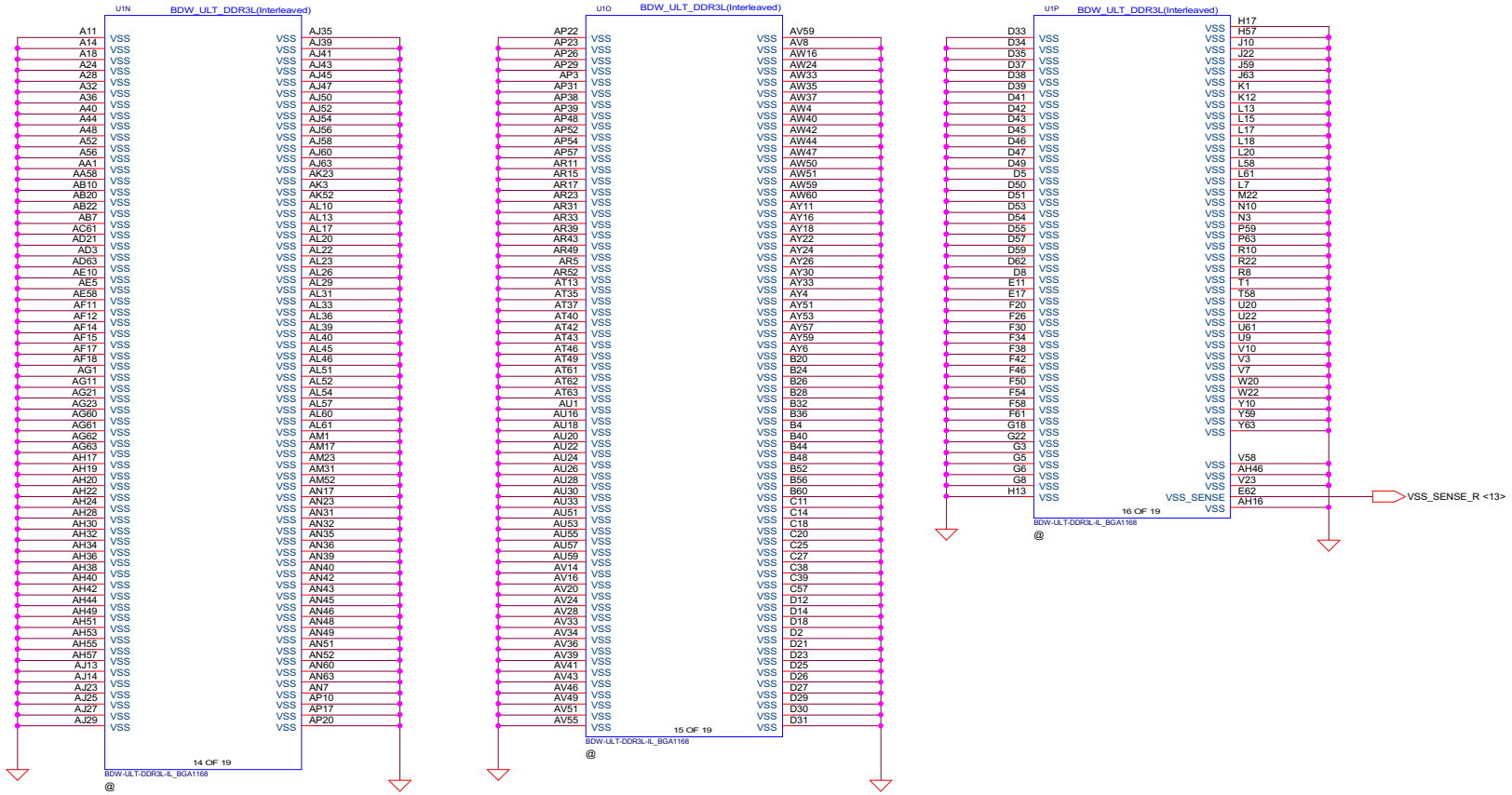

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Compal Electronics, Inc.			
Title	HSW MCP(10/11) GND		
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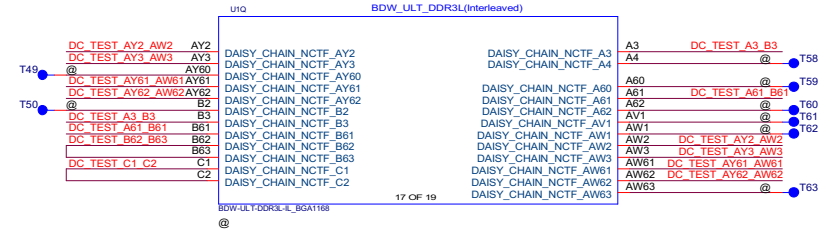
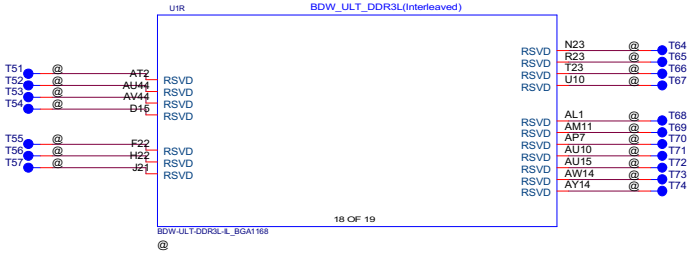
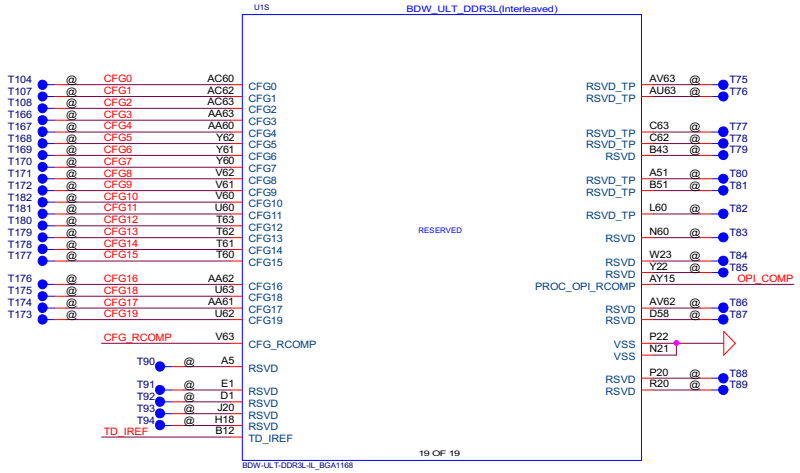
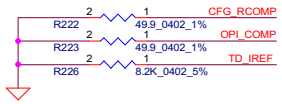
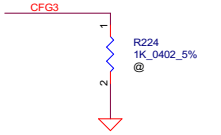




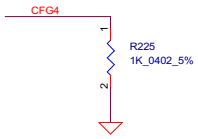




CFG Straps for Processor



Physical Debug Enable (DFX Privacy)	
CFG3	1: DISABLED 0: ENABLED; SET DFX ENABLED BIT IN DEBUG INTERFACE MSR



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

Security Classification	Compal Secret Data		
Issued Date	2014/09/16	Deciphered Date	2014/05/24

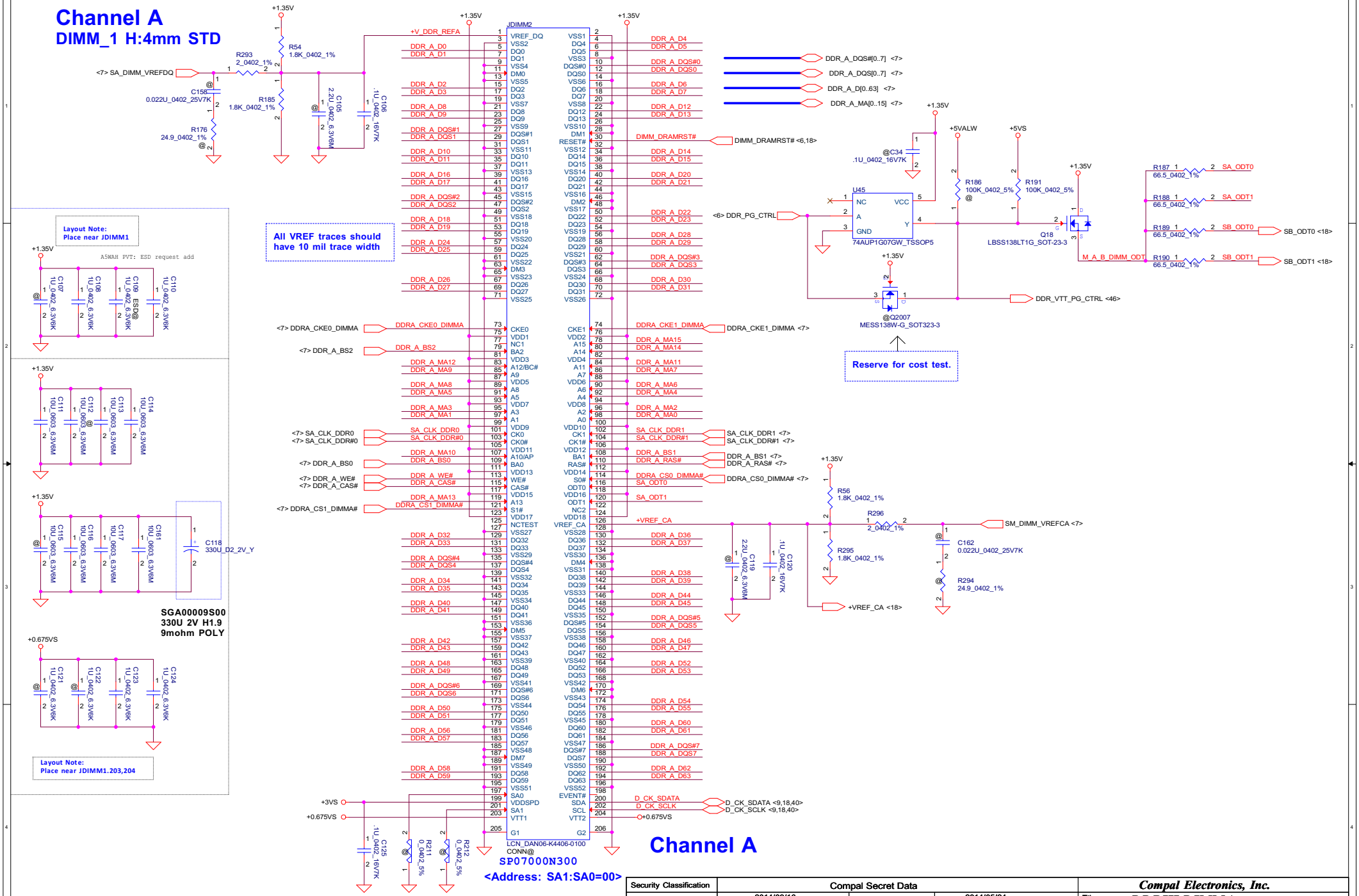
Compal Electronics, Inc.

Title: BDW MCP(11/11) RSVD

Size: Custom | DocumentNumber: A4WAB M/B LA-C341P | Rev: 0.2

Date: Wednesday, March 18, 2015 | Sheet 16 of 56

Channel A
DIMM_1 H:4mm STD



Security Classification	Compal Secret Data		
Issued Date	2014/09/16	Deciphered Date	2014/05/24

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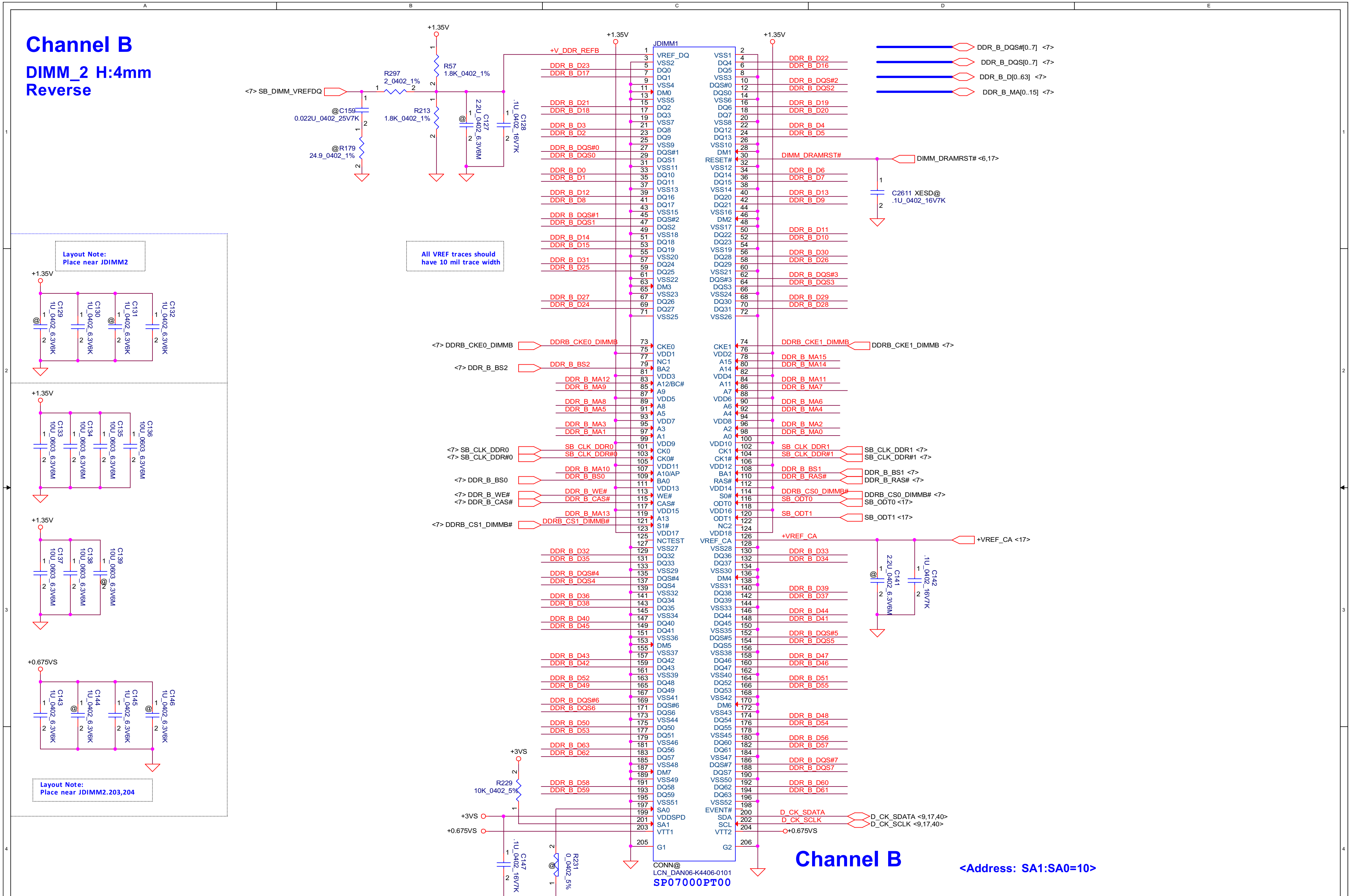
Compal Electronics, Inc.

Title: **DDRIII DIMMA**

Size: Custom | Document Number: **A4WAB M/B LA-C341P** | Rev: 0.2

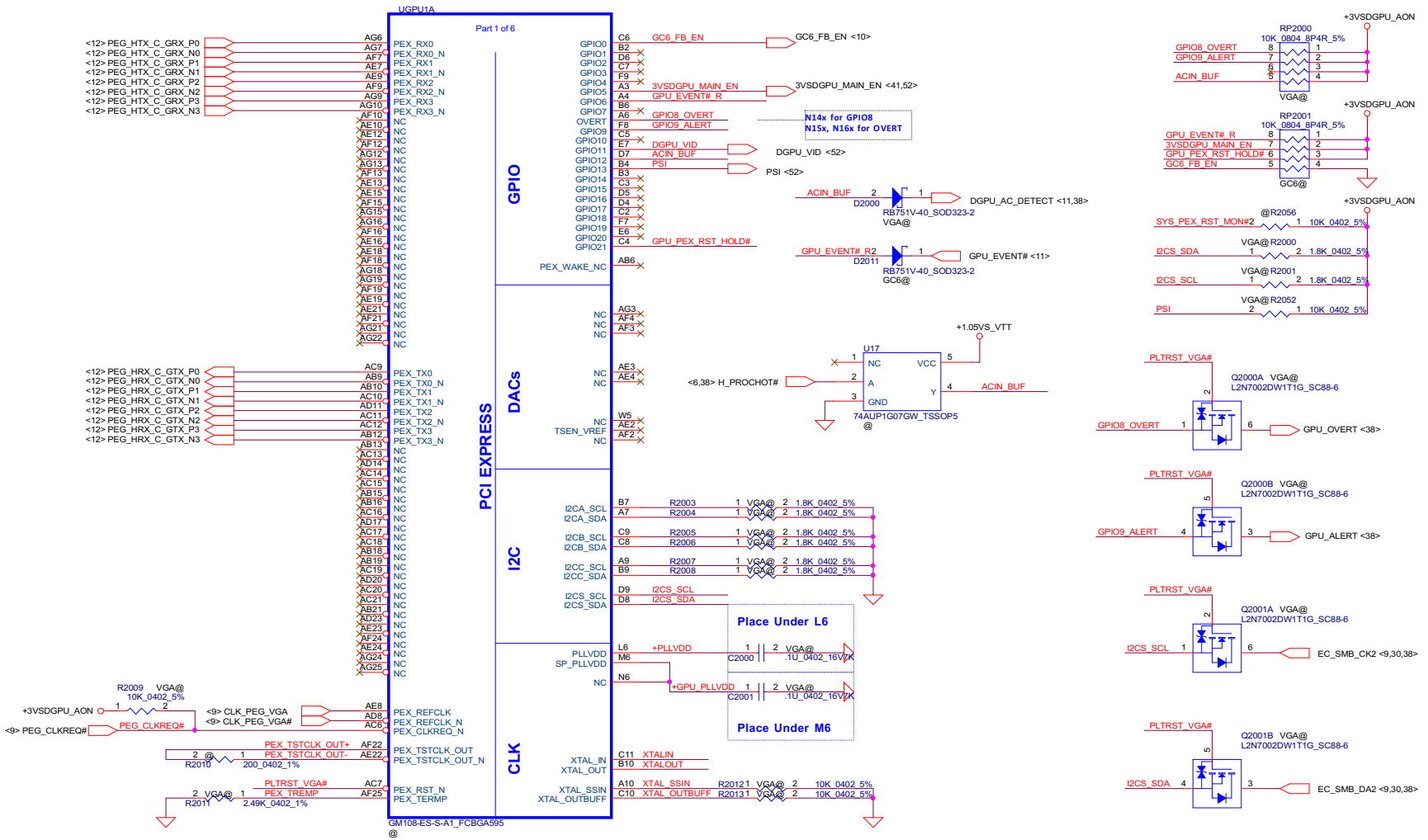
Date: Wednesday, March 18, 2015 | Sheet 17 of 56



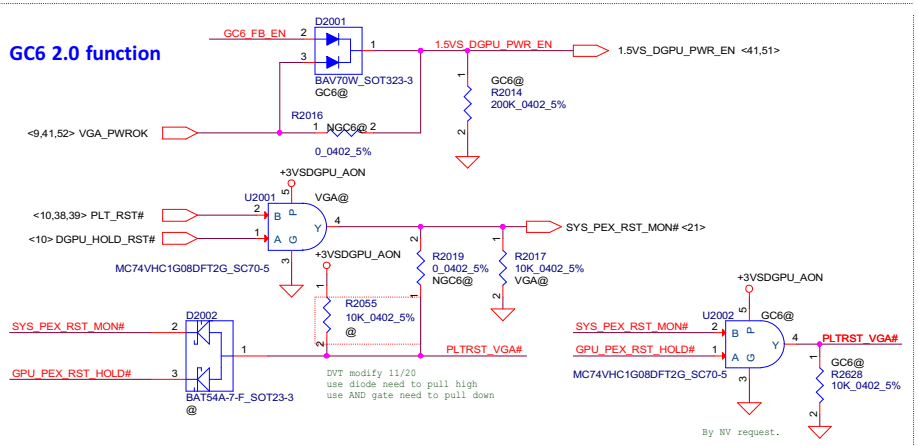
Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2014/09/16	Deciphered Date	2014/05/24	Title: DDRIII DIMMB

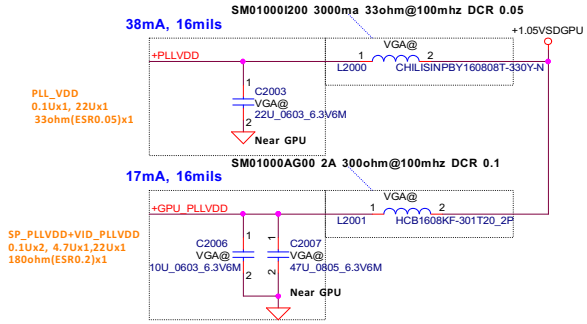
Size: Custom | Document Number: A4WAB M/B LA-C341P | Rev: 0.2

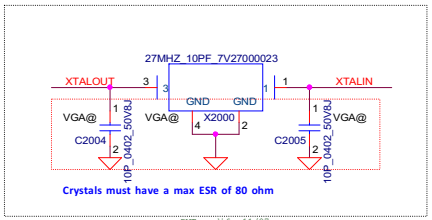
Date: Wednesday, March 18, 2015 | Sheet 18 of 56



GPIO	I/O	USAGE
GPIO0	I	GC6_FB_EN
GPIO1	O	MEM_VDD_CTL
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VCC
GPIO4	O	LCD_BL_EN
GPIO5	O	3V3_MAIN_EN
GPIO6	I	GPU_EVENT#
GPIO7	O	3D Vision
GPIO8	I	SYS_PEX_RST_MON#
GPIO9	I/O	ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	PWM_VID
GPIO12	I	PWR_LEVEL
GPIO13	O	PSI
GPIO14	I	HPD_A
GPIO15	I	HPD_C
GPIO16		RESERVED
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F or HPD_B
GPIO20		Reserved
GPIO21	O	GPU_PEX_RST_HOLD#
GPIO22		
GPIO23		
GPIO24		







Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2014/05/24

Compal Electronics, Inc.	
Title	N16X PEG & GPIO 1/9
Size: Custom	DocumentNumber: A4WAB M/B LA-C341P
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Date: Wednesday, March 18, 2015	Sheet 19 of 56

VRAM Interface

UGPU1

N16S-GT
SGT@
SA000087F10

R3 P/N:

UGPU1

N16V-GM
VGM@
SA000088R20

R3 P/N:

<24,25> MDA[15..0] → MDA[15..0]
<24,25> MDA[31..16] → MDA[31..16]
<26,27> MDA[47..32] → MDA[47..32]
<26,27> MDA[63..48] → MDA[63..48]

UGPU1B

Part 2 of 6

MEMORY INTERFACE A

MDA0	E18	FBA_D00	
MDA1	F18	FBA_D01	
MDA2	E16	FBA_D02	
MDA3	F17	FBA_D03	
MDA4	D20	FBA_D04	
MDA5	D21	FBA_D05	
MDA6	F20	FBA_D06	
MDA7	E21	FBA_D07	
MDA8	E15	FBA_D08	
MDA9	D15	FBA_D09	
MDA10	F15	FBA_D10	
MDA11	F13	FBA_D11	
MDA12	C13	FBA_D12	
MDA13	B13	FBA_D13	
MDA14	E13	FBA_D14	
MDA15	D13	FBA_D15	
MDA16	B15	FBA_D16	
MDA17	C16	FBA_D17	
MDA18	A13	FBA_D18	
MDA19	A15	FBA_D19	
MDA20	B18	FBA_D20	
MDA21	A18	FBA_D21	
MDA22	A19	FBA_D22	
MDA23	C19	FBA_D23	
MDA24	B24	FBA_D24	
MDA25	C23	FBA_D25	
MDA26	A25	FBA_D26	
MDA27	A24	FBA_D27	
MDA28	A21	FBA_D28	
MDA29	B21	FBA_D29	
MDA30	C20	FBA_D30	
MDA31	C21	FBA_D31	
MDA32	R22	FBA_D32	
MDA33	R24	FBA_D33	
MDA34	T22	FBA_D34	
MDA35	R23	FBA_D35	
MDA36	N25	FBA_D36	
MDA37	N26	FBA_D37	
MDA38	N23	FBA_D38	
MDA39	N24	FBA_D39	
MDA40	V23	FBA_D40	
MDA41	V22	FBA_D41	
MDA42	T23	FBA_D42	
MDA43	U22	FBA_D43	
MDA44	Y24	FBA_D44	
MDA45	AA24	FBA_D45	
MDA46	Y22	FBA_D46	
MDA47	AA23	FBA_D47	
MDA48	AD27	FBA_D48	
MDA49	AB25	FBA_D49	
MDA50	AD26	FBA_D50	
MDA51	AC25	FBA_D51	
MDA52	AA27	FBA_D52	
MDA53	AA26	FBA_D53	
MDA54	W26	FBA_D54	
MDA55	Y25	FBA_D55	
MDA56	R26	FBA_D56	
MDA57	T25	FBA_D57	
MDA58	N27	FBA_D58	
MDA59	R27	FBA_D59	
MDA60	V26	FBA_D60	
MDA61	V27	FBA_D61	
MDA62	W27	FBA_D62	
MDA63	W25	FBA_D63	

	F16	FB_PLLAVDD_1	
	P22	FB_PLLAVDD_2	
T97 @	D23	FB_VREF_PROBE	
	H22	FB_DLLAVDD	
	F3	FB_CLAMP	
	F22	FBA_CMD34	
	J22	FBA_CMD35	

FBA_CMD0	C27	CMDA0	CMDA[31..0] <24,25,26,27>
FBA_CMD1	C26	CMDA1	
FBA_CMD2	E24	CMDA2	
FBA_CMD3	F24	CMDA3	
FBA_CMD4	D27	CMDA4	
FBA_CMD5	D26	CMDA5	
FBA_CMD6	F25	CMDA6	
FBA_CMD7	F26	CMDA7	
FBA_CMD8	F23	CMDA8	
FBA_CMD9	G22	CMDA9	
FBA_CMD10	G23	CMDA10	
FBA_CMD11	G24	CMDA11	
FBA_CMD12	F27	CMDA12	
FBA_CMD13	G25	CMDA13	
FBA_CMD14	G27	CMDA14	
FBA_CMD15	G26	CMDA15	
FBA_CMD16	M24	CMDA16	
FBA_CMD17	M23	CMDA17	
FBA_CMD18	K24	CMDA18	
FBA_CMD19	K23	CMDA19	
FBA_CMD20	M27	CMDA20	
FBA_CMD21	M26	CMDA21	
FBA_CMD22	M25	CMDA22	
FBA_CMD23	K26	CMDA23	
FBA_CMD24	K22	CMDA24	
FBA_CMD25	J23	CMDA25	
FBA_CMD26	J25	CMDA26	
FBA_CMD27	J24	CMDA27	
FBA_CMD28	K27	CMDA28	
FBA_CMD29	K25	CMDA29	
FBA_CMD30	J27	CMDA30	
FBA_CMD31	J26	CMDA31	

PVT modify 01/13
DQSA, DQSA# reverse

FBA_DQM0	D19	DQMA0	DQMA[3..0] <24,25>
FBA_DQM1	D14	DQMA1	
FBA_DQM2	C17	DQMA2	
FBA_DQM3	C22	DQMA3	
FBA_DQM4	P24	DQMA4	DQMA[7..4] <26,27>
FBA_DQM5	W24	DQMA5	
FBA_DQM6	AA25	DQMA6	
FBA_DQM7	U25	DQMA7	
FBA_DQS_RN0	F19	DQSA#0	DQSA#[3..0] <24,25>
FBA_DQS_RN1	C14	DQSA#1	
FBA_DQS_RN2	A16	DQSA#2	
FBA_DQS_RN3	A22	DQSA#3	
FBA_DQS_RN4	P25	DQSA#4	DQSA#[7..4] <26,27>
FBA_DQS_RN5	W22	DQSA#5	
FBA_DQS_RN6	AB27	DQSA#6	
FBA_DQS_RN7	T27	DQSA#7	
FBA_DQS_WP0	E19	DQSA0	DQSA[3..0] <24,25>
FBA_DQS_WP1	C15	DQSA1	
FBA_DQS_WP2	B16	DQSA2	
FBA_DQS_WP3	B22	DQSA3	DQSA[7..4] <26,27>
FBA_DQS_WP4	R25	DQSA4	
FBA_DQS_WP5	W23	DQSA5	
FBA_DQS_WP6	AB26	DQSA6	
FBA_DQS_WP7	T26	DQSA7	

FBA_CLK0	D24	CLKA0 <24,25>	
FBA_CLK0_N	D25	CLKA0# <24,25>	
FBA_CLK1	N22	CLKA1 <26,27>	
FBA_CLK1_N	M22	CLKA1# <26,27>	
FBA_WCK01	D18		
FBA_WCK01_N	C18		
FBA_WCK23	D17		
FBA_WCK23_N	D16		
FBA_WCK45	T24		
FBA_WCK45_N	U24		
FBA_WCK67	V24		
FBA_WCK67_N	V25		

GM108-ES-S-A1_FCBGA595
@

NV 15x DG-06803-V03
NV 16x DG-07158-V04

GPU Package	Rail	Capacitor Type		Footprint	Population	Location
GB2B-64	FBx_PLL_AVDD and FB_DLL_AVDD Combined	0.1 µF	X7R	0402	2	Under GPU
		22 µF	X5R	0805	1	Near GPU
		Bead Type				
		30 Ω (ESR=0.010 Ω)		0603	1	Near GPU

SM01000I200 3000ma 33ohm@100mhz DCR 0.05

+1.05VSDGPU → VGA@ L2002 CHILISINPBY160808T-330Y-N → +FB_PLLAVDD
15+55mA

C2008 22U_0603_6.3V6M VGA@
C2011 .1U_0402_16V7K VGA@
C2010 .1U_0402_16V7K VGA@
C2009 .1U_0402_16V7K VGA@

Place Near GPU
Place Under F16 P22 H22

1 VGA@ 2 10K_0402_5% R2028 FB_CLAMP

+1.5VSDGPU → 60.4_0402_1% R2020 FBA_CMD34
+1.5VSDGPU → 60.4_0402_1% R2022 FBA_CMD35

+1.5VSDGPU

A5MUB exchange

RP33 VGA@ 100_0804_8P4R_5%: CMDA23, CMDA21
RP42 VGA@ 100_0804_8P4R_5%: CMDA24, CMDA26
RP43 VGA@ 100_0804_8P4R_5%: CMDA10, CMDA22
RP44 VGA@ 100_0804_8P4R_5%: CMDA4, CMDA12
RP45 VGA@ 100_0804_8P4R_5%: CMDA8, CMDA14
RP46 VGA@ 100_0804_8P4R_5%: CMDA9, CMDA29
RP47 VGA@ 100_0804_8P4R_5%: CMDA5, CMDA13
RP48 VGA@ 100_0804_8P4R_5%: CMDA6, CMDA7
RP49 VGA@ 100_0804_8P4R_5%: CMDA27, CMDA30
RP50 VGA@ 100_0804_8P4R_5%: CMDA28, CMDA25
RP51 VGA@ 100_0804_8P4R_5%: CMDA15, CMDA11

+1.5VSDGPU
C2083 @ .1U_0402_16V7K
C2084 @ .1U_0402_16V7K
C2085 @ .1U_0402_16V7K
C2086 @ .1U_0402_16V7K
C2087 @ .1U_0402_16V7K
C2088 @ .1U_0402_16V7K
C2090 @ .1U_0402_16V7K
C2091 @ .1U_0402_16V7K
C2093 @ .1U_0402_16V7K
C2089 @ .1U_0402_16V7K
C2092 @ .1U_0402_16V7K

Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2014/05/24

Compal Electronics, Inc.

Title: N16X VRAM 2/9

Size: Custom | DocumentNumber: A4WAB M/B LA-C341P | Rev: 0.2

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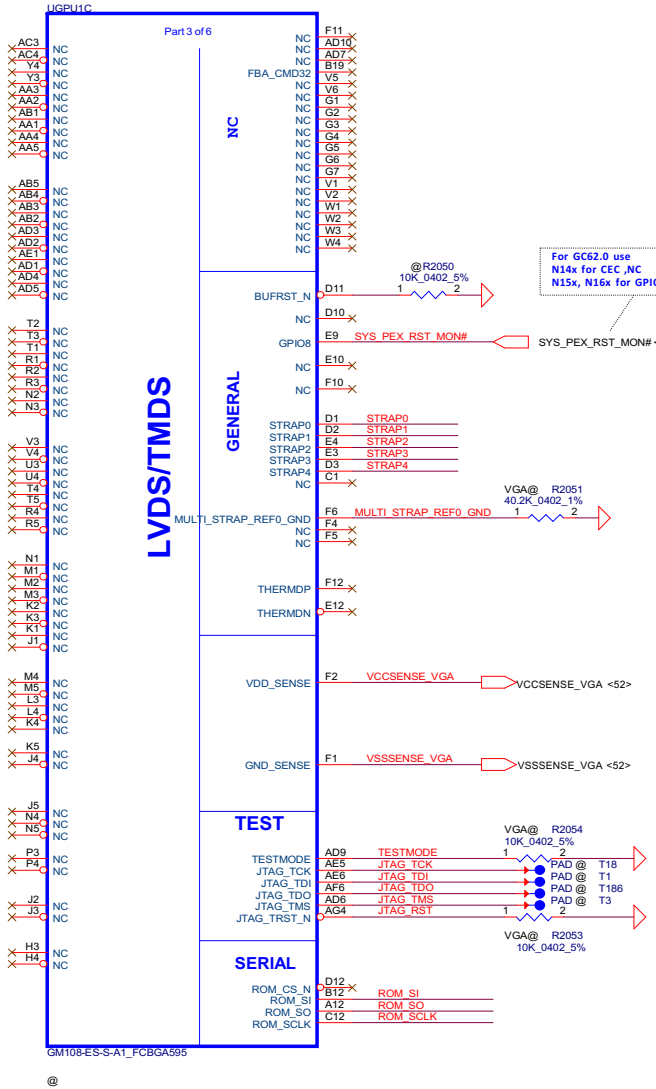
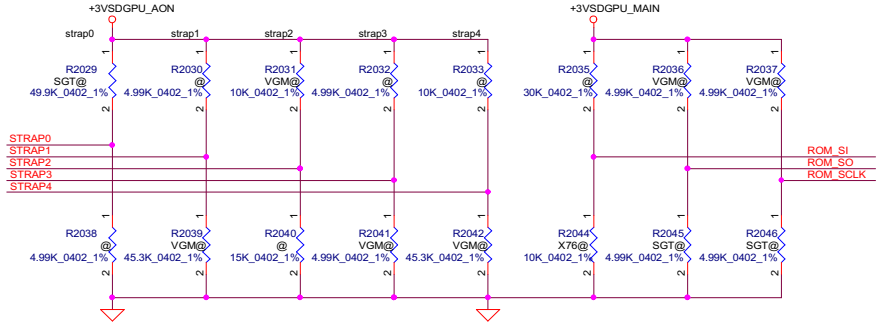


MULTI LEVEL STRAPS



N16V-GM Option Component

STRAP0 ---> R2029 2 VGM@ 45.3K_0402_1% SD034453280

For N16S-GT Binary strap table — Decive ID : 0x1347

GPU	VRAM Voltage	RANK	X76	Freq	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N16S-GT	+1.5V	Dual	X76614BOL05	1GHz	256Mx16x8 4G	0x0 (SA00006E840) Hynix H5TC4G63AFR-11C	PU 49.9K	NC	NC	NC	NC	PD 4.99K	PD 4.99K	PD 4.99K
			X76614BOL04			0x1 (SA000077K20) Micron MT41J256M16HA-093G:E						PD 10K		
			X76614BOL06			0x2 (SA000076P20) Samsung K4W4G1646D-BC1A						PD 15K		
			X76614BOL14			0xC (SA00008DN10) Hynix H5TC4G63CFR-N0C						PU 24.9K		
	+1.5V	Single	X76614BOL11	1GHz	256Mx16x4 2G	0x0 (SA00006E840) Hynix H5TC4G63AFR-11C						PD 4.99K		
			X76614BOL10			0x1 (SA000077K20) Micron MT41J256M16HA-093G:E						PD 10K		
			X76614BOL12			0x2 (SA000076P20) Samsung K4W4G1646D-BC1A						PD 15K		
			X76614BOL16			0x5 (SA00008DN10) Hynix H5TC4G63CFR-N0C						PD 30.1K		

For N16V-GM Binary strap table — Decive ID : 0x1299

GPU	VRAM Voltage	RANK	X76	Freq	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N16V-GM	+1.35V	Dual	X76614BOL08	900MHz	256Mx16x8 4G	0xE (SA00006E840) Hynix H5TC4G63AFR-11C	PU 45.3K	PD 45.3K	PU 10K	PD 4.99K	PD 45.3K	PU 34.8K	PU 4.99K	PU 4.99K
			X76614BOL07			0xD (SA000077K20) Micron MT41J256M16HA-093G:E						PU 30.1K		
			X76614BOL09			0xC (SA000076P20) Samsung K4W4G1646D-BC1A						PU 24.9K		
			X76614BOL15			0xA (SA00008DN10) Hynix H5TC4G63CFR-N0C						PU 15K		
	+1.5V	Single	X76614BOL02	1GHz	256Mx16x4 2G	0x2 (SA00006E840) Hynix H5TC4G63AFR-11C						PD 15K		
			X76614BOL01			0x1 (SA000077K20) Micron MT41J256M16HA-093G:E						PD 10K		
			X76614BOL03			0x4 (SA000076P20) Samsung K4W4G1646D-BC1A						PD 24.9K		
			X76614BOL13			0x9 (SA00008DN10) Hynix H5TC4G63CFR-N0C						PU 10K		

Compal Electronics, Inc.

Title: N16X STRAPS 3/9

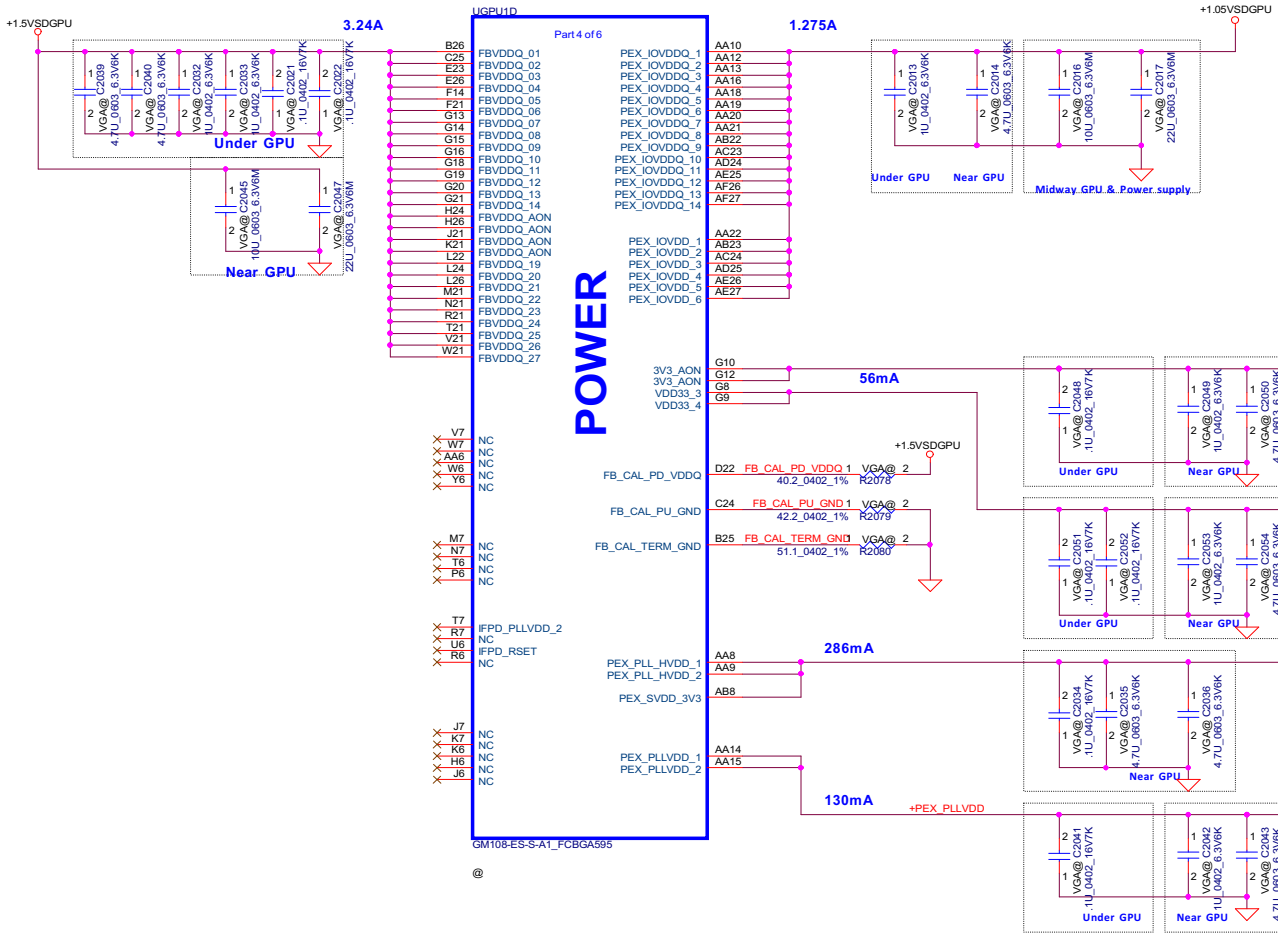
Size: Custom | Document Number: A4WAB M/B LA-C341P | Rev: 0.2

Date: Wednesday, March 18, 2015 | Sheet 21 of 56

NV 15x DG-06803-V03
NV 16x DG-07158-V04

GPU Package Type	Capacitor Type		Footprint		Population	Location
GB2B-64 DDR3	0.1μF	X7R	0402	2	2	Under GPU
	1 μF	X7R	0603	2	2	Under GPU
	4.7 μF	X6S	0603	2	2	Under GPU
	10 μF	X5R	0805	1	1	Near GPU
	22 μF	X5R	0805	1	1	Near GPU

GPU Package Type	Capacitor Type		Footprint	Population	Location
GB2B-64	1.0 μF	X6S	0402	1	Under GPU
	4.7 μF	X6S	0603	1	Near GPU
	10 μF	X5R	0805	1	Midway between GPU and Power Supply
	22 μF	X5R	0805	1	Midway between GPU and Power Supply

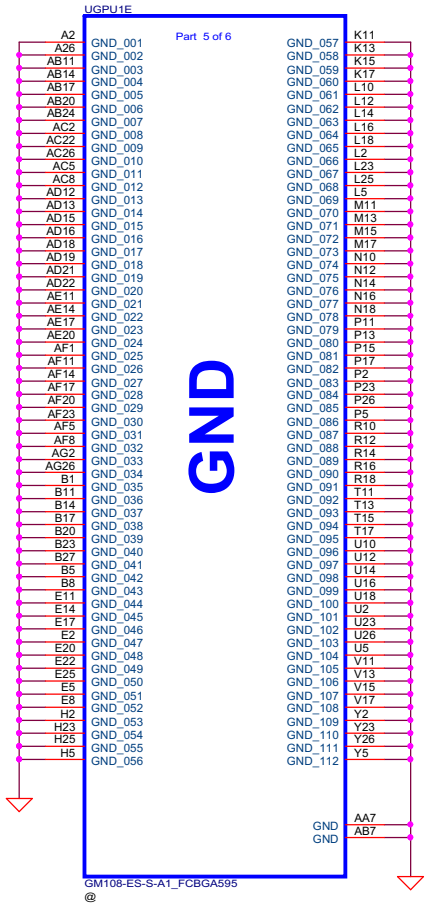


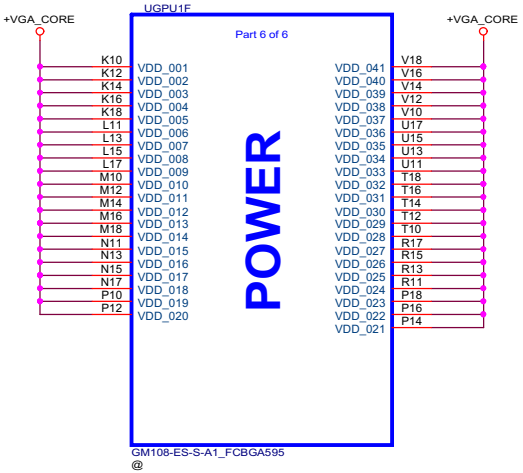
GPU Package	Rail	Capacitor Type		Footprint		Population	Location
GB2B-64 GB4B-128 GB3-256	3V3_MAIN	0.1μF	X6S	0402	2	2	Under GPU
		1 μF	X5R	0603	1	1	Near GPU
		4.7 μF	X5R	0603	1	1	Near GPU
GB2B-64 GB4B-128 GB3-256	3V3_AON	0.1μF	X6S	0402	1	1	Under GPU
		1 μF	X5R	0603	1	1	Near GPU
		4.7 μF	X5R	0603	1	1	Near GPU

Capacitor Type		Footprint	Population	Location
0.1 μF	X5R	0402	1	Near GPU
4.7 μF	X5R	0603	2	Near GPU

Capacitor Type		Footprint	Population	Location
0.1 μF	X6S	0402	1	Under GPU
1.0 μF	X5R	0603	1	Near GPU
4.7 μF	X5R	0805	1	Near GPU

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/10/01	Deciphered Date 2014/05/24	Title N16X POWER & GND 4/9
			Size Custom DocumentNumber A4WAB M/B LA-C341P Rev 0.2
			Date: Wednesday, March 18, 2015 Sheet 22 of 56





NV 15x DG-06803-V03
NV 16x DG-07158-V04

GPU Package Type	Capacitor Type		Footprint		Population	Location	Comments
GB2B-64	4.7 µF	X6S	0603	10	10	Under GPU	
	1 µF	X6S	0402	4	4	Under GPU	
	47 µF	X5R	0805	1	1	Near GPU	
	22 µF	X5R	0805	1	1	Near GPU	
	4.7 µF	X5R	0805	5	5	Near GPU	
	330 µF	POS	7343	1	1	Near GPU	ESR ≤ 6 mΩ

DA-07312-V02

Table 6. EDP-Peak [3]

Products	VRM Type	GPU Core	GPU FBIO			FB Total [1,5]	1.05V Total [2]
		–	1.5V [4]	1.35V [4]	1.5V [4]	1.35V [4]	1.05V [4]
		(A)	(A)	(A)	(A)	(A)	(A)
N16S-GT	DDR3/L	51	2.56	2.18	4.08	3.63	2.09
N16S-GM	DDR3/L	32	2.56	2.18	4.08	3.62	2.09
N16S-LP	DDR3L	29	N/A	2.13	N/A	3.54	2.09

Notes:
1. FB Total = GPU FBIO + VRAM IO + VRAM Core = FBVDD + FBVDDQ
2. 1.05V Total includes the PCIe and other 1.05V power rails.
3. Worst case current is observed at the temperature of the GPS Thermal Control Limit defined in Table 3.
4. Power supply rail voltages set to maximum DC tolerance.
5. VRAM Total power is for reference only. For absolute ratings, please contact VRAM manufacturer.

DA-07314-V02

Table 6. EDP-Peak [3]

Products	VRM Type	GPU Core	GPU FBIO	FB Total [1,5]	1.05V Total [2]
		–	1.5/1.35V [4]	1.5/1.35V [4]	1.05V [4]
		(A)	(A)	(A)	(A)
N16V-GM	DDR3/L	40.97	3.87	5.86	1.74

Notes:
1. FB Total = GPU FBIO + VRAM IO + VRAM Core = FBVDD + FBVDDQ
2. 1.05V Total includes the PCIe and other 1.05V power rails.
3. Worst case current is observed at the temperature of the GPS Thermal Control Limit defined in Table 3.
4. Power supply rail voltages set to maximum DC tolerance.
5. VRAM Total power is for reference only. For absolute ratings, please contact VRAM manufacturer.

Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2014/05/24

Compal Electronics, Inc.

Title: N16X POWER & GND 5/9

Size: Custom | Document Number: A4WAB M/B LA-C341P | Rev: 0.2

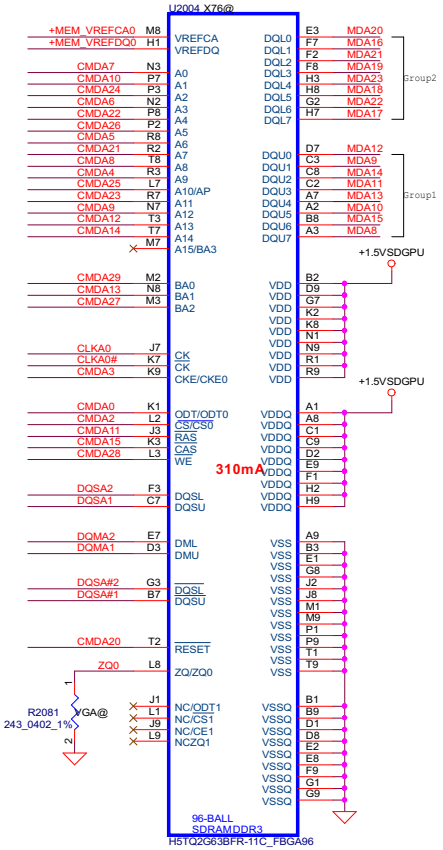
Date: Wednesday, March 18, 2015 | Sheet 23 of 56

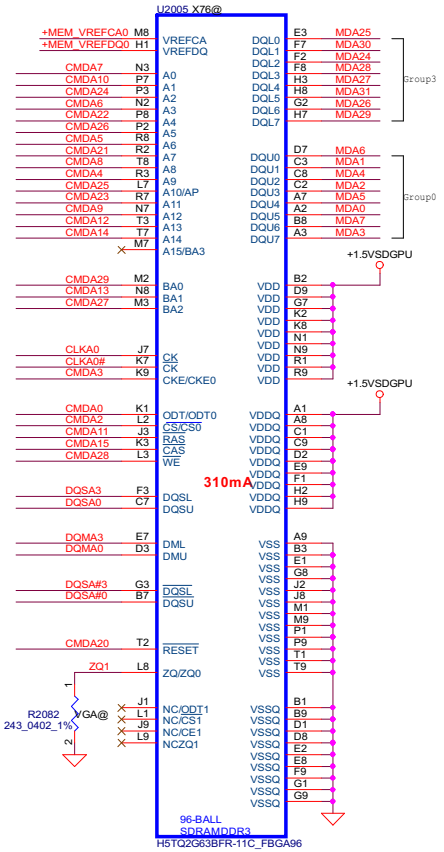
VRAM DDR3 chips

<20,25,26,27> DQSA[7..0] → DQSA[7..0]
<20,25,26,27> DQSA#[7..0] → DQSA#[7..0]
<20,25,26,27> DQMA[7..0] → DQMA[7..0]
<20,25,26,27> MDA[63..0] → MDA[63..0]
<20,25,26,27> CMDA[30..0] → CMDA[30..0]

Lower Rank 0 BOT SIDE

VRAM P/N: SA00006E840



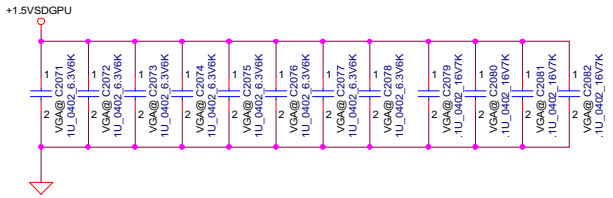


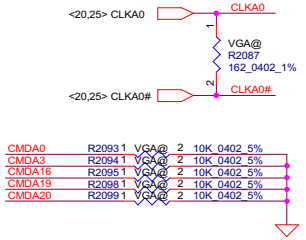
Mode E Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1*	
CMD2	CS0*			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS*	RAS*	RAS*	RAS*
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS*	CAS*	CAS*	CAS*
CMD16		ODT		ODT
CMD17				CS1*
CMD18		CS0*		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE*	WE*
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE*	WE*	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2
Not Available				

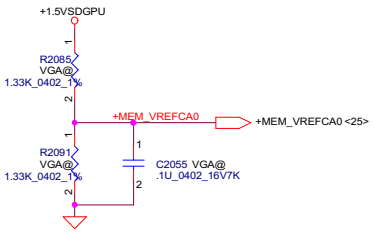
	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

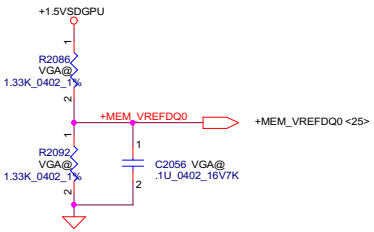
Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

Capacitor Type			Population FBVDDQ	Population FBVDD	Location
FBVDD/Q Combined					
0.1 µF	X7R	0402	2		Under DRAM
1.0 µF	X7R	0603	4		Under DRAM
10 µF	X5R	0805	0		Close to DRAM









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Issued Date	2013/10/01	Deciphered Date	2014/05/24

Compal Electronics, Inc.

Title: N16X Upper Rank0 6/9

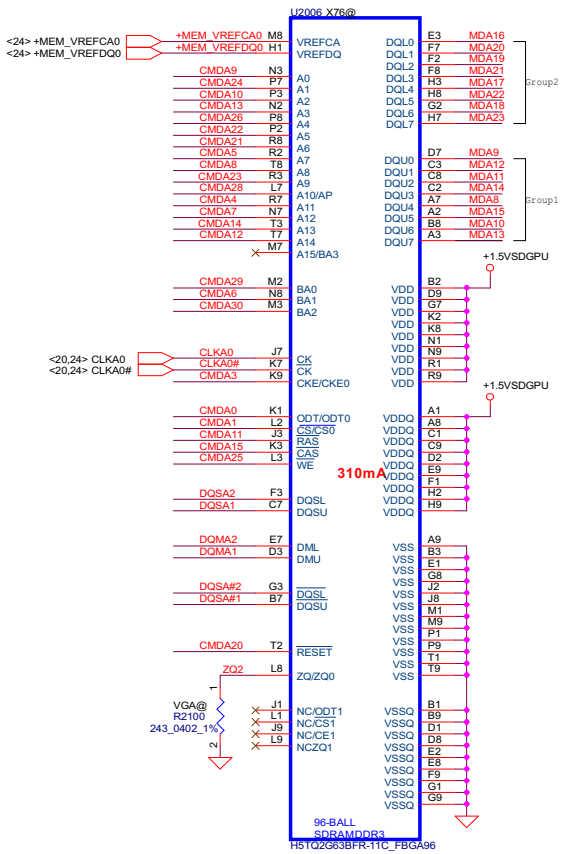
Size: Custom | Document Number: A4WAB M/B LA-C341P | Rev: 0.2

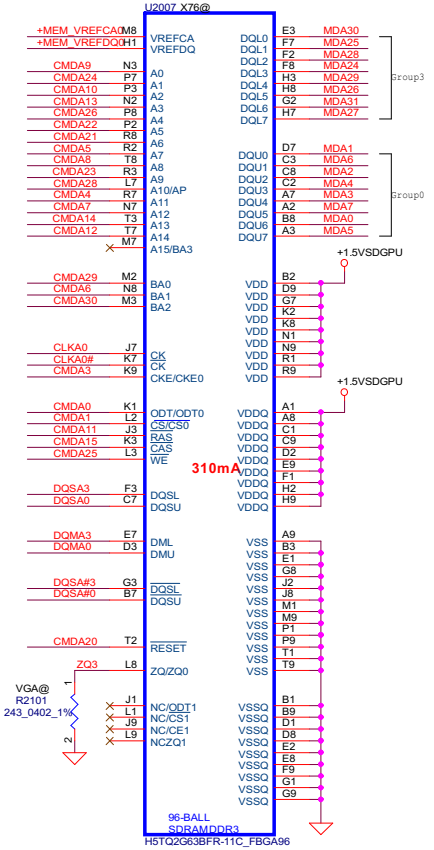
Date: Wednesday, March 18, 2015 | Sheet 24 of 56

VRAM DDR3 chips

<20,24,26,27> DQSA[7..0] → DQSA[7..0]
<20,24,26,27> DQSA#[7..0] → DQSA#[7..0]
<20,24,26,27> DQMA[7..0] → DQMA[7..0]
<20,24,26,27> MDA[63..0] → MDA[63..0]
<20,24,26,27> CMDA[30..0] → CMDA[30..0]

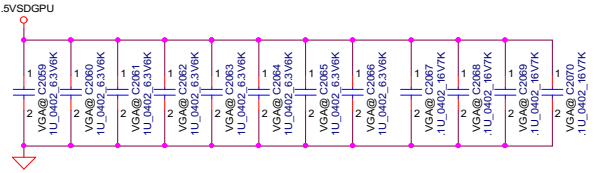
Lower Rank 1 TOP SIDE





Mode E Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1*	
CMD2	CS0*			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS*	RAS*	RAS*	RAS*
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS*	CAS*	CAS*	CAS*
CMD16		ODT		ODT
CMD17				CS1*
CMD18		CS0*		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE*	WE*
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE*	WE*	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2
Not Available				

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination



Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2014/05/24

Compal Electronics, Inc.

Title: N16X Upper Rank1 7/9

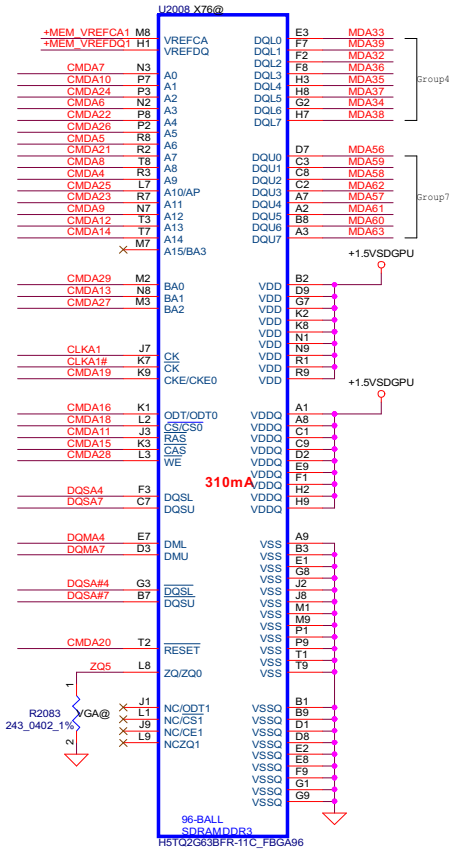
Size: Custom | DocumentNumber: A4WAB M/B LA-C341P | Rev: 0.2

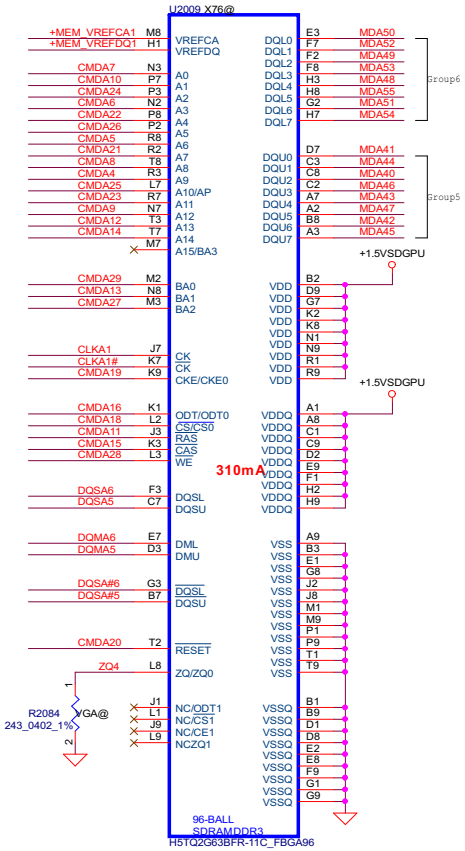
Date: Wednesday, March 18, 2015 | Sheet 25 of 56

VRAM DDR3 chips

<20,24,25,27> DQSA[7..0] DQSA[7..0]
<20,24,25,27> DQSA#[7..0] DQSA#[7..0]
<20,24,25,27> DQMA[7..0] DQMA[7..0]
<20,24,25,27> MDA[63..0] MDA[63..0]
<20,24,25,27> CMDA[30..0] CMDA[30..0]

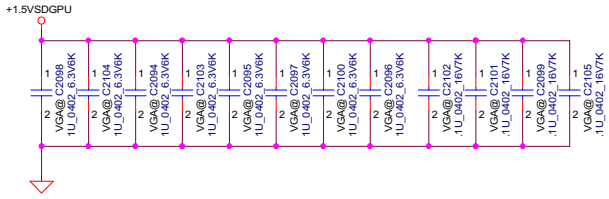
Upper Rank 0 BOT SIDE

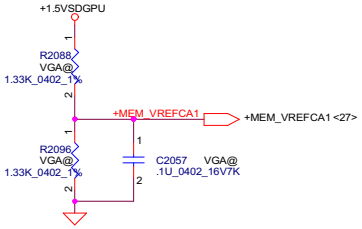


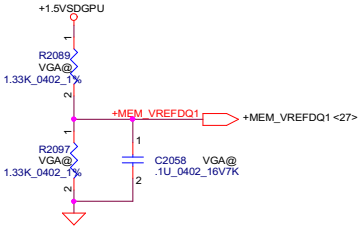


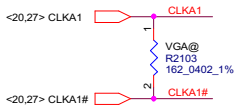
Mode E Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1*	
CMD2	CS0*			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS*	RAS*	RAS*	RAS*
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS*	CAS*	CAS*	CAS*
CMD16		ODT		ODT
CMD17				CS1*
CMD18		CS0*		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE*	WE*
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE*	WE*	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2
Not Available				

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination









Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2014/05/24

Compal Electronics, Inc.

Title: N16X Lower Rank0 8/9

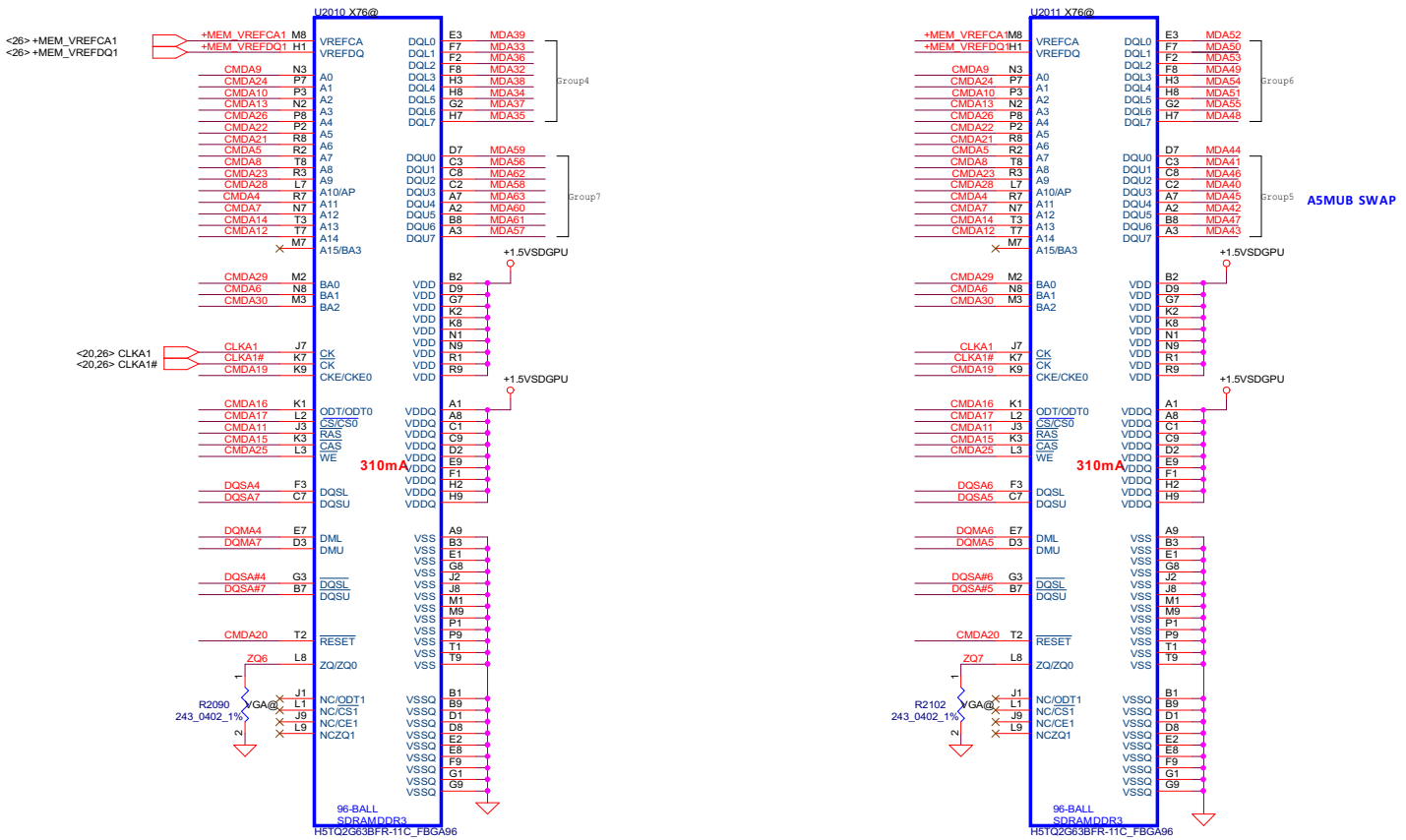
Size: Custom | Document Number: A4WAB M/B LA-C341P | Rev: 0.2

Date: Wednesday, March 18, 2015 | Sheet 26 of 56

VRAM DDR3 chips

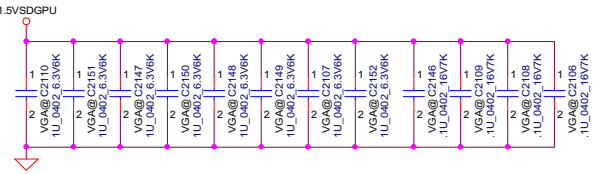
<20,24,25,26> DQSA[7..0] → DQSA[7..0]
<20,24,25,26> DQSA#[7..0] → DQSA#[7..0]
<20,24,25,26> DQMA[7..0] → DQMA[7..0]
<20,24,25,26> MDA[63..0] → MDA[63..0]
<20,24,25,26> CMDA[30..0] → CMDA[30..0]

Upper Rank 1 TOP SIDE



Mode E Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1*	
CMD2	CS0*			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS*	RAS*	RAS*	RAS*
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS*	CAS*	CAS*	CAS*
CMD16		ODT		ODT
CMD17				CS1*
CMD18		CS0*		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE*	WE*
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE*	WE*	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2
Not Available				

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination



Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2014/05/24

Compal Electronics, Inc.

Title: N16X Lower Rank1 9/9

Size: Custom | Document Number: A4WAB M/B LA-C341P | Rev: 0.2

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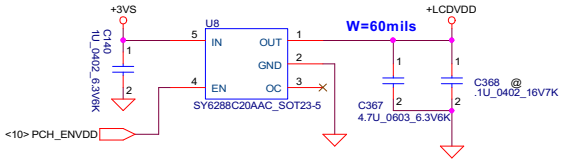
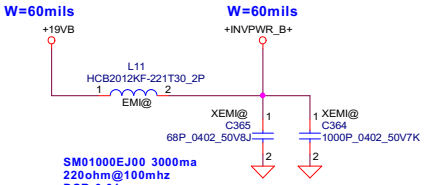
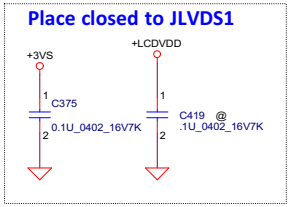
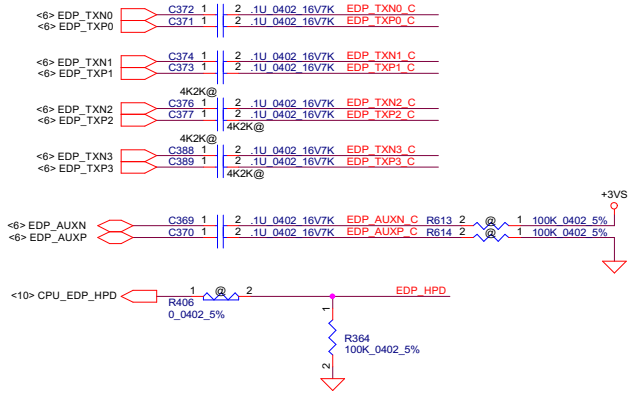
EDP / LVDS conn.

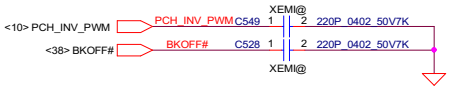
LCD POWER CIRCUIT



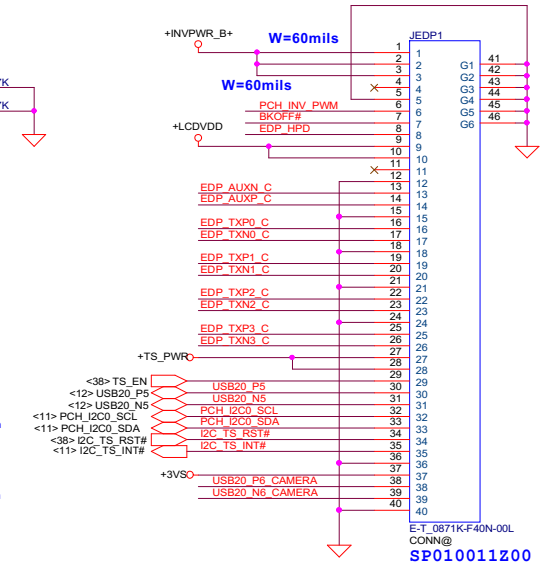




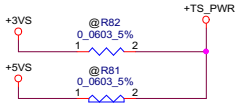




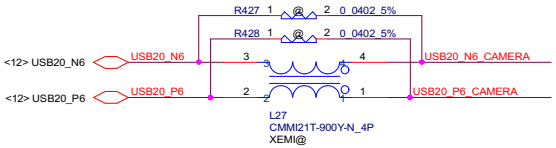
Follow A4QAS pin assignment
LCD/ LED PANEL Conn.



Touch Screen

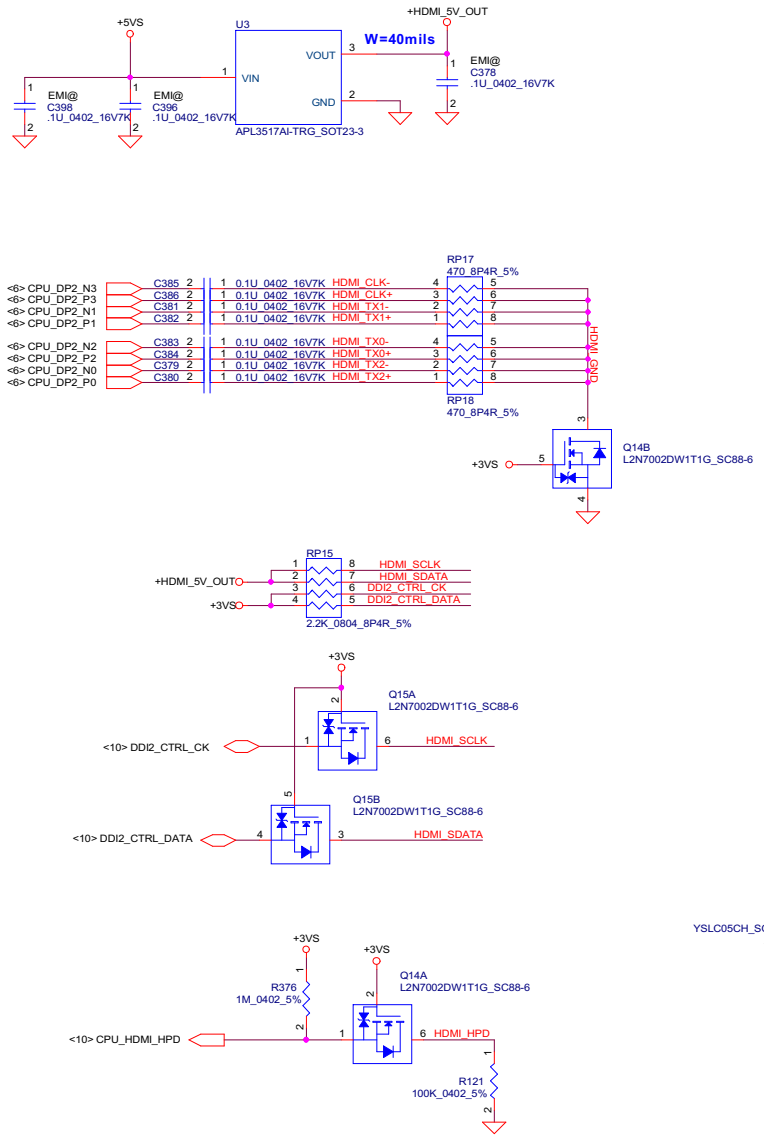


Camera

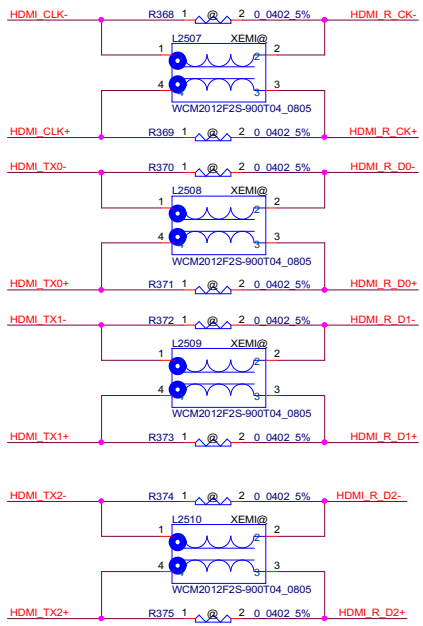


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/09/16	Deciphered Date	2014/05/24
Title	eDP Connector		
Size: Custom	DocumentNumber: A4WAB M/B LA-C341P		Rev: 0.2
Date: Wednesday, March 18, 2015	Sheet 28 of 56		

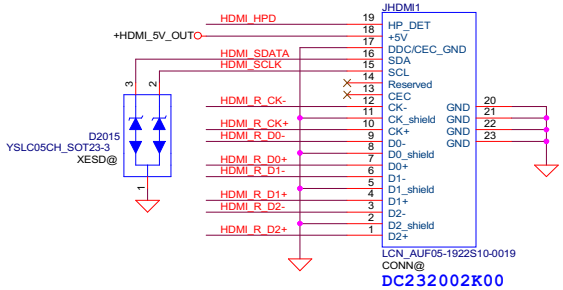
HDMI conn.



SM070001310 400ma 90ohm@100mhz DCR 0.3



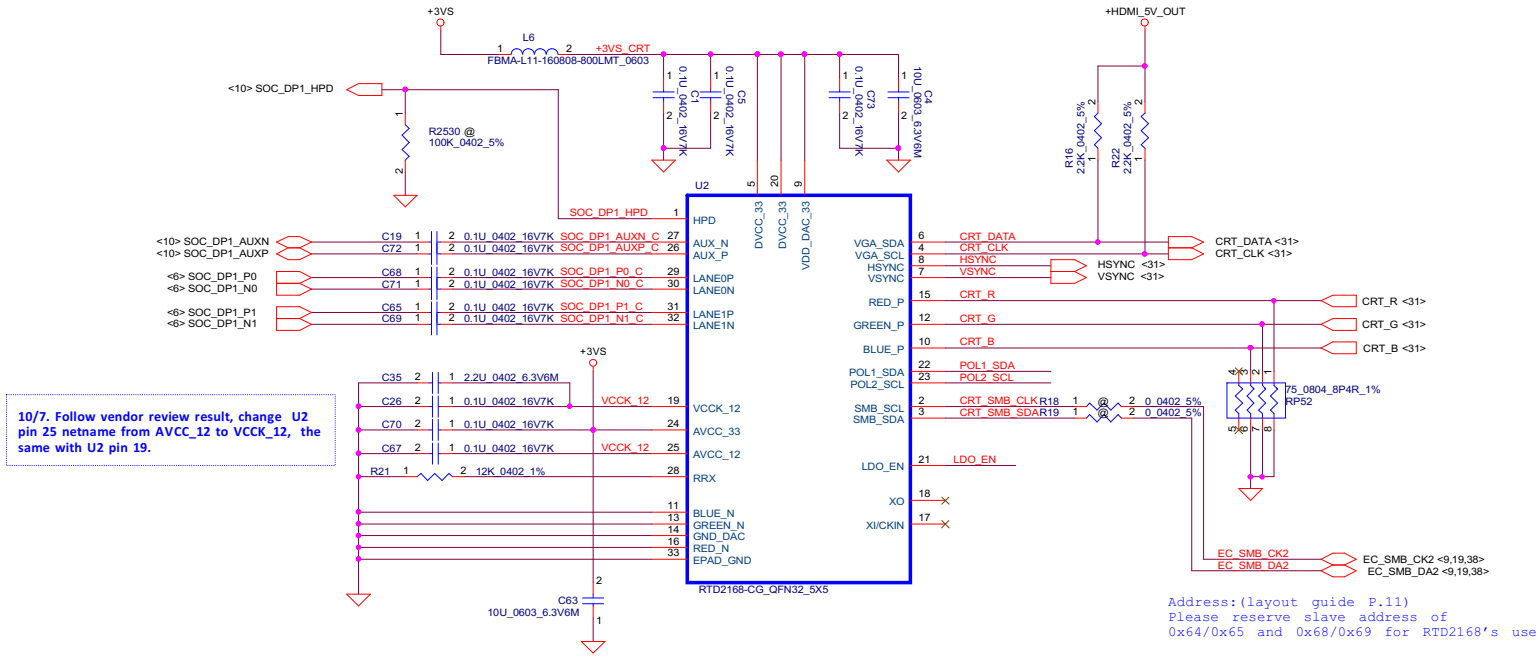
HDMI connector



Security Classification	Compal Secret Data		
Issued Date	2014/09/16	Deciphered Date	2014/05/24

Compal Electronics, Inc.			
Title	HDMI Conn		
Size: Custom	DocumentNumber: A4WAB M/B LA-C341P		Rev: 0.2
Date: Wednesday, March 18, 2015	Sheet 29 of 56		

DP to VGA Realtek RTD2168



		POL_SDA	
		0	1
POL_SCL	0	X	EP
	1	*ROM	EEPROM

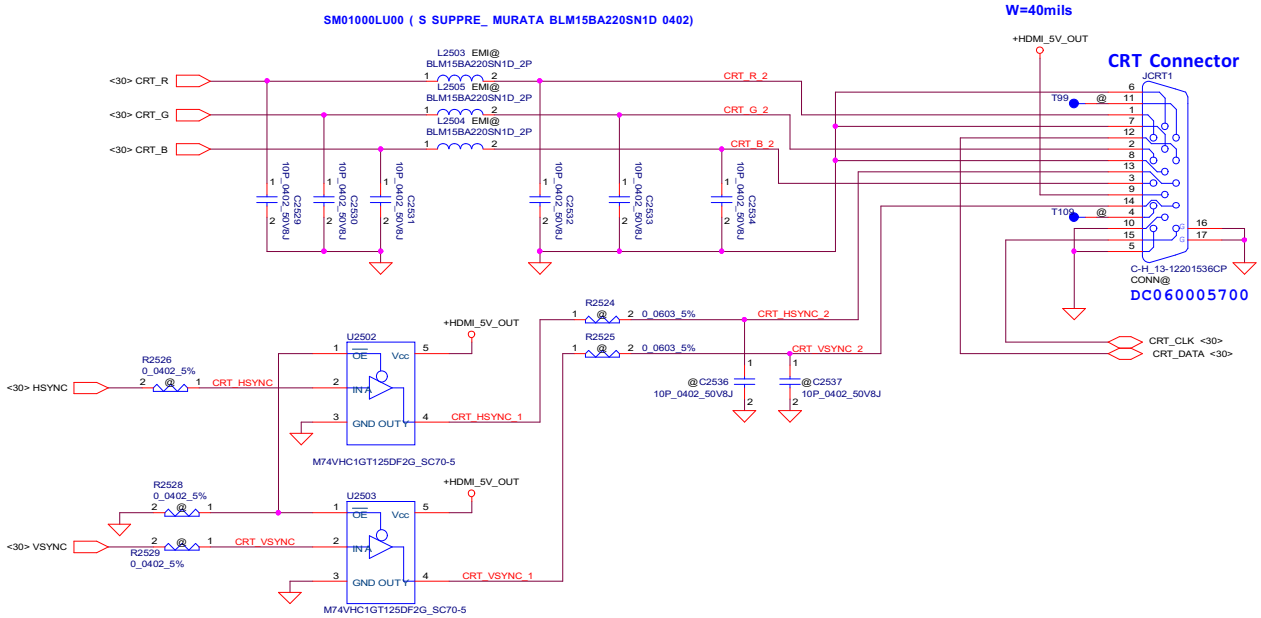
ROM: Internal ROM
EP: Programmed external EC
EEPROM: External ROM

LDO_EN:
*1: Internal 1.2V
0: External 1.2V

Security Classification	Compal Secret Data		
Issued Date	2014/09/16	Deciphered Date	2014/05/24

Compal Electronics, Inc.			
Title	Realtek RTD2168		
Size: Custom	DocumentNumber: A4WAB M/B LA-C341P		Rev: 0.2
Date: Wednesday, March 18, 2015	Sheet 30 of 56		

CRT conn.



SecurityClassification	Compal Secret Data		
Issued Date	2014/09/16	Deciphered Date	2014/05/24

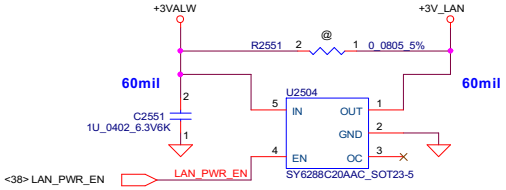
Compal Electronics, Inc.

Title: CRT Connector

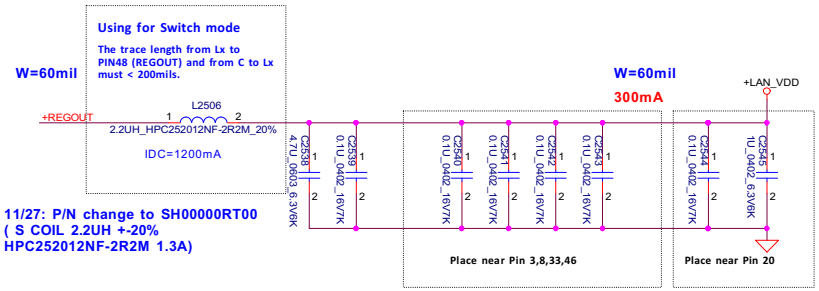
Size: Custom | DocumentNumber: A4WAB M/B LA-C341P | Rev: 0.2

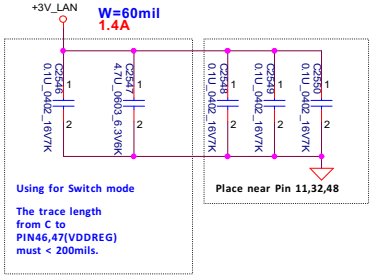
Date: Wednesday, March 18, 2015 | Sheet 31 of 56

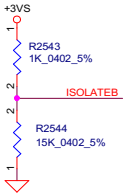
LAN-RTL8411B

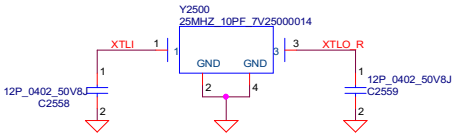


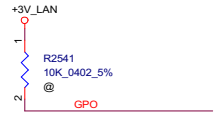
From EC
High active.
EN threshold voltage min:1.2V typ:1.6V max:2.0V
Current limit threshold 1.5~2.8A
+3V_LAN Rising time must >0.5ms and <100ms



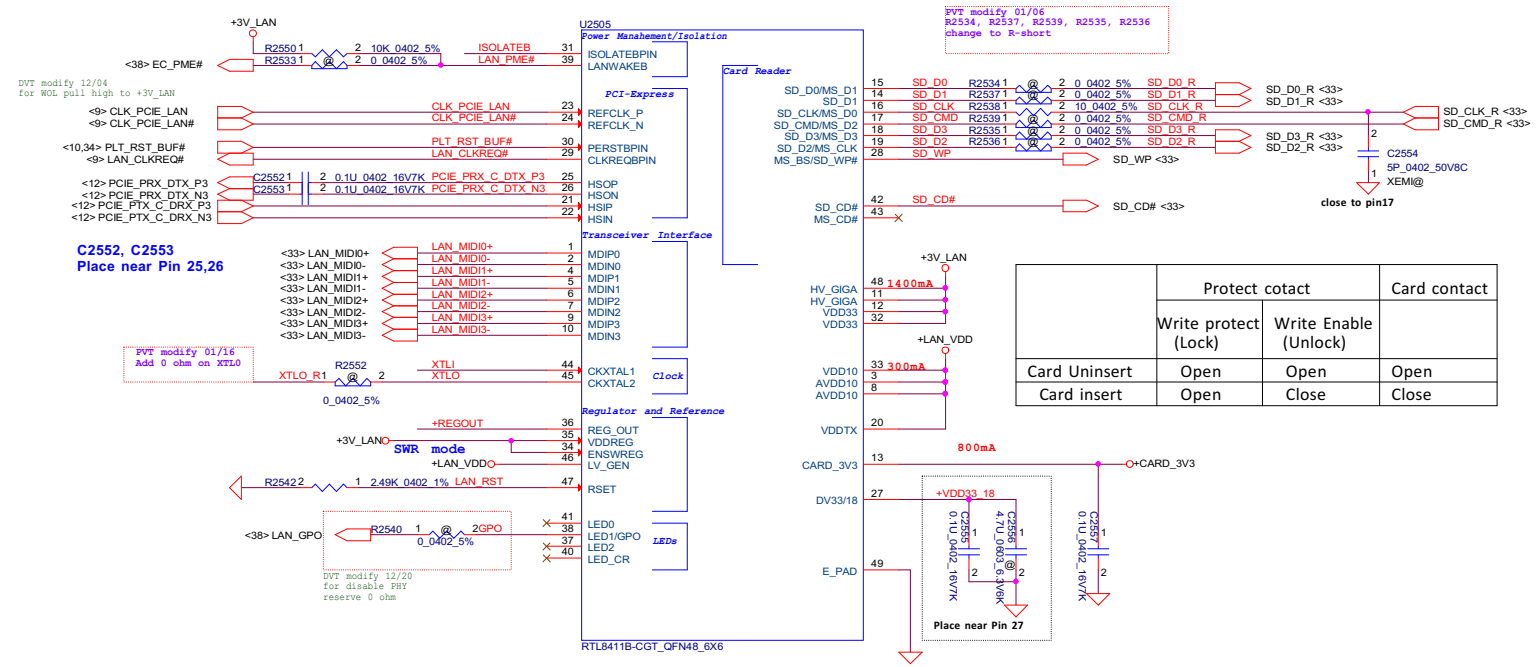








reserve EC_PME# pull high 100K to +3VALW_EC



	Protect cotact		Card contact
	Write protect (Lock)	Write Enable (Unlock)	
Card Uninsert	Open	Open	Open
Card insert	Open	Close	Close

Security Classification	Compal Secret Data		
Issued Date	2014/09/16	Deciphered Date	2014/05/24

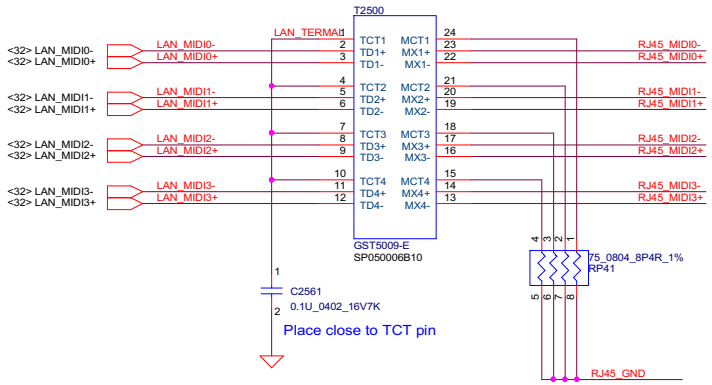
Compal Electronics, Inc.

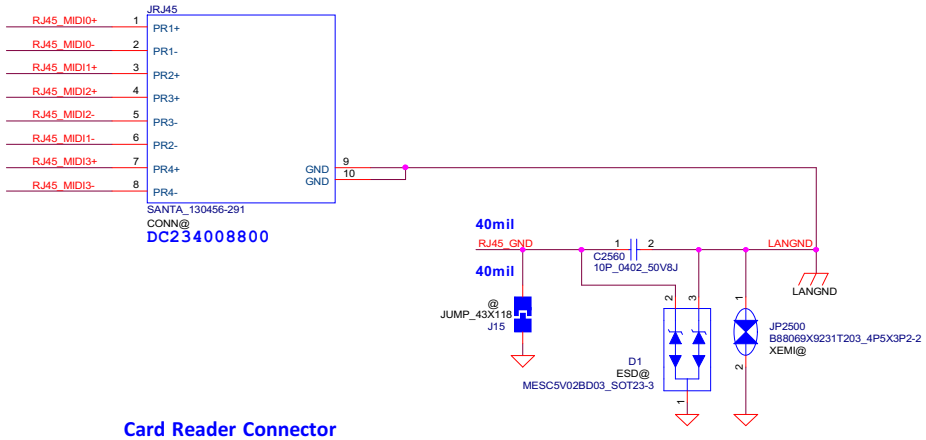
Title: LAN RTL8411-CG

Size: Custom | DocumentNumber: A4WAB M/B LA-C341P | Rev: 0.2

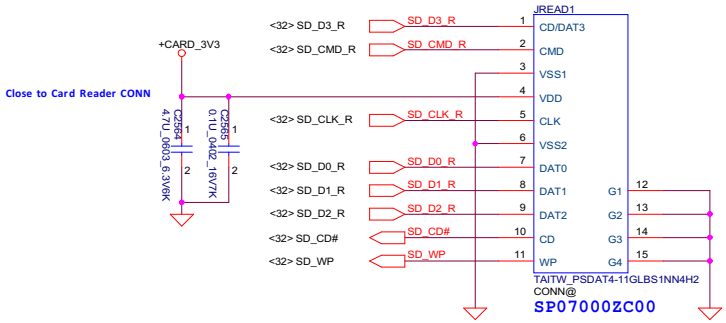
Date: Wednesday, March 18, 2015 | Sheet 32 of 56

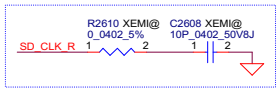
RJ45 / Card Reader conn.





Card Reader Connector



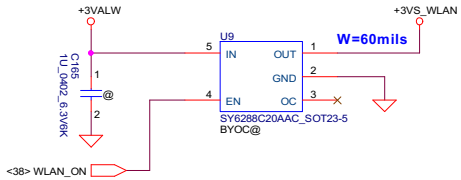


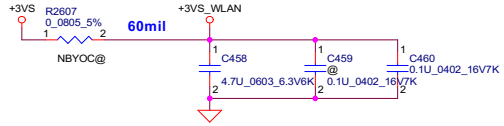
Close to JREAD1 for EMI

Security Classification	Compal Secret Data		
Issued Date	2014/09/16	Deciphered Date	2014/05/24

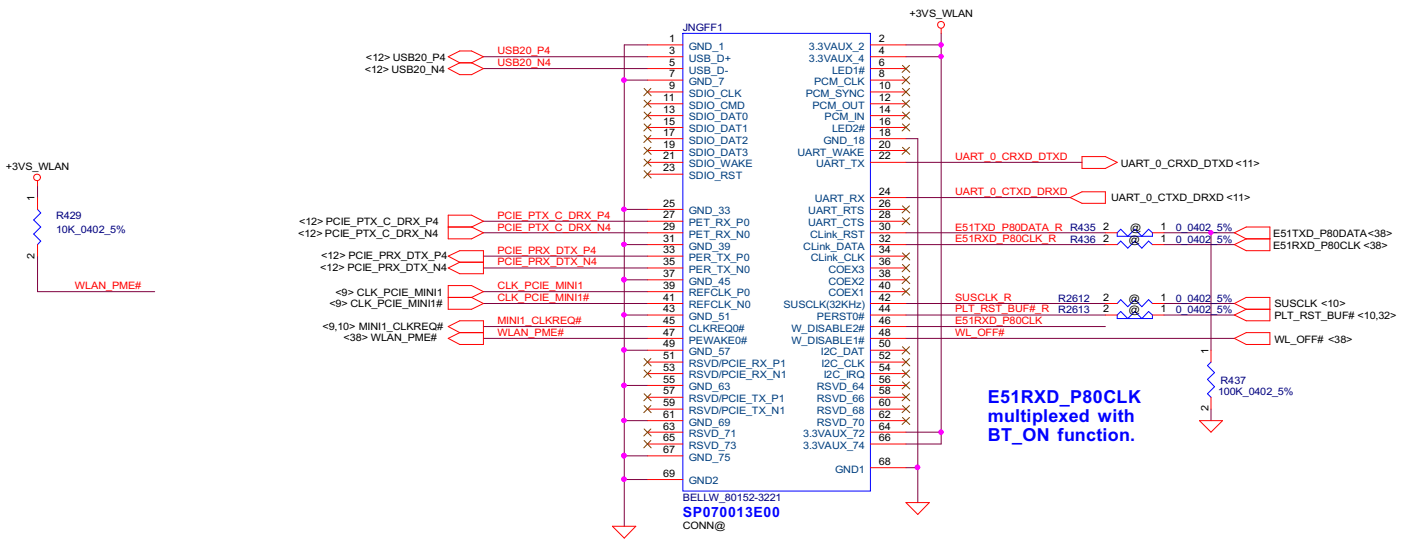
Compal Electronics, Inc.	
Title	LAN RJ45/CR SD Connector
Size: Custom	DocumentNumber: A4WAB M/B LA-C341P
Rev	0.2
Date: Wednesday, March 18, 2015	Sheet 33 of 56

Wireless LAN





NGFF Card E key module pin define



Security Classification	Compal Secret Data		
Issued Date	2014/09/16	Deciphered Date	2014/05/24

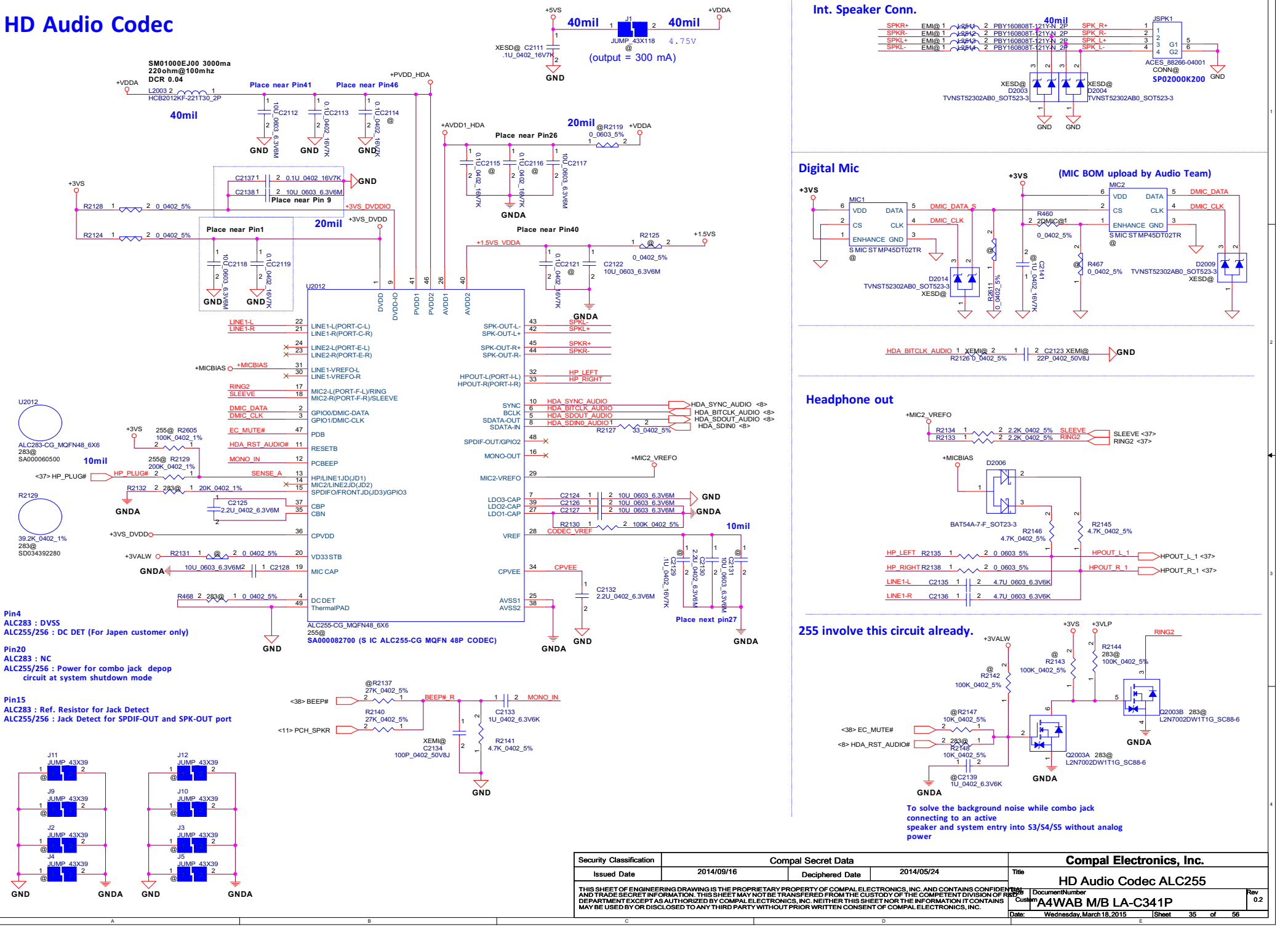
Compal Electronics, Inc.

Title: NGFF CARD (WLAN)

Size: Custom | DocumentNumber: A4WAB M/B LA-C341P | Rev: 0.2

Date: Wednesday, March 18, 2015 | Sheet 34 of 56

HD Audio Codec



Int. Speaker Conn.

Digital Mic

(MIC BOM upload by Audio Team)

Headphone out

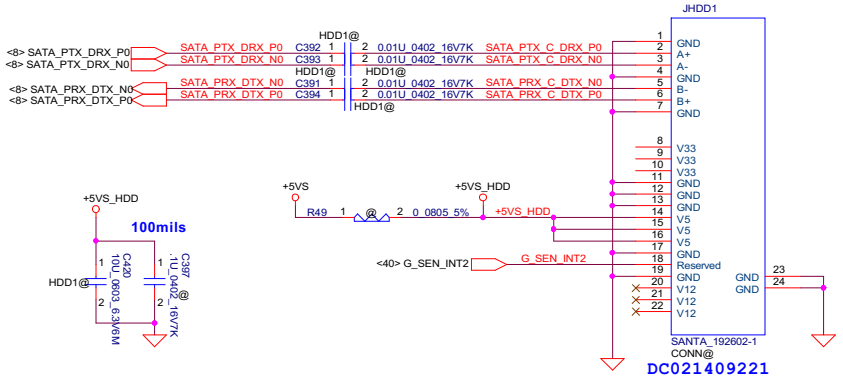
255 involve this circuit already.

To solve the background noise while combo jack connecting to an active speaker and system entry into S3/S4/S5 without analog power

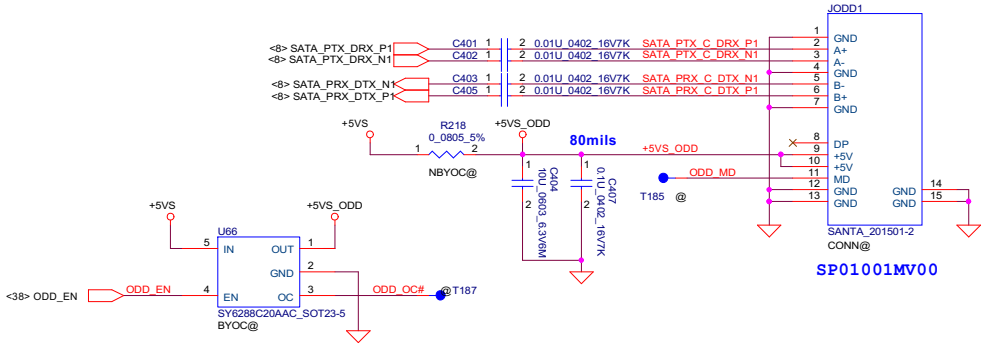
Security Classification	Compal Secret Data		
Issued Date	2014/09/16	Deciphered Date	2014/05/24

Compal Electronics, Inc.	
Title	HD Audio Codec ALC255
Size: Custom	Document Number: A4WAB M/B LA-C341P
Rev	0.2
Date: Wednesday, March 18, 2015	Sheet 35 of 56

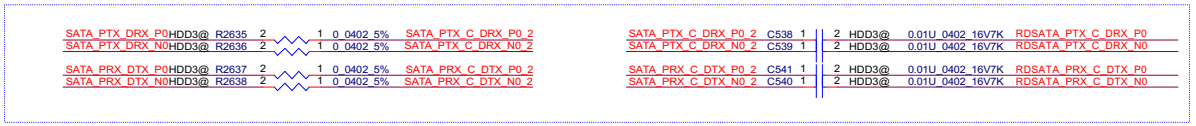
SATA HDD1 Conn.



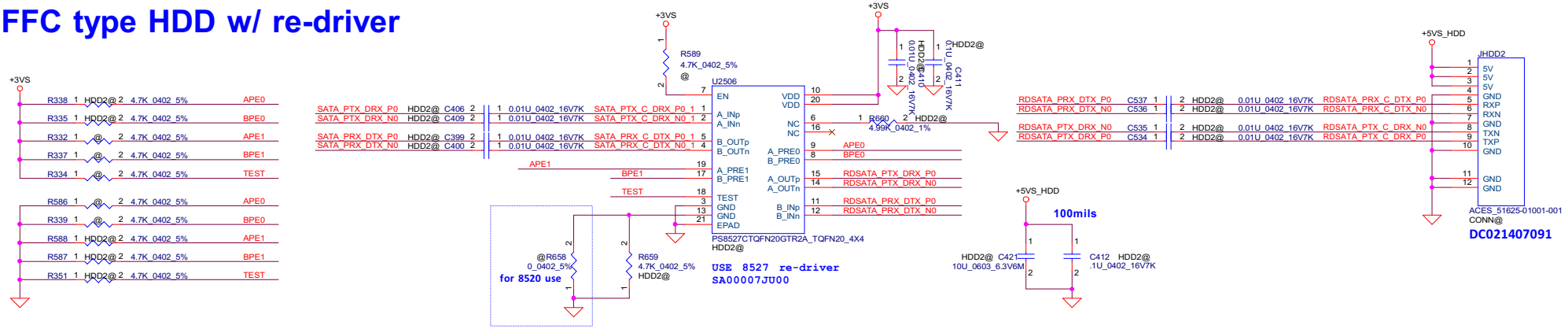
SATA ODD Conn.



FFC type HDD w/o re-driver



FFC type HDD w/ re-driver



SATA HDD2 Conn.

Security Classification	Compal Secret Data		
Issued Date	2014/09/16	Deciphered Date	2014/05/24

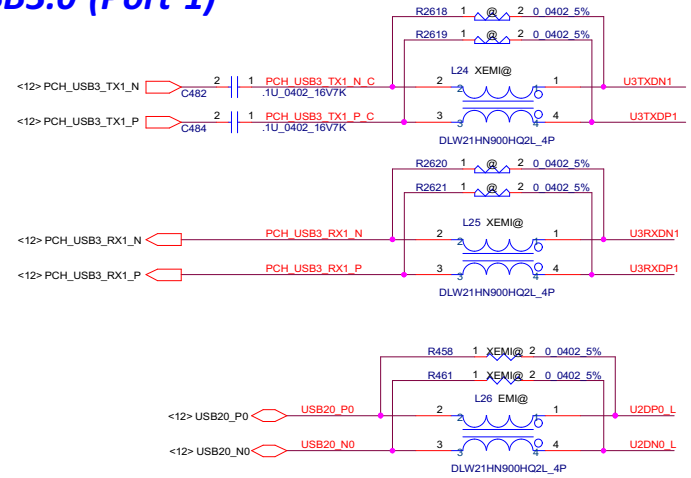
Compal Electronics, Inc.

Title: HDD/ODD/ HDD Re-Driver

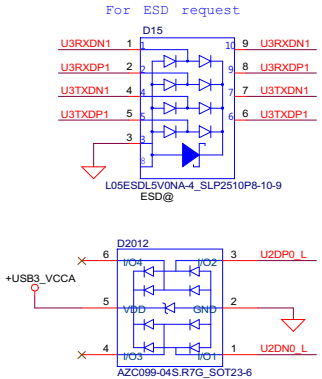
Size: Custom | DocumentNumber: A4WAB M/B LA-C341P | Rev: 0.2

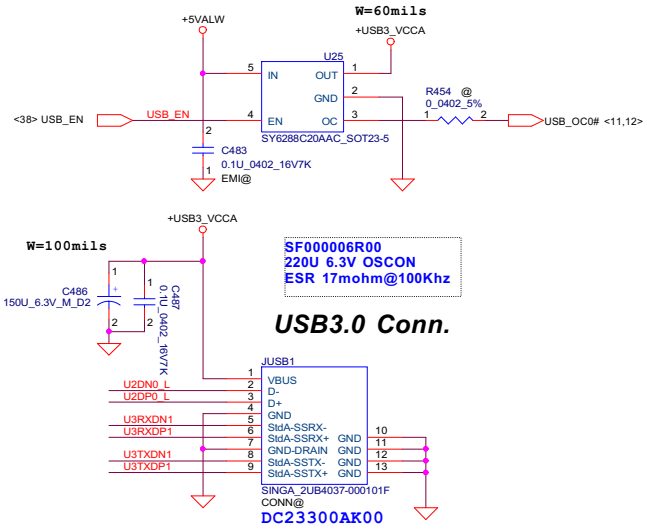
Date: Wednesday, March 18, 2015 | Sheet 36 of 56

USB3.0 (Port 1)

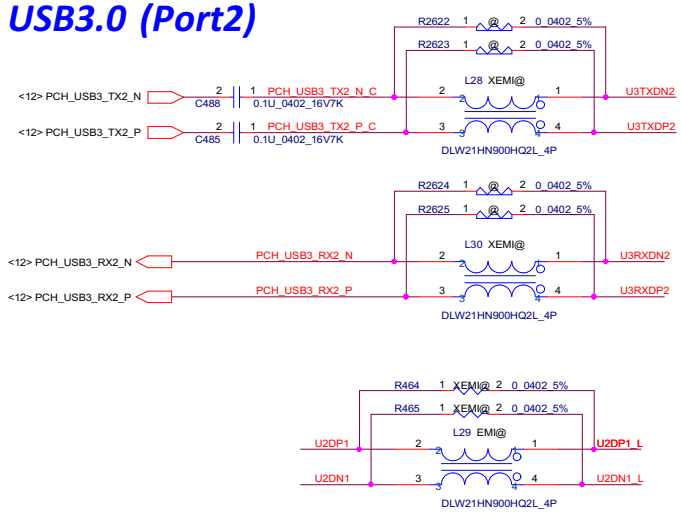


For ESD request

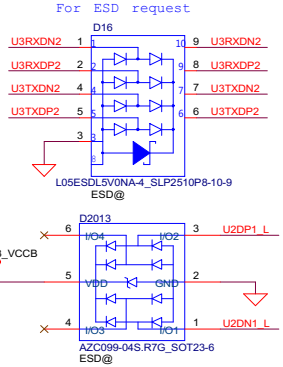


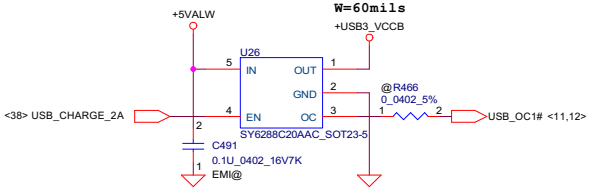


USB3.0 (Port2)



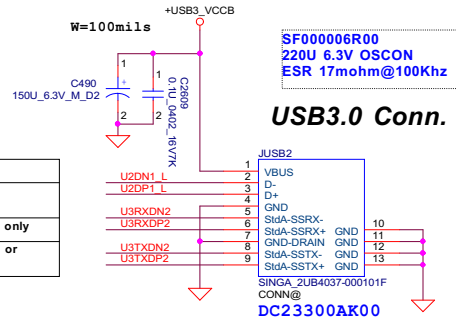
For ESD request

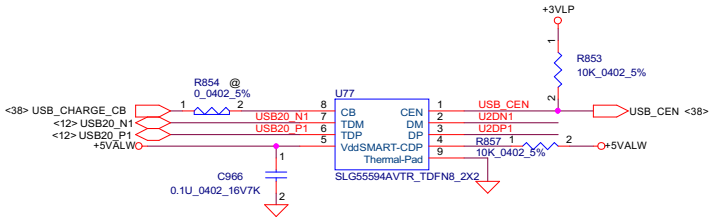




USB Host Charger

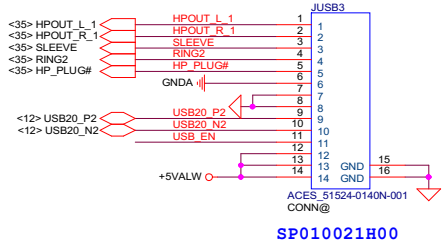
CB	SELCDP	
0	X	DCP(Dedicated Charging Port) autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP(Standard Downstream Port) only
1	1	S0 charging with CDP(Charging Downstream Port) or SDP only





USB/B (USB 2.0 + AUDIO)

Need check Audio Pin Sequence



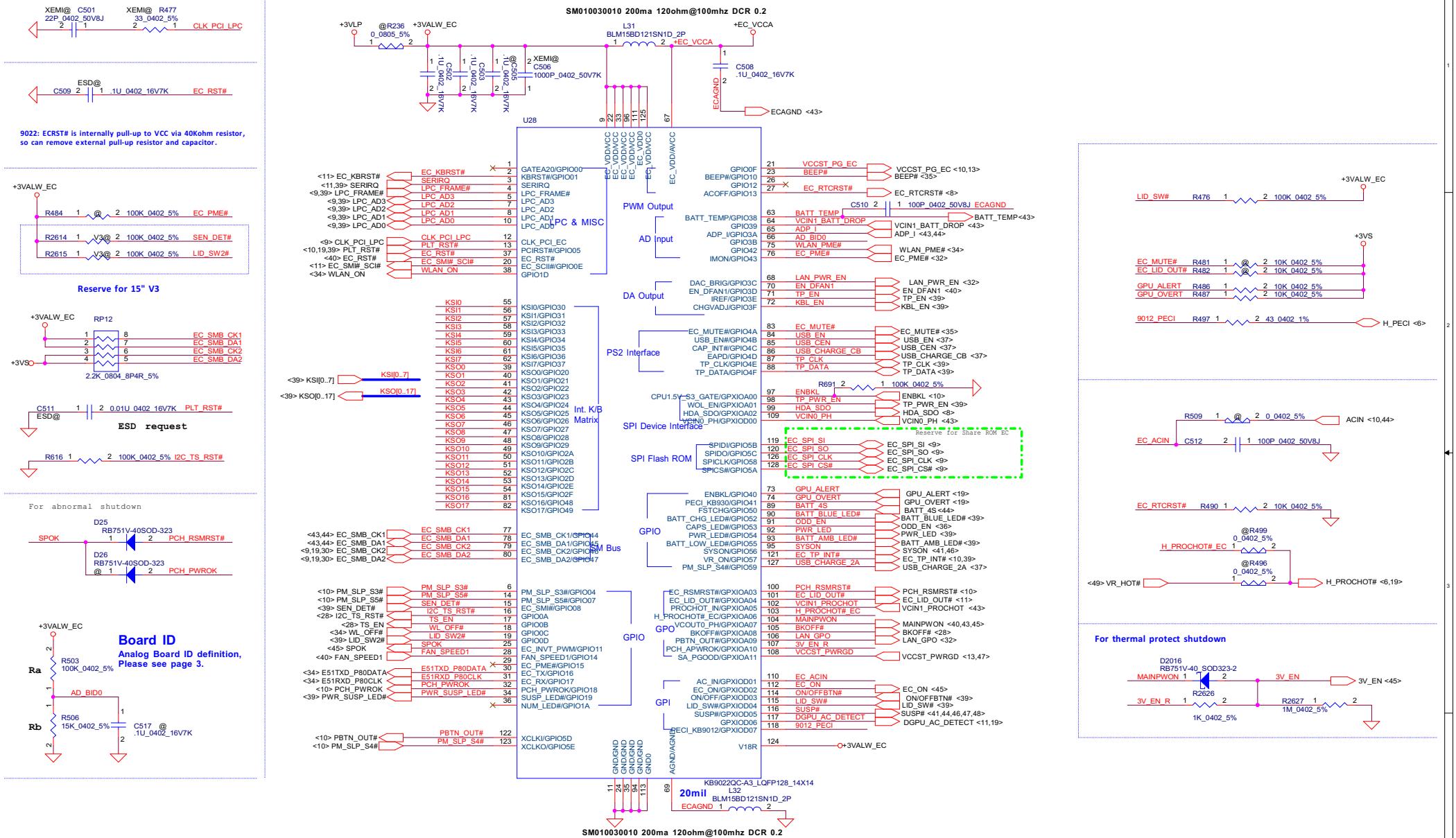
Security Classification	Compal Secret Data		
Issued Date	2014/09/16	Deciphered Date	2014/05/24

Compal Electronics, Inc.

Title: USB3.0 Conn/USB_B/PWR_B

Size: Custom | DocumentNumber: A4WAB M/B LA-C341P | Rev: 0.2

Date: Wednesday, March 18, 2015 | Sheet 37 of 56



Security Classification	Compal Secret Data		
Issued Date	2014/09/16	Deciphered Date	2014/05/24

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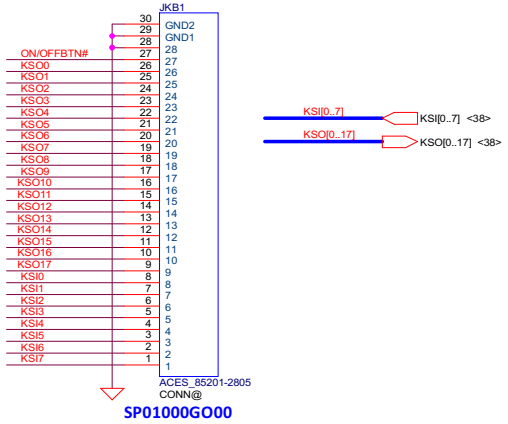
Compal Electronics, Inc.

Title: EC ENE-KB9022

Size: Custom | DocumentNumber: A4WAB M/B LA-C341P | Rev: 0.2

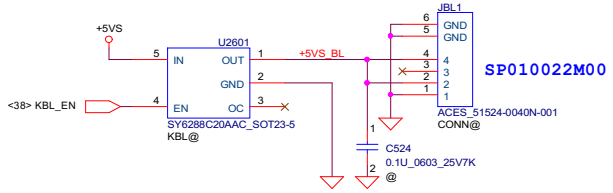
Date: Wednesday, March 18, 2015 | Sheet 38 of 56

KB Conn.



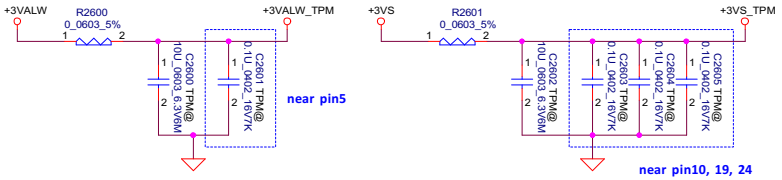
SP01000GO00

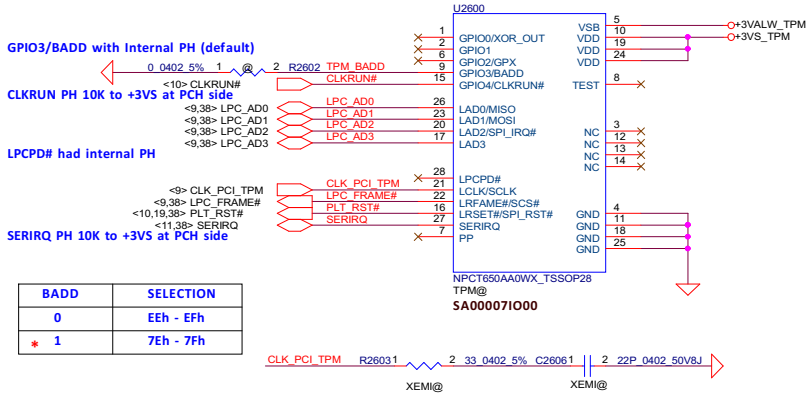
KB BackLight



SP010022M00

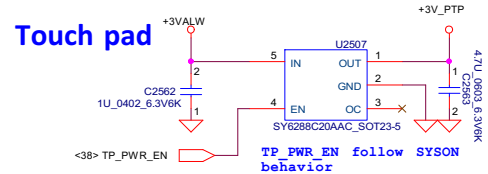
TPM

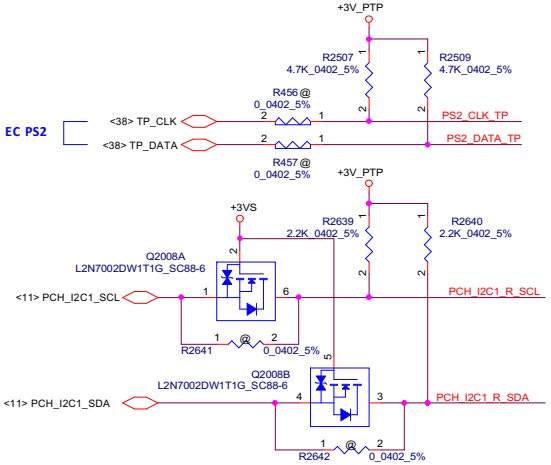


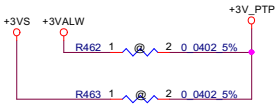


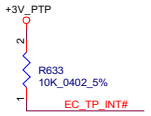
BADD	SELECTION
0	EEh - EFh
* 1	7Eh - 7Fh

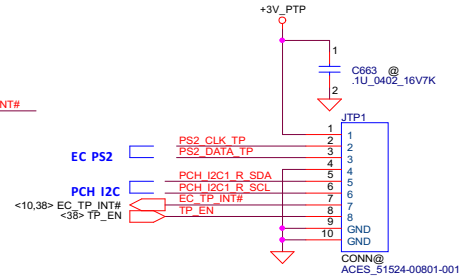
Touch pad





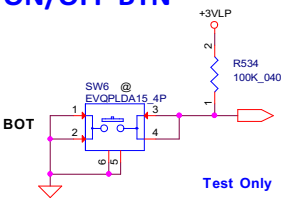






SP01001A910

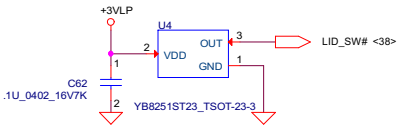
ON/OFF BTN



Test Only

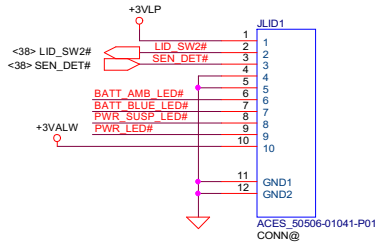
SN100000K00

Lid Switch



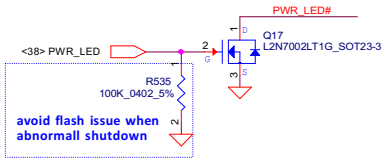
SA00008K800, S IC APX8132AI-TRG SOT-23 3P HALL SENSOR

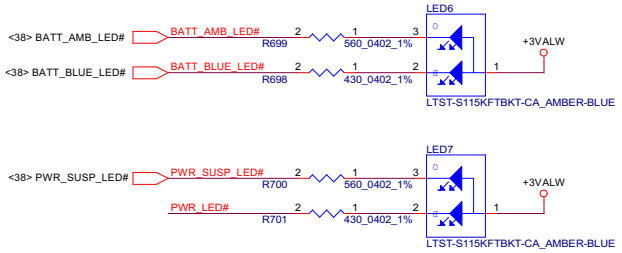
Lid Switch 2 (reserve for 15")



SP01001FR00

LED





Security Classification	Compal Secret Data		
Issued Date	2014/09/16	Deciphered Date	2014/05/24

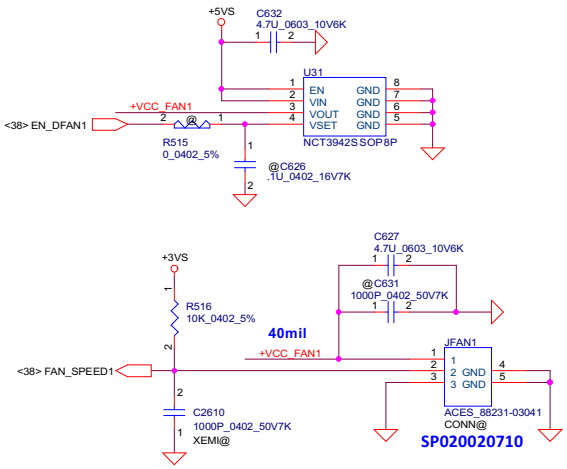
Compal Electronics, Inc.

Title: KB & TP & TPM Connector & LED

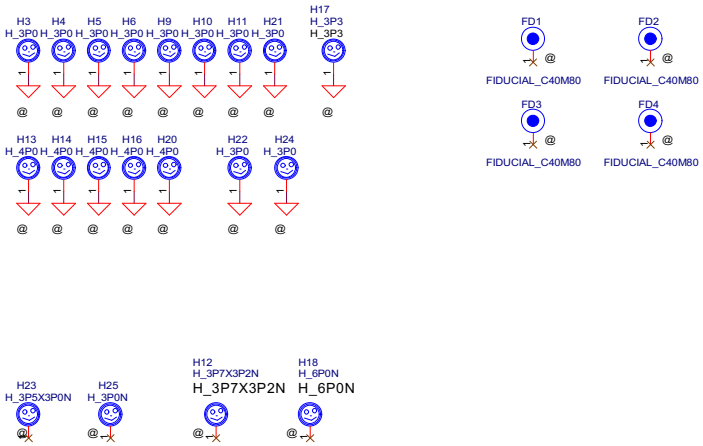
Size: Custom | Document Number: A4WAB M/B LA-C341P | Rev: 0.2

Date: Wednesday, March 18, 2015 | Sheet 39 of 56

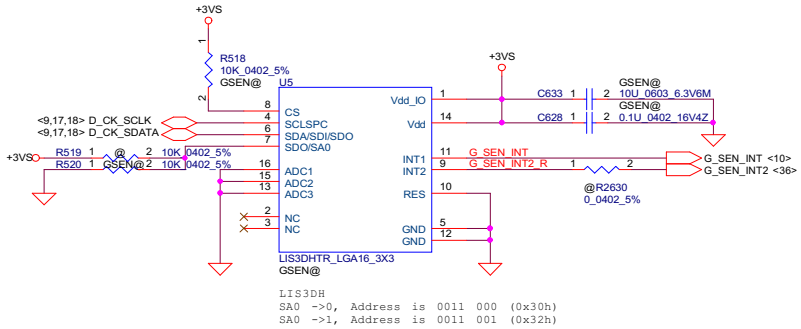
FAN1 Conn



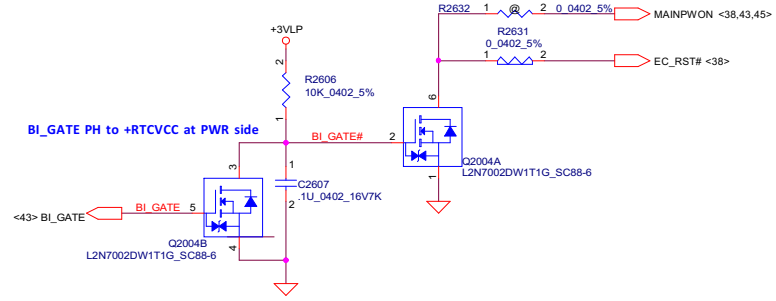
Screw Hole



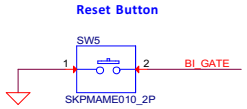
G-Sensor



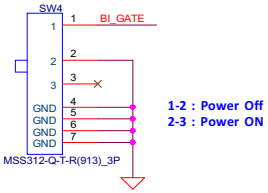
Reset Circuit



Reset Button



BI SW



Security Classification	Compal Secret Data		
Issued Date	2014/09/16	Deciphered Date	2014/05/24

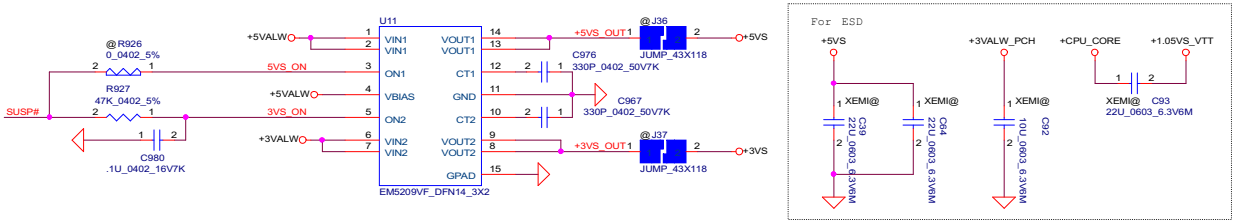
Compal Electronics, Inc.

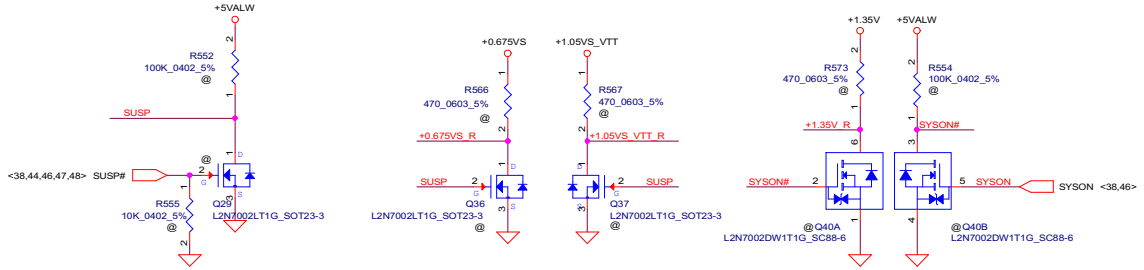
Title: FAN & Screw Hole & Reset

Size: Custom | DocumentNumber: A4WAB M/B LA-C341P | Rev: 0.2

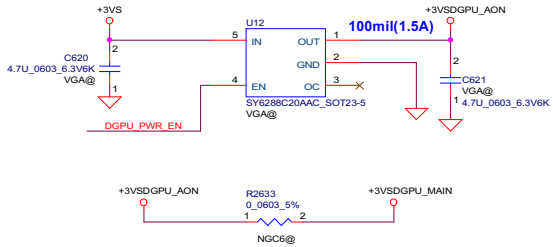
Date: Wednesday, March 18, 2015 | Sheet 40 of 56

DC & VGA Interface

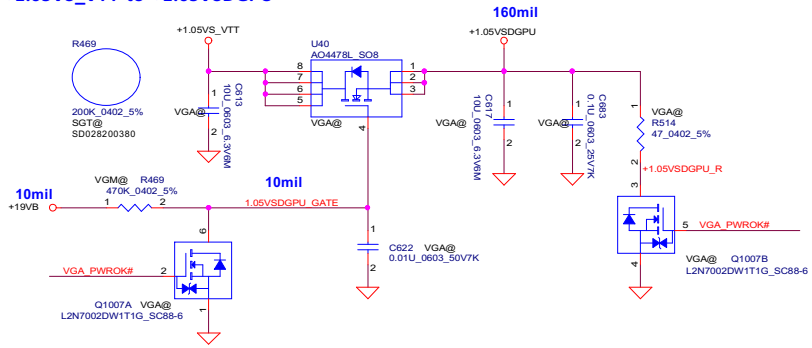




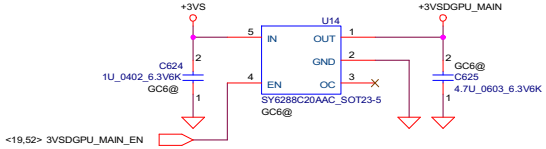
+3VS to +3VSDGPU_AON for GPU



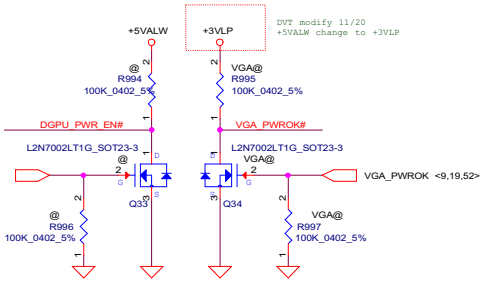
+1.05VS_VTT to +1.05VSDGPU

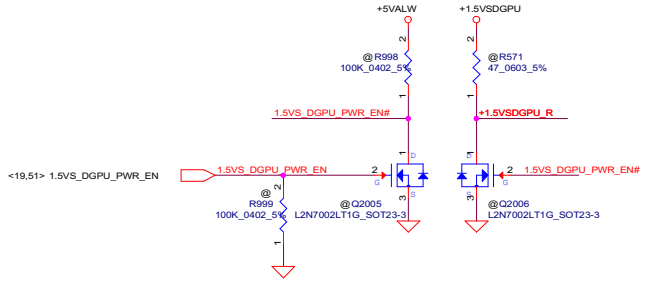


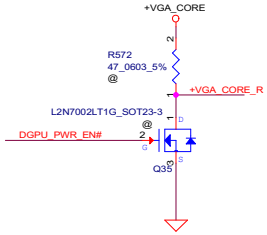
+3VS to +3VSDGPU_MAIN for GC6-2.0



3VSDGPU_MAIN_EN From GPU







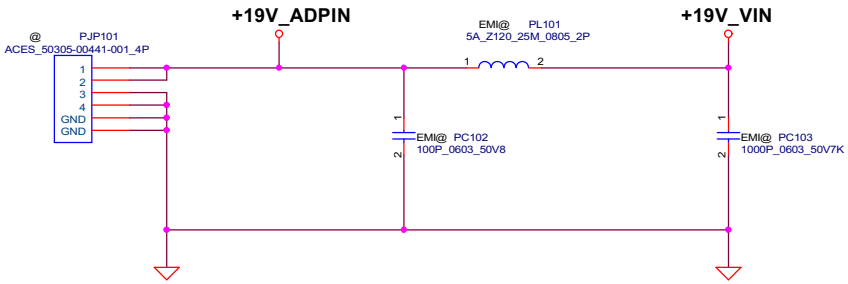
SecurityClassification	Compal Secret Data		
Issued Date	2014/09/16	Deciphered Date	2014/05/24

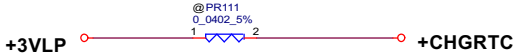
Compal Electronics, Inc.

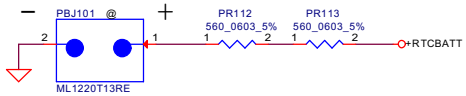
Title: DC Interface

Size: Custom | DocumentNumber: A4WAB M/B LA-C341P | Rev: 0.2

Date: Wednesday, March 18, 2015 | Sheet 41 of 56





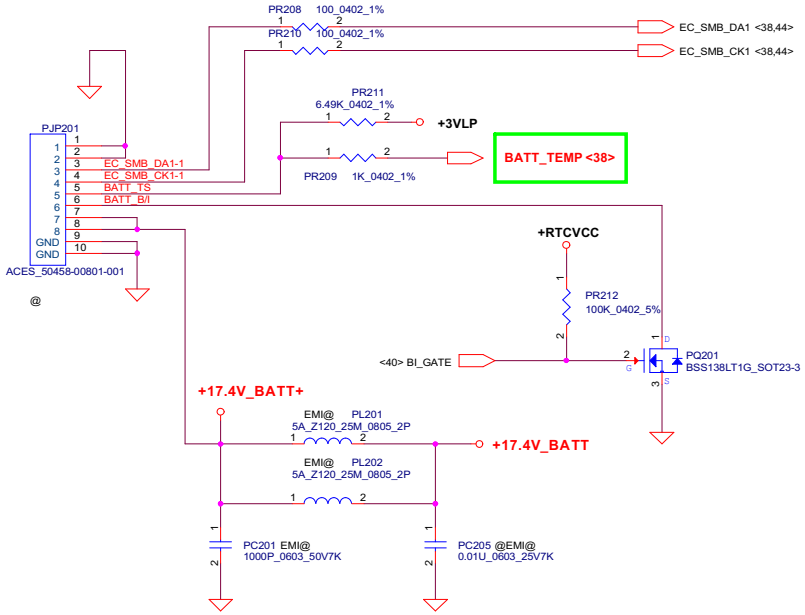


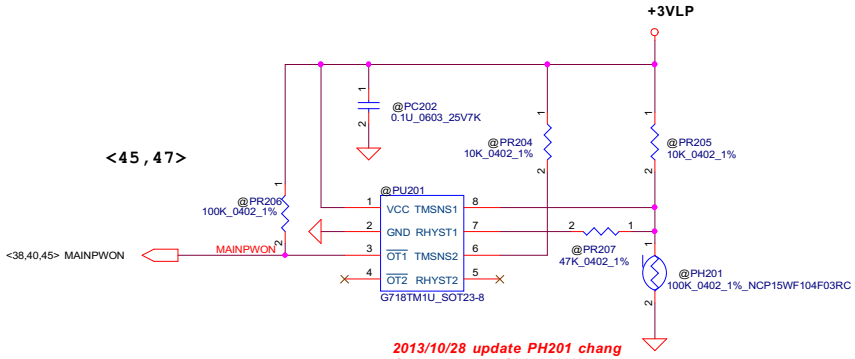
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/10/01	Deciphered Date	2014/05/24

Title: *DCIN*

Size: Custom | DocumentNumber | Rev: 1.0

Date: Wednesday, March 18, 2015 | Sheet 42 of 56





2013/10/28 update PH201 chang
Common part SL200002H00

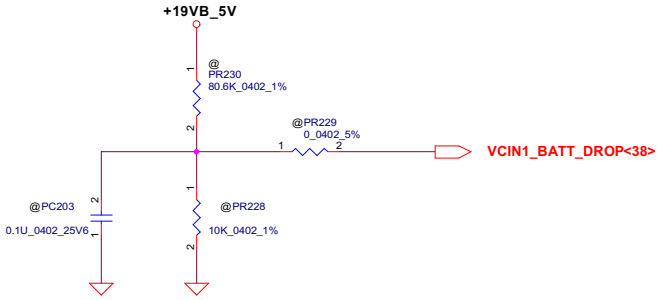
2014/09/30 update

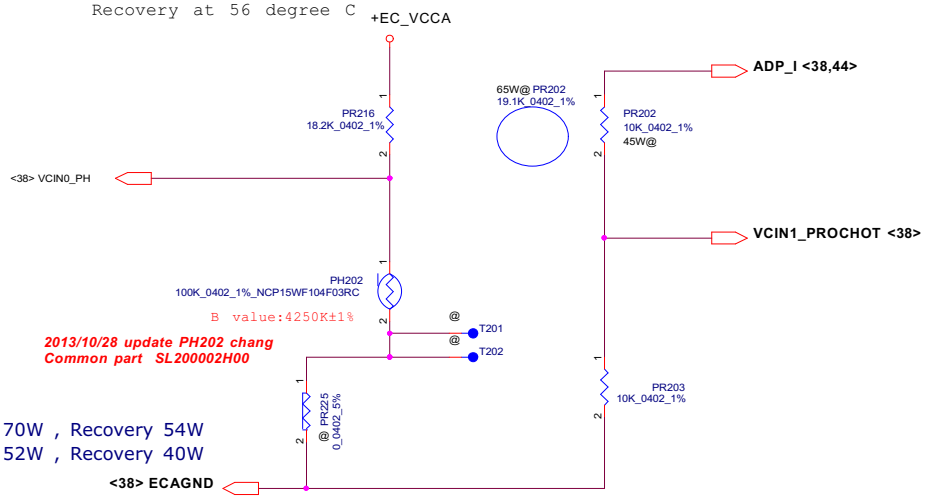
For KB9022 sense 20mΩ	Active	Recovery
45W PR202 10K ohm SD034100280	58.5W,0.61V	45W,0.47V
65W PR202 19.1K ohm SD034191280	84.5W,0.61V	65W,0.47V

PH202 under CPU botten side :
CPU thermal protection at 90 degree C (shutdown)
Recovery at 56 degree C

2013/10/02
Add for ENE9022 Battery Voltage drop detection.
Connect to ENE9022 pin64 AD1.

Battery is 3-cell design.
B+=9V





2013/10/28 update PH202 chang
Common part SL200002H00

For 65W adapter==>action 70W , Recovery 54W
For 40W adapter==>action 52W , Recovery 40W

Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2014/05/24

Compal Electronics, Inc.

Title: ***BATTERY CONN / OTP***

Size	DocumentNumber	Rev
Custom		1.0

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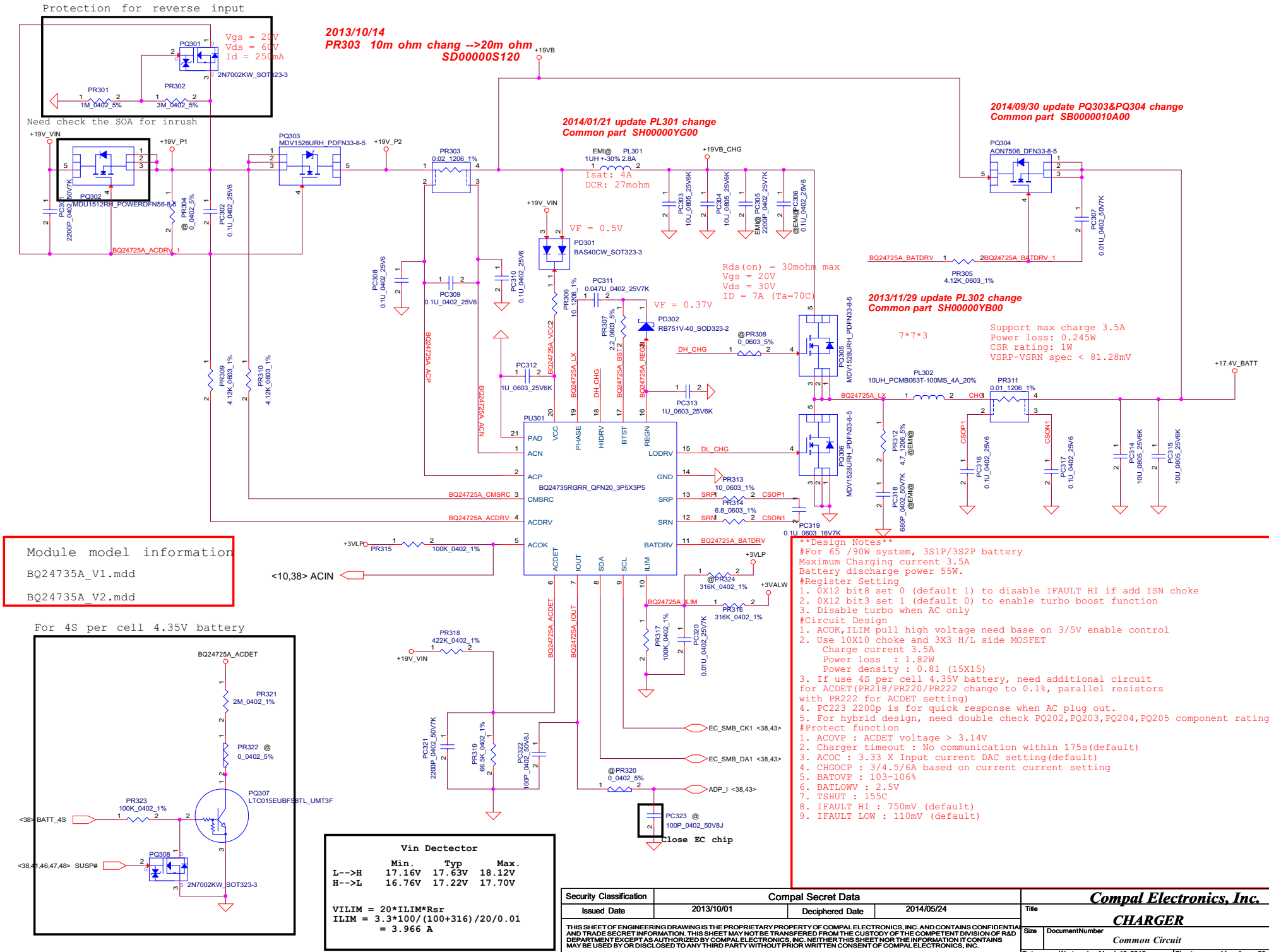
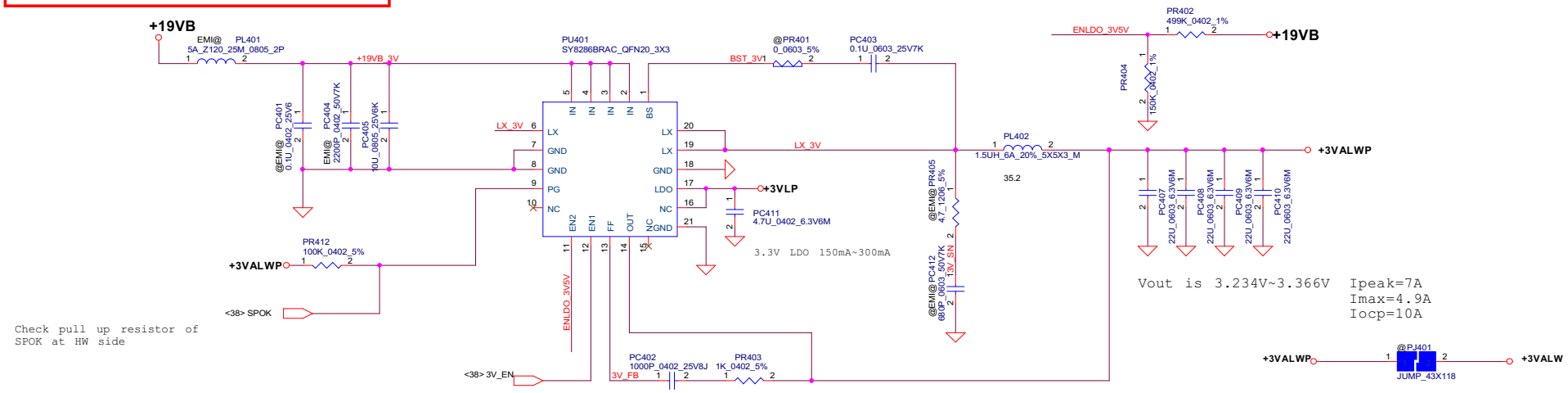

Protection for reverse input
Vgs = 20V
Vds = 60V
Id = 250mA
2N7002KW_SOT323-3
2013/10/14
PR303 10m ohm chang -->20m ohm
SD00000S120
Need check the SOA for inrush
2014/01/21 update PL301 change
Common part SH00000YG00
2014/09/30 update PQ303&PQ304 change
Common part SB0000010A00
Isat: 4A
DCR: 27mohm
VF = 0.5V
VF = 0.37V
Rds(on) = 30mohm max
Vgs = 20V
Vds = 30V
ID = 7A (Ta=70C)
2013/11/29 update PL302 change
Common part SH00000YB00
7*7*3
Support max charge 3.5A
Power loss: 0.245W
CSR rating: 1W
VSRP-VSRN spec < 81.28mV
BQ24735RGRR_QFN20_3P5X3P5
Module model information
BQ24735A_V1.mdd
BQ24735A_V2.mdd
For 4S per cell 4.35V battery
<10,38> ACIN
Vin Dectector
Min. Typ Max.
L-->H 17.16V 17.63V 18.12V
H-->L 16.76V 17.22V 17.70V
VILIM = 20*ILIM*Rsr
ILIM = 3.3*100/(100+316)/20/0.01
= 3.966 A
Design Notes
#For 65 /90W system, 3S1P/3S2P battery
Maximum Charging current 3.5A
Battery discharge power 55W.
#Register Setting
1. 0X12 bit8 set 0 (default 1) to disable IFAULT HI if add ISN choke
2. 0X12 bit3 set 1 (default 0) to enable turbo boost function
3. Disable turbo when AC only
#Circuit Design
1. ACOK,ILIM pull high voltage need base on 3/5V enable control
2. Use 10X10 choke and 3X3 H/L side MOSFET
Charge current 3.5A
Power loss : 1.82W
Power density : 0.81 (15X15)
3. If use 4S per cell 4.35V battery, need additional circuit for ACDET(PR218/PR220/PR222 change to 0.1%, parallel resistors with PR222 for ACDET setting)
4. PC223 2200p is for quick response when AC plug out.
5. For hybrid design, need double check PQ202,PQ203,PQ204,PQ205 component rating
#Protect function
1. ACOVP : ACDET voltage > 3.14V
2. Charger timeout : No communication within 175s(default)
3. ACOC : 3.33 X Input current DAC setting(default)
4. CHGOCP : 3/4.5/6A based on current current setting
5. BATOVP : 103-106%
6. BATLOWV : 2.5V
7. TSHUT : 155C
8. IFAULT HI : 750mV (default)
9. IFAULT LOW : 110mV (default)
Close EC chip
Security Classification
Compal Secret Data
Issued Date
2013/10/01
Deciphered Date
2014/05/24
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.
Compal Electronics, Inc.
Title
CHARGER
Size
DocumentNumber
Common Circuit
Rev
1.0
Date: Wednesday, March 18, 2015
Sheet 44 of 56

Module model information

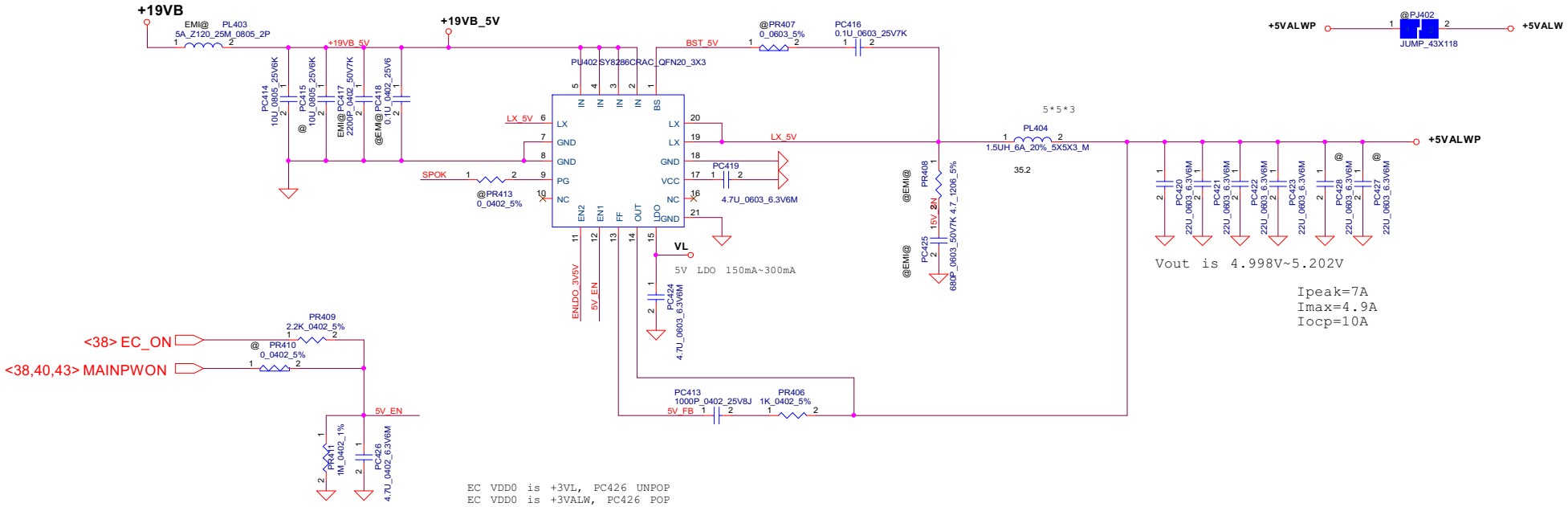
SY8208B_V2.mdd

SY8208C_V2.mdd

EN1 and EN2 dont't floating



Check pull up resistor of SPOK at HW side



EC VDD0 is +3VL, PC426 UNPOP
EC VDD0 is +3VALW, PC426 POP

Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2014/05/24

Compal Electronics, Inc.

Title: +3VALW/+5VALW

Size: Custom | Document Number | Rev: 1.0

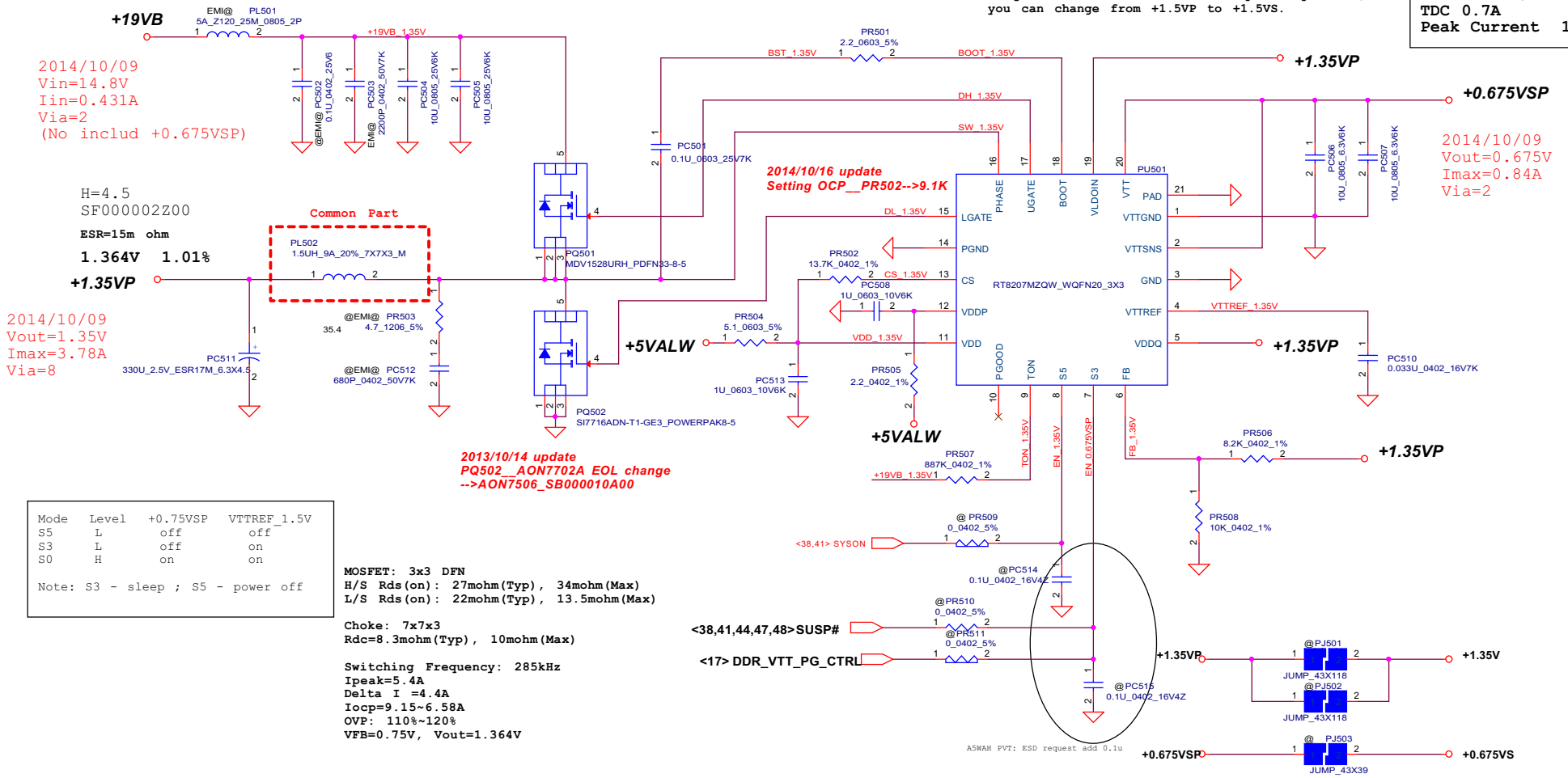
Date: Wednesday, March 18, 2015 | Sheet 45 of 56

Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer

Pin19 need pull separate from +1.5VP.
If you have +1.5V and +0.75V sequence question,
you can change from +1.5VP to +1.5VS.

0.75Volt +/- 5%
TDC 0.7A
Peak Current 1A



Mode	Level	+0.75VSP	VTTREF_1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

MOSFET: 3x3 DFN
H/S Rds(on): 27mohm(Typ), 34mohm(Max)
L/S Rds(on): 22mohm(Typ), 13.5mohm(Max)

Choke: 7x7x3
Rdc=8.3mohm(Typ), 10mohm(Max)

Switching Frequency: 285kHz
Ipeak=5.4A
Delta I =4.4A
Iocp=9.15~6.58A
OVP: 110%~120%
VFB=0.75V, Vout=1.364V

Security Classification	Compal Secret Data		
Issued Date	2013/10/01	Deciphered Date	2014/05/24

Compal Electronics, Inc.

Title: +1.35VP/+0.675VSP

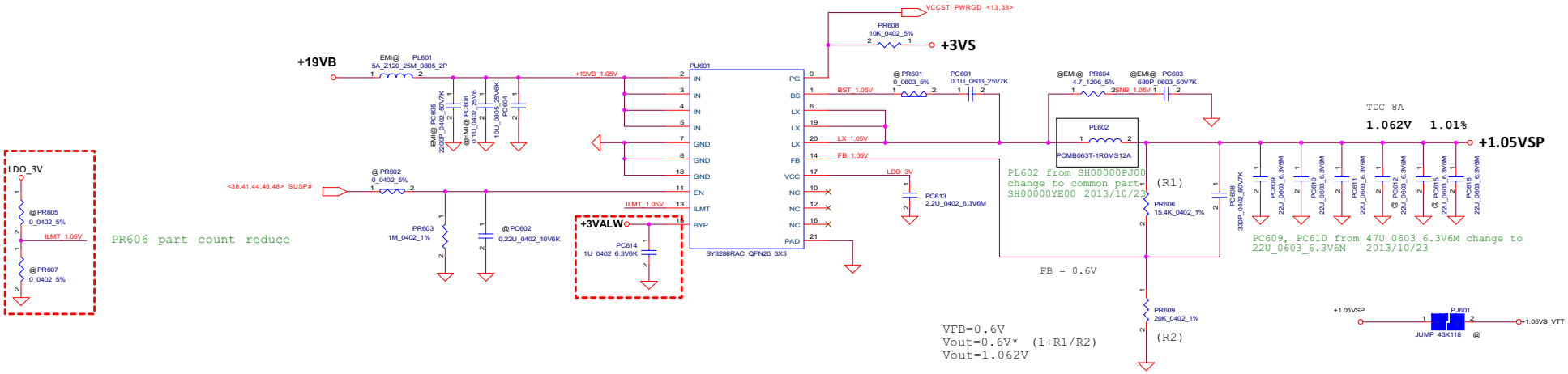
Size: Custom | Document Number | Rev: 1.0

Date: Wednesday, March 18, 2015 | Sheet 46 of 56

Module model information

SY8208D_V1.mdd

EN pin don't floating
If have pull down resistor at HW side, pls delete PR2



PR606 part count reduce

PL602 from SH00000PJ00 change to common part SH00000YE00 2013/10/23

PC609, PC610 from 47U_0603_6.3V6M change to 22U_0603_6.3V6M 2013/10/23

FB = 0.6V

VFB=0.6V
Vout=0.6V* (1+R1/R2)
Vout=1.062V

The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

Module model information

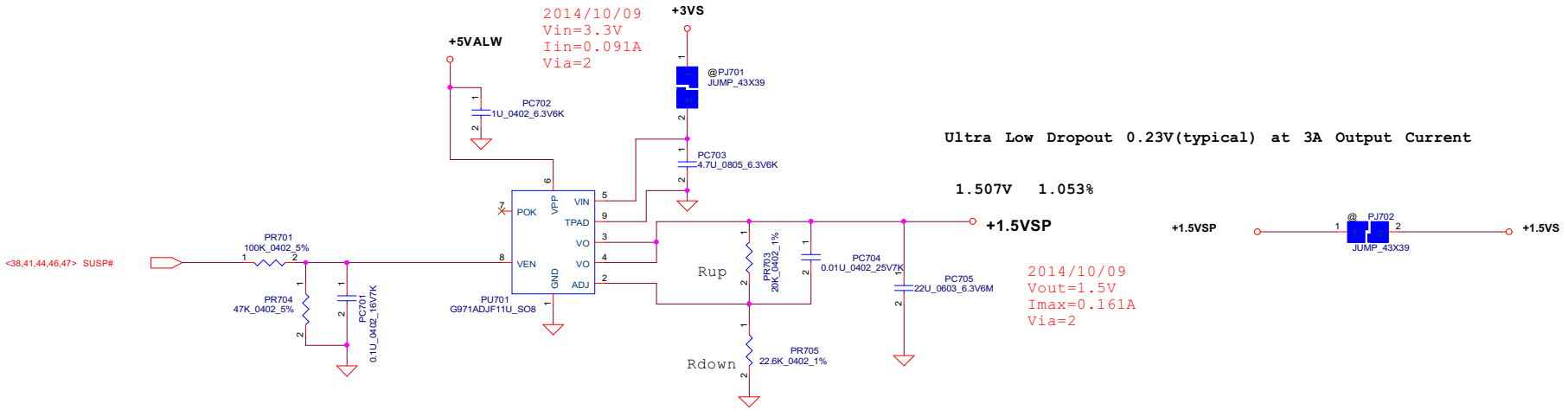
SY8208D_V1.mdd

Compal Electronics, Inc.

Title: +1.05VSP

Size: C | DocumentNumber | Rev: 1.0

Date: Wednesday, March 18, 2015 | Sheet 47 of 56



Vout=0.8V* (1+Rup/Rdown)

Ultra Low Dropout 0.23V(typical) at 3A Output Current

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/10/01	Deciphered Date	2014/05/24
Title	*+1.5VSP*		
Size: Custom	DocumentNumber		Rev: 1.0
Date: Wednesday, March 18, 2015	Sheet 48 of 56		

Module model information:
ISL95813 (for 15W & 28W CPU)

Location	15W	28W	Note
	TDC 14A MAX 32A OCP 38.4A Loadline=-2.0mv/A	TDC 19A MAX 40A OCP 48A Loadline=-2.0mv/A	
PR820	392 Ohm	499Ohm	OCP
PR816	1.27kOhm	1.58kOhm	Droop
PC816	0.033uF	0.022uF	RC Match
PR804	90.9kOhm	113kOhm	PROG1
PR807	93.1kOhm	95.3kOhm	IMON
PC811	0.1uF (0402)	0.1uF (0402)	RC Filter

Base on BDW PDDG Rev_0_73

H-side MOS: MDV1525URH
Rds(on):
<10.1mohm@Vgs=10V
<14.0mohm@Vgs=4.5V
Id :24A@Vgs=10V

L-side MOS: MDU1511RH
Rds(on):
<2.4mohm@Vgs=10V
<3.3mohm@Vgs=4.5V
Id :100A@Vgs=10V

-->20130828
Choke: 0.15UH (Size:7*7*4)
SH00000U300
Rdc=0.66mohm +-7%
Heat Rating Current=36A
Saturation Current=45A

+1.05VS_VTT
Follow intel guideline
PR802 130_0402_1%
PR803 54.9_0402_1%
PC802 1U_0402_6.3V6K

<13> VR_SVID_DATA
Note:
VR_SVID_ALRT# Pull high on HW side
<13> VR_ALERT#
<13> VR_SVID_CLK
<13> VR_ON
PR805 1.91K_0402_1%
<13> VGATE
PC808 1000P_0402_50V7K
PR807 93.1K_0402_1%
<38> VR_HOT#
PH802 470K_0402_5%_TSM0B474J4702RE
PR810 5.62K_0402_1%
PR811 27.4K_0402_1%
PC809 47P_0402_50V8J

Over temperature protection:
OTP Setting: 100C active
Pin5 (NTC) voltage <0.88V, Protect
Pin5 (NTC) voltage >0.92v, recovery

2013/10/28 update PH802 chang
Common part SL200002E00

PU801
ISL95813HRZ-T_QFN20_3X4
PAD, SCLK, ALERT#, SDA, PRGM1
VR_ON, PGOOD, IMON, VR_HOT#, NTC, COMP, FB, RTN, ISUMN, ISUMP
LGATE, PHASE, UGATE, BOOT, VCC, PRGM2

15W@ PR804 90.9K_0402_1%
28W@ PR804 113K_0402_1%
Note:
PR804=113K
=>Icc(max)=40A
fsw=700KHz

@PR806 0_0603_5%
PR801 2.2_0603_5%
PC801 0.22U_0603_16V7K
PC811 0.1U_0402_25V6
+5VS

PR812 124K_0402_1%
Note:
PR812=124K
=>Slew rate=53mV/us
Vboot = 1.7V

PR813 3.65K_0402_1%
PC813 6800P_0402_25V7K
33P_0402_50V8J PC812
PR814 2K_0402_1%
@PC814 330P_0402_50V7K
@PC815 390P_0402_50V7K
PR815 10_0402_1%
PR816 1.27K_0402_1%
Droop
15W@
28W@ PR816 1.58K_0402_1%
PR817 20M_0402_5%
RC Match
PC816 0.033U_0402_16V7K
15W@
28W@ PC816 0.022U_0402_16V7K
PC817 0.1U_0402_16V4Z
PR819 11K_0402_1%
PR818 2.61K_0402_1%
PH801 10KB_0402_5%_ERTJ0ER103J

2013/10/28 update PH801 chang
Common part SL200002G00

<13> VCC_SENSE
<13> VSS_SENSE
@PC818 330P_0402_50V7K
PC820 0.01U_0402_50V7K
@PC819 0.082U_0402_16V7K
28W@ PR820 499_0402_1%
OCP Setting
15W: 38A
28W: 48A
PR820 15W@ 392_0402_1%
@PC821 4700P_0402_25V7K
@PR821 1.5K_0402_1%

Local sense put on HW site

PQ801 PQ803 PQ802 MDU1516URH_POWERDFN56-8-5
MDU1511RH_POWERDFN56-8-5
28W@ PQ802

+19VB_CPU
PL803 EMI@ 5A_Z120_25M_0805_2P
PL801 EMI@ 5A_Z120_25M_0805_2P
+19VB
PC803 10U_0805_25V6K
PC804 10U_0805_25V6K
@EMI@ PC805 0.01U_0402_50V7K
EMI@ PC806 2200P_0402_50V7K
PC807 68U_25V_M_R0.36
Height 8 mm
100u_SF000000I80
Height 6 mm
68u_SF000000W00
2014/10/09
Vin=14.8V
Iin=3.193A
Via=8

2014/01/21 update PL802 change
Common part SH000011H00
PL802 0.22UH20%FDUE0640J-H25A
+CPU_CORE
@EMI@ PR808 4.7_1206_5%
@EMI@ PC810 680P_0603_50V7K
PR809 3.65K_0603_1%

TDC 19A
MAX 40A
OCP 48A
Loadline=-2.0mv/A

2014/10/09
Vout=1.35V
Imax=28A
Via=56

Title	CPU_CORE/GFX_CORE		
Size	DocumentNumber	A4WAB M/B LA-C341P	Rev 1.0
Date: Wednesday, March 18, 2015	Sheet 49 of 56		

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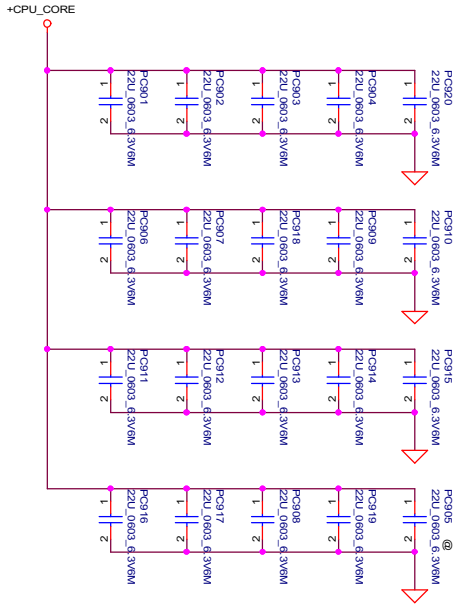
PWR Rule
需確認最新SPEC.
Modify 8/6.



30 X 22uF 0805
2012/10/23
check the output cap Qty!!!
2012/10/24
23 pcs 22uF and reserve 7 pcs
2013/01/14
22uF*17 unpop:22uF*3

20130828
15W: 22uF*14
28W: 22uF*16

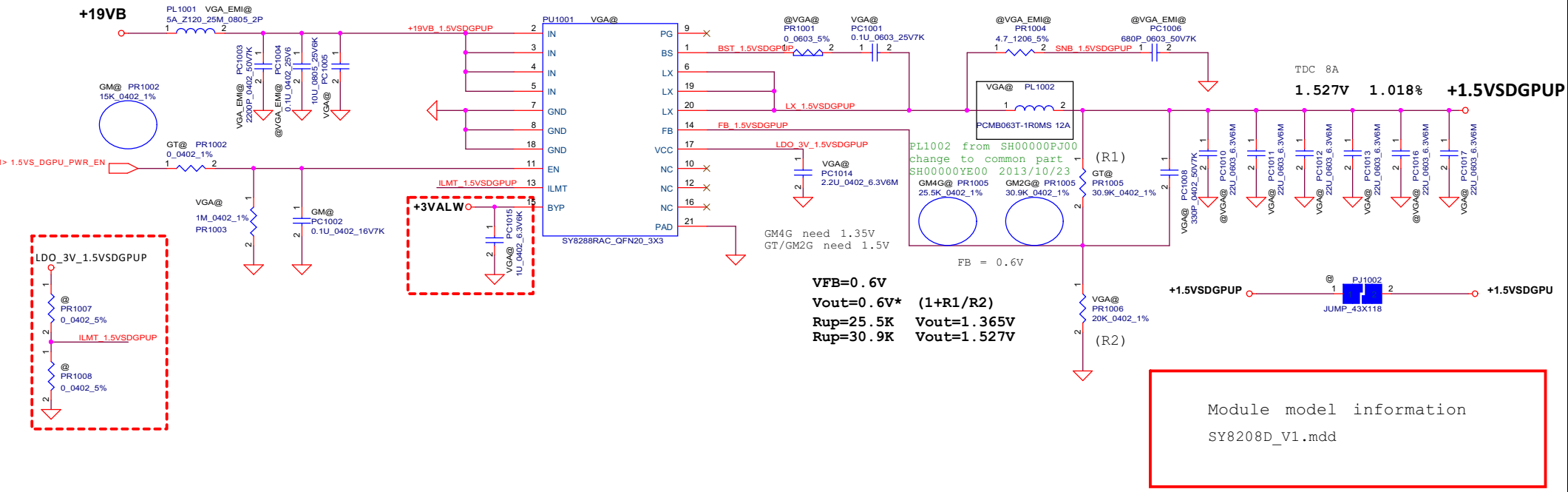
Compal Electronics, Inc.

Title: *CPU CORE CAP*

Size	DocumentNumber	Rev
Custom		1.0

Date: Wednesday, March 18, 2015 | Sheet 50 of 56

EN pin don't floating
If have pull down resistor at HW side, pls delete PR2



Module model information
SY8208D_V1.mdd

The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/10/01	Deciphered Date	Title: 1.5VSDGPUP
			Size: Document Number: Rev: 1.0
			Date: Wednesday, March 18, 2015 Sheet 51 of 56

Module model information:
RT8813A_V1A for IC module
RT8813A_V1B for SW module

PSI :
1 phase with DEM 0V to 0.8V
1 phase with CCM 1.2V to 1.8V
2 phase with CCM 2.4V to 5.5V

EN High Threshold = 1.6V

Vboot=Vvref*Rref2/(Rref1+Rref2+Rboot)
Rt=Rrefadj // (Rboot+Rref2)
Vmin= Vvref*[Rref2/(Rref2+Rboot)]*[Rt/(Rref1+Rt)]
Vmax=Vvref*Rref2/[(Rref1//Rrefadj)+Rboot+Rref2]
Vout=Vmin+N*Vstep
Vstep=(Vmax-Vmin)/Nmax

PWM-VID Spec and component Values

PWM-VID Spec		Config B	Config C	Config D
Vmin		0.6V	0.65V	0.9V
Vmax		1.2V	1.15V	1.15V
Vboot		0.9V	0.9V	1.028V
Voltage step		6.25mV	25mV	12.5mV
N of Voltage level		96	20	20
Rrefadj	PR1209	20K	39K	27K
Rref1	PR1208	20K	30K	7.5K
Rboot	PR1211	2K	3K	0
Rref2=PR1210 +PR1224	PR1210	18K	24K	6.2K
	PR1224	0	3K	1.74K
C	PC1210	2.7nf	1.8nf	5.6nf
		N15S-GT N16S-GT N16V-GM	N15V-GL	N15V-GM

Current Limit threshold setting
Rocset= (Ivalley * Rds(on) + 40 mV) / 10uA

I_ripple=(19-0.9)*0.9/
(304.89Khz*0.36u*19)=7.811A

OCP=54A/2=27A per phase
Ivalley=27A-7.811A/2=23.1A

H-side MOS:AON6552
Rds(on):
5.6mohm@Vgs=10V
6.7mohm@Vgs=4.5V
Id :20A@Ta=25 degC

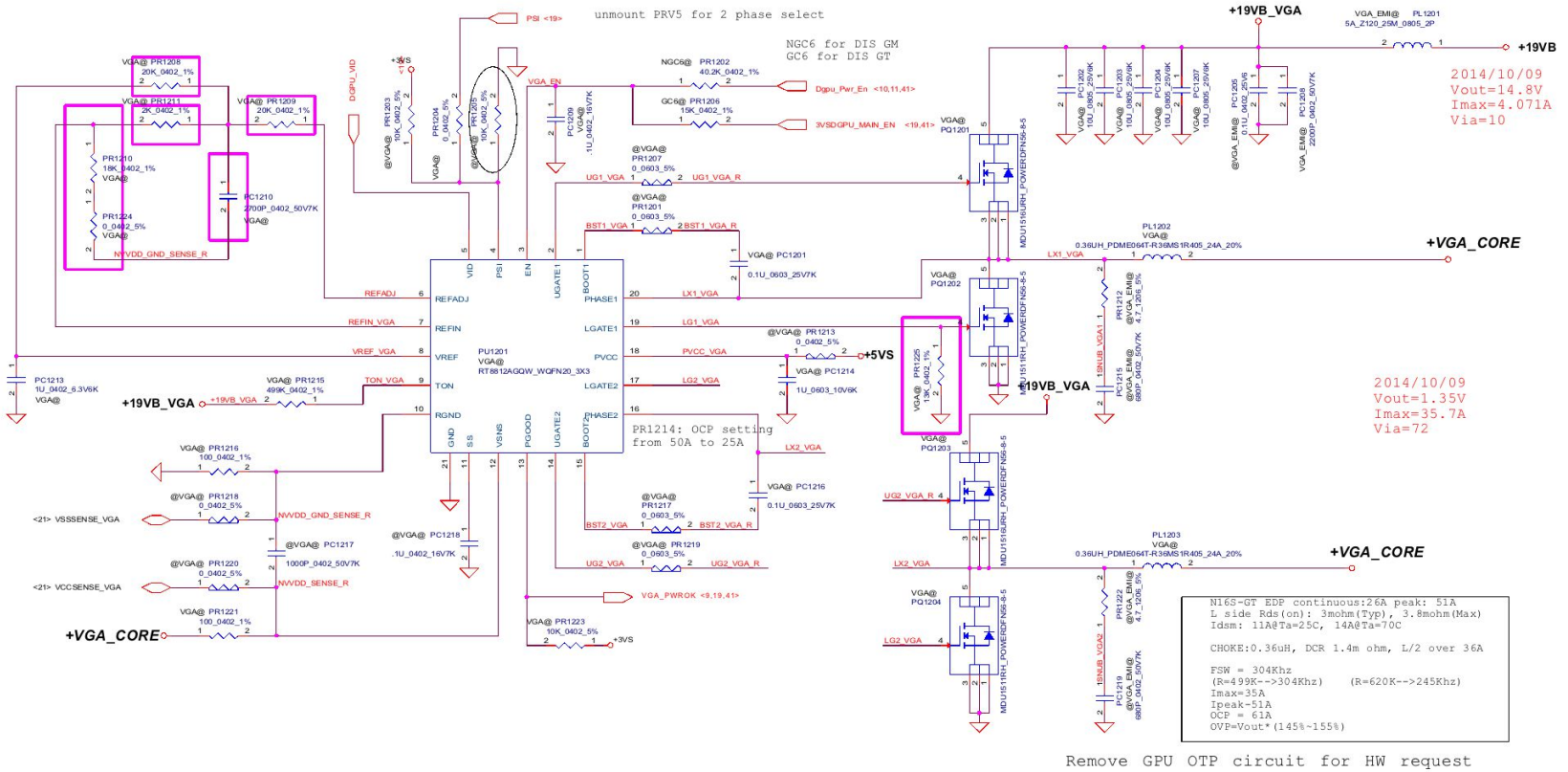
L-side MOS:AON6554
Rds(on):
3.2mohm@Vgs=10V
3~3.8mohm@Vgs=4.5V
Id :85A@Ta=25 degC

Choke: 0.22uH (Size:7*7*4)
Rdc=0.97mohm +-5%
Heat Rating Current=34A
Saturation Current=25A

C=3*330uF (9mohm)=990uF
Vripple=Iripple*ESR(min)=7.811A*3mohm=23.4mV

Different VGA Chip (different EDP-Peak Current) need select different solution

VGA Chip	N14P-GV	N14P-GV2	N14M-GS	N14M-LP	N14P-LP	N14P-GE	N14P-GS	N14P-GT	N15S-GT	N15V-GM
OpenVReg Configurations	Config B	Config B	Config B	Config B	Config B	Config B	Config B	Config B	Config B	Config C
Rated TDP Power at Tj=102C	18W	25W	18W	13W	18.9W	25W	25.6W	35.5W	18W	18.16W
Boosted GPU Total at Tj=102C	25W	32W	25W	20W	23W	N/A	30W	40W	25W	24.72W
EDP-Continuous at Tj=102C	24A	32A	26A	22A	25A	27A	38A	45A	31A	29.2A
EDP-Peak at Tj=102C	35A	55A	45A	35A	35A	40A	60A	75A	60A	44.3A
Istep max (Evaluation)	15A	27A	25A	20A	14A	12A	31.5A	35A		
OCP Setting Current	42A	66A	54A	42A	42A	48A	72A	90A	72A	54A
Rocset	8.96K	12.45K	10.7K	8.96K	8.96K	9.83K	8.3K	9.39K	13K	10.2K
Recommendation	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H2L	2phase 1H2L	2phase 1H1L	2phase 1H1L
Polymer Cap (330uF)	6mohm * 2	9mohm * 3	9mohm * 3	6mohm * 2	6mohm * 2	6mohm * 2	6mohm * 3 (L=0.22uH)	4.5mohm * 3 (L=0.15uH)		
Or OSCON (390uF)	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	NULL	NULL	GT@	GM@



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Compal Electronics, Inc.

Title: **RT8812**

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		1.0

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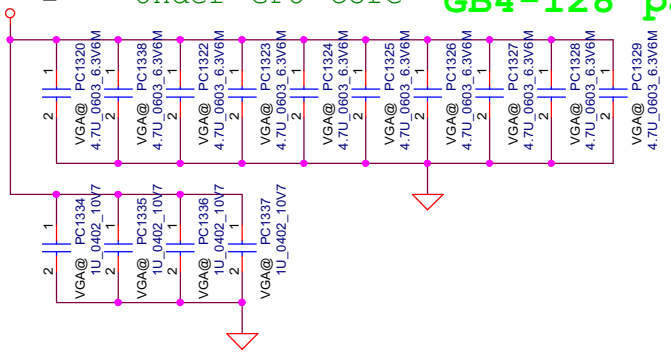
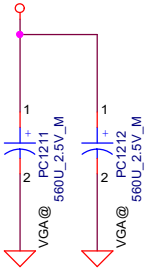
+VGA_CORE Under GPU Core GB4-128 package



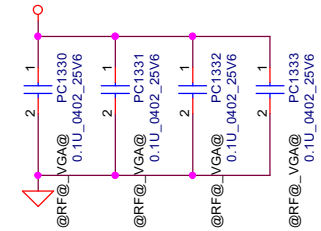
+VGA_CORE



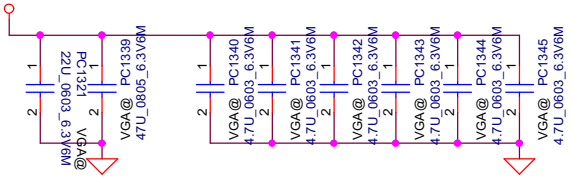
N15x 2013/12/10
Under
4.7uF_0603_10pcs
1uF_0402_4pcs
Near
47uF_0805_1pcs
22uF_0603_1pcs(2PCS unpop)
4.7uF_0805_5pcs

N15x2013/10/17
Under
4.7uF_0603_15pcs
1uF_0402_8pcs
Near
47uF_0805_0pcs
22uF_0603_9pcs(2PCS unpop)
4.7uF_0805_5pcs

+VGA_CORE



+VGA_CORE Near GPU Core



N15x2013/10/02
Under
4.7uF_0603_15pcs
1uF_0402_8pcs
Near
47uF_0805_0pcs
22uF_0805_14pcs
4.7uF_0805_5pcs

N14x
Under
4.7uF_0603_10pcs
0.1uF_0402_4pcs
Near
47uF_0805_1pcs
22uF_0805_1pcs
4.7uF_0805_5pcs

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Title: *VGA_CORE CAP*

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Custom		1.0

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	PG#	Modify List	Date	Phase
1	Design Update	BOM Stucture Identical	P.51	Add GT GM2G for PR1005	20141120	DVT
2	Design Update	IC will Stop Production	P.48	Change the PU701 from APL5930KAI to G971ADJF11U	20141120	DVT
3	Design Update	Nvidia N16S-GT and N16V-GM Open VReg Configuration both use B	P.52	PR1208:20kOhm, PR120920kOhm, PR1210:18kOhm PR1211:2kOhm, PR1224:0Ohm, PC1210:2700pF PR1225:13kOhm	20141120	DVT
4	Design Update	CPU Load Line Request	P.49 P.50	Change the PR817 from 4.99MOhm to 20MOhm. Change the PR807 from 121kOhm to 93.1kOhm. Change the PR813 from 1.91kOhm to 3.65kOhm. Change the PC917 PC908 and PC919 from @ to 22uF.	20141128	DVT
5	Design Update	Solution Change	P.45 P.47 P.51	Change the PU401 from SYX198BQNC to SY8286BRAC Change the PU402 from SYX198CQNC to SY8286CRAC Change the PU601 from SYX198DQNC to SY8288RAC Change the PU1001 from SYX198DQNC to SY8288RAC	20141128	DVT
6	Design Update	RC Value for GPU Sequence Fine Tune GC6 Function	P.51 P.52	GM: PR1002:15kOhm, PC1002:0.1uF. GT: PR1002:4.7kOhm, PC1002:0.1uF. GM(No Support GC6, Use DGPU_PWR_EN) PR1202:40.2kOhm, PC1209:0.1uF. GT(Support GC6, Use 3VSDGPU_MAIN_EN) PR1206:20kOhm, PC1209:0.1uF.	20141128	DVT
7	Design Update	EMI request	P.44	Add PL301 Delete PJ301	20141203	DVT
8	Design Update	FAE request	P.45 P.47 P.51	Change the PC403、PC416、PC601、PC1001 from 1000P_0402_25V8J to 0.1U_0603_25V7K	20141204	DVT
9	Design Update	FAE request	P.45	Change the PC411 from 4.7U_0603_6.3V6M to 4.7U_0402_6.3V6M	20141205	DVT
10	Design Update	Solution Change	P.51	Change the PR1002 from 15K_0402_5% to 15K_0402_1% at GM Change the PR1002 from 4.7K_0402_5% to 10K_0402_1% at GT	20141215	DVT
11	Design Update	Solution Change	P.46	Change the PU501 from RT8207P to RT8207M	20150105	PVT
12	Design Update	GPU sequence fine tune RC value	P.51 P.52	GT: PR1002 change to 0 ohm and depop PC1002. GT: PR1206 change to 15k ohm.	20150119	PVT
13	Design Update	Solution Change	P.44 P.46 P.49	PQ303 change to MDV1526URH. PQ305,PQ306,PQ501 change to MDV1528URH. PQ502 change to SI7716ADN. PQ801,PQ1201,PQ1203 change to MDU1516URH. PQ802,PQ803,PQ1202,PQ1204 change to MDU1511RH.	20150119	PVT
14	Design Update	Thermal request	P.43	Change the PR216 from 16.9K to 18.2K	20150122	PVT
15	Design Update	Solution Change	P.44~47 P.49 P.51~52	Change the PR308 PR401 PR407 PR511 PR601 PR602 PR806 PR1001 PR1002 PR1201 PR1207 PR1217 PR1219 from 0ohm to R-short	20150122	PVT
16	Design Update	DFX request	P.43	Change the PJP201 footprint from ACES_50458-00801-001_8P-T to CVILU_CI9908M2HR0-NH_8P	20150122	PVT

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Title: PIR (PWR)

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Version change list (P.I.R. List)

Item	Page	Title	Date	Issue Description	Solution Description	Phase	Rev.
1	35	Codec	11/10	PC Beep is digital signal	Change C2134 pin 2 connect from GNDA to GND.	DVT	0.2
2	37	USB charger	11/12	USB charger function abnormal.	Change U25 pin 4 from USB_CHARGE_2A to USB_EN Change U26 pin 4 from USB_EN to USB_CHARGE_2A	DVT	0.2
3	37	USB charger	11/17	Board ID change for DVT.	Change R506 from 0_0402_5% to 12K_0402_5%.	DVT	0.2
4	02	Block Diagram	11/19	Some block diagram descirptoin mistake.	Correct block diagram description.	DVT	0.2
5	38	EC	11/19	To solve 3V_EN need to connect to "Fixed code drive high" pin	change 3V_EN from pin 86 to 107, and original pin107 "DGPU_AC_DETECT" signal connect to EC pin 117 (NC now)	DVT	0.2
6	37	USB2.0	11/ 20	Follow EMI's request mail 1120.	Change L26 & L29 from CMMI21T-900Y-N_4P (0805 size) to MCM1012B900F06BP_4P (0504 size), and remove R458, R461, R454, R465 0_0402_5% co-lay resistors.	DVT	0.2
7	37	USB	11/ 26	JUSB3 change from bottom to top side.	Reverse JUSB3 pin connection.	DVT	0.2
8	32	LAN	11/ 27	Request by DFb	Change L2506 from SHI0000AA00 (S INDUC_ 2.2UH +-5% NLC252018T-2R2J-N) [2.2mm height] to SH00000RT00 (S COIL 2.2UH +-20% HPC252012NF-2R2M 1.3A) [1.2mm height)	DVT	0.2
9	39	LED	11/ 27	LED light test	Change R699 & R700 from 301_0402_1% to 470_0402_1%.	DVT	0.2
10	32	Crystal	11/ 27	Crystal EA.	Change C2558 & C2559 from 10P_0402_50V8J to 12P_0402_50V8J	DVT	0.2
11	40	Reset switch	12/ 01	RESET button 接EC_RST# or MAINPWON?	Add R2632 R-short connect to MAINPWON.	DVT	0.2
12	24, 25 26, 27	VRAM	12/ 01	fine tune VRAM	Swap U2004 & U2006 group2 connection. Swap U2008 & U2010 group4 connection.	DVT	0.2
13	40	Batt Switch	12/ 01	DFb request	Change SW4 from DE100000T00 to SN200003I00.	DVT	0.2
14	36	FFC HDD	12/ 01	FFC type HDD could pass Gen2 & Gen3 TX and iEMT EA	Add C413~C416, C538~C541 cap for co-layout without re-driver path.	DVT	0.2
15	19	NV	12/ 02	NV and EC didn't implement GPU_OVERT & GPU_ALERT code.	Change Q2000 from VGA@ to @.	DVT	0.2
16	19	NV	12/ 02	Follow NV's suggestion	1. Change D2002 & R2055 from GC6@ to @, change U2002 & R2628 from @ to GC6@. 2. Change Q2001 pin 2 & 5 from connect +3VSDGPU_MAIN to PLTRST_VGA#.	DVT	0.2
17	41	NV	12/ 03	N16V-GM not support GC6 2.0	Change J14 jumper to R2633 0_0603_5%	DVT	0.2
18	31	CRT	12/ 03	CRT EA RGB rise time fail	Change L2503 from SM01000FH00 (S SUPPRE_ MURATA BLM15BB470SN1D 0402) to SM01000LU00 (S SUPPRE_ MURATA BLM15BA220SN1D 0402)	DVT	0.2
19	35	Part Reference	12/ 03	Correct part referernce type	Change R2120~R2123 to L2511~L2514	DVT	0.2

Security Classification	Compal Secret Data		Compal Electronics, Inc.
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Title	PIR-HW		
Size: Custom	Document Number: Z5WAH M/B LA-B161P		Rev: 1.0
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Item	Page	Title	Date	Issue Description	Solution Description	Phase	Rev.
42	40	Reset button	1/21	follow 2015 project design. Press reset button to pull down EC_RST# signal.	Change R2632 from R-short to non-pop. Change R2631 from non-pop to R-short.	PVT	1.0
43		NPI confirm	1/22	NPI test confirm ready.	1. Change R65, R427, R428, R368~R375,R2552, R2125, R2131, R2611, R467, R2618~R2626, R854 from 0_0402_5% to R-short. 2. Change R2075, R81 from 0_0603_5% to R-short.	PVT	1.0
44	39	update footprint	1/22	Link LED symbol to CIS.	Correct LED6 & LED7 footprint from LED_HT-210UD5-NB5_3P to LED_LTST-S115KFTBKT-CA_3P	PVT	1.0
45	37	USB power switch	1/22	Follow 2015 project USB power switch OC pin design.	Change R454 & R466 from R-short to non-pop.	PVT	1.0

Item	Page	Title	Date	Issue Description	Solution Description	Phase	Rev.
21	17	Test	12/05	Test plan	Reserve Q2007 , place close to U45.	DVT	0.2
22	10	Test	12/05	Test plan	Reserve R2634 , place close to U30.	DVT	0.2
23	13,17	DRAM	12/10	Choose cap. for better placement.	Depop C18, pop C118.	DVT	0.2
24	39	Lid SW	12/10	Change main source.	Change U4 PN to SA00008K800.	DVT	0.2
25	37	USB20 choke	12/17	SM070003K00 will shift when SMT and prohibit by factory.	Change L26 & L29 to SM070003Y00.	DVT	0.2
26	19	NV	12/17	To prevent could not read or read wrong graphic temperature via I2C and cause over temperature.	Add Q2000 to let GPU_OVERT work.	DVT	0.2
27	19	NV	12/17	VGA_PWROK pull high to +3VS via 10K ohm, but R2014 10K pull down willl make VGA_PWROK high voltage level out of spec.	Change R2014 from 10K to 200K ohm. (Follow NV reference schematic.)	DVT	0.2
28	38	Board ID	12/22	Change board ID for PCB Revision 0.3	Change R506 from SD028120280 12K ohm to SD028150280 15K ohm	PVT	1.0
29	13, 17	POS Cap	12/22	Follow schematic design common rule, POS Cap should use Serial P/N	Change C18 & C118 from SGA20331E10 to SGA00009S00	PVT	1.0
30	39	ON/OFF button	12/30	SW6 is for RD test at NPI phase only.	Change SW6 from DB@ to @.	PVT	1.0
31	39	LED	12/30	LED test with DVT ME module.	Change R699 & R700 from 470 ohm (SD034470080) to 560 ohm (SD000008380) Change R698 & R701 from 390 ohm (SD00000QZ00) to 430 ohm (SD00000LM00)	PVT	1.0
32	19	NV	12/30	GPU throttle test.	Reserve U17 for test.	PVT	1.0
33	39	NV	12/30	Reserve level shift circuit to prevent Elan touch pad back drive issue.	Reserve Q2008, R2640~R2642 level shift circuit.	PVT	1.0
34		Component	1/7	Follow standard part	Change Q7, Q8, Q14, Q15, Q40, Q1007, Q2000, Q2001, Q2003, Q2004, Q2008 from SB00000DH00 (S TR DMN66D0LDW-7 2N SOT363-6) to SB00000PV00 (S TR L2N7002DW1T1G 2N SC88-6)	PVT	1.0
35	36	Test	1/8	Reserve G-SEN_INT2 connector to JHDD2.	Reserve R2643 & R2644.	PVT	1.0
36	34	WLAN	1/12	SUSCLK will back drive to +3VS_WLAN when S3 or S5 with Broadcome NFA435 module. Check module datasheet not support SUSCLK, and intel module could define as NC.	Change R2612 from R-short to non-pop.	PVT	1.0
37	40	Screw hole	1/12	ME change NGFF standoff hole from 3.2 change to 3.3mm	Change H17 Footprint from H_3P2 to H_3P3.	PVT	1.0
38	35	Codec	1/19	ALC255 have PC beep in detect ciucuit in chip. Signal level under 400mV will disable PC Beep function.	Change R2140 from SD028470280 (47K_0420_5%) to SD028270280 (27K_0402_5%)	PVT	1.0
39	41	NV	1/19	To meet N16S-GT power sequence	Add virtual symbol R469 for SGT@, change vaule from 47K_0402_5% to 20K_0402_5%. Original R469 change from VGA@ to VGM@.	PVT	1.0
40	37	USB Charger	1/19	USB charger CB pin need a dedicate pin to control behavior.	Change USB charger CB control pin from SUSP# to USB_CHARGE_CB connect to EC pin 86.	PVT	1.0
41	18	ESD	1/21	ESD Jason request to reserve a cap for DIMM_DRAMRST#.	Reserve C2611.	PVT	1.0