


LCFC Confidential

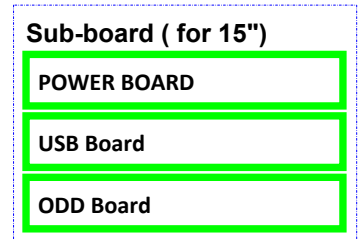
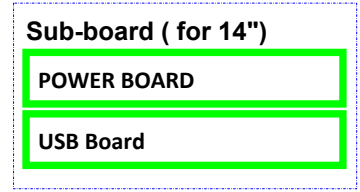
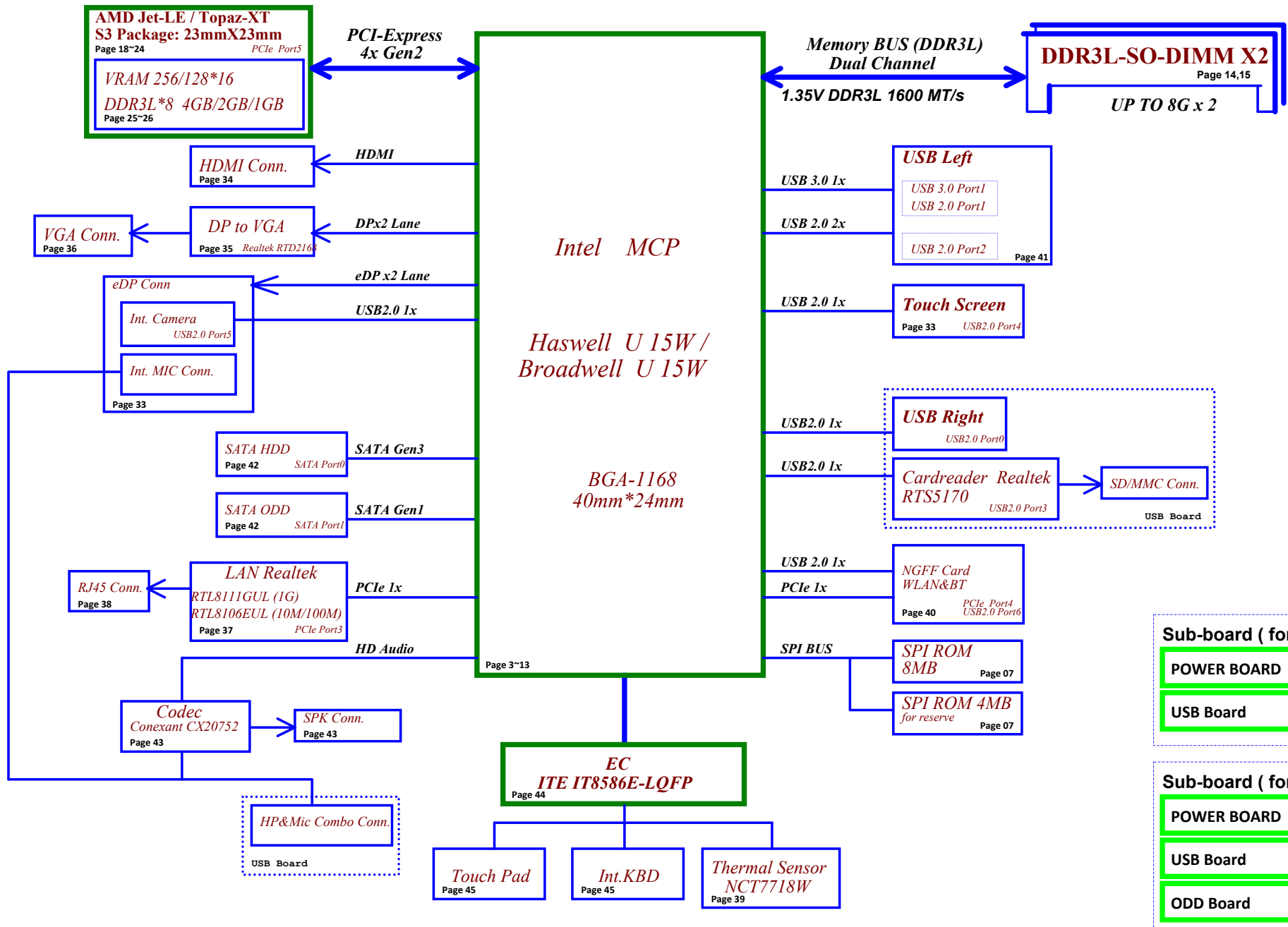
ACLU3 M/B Schematics Document

Intel Broadwell U-Processor with DDRIII L + AMD Jet-LE/Topaz-XT GPU

2014-09-10

REV: 0.4

Security Classification	LC Future Center Secret Data			Title		
Issued Date	2013/08/08	Deciphered Date	2013/08/05	Cover Page		
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Security Classification		LC Future Center Secret Data		Title	
Issued Date	2013/08/08	Deciphered Date	2013/08/05	Block Diagram	
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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane	B+	+3VALW	+3VALW_PCH	+1.35V	+5VS
					+3VS
State					+1.5VS
					+1.35VS
					+1.05VS
					+0.675VS
					CPU_CORE
					+VGA_CORE
					+3VGS
					+1.8VGS
					+1.35VGS
					+0.95VGS
S0	O	O	O	O	O
S3	O	O	O	O	X
S3 Battery only	O	O	O	O	X
S5 S4/AC Only	O	O	O	X	X
S5 S4 Battery only	O	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

USB 2.0 XHCI		USB 3.0 XHCI	
0	USB Port (Right Side)		
1	USB Port1 (Left Side)	1	USB Port1 (Left Side)
2	USB Port2 (Left Side)	2	
3	Cardreader	3	
4	TOUCH PANEL	4	
5	Camera		
6	NGFF(WLAN)		
7			

BOM Structure Table

BOM Structure	BTO Item
@	Not stuff
14@	For 14" part
15@	For 15" part
UMA@	UMA SKU part
PX@	Discrete GPU SKU part
100M@	100M LAN Part
GIGA@	GIGA LAN Part
JET@	For AMD Jet GPU part
TOPAZ@	For AMD Topaz GPU part
RANKA@	For VRAM RankA part
RANKB@	For VRAM RankB part
ME@	ME part(connector, hole)
TS@	For support touch panel sku part
AOAC@	AOAC support part
H2@	Hynix 128Mx16 VRAM part
H4@	Hynix 256Mx16 VRAM part
M2@	Micron 128Mx16 VRAM part
M4@	Micron 256Mx16 VRAM part
S2@	Samsung 128Mx16 VRAM part
S4@	Samsung 256Mx16 VRAM part
H2GX4@	Hynix 128Mx16 VRAM x4pcs sku
M2GX4@	Micron 128Mx16 VRAM x4pcs sku
S2GX4@	Samsung 128Mx16 VRAM x4pcs sku
H4GX4@	Hynix 256Mx16 VRAM x4pcs sku
M4GX4@	Micron 256Mx16 VRAM x4pcs sku
S4GX4@	Samsung 256Mx16 VRAM x4pcs sku
H2GX8@	Hynix 128Mx16 VRAM x8pcs sku
M2GX8@	Micron 128Mx16 VRAM x8pcs sku
S2GX8@	Samsung 128Mx16 VRAM x8pcs sku
H4GX8@	Hynix 256Mx16 VRAM x8pcs sku
M4GX8@	Micron 256Mx16 VRAM x8pcs sku
S4GX8@	Samsung 256Mx16 VRAM x8pcs sku
CD@	Cost down part
BCD@	Cost down part for BDW project
SINGLE@	Single Rank VRAM sku
DUAL@	Dual Rank VRAM sku

SMBUS Control Table

	SOURCE	VGA	BATT	IT8586E	SODIMM	WLAN WIMAX	Thermal Sensor	PCH	TP Module	charger
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VALW	X	V	V +3VALW	X	X	X	X	X	V
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	V +3VGS	X	V +3VS	X	X	V +3VS	X +3VALW_PCH	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	V +3VS	V +3VS	X	V +3VALW_PCH	X	X

PCIe PORT LIST

Port	Device
1	
2	
3	LAN
4	WLAN
5	Discrete GPU
6	

EC SM Bus1 address

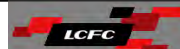
EC SM Bus2 address

PCH SM Bus address

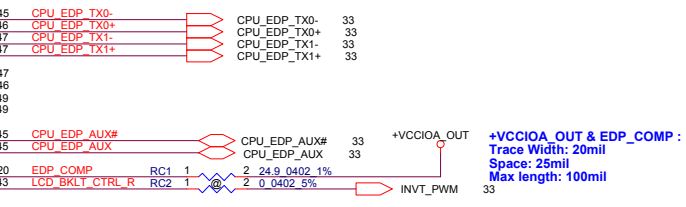
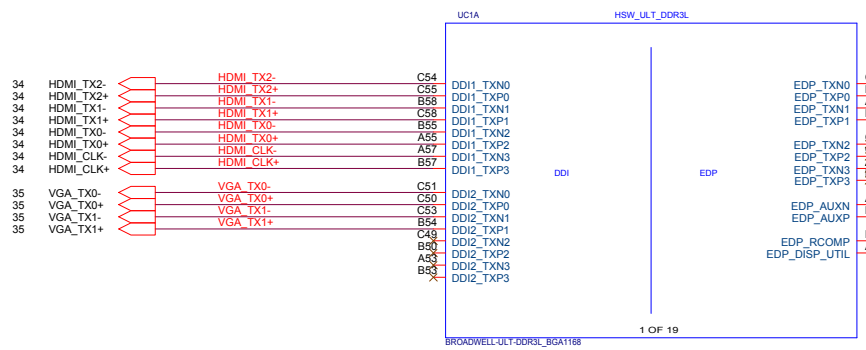
Device	Address	Device	Address	Device	Address
Smart Battery	0X16	Thermal Sensor NCT7718W	1001_100xb	DDR DIMMA	1010 000Xb
Charger	0001 0010 b	VGA	0x41(default)	DDR DIMMB	1010 010Xb
		PCH	need to update	Wlan	Rsvd

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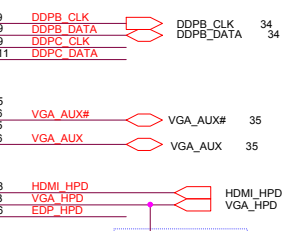
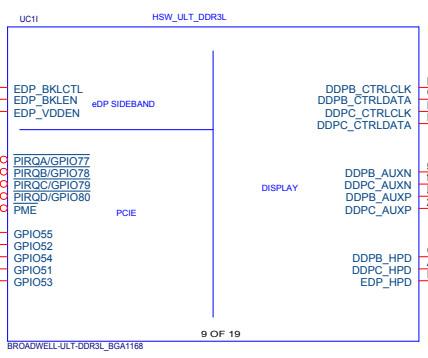
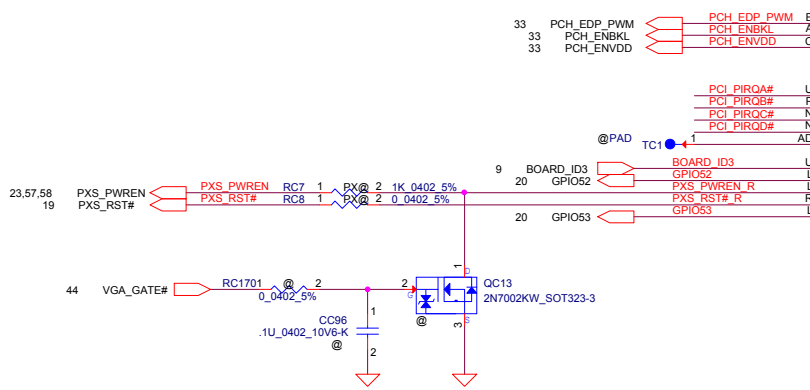
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HDMI D2
HDMI D1
HDMI D0
HDMI CLK
DP TO VGA Converter

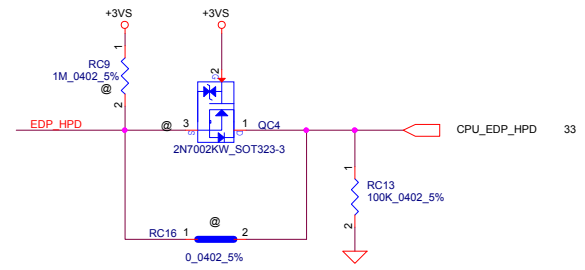
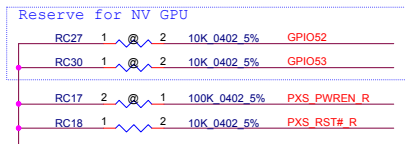
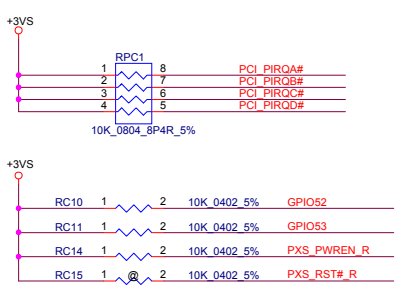


+VCCIOA_OUT & EDP_COMP :
Trace Width: 20mil
Space: 25mil
Max length: 100mil



DDPx_CTRLDATA
The signal has a weak internal pull-down.
* H Port is detected.
L Port is not detected.

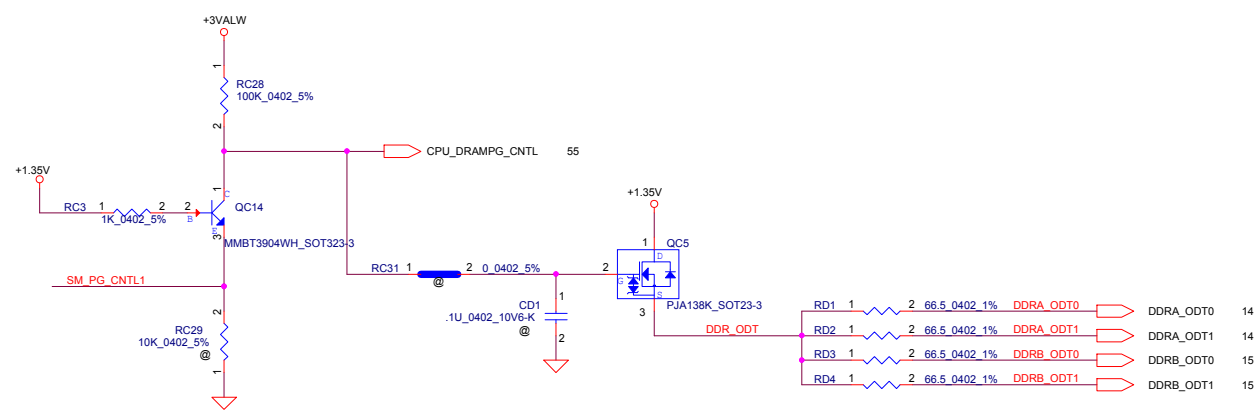
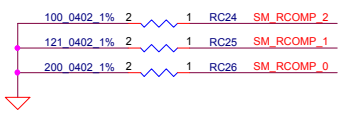
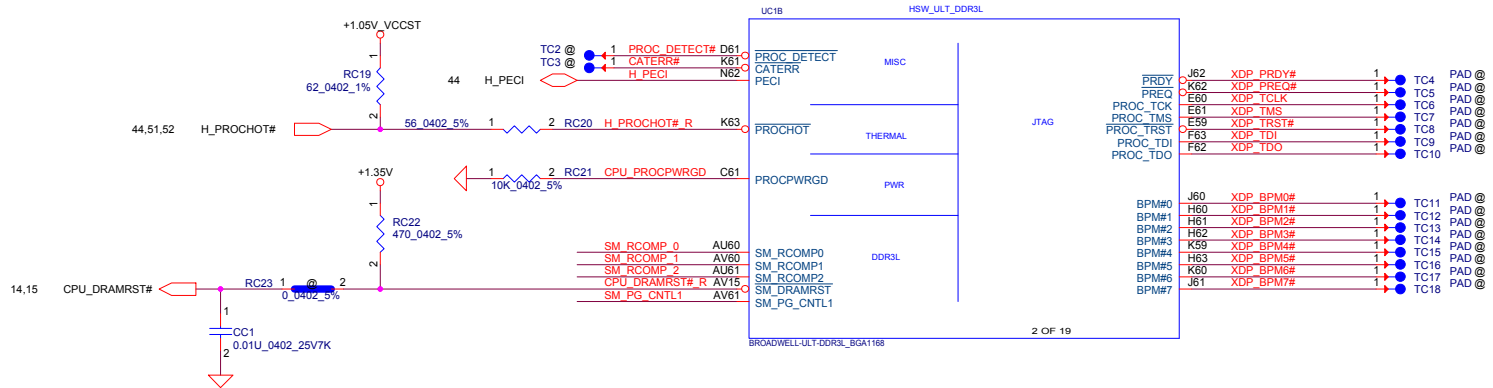
VGA HPDI pull down 100K at DP To VGA Converter side.



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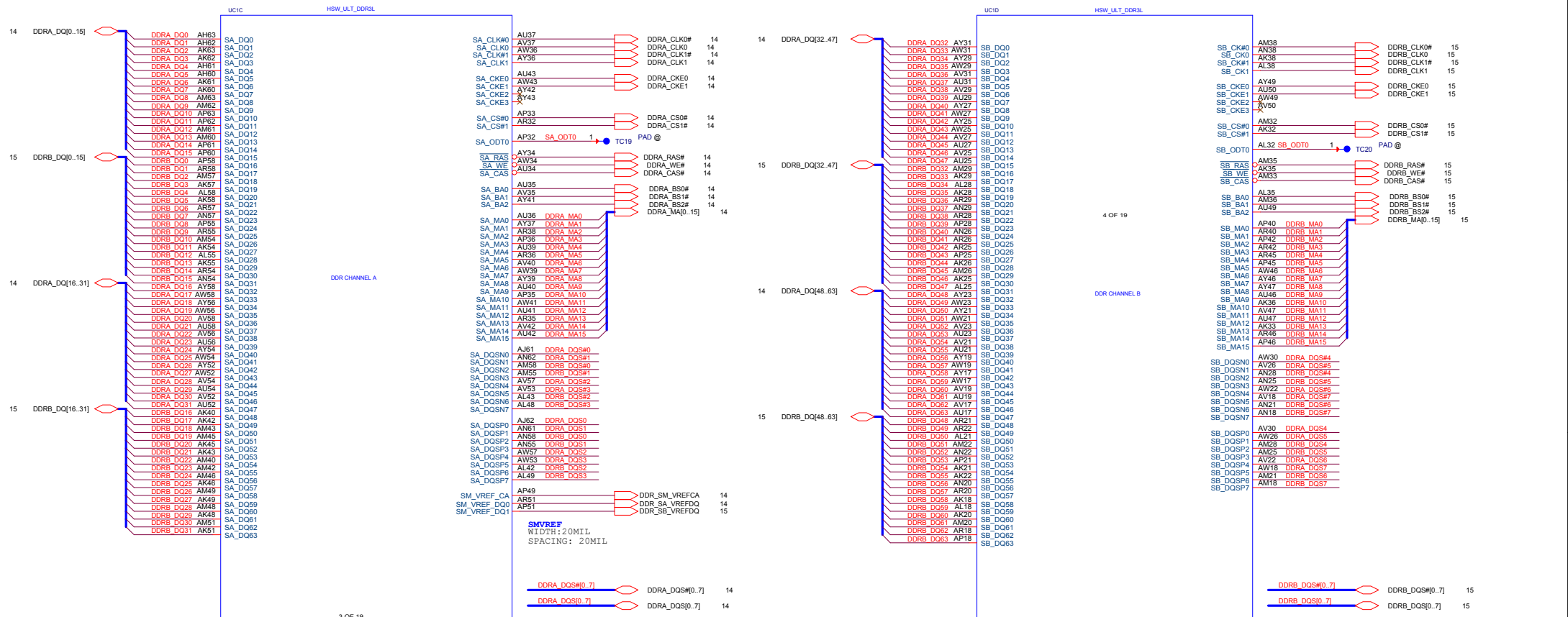
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Title	Document Number	Rev
MCP (DDI,EDP)	ACLU3	0.4
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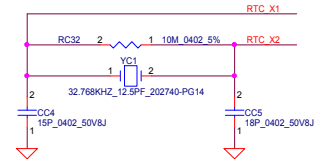


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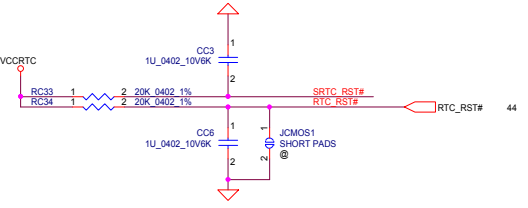
Title		
MCP (MISC, THERMAL, JTAG)		
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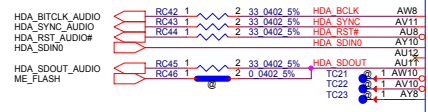
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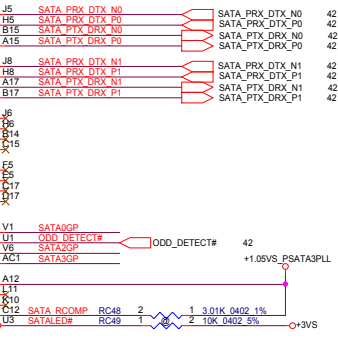
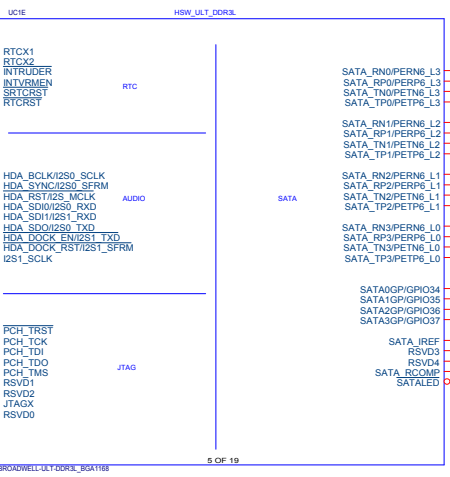
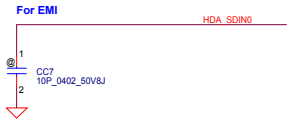
CRYSTAL
 1. Space 15mil
 2. No trace under crystal
 3. Place on opposite side of MCP for temp influence



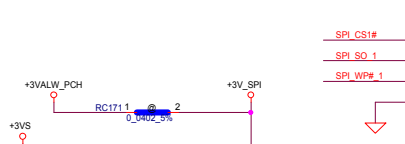
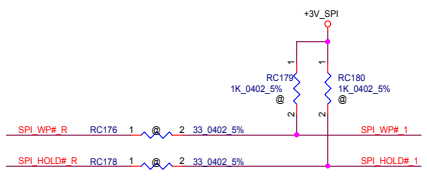
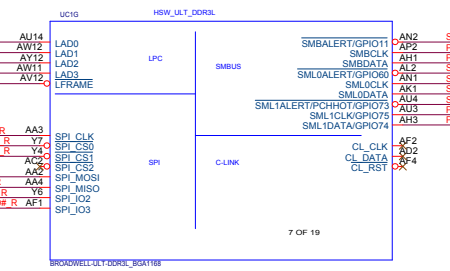
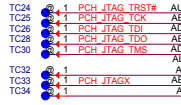
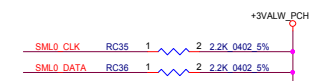
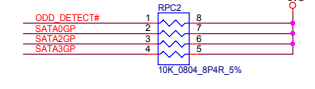
INTVRMEN
 H Integrated VRM enable (Default)
 L Integrated VRM disable
 (INTVRMEN should always be pull high.)



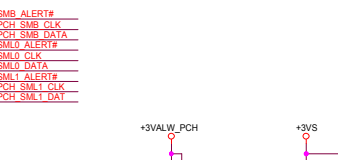
HDA_SDO This signal has a weak internal pull-down.
 0 = Enable security measures defined in the Flash Descriptor.
 1 = Disable Flash Descriptor Security(override). This strap should only be asserted high during external pull-up in manufacturing/debug environments ONLY.



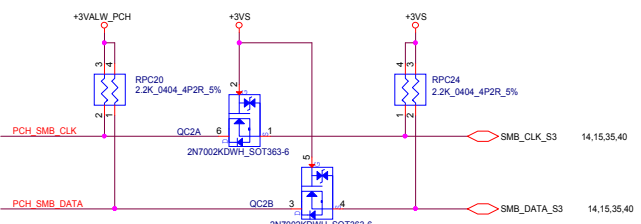
IREF6RCOMP
 Width: 12-15mil
 Space: 12mil
 Length: 500mil



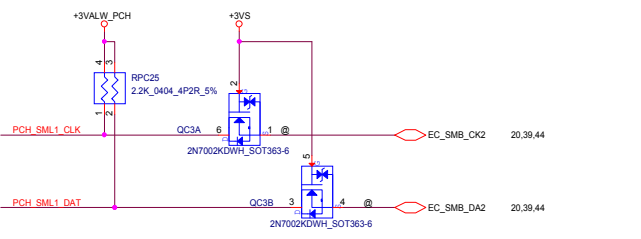
+3V_SPI
 1. If support DS3, connect to +3VS and don't support EC mirror code;
 2. If don't support DS3, connect to +3VALW_PCH and support EC mirror code.



DIMM1, DIMM2, NGFF

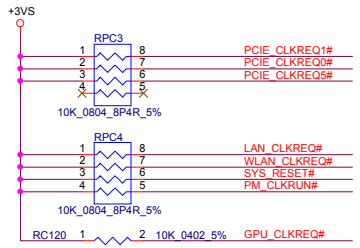


GPU, EC, Thermal Sensor



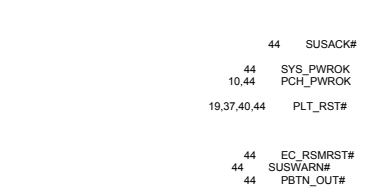
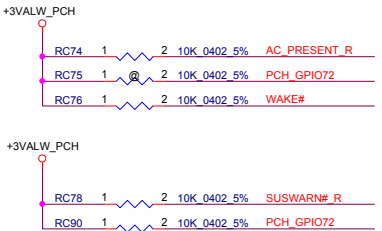
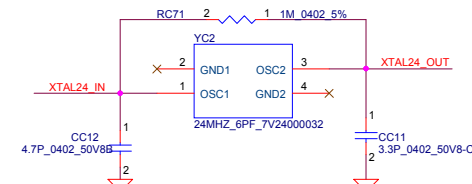
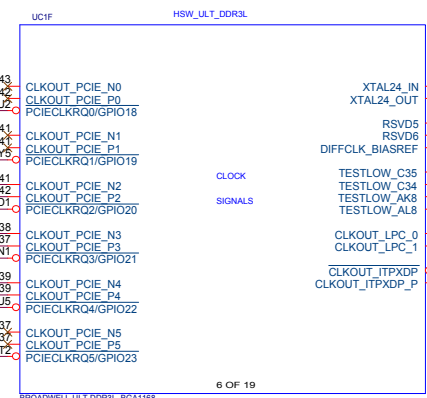
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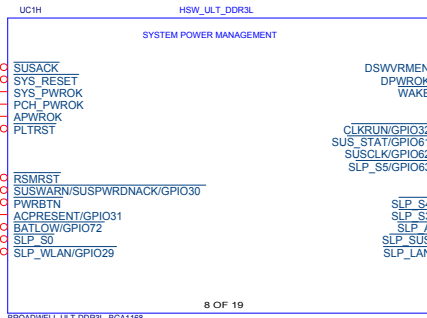


PCIE CLK2 LAN
PCIE CLK3 WLAN
PCIE CLK4 GPU

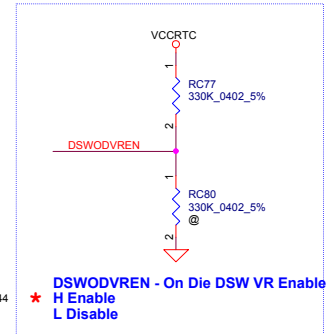
37 CLK_PCIE_LAN#
 37 CLK_PCIE_LAN#
 37 LAN_CLKREQ#
 40 CLK_PCIE_WLAN#
 40 CLK_PCIE_WLAN#
 40 WLAN_CLKREQ#
 19 CLK_PCIE_GPU#
 19 CLK_PCIE_GPU#
 20 GPU_CLKREQ#



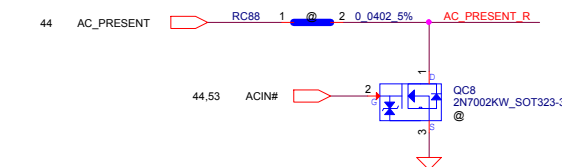
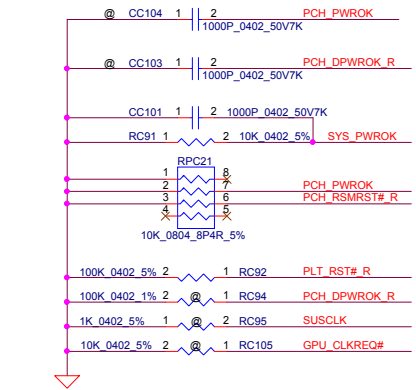
Reserve for DS3
 44 SUSACK#
 44 SYS_PWROK
 10,44 PCH_PWROK
 19,37,40,44 PLT_RST#
 44 EC_RSMRST#
 44 SUSWARN#
 44 PBTN_OUT#



44 SUSACK#
 44 SYS_PWROK
 10,44 PCH_PWROK
 19,37,40,44 PLT_RST#
 44 EC_RSMRST#
 44 SUSWARN#
 44 PBTN_OUT#

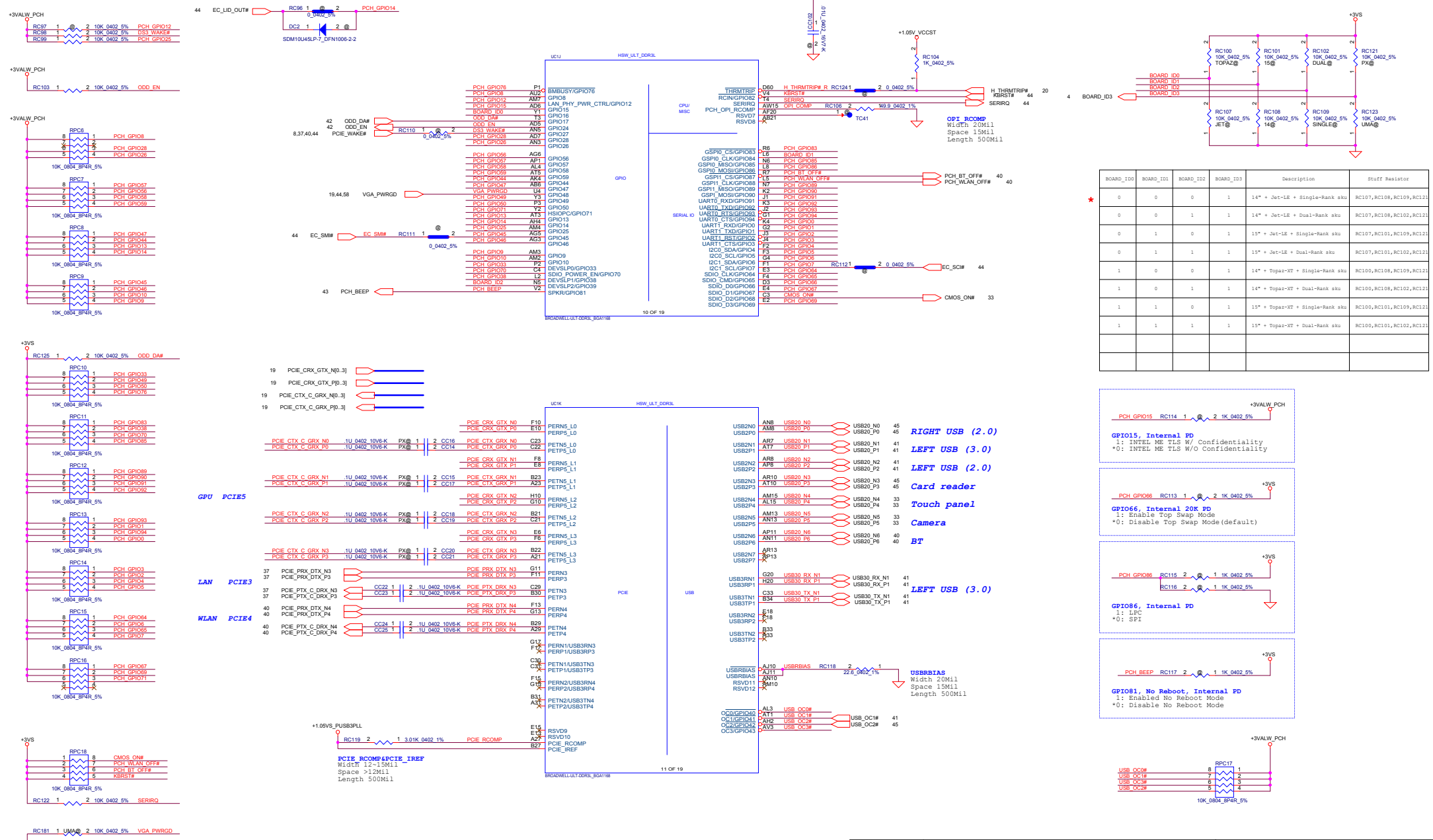


* DSWODVREN - On Die DSW VR Enable
 H Enable
 L Disable



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BOARD_ID0	BOARD_ID1	BOARD_ID2	BOARD_ID3	Description	Stuff Resistor
0	0	0	1	14" + Jet-LE + Single-Rank sku	RC107,RC108,RC109,RC121
0	0	1	2	14" + Jet-LE + Dual-Rank sku	RC107,RC108,RC102,RC121
0	1	0	1	15" + Jet-LE + Single-Rank sku	RC107,RC101,RC109,RC121
0	1	1	1	15" + Jet-LE + Dual-Rank sku	RC107,RC101,RC102,RC121
1	0	0	1	14" + Topaz-XT + Single-Rank sku	RC100,RC108,RC109,RC121
1	0	1	1	14" + Topaz-XT + Dual-Rank sku	RC100,RC108,RC102,RC121
1	1	0	1	15" + Topaz-XT + Single-Rank sku	RC100,RC101,RC109,RC121
1	1	1	1	15" + Topaz-XT + Dual-Rank sku	RC100,RC101,RC102,RC121

RIGHT USB (2.0)

LEFT USB (3.0)

LEFT USB (2.0)

Card reader

Touch panel

Camera

BT

LEFT USB (3.0)

USBRRBIAS

LEFT USB (3.0)

GPIO15, Internal PD
1: INTEL ME TLS W/ Confidentiality
*0: INTEL ME TLS W/O Confidentiality

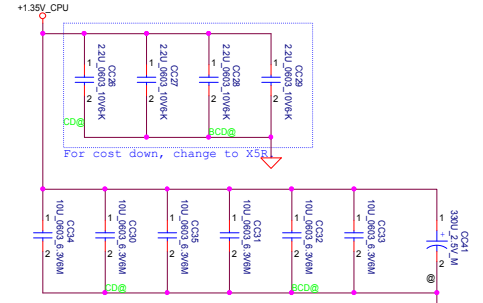
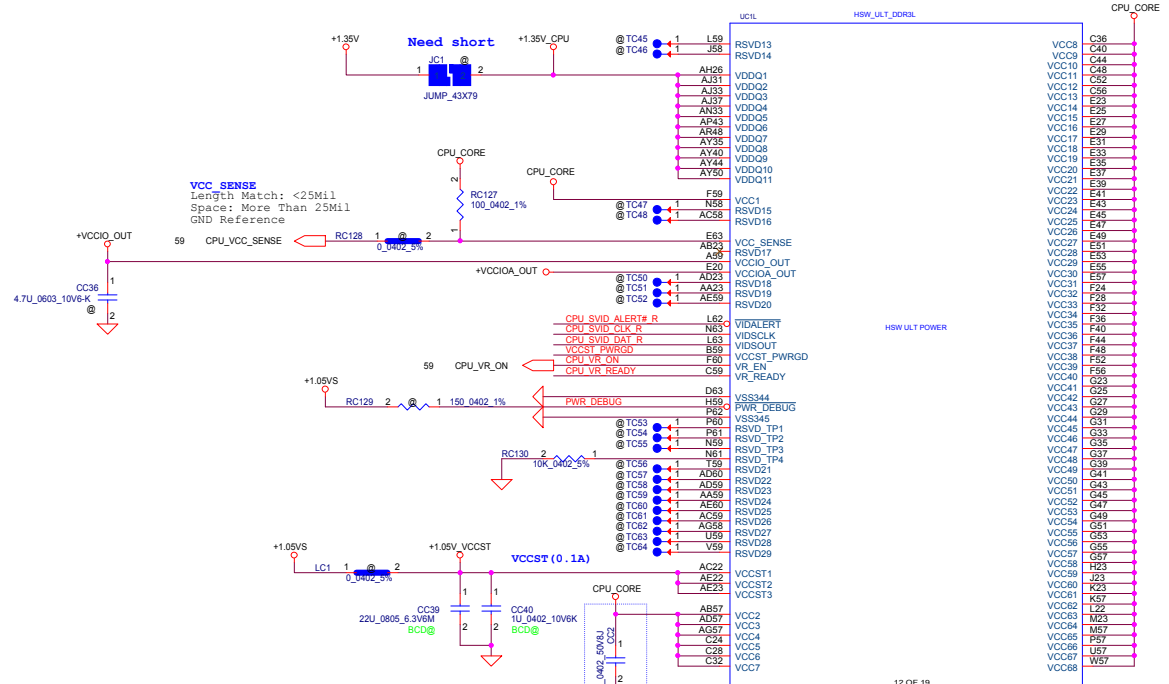
GPIO66, Internal 20K PD
1: Enable Top Swap Mode
*0: Disable Top Swap Mode (default)

GPIO86, Internal PD
1: I2C
*0: SPI

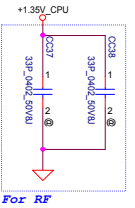
GPIO81, No Reboot, Internal PD
1: Enabled No Reboot Mode
*0: Disable No Reboot Mode

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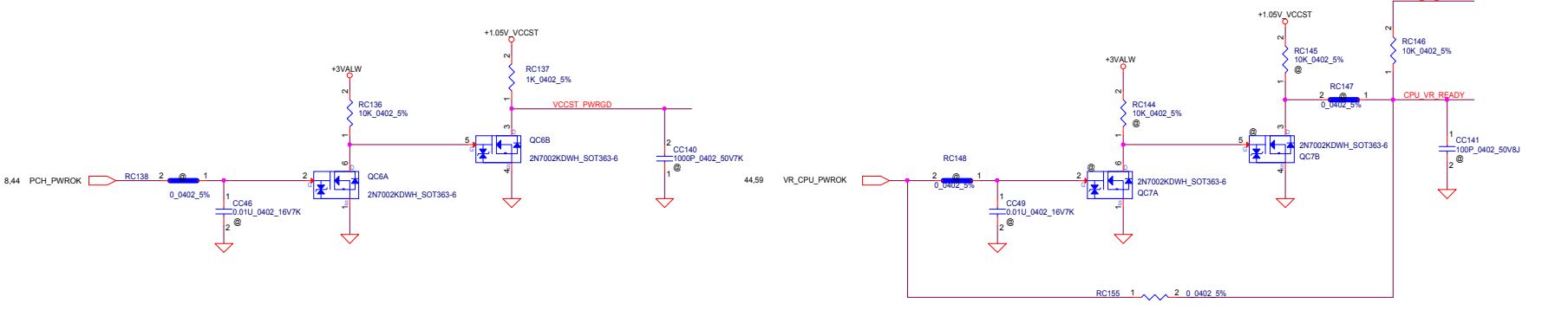
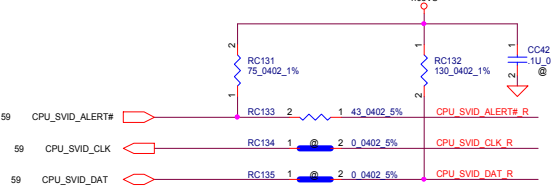
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1.35V_CPU (1.4A)
 HW 4PCS 2.2UF CAP Mounted
 HW 6PCS 10UF CAP Mounted
 PWR 2PCS 470U Near VR Output



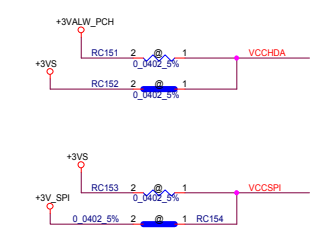
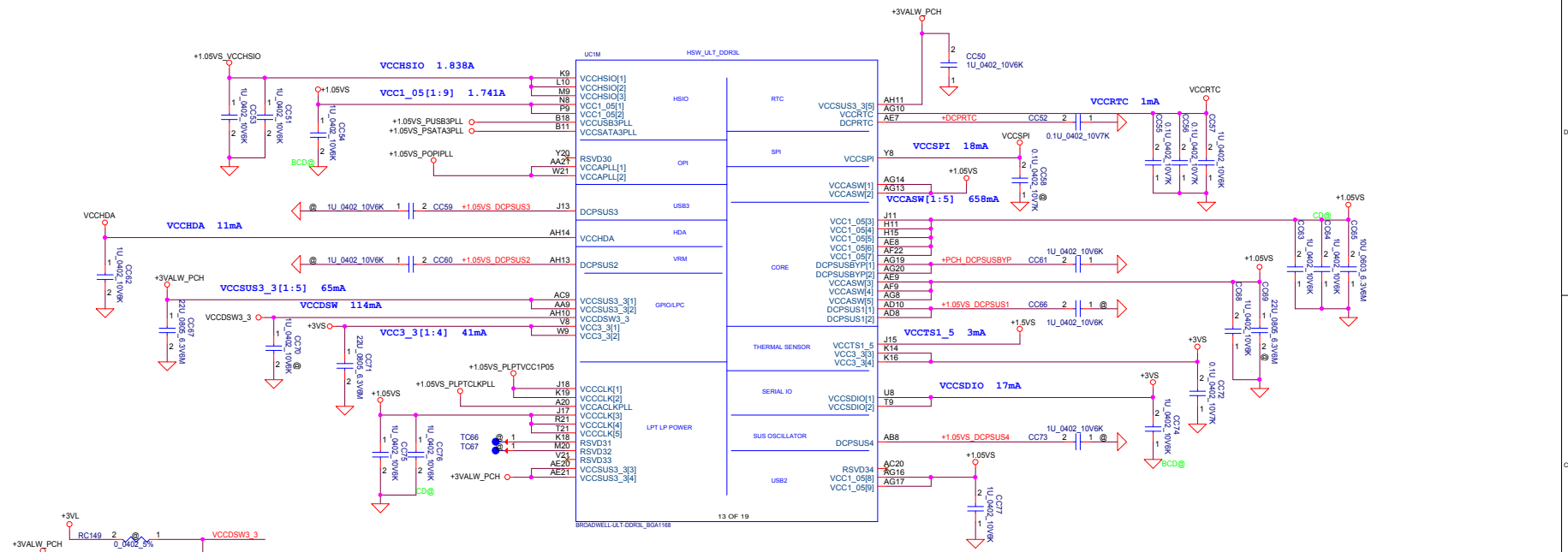
SVID
 1, Stripline Line, No More Than 6000Mil
 2, Alert# Route Between CLK and Data
 3, CLK Length < Data Length < CLK Length + 2000Mil
 4, Space at least 18Mil



UC1L	HSW_ULI_DDR1L	CPU_CORE
RSVD13	VCC8	C36
RSVD14	VCC9	C40
AH26	VCC10	C44
AJ31	VCC11	C52
AJ33	VDD01	C58
AJ37	VDD02	E23
AN33	VDD03	VCC13
AP43	VDD04	VCC14
AR48	VDD05	VCC15
AY35	VDD06	VCC16
AY40	VDD07	VCC17
AY44	VDD08	VCC18
AY50	VDD09	VCC19
	VDD10	VCC20
	VDD11	E37
	VCC1	E39
	VCC2	E41
	VCC3	E43
	VCC4	E45
	VCC5	E47
	VCC6	E49
	VCC7	E51
	VCC8	E53
	VCC9	E55
	VCC10	E57
	VCC11	F24
	VCC12	F28
	VCC13	F32
	VCC14	F36
	VCC15	F40
	VCC16	F44
	VCC17	F48
	VCC18	F52
	VCC19	F56
	VCC20	G23
	VCC21	G25
	VCC22	G27
	VCC23	G29
	VCC24	G31
	VCC25	G33
	VCC26	G35
	VCC27	G37
	VCC28	G39
	VCC29	G41
	VCC30	G43
	VCC31	G45
	VCC32	G47
	VCC33	G49
	VCC34	G51
	VCC35	G53
	VCC36	G55
	VCC37	G57
	VCC38	H23
	VCC39	K23
	VCC40	K27
	VCC41	L27
	VCC42	M23
	VCC43	M27
	VCC44	M31
	VCC45	M35
	VCC46	M39
	VCC47	M43
	VCC48	M47
	VCC49	M51
	VCC50	M55
	VCC51	M59
	VCC52	M63
	VCC53	M67
	VCC54	M71
	VCC55	M75
	VCC56	M79
	VCC57	M83
	VCC58	M87
	VCC59	M91
	VCC60	M95
	VCC61	M99
	VCC62	M103
	VCC63	M107
	VCC64	M111
	VCC65	M115
	VCC66	M119
	VCC67	M123
	VCC68	M127

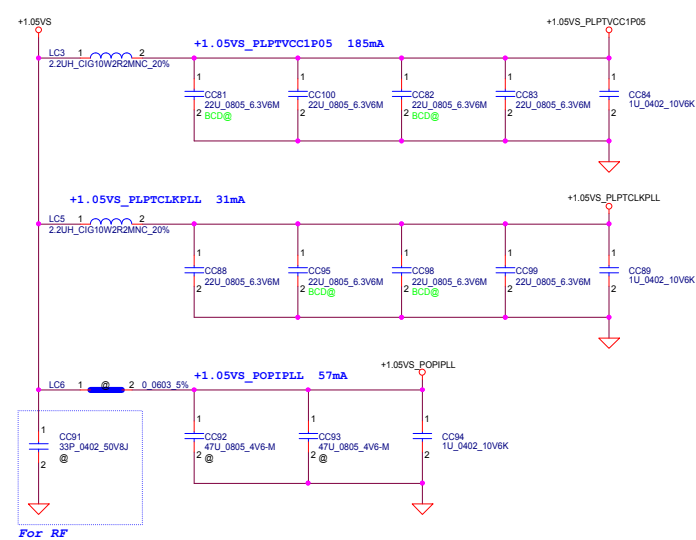
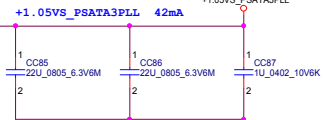
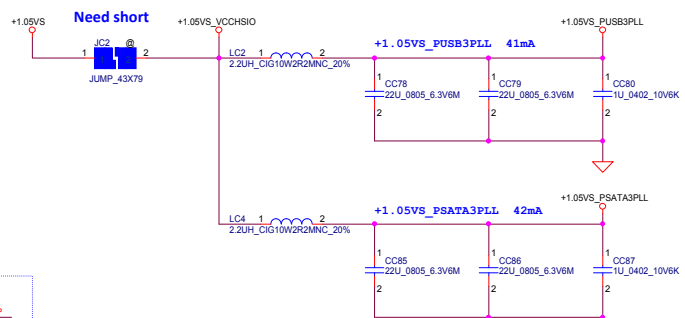
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Issued Date	2013/08/08	Deciphered Date	2013/08/05	Size	Document Number
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Date:	Wednesday, September 17, 2014	Sheet	10	of	50

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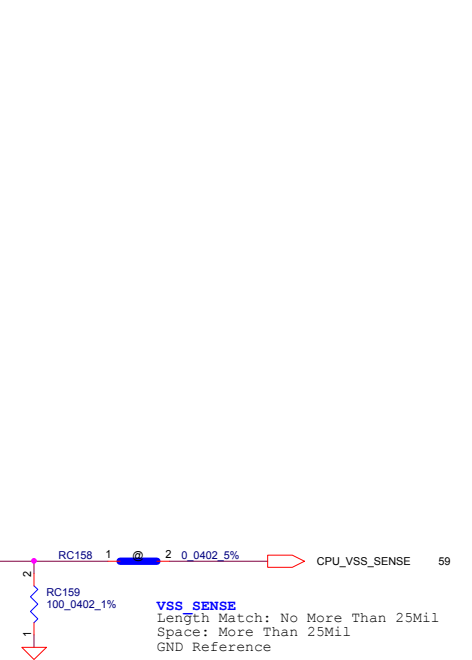
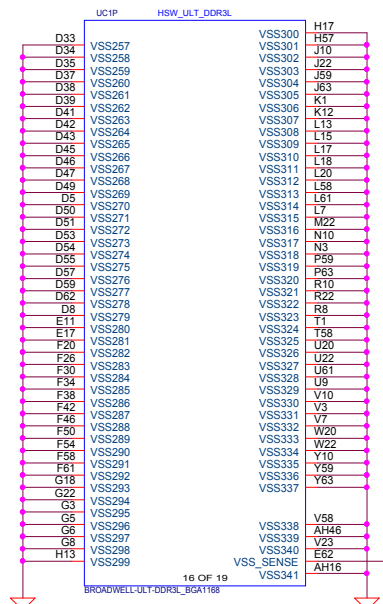
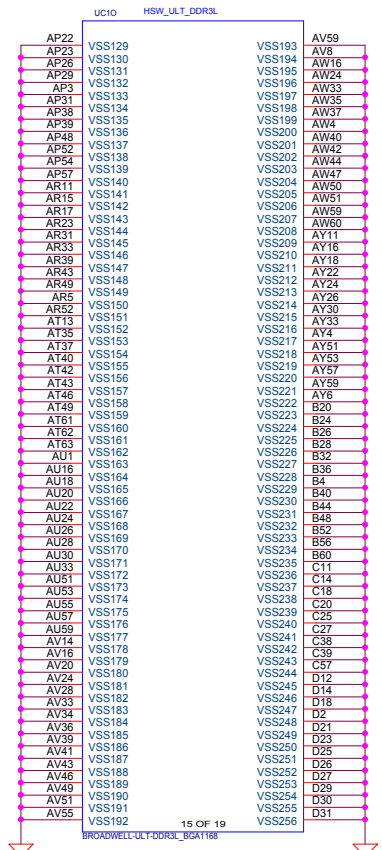
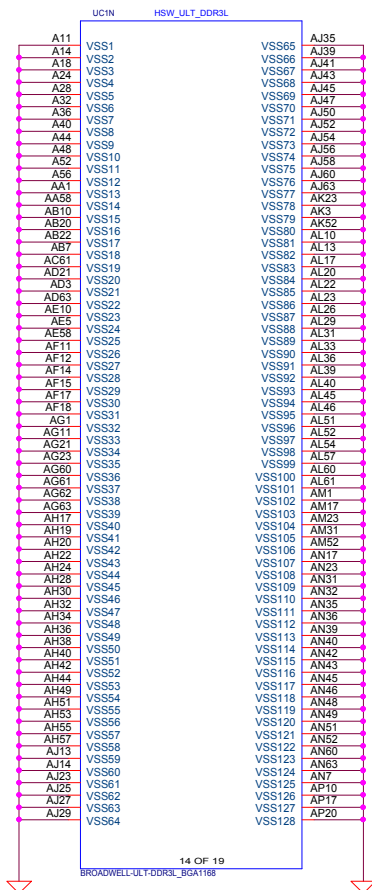



VCCSW3_3 CC80 1 2 0.47U_0402_25V6K +PCH_DCPUSBYSP

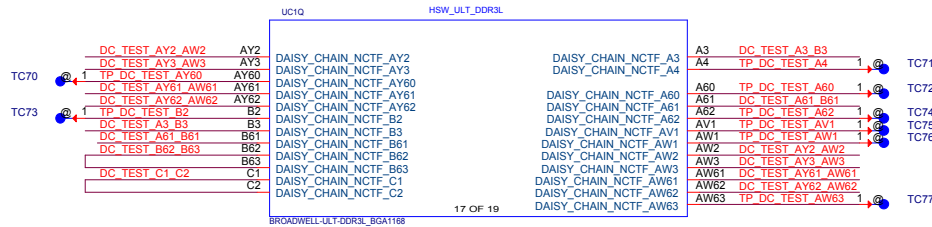
For Intel recommend, place one 0.47uF capacitor to address temporary inrush current. (DOC. 489999)



For RF

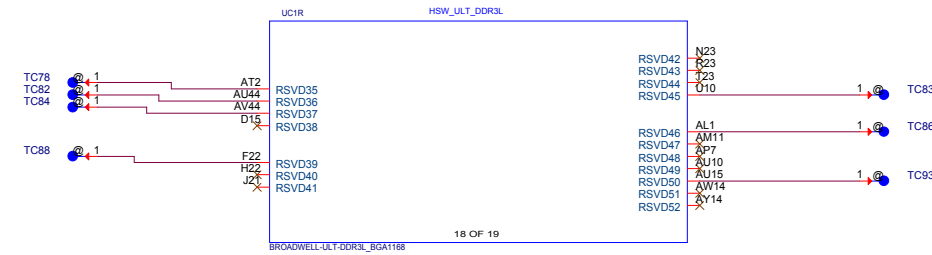


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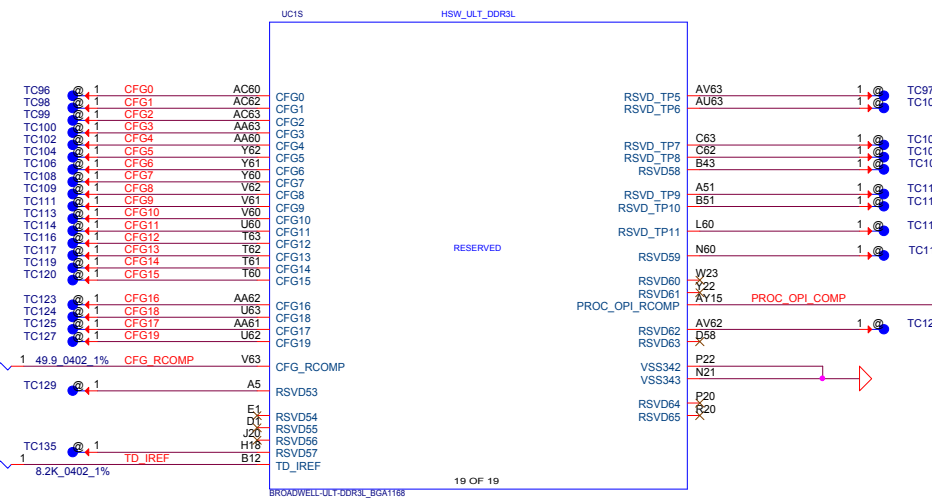
BROADWELL-ULT-DDR3L_BGA1188

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BROADWELL-ULT-DDR3L_BGA1188

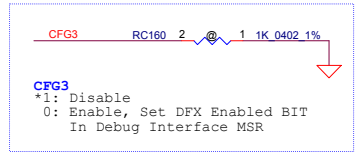
18 OF 19



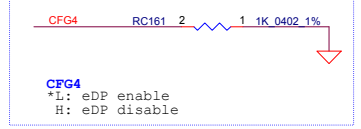
BROADWELL-ULT-DDR3L_BGA1188

19 OF 19

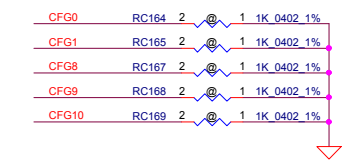
CFG_RCAMP&TD_IREF
Width 20Mil
Space 15Mil
Length 500Mil



CFG3
*1: Disable
0: Enable, Set DFX Enabled BIT
In Debug Interface MSR



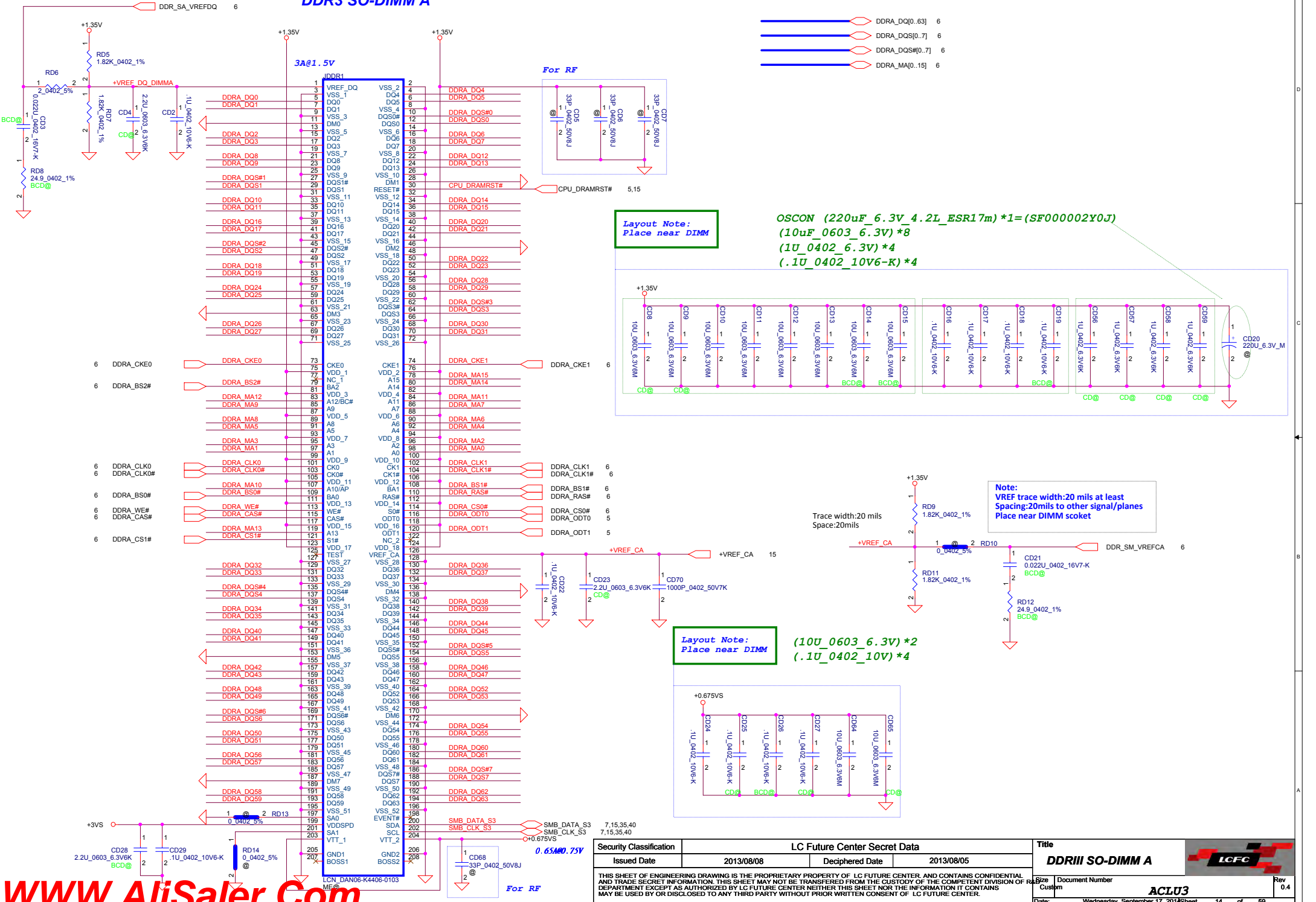
CFG4
*L: eDP enable
H: eDP disable



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Title		
MCP (OTHER)		
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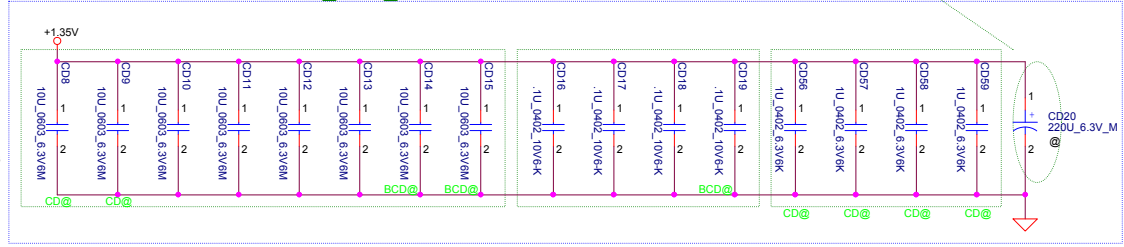
DDR3 SO-DIMM A



- DDRA_DQ[0..63] 6
- DDRA_DQS[0..7] 6
- DDRA_DQS#[0..7] 6
- DDRA_MA[0..15] 6

Layout Note:
Place near DIMM

OSCON (220uF_6.3V_4.2L_ESR17m) *1=(SF000002Y0J)
(10uF_0603_6.3V) *8
(1U_0402_6.3V) *4
(.1U_0402_10V6-K) *4

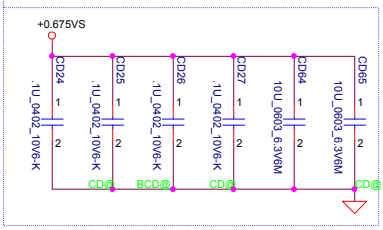


Note:
VREF trace width:20 mils at least
Spacing:20mils to other signal/planes
Place near DIMM socket

Trace width:20 mils
Space:20mils

Layout Note:
Place near DIMM

(10U_0603_6.3V) *2
(.1U_0402_10V) *4

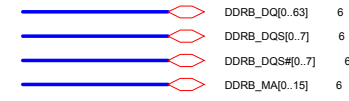


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DDR3 SO-DIMM B

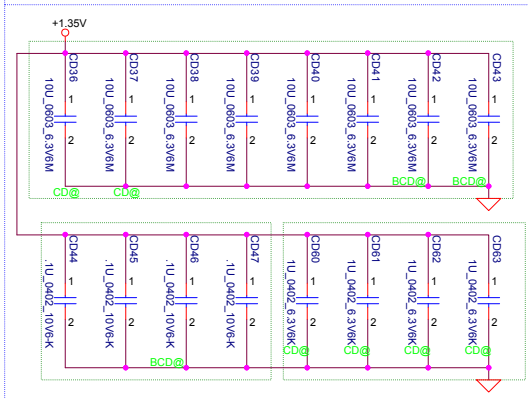
Swap Table



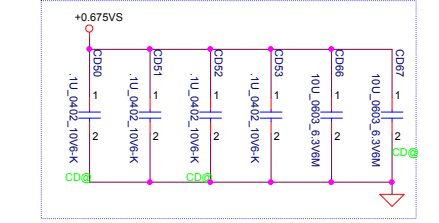
Pin Number	Pin Name	Net Name
5	DQ0	DDR_B_DQ17
7	DQ1	DDR_B_DQ23
15	DQ2	DDR_B_DQ18
17	DQ3	DDR_B_DQ21
4	DQ4	DDR_B_DQ16
6	DQ5	DDR_B_DQ22
16	DQ6	DDR_B_DQ19
18	DQ7	DDR_B_DQ20
10	DQS#0	DDR_B_DQS#2
12	DQS#0	DDR_B_DQS#2
21	DQ8	DDR_B_DQ3
23	DQ9	DDR_B_DQ5
33	DQ10	DDR_B_DQ6
35	DQ11	DDR_B_DQ1
22	DQ12	DDR_B_DQ2
24	DQ13	DDR_B_DQ4
34	DQ14	DDR_B_DQ0
36	DQ15	DDR_B_DQ7
27	DQS#1	DDR_B_DQS#0
29	DQS#1	DDR_B_DQS#0
39	DQ16	DDR_B_DQ8
41	DQ17	DDR_B_DQ10
51	DQ18	DDR_B_DQ14
53	DQ19	DDR_B_DQ15
40	DQ20	DDR_B_DQ13
42	DQ21	DDR_B_DQ12
50	DQ22	DDR_B_DQ9
52	DQ23	DDR_B_DQ11
45	DQS#2	DDR_B_DQS#1
47	DQS#2	DDR_B_DQS#1
57	DQ24	DDR_B_DQ27
59	DQ25	DDR_B_DQ26
67	DQ26	DDR_B_DQ28
69	DQ27	DDR_B_DQ24
56	DQ28	DDR_B_DQ31
58	DQ29	DDR_B_DQ30
68	DQ30	DDR_B_DQ29
70	DQ31	DDR_B_DQ25
62	DQS#3	DDR_B_DQS#3
64	DQS#3	DDR_B_DQS#3
129	DQ32	DDR_B_DQ33
131	DQ33	DDR_B_DQ36
141	DQ34	DDR_B_DQ39
143	DQ35	DDR_B_DQ38
130	DQ36	DDR_B_DQ37
132	DQ37	DDR_B_DQ32
140	DQ38	DDR_B_DQ35
142	DQ39	DDR_B_DQ34
135	DQS#4	DDR_B_DQS#4
137	DQS#4	DDR_B_DQS#4
147	DQ40	DDR_B_DQ40
149	DQ41	DDR_B_DQ43
157	DQ42	DDR_B_DQ42
159	DQ43	DDR_B_DQ44
146	DQ44	DDR_B_DQ45
148	DQ45	DDR_B_DQ41
158	DQ46	DDR_B_DQ46
160	DQ47	DDR_B_DQ47
152	DQS#5	DDR_B_DQS#5
154	DQS#5	DDR_B_DQS#5
163	DQ48	DDR_B_DQ52
165	DQ49	DDR_B_DQ51
175	DQ50	DDR_B_DQ50
177	DQ51	DDR_B_DQ48
164	DQ52	DDR_B_DQ49
166	DQ53	DDR_B_DQ53
174	DQ54	DDR_B_DQ54
176	DQ55	DDR_B_DQ55
169	DQS#6	DDR_B_DQS#6
171	DQS#6	DDR_B_DQS#6
181	DQ56	DDR_B_DQ62
183	DQ57	DDR_B_DQ57
191	DQ58	DDR_B_DQ59
193	DQ59	DDR_B_DQ63
180	DQ60	DDR_B_DQ56
182	DQ61	DDR_B_DQ61
192	DQ62	DDR_B_DQ58
194	DQ63	DDR_B_DQ60
186	DQS#7	DDR_B_DQS#7
188	DQS#7	DDR_B_DQS#7

For RF

Layout Note: Place near DIMM
 (10uF_0603_6.3V)*8
 (1U_0402_6.3V)*8
 (.1U_0402_10V6-K)*4



Layout Note: Place near DIMM
 (10U_0603_6.3V)*2
 (.1U_0402_10V)*4


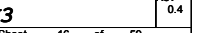


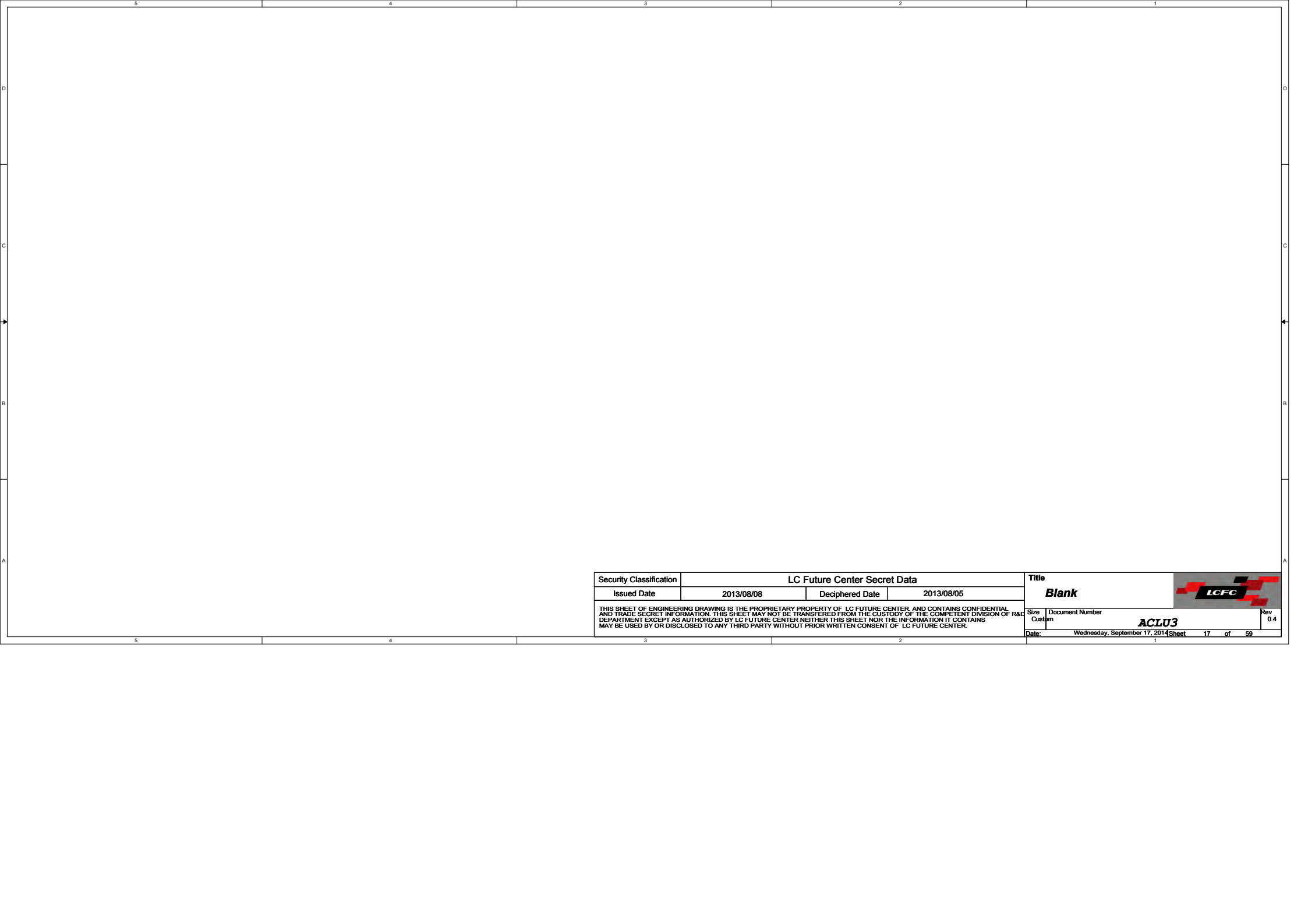
For RF


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Title	DDR3 SO-DIMM B	
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5	4	3	2	1
A	B	C	D	A

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				Custom	0.4
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Power-Up/Down Sequence

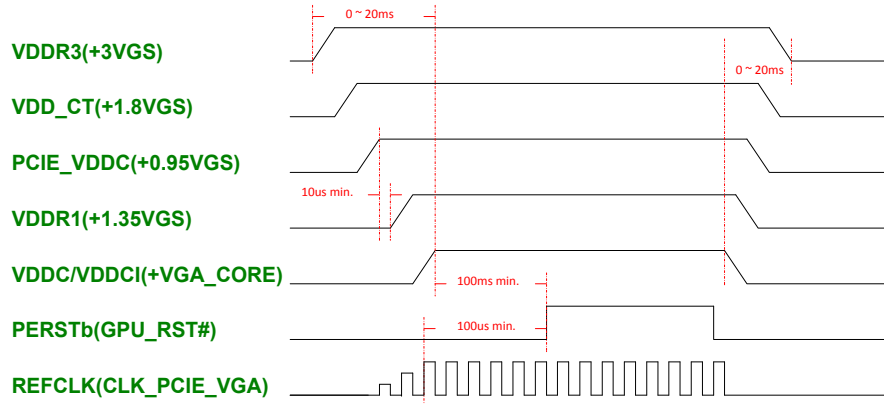
"Topaz" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μs.

It is recommended that the 3.3-V rail ramp up first. The 3.3-V, 1.8-V, and 0.95-V rails must reach their ready state at least 10 μs before VDDC, VDDCI, and VMEMIO start to ramp up.

The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as ≤ 50 mV/μs).

For power down, reversing the ramp-up sequence is recommended.




CONFIGURATION STRAPS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1= INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

MLPS Bit	Strap Name	Description	RECOMMENDED SETTINGS
PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	Define the ROM type when STRAP_BIOS_ROM_EN = 1. Define the primary memory-aperture size when STRAP_BIOS_ROM_EN = 0. 100 = 256MB	X
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	AUD_PORT_CONN_PINSTRAP[0]	The LSB (least significant bit) of the strap option that indicates the number of audio-capable display outputs.	1
PS_1[1]	STRAP_BIF_GEN3_EN_A	1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported. 0= Not support	X
PS_1[2]	STRAP_BIF_CLK_PM_EN	0 = The CLKREQB power management capability is disabled 1 = The CLKREQB power management capability is enabled	0
PS_1[3]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	0 = The transmitter half-swing is enabled 1 = The transmitter full-swing is enabled	1
PS_1[5]	STRAP_TX_DEEMPH_EN	0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled. 1= Enable	X
PS_2[1]	N/A	Reserved.	0
PS_2[2]	N/A	Reserved.	0
PS_2[3]	STRAP_BIOS_ROM_EN	0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device. 0= Disable	X
PS_2[4]	STRAP_BIF_VGA_DIS	0 = VGA controller capacity enabled. 1 = The device will not be recognized as the system's VGA controller.	1
PS_2[5]	N/A	Reserved	1
PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	Board configuration related strapping, such as for memory ID 000 = Hynix 256M*16 001 = Hynix 128M*16 100 = Samsung 256M*16 011 = Samsung 128M*16 010 = Micron 256M*16 111 = Micron 128M*16	X
PS_3[4] PS_3[5]	AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[2]	Determines the maximum number of digital display audio endpoints that will be presented to the OS and user.(Combine with PS_0[5]) 111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable.	11

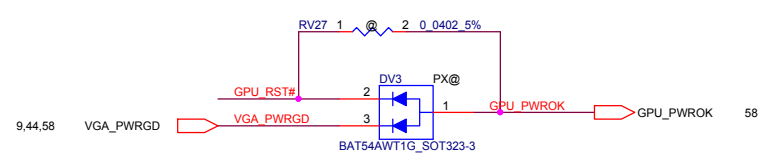
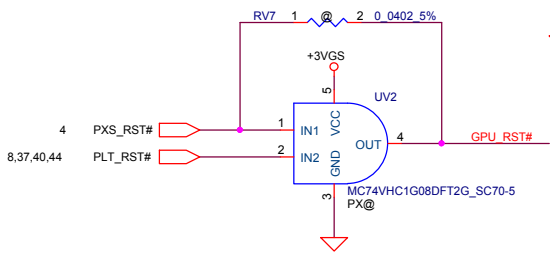
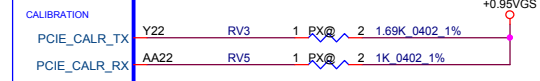
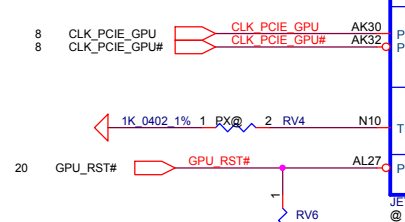
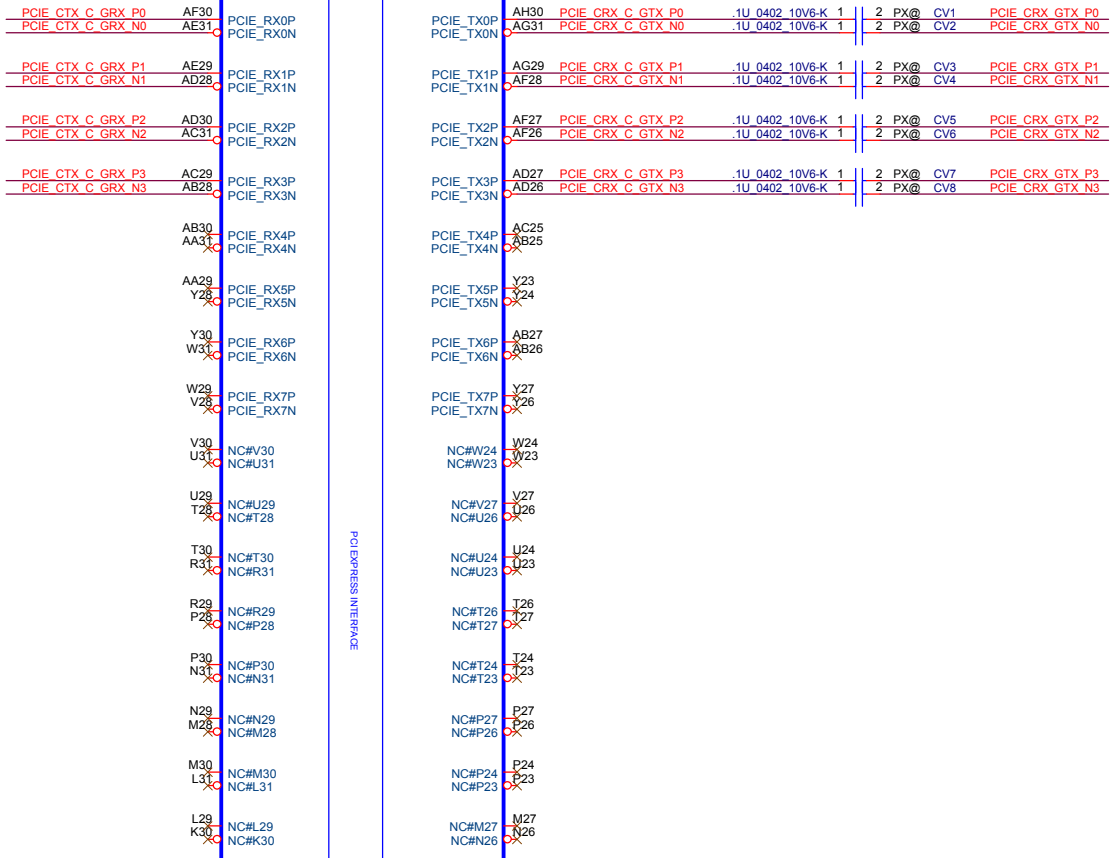
VRAM ID config

Memory Type		VRAM ID PS_3[3:1]	PU resistor RV33	PD resistor RV36
128Mx16	Hynix H5TC2G63FFR-11C	100	4.53K	4.99K
	Micron MT41J128M16JT-093G	111	4.75K	NC
	Samsung K4W2G1646Q-BC1A	110	3.4K	10K
256Mx16	Hynix H5TC4G63AFR-11C	000	NC	4.75K
	Micron MT41J256M16HA-093G	010	4.53K	2K
	Samsung K4W4G1646D-BC1A	001	8.45K	2K
	Micron MT41K256M16HA-107G	011	6.98K	4.99K

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Date: Wednesday, September 17, 2014				Rev 0.4 Sheet 18 of 59

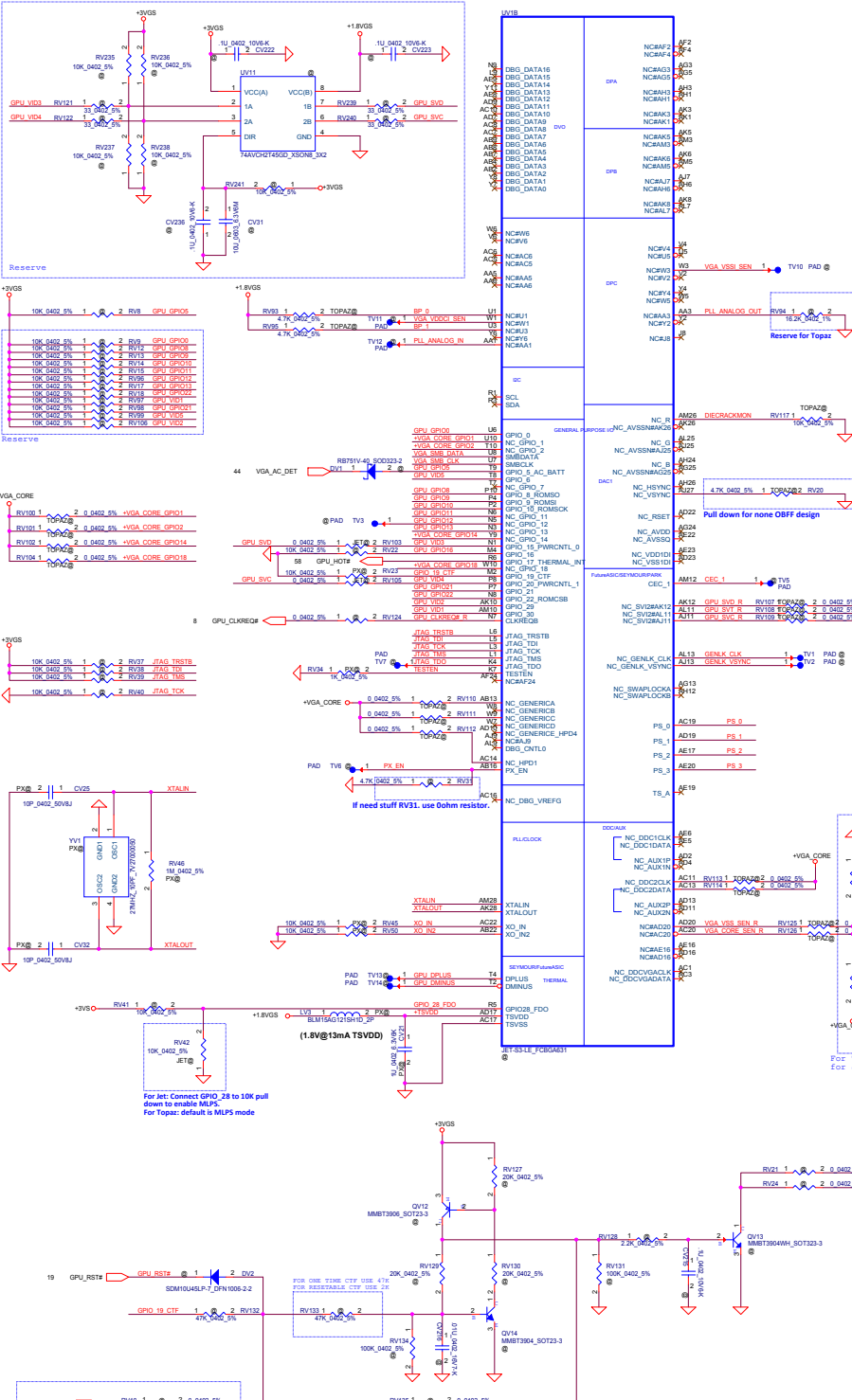
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 9 PCIE_CTX_C_GRX_N[3..0] PCIE_CTX_C_GRX_N[3..0]

PCIE_CRX_GTX_P[3..0] PCIE_CRX_GTX_P[3..0] 9
 PCIE_CRX_GTX_N[3..0] PCIE_CRX_GTX_N[3..0] 9



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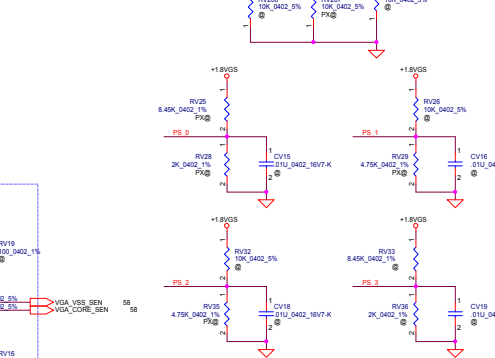
CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

MLPS Bit	Strap Name	Description	RECOMMENDED SETTINGS
PS_0[0]	NCM_CONFIG[0]	Define the ROM type when STRAP_BIOS_ROM_EN = 1	0 = Intel BIOS ROM, 1 = Micron BIOS ROM, 2 = 0
PS_0[1]	NCM_CONFIG[1]	Define the primary memory address base when STRAP_BIOS_ROM_EN = 0	100 = 256MB
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	AUD_PORT_CONN_PINSTRAP[0]	The LSB (least significant bit) of the strap option that indicates the number of auto-capable display outputs.	1
PS_1[0]	STRAP_BIF_GEN0_EN_A	1 = PCIe GEN3 is supported 0 = PCIe GEN3 is not supported.	On Not support X
PS_1[2]	STRAP_BIF_CLK_PM_LEN	0 = The CLKREQ power management capability is disabled 1 = The CLKREQ power management capability is enabled.	0
PS_1[3]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	STRAP_TX_CPD_DRV_FULL_SWING	0 = The transmitter full swing is enabled 1 = The transmitter full swing is disabled.	1
PS_1[5]	STRAP_TX_DEEMPH_LEN	0 = Tx deemphasis disabled 1 = Tx deemphasis enabled.	1 Enable X
PS_2[0]	N/A	Reserved.	0
PS_2[1]	N/A	Reserved.	0
PS_2[2]	STRAP_BIOS_ROM_EN	1 = Disable the external BIOS ROM device 0 = Enable the external BIOS ROM device.	On Disable X
PS_2[4]	STRAP_BIF_VGA_DIS	0 = VGA controller capacity enabled 1 = The device will not be recognized as the system's VGA controller.	1
PS_2[5]	N/A	Reserved.	1
PS_3[0]	BOARD_CONFIG[0]	Board configuration related strap, such as for memory ID	X
PS_3[1]	BOARD_CONFIG[1]	00 = Hynix 52M16 01 = Hynix 128M16	X
PS_3[2]	BOARD_CONFIG[2]	00 = Samsung 25M16 01 = Samsung 25M16 10 = Micron 25M16 11 = Micron 128M16	X
PS_3[4]	AUD_PORT_CONN_PINSTRAP[1]	Determines the maximum number of digital display auto endpoints that will be presented to the OS and user (constrain with PS_0[5])	11 = No usable endpoints. 10 = One usable endpoint. 01 = Two usable endpoints. 00 = Three usable endpoints. 00 = Four usable endpoints. 00 = Five usable endpoints. 00 = Six usable endpoints. 00 = All endpoints are usable.
PS_3[5]	AUD_PORT_CONN_PINSTRAP[2]		11 = No usable endpoints.

SVC SVD Output Voltage (V)

SVC	SVD	Output Voltage (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



Capacitor Value (nF) Bits [5:4]

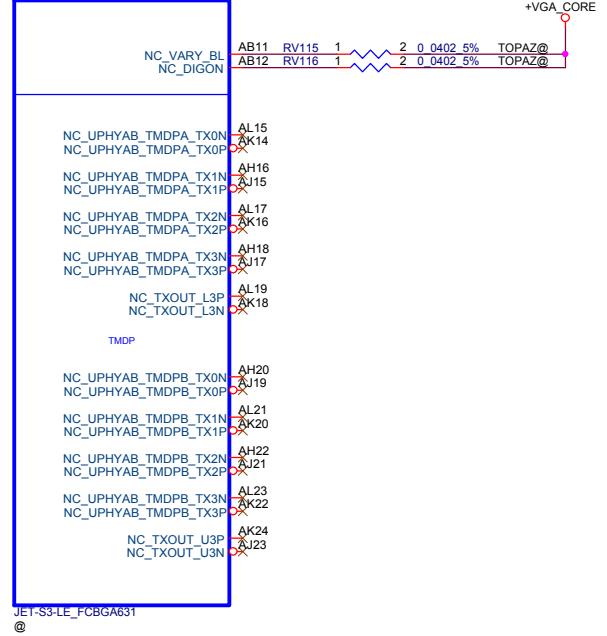
Capacitor Value (nF)	Bits [5:4]
680	00
82	01
10	10
NC	11

R_pu (Ω) R_pd (Ω) Bits [3:1]


R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4900	011
4530	4900	100
3240	5620	101
3400	10000	110
4750	NC	111

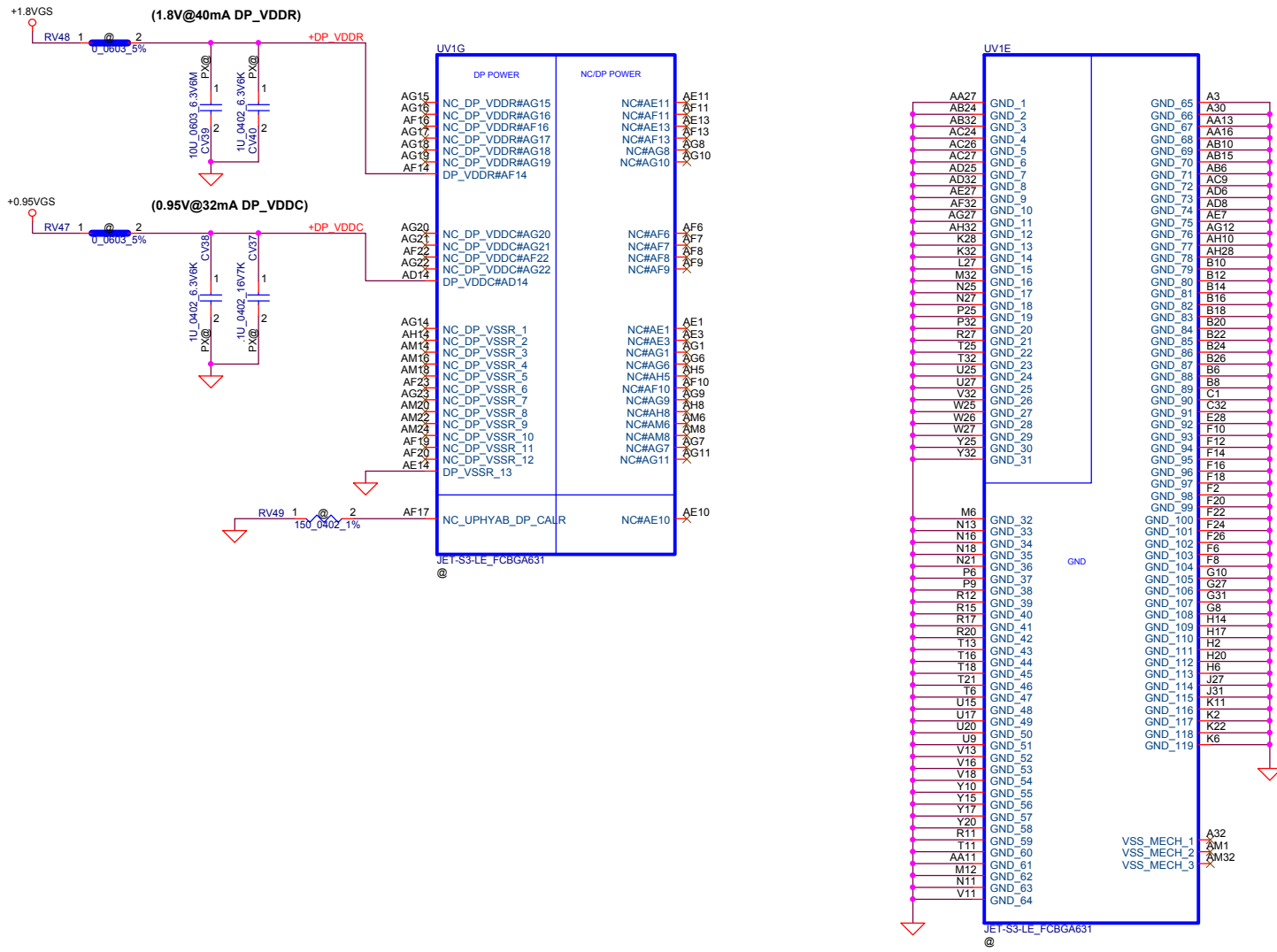
Note: 0402 1% resistors are required.

UV1F



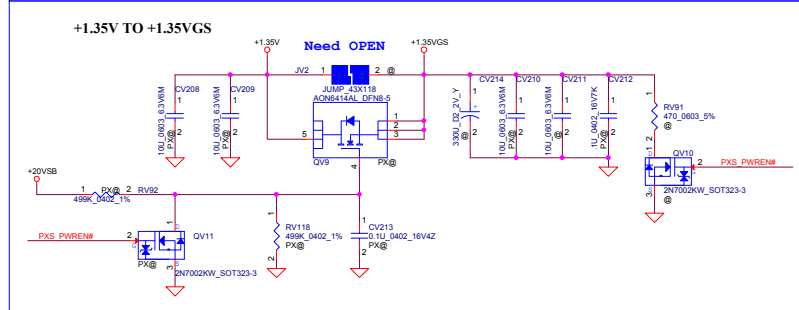
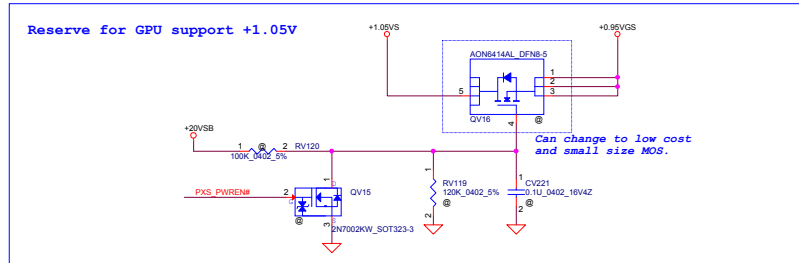
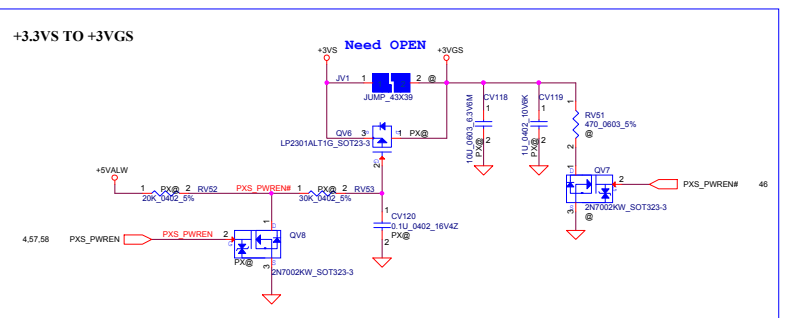
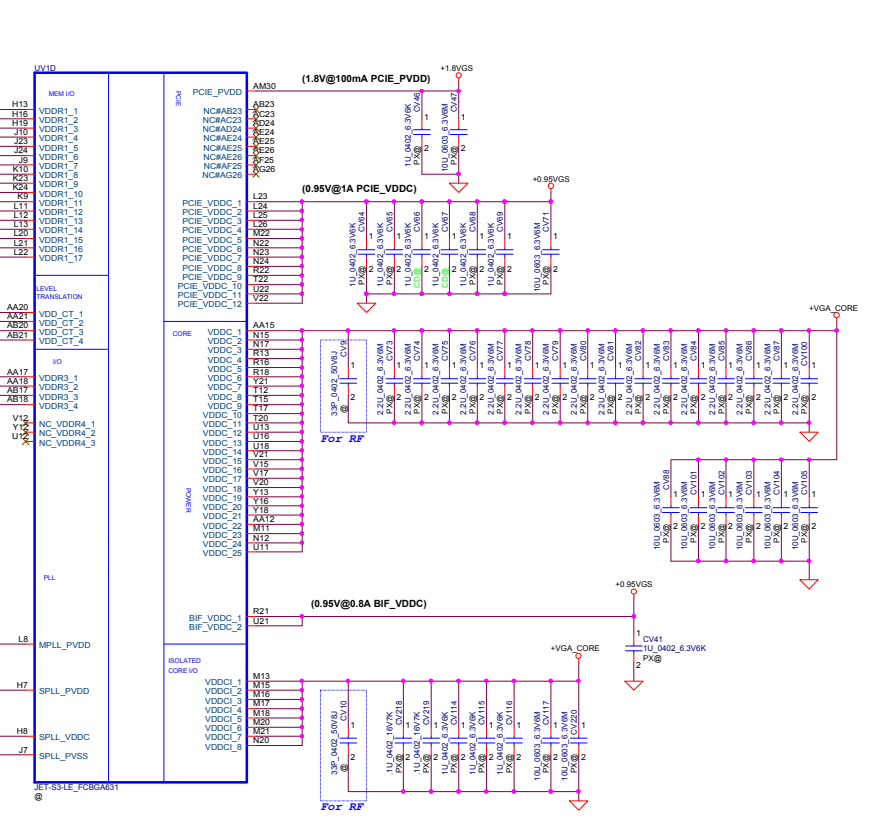
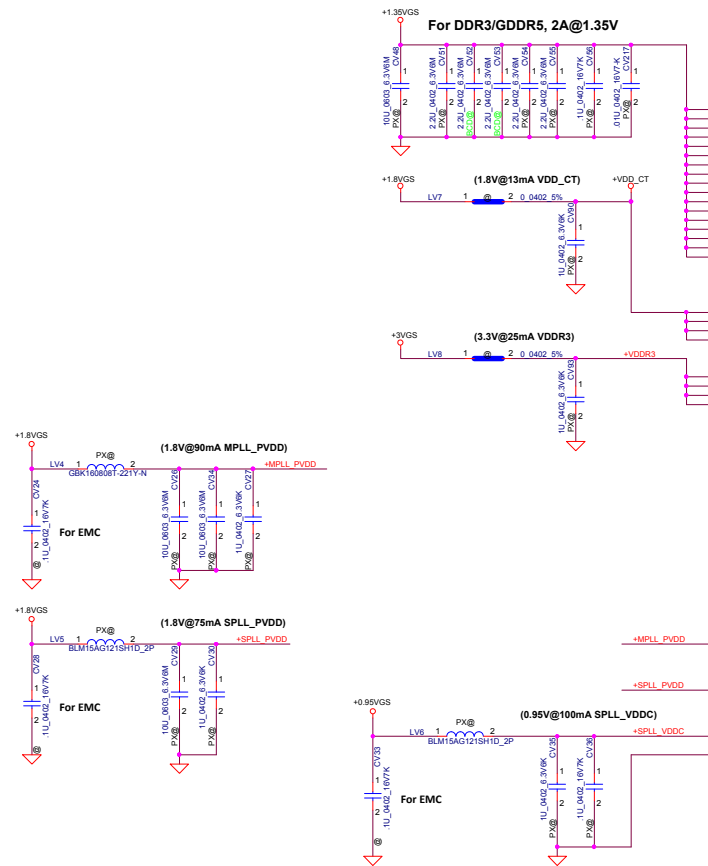
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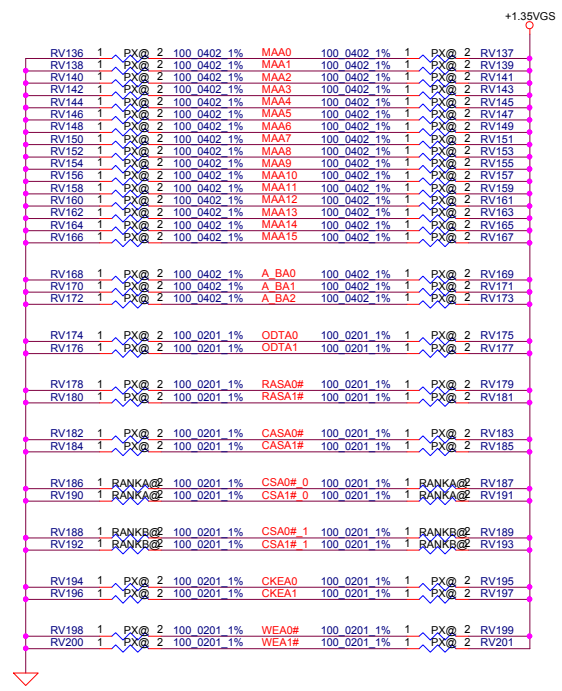
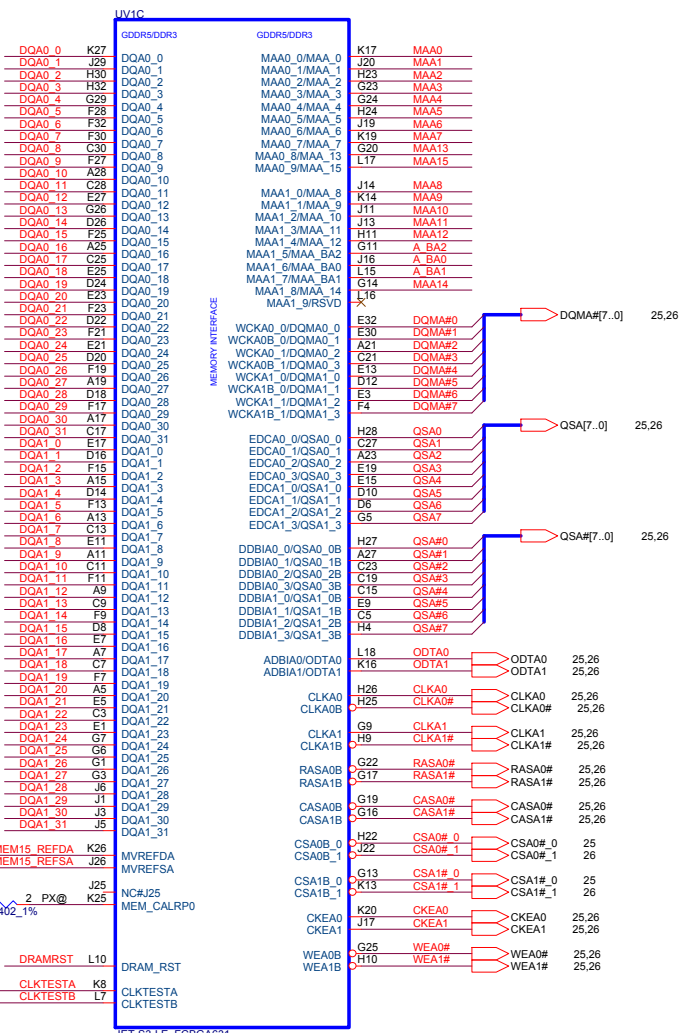
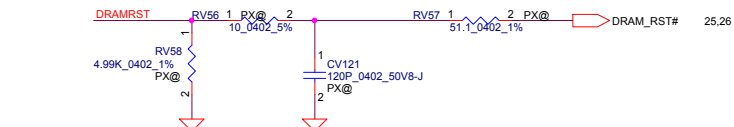
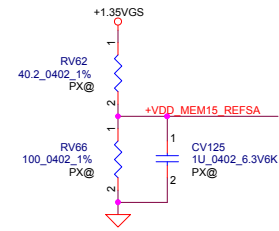
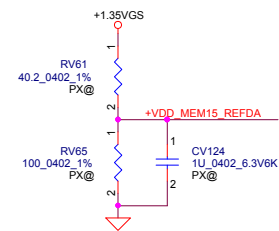
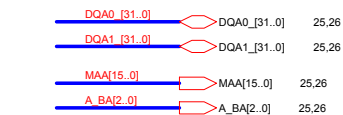
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ATI_JET-LE_TMDP		
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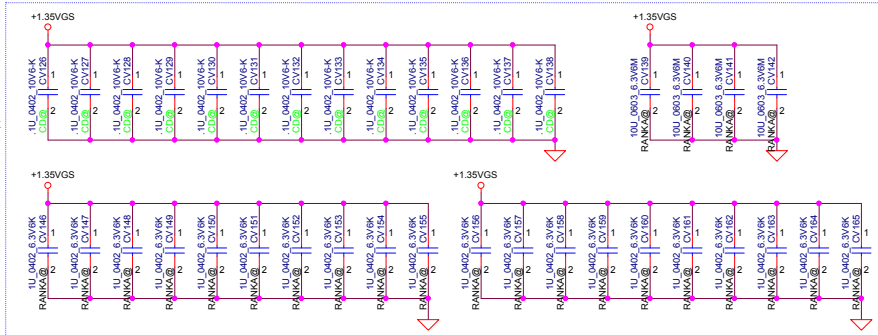
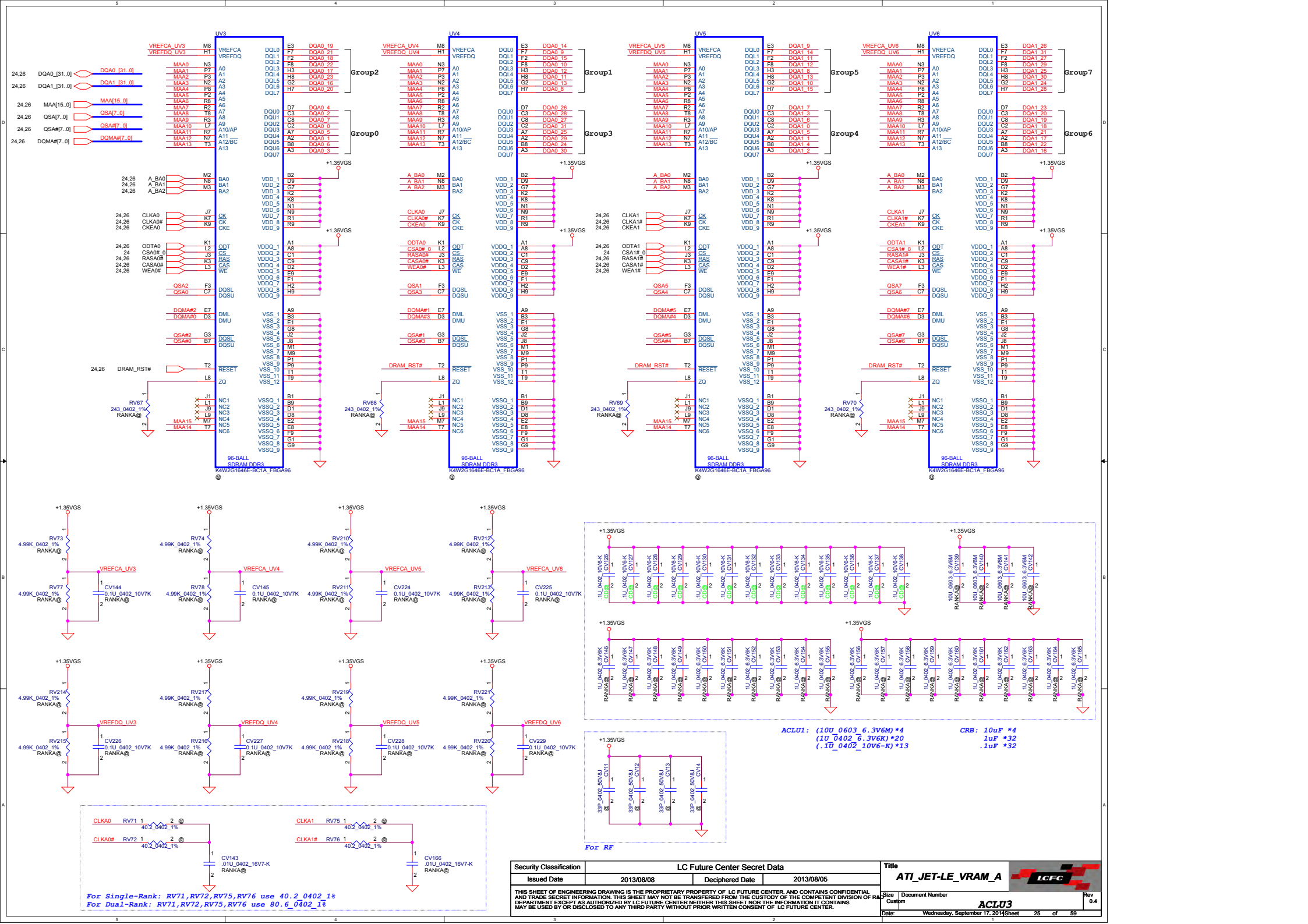
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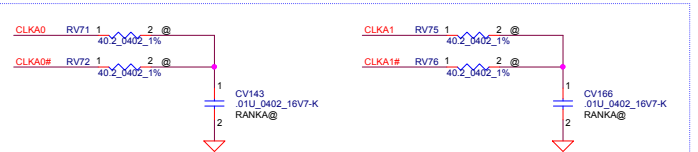
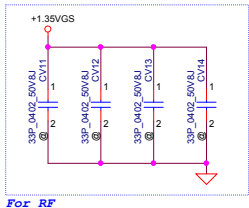


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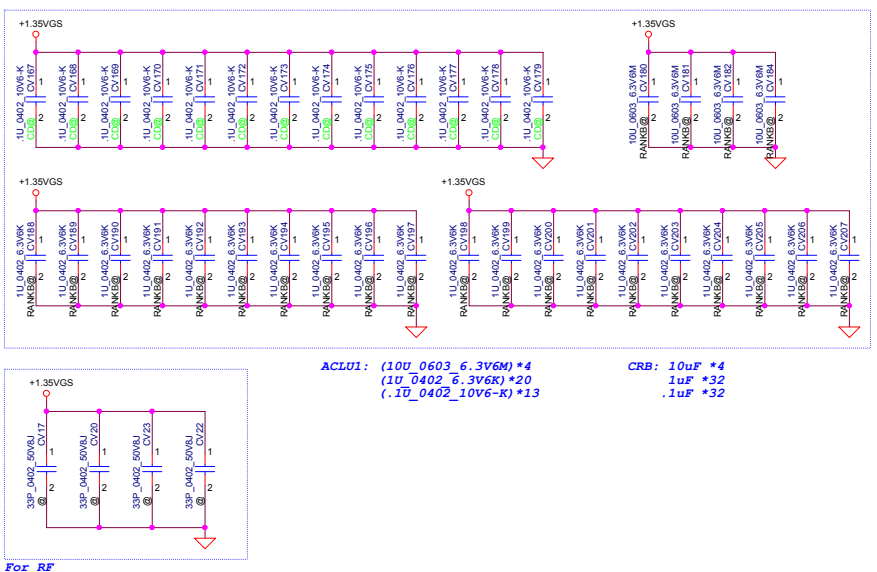
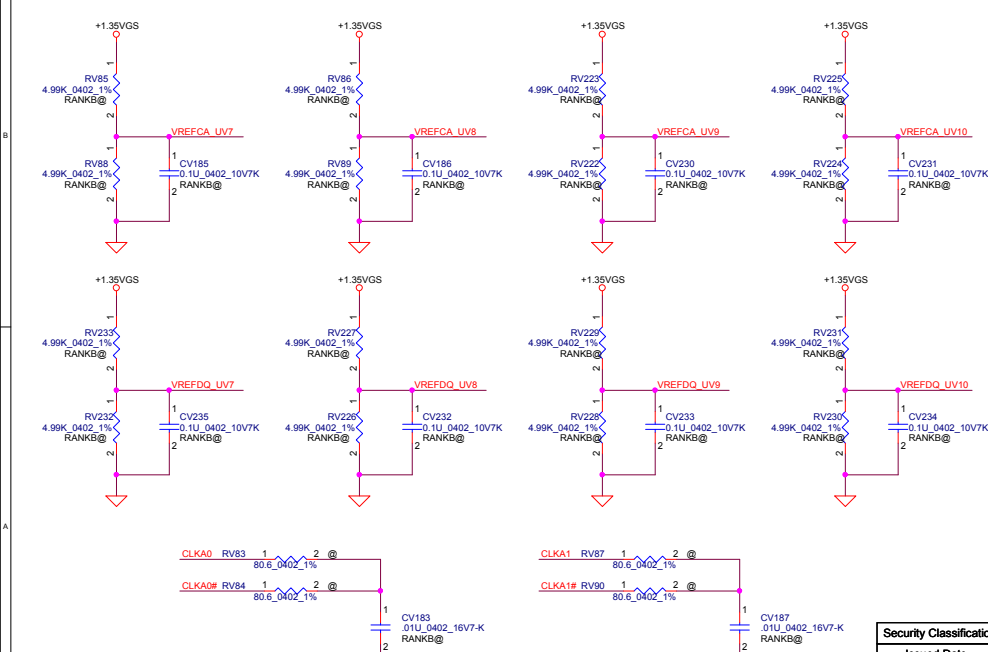
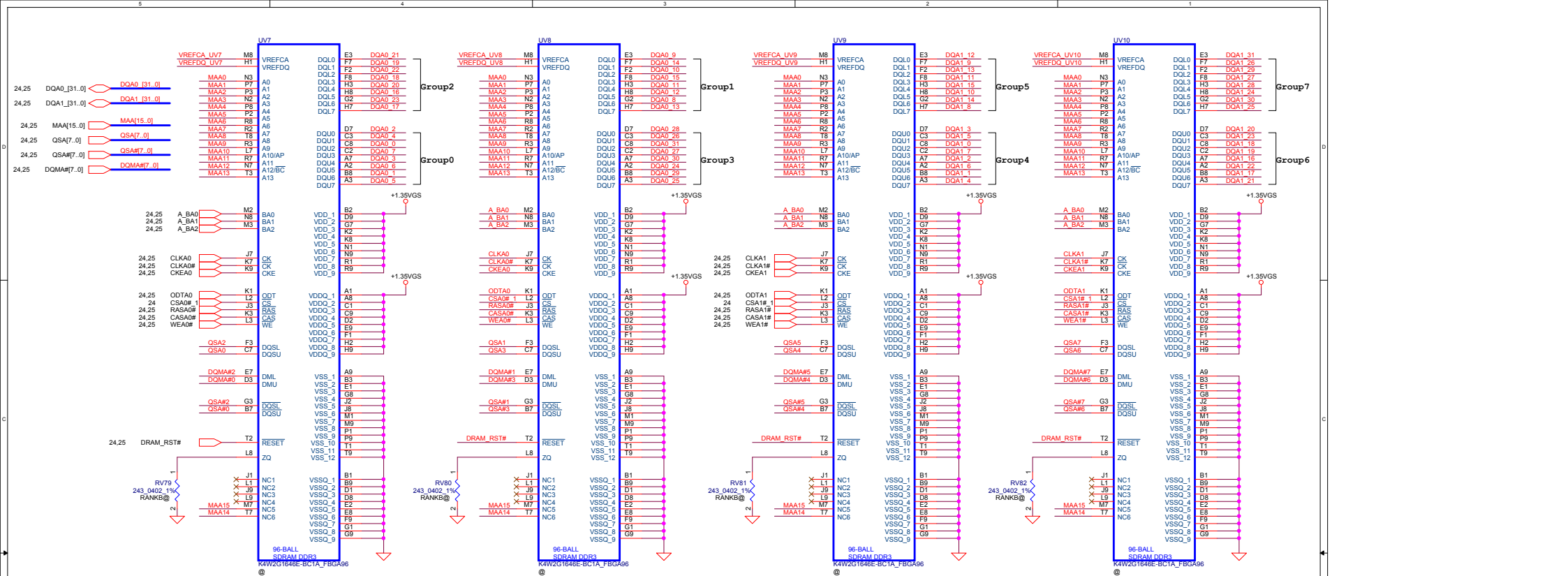
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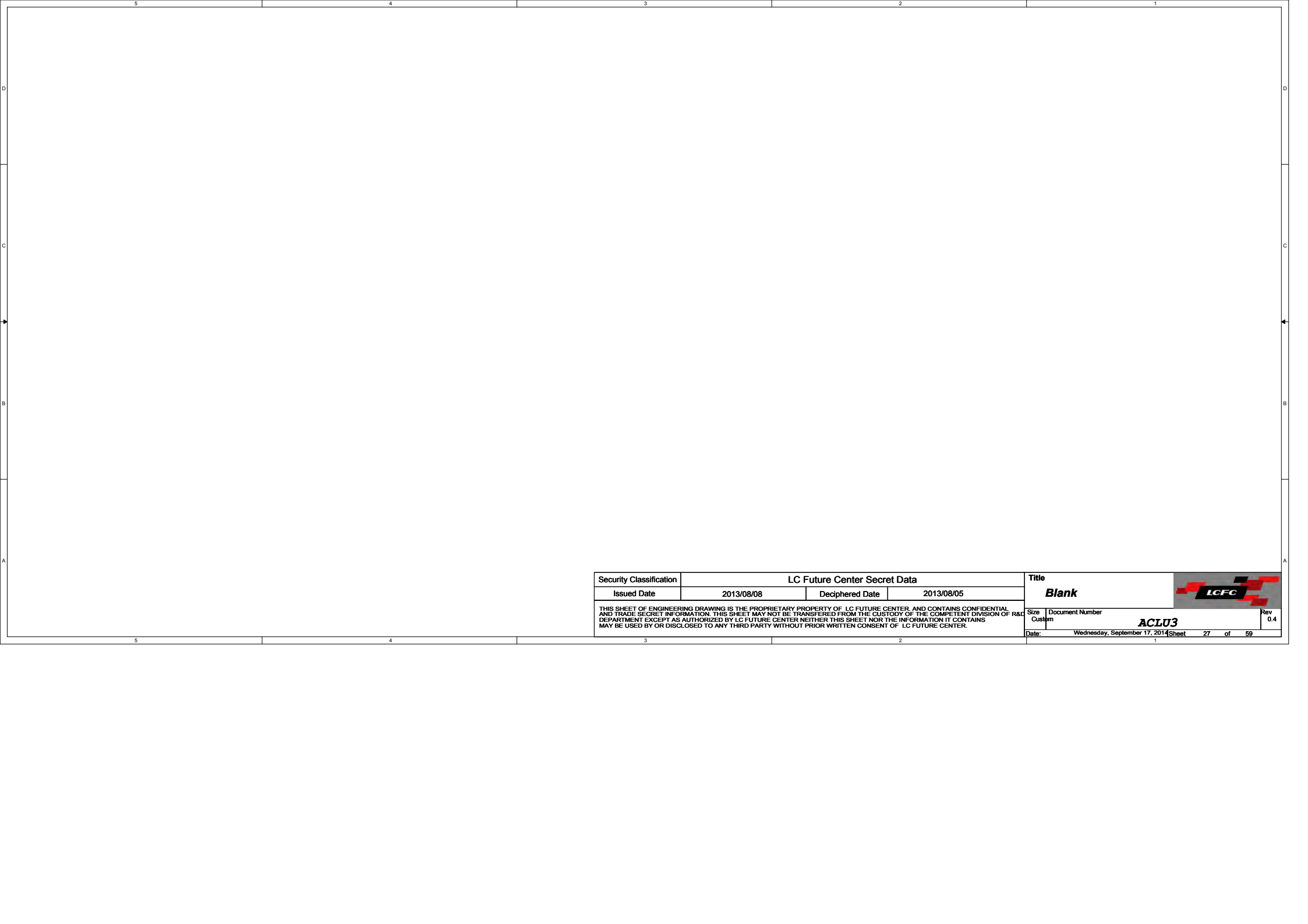



For Single-Rank: RV71, RV72, RV75, RV76 use 40.2 0402 1%
 For Dual-Rank: RV71, RV72, RV75, RV76 use 80.6 0402 1%

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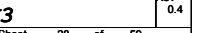


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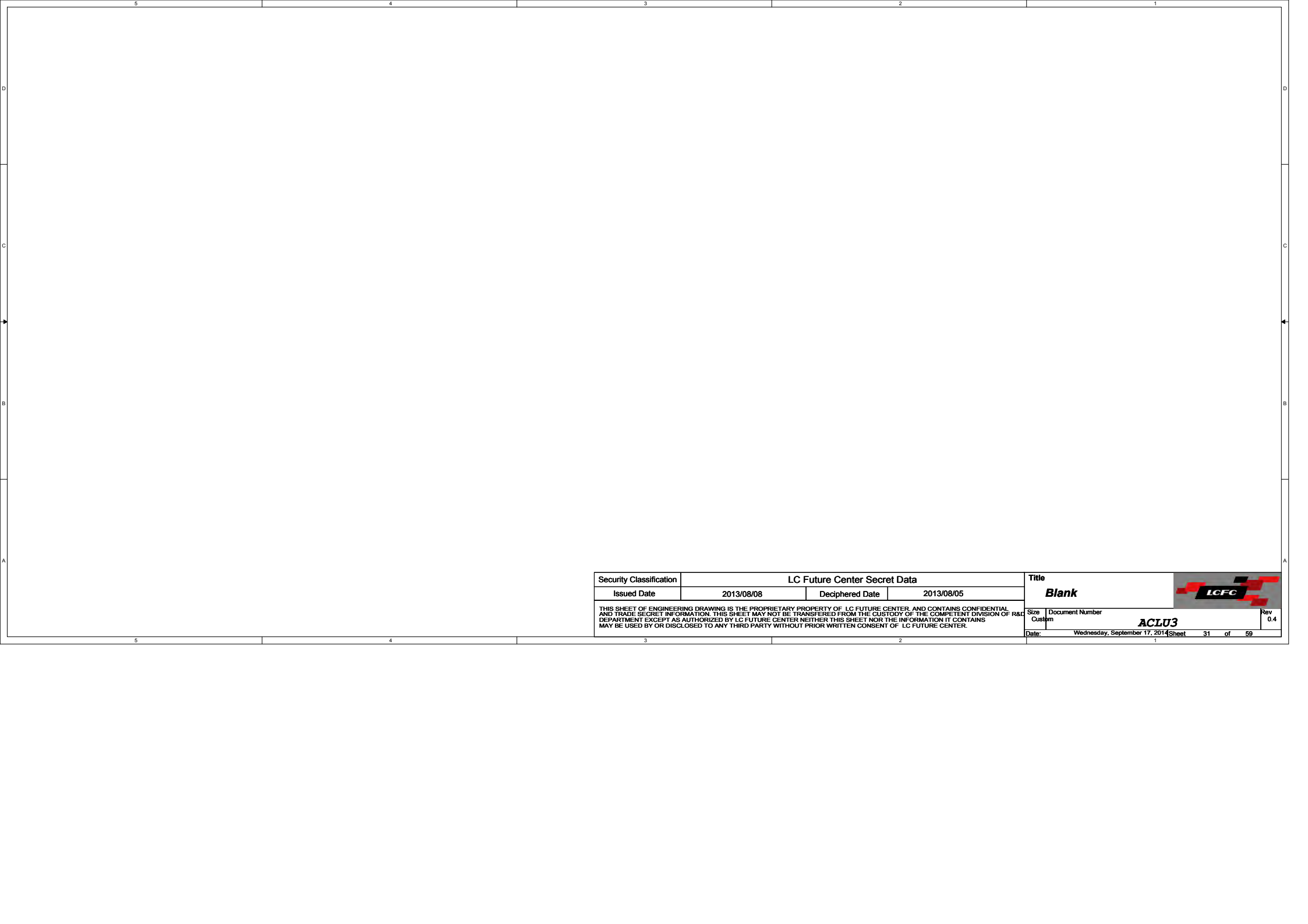
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Date:	Wednesday, September 17, 2014	Sheet	29	of	59											
Date:	Wednesday, September 17, 2014	Sheet	29	of	59											



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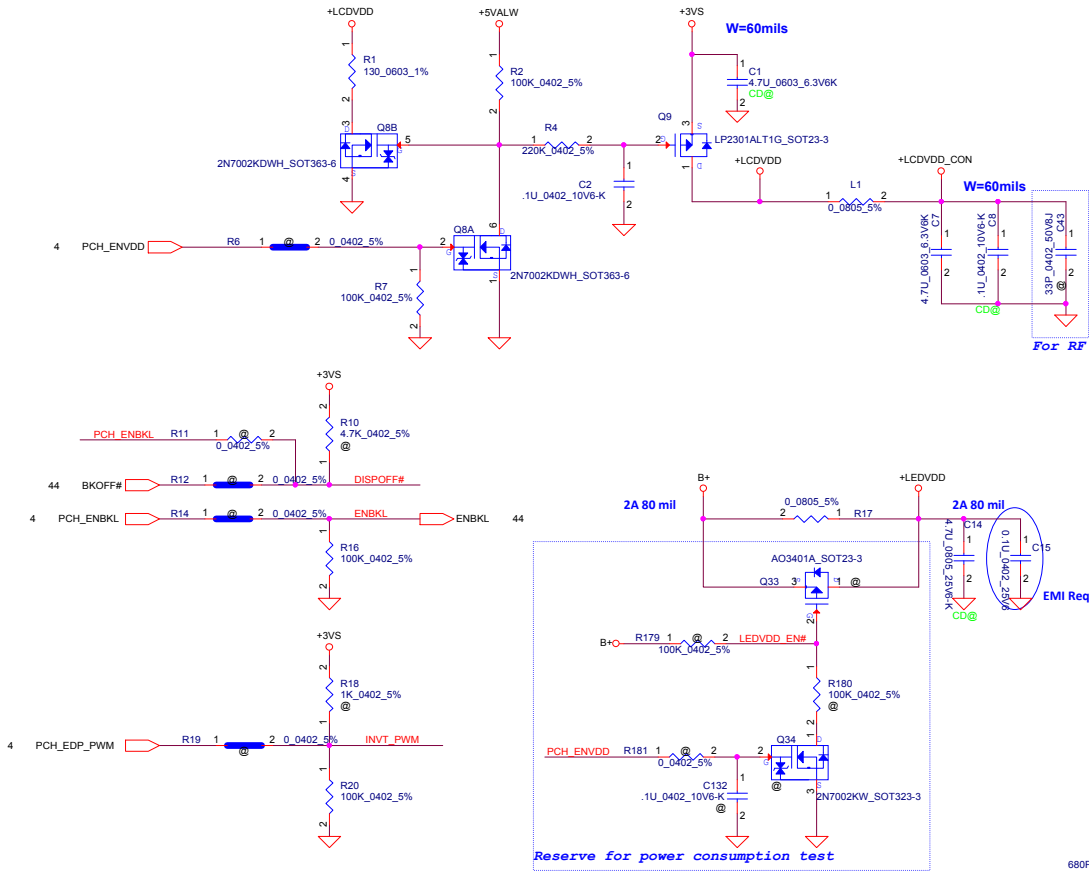


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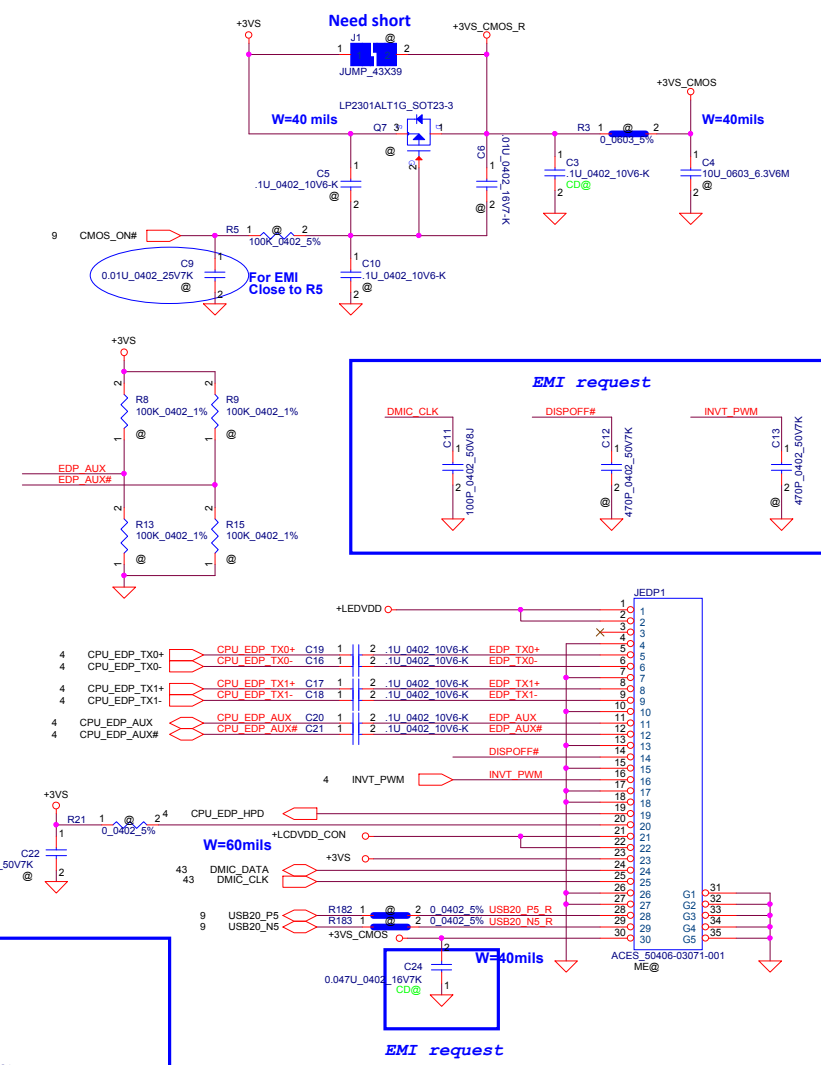
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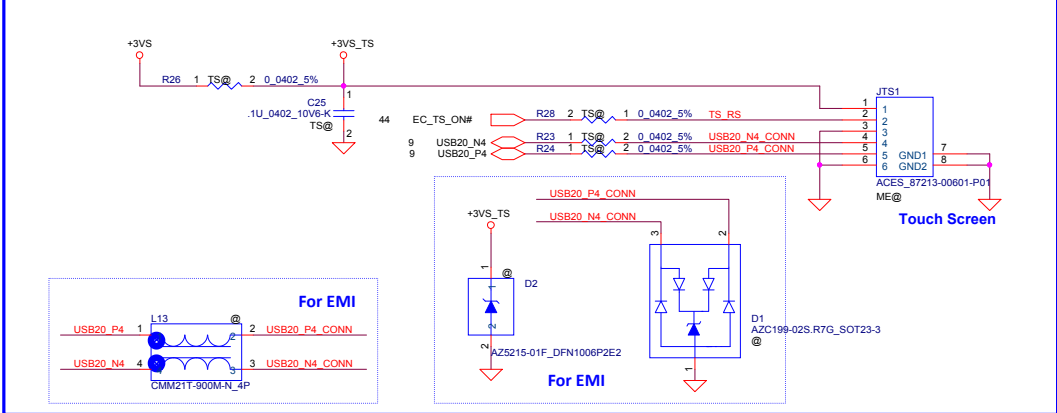
LCD POWER CIRCUIT



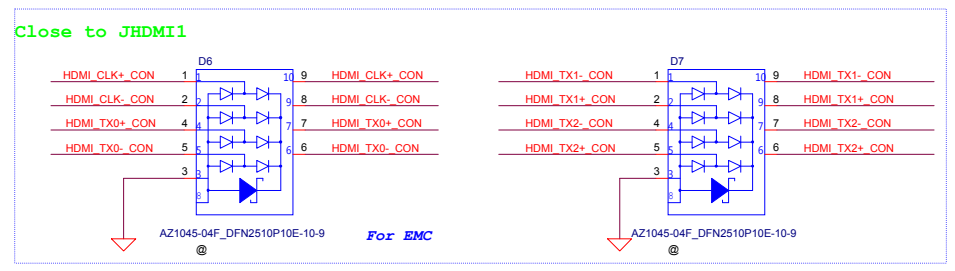
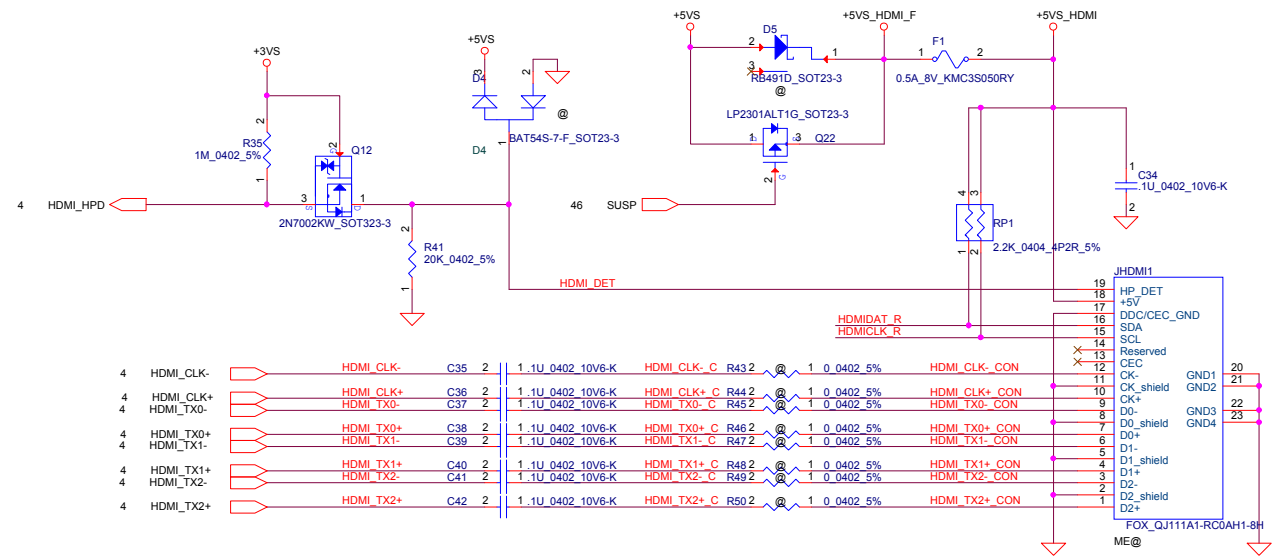
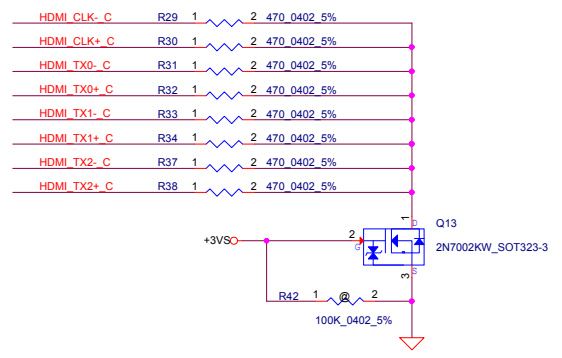
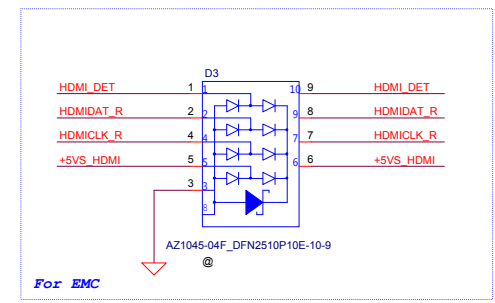
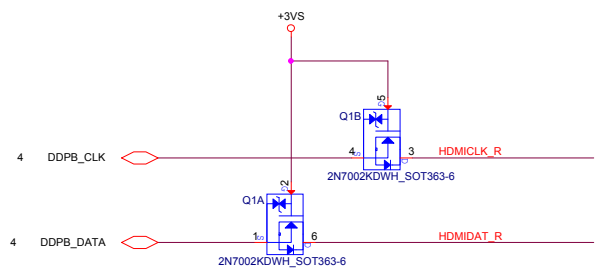
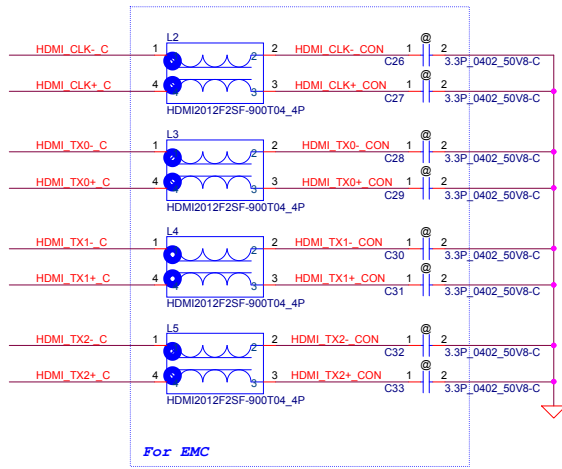
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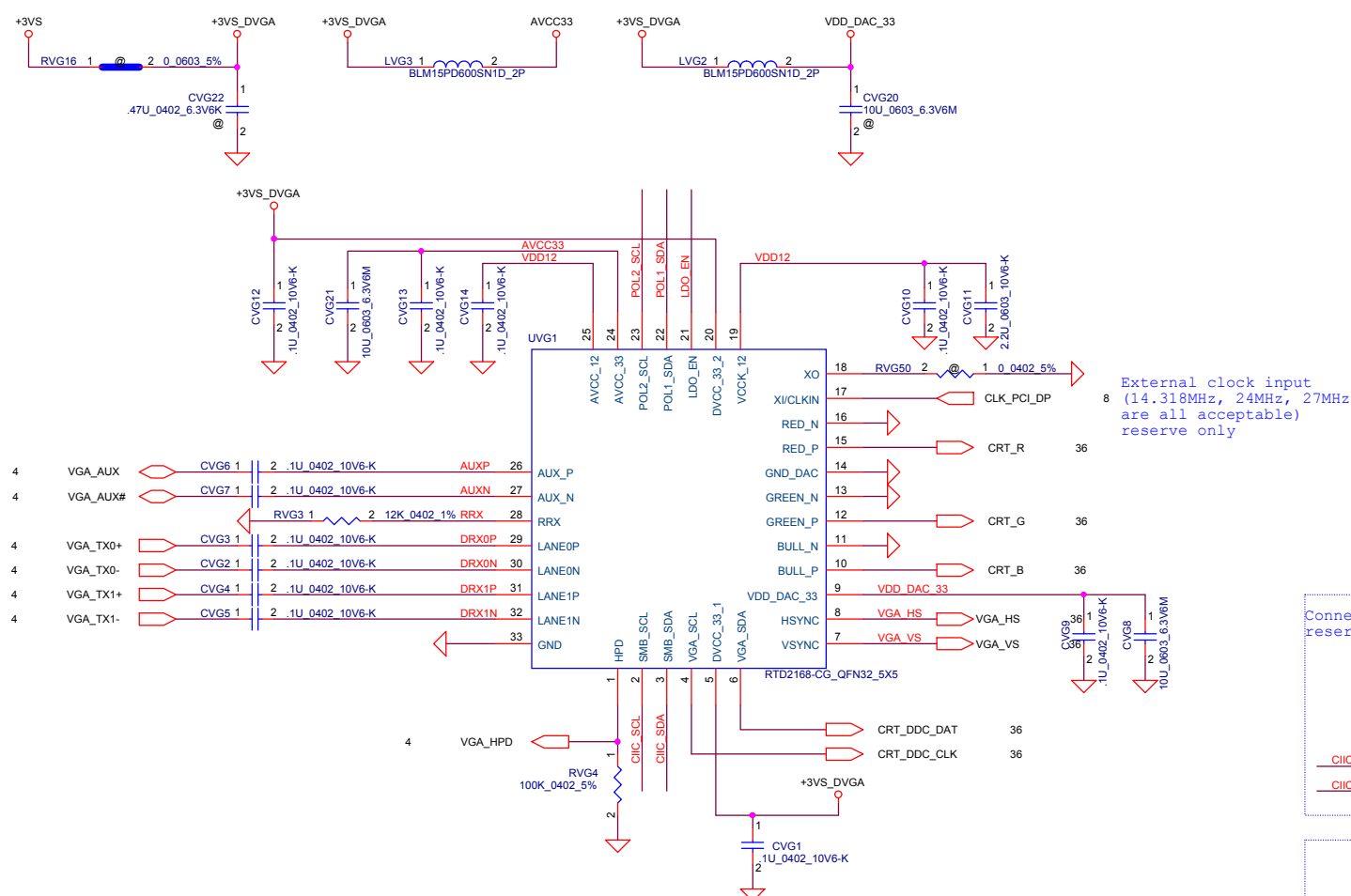
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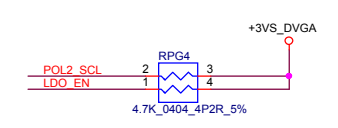
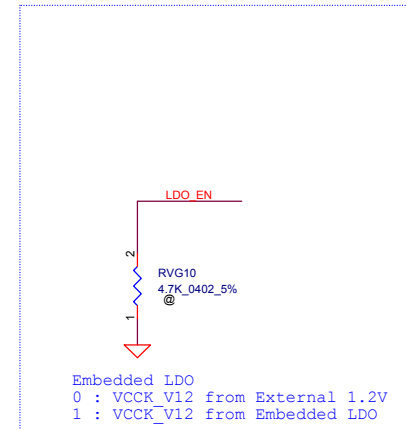
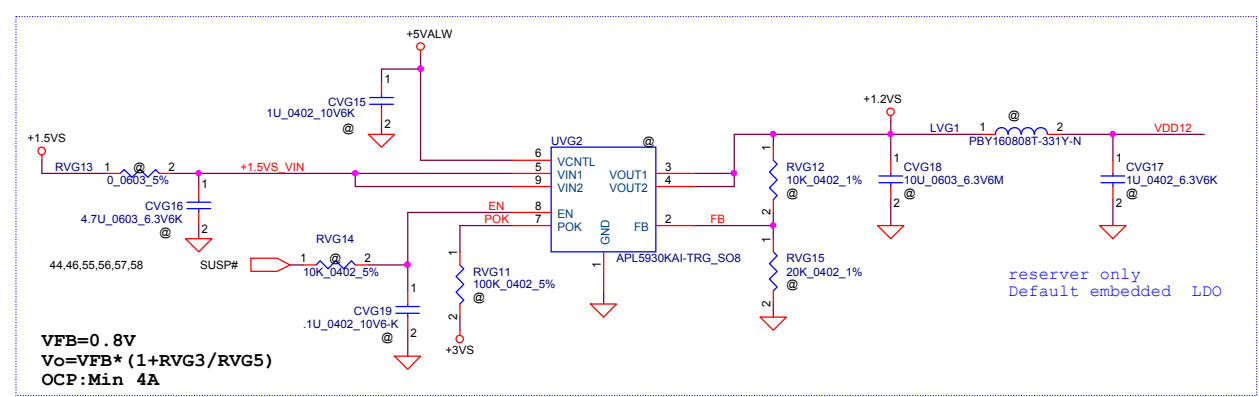
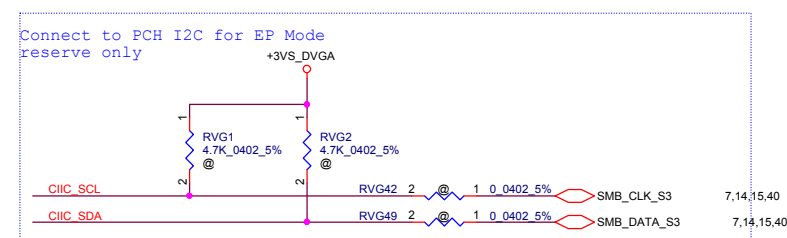
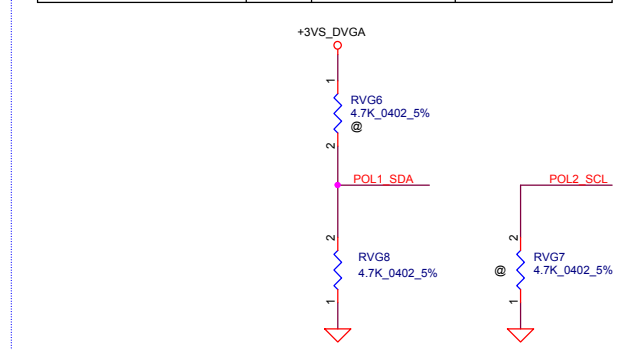
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2013/08/08	Deciphered Date	2013/08/05	eDP/ CMOS/Touch screen	
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Size	Document Number	Rev		0.4	
Custom	ACLU3	Date:		Wednesday, September 17, 2014 Sheet 33 of 59	



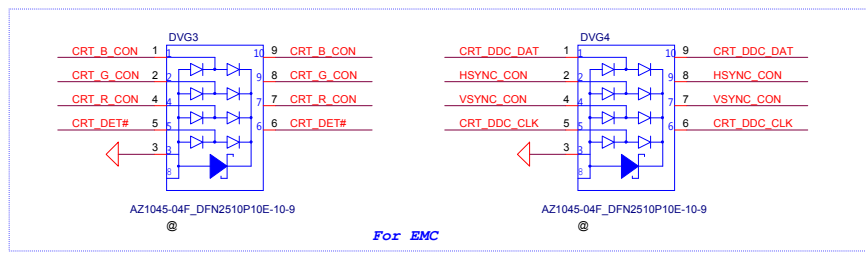
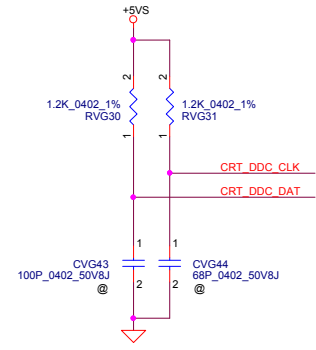
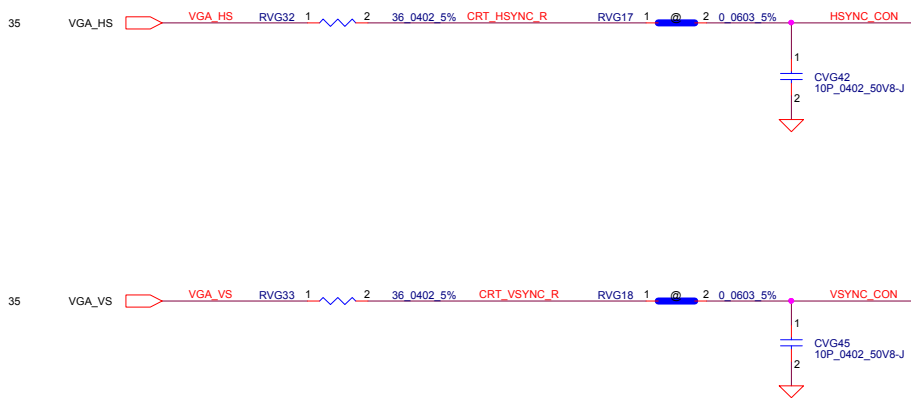
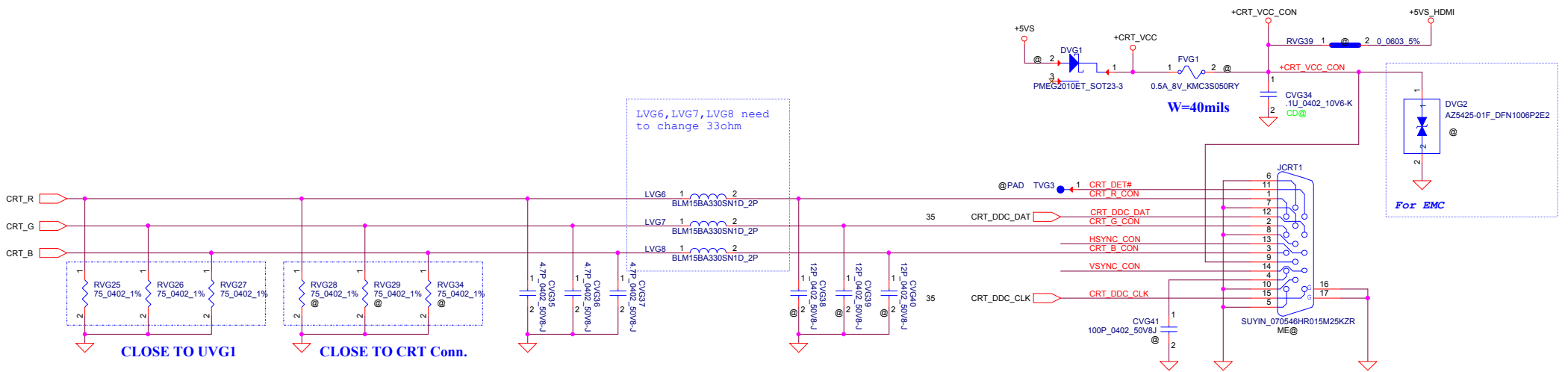
Security Classification	LC Future Center Secret Data		Title
Issued Date	2013/08/08	Deciphered Date	2013/08/05
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Date:	Wednesday, September 17, 2014	Sheet	34 of 59



		POL1_SDA (PIN22)	
		0	1
POL2_SCL (PIN23)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

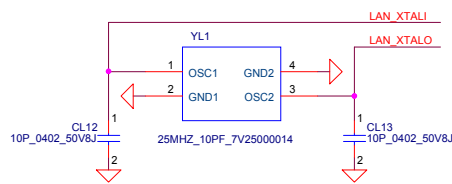
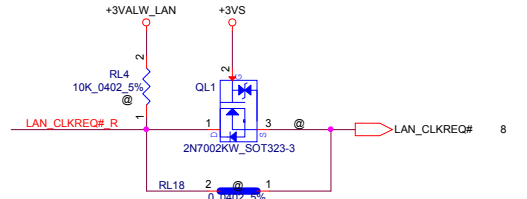
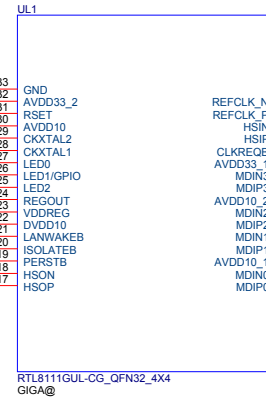
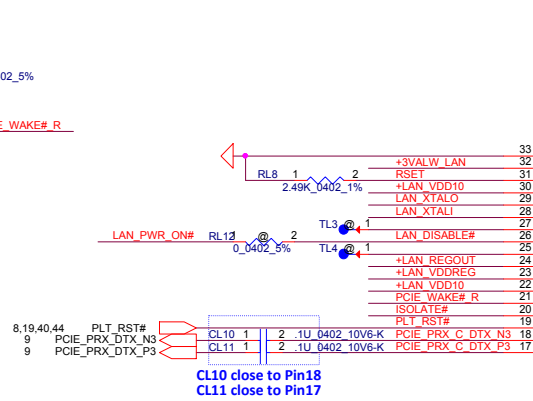
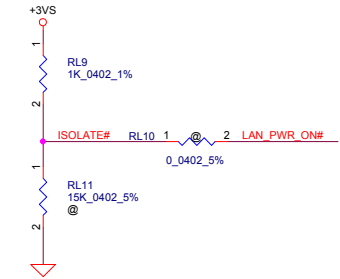
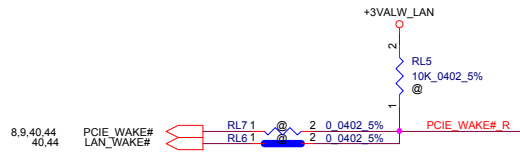
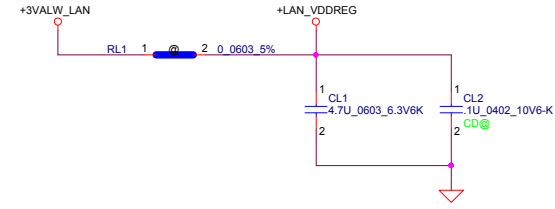
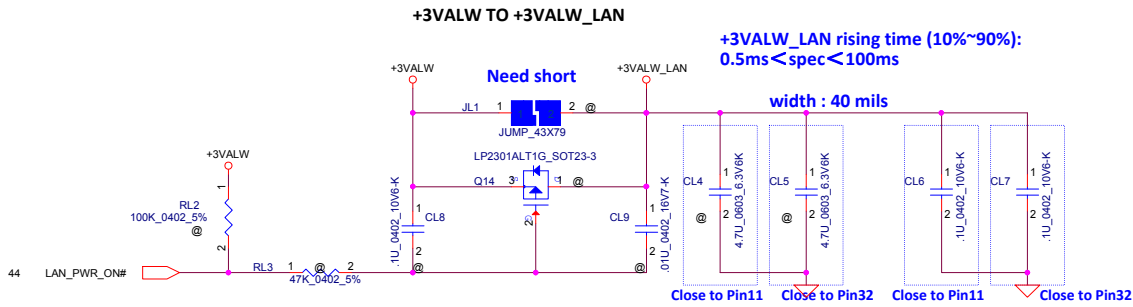


CRT Connector

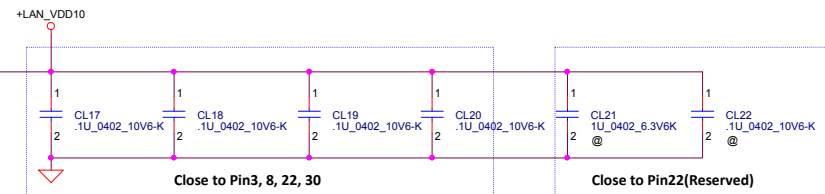
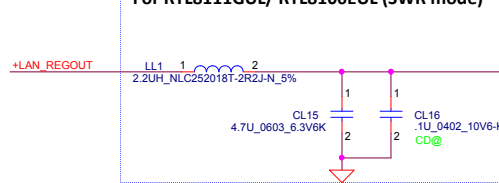


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Issued Date	2013/08/08	Deciphered Date	2013/08/05
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CRT	ACL03	0.4
Date:	Wednesday, September 17, 2014	Sheet 36 of 59



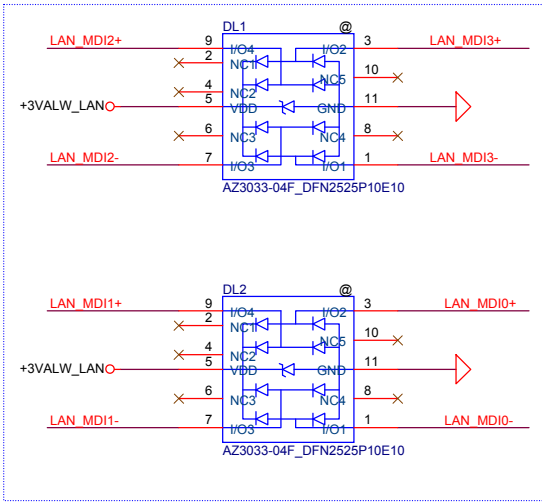
For RTL8111GUL/RTL8106EUL (SWR mode)



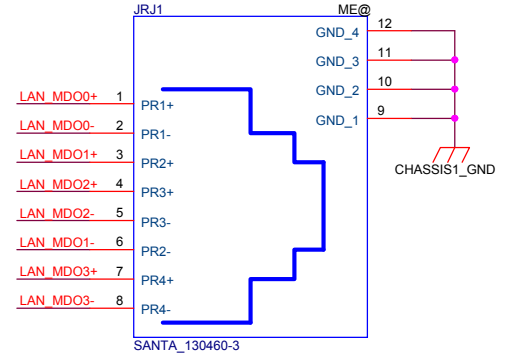
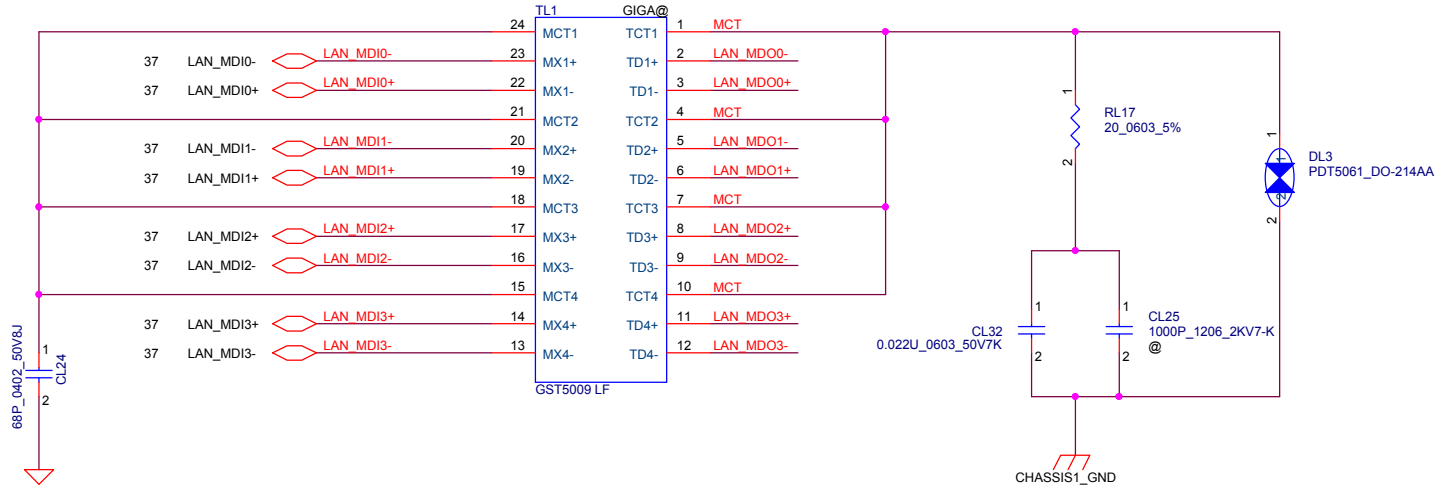
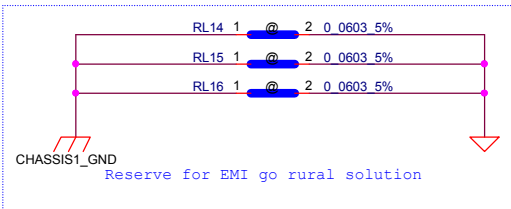
Layout Note: LL1 must be within 200mil to Pin24.
CL15, CL16 must be within 200mil to LL1
+LAN_REGOUT: Width =60mil


Security Classification	LC Future Center Secret Data		Title	LAN_RTL8111GUL/RTL8106E
Issued Date	2013/08/08	Deciphered Date	2013/08/05	
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Size Custom	Document Number	ACLU3		Rev 0.4
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DL1/DL2
1'S PN:SC300003M00

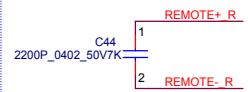


Place Close to TL1

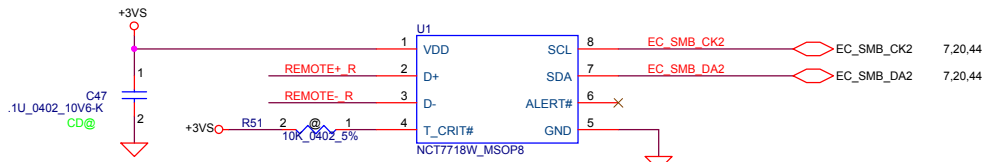


Security Classification	LC Future Center Secret Data			Title	 LAN_Transformer
Issued Date	2013/08/08	Deciphered Date	2013/08/05	Document Number	
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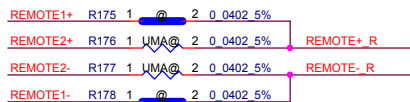
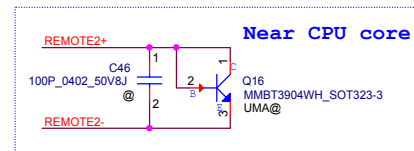
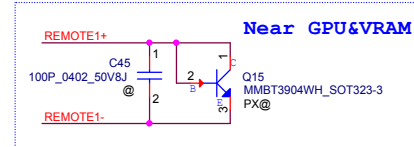
Close to U1



SMSC thermal sensor placed near DIMM

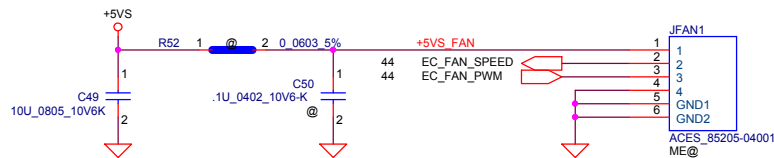



Address 1001_100xb



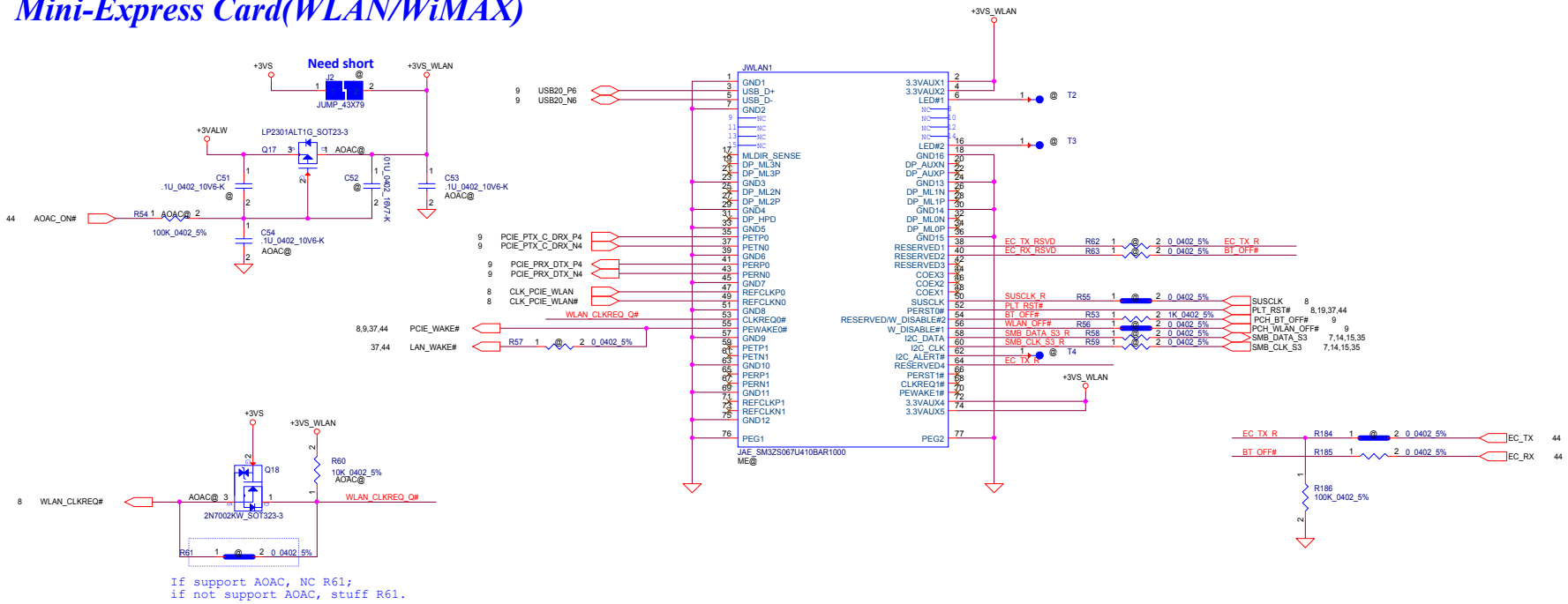
REMOTE+/- R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

FAN Conn

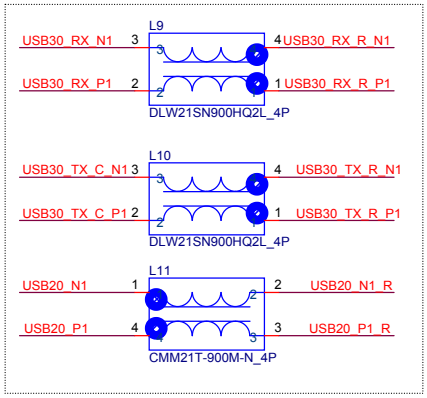
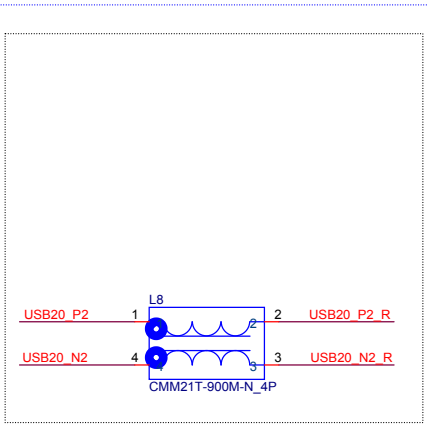
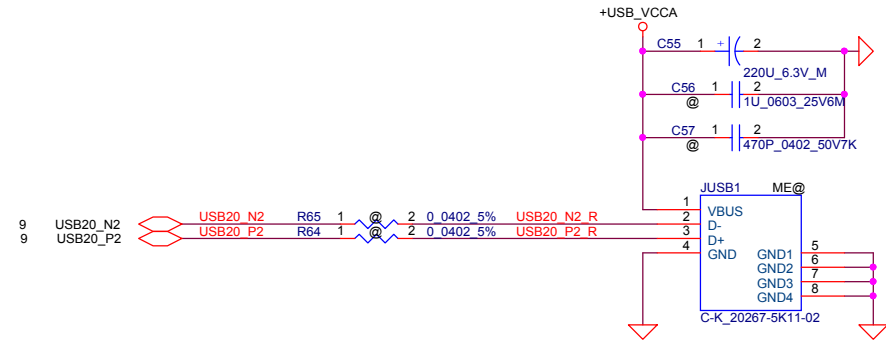
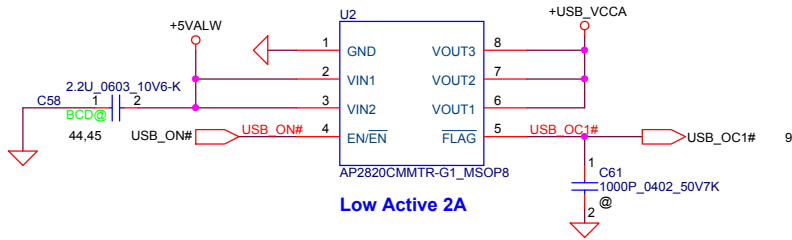


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Size	Document Number	Date:		Rev
Custom	ACLU3	Wednesday, September 17, 2014 Sheet 39 of 59		0.4

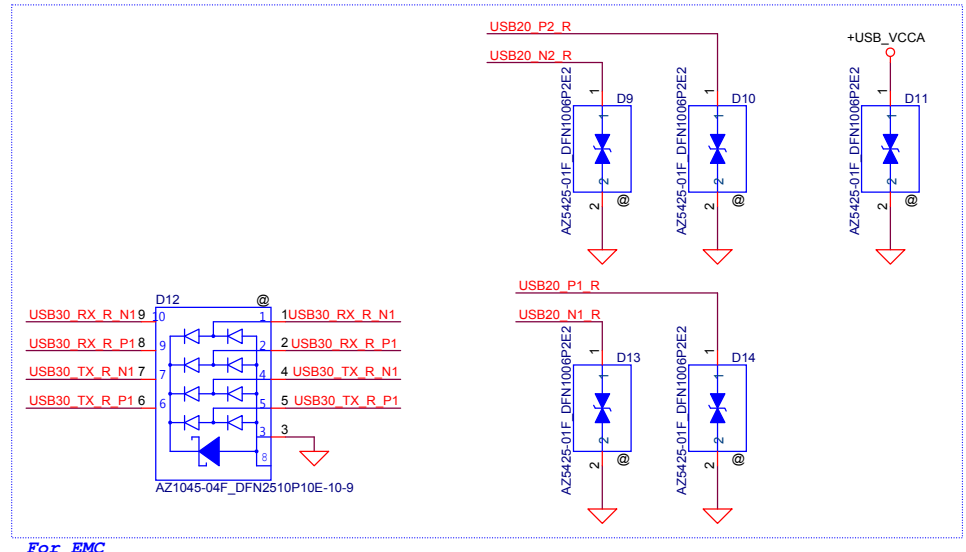
Mini-Express Card(WLAN/WiMAX)



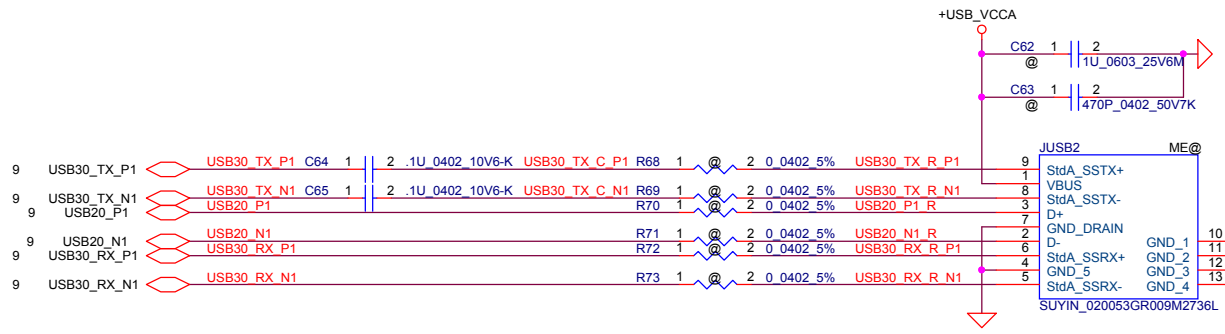
LEFT SIDE USB3.0 PORT X2



For EMC



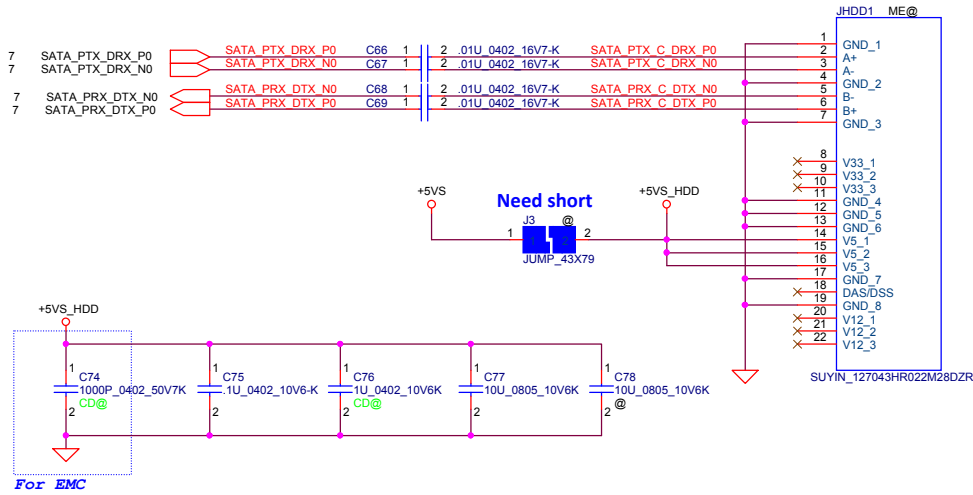
For EMC



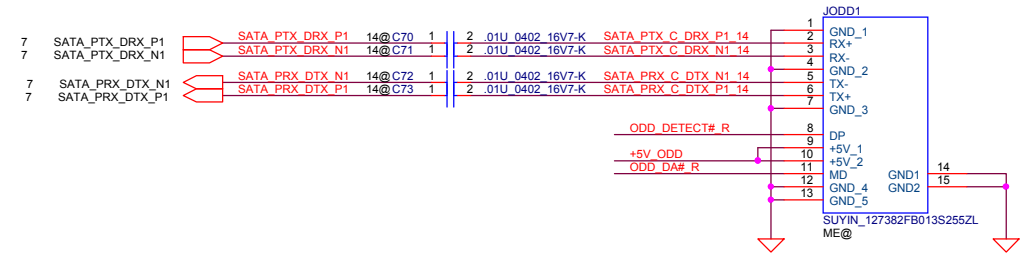
Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05
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Title	USB2.0/USB3.0 PORT (LEFT)	
Size	Document Number	Rev
Custom	ACLU3	0.4
Date:	Wednesday, September 17, 2013	Sheet 41 of 59

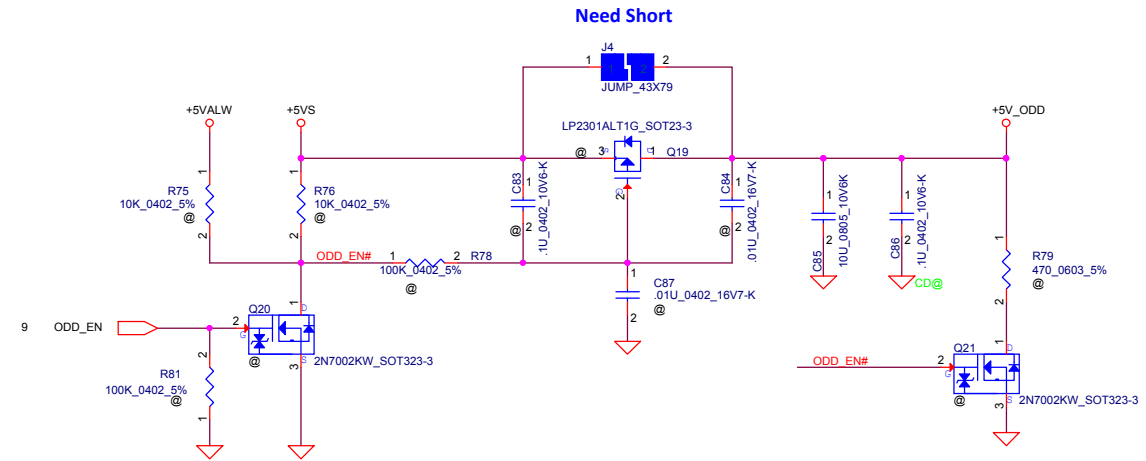
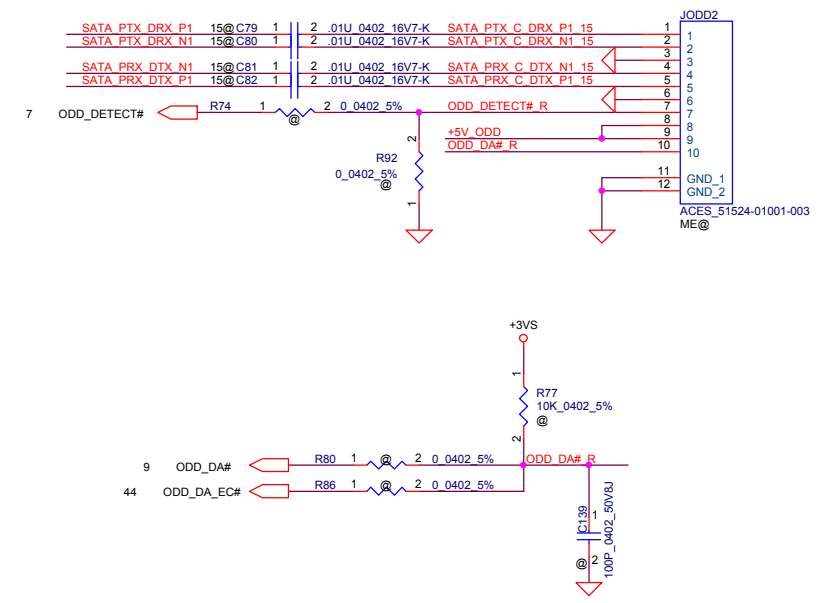
SATA HDD Conn.



FOR 14" SATA ODD Conn.



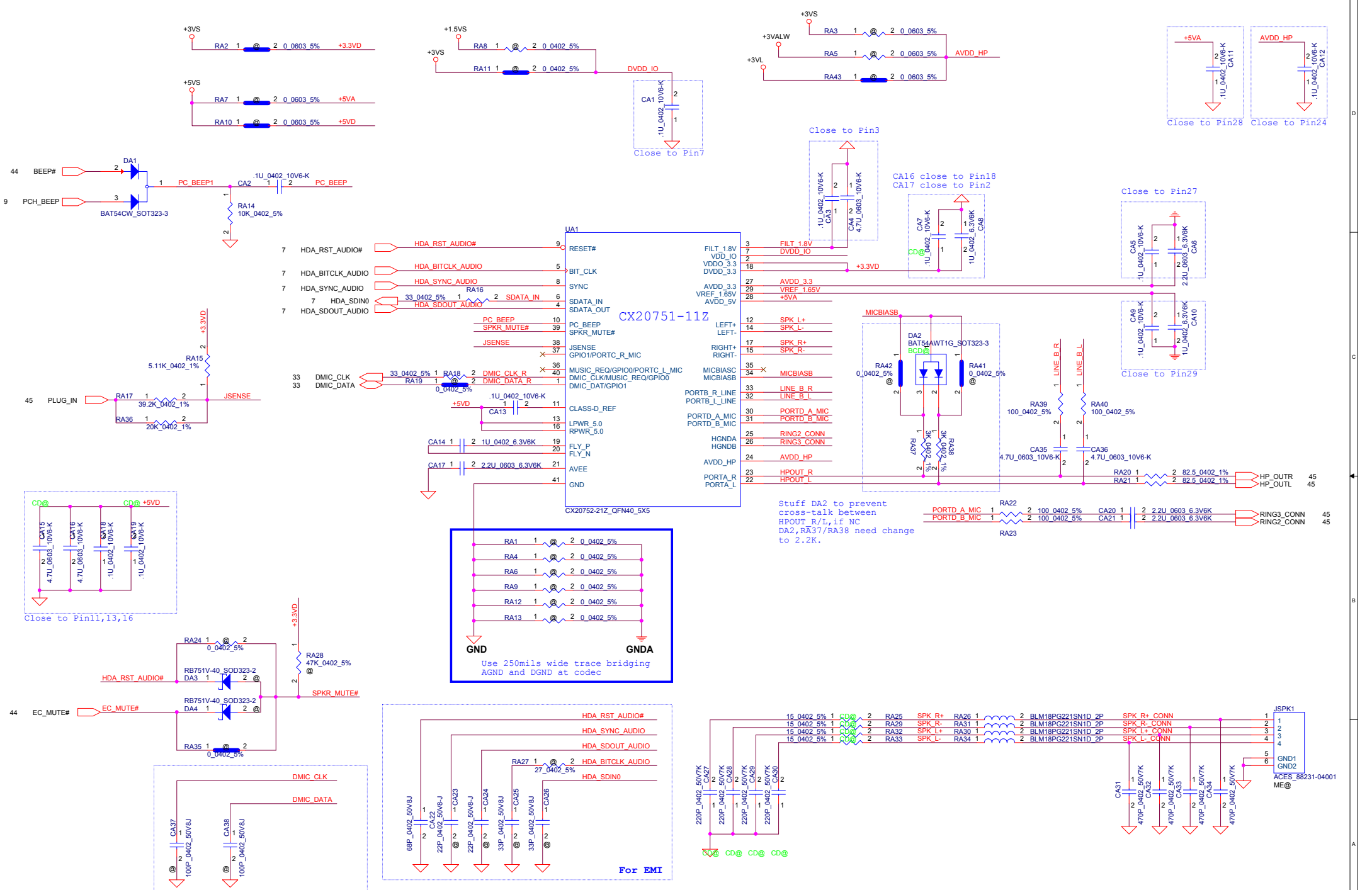
FOR 15" SATA ODD FFC Conn



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ACL03

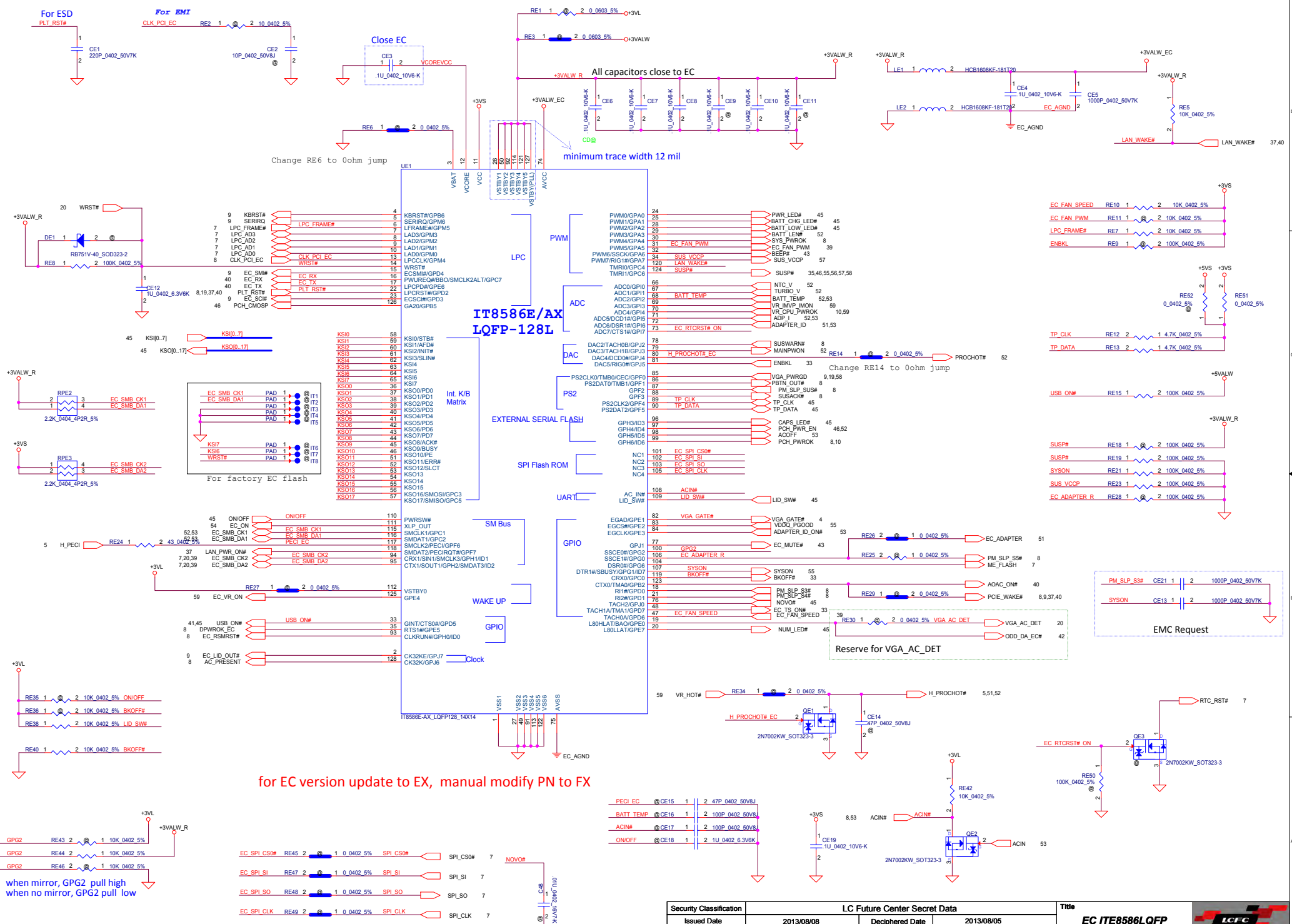


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Issued Date	2013/08/08	Deciphered Date
		2013/08/05

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Title	Revision
Codec_CX20752	0.4
Document Number	Rev
Custom	0.4
Date	Wednesday, September 17, 2014
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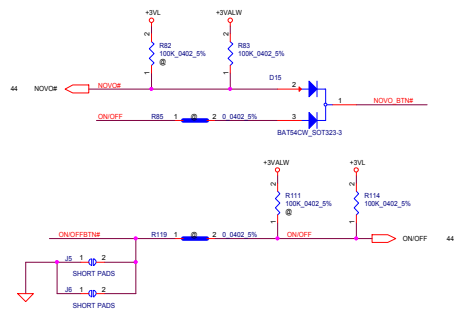
for EC version update to EX, manual modify PN to FX

when mirror, GP2 pull high
when no mirror, GP2 pull low

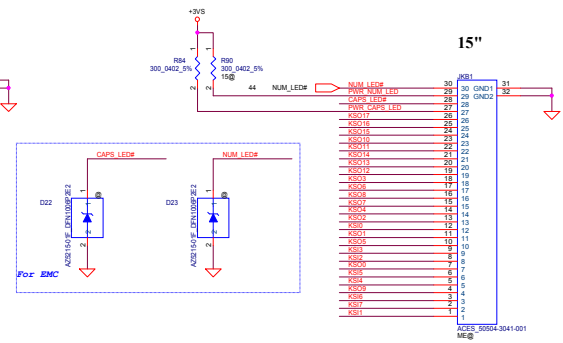
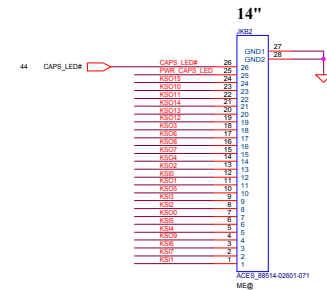
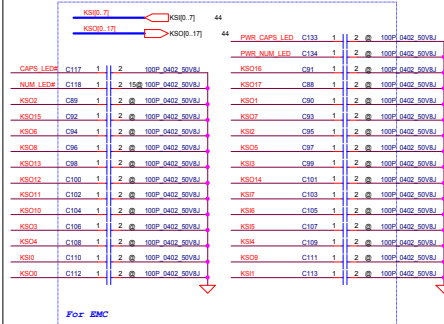
WWW.AliSaler.Com

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Size	Document Number	ACLU3		Rev
C		44		04
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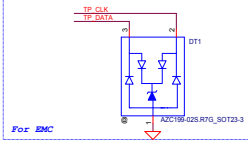
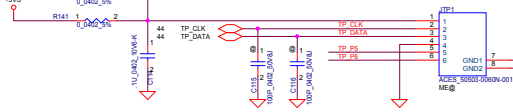
ON/OFF switch



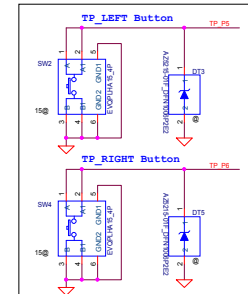
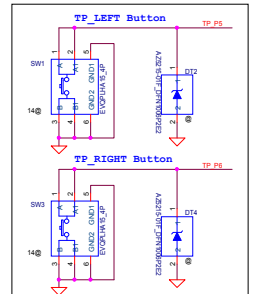
K/B Connector



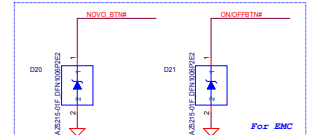
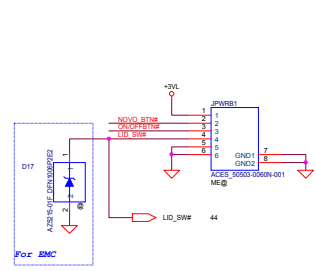
TP/B Connector



For 14"		For 15"	
1	VDD	1	VDD
2	CLK	2	CLK
3	DAT	3	DAT
4	GND	4	GND
5	TP-L	5	TP-L
6	TP-R	6	TP-R

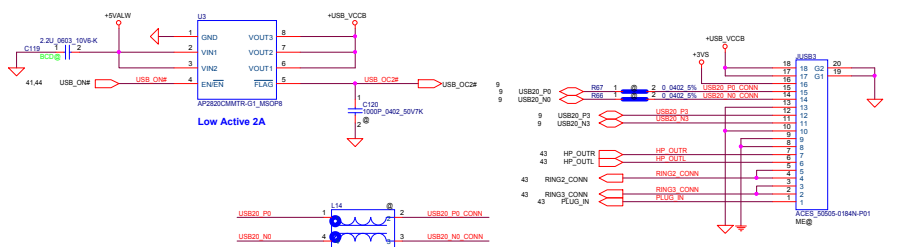


PWR/B Connector

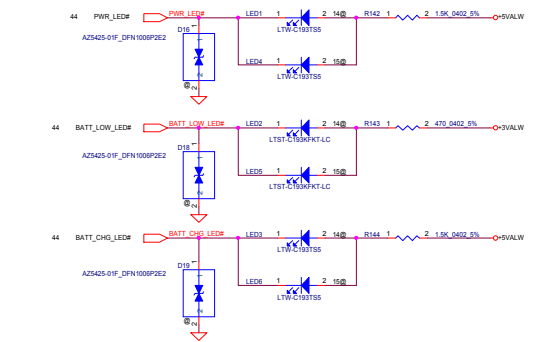


USB I/O Connector

Right Side USB2.0 Port X 1 (USB/B)

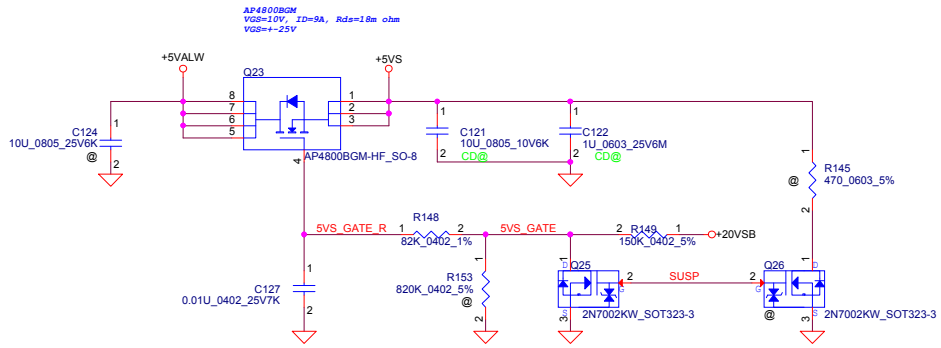


LED

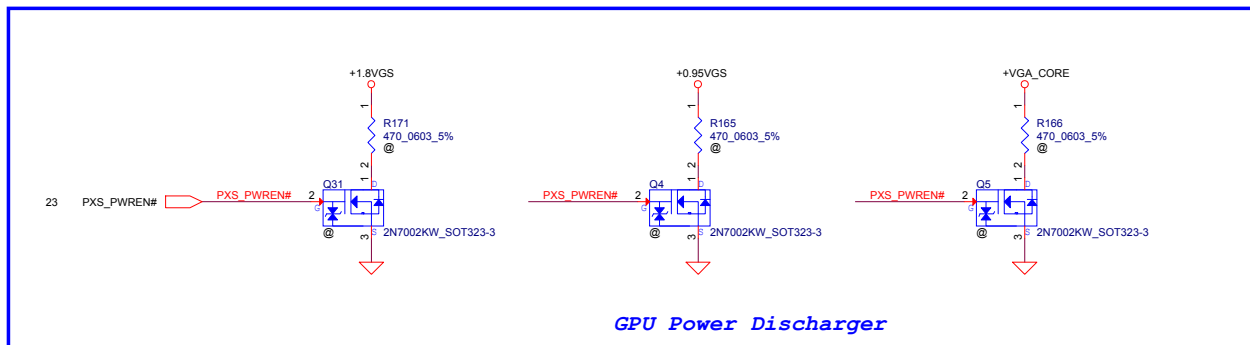
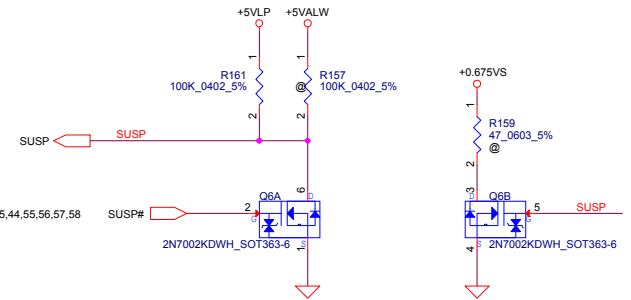
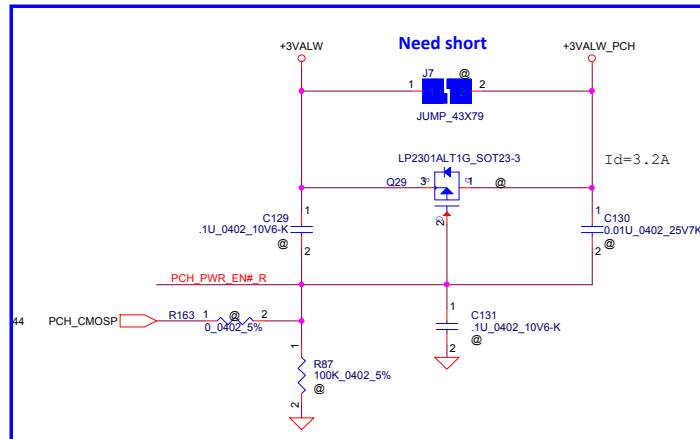
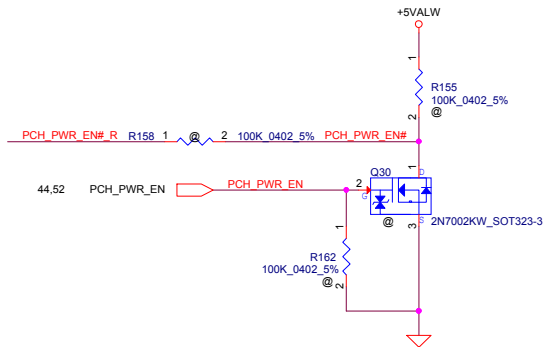
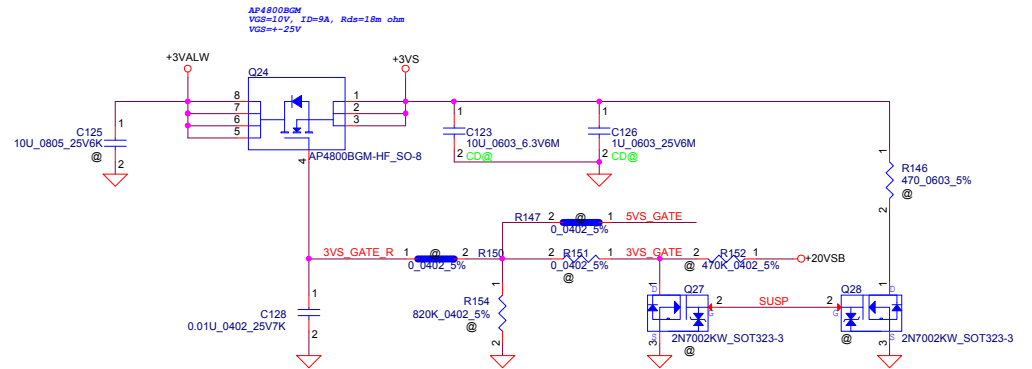



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Site Code	Document Number	Rev	64
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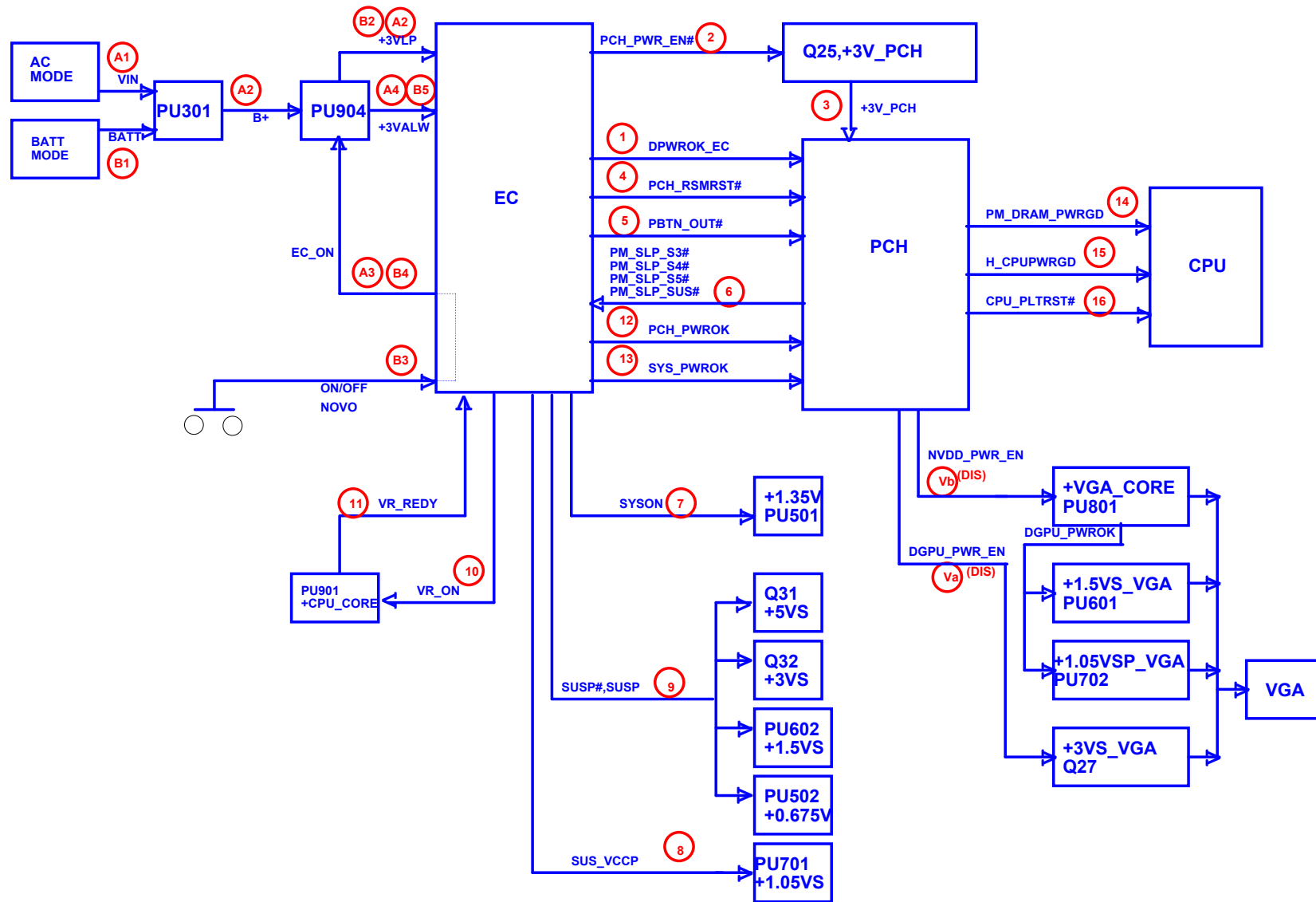
+5VALW to +5VS



+3VALW to +3VS

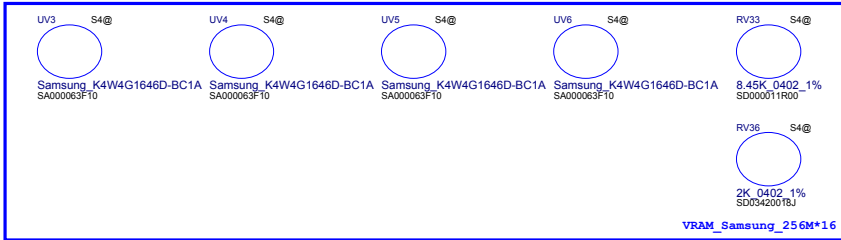
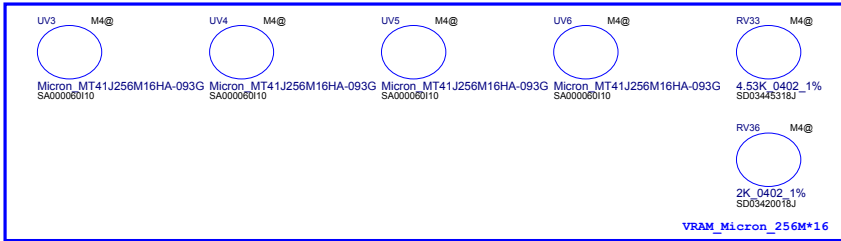
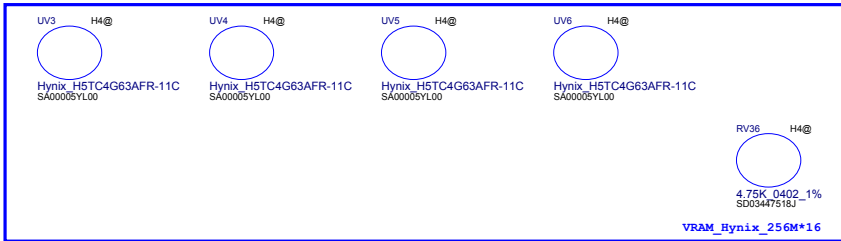
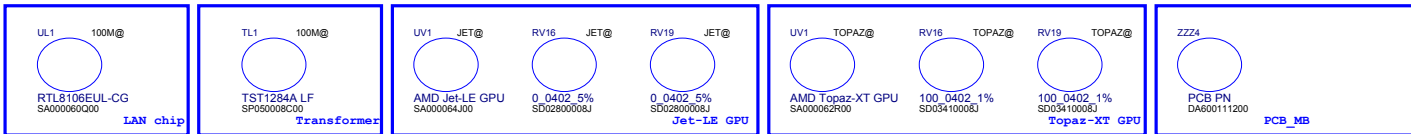


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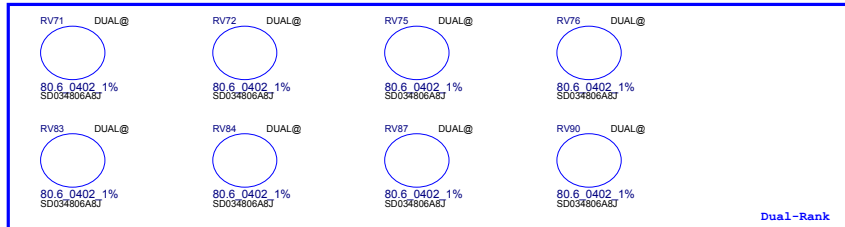
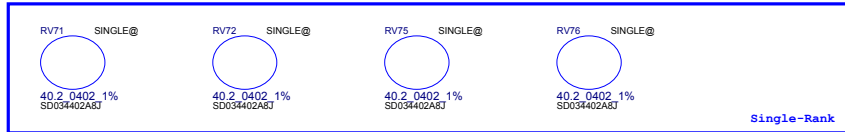
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Title	Power sequence Block		
Document Number	ACL03	Rev	
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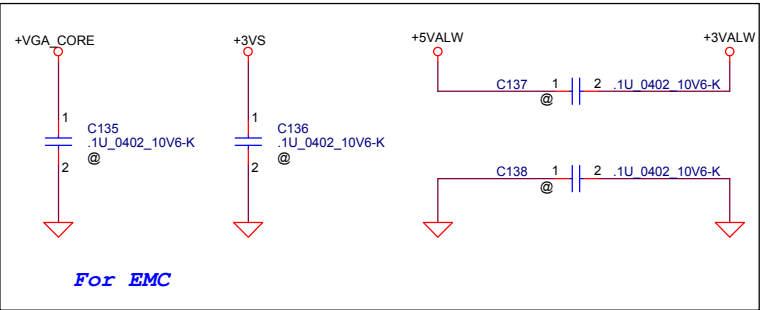
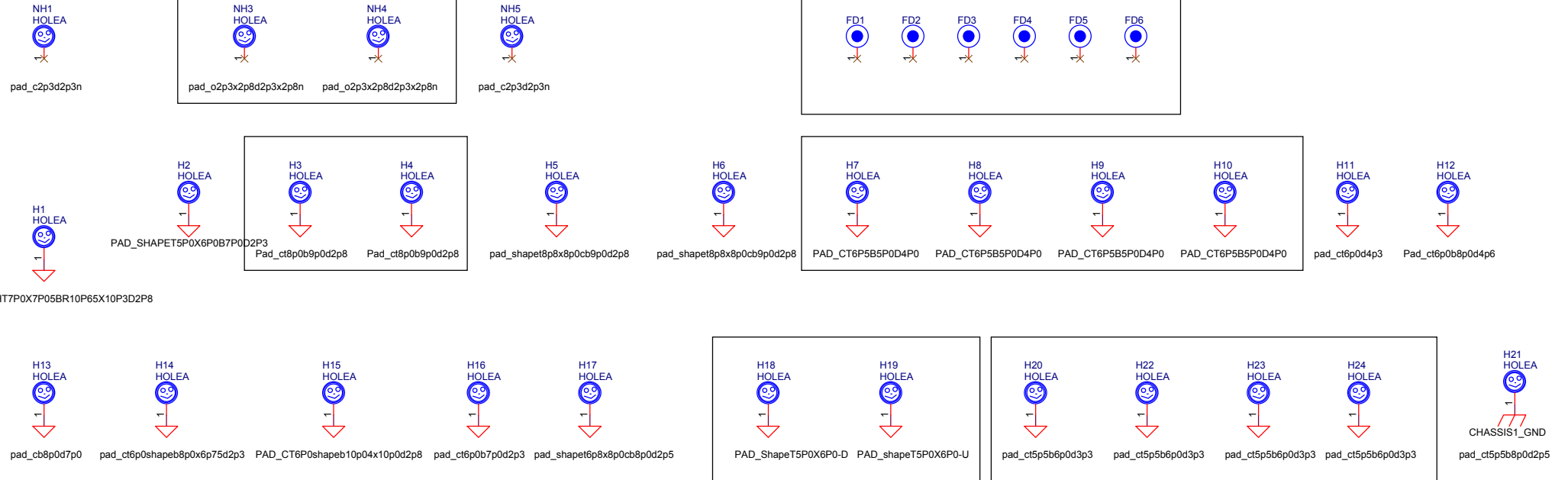



Board ID

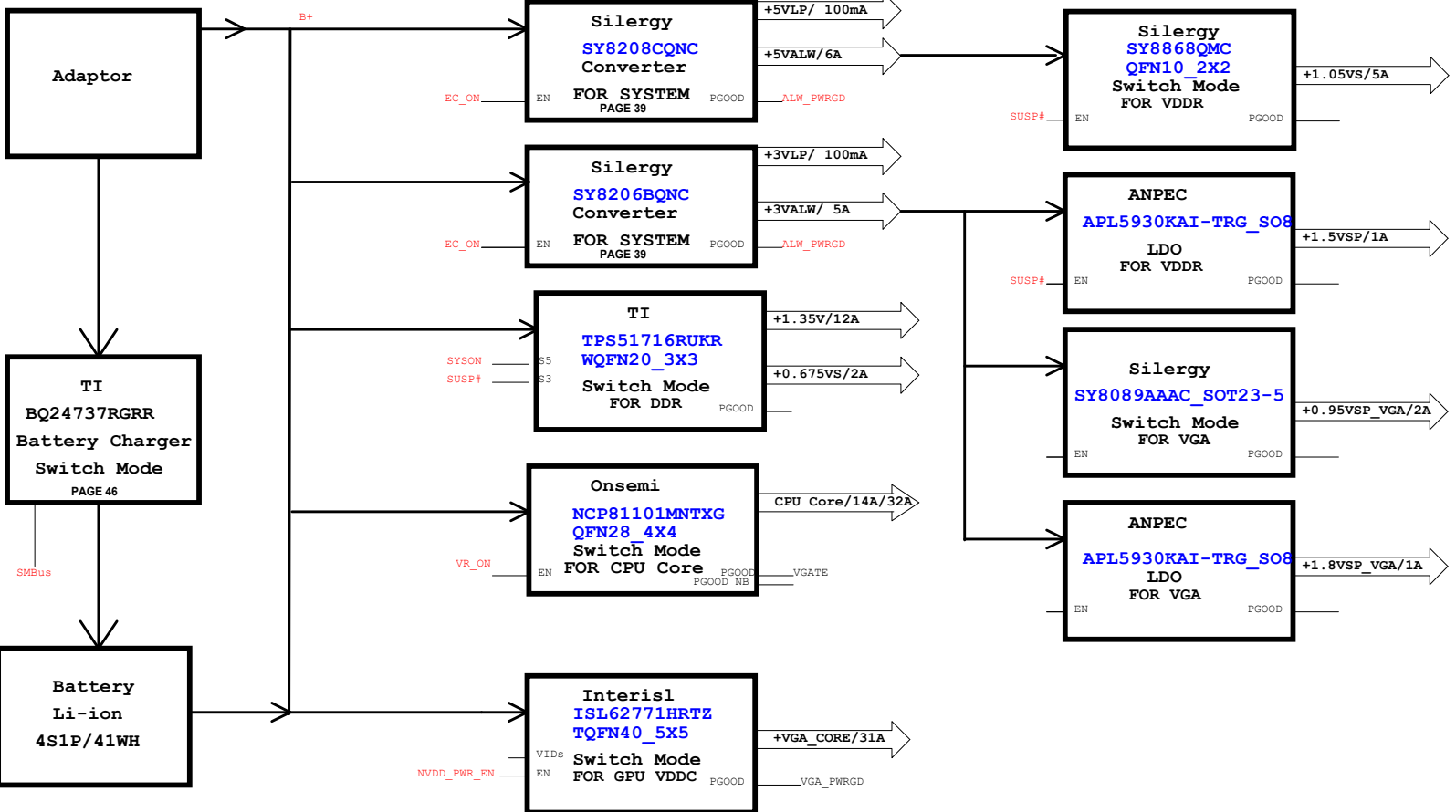
BOARD_ID0	BOARD_ID1	BOARD_ID2	BOARD_ID3	Description	Stuff Resistor
0	0	0	1	14" + Jet-LE + Single-Rank sku	RC107,RC108,RC109,RC12
0	0	1	1	14" + Jet-LE + Dual-Rank sku	RC107,RC108,RC102,RC12
0	1	0	1	15" + Jet-LE + Single-Rank sku	RC107,RC101,RC109,RC12
0	1	1	1	15" + Jet-LE + Dual-Rank sku	RC107,RC101,RC102,RC12
1	0	0	1	14" + Topaz-XT + Single-Rank sku	RC100,RC108,RC109,RC12
1	0	1	1	14" + Topaz-XT + Dual-Rank sku	RC100,RC108,RC102,RC12
1	1	0	1	15" + Topaz-XT + Single-Rank sku	RC100,RC101,RC109,RC12
1	1	1	1	15" + Topaz-XT + Dual-Rank sku	RC100,RC101,RC102,RC12



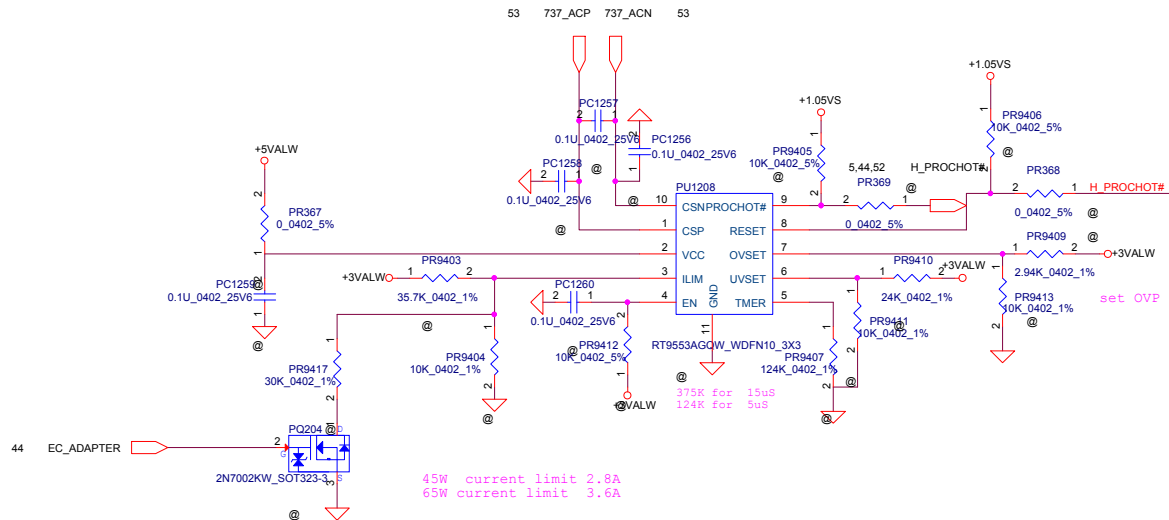
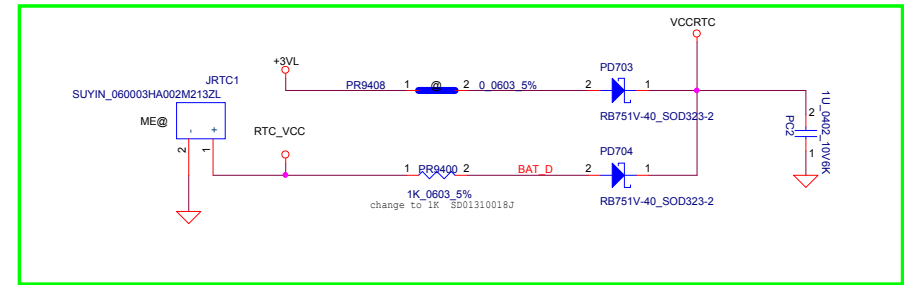
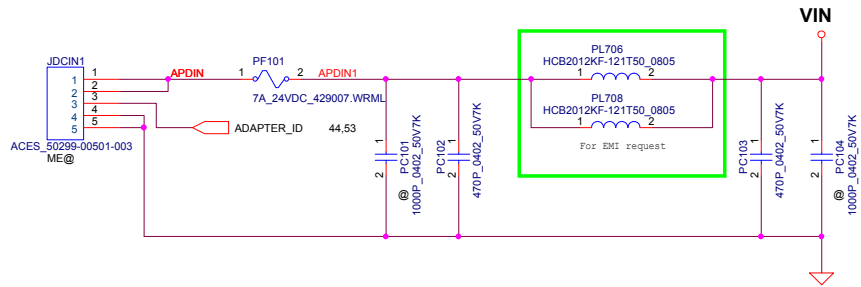
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			Power Diagram ACLU3&ACLU4 Wednesday, September 17, 2014 Sheet 50 of 50

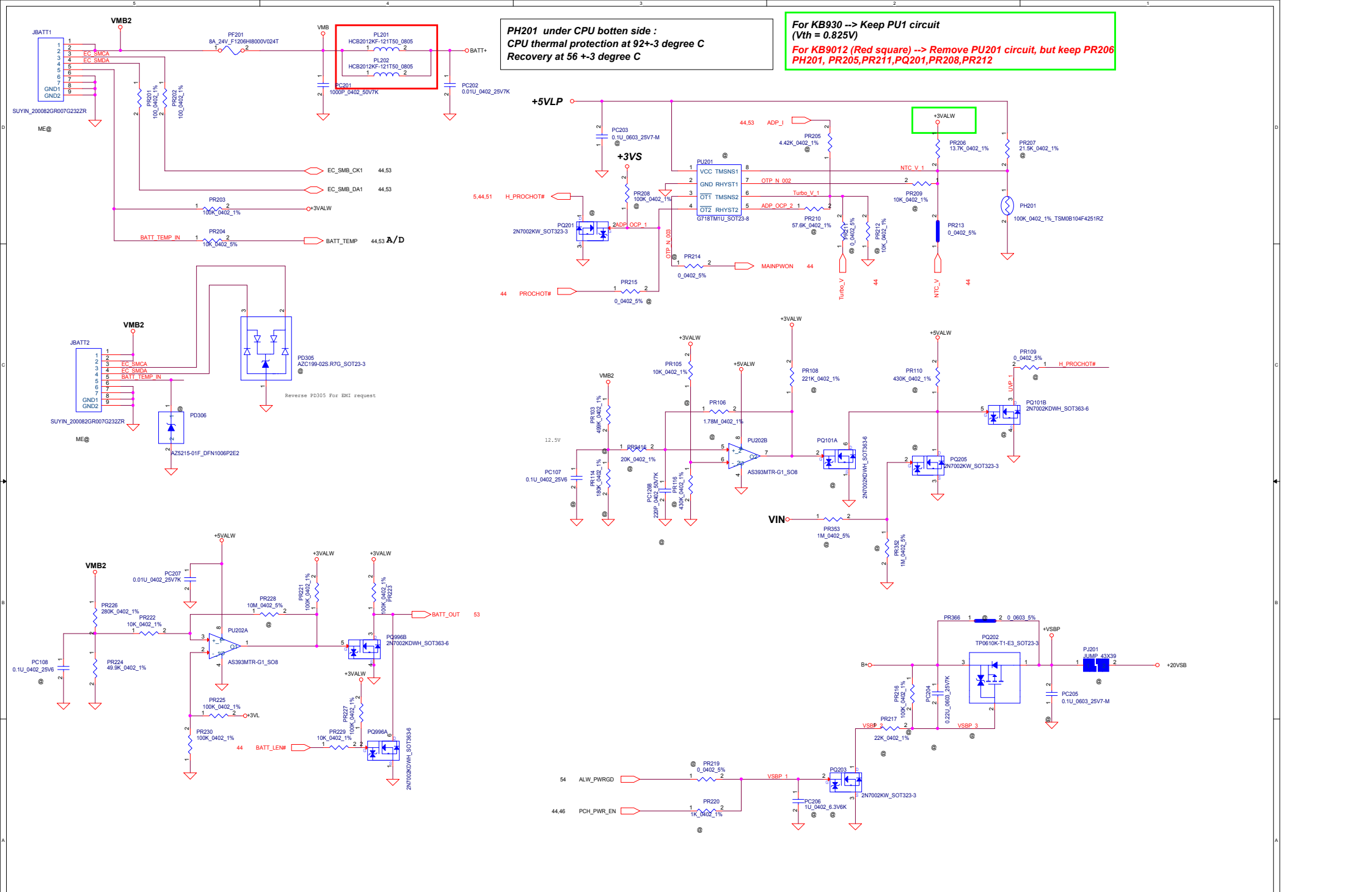


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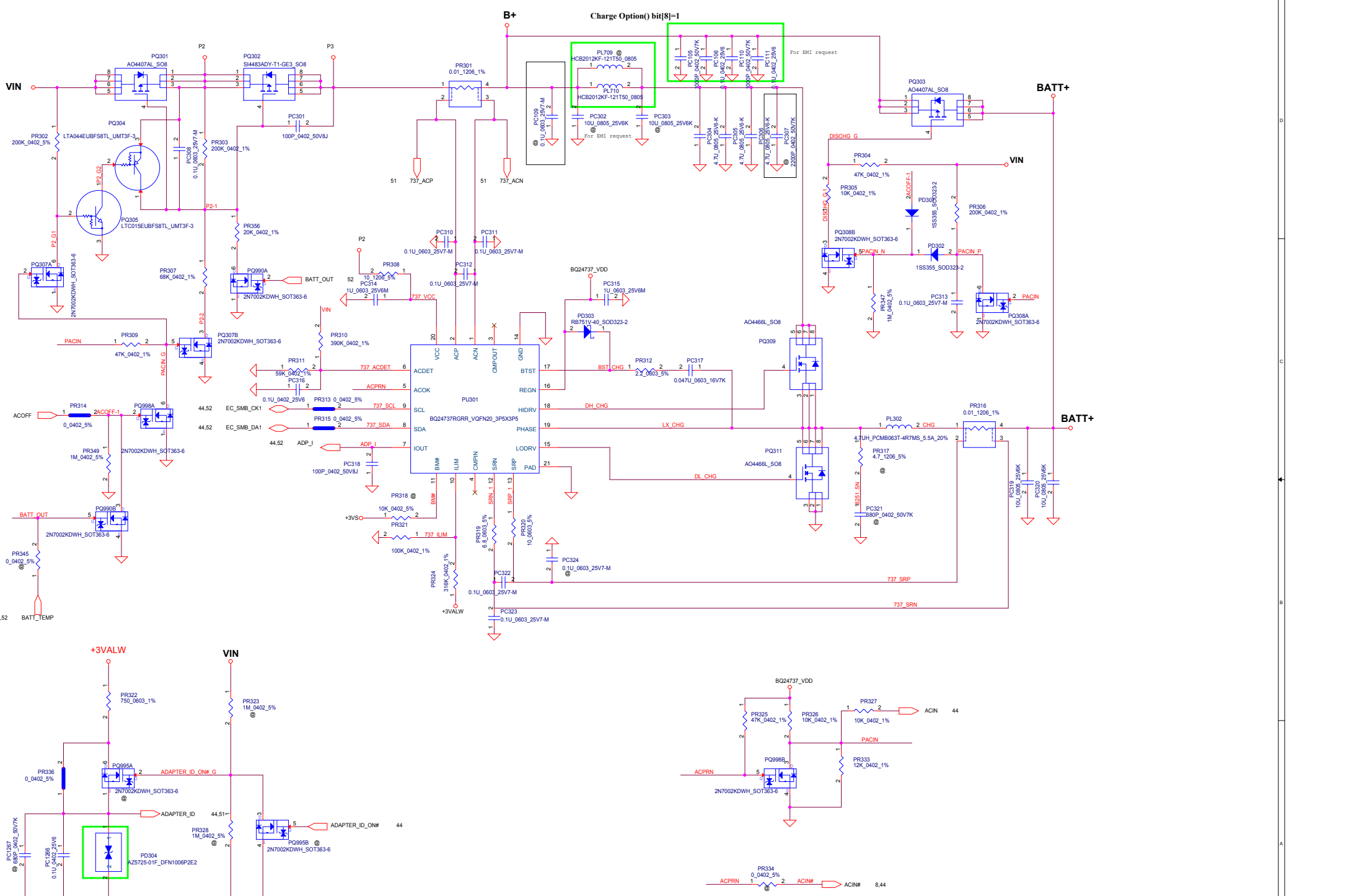
ACL03 & ACL04




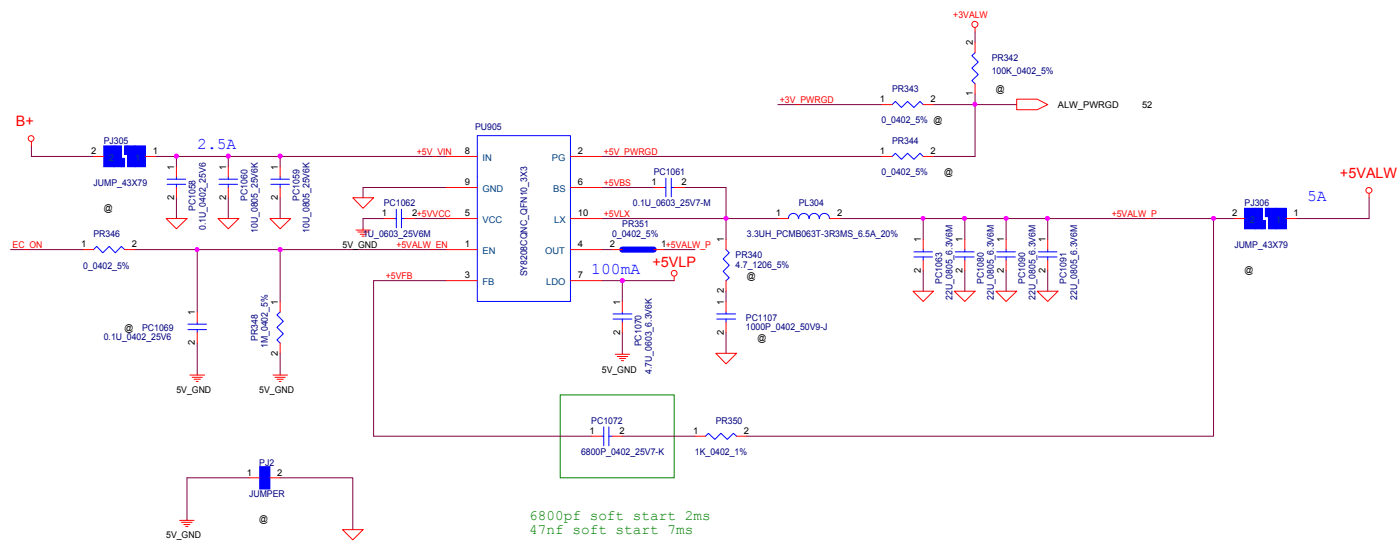
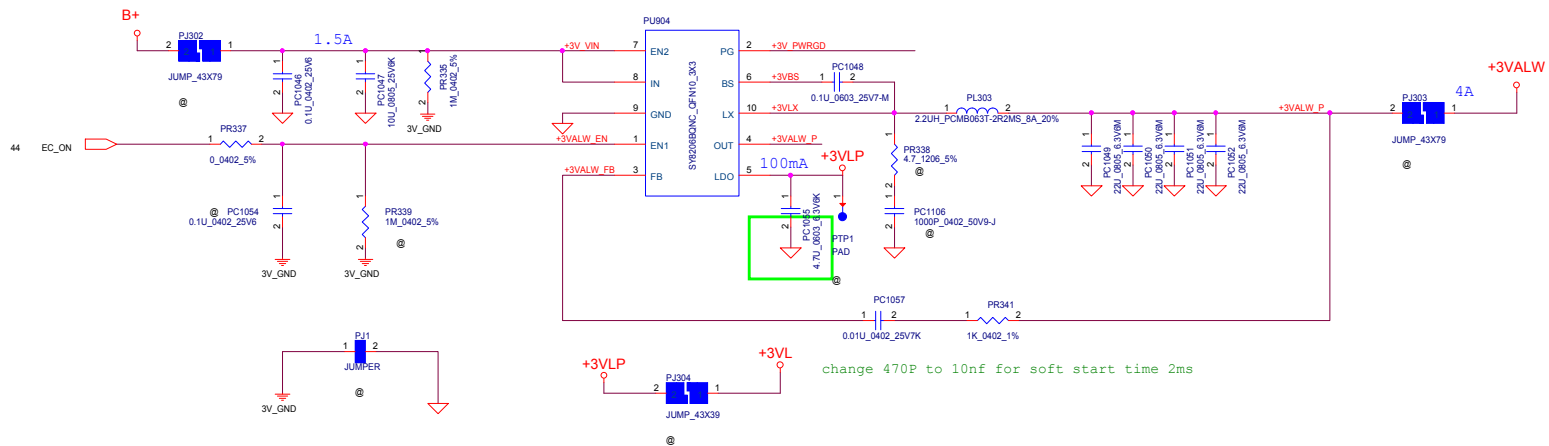
PH201 under CPU bottom side :
 CPU thermal protection at 92+/-3 degree C
 Recovery at 56 +/-3 degree C


For KB930 --> Keep PU1 circuit
 (Vth = 0.825V)
 For KB9012 (Red square) --> Remove PU201 circuit, but keep PR206
 PH201, PR205, PR211, PQ201, PR208, PR212

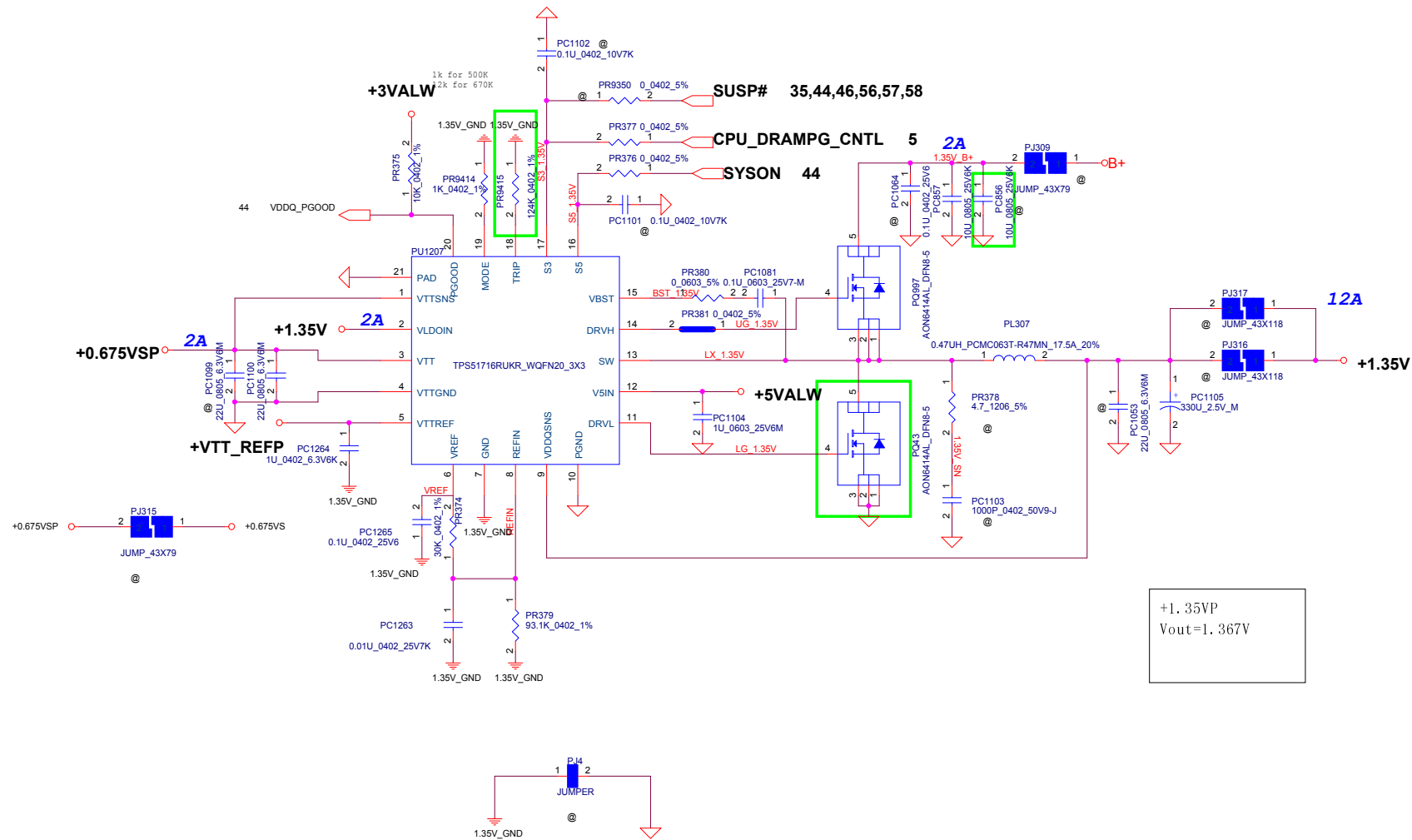
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Date: Wednesday, September 17, 2014 11:20:53 AM				Sheet 53 of 59

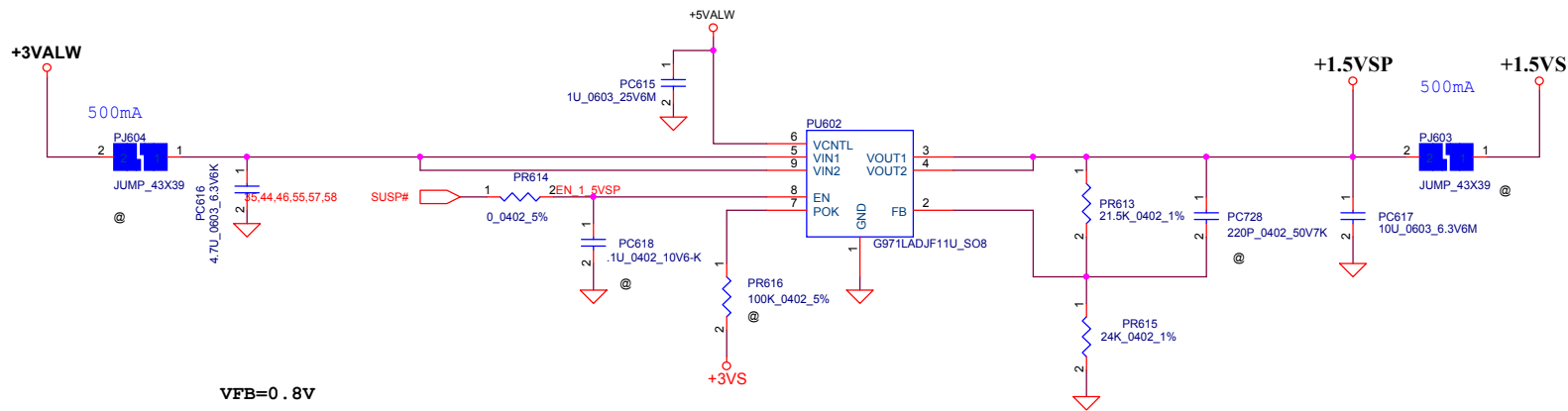


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1.35VS/+0.675VS		
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VFB=0.8V

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			Custom	0.4
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44,46,55,56,58

SUSP#

SUS_VCCP

VFB=0.6V

5A

+1.05VS

1A

2A

+0.95VSP_VGA

+0.95VGS

4,23,58 PXS_PWREN

SUSP#

VFB=0.8V

+1.8VGS

+1.8VGS

+3VALW

500mA

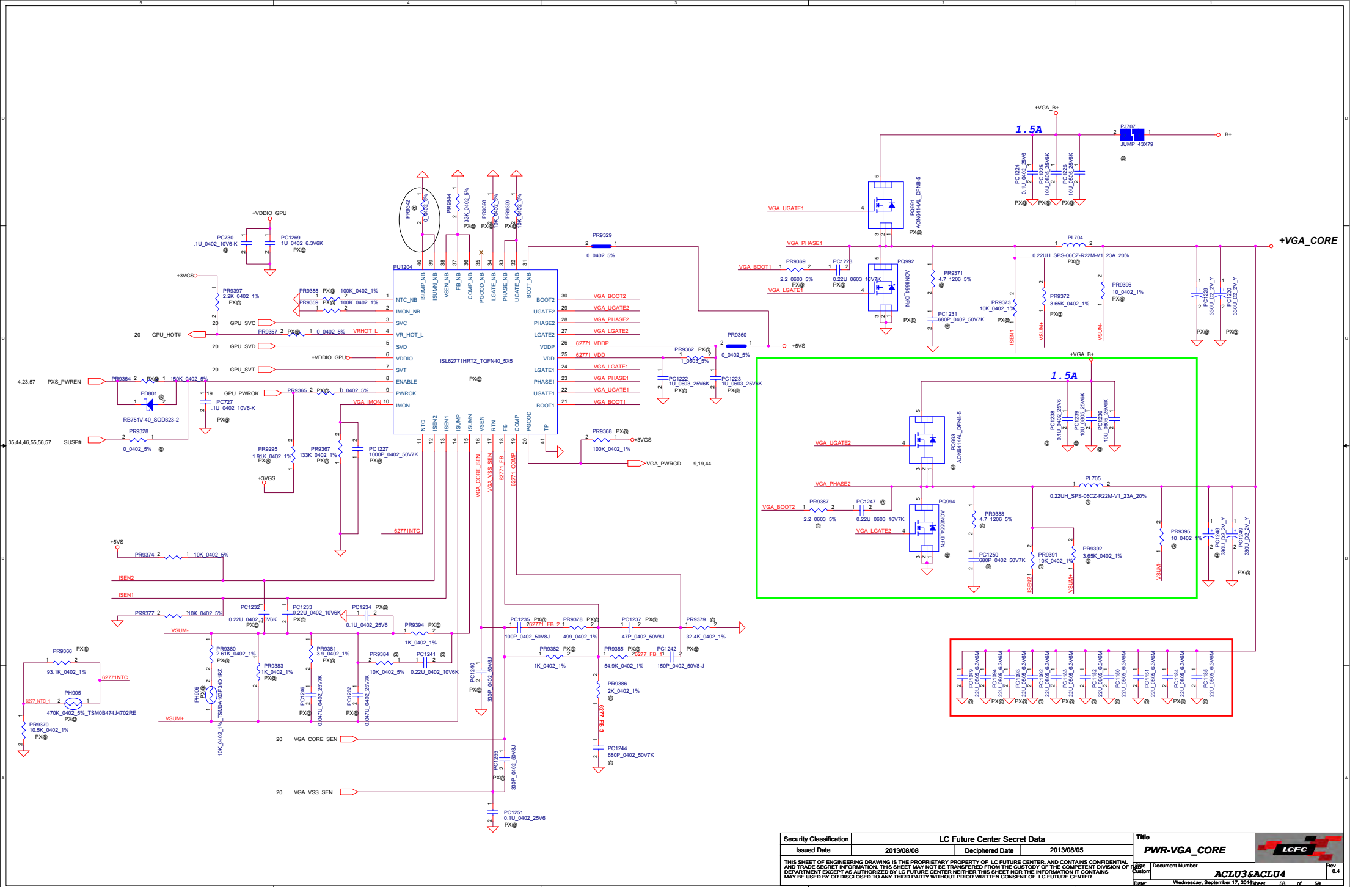
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500mA

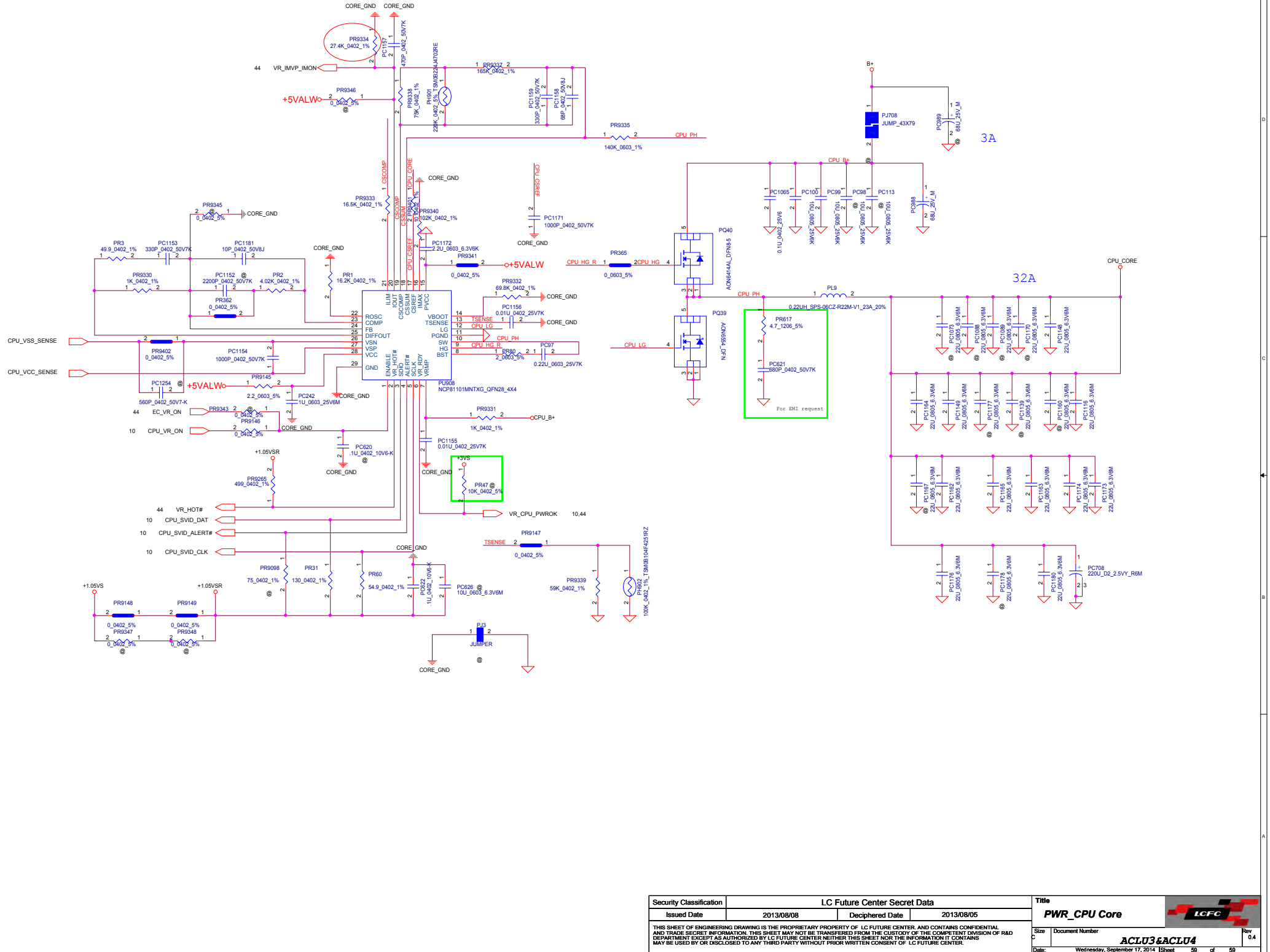
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				ACL03&ACL04	
				Date:	Wednesday, September 17, 2014 Sheet 59 of 59