# COMPAL CONFIDENTIAL

**MODEL NAME : VALA0**

**PCB NO : LA-9411P**
**GPIO P/N: 2012.12.20 Rev 3.0C**

**BOM P/N :**

**4319L231L01 SMT MB A9411 VALA0 DSC TPM R1**
**4319L231L02 SMT MB A9411 VALA0 DSC DTP R1**
**4319L231L03 SMT MB A9411 VALA0 DSC TPM WO EXP R1**
**4319L231L04 SMT MB A9411 VALA0 DSC DTP WO EXP R1**
**4319L231L05 SMT MB A9411 VALA0 DSC TPM R1**
**4319L231L06 SMT MB A9411 VALA0 DSC DTP R1**
**4319L231L07 SMT MB A9411 VALA0 DSC TPM WO EXP R1**
**4319L231L08 SMT MB A9411 VALA0 DSC DTP WO EXP R1**

# SALADO 15 HSW

## HASWELL + LYNX POINT

## 2013_04_10

**REV : 1.0 (A00)**

**@ : Nopop Component**
**CONN@ : Connector Component**

| | L01/L02/L5/L6 | L03/L04/L7/L8 |
|---|---|---|
| 15MDC@ : MDC | V | V |
| 15G@ : Only for 15 Discrete | V | V |
| PXDP@ : PCH XDP | | |
| EMC@ : EMI/ESD/RF | V | V |
| EXP@ : Express Card | V | V |
| CXDP@ : CPU XDP | | |

MB PCB

| Part Number | Description |
|---|---|
| DAA00005Q00 | PCB 0LH LA-9411P REV0 M/B DSC |





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Title: Cover Page

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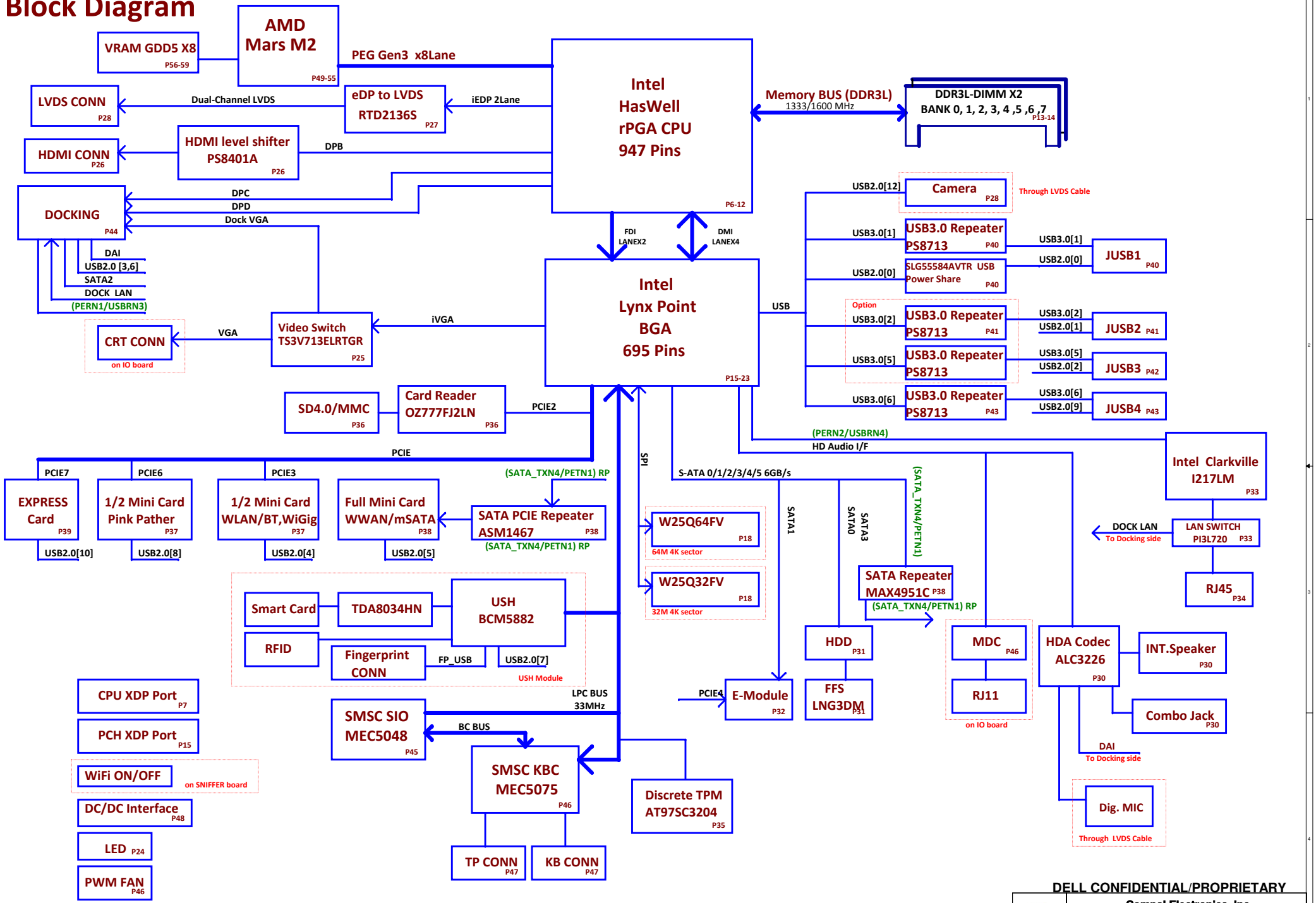
# Block Diagram

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Title: Block Diagram

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## POWER STATES

| Signal / State | SLP S3# | SLP S4# | SLP S5# | SLP A# | ALWAYS PLANE | M PLANE | SUS PLANE | RUN PLANE | CLOCKS |
|---|---|---|---|---|---|---|---|---|---|
| S0 (Full ON) / M0 | HIGH | HIGH | HIGH | HIGH | ON | ON | ON | ON | ON |
| S3 (Suspend to RAM) / M3 | LOW | HIGH | HIGH | HIGH | ON | ON | ON | OFF | OFF |
| S4 (Suspend to DISK) / M3 | LOW | LOW | HIGH | HIGH | ON | ON | OFF | OFF | OFF |
| S5 (SOFT OFF) / M3 | LOW | LOW | LOW | HIGH | ON | ON | OFF | OFF | OFF |
| S3 (Suspend to RAM) / M-OFF | LOW | HIGH | HIGH | LOW | ON | OFF | ON | OFF | OFF |
| S4 (Suspend to DISK) / M-OFF | LOW | LOW | HIGH | LOW | ON | OFF | OFF | OFF | OFF |
| S5 (SOFT OFF) / M-OFF | LOW | LOW | LOW | LOW | ON | OFF | OFF | OFF | OFF |

## PM TABLE

| power plane / State | +PWR_SRC<br>+PWR_SRC_S<br>+5V_ALW<br>+3.3V_ALW<br>+3.3V_ALW_PCH<br>+3.3V_RTC_LDO | +3.3V_SUS<br>+1.35V_MEM | +5V_RUN<br>+3.3V_RUN<br>+1.5V_RUN<br>+0.675V_DDR_VTT<br>+VCC_CORE<br>+1.05V_RUN<br>+GPU_CORE<br>+1.35V_MEM_GFX<br>+1.8V_RUN_GFX<br>+VGA_PCIE<br>+3.3V_RUN_GFX<br>+VDDCI | +3.3V_M<br>+1.05V_M | +3.3V_M<br>+1.05V_M<br>(M-OFF) |
|---|---|---|---|---|---|
| S0 | ON | ON | ON | ON | ON |
| S3 | ON | ON | OFF | ON | OFF |
| S5 S4/AC | ON | OFF | OFF | ON | OFF |
| S5 S4/AC don't exist | OFF | OFF | OFF | OFF | OFF |

| | USB 2.0 PORT# | USB 3.0 PORT# | DESTINATION |
|---|---|---|---|
| PCH | 0 | 1 | Right Side Top (JUSB1) |
| | 1 | 2 | Right Side Middle (JUSB2) |
| | 2 | 5 | Right Side bottom (JUSB3) |
| | 3 | 3 (PERN1/USBRN3) | DOCKING (JDOCK1) |
| | 4 | | WLAN (JMINI2) |
| | 5 | | WWAN (JMINI1) |
| | 6 | | DOCKING (JDOCK1) |
| | 7 | | USH (JUSH1) |
| | 8 | | Pink Pather (JMINI3) |
| | 9 | 6 | Left Side (JUSB4) |
| | 10 | | Express card (JEXP1) |
| | 11 | | None |
| | 12 | | CAMERA (JCAM1) |
| | 13 | | None |

| PCI EXPRESS | DESTINATION |
|---|---|
| Lane 1 (SATA_TXN4/PETN1) | WWAN (JMINI1) SATA by default |
| Lane 2 (SATA_RXN5/PERN2) | None |
| Lane 2 (PERN2/USBRN4) | 10/100/1G LOM |
| Lane 3 | WLAN (JMINI2) |
| Lane 4 | E3 Module Bay (JSATA2) |
| Lane 5 | None |
| Lane 6 | Pink Pather (JMINI3) |
| Lane 7 | Express card (JEXP1) |
| Lane 8 | MMI |

| SATA | DESTINATION |
|---|---|
| SATA 0 | HDD (JSATA1) |
| SATA 1 | ODD (JSATA2) |
| SATA 2 | Dock (JDOCK1) |
| SATA 3 | NA |
| SATA 4 (SATA_TXN4/PETN1) | WWAN (JMINI1)<br>SATA by default |

| DISPLAY Ports On CPU | Connetion |
|---|---|
| DDIB | MB HDMI (JHDMI1) |
| DDIC | Dock DP port 1 |
| DDID | Dock DP port 2 |

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Title: Index and Configuration

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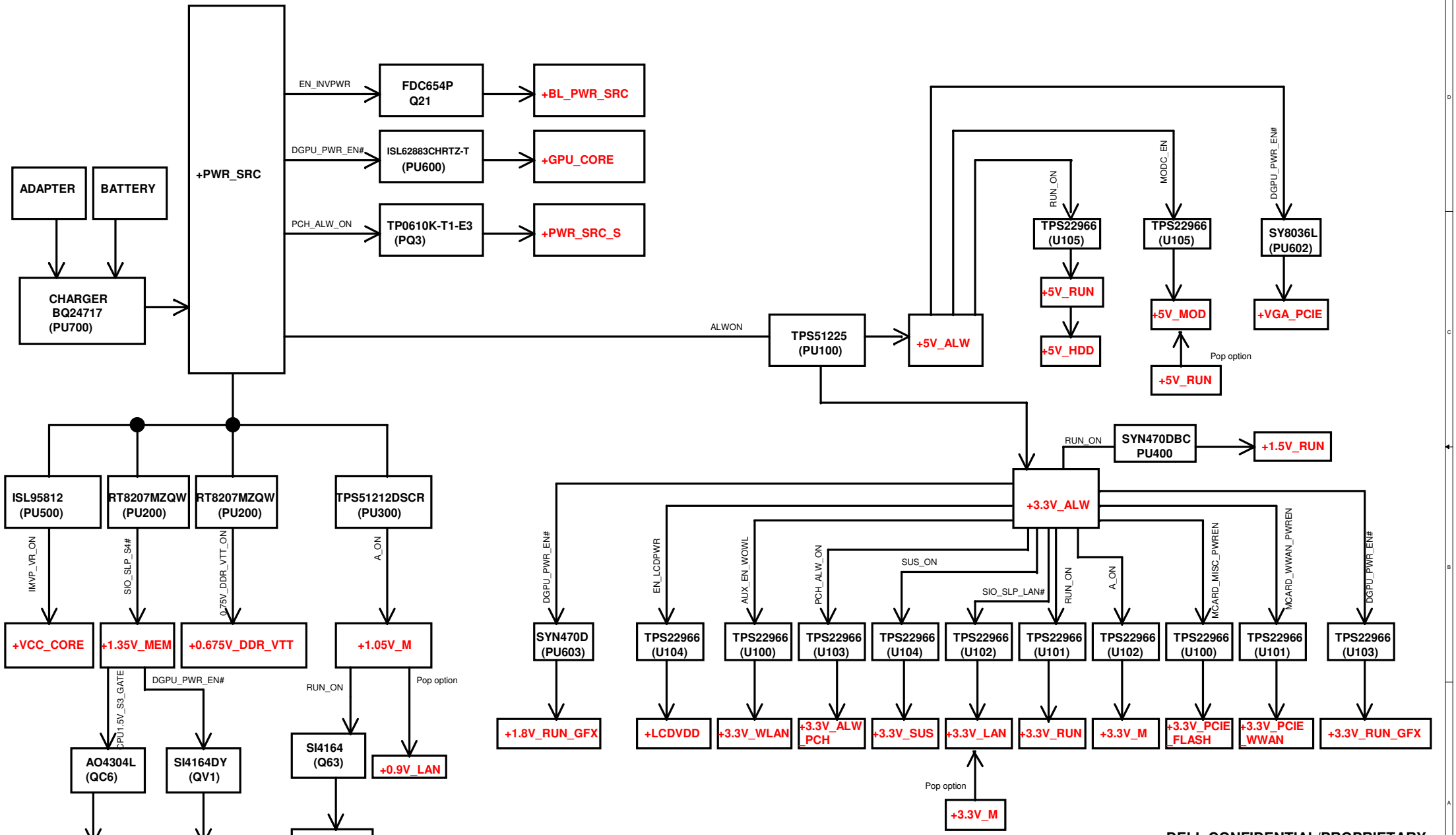


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Title: Power Rail

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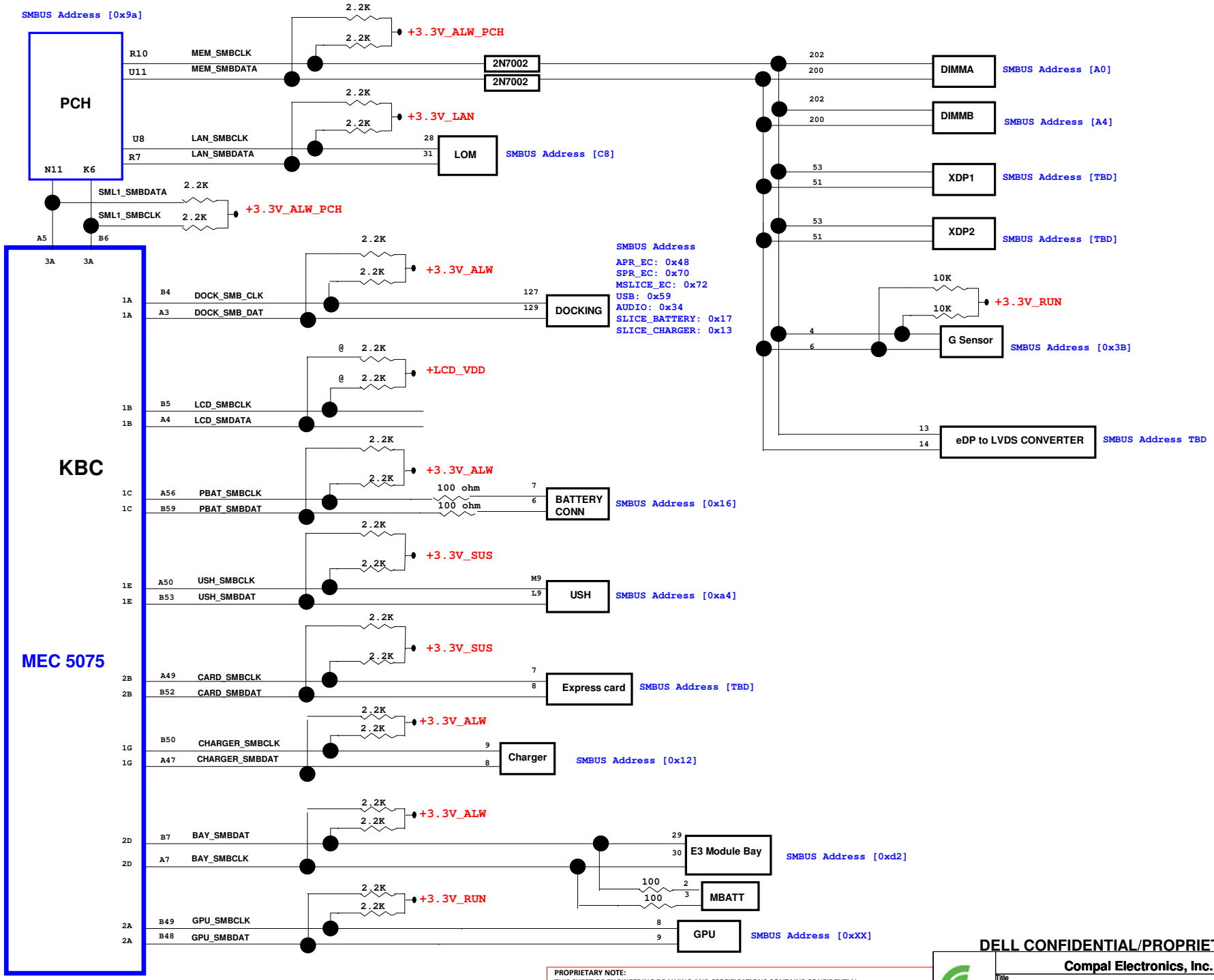


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Title: SMBus block diagram

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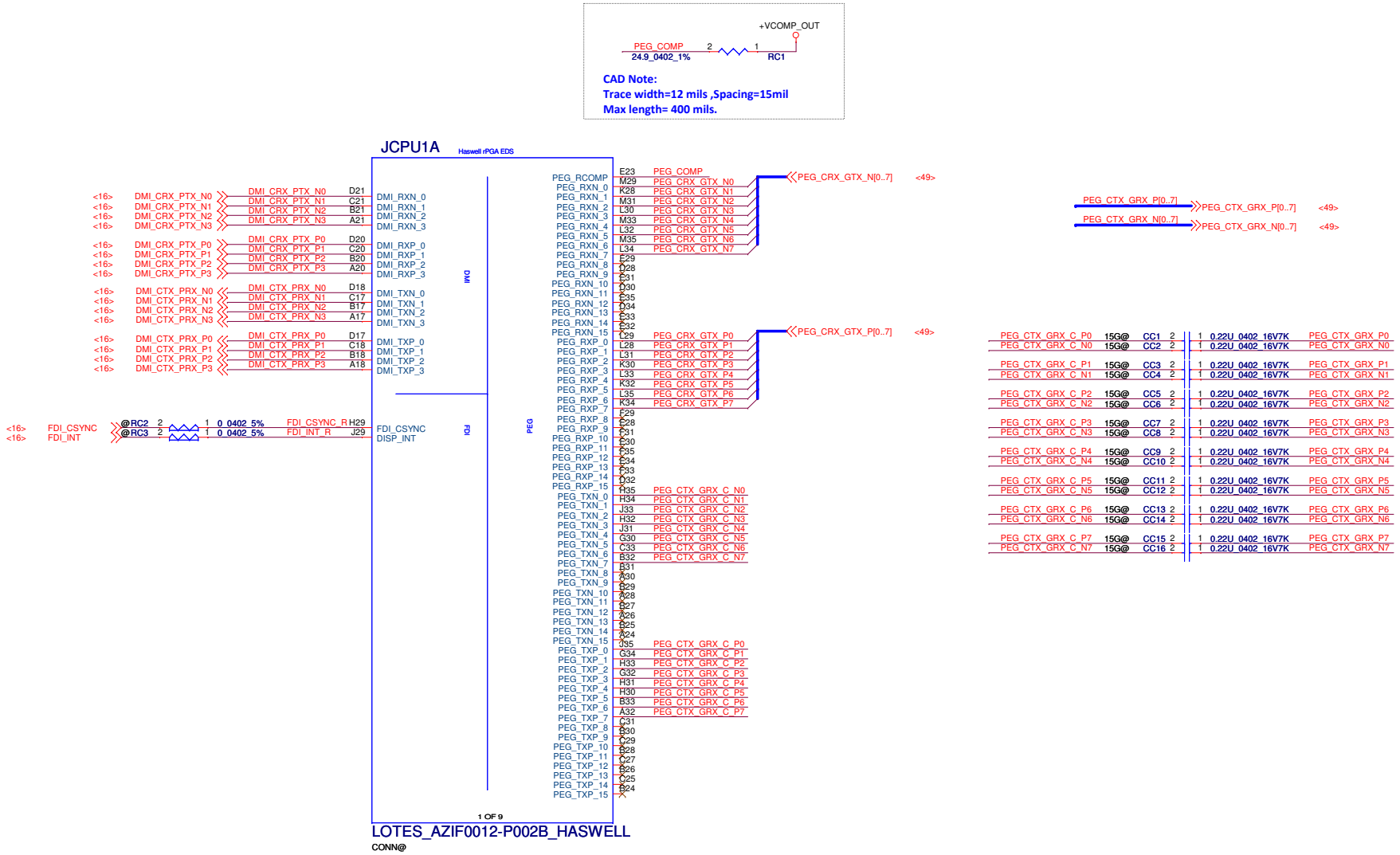





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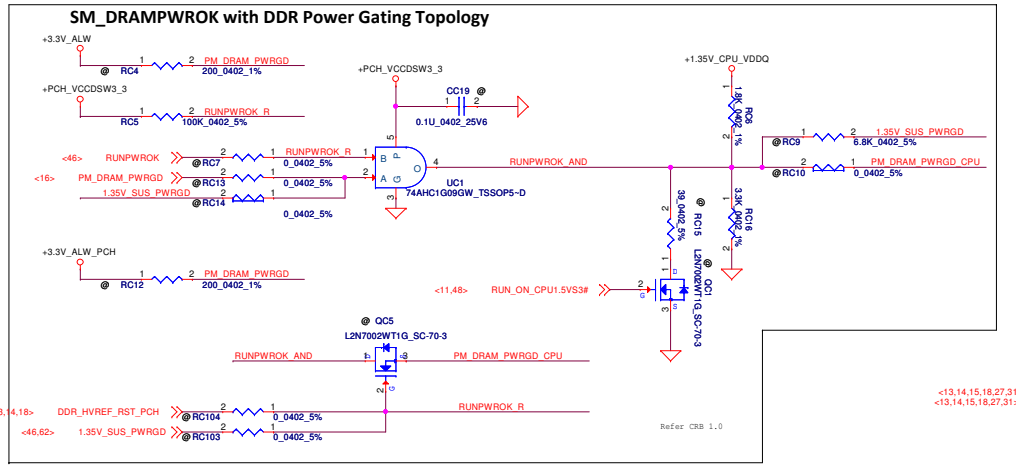


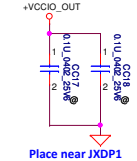


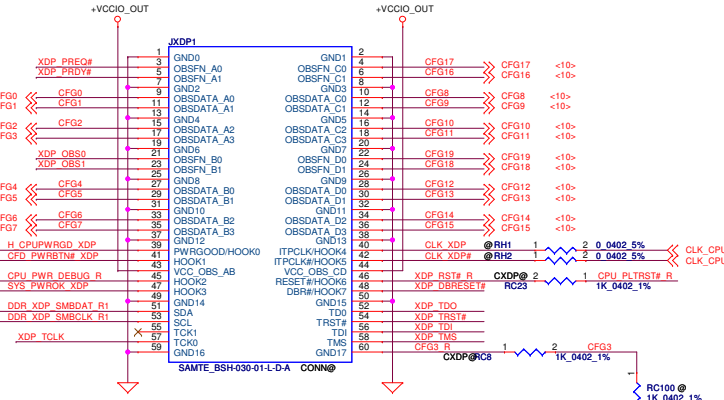


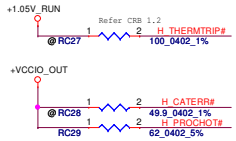


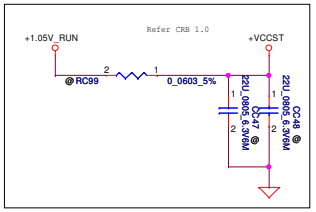


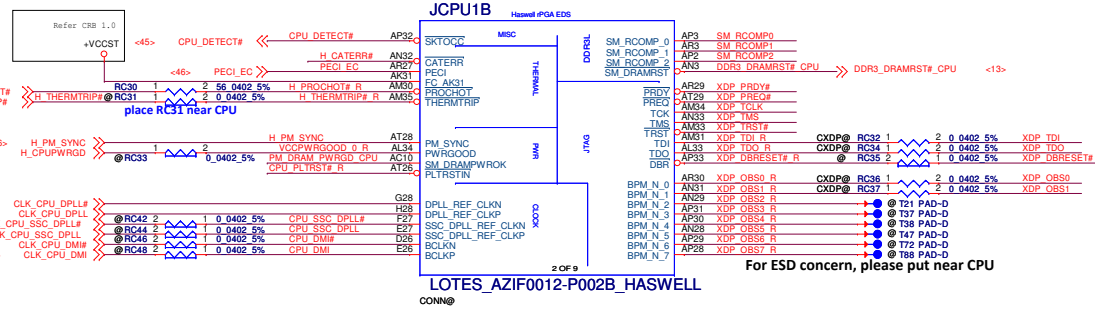


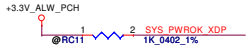


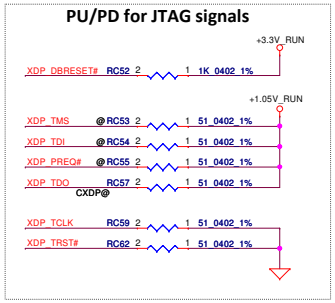


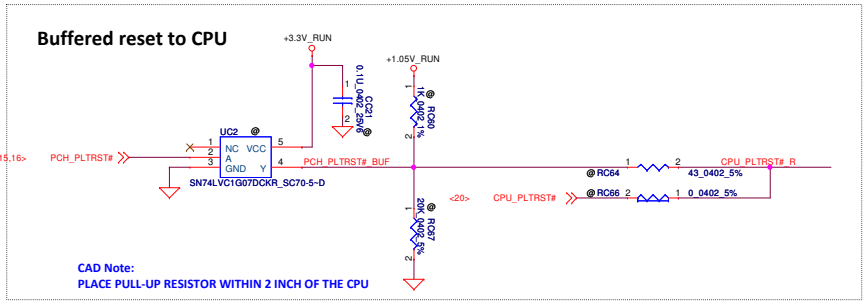


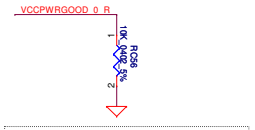


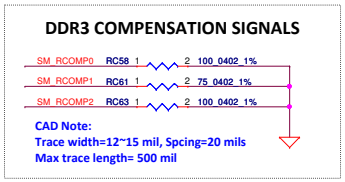




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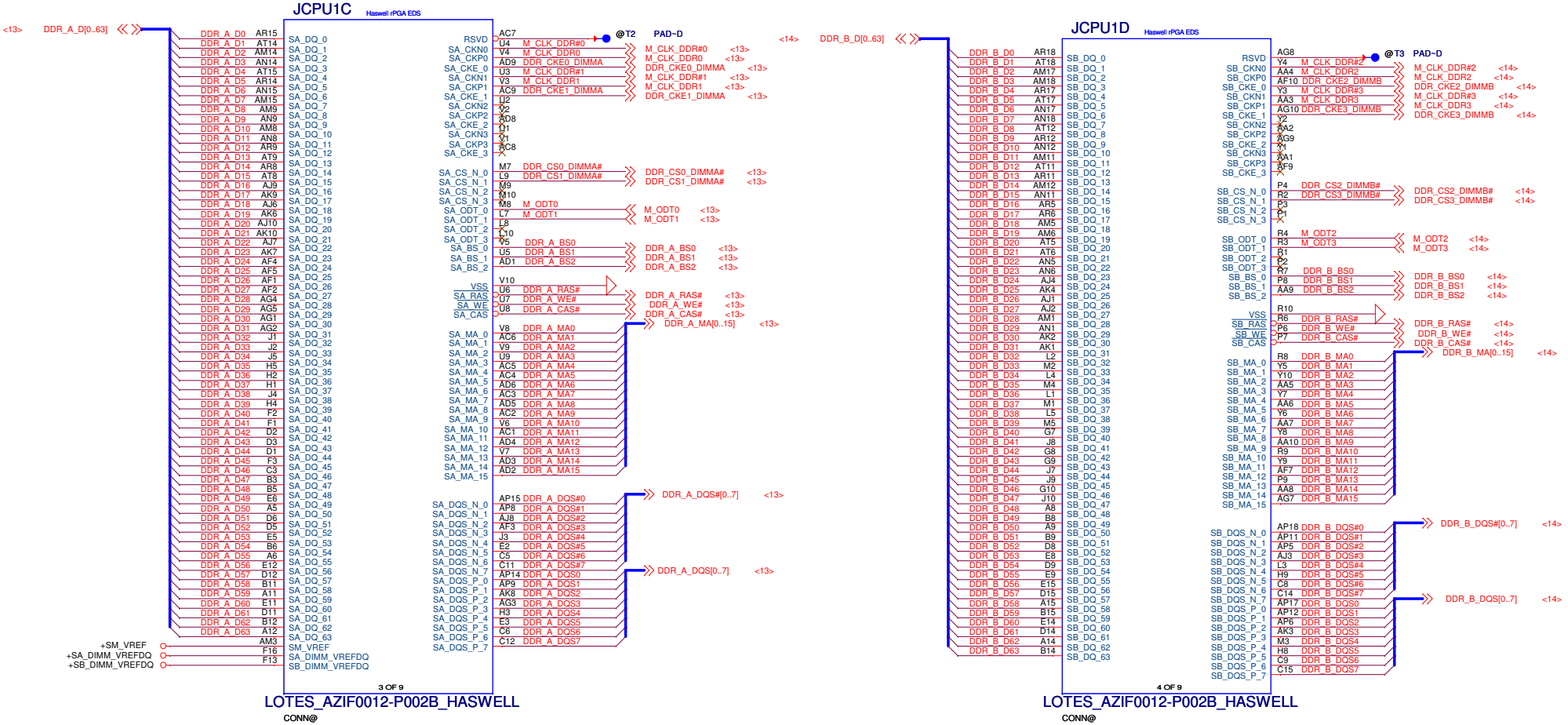




| | | |
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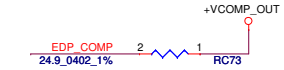
## COMPENSATION PU FOR eDP




CAD Note:Trace width=20 mils ,Spacing=25mil, Max length=100 mils.

## JCPU1H

Haswell rPGA EDS

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| <26> | TMDSB_CPU_N2 | TMDSB_CPU_N2 | T28 | DDIB_TXN0 | | | | | |
| <26> | TMDSB_CPU_P2 | TMDSB_CPU_P2 | U28 | DDIB_TXP0 | | | | | |
| <26> | TMDSB_CPU_N1 | TMDSB_CPU_N1 | T30 | DDIB_TXN1 | | | | | |
| <26> | TMDSB_CPU_P1 | TMDSB_CPU_P1 | U30 | DDIB_TXP1 | | | | | |
| <26> | TMDSB_CPU_N0 | TMDSB_CPU_N0 | U29 | DDIB_TXN2 | | | | | |
| <26> | TMDSB_CPU_P0 | TMDSB_CPU_P0 | V29 | DDIB_TXP2 | | | | | |
| <26> | TMDSB_CPU_CLK# | TMDSB_CPU_CLK# | V31 | DDIB_TXN3 | | | | | |
| <26> | TMDSB_CPU_CLK | TMDSB_CPU_CLK | V31 | DDIB_TXP3 | | | | | |
| <44> | DPC_CPU_LANE_N0 | DPC_CPU_LANE_N0 | T34 | DDIC_TXN0 | | | | | |
| <44> | DPC_CPU_LANE_P0 | DPC_CPU_LANE_P0 | U34 | DDIC_TXP0 | | | | | |
| <44> | DPC_CPU_LANE_N1 | DPC_CPU_LANE_N1 | U35 | DDIC_TXN1 | | | | | |
| <44> | DPC_CPU_LANE_P1 | DPC_CPU_LANE_P1 | V35 | DDIC_TXP1 | DDI | | | | |
| <44> | DPC_CPU_LANE_N2 | DPC_CPU_LANE_N2 | U32 | DDIC_TXN2 | | | | | |
| <44> | DPC_CPU_LANE_P2 | DPC_CPU_LANE_P2 | T32 | DDIC_TXP2 | | | | | |
| <44> | DPC_CPU_LANE_N3 | DPC_CPU_LANE_N3 | U33 | DDIC_TXN3 | | | | | |
| <44> | DPC_CPU_LANE_P3 | DPC_CPU_LANE_P3 | V33 | DDIC_TXP3 | | | | | |
| <44> | DPD_CPU_LANE_N0 | DPD_CPU_LANE_N0 | P29 | DDID_TXN0 | | | | | |
| <44> | DPD_CPU_LANE_P0 | DPD_CPU_LANE_P0 | R29 | DDID_TXP0 | | | | | |
| <44> | DPD_CPU_LANE_N1 | DPD_CPU_LANE_N1 | N28 | DDID_TXN1 | | | | | |
| <44> | DPD_CPU_LANE_P1 | DPD_CPU_LANE_P1 | P28 | DDID_TXP1 | | | | | |
| <44> | DPD_CPU_LANE_N2 | DPD_CPU_LANE_N2 | P31 | DDID_TXN2 | | | | | |
| <44> | DPD_CPU_LANE_P2 | DPD_CPU_LANE_P2 | R31 | DDID_TXP2 | | | | | |
| <44> | DPD_CPU_LANE_N3 | DPD_CPU_LANE_N3 | N30 | DDID_TXN3 | | | | | |
| <44> | DPD_CPU_LANE_P3 | DPD_CPU_LANE_P3 | P30 | DDID_TXP3 | | | | | |

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| | | | | | | |
|---|---|---|---|---|---|---|
| EDP_AUXN | M27 | EDP_CPU_AUX# | EDP_CPU_AUX# | <27> | | |
| EDP_AUXP | N27 | EDP_CPU_AUX | EDP_CPU_AUX | <27> | | |
| EDP_HPD | P27 | EDP_HPD# | | | | |
| EDP_RCOMP | E24 | EDP_COMP | | | | |
| EDP_DISP_UTIL | R27 | | | | | |
| | | | | | | |
| EDP_TXN_0 | P35 | EDP_CPU_LANE_N0 | EDP_CPU_LANE_N0 | <27> | | |
| EDP_TXP_0 | R35 | EDP_CPU_LANE_P0 | EDP_CPU_LANE_P0 | <27> | | |
| EDP_TXN_1 | N34 | EDP_CPU_LANE_N1 | EDP_CPU_LANE_N1 | <27> | | |
| EDP_TXP_1 | P34 | EDP_CPU_LANE_P1 | EDP_CPU_LANE_P1 | <27> | | |
| FDI_TXN_0 | P33 | FDI_CTX_PRX_N0 | FDI_CTX_PRX_N0 | <16> | | |
| FDI_TXP_0 | R33 | FDI_CTX_PRX_P0 | FDI_CTX_PRX_P0 | <16> | | |
| FDI_TXN_1 | N32 | FDI_CTX_PRX_N1 | FDI_CTX_PRX_N1 | <16> | | |
| FDI_TXP_1 | P32 | FDI_CTX_PRX_P1 | FDI_CTX_PRX_P1 | <16> | | |

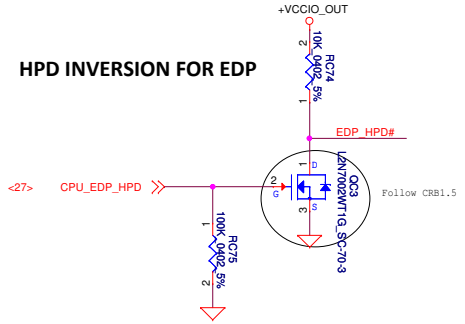
eDP

PAD~D T4 @

LOTES_AZIF0012-P002B_HASWELL

CONN@

## HPD INVERSION FOR EDP








| | | |
|---|---|---|
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| Title: CPU (4/7) | | |
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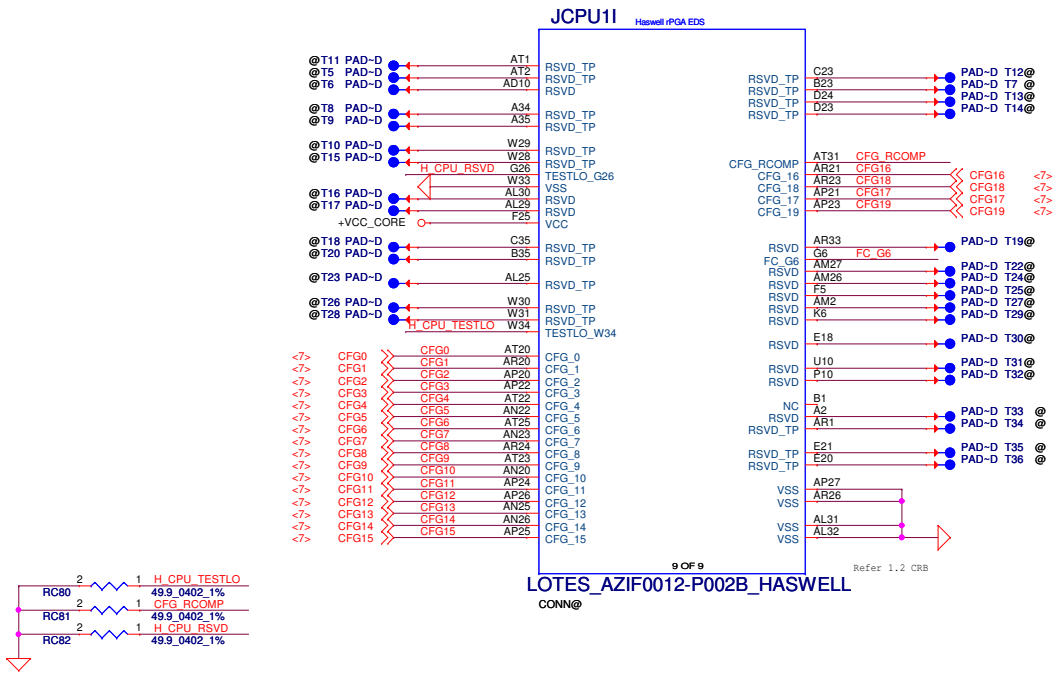
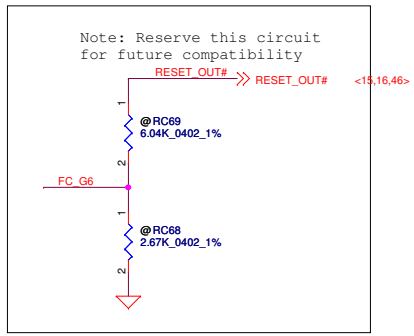
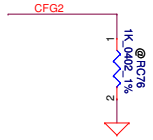
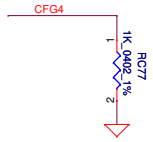
# CFG STRAPS for CPU



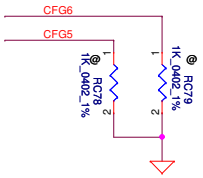



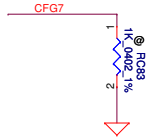

| PEG Static Lane Reversal - CFG2 is for the 16x | |
|---|---|
| CFG2 | 1:(Default) Normal Operation; Lane # definition matches socket pin map definition<br>0:Lane Reversed |




| Display Port Presence Strap | |
|---|---|
| CFG4 | 1 : Disabled; No Physical Display Port attached to Embedded Display Port<br>0 : Enabled; An external Display Port device is connected to the Embedded Display Port |




| PCIE Port Bifurcation Straps | |
|---|---|
| CFG[6:5] | 11: (Default) x16 - Device 1 functions 1 and 2 disabled<br>10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled<br>01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)<br>00: x8,x4,x4 - Device 1 functions 1 and 2 enabled |




| PEG DEFER TRAINING | |
|---|---|
| CFG7 | 1: (Default) PEG Train immediately following xxRESETB de assertion<br>0: PEG Wait for BIOS for training |



Compal Electronics, Inc.

| | | |
|---|---|---|
| Title | CPU (5/7) | |
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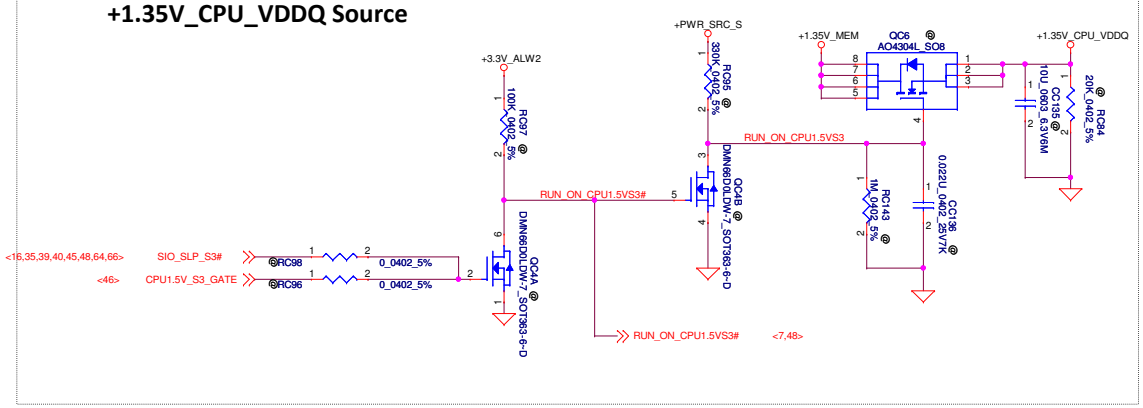
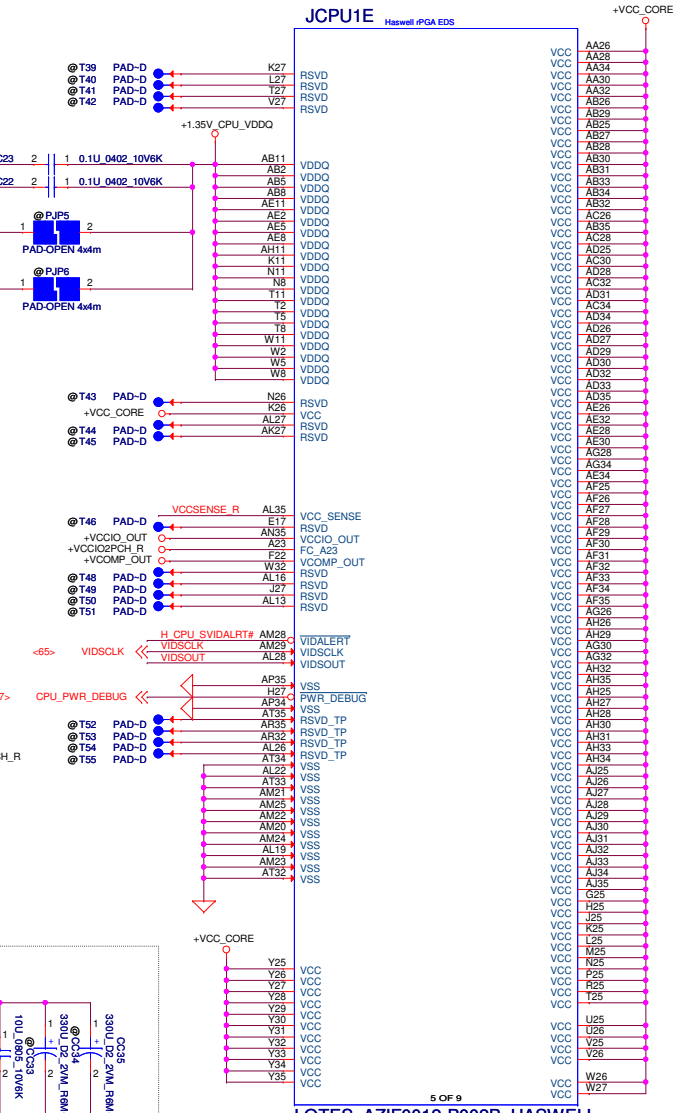
## +1.35V_CPU_VDDQ Source




## JCPU1E

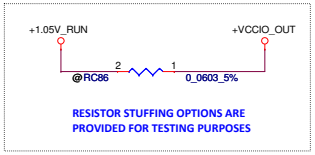
Haswell rPGA EDS

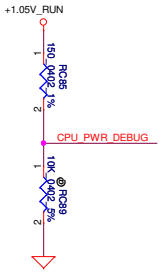



LOTES_AZIF0012-P002B_HASWELL

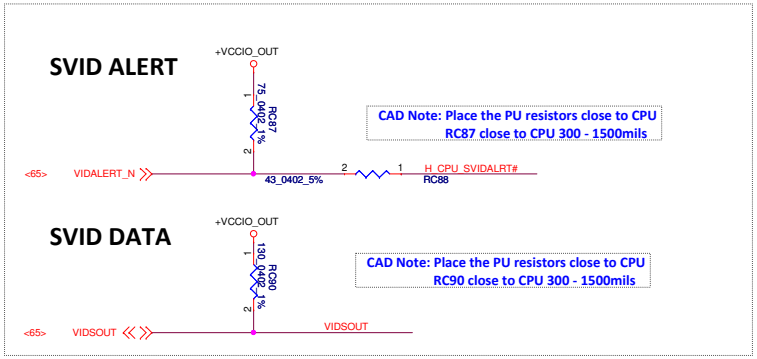
CONN@

## +1.05V_RUN / +VCCIO_OUT

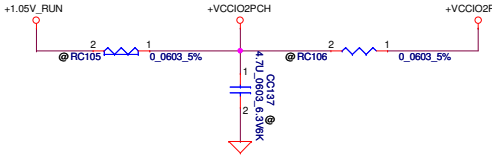


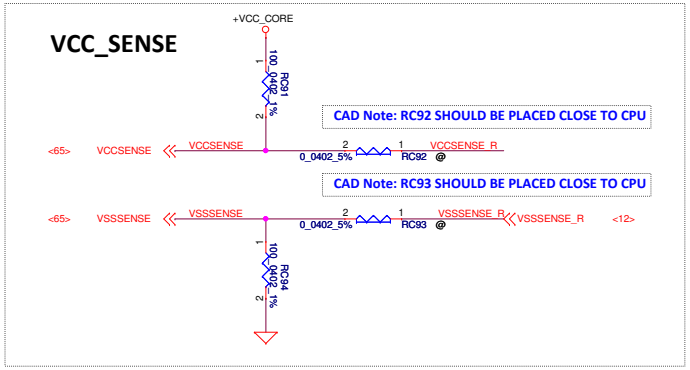

## SVID ALERT / SVID DATA



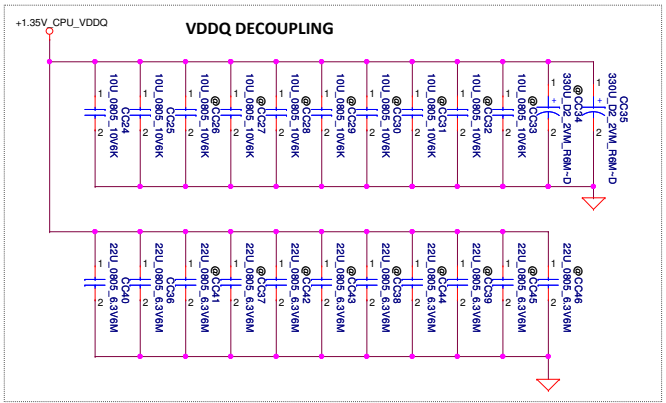

## +1.05V_RUN / +VCCIO2PCH / +VCCIO2PCH_R




## VCC_SENSE




## VDDQ DECOUPLING

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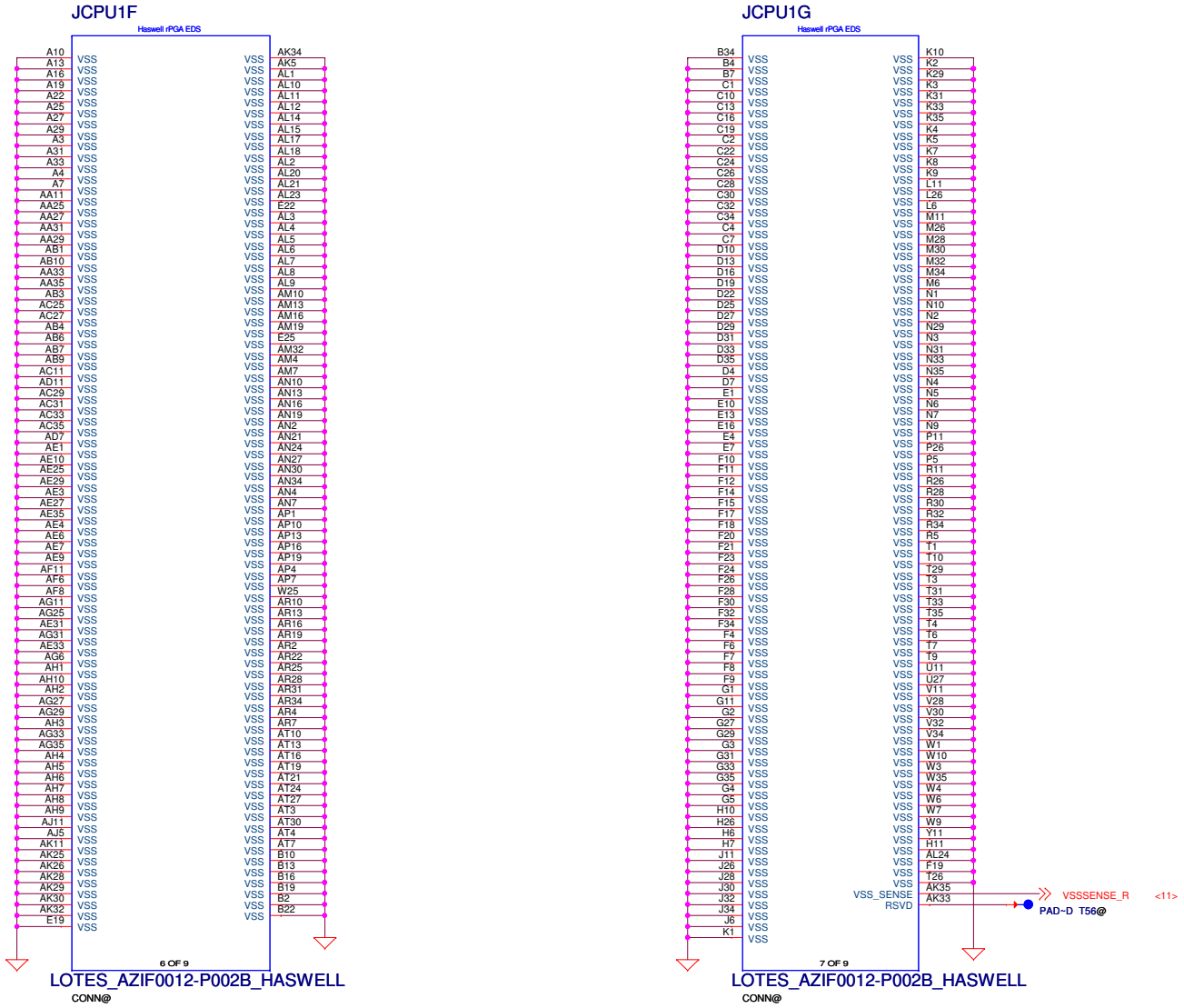
| | | |
|---|---|---|
| Compal Electronics, Inc. | | |
| Title: CPU (6/7) | | |
| Size | Document Number: LA-9411P | Rev: 1.0 |
| Date: Wednesday, April 10, 2013 | Sheet 11 of 77 | |

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Compal Electronics, Inc.

Title: CPU (7/7)

Size: | Document Number: LA-9411P | Rev: 1.0

Date: Wednesday, April 10, 2013 | Sheet 12 of 77

Populate RD1, De-Populate RD3 for Intel DDR3
VREFDQ multiple methods M1
Populate RD7, De-Populate RD1 for Intel DDR3
VREFDQ multiple methods M3

# JDIMM1 H=5.2mm

+V_DDR_REF, +SA_DIMM1_VREFDQ, +SA_DIMM_VREFDQ, +DIMM1_VREF_DQ
traces should be at least 20 mils wide and 20 mils spacing to other signals /planes.

Layout Note:
Place near JDIMM1

Layout Note:
Place near JDIMM1.203,204

All VREF traces should
have 10 mil trace width

+V_DDR_REF, +SM_VREF_DIMM, +DIMM1_VREF_CA,+SM_VREF, +DIMM1_VREF_CA
traces should be at least 20 mils wide and 20 mils spacing to other signals /planes.



Compal Electronics, Inc.

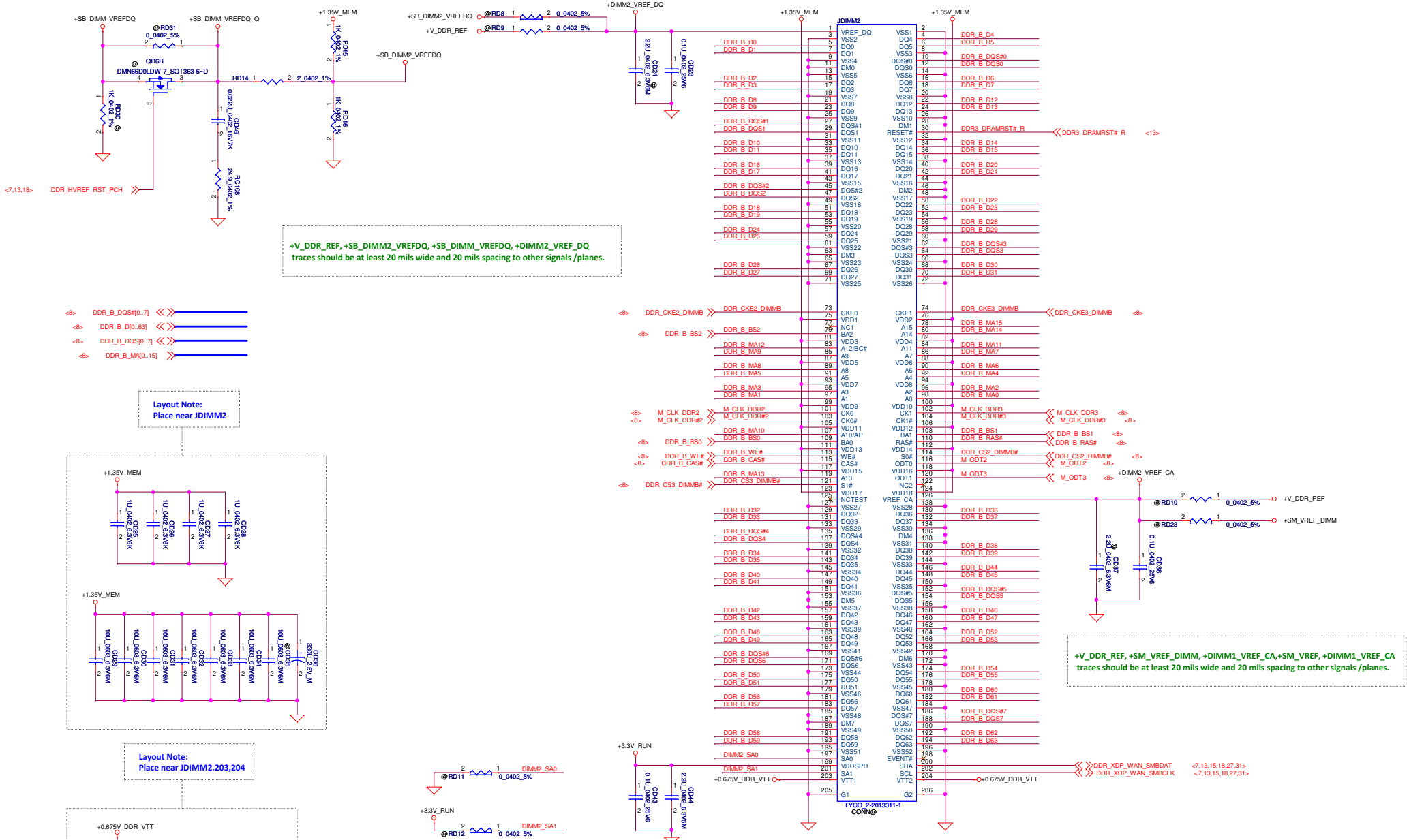
Title: DDRIII-SODIMM SLOT1

Size: | Document Number: LA-9411P | Rev: 1.0

Date: Wednesday, April 10, 2013 | Sheet 13 of 77

Populate RD4, De-Populate RD9 for Intel DDR3 VREFDQ multiple methods M1
Populate RD8, De-Populate RD8 for Intel DDR3 VREFDQ multiple methods M3

# JDIMM2 H=9.2mm



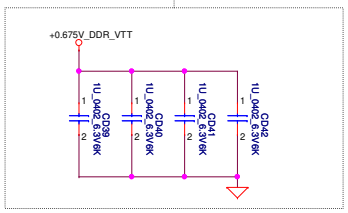

+V_DDR_REF, +SB_DIMM2_VREFDQ, +SB_DIMM_VREFDQ, +DIMM2_VREF_DQ traces should be at least 20 mils wide and 20 mils spacing to other signals /planes.

<8> DDR_B_DQS#[0..7]
<8> DDR_B_D[0..63]
<8> DDR_B_DQS[0..7]
<8> DDR_B_MA[0..15]

Layout Note:
Place near JDIMM2




Layout Note:
Place near JDIMM2.203,204




+V_DDR_REF, +SM_VREF_DIMM, +DIMM1_VREF_CA,+SM_VREF, +DIMM1_VREF_CA traces should be at least 20 mils wide and 20 mils spacing to other signals /planes.



| | | |
|---|---|---|
| Compal Electronics, Inc. | | |
| Title: DDRIII-SODIMM SLOT2 | | |
| Size | Document Number: LA-9411P | Rev: 1.0 |
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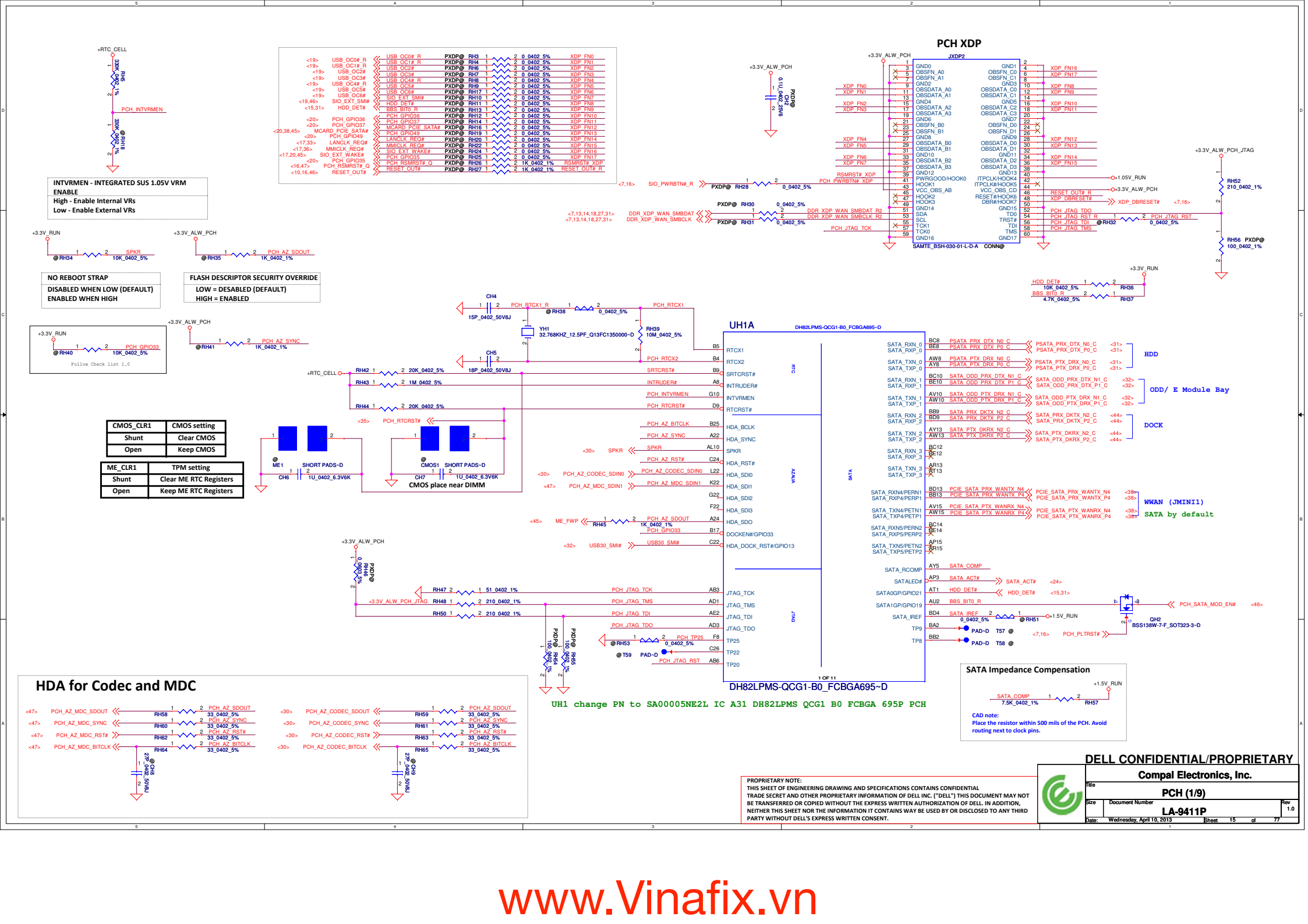

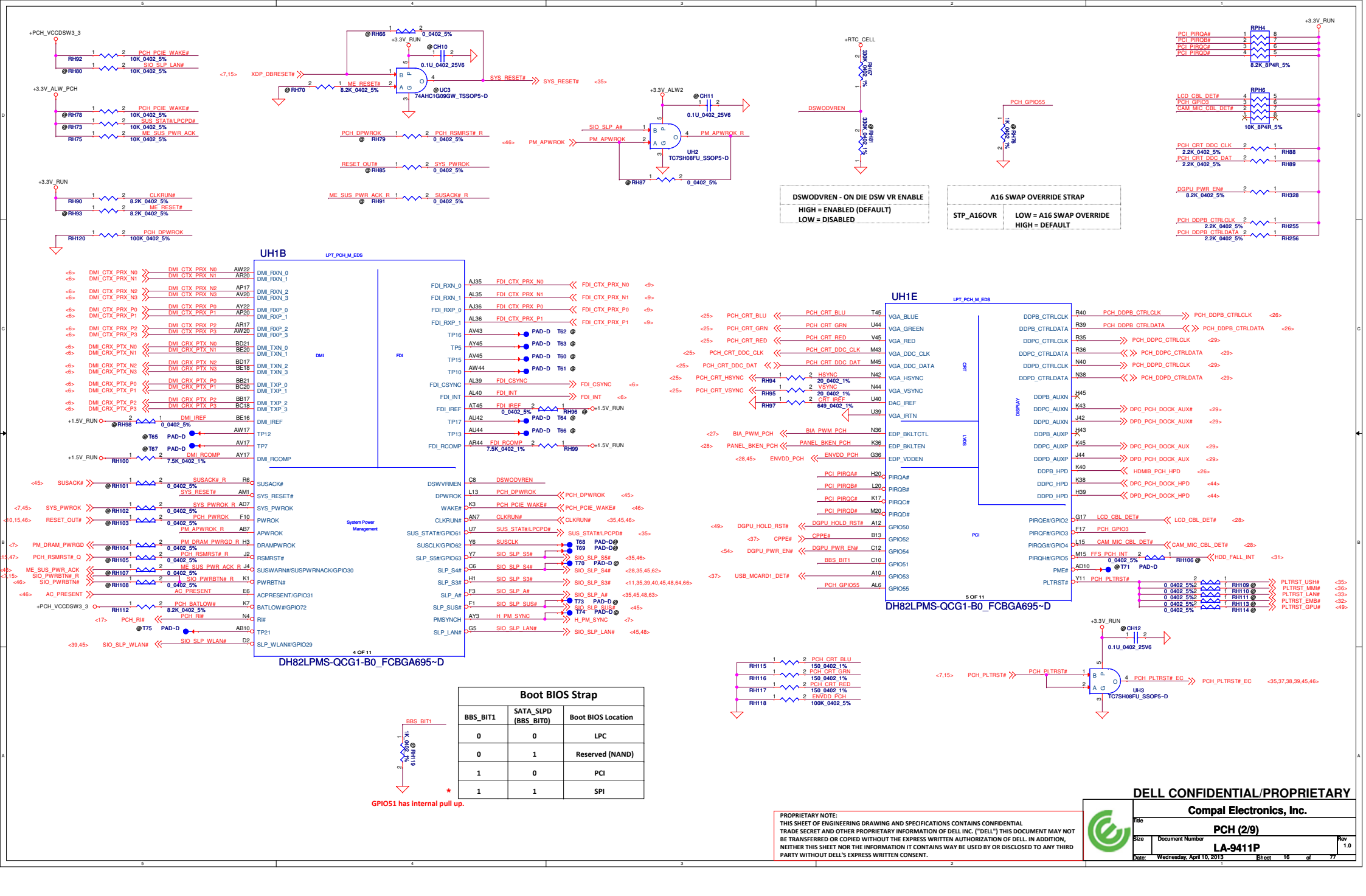

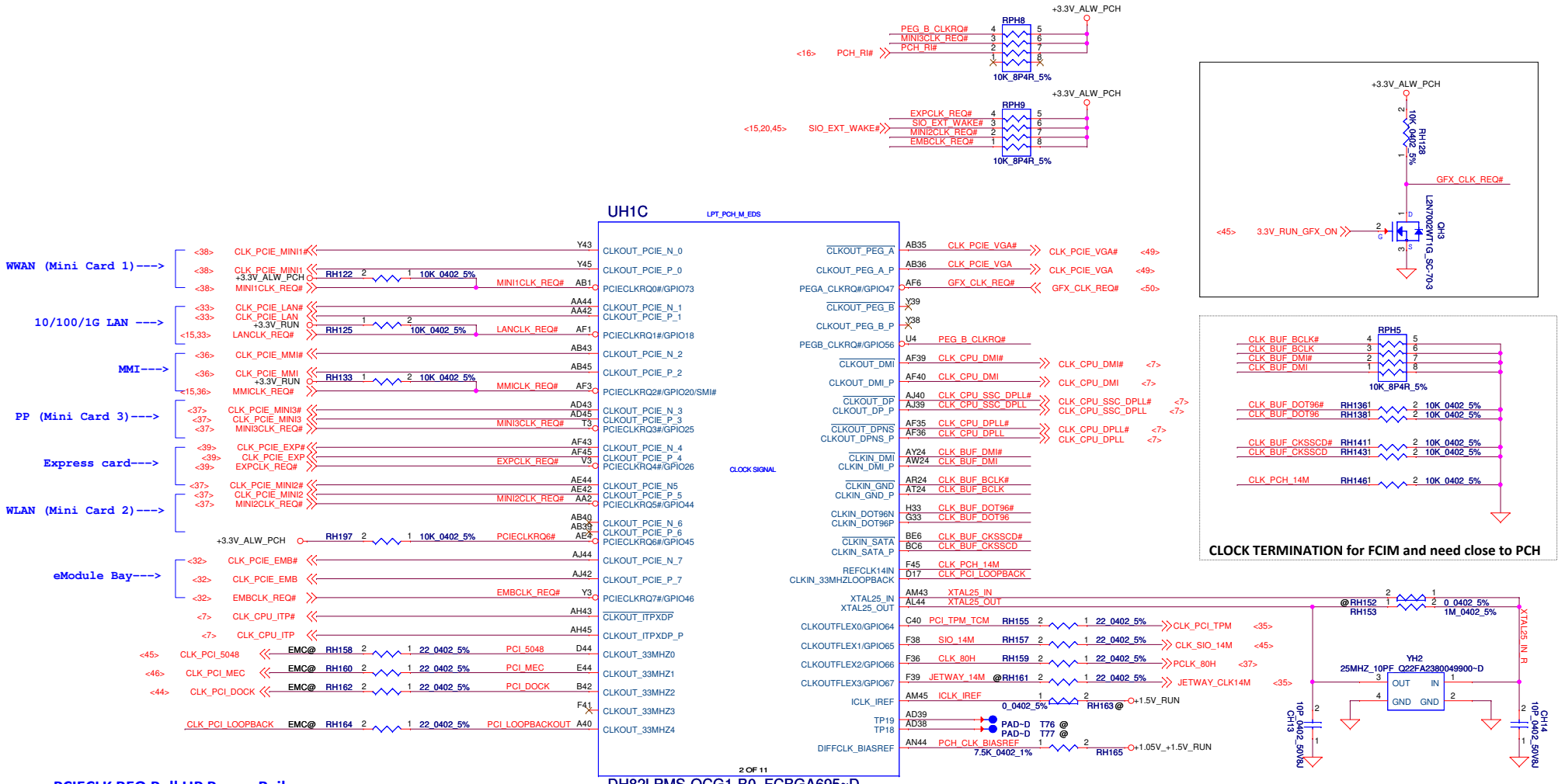


**PCIECLK REQ Pull UP Power Rail:**
**SUS Rail : 0 3 4 5 6 7**
**Core Rail: 1 2**

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| Size | Document Number: LA-9411P |
| Rev | 1.0 |
| Date: | Wednesday, April 10, 2013 |
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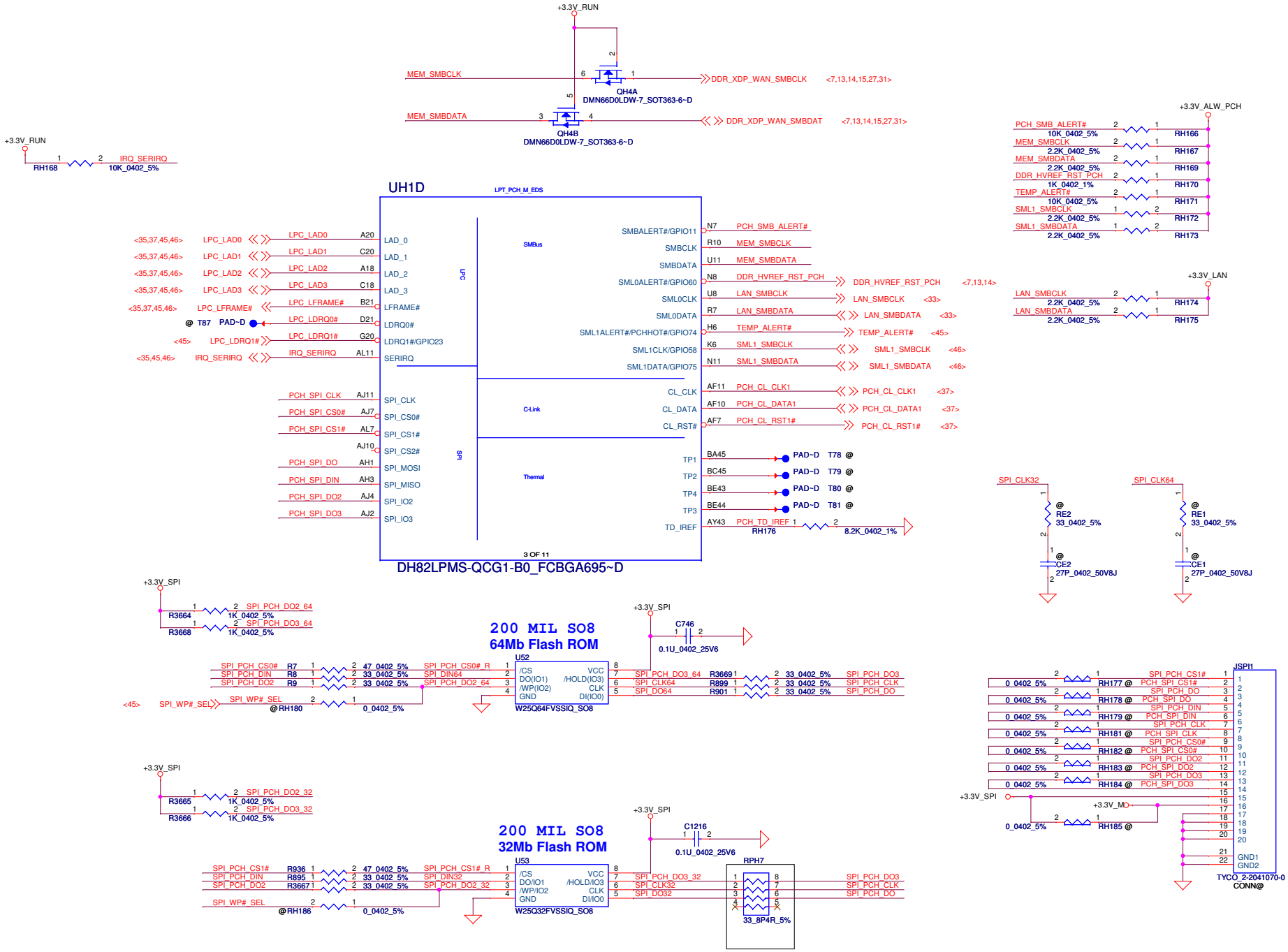
+3.3V_RUN
MEM_SMBCLK
DDR_XDP_WAN_SMBCLK <7,13,14,15,27,31>
QH4A
DMN66D0LDW-7_SOT363-6~D
MEM_SMBDATA
DDR_XDP_WAN_SMBDAT <7,13,14,15,27,31>
QH4B
DMN66D0LDW-7_SOT363-6~D
+3.3V_RUN
IRQ_SERIRQ
RH168
10K_0402_5%
+3.3V_ALW_PCH
PCH_SMB_ALERT# RH166 10K_0402_5%
MEM_SMBCLK RH167 2.2K_0402_5%
MEM_SMBDATA RH169 2.2K_0402_5%
DDR_HVREF_RST_PCH RH170 1K_0402_1%
TEMP_ALERT# RH171 10K_0402_5%
SML1_SMBCLK RH172 2.2K_0402_5%
SML1_SMBDATA RH173 2.2K_0402_5%
+3.3V_LAN
LAN_SMBCLK RH174 2.2K_0402_5%
LAN_SMBDATA RH175 2.2K_0402_5%
UH1D
LPT_PCH_M_EDS
LPC
LAD_0
LAD_1
LAD_2
LAD_3
LFRAME#
LDRQ0#
LDRQ1#/GPIO23
SERIRQ
SPI
SPI_CLK
SPI_CS0#
SPI_CS1#
SPI_CS2#
SPI_MOSI
SPI_MISO
SPI_IO2
SPI_IO3
SMBus
SMBALERT#/GPIO11
SMBCLK
SMBDATA
SML0ALERT#/GPIO60
SML0CLK
SML0DATA
SML1ALERT#/PCHHOT#/GPIO74
SML1CLK/GPIO58
SML1DATA/GPIO75
C-Link
CL_CLK
CL_DATA
CL_RST#
Thermal
TP1
TP2
TP4
TP3
TD_IREF
3 OF 11
DH82LPMS-QCG1-B0_FCBGA695~D
SPI_CLK32
SPI_CLK64
RE2 33_0402_5%
RE1 33_0402_5%
CE2 27P_0402_50V8J
CE1 27P_0402_50V8J
200 MIL SO8
64Mb Flash ROM
U52
W25Q64FVSSIQ_SO8
C746 0.1U_0402_25V6
200 MIL SO8
32Mb Flash ROM
U53
W25Q32FVSSIQ_SO8
C1216 0.1U_0402_25V6
RPH7
33_8P4R_5%
JSPI1
TYCO_2-2041070-0
CONN@
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Title
PCH (4/9)
Size
Document Number
LA-9411P
Rev
1.0
Date: Wednesday, April 10, 2013
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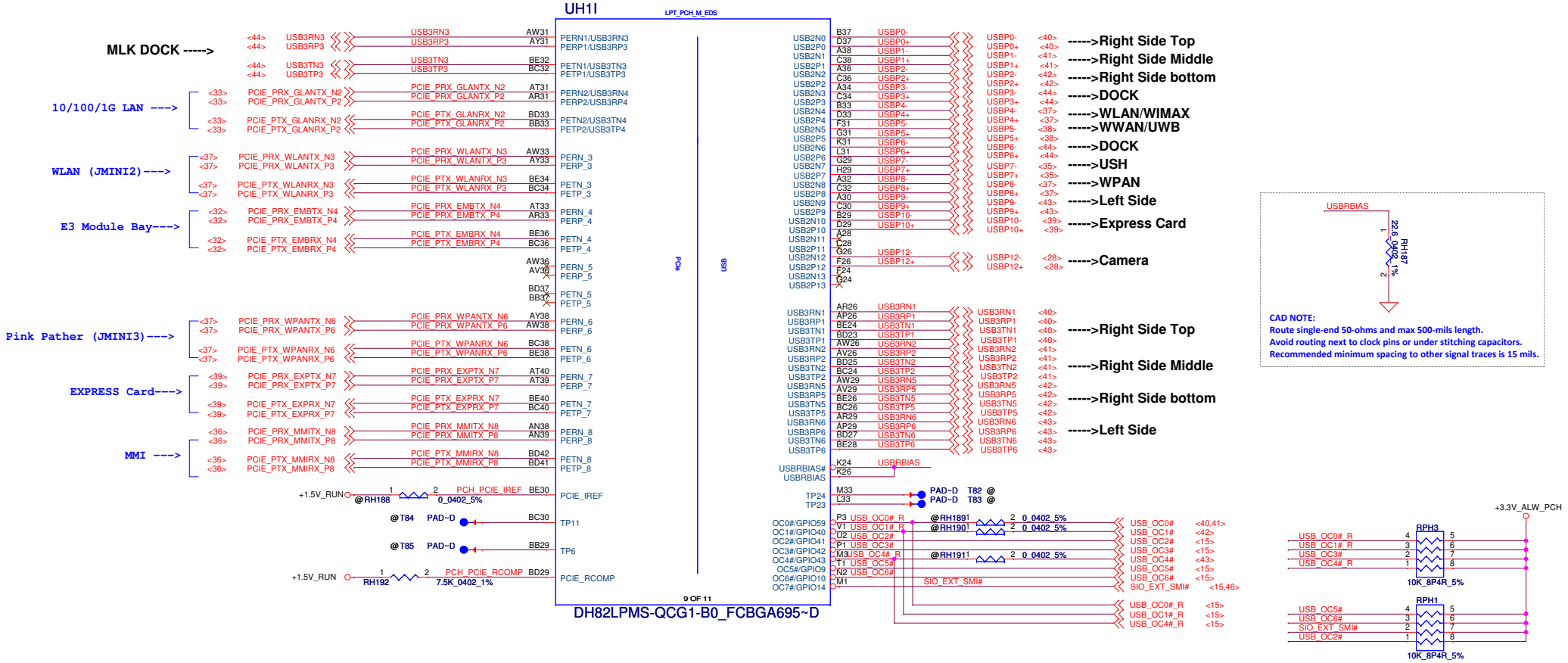






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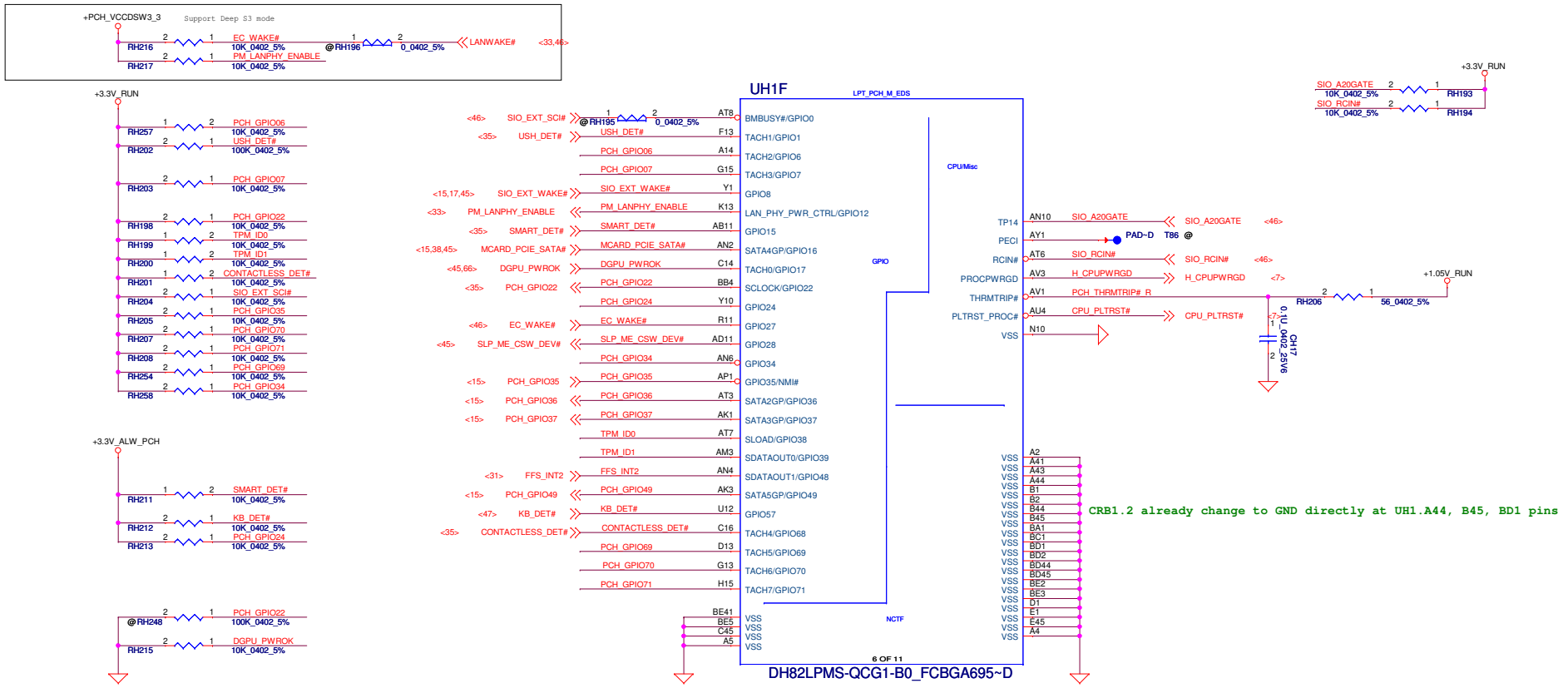
| Date: Wednesday, April 10, 2013 | Sheet 19 of 77 | |



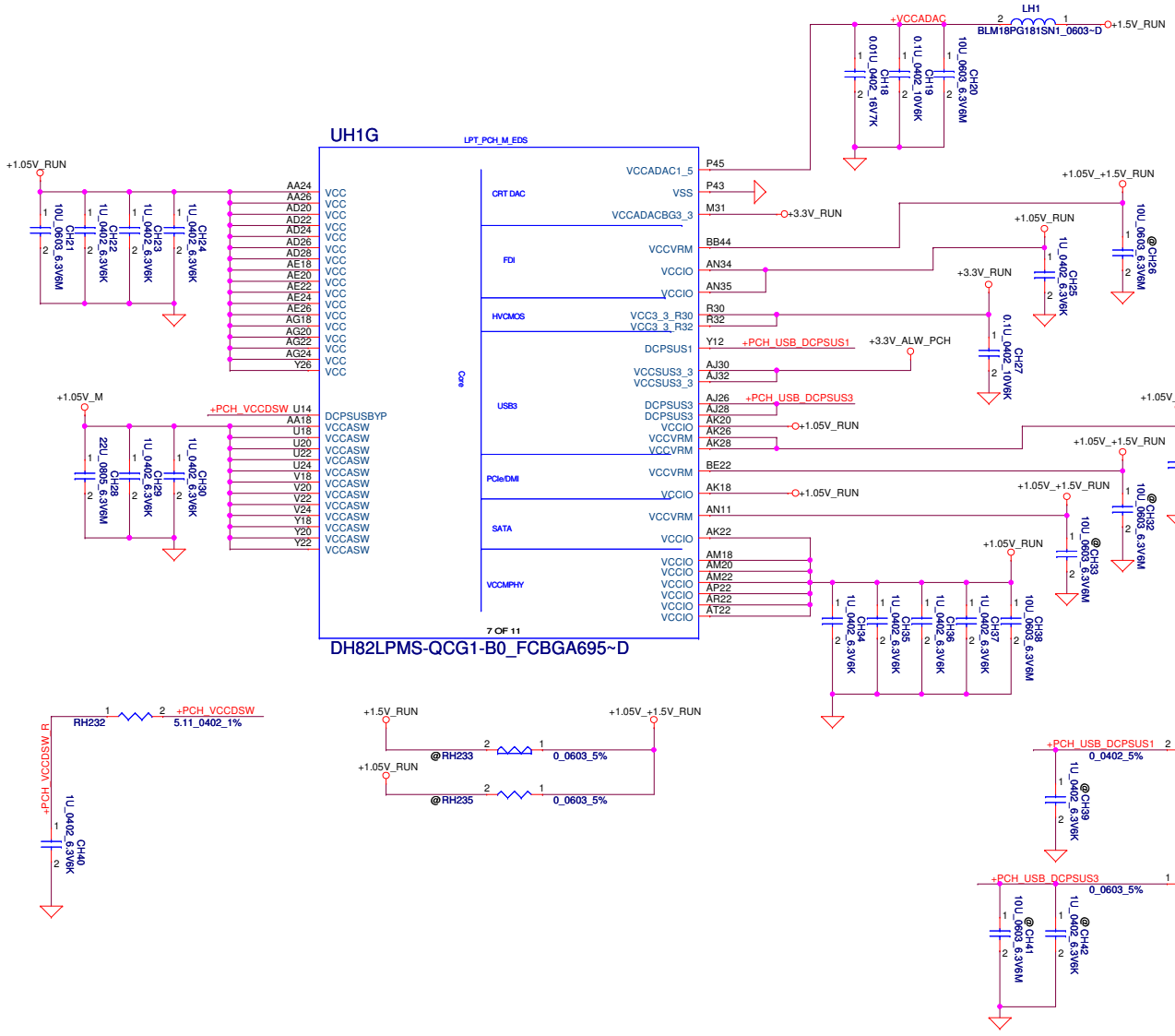

| PLL ON DIE VR ENABLE |
|---|
| ENABLED - HIGH(DEFAULT) |
| DISABLED - LOW |

| Config | GPIO16,49 |
|---|---|
| USB X4,PCIEX8,SATAX6 | 11 |
| * USB X6,PCIEX8,SATAX4 | 01 |

| Fixed Signals | | | | Muxed Signals | | Fixed Signals | | | | | | Muxed Signals | | Fixed Signals | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| USB3 1 | USB3 2 | USB3 5 | USB3 6 | PCIE 1 (00) | PCIE 2 (00) | PCIE 3 | PCIE 4 | PCIE 5 | PCIE 6 | PCIE 7 | PCIE 8 | SATA 4 (00) | SATA 5 (00) | SATA 0 | SATA 1 | SATA 2 | SATA 3 |
| | | | | USB3 3 (01) | USB3 4 (01) | | | | | | | PCIE 1 (01) | PCIE 2 (01) | | | | |



| Compal Electronics, Inc. | | |
|---|---|---|
| Title: PCH (6/9) | | |
| Size | Document Number: LA-9411P | Rev: 1.0 |
| Date: Wednesday, April 10, 2013 | Sheet 20 of 77 | |




| PCH Power Rail Table | | |
|---|---|---|
| Voltage Rail | Voltage | S0 Iccmax Current (A) |
| VCC | 1.05V | 1.29 A |
| VCCIO | 1.05V | 3.629 A |
| VCCADAC1_5 | 1.5V | 0.070 A |
| VCCADAC3_3 | 3.3V | 0.0133 A |
| VCCCLK | 1.05V | 0.306 A |
| VCCCLK3_3 | 3.3V | 0.055 A |
| VCCVRM | 1.5V | 0.179 A |
| VCC3_3 | 3.3V | 0.133 A |
| VCCASW | 1.05V | 0.67 A |
| VCCSUSHDA | 3.3V | 0.01 A |
| VCCSPI | 3.3V | 0.022 A |
| VCCSUS3_3 | 3.3V | 0.261 A |
| VCCDSW3_3 | 3.3V | 0.015 A |
| V_PROC_IO | 1.05V | 0.004 A |

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Title: PCH (7/9)

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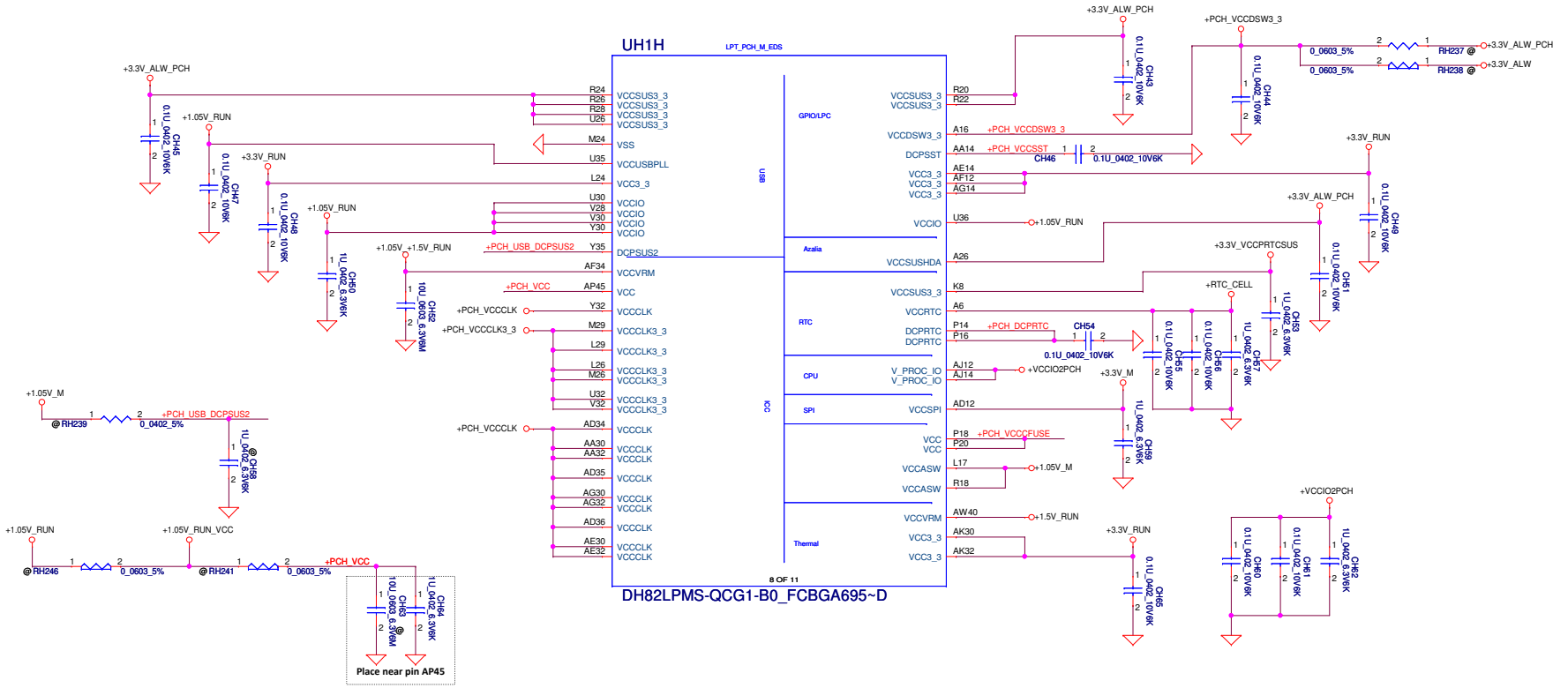
Support DEEP SX: populated RH238, de-populated RH237




## PCH Power Rail Table

| Voltage Rail | Voltage | S0 Iccmax Current (A) |
|---|---|---|
| VCC | 1.05V | 1.29 A |
| VCCIO | 1.05V | 3.629 A |
| VCCADAC1_5 | 1.5V | 0.070 A |
| VCCADAC3_3 | 3.3V | 0.0133 A |
| VCCCLK | 1.05V | 0.306 A |
| VCCCLK3_3 | 3.3V | 0.055 A |
| VCCVRM | 1.5V | 0.179 A |
| VCC3_3 | 3.3V | 0.133 A |
| VCCASW | 1.05V | 0.67 A |
| VCCSUSHDA | 3.3V | 0.01 A |
| VCCSPI | 3.3V | 0.022 A |
| VCCSUS3_3 | 3.3V | 0.261 A |
| VCCDSW3_3 | 3.3V | 0.015 A |
| V_PROC_IO | 1.05V | 0.004 A |



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Title: PCH (8/9)

Size | Document Number: LA-9411P | Rev: 1.0

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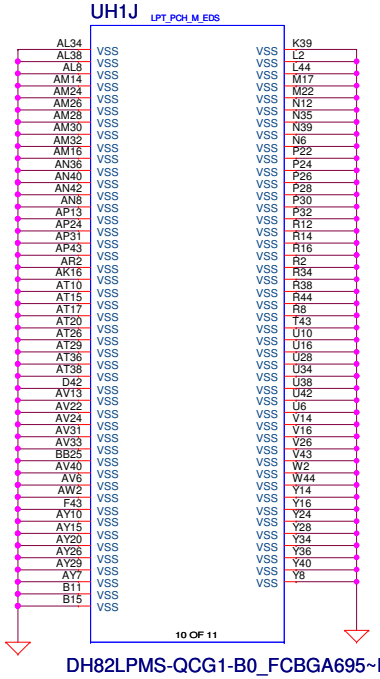


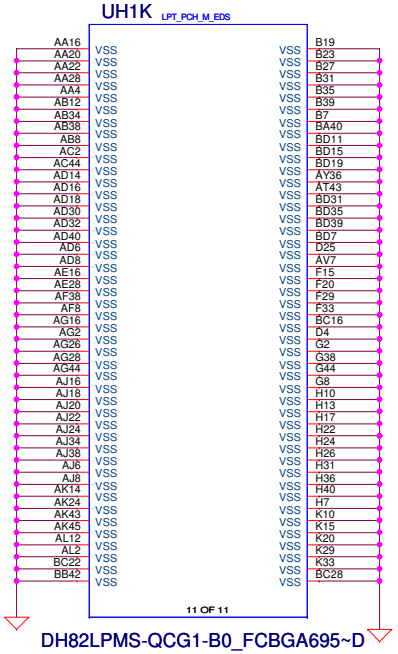






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Title: PCH (9/9)

Size | Document Number: LA-9411P | Rev: 1.0

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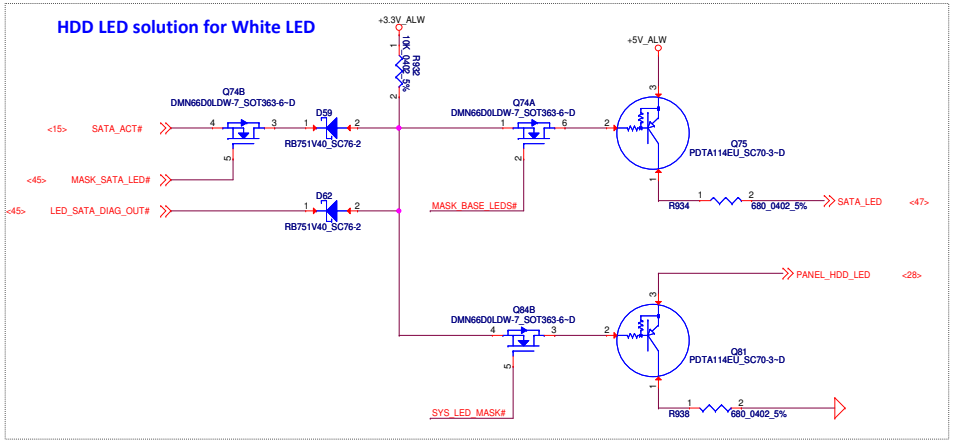
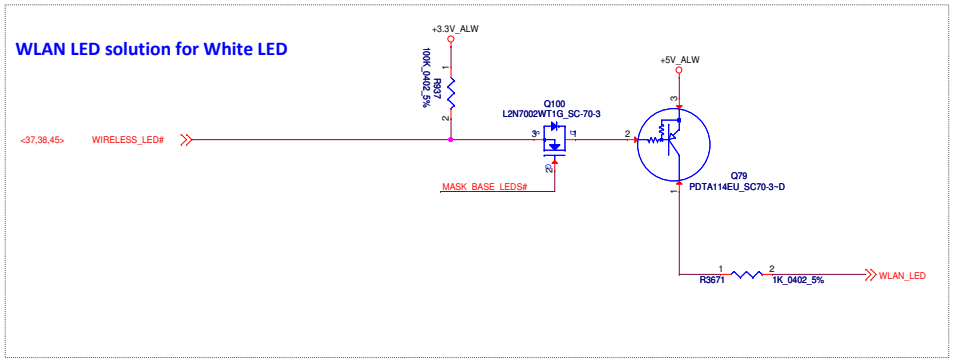
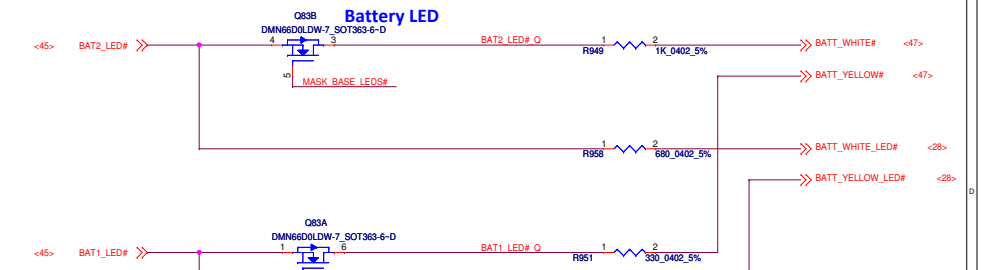
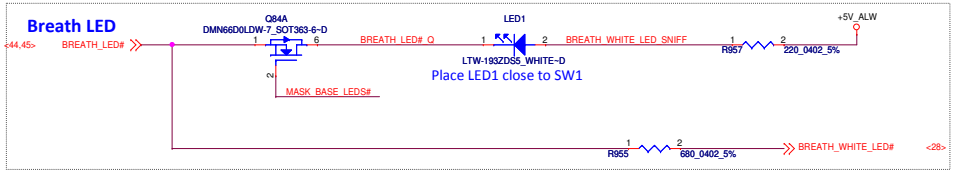
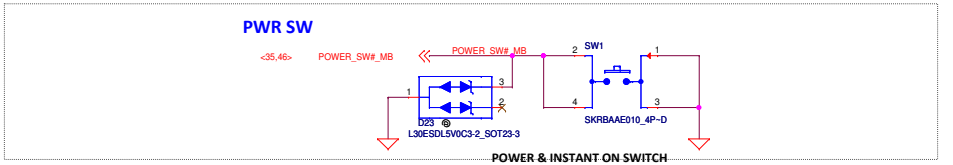
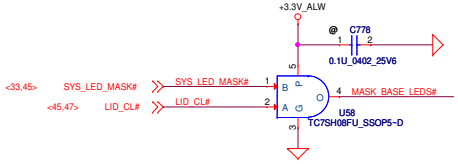


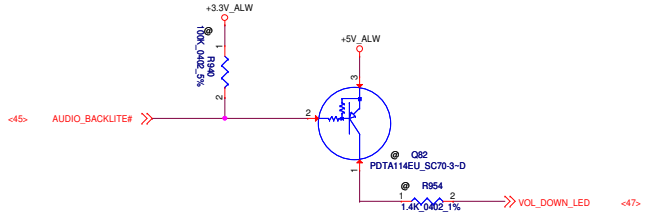



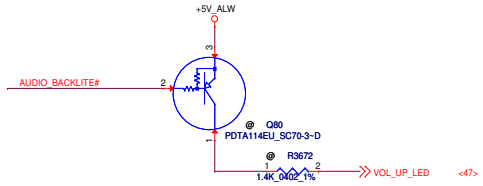



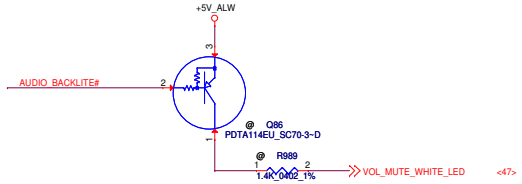



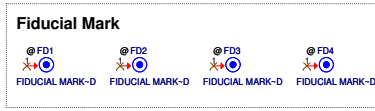



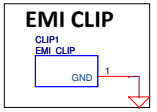



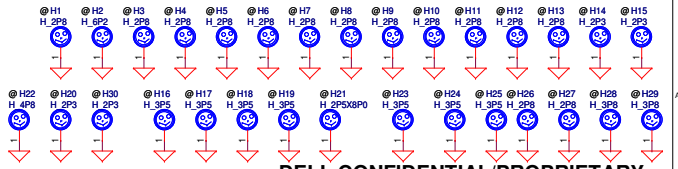





| LED Circuit Control Table | | |
|---|---|---|
| | SYS_LED_MASK# | LID_CL# |
| Mask All LEDs (Sniffer Function) | 0 | X |
| Mask Base MB LEDs (Lid Closed) | 1 | 0 |
| Do not Mask LEDs (Lid Opened) | 1 | 1 |

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| | |
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| Title | PWR SW/LED/PAD/ME |
| Size | Document Number: LA-9411P |
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| Date: | Wednesday, April 10, 2013 |
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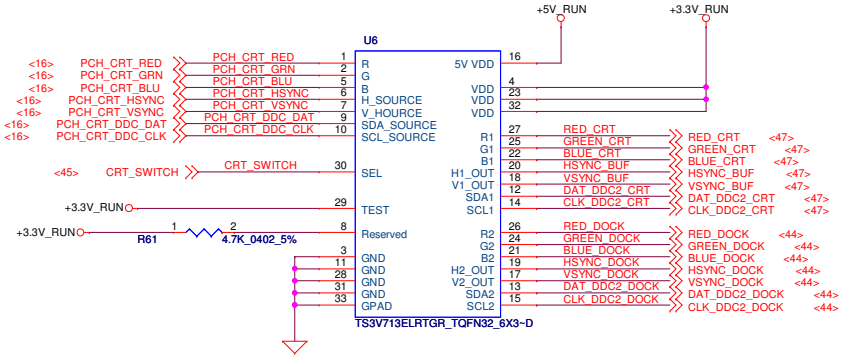
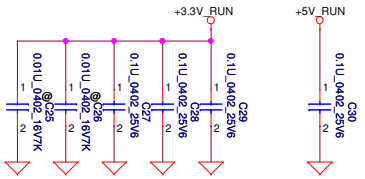
# SW for MB/DOCK




| SEL1/SEL2 | Chanel | Source |
|---|---|---|
| 0 | A=B1 | MB |
| 1 | A=B2 | APR/SPR |







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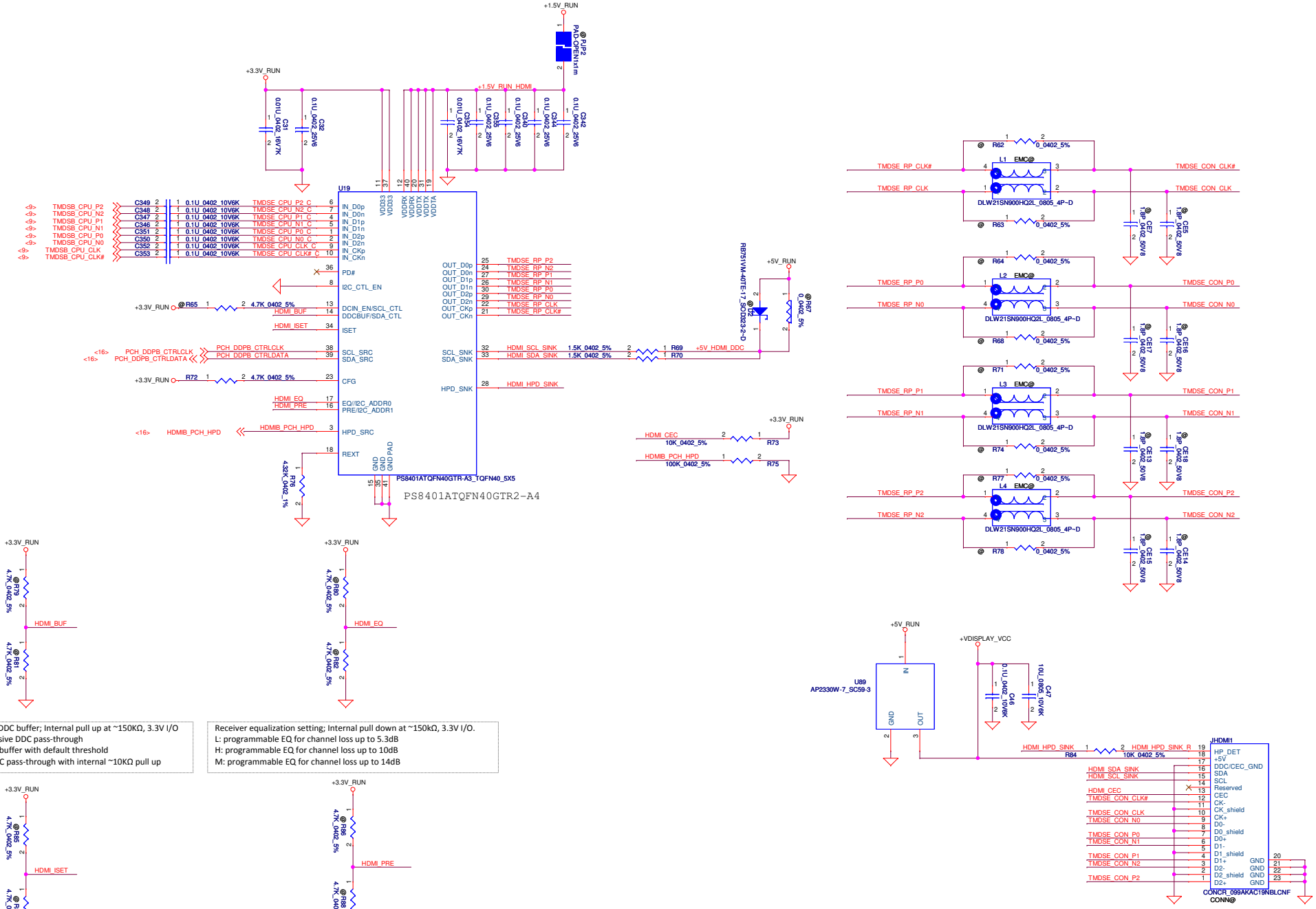
Title: CRT SW
Size: | Document Number: LA-9411P | Rev: 1.0
Date: Wednesday, April 10, 2013 | Sheet 25 of 77



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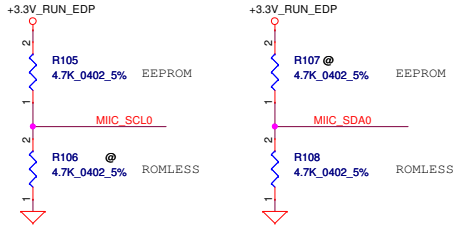
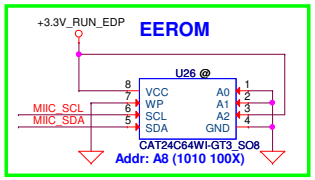
Compal Electronics, Inc.

Title: HDMI CONN

Size: | Document Number: LA-9411P | Rev: 1.0

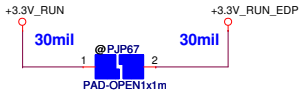
Date: Wednesday, April 10, 2013 | Sheet 26 of 77

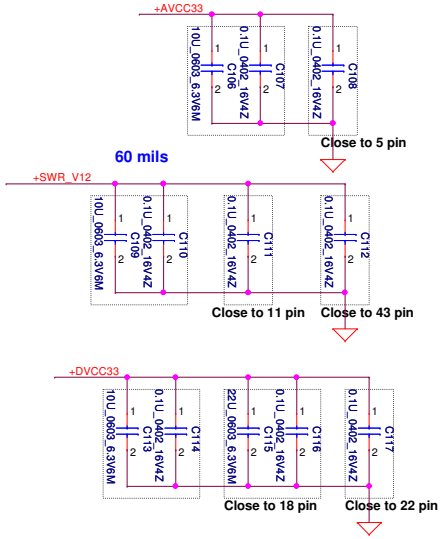


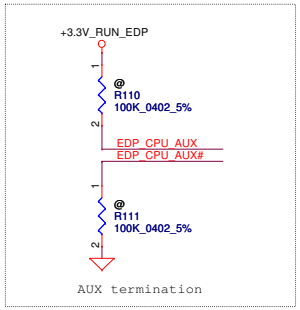



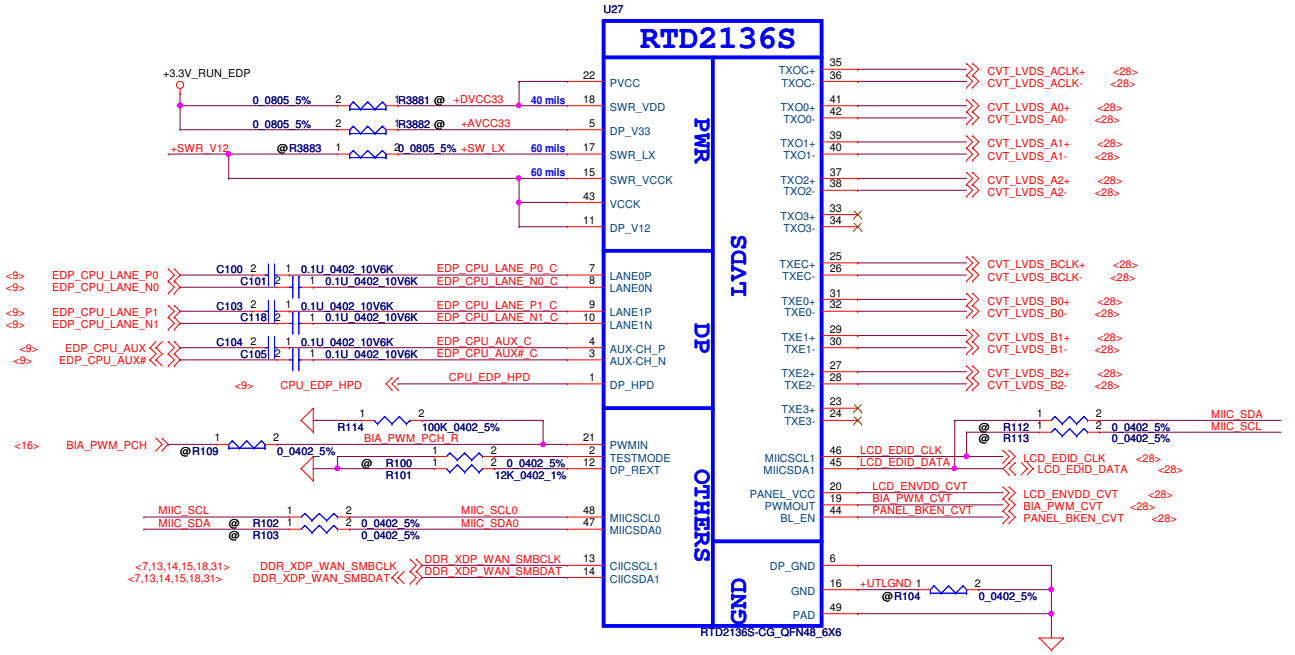

**Power Consumption:**

**Pin5 (DPV33) < 20mA**
**Pin 11 (DPV12) < 100mA**
**Pin 15 (SWR_VCCK) < 100mA (layout trace > 60 mil)**
**Pin 17 (SWR_LX) < 600mA (layout trace > 60 mil)**
**Pin 18 (SWR_VDD) < 200mA (layout trace > 40 mil)**
**Pin 22 (PVCC) < 50 mA**
**Pin 43 (VCCK) < 50mA**




Symbol need to update

**1. RTD2136S:SA00004NW10 Populated R102, R103, R107; De-populated R108**
***** 2. RTD2136R SA000067100 : De-Populated R102, R103, R107; Populate R108;**





Compal Electronics, Inc.

Title: eDP to LVDS CONVERTER

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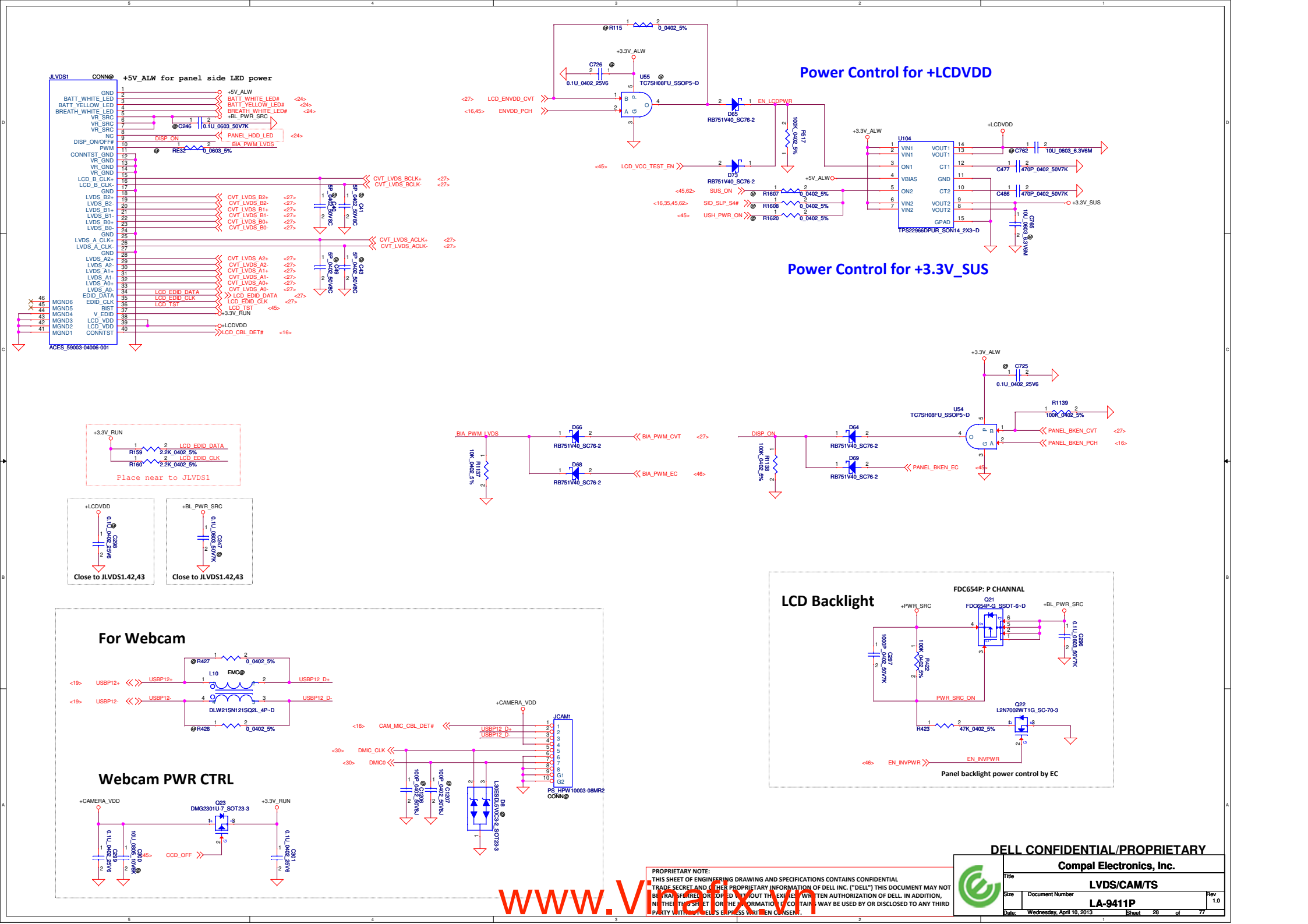
+5V_ALW for panel side LED power
JLVDS1
CONN@
ACES_59003-04006-001
Power Control for +LCDVDD
Power Control for +3.3V_SUS
U104
TPS22966DPUR_SON14_2X3-D
U54
TC7SH08FU_SSOP5-D
U55
TC7SH08FU_SSOP5-D
Place near to JLVDS1
Close to JLVDS1.42,43
Close to JLVDS1.42,43
For Webcam
Webcam PWR CTRL
LCD Backlight
FDC654P: P CHANNAL
Q21
FDC654P-G_SSOT-6-D
Q22
L2N7002WT1G_SC-70-3
Q23
DMG2301U-7_SOT23-3
JCAM1
PS_HPW10003-08MR2
CONN@
Panel backlight power control by EC
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Compal Electronics, Inc.
LVDS/CAM/TS
LA-9411P
Wednesday, April 10, 2013
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PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.
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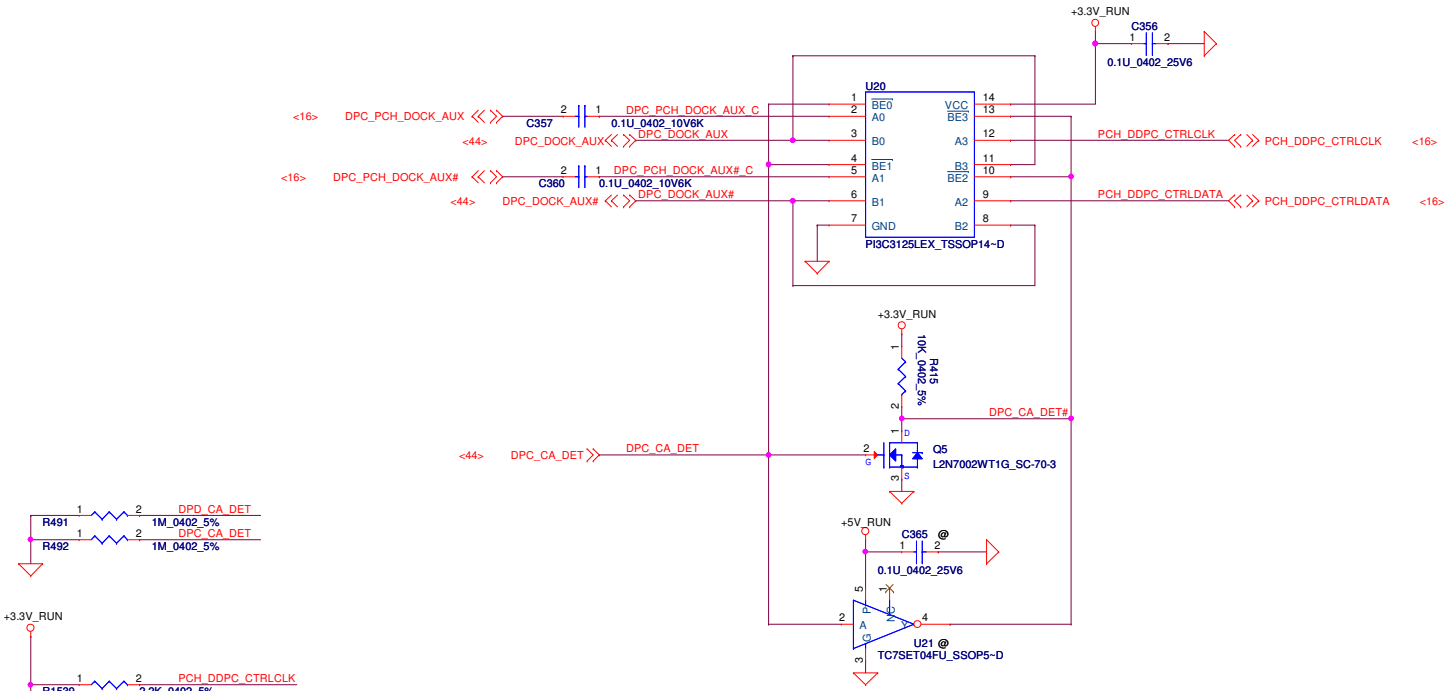
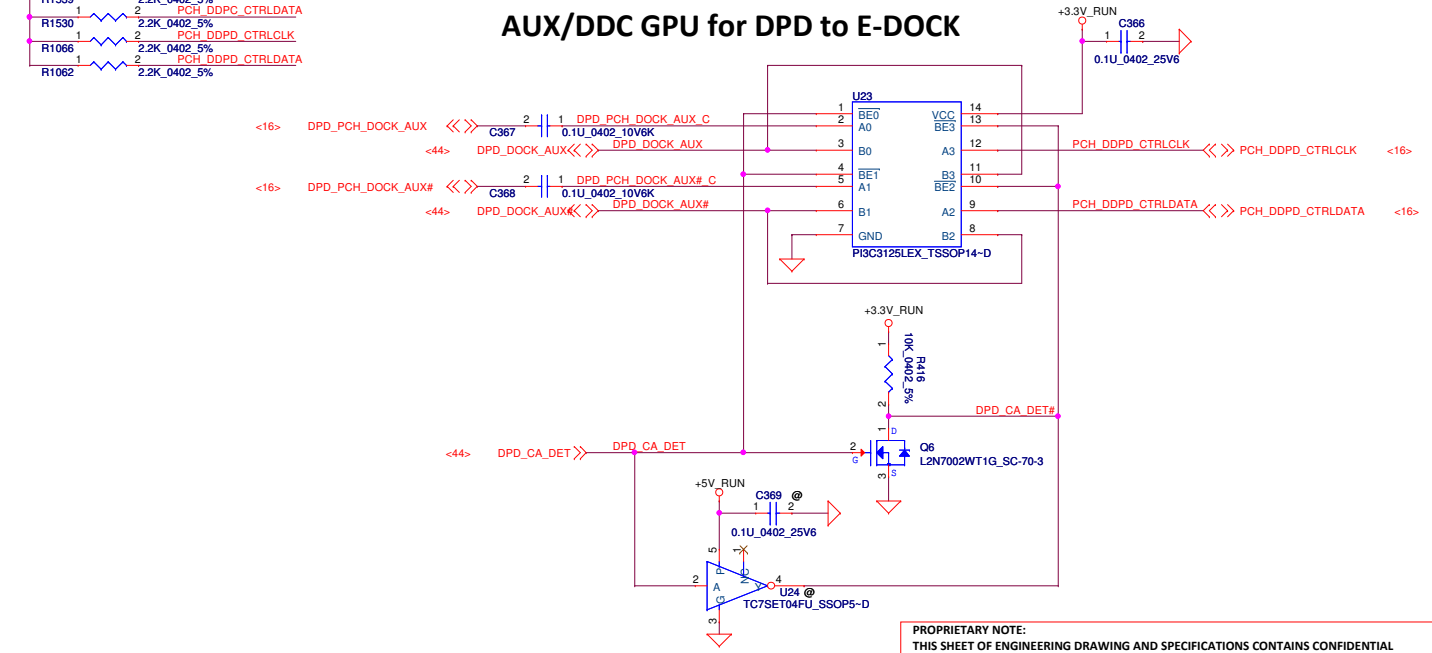
# AUX/DDC GPU for DPC to E-DOCK




# AUX/DDC GPU for DPD to E-DOCK

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| | | |
|---|---|---|
| Compal Electronics, Inc. | | |
| Title: DP SW | | |
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# Internal Speakers Header

INT_SPK_L+, INT_SPKL_L+ :40 mils trace, keep 10mils spacing
INT_SPK_L-, INT_SPKL_L- :40 mils trace, keep 10mils spacing
INT_SPK_R+, INT_SPKR_R+ :40 mils trace, keep 10mils spacing
INT_SPK_R-, INT_SPKR_R- :40 mils trace, keep 10mils spacing
INT_SPK_L-, INT_SPKL_L- with INT_SPK_R+, INT_SPKR_R+ keep 20mils spacing

INT_SPK_L+ EMC@ L113 PBY160808T-300Y-N_2P INT_SPKL_L+
INT_SPK_L- EMC@ L114 PBY160808T-300Y-N_2P INT_SPKL_L-
INT_SPK_R+ EMC@ L115 PBY160808T-300Y-N_2P INT_SPKR_R+
INT_SPK_R- EMC@ L116 PBY160808T-300Y-N_2P INT_SPKR_R-
JSPK1 GND GND
ACES_50279-0040N-001 CONN@

Need to Link CIS

C973 100P_0402_50V7K
C974 100P_0402_50V7K
C975 100P_0402_50V7K
C976 100P_0402_50V7K
R1680 0_0402_5%
R1681 0_0402_5%
R1682 0_0402_5%
R1683 0_0402_5%

Close to U74

DVDD_IO should match with HDA Bus level

+3.3V_RUN PJP60 JUMP_43X79
+3.3V_RUN_DVDD C962 1U_0603_10V6K C964 0.1U_0402_25V6
+3.3V_RUN_DVDD C963 0.1U_0402_25V6 C965 10U_0805_10V6K
+DVDD_CORE C954 10U_0805_10V6K

U74 ALC3226-CG_QFN48_7X7
DREG_OUT DVDD-IO DVDD BIT-CLK SDATA-OUT SYNC SDATA-IN RESET# I2S_MCLK I2S_SCLK I2S_DOUT I2S_LRCK I2S_DIN MIC1-L MIC1-R EAPD/PD DVSS PVSS GND
AVDD1 AVDD2/HVDD(3.3) PVDD2 PVDD1 Sense A Sense B LINE1-L/RING2 LINE1-R/SLEEVE LINE1-VREFO HPOUT-L/MIC-CAP AVSS2/HPOUT-L HP-OUT-R SPK-L+ SPK-L- SPK-R+ SPK-R- PCBEEP GPIO0/DMIC-CLK GPIO1/DMIC-DATA DMIC1/GPIO2 GPIO3 MONO-OUT/CBP CBN CBP/AVSS2 LDO-CAP JDREF CPVEE VREF MIC1-VREFO AVSS1

<15> PCH_AZ_CODEC_BITCLK PCH_AZ_CODEC_BITCLK
<15> PCH_AZ_CODEC_SDOUT PCH_AZ_CODEC_SDOUT
<15> PCH_AZ_CODEC_SYNC
Place R1096 close to codec
<15> PCH_AZ_CODEC_SDIN0 R1096 22_0402_5% PCH_AZ_SDIN0_R
<15> PCH_AZ_CODEC_RST# PCH_AZ_CODEC_RST#

<44> DAI_12MHZ# DAI_12MHZ# R1654 22_0402_5% I2S_MCLK
<44> DAI_BCLK# DAI_BCLK# R1668 22_0402_5% I2S_BCLK
<44> DAI_DO# DAI_DO# R1097 33_0402_5% I2S_DO
<44> DAI_LRCK# DAI_LRCK#
<44> DAI_DI DAI_DI
C986 22P_0402_50V8J
C987 22P_0402_50V8J

BCLK: Audio serial data bus bit clock input/output
LRCK: Audio serial data bus word clock input/output

MIC1_L MIC1_R
<45> AUD_NB_MUTE# AUD_NB_MUTE# R1099 10K_0402_5% C967 1U_0603_10V6K

place close to pin27
+VDDA_AVDD C957 0.1U_0402_25V6 C955 10U_0805_10V6K
L77 BLM21PG600SN1D_0805-D +5V_RUN
C968, C956 place close to pin38
PJP80 PAD-OPEN1x1m +3.3V_RUN
C959, C958 place close to pin39
C958 10U_0805_10V6K C959 0.1U_0402_25V6 C960 0.1U_0402_25V6 C961 10U_0805_10V6K
C961, C960 place close to pin45
+5V_RUN PAD-OPEN1x1m PJP81

+VDDA_AVDD2 +VDDA_PVDD AUD_SENSE_A AUD_SENSE_B RING2 SLEEVE +VREFOUT
C969 2 10U_0805_10V6K
AUD_HP_OUT_L AUD_HP_OUT_R
INT_SPK_L+ INT_SPK_L-
INT_SPK_R+ INT_SPK_R-
AUD_PC_BEEP
C989 place close to pin2
C989 22P_0402_50V8J
DMIC_CLK_L EMC@ LE3 BLM18BB221SN1D_2P DMIC_CLK DMIC0 <28>
Place LE3 close to codec
R169 0_0402_5% EN_I2S_NB_CODEC# EN_I2S_NB_CODEC# <45>
C962 2.2U_0603_16V6K
+MIC1_VREF_OUT
C1107 0.1U_0402_25V6
C1214 2.2U_0603_16V6K
C965 2.2U_0603_16V6K
R1642 20K_0402_1%
C963 10U_0805_10V6K

C1105 0.1U_0402_25V6 R1119 100K_0402_5% SPKR <15>
C1106 0.1U_0402_25V6 R1120 100K_0402_5% BEEP <46>
R1141 10K_0402_5%
R1142 10K_0402_5%

SLEEVE and RING2 Routing 40 mils.

Close to U74 pin5
PCH_AZ_CODEC_SDOUT
R1077 47_0402_5%
C978 0.1U_0402_10V6K

Close to U74 pin6
PCH_AZ_CODEC_BITCLK
R1076 33_0402_5%
C977 10P_0402_50V8J

When no external power, it Sleeve will be floating mode and no reference GND.

+RTC_CELL
R1084 100K_0402_5%
SLEEVE
PCH_AZ_CODEC_RST# R39 0_0402_5%
AUD_NB_MUTE# R40 0_0402_5%
Q327A Q327B DMN66D0LDW-7_SOT363-6-D
C970 1U_0603_10V6K

place at AGND and DGND plane
R5 0_0402_5%
R6 0_0402_5%
R15 0_0402_5%

place at Codec bottom side
PJP62 PAD-OPEN1x1m

support universal Jack
MIC1_L C195 4.7U_0603_6.3V6K MIC1_L_C R198 1K_0402_5% AUD_HP_OUT_L1
MIC1_R C196 4.7U_0603_6.3V6K MIC1_R_C R199 1K_0402_5% AUD_HP_OUT_R1
RB751VM-40TE17_SOD323-2-D D11 D12
R209 4.7K_0402_5%
R210 4.7K_0402_5%

SLEEVE R1145 2.2K_0402_5%
RING2 R1146 2.2K_0402_5%
+VREFOUT

AUD_SENSE_A
Place closely to Pin 13.
R1086 39.2K_0402_1%
base E-team detect issue , reserve RC to delay time
Q324 L2N7002DW1T1G_SC-70-3
AUD_HP_NB_SENSE
C972 0.1U_0402_25V6
C1247 10U_0805_10V6K

Add for solve pop noise and detect issue
Place closely to Pin 14
AUD_SENSE_B
+3.3V_RUN
R1079 39.2K_0402_1%
R1080 20K_0402_1%
R1081 100K_0402_5%
R1082 100K_0402_5%
<45> DOCK_HP_DET
Q106A Q106B DMN66D0LDW-7_SOT363-6-D
DOCK_MIC_DET <45>

Symbol need update
RING2 AUD_HP_OUT_L R1677 9.1_0402_1% AUD_HP_OUT_L1
AUD_HP_OUT_R SLEEVE R1679 9.1_0402_1% AUD_HP_OUT_R1
R54 R56 R57 R58 0_0603_5%

+3.3V_RUN R1100 10K_0402_5%

## Combo Jack

Normal
Open

JHP1 SINGA_2SJ3080-001111F CONN@
RING2_L AUD_HP_OUT_L2 AUD_HP_NB_SENSE AUD_HP_OUT_R2 EXT_MIC
C1211 220P_0402_50V7K
C1212 220P_0402_50V7K
C1213 220P_0402_50V7K
C1215 220P_0402_50V7K
R1676 0_0402_5%
D32 D33 D31 L03SD5.0VXCS2-2_SOT23-3
EMC@
R1088 100K_0402_5%
AUD_HP_NB_SENSE <45>

RING2_L, RING2, AUD_HP_OUT_L2, AUD_HP_OUT_L1, AUD_HP_OUT_L, AUD_HP_OUT_R2, AUD_HP_OUT_R1, AUD_HP_OUT_R, EXT_MIC, SLEEVE Trace width to 15mils.

| Resistor | SENSE_A | SENSE_B |
|---|---|---|
| 39.2K | PORT A | PORT E |
| 20K | PORT B | PORT F |
| 10K | NA | DMIC0 |
| 5.11K | SPDIFOUT0 | SPDIFOUT1 (DMIC1) |
| 2.49K | Pull-up to AVDD | |

| | |
|---|---|
| PORT A | External MIC |
| PORT B | HeadPhone Out |
| PORT C | Dock Audio |
| PORT D | Internal SPK |

Notes:
Keep PVDD supply and speaker traces routed on the DGND plane.
Keep away from AGND and other analog signals



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Title: Codec
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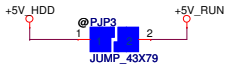
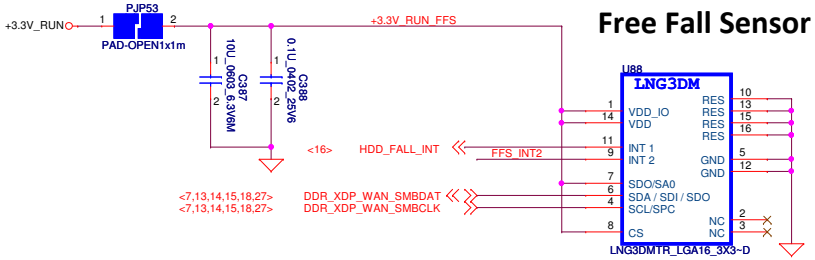
## HDD PWR

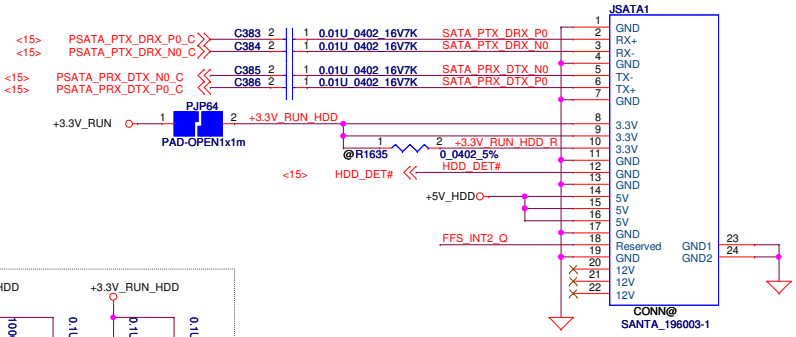



SHORT DEFAULT

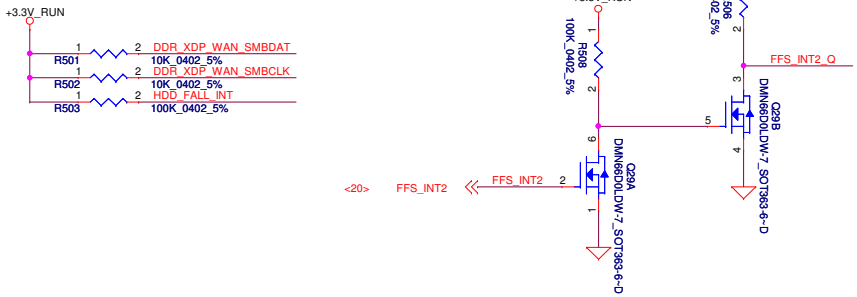
## Free Fall Sensor

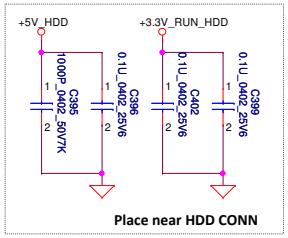


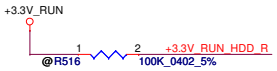

## HDD CONN




Main SATA +5V Default







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Title: HDD
Size: Document Number: LA-9411P
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Date: Wednesday, April 10, 2013
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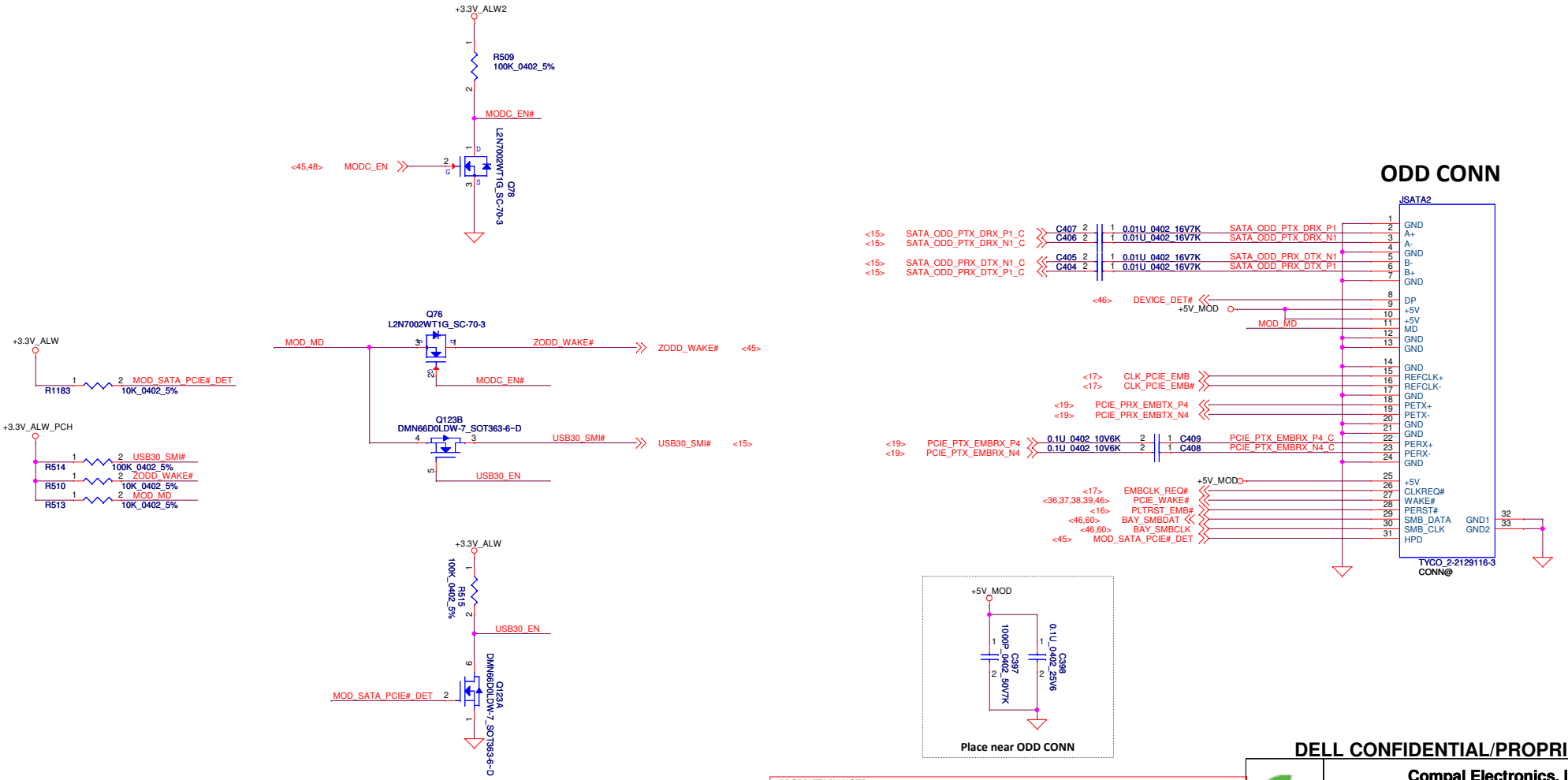


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| | | |
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| Title: ODD | | |
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| Date: Wednesday, April 10, 2013 | Sheet 32 of 77 | |

Confirm INTEL whether remove R548 +1.05V_M directly.

Place R548, C462, C463 and L29 close to U31

Pin 6 is SVR_EN in Clarkville

Pin 2 is WAKE_EN in Clarkville

Internal SRV

Note:
+1.0V_LAN will work at 0.95V to 1.15V

Place C1178 close to pin5

SMBus Device Address 0xC8

Need update symbol pin 5

| SI3456DDV | | |
|---|---|---|
| VDS | RDS(on) | ID(A) |
| 30 | 0.04ohm at VGS=10V | 6.3A |
| 30 | 0.05ohm at VGS=4.5V | 5.7A |

| 0.9Vdc POWER OPTIONS | |
|---|---|
| Shared with PCH 1.05V SVR | * |
| STUFF: R548<br>NO STUFF: L29 | STUFF: L29<br>NO STUFF: R548 |

## LAN ANALOG SWITCH

Layout Notice : Place R as close PI3L500 as possible

| DOCKED | 1: TO DOCK |
|---|---|
| | 0: TO RJ45 |

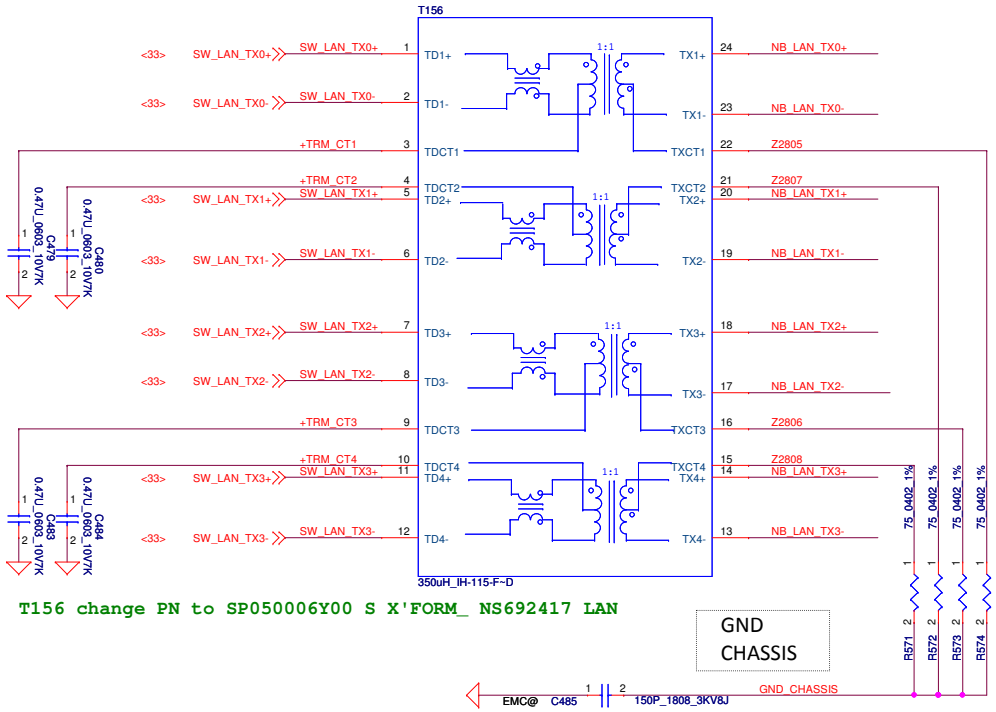


Compal Electronics, Inc.

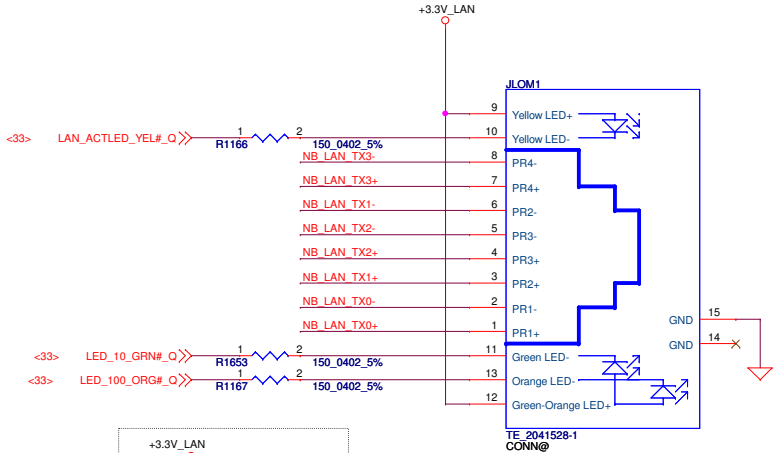
Title: LAN

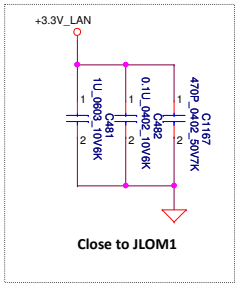
Size: | Document Number: LA-9411P | Rev: 1.0

Date: Wednesday, April 10, 2013 | Sheet 33 of 77




T156 change PN to SP050006Y00 S X'FORM_ NS692417 LAN






Compal Electronics, Inc.

Title: RJ45 Conn

Size | Document Number: LA-9411P | Rev: 1.0

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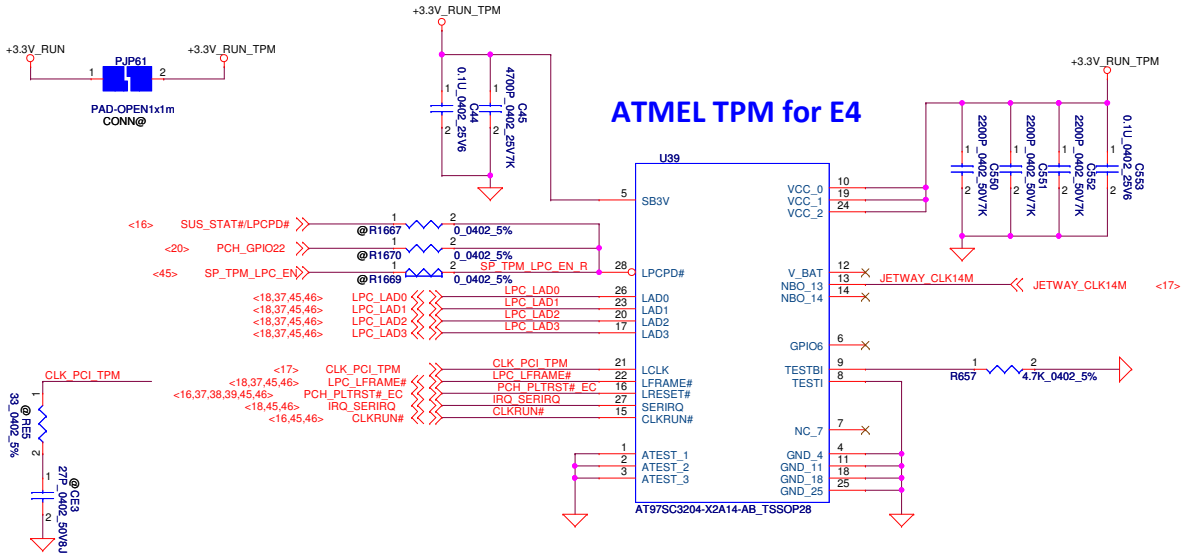
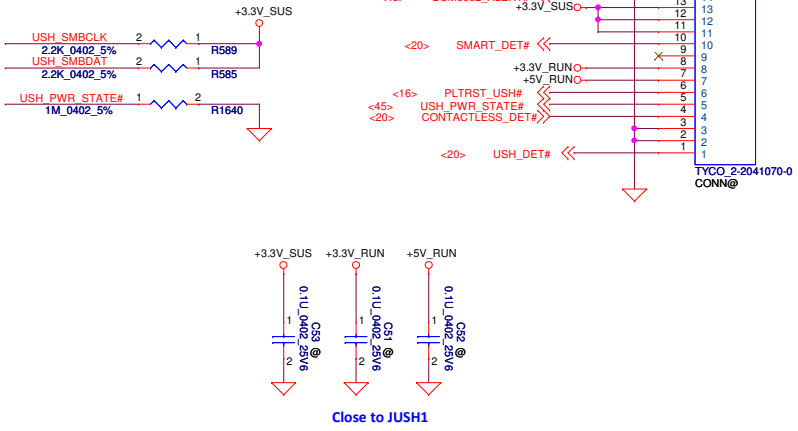
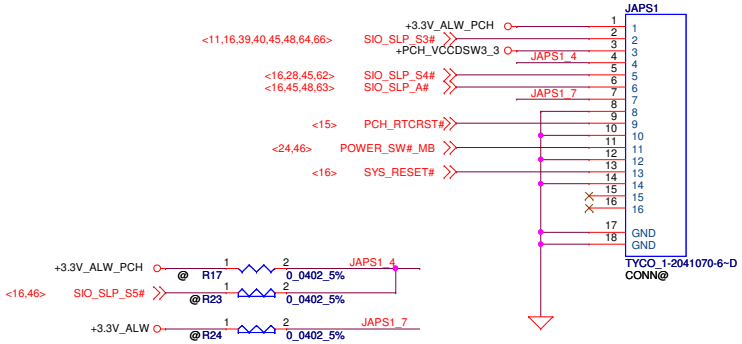



Check ME about wire to board PN






Compal Electronics, Inc.

Title: USH board conn / TPM

Size | Document Number: LA-9411P | Rev: 1.0

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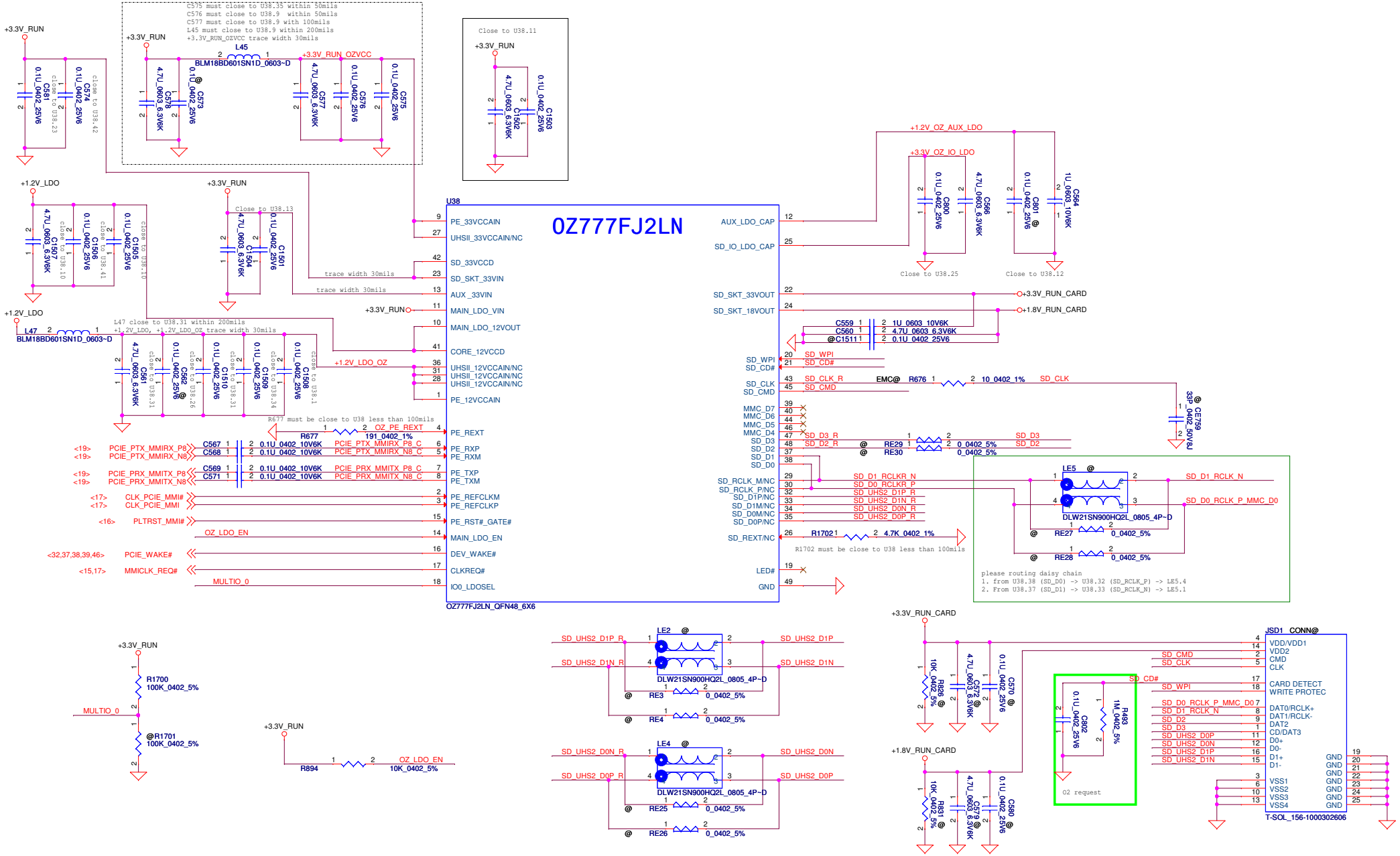
U38
0Z777FJ2LN
OZ777FJ2LN_QFN48_6X6
PE_33VCCAIN
UHSII_33VCCAIN/NC
SD_33VCCD
SD_SKT_33VIN
AUX _33VIN
MAIN_LDO_VIN
MAIN_LDO_12VOUT
CORE_12VCCD
UHSII_12VCCAIN/NC
UHSII_12VCCAIN/NC
UHSII_12VCCAIN/NC
PE_12VCCAIN
PE_REXT
PE_RXP
PE_RXM
PE_TXP
PE_TXM
PE_REFCLKM
PE_REFCLKP
PE_RST#_GATE#
MAIN_LDO_EN
DEV_WAKE#
CLKREQ#
IO0_LDOSEL
AUX_LDO_CAP
SD_IO_LDO_CAP
SD_SKT_33VOUT
SD_SKT_18VOUT
SD_REXT/NC
LED#
GND
+3.3V_RUN
+1.2V_LDO
+3.3V_RUN_OZVCC
+1.2V_OZ_AUX_LDO
+3.3V_OZ_IO_LDO
+1.2V_LDO_OZ
OZ_LDO_EN
MULTIO_0
+3.3V_RUN_CARD
+1.8V_RUN_CARD
JSD1 CONN@
T-SOL_156-1000302606
DLW21SN900HQ2L_0805_4P~D
BLM18BD601SN1D_0603~D
C575 must close to U38.35 within 50mils
C576 must close to U38.9 within 50mils
C577 must close to U38.9 within 100mils
L45 must close to U38.9 within 200mils
+3.3V_RUN_OZVCC trace width 30mils
L47 close to U38.31 within 200mils
+1.2V_LDO, +1.2V_LDO_OZ trace width 30mils
R677 must be close to U38 less than 100mils
R1702 must be close to U38 less than 100mils
trace width 30mils
please routing daisy chain
1. from U38.38 (SD_D0) -> U38.32 (SD_RCLK_P) -> LE5.4
2. From U38.37 (SD_D1) -> U38.33 (SD_RCLK_N) -> LE5.1
only for MMC/SD
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Compal Electronics, Inc.
Card Reader
LA-9411P
Rev 1.0
Wednesday, April 10, 2013
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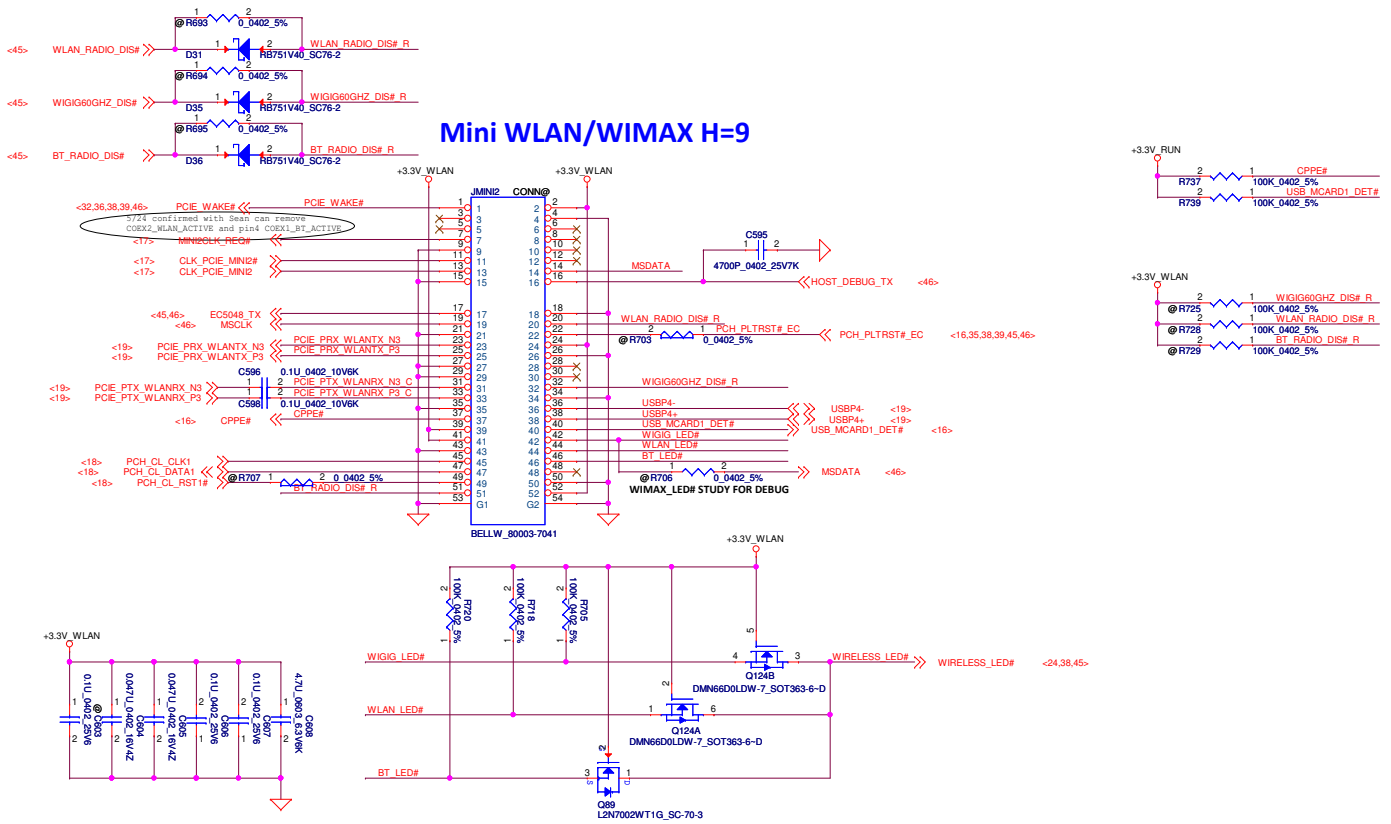
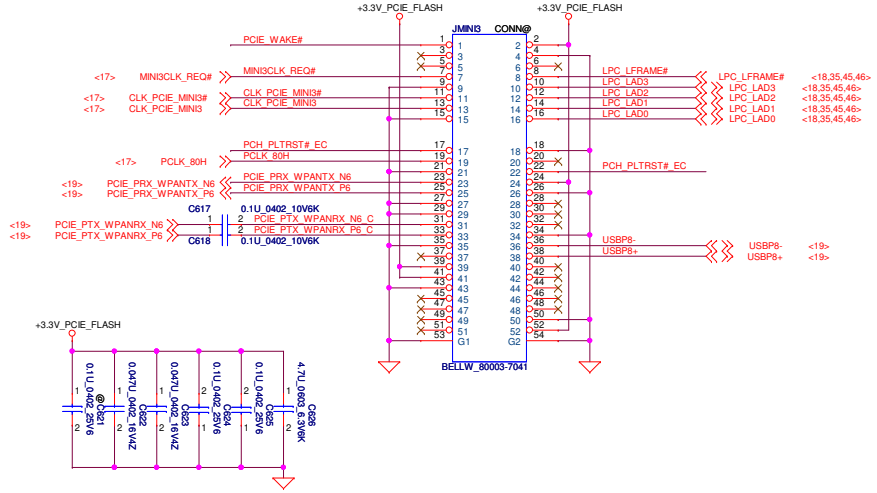



## 1/2 Minicard Pink Pather/60GHz Card H=9

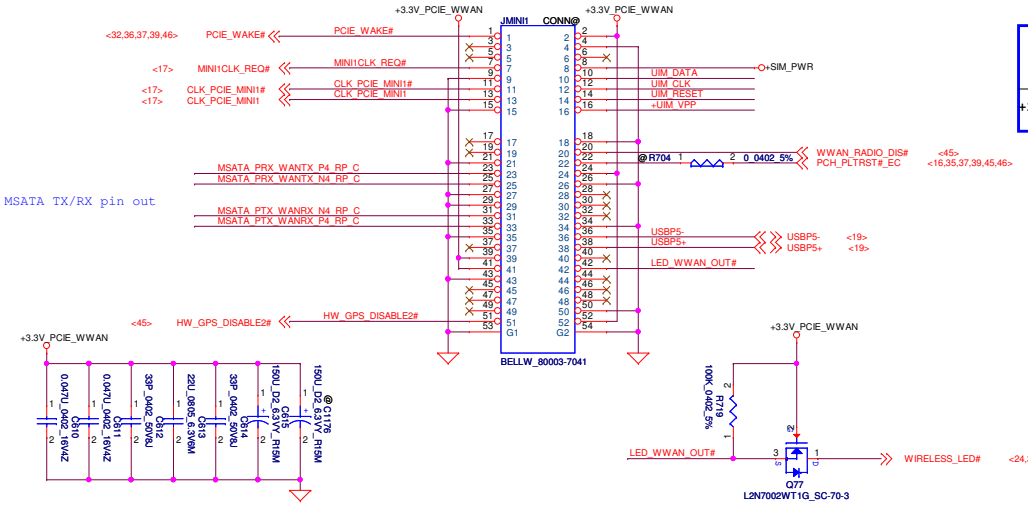







| | | |
|---|---|---|
| Compal Electronics, Inc. | | |
| Title: WLAN/Pink Pather Mini Card | | |
| Size | Document Number: LA-9411P | Rev: 1.0 |
| Date: Wednesday, April 10, 2013 | Sheet 37 of 77 | |

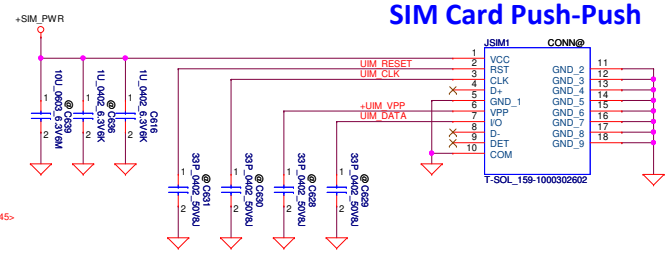
# Mini WWAN/GPS/LTE/UWB H=9



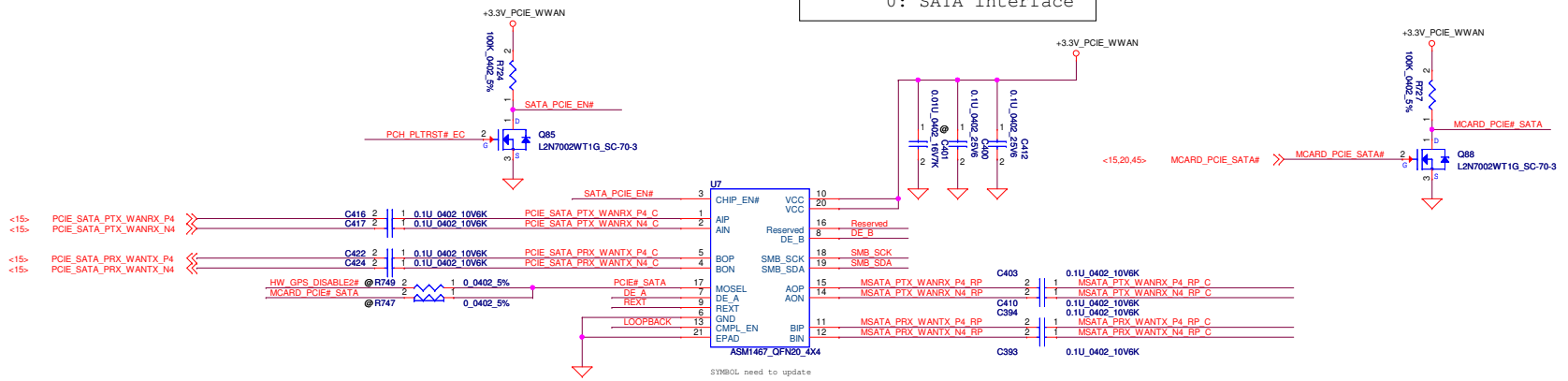

(1) Wake Enabled and Active
(2) Wake NOT Enabled nor Active

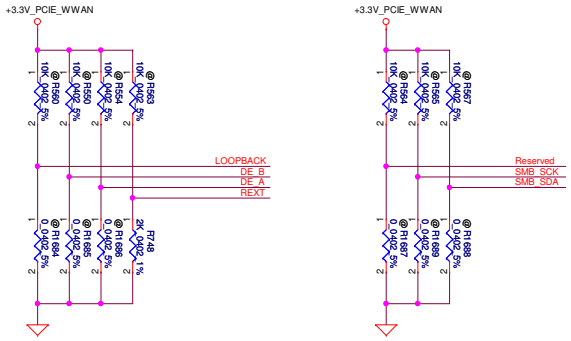
| PWR Rail | Voltage Tolerance | D0-D2&D3 hot Power | | D3 cold Power | |
|---|---|---|---|---|---|
| | | Peak(mA) | Typ(mA) | Peak(mA) | Typ(mA) |
| +3.3V_PCIE_WWAN | +-9% | 2750 | 800 | 800 (1)<br>5 (2) | 150 (1) |

## SIM Card Push-Push




MOSEL 1: PCIE interface
0: SATA interface





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| | | |
|---|---|---|
| Title | WWAN Mini Card | |
| Size | Document Number | Rev |
| | LA-9411P | 1.0 |
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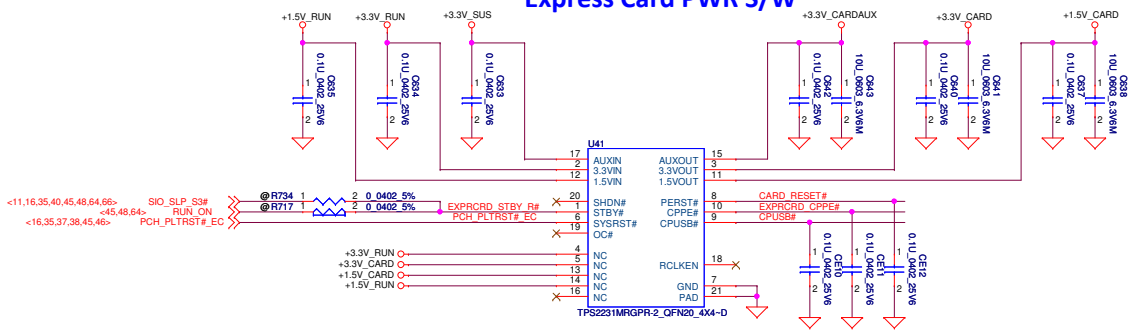
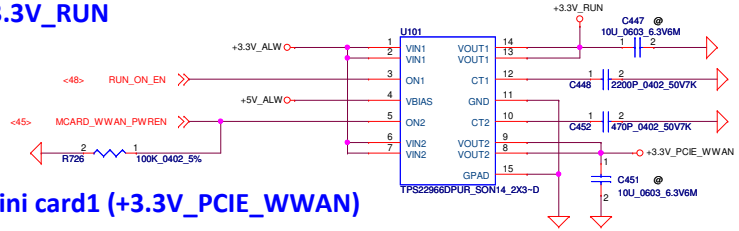
## Express Card PWR S/W




## Express Card Conn.

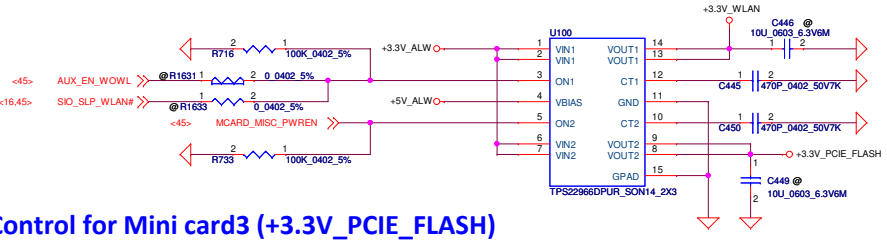
Note: Add connection on pin4, pin5, pin 13 and pin14 to support GMT 2nd source part

## Power Control for +3.3V_RUN

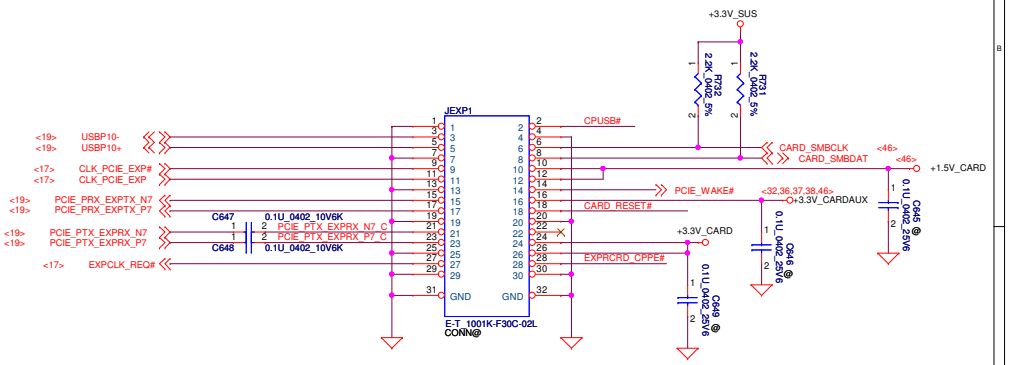



## Power Control for Mini card1 (+3.3V_PCIE_WWAN)

## Power Control for Mini card2 (+3.3V_WLAN)




## Power Control for Mini card3 (+3.3V_PCIE_FLASH)



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Title: PCIE-SATA SW / PCIE PWR

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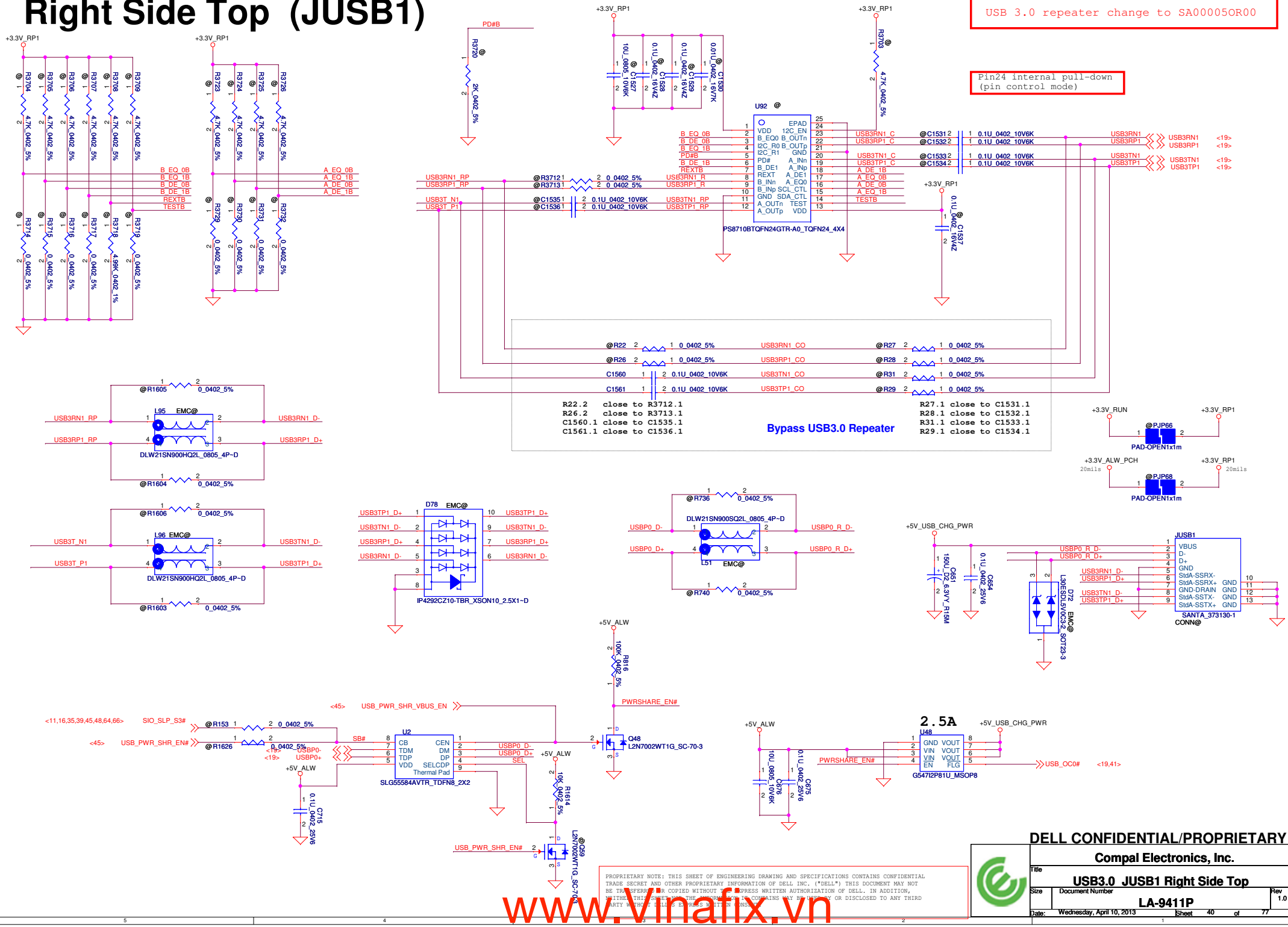
# Right Side Top (JUSB1)

USB 3.0 repeater change to SA00005OR00

Pin24 internal pull-down (pin control mode)

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Title: USB3.0 JUSB1 Right Side Top

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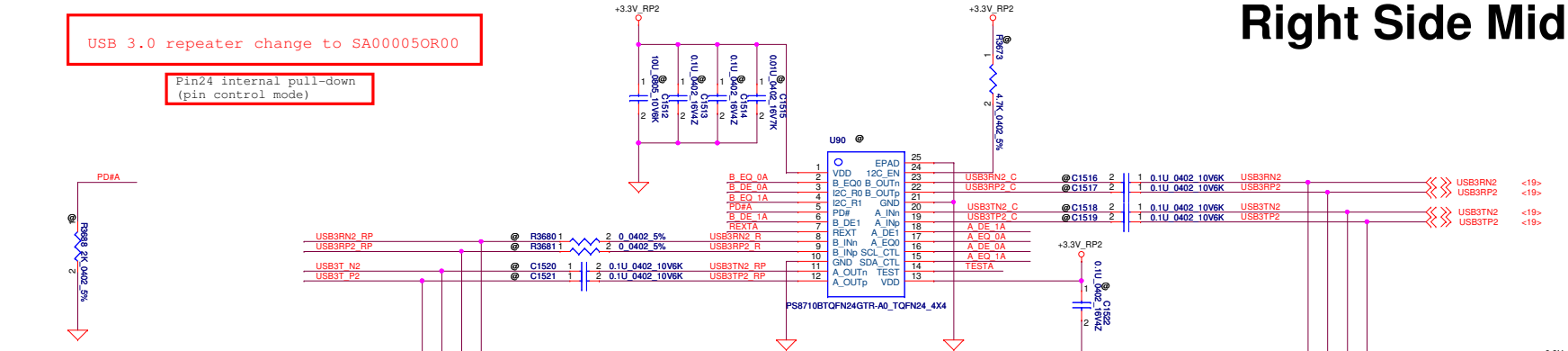
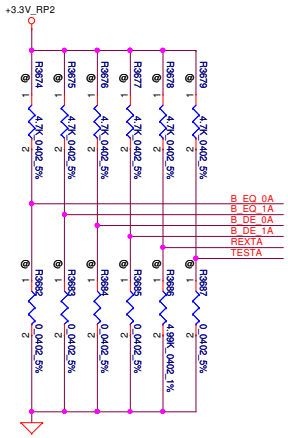
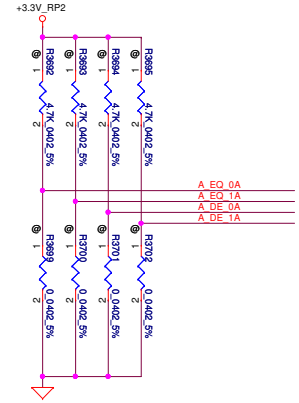
# Right Side Middle (JUSB2)

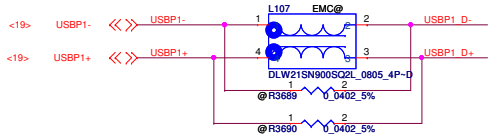
USB 3.0 repeater change to SA00005OR00

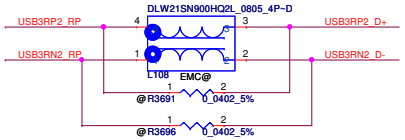
Pin24 internal pull-down
(pin control mode)

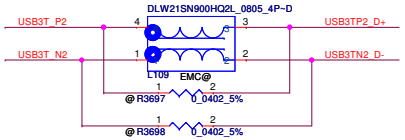


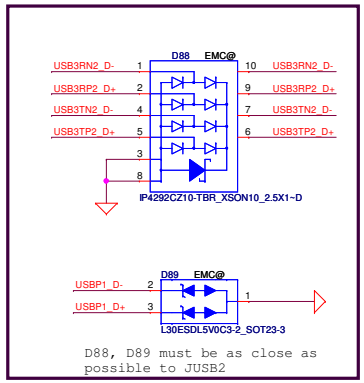



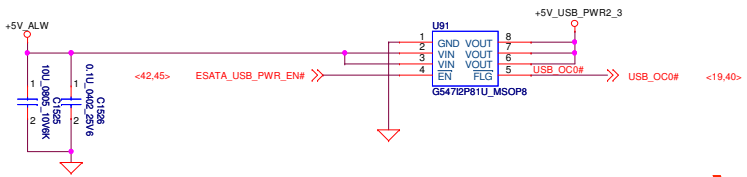



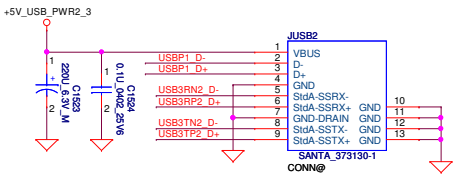



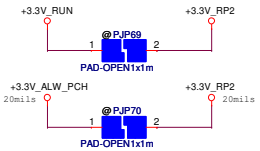



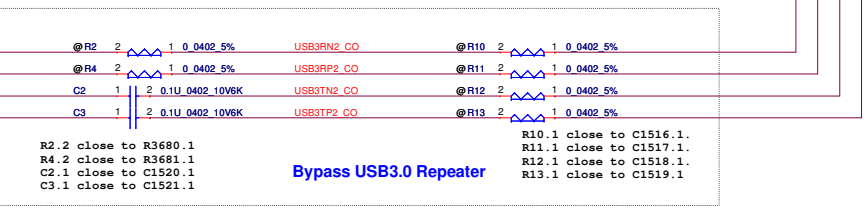




Parade

| A_EQ0 | A_EQ1 | B_EQ0 | B_EQ1 | Recommended EQ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | EQ enable |
| 0 | 1 | 0 | 1 | loss up to 14.5dB |
| 1 | 0 | 1 | 0 | loss up to 7dB |
| 1 | 1 | 1 | 1 | loss up to 11.5dB |

Both A_EQ&B_EQ have internal pull-down 150k

Pericom

| EQ A/B | EQ setting |
|---|---|
| 0 | 3dB |
| OPEN | 6dB |
| 1 | 9dB |

| DE A/B | DE setting |
|---|---|
| 0 | 0dB |
| OPEN | -3dB |
| 1 | -6dB |

| A_DE0 | A_DE1 | B_DE0 | B_DE1 | Recommended De-Emphaisis |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | -3.5dB |
| 0 | 1 | 0 | 1 | -7dB |
| 1 | 0 | 1 | 0 | 0dB |
| 1 | 1 | 1 | 1 | 5dB boost output swing |

Both A_DE&B_DE have internal pull-down 150k



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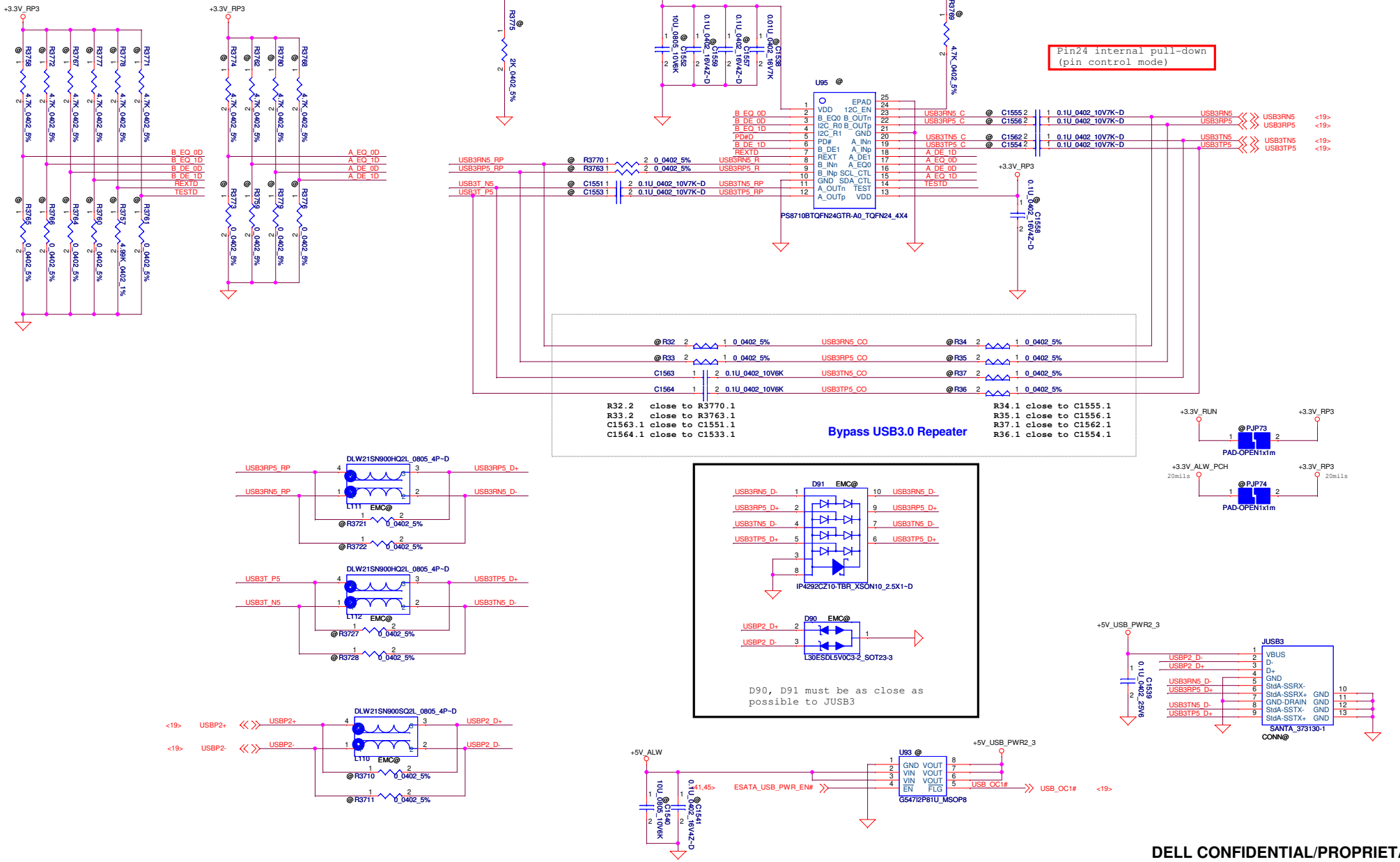
# Right Side bottom (JUSB3)

USB 3.0 repeater change to SA00005OR00

Pin24 internal pull-down (pin control mode)

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| | | |
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| Title: USB3.0 JUSB3 Right Side bot | | |
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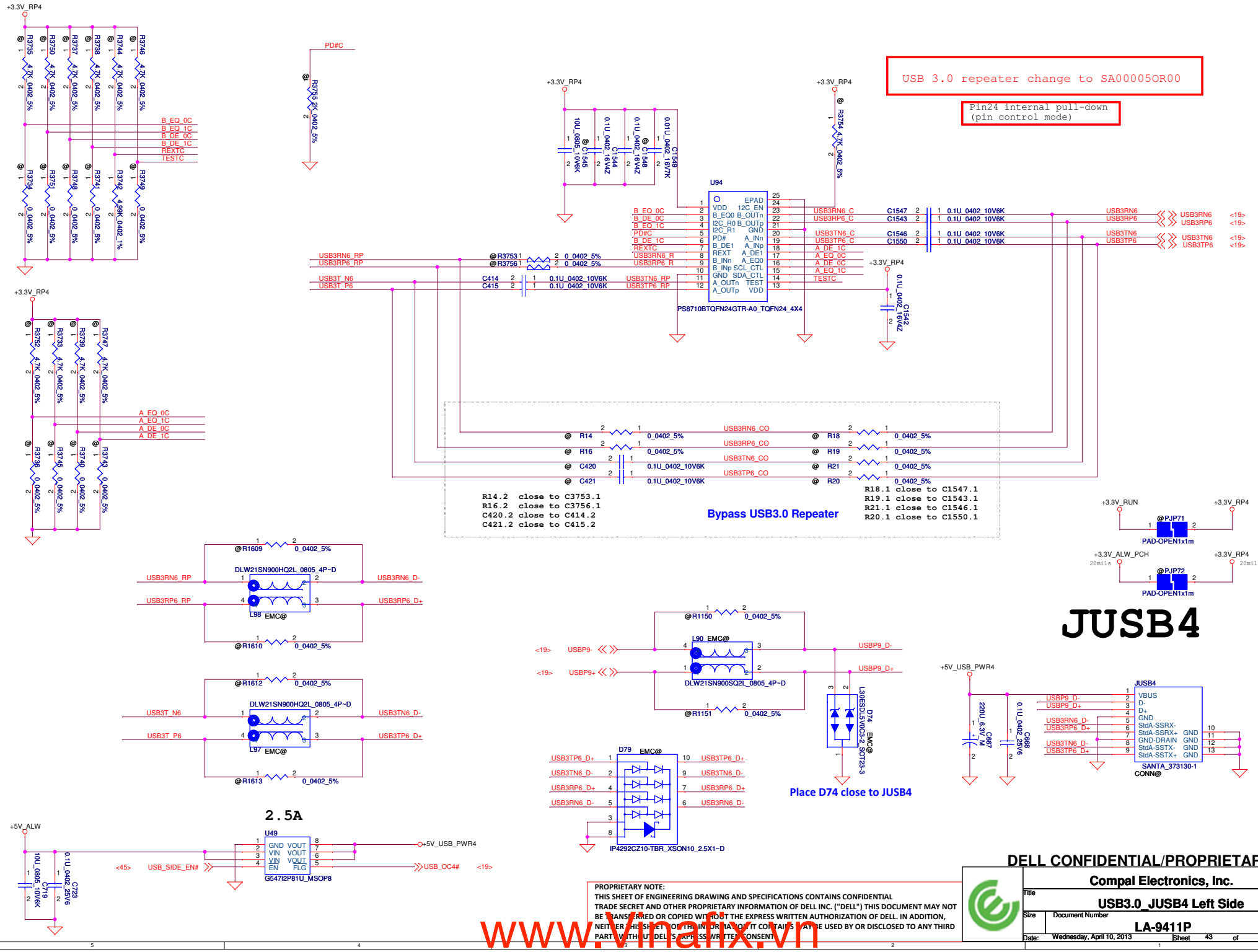
USB 3.0 repeater change to SA00005OR00
Pin24 internal pull-down (pin control mode)
U94
PS8710BTQFN24GTR-A0_TQFN24_4X4
Bypass USB3.0 Repeater
R14.2 close to C3753.1
R16.2 close to C3756.1
C420.2 close to C414.2
C421.2 close to C415.2
R18.1 close to C1547.1
R19.1 close to C1543.1
R21.1 close to C1546.1
R20.1 close to C1550.1
JUSB4
2.5A
U49
G547I2P81U_MSOP8
IP4292CZ10-TBR_XSON10_2.5X1~D
Place D74 close to JUSB4
SANTA_373130-1
CONN@
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USB3.0_JUSB4 Left Side
LA-9411P
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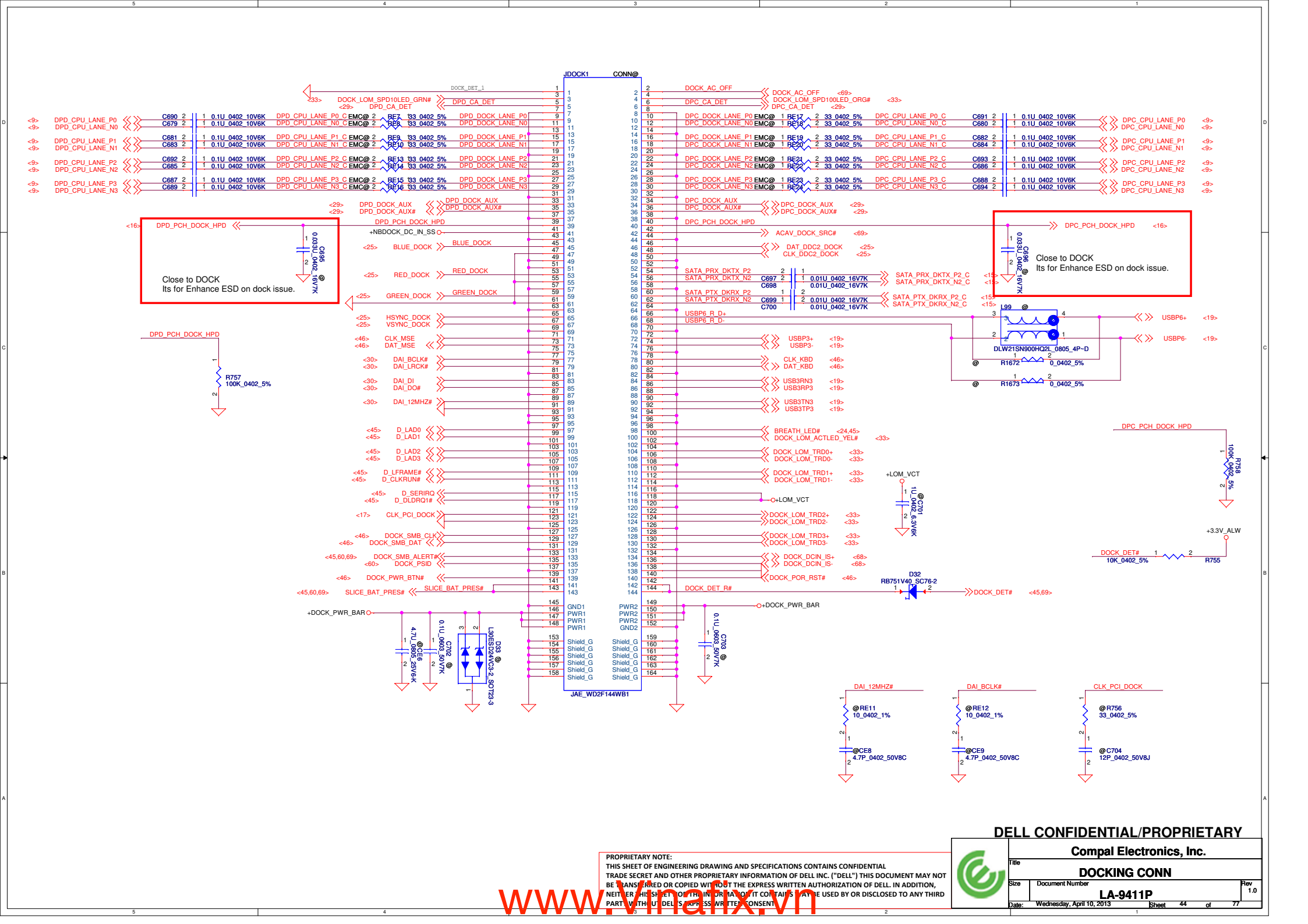


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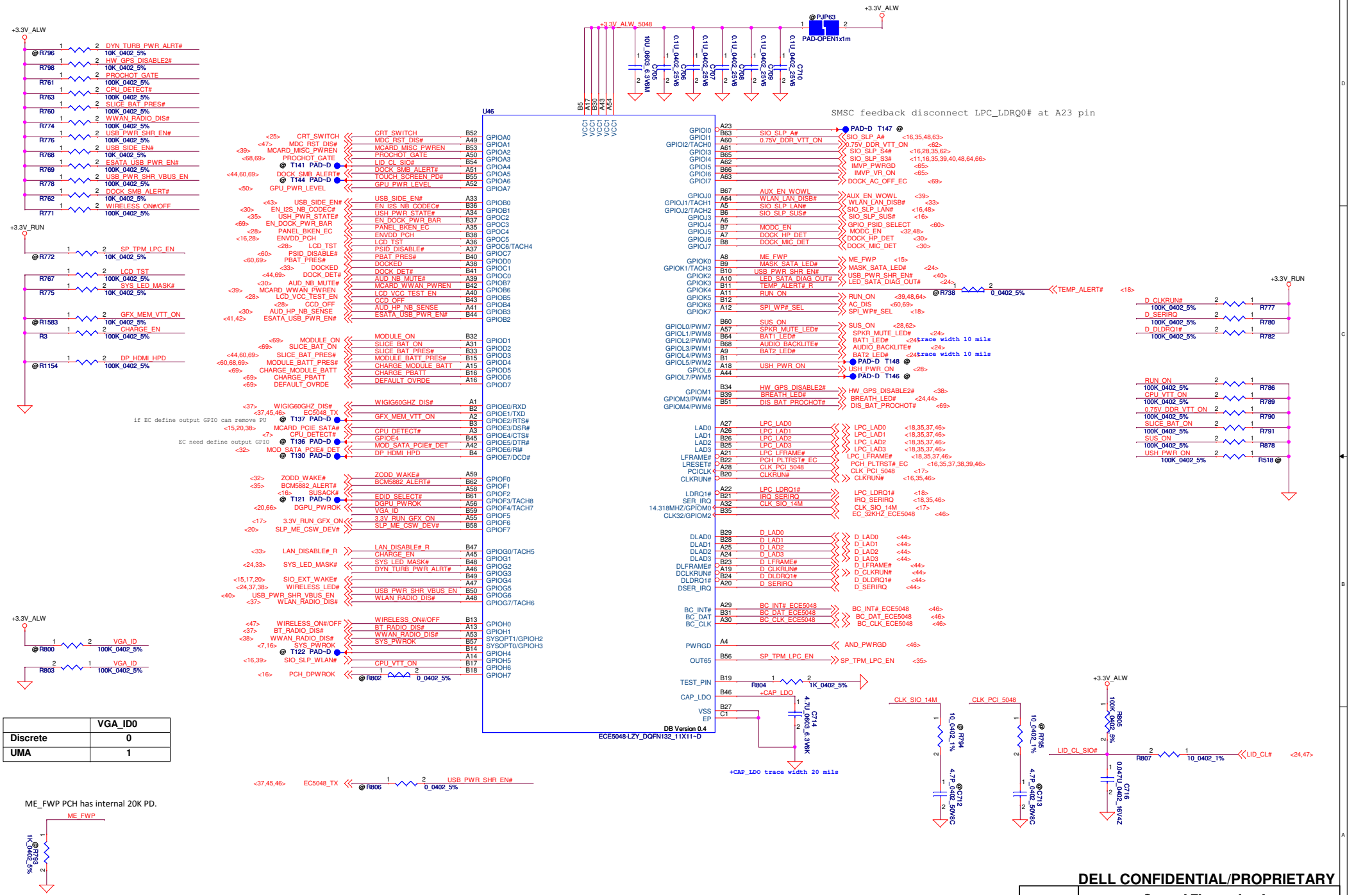


| | VGA_ID0 |
|---|---|
| Discrete | 0 |
| UMA | 1 |



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Title: ECE5048

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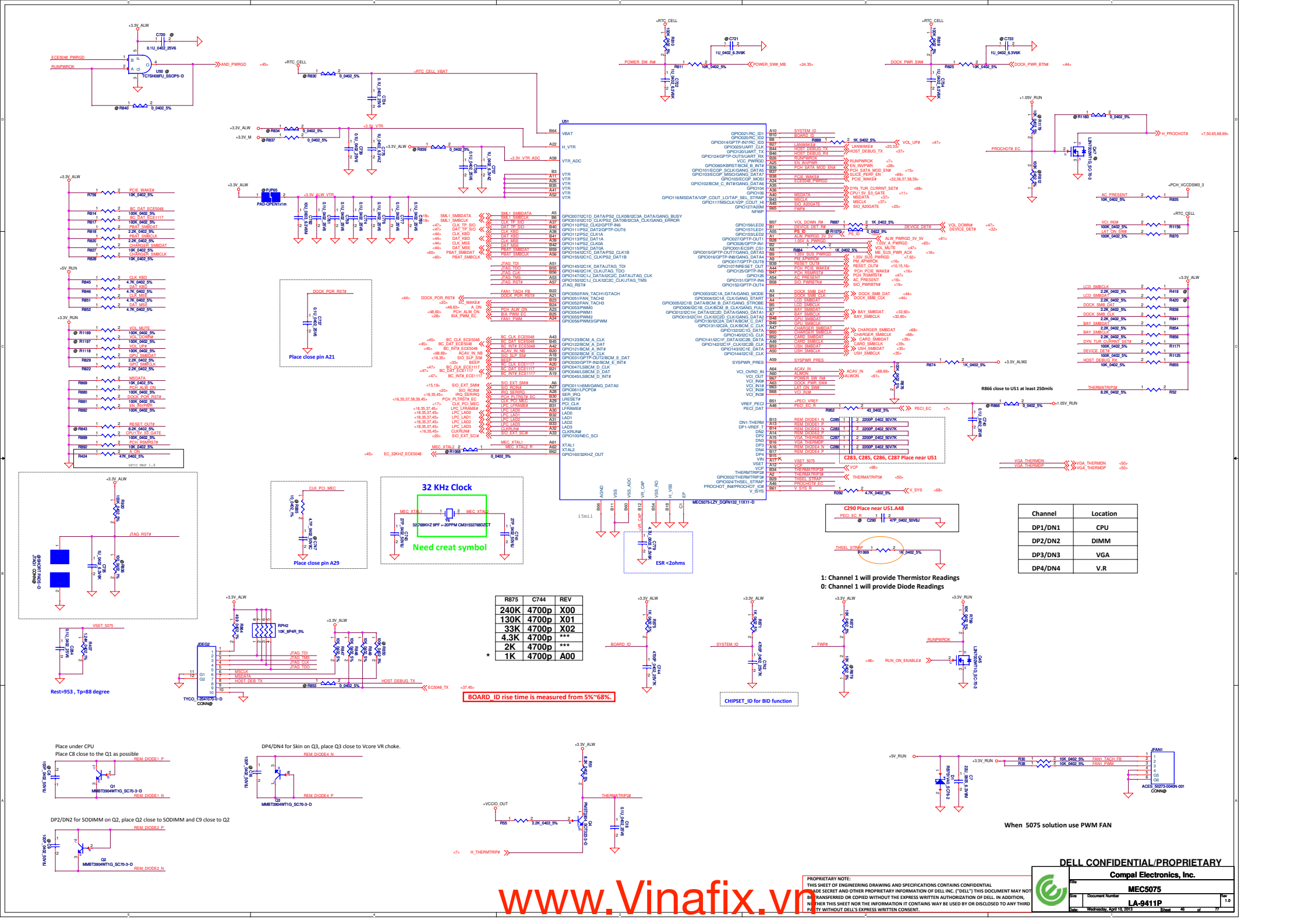


| R875 | C744 | REV |
|---|---|---|
| 240K | 4700p | X00 |
| 130K | 4700p | X01 |
| 33K | 4700p | X02 |
| 4.3K | 4700p | *** |
| 2K | 4700p | *** |
| 1K | 4700p | A00 |

*

| Channel | Location |
|---|---|
| DP1/DN1 | CPU |
| DP2/DN2 | DIMM |
| DP3/DN3 | VGA |
| DP4/DN4 | V.R |



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Title: MEC5075

Size: | Document Number: LA-9411P | Rev: 1.0

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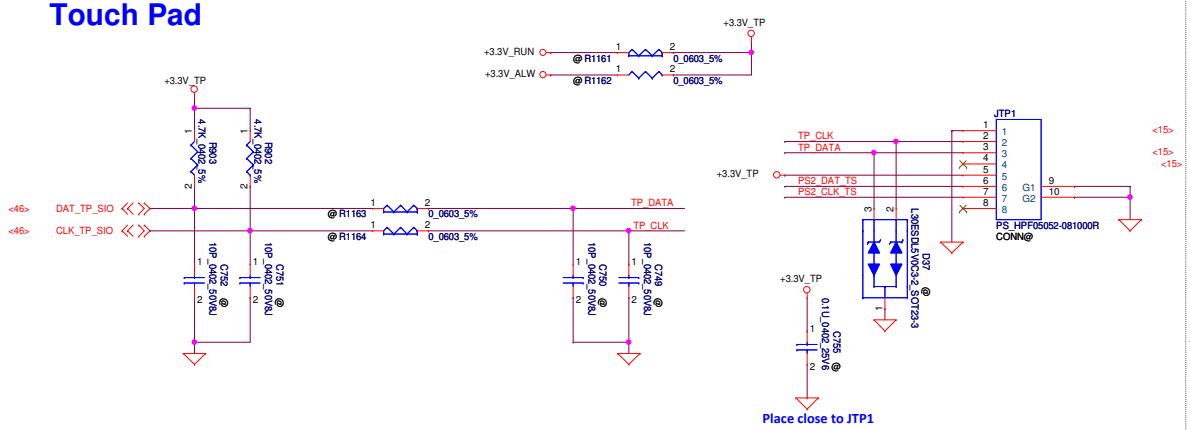
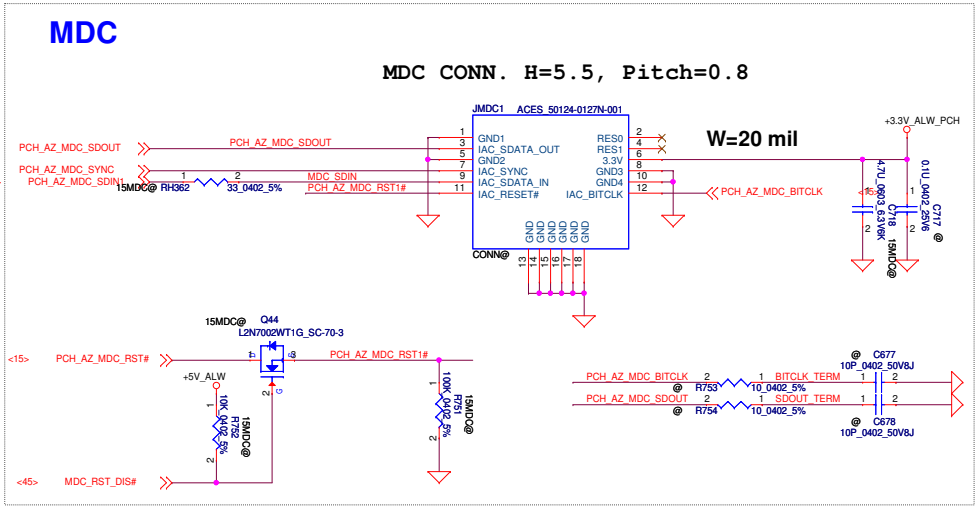
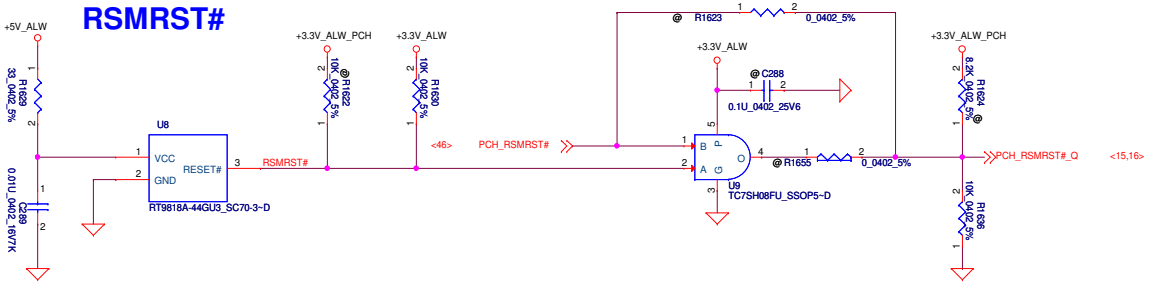
## Touch Pad



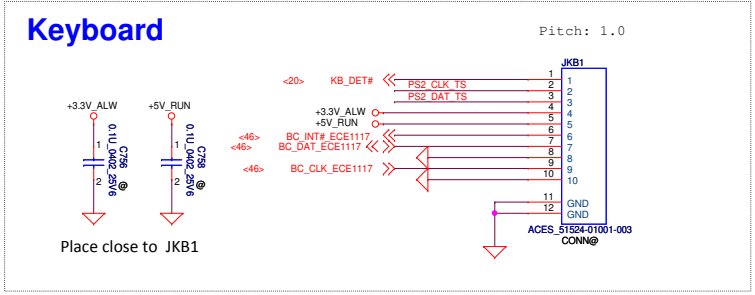

## MDC



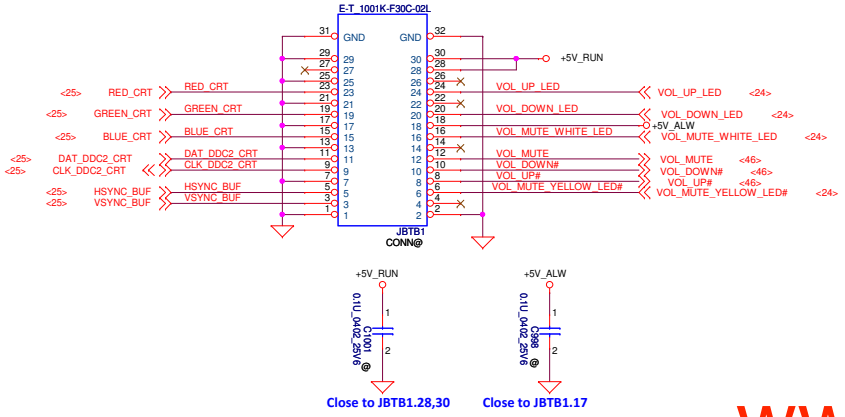

## RSMRST#



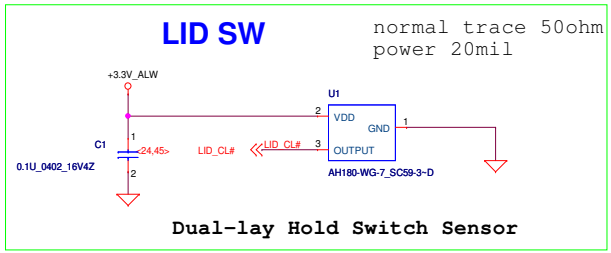

## Keyboard

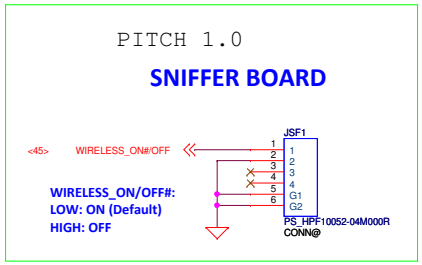


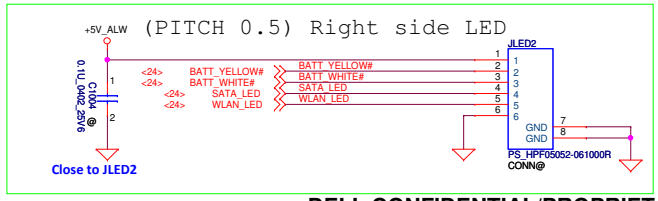

## I/O Borad




## LID SW

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| Size | Document Number: LA-9411P |
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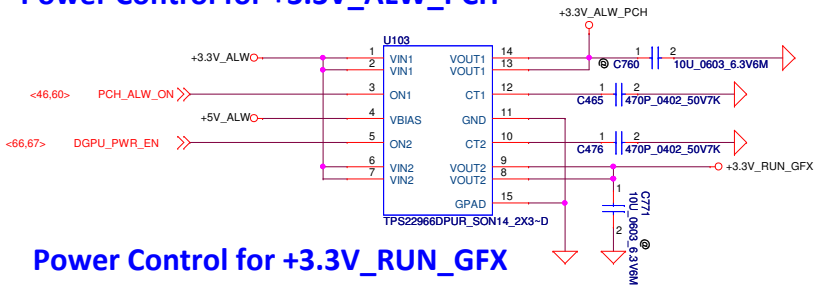
## Power Control for +3.3V_ALW_PCH



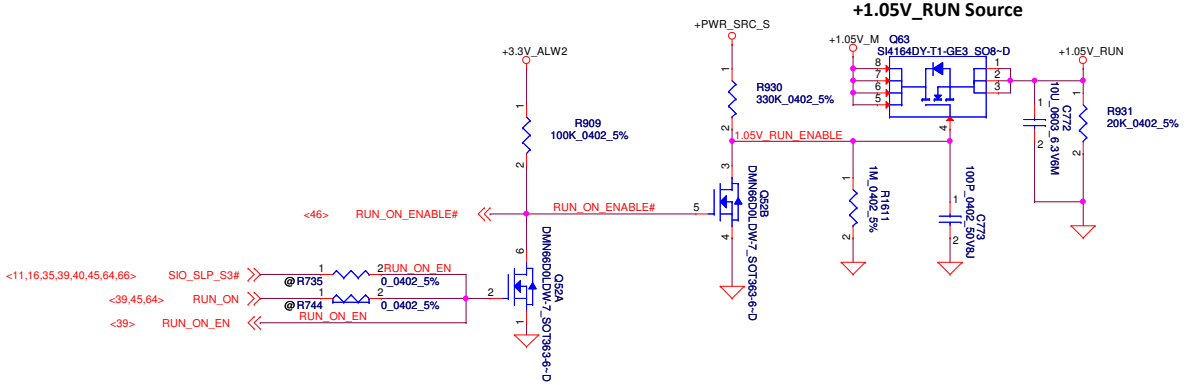

## Power Control for +3.3V_RUN_GFX

## DC/DC Interface

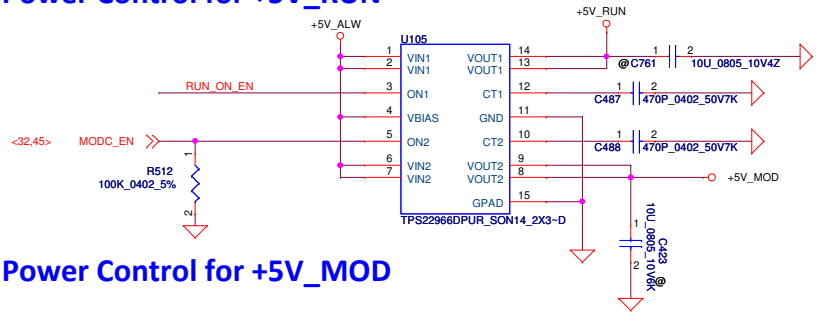
SI4164DY

| VDS | RDS(on) | ID(A) |
|---|---|---|
| 30 | 0.0032ohm at VGS=10V | 30A |
| 30 | 0.0039ohm at VGS=4.5V | 26.3A |

### +1.05V_RUN Source

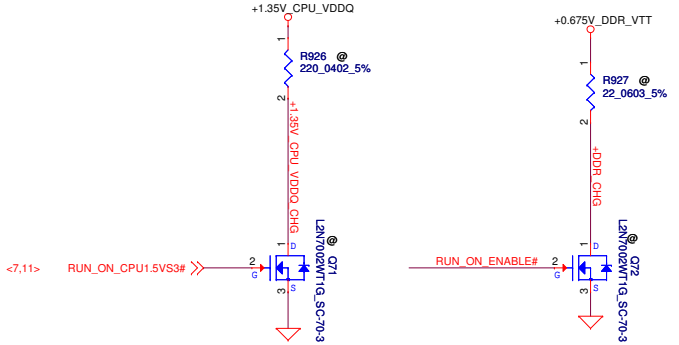


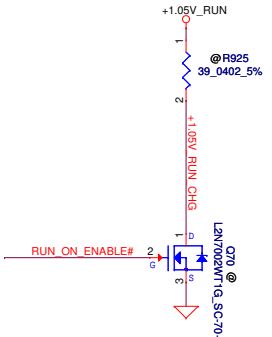

## Power Control for +5V_RUN



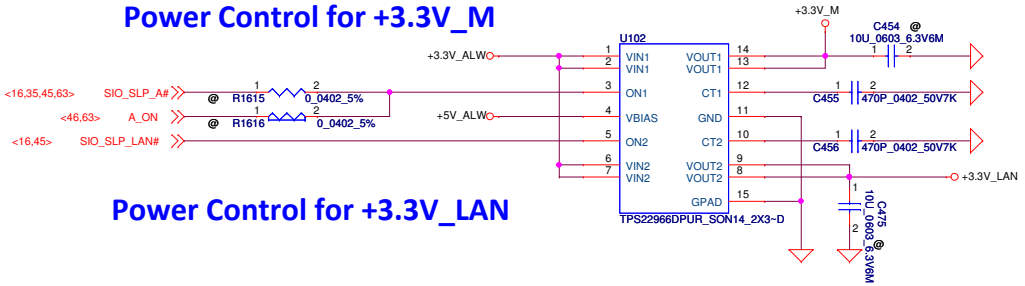

## Power Control for +5V_MOD

## Discharge Circuit




## Power Control for +3.3V_M




## Power Control for +3.3V_LAN

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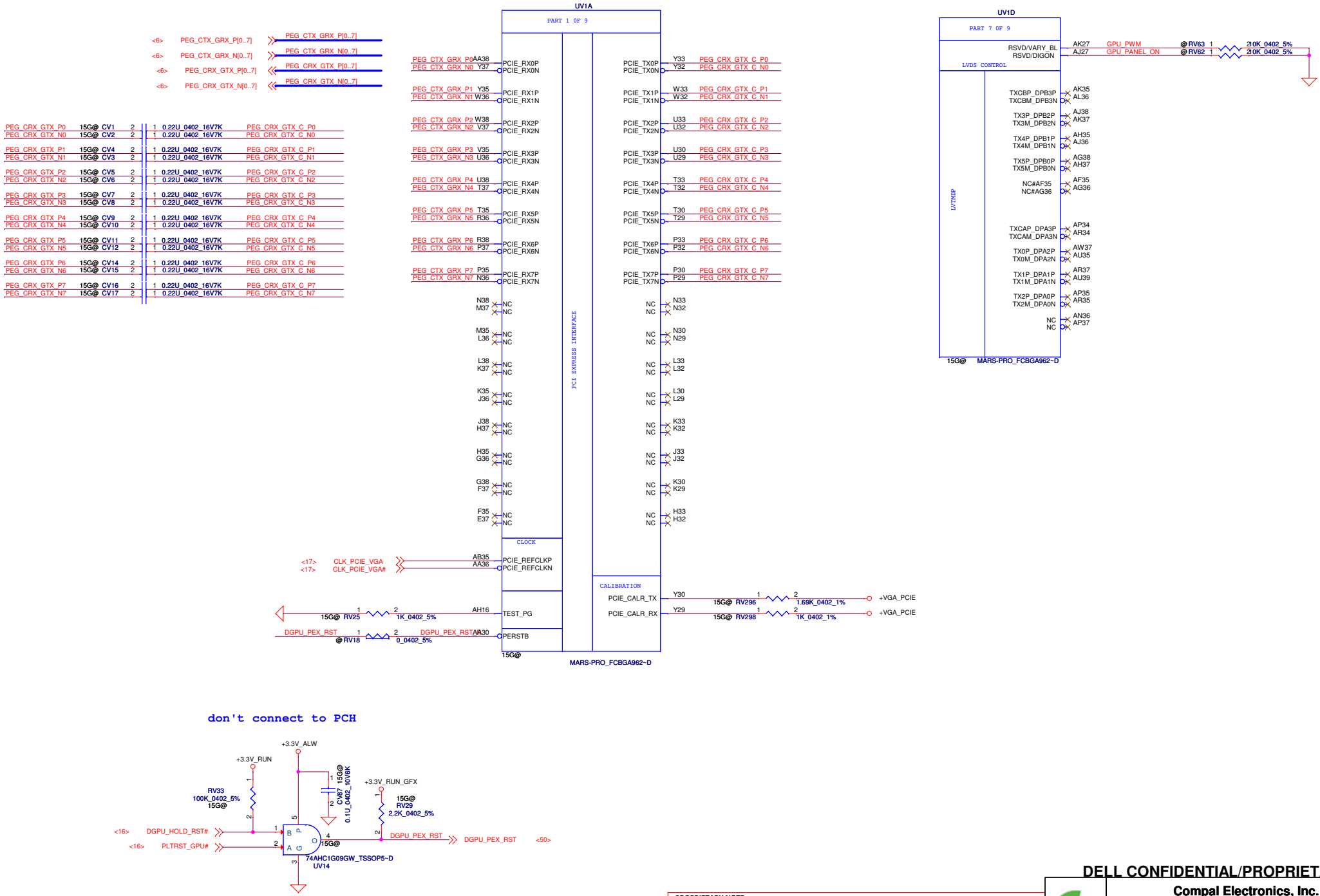
| | |
|---|---|
| Compal Electronics, Inc. | |
| Title | POWER CONTROL |
| Size | Document Number: LA-9411P |
| Rev | 1.0 |
| Date: | Wednesday, April 10, 2013 |
| Sheet | 48 of 77 |



# CONFIGURATION STRAPS

**ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET**

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

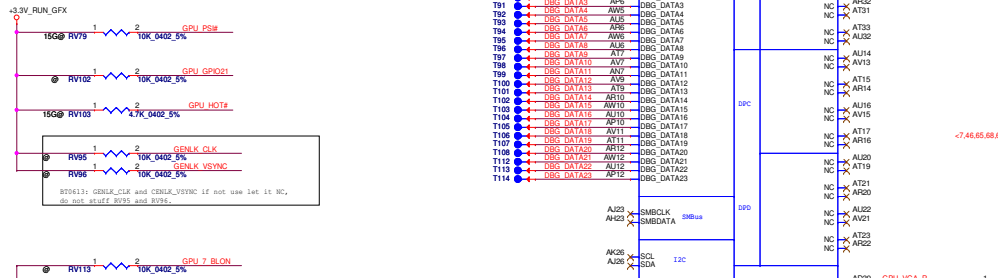
| STRAPS | PIN | DESCRIPTION OF DEFAULT SETTINGS | | RECOMMENDED SETTINGS |
|---|---|---|---|---|
| TX_PWRS_ENB | GPIO0 | PCIE FULL TX OUTPUT SWING | 0: 50% swing<br>1: Full swing | X |
| TX_DEEMPH_EN | GPIO1 | PCIE TRANSMITTER DE-EMPHASIS | 0: disable<br>1: enable | X |
| RSVD | GPIO2 | Advertises PCIE speed when compliance test | 0: 2.5GT/s<br>1: 5GT/s | 0 |
| RSVD | GPIO8 | RESERVED | | 0 |
| BIF_VGA DIS | GPIO9 | VGA ENABLED | | 0 |
| RSVD | GPIO21 | RESERVED | | 0 |
| BIOS_ROM_EN | GPIO_22_ROMCSB | ENABLE EXTERNAL BIOS ROM | 0: disable<br>1: enable | X |
| ROMIDCFG(2:0) | GPIO[13:11] | SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT | | XXX |
| VIP_DEVICE_STRAP_ENA | V2SYNC | IGNORE VIP DEVICE STRAPS | | 0 |
| RSVD | H2SYNC | | | 0 |
| RSVD | GENERICC | | | 0 |
| AUD[1]<br>AUD[0] | HSYNC<br>VSYNC | AUD[1] AUD[0]<br>0 0 No audio function<br>0 1 Audio for DisplayPort and HDMI if dongle is detected<br>1 0 Audio for DisplayPort only<br>1 1 Audio for both DisplayPort and HDMI | | 11 |

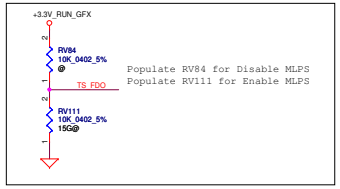
## AMD RESERVED CONFIGURATION STRAPS

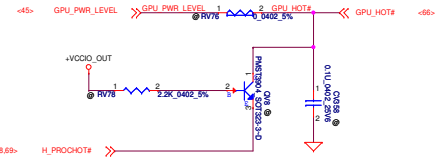
**ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET**

| GPIO21 | H2SYNC | GENERICC | GPIO2 | GPIO8 |
|---|---|---|---|---|

## STRAPS



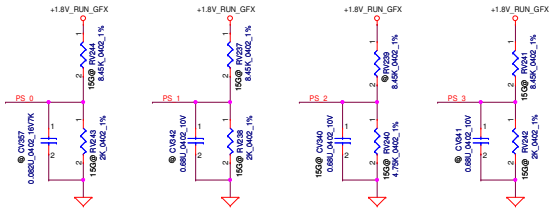



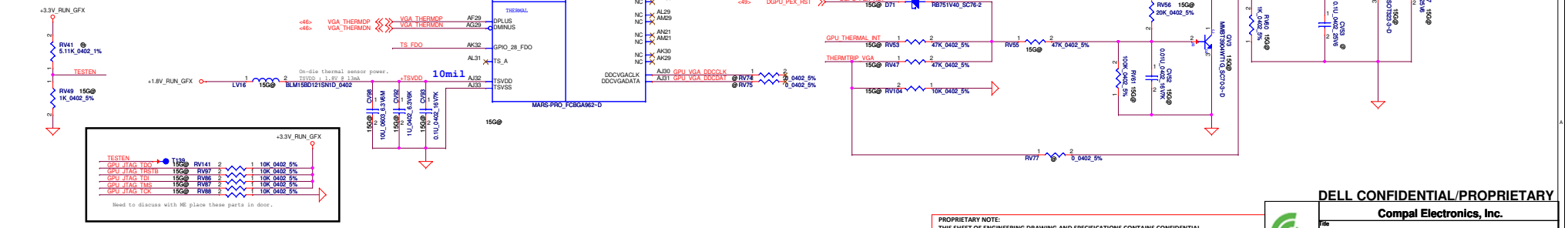

| GPU_PWR_LEVEL | |
|---|---|
| LOW | Low Performance |
| HIGH | High Performance |

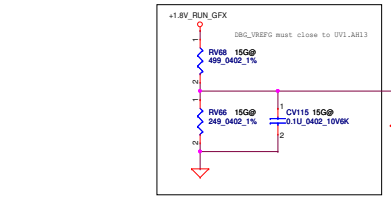
| PS_3_[3:2:1] for MEMID | RV241_PD | RV242_PD | CV341 |
|---|---|---|---|
| 001: Hynix H5GQ2H24AFR (1.35V) | 8.45K | 2K | NC |
| 010: Samsung K4G20325FD (1.35V) | 4.53K | 2K | NC |

When use Samsung VRAM SA00005B70L, please change this RV241 to 4.53Kohm (SD034453181).




| | | |
|---|---|---|
| TX_PWRS_ENB | GPIO0 | Transmitter Power Saving Enable<br>0: 50% Tx output swing for mobile mode<br>1: full Tx output swing (Default setting for Desktop) |
| TX_DEEMPH_EN | GPIO1 | PCI Express Transmitter De-emphasis Enable<br>0: Tx de-emphasis diabled for mobile mode<br>1: Tx de-emphasis enabled (Defailt setting for desktop) |



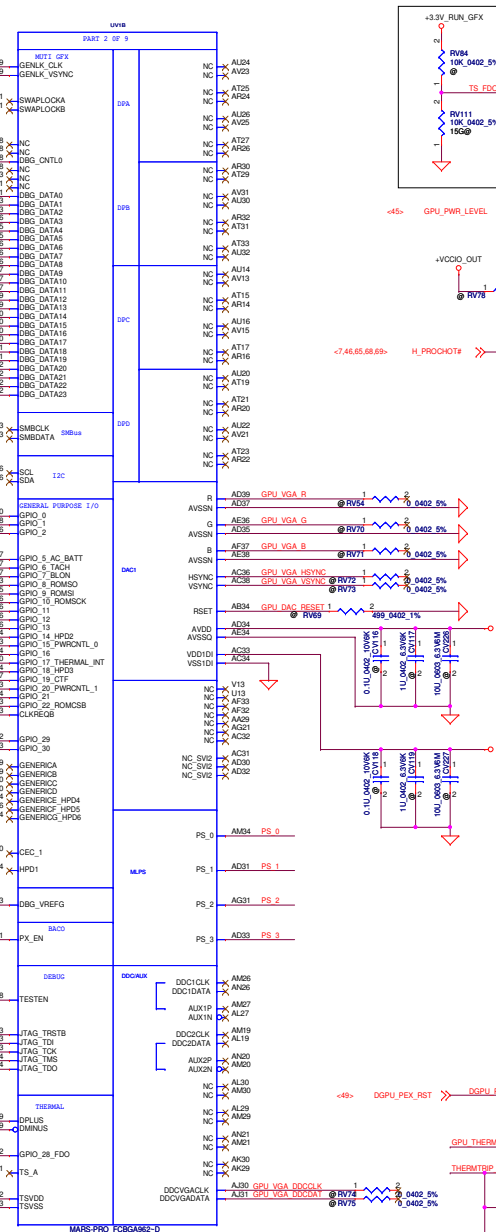


















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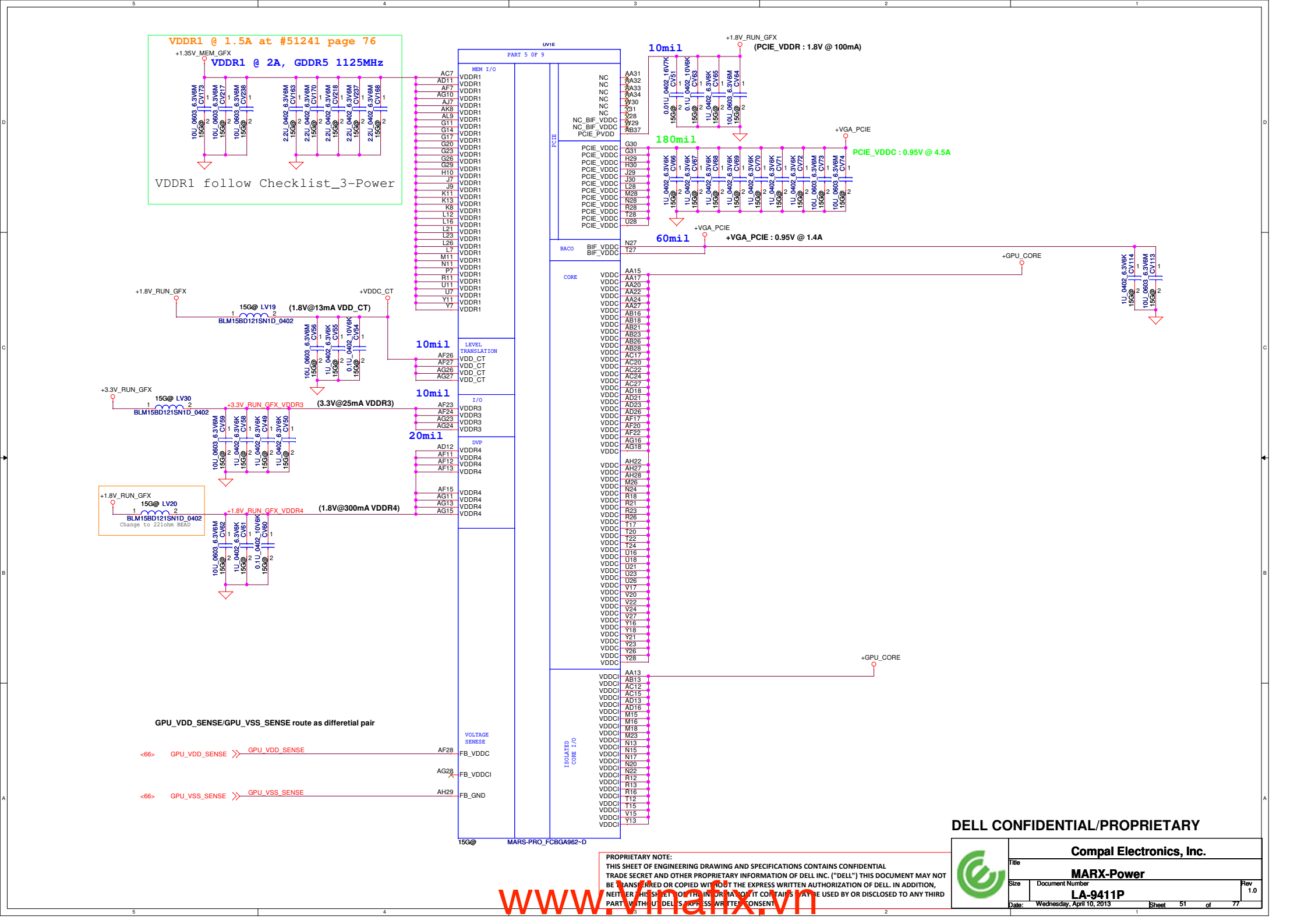
Title: MARX-GPIO,HDMI,DP,DAC

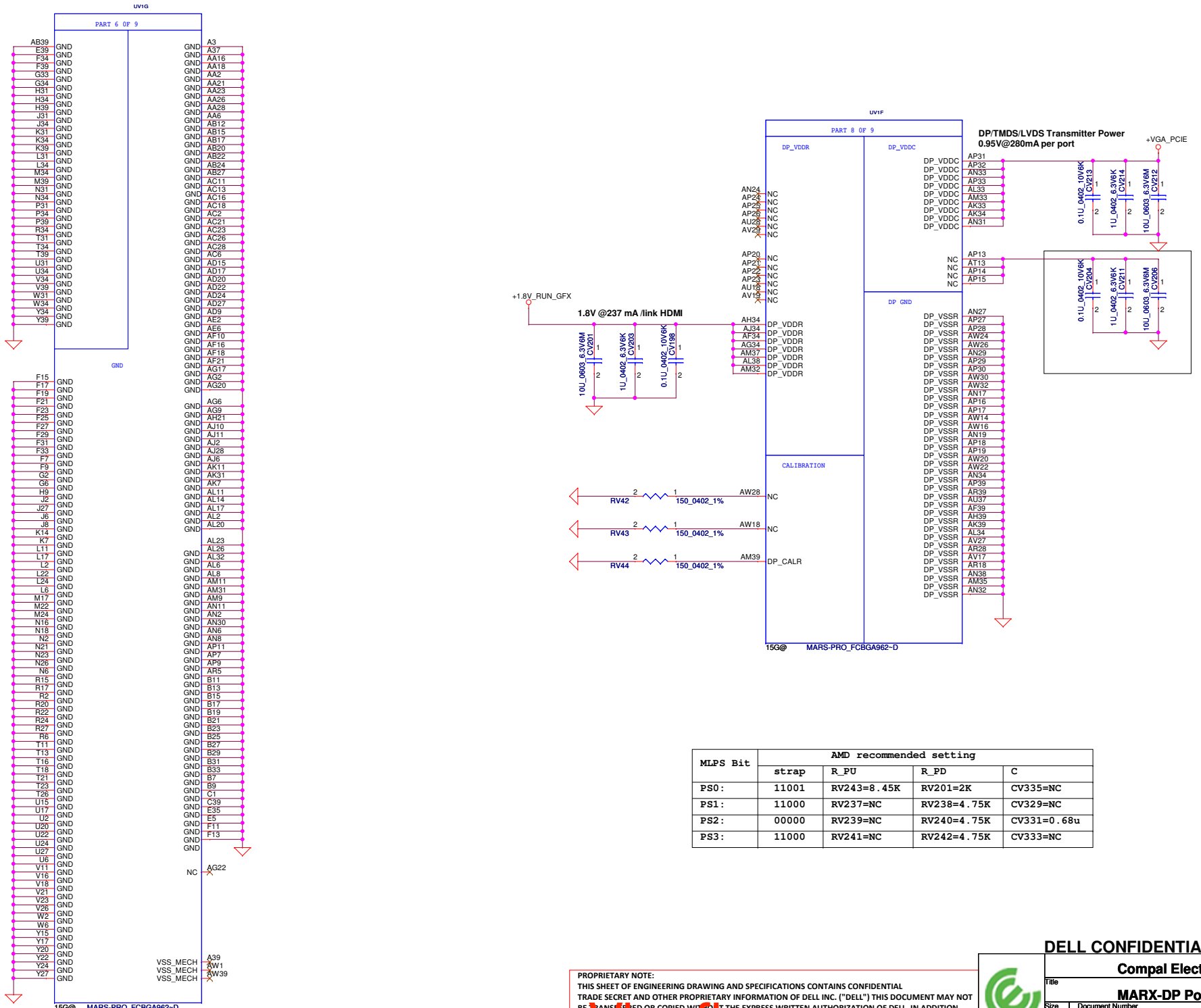
Size: Document Number: LA-9411P Rev: 1.0

Date: Wednesday, April 10, 2013 Sheet 50 of 77






| | |
|---|---|
| Compal Electronics, Inc. | |
| Title | MARX-Power |
| Size | Document Number: LA-9411P |
| Rev | 1.0 |
| Date: | Wednesday, April 10, 2013 |
| Sheet | 51 of 77 |




| MLPS Bit | AMD recommended setting | | | |
|---|---|---|---|---|
| | strap | R_PU | R_PD | C |
| PS0: | 11001 | RV243=8.45K | RV201=2K | CV335=NC |
| PS1: | 11000 | RV237=NC | RV238=4.75K | CV329=NC |
| PS2: | 00000 | RV239=NC | RV240=4.75K | CV331=0.68u |
| PS3: | 11000 | RV241=NC | RV242=4.75K | CV333=NC |

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Title: MARX-DP Power,GND
Size: Document Number: LA-9411P
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Date: Wednesday, April 10, 2013
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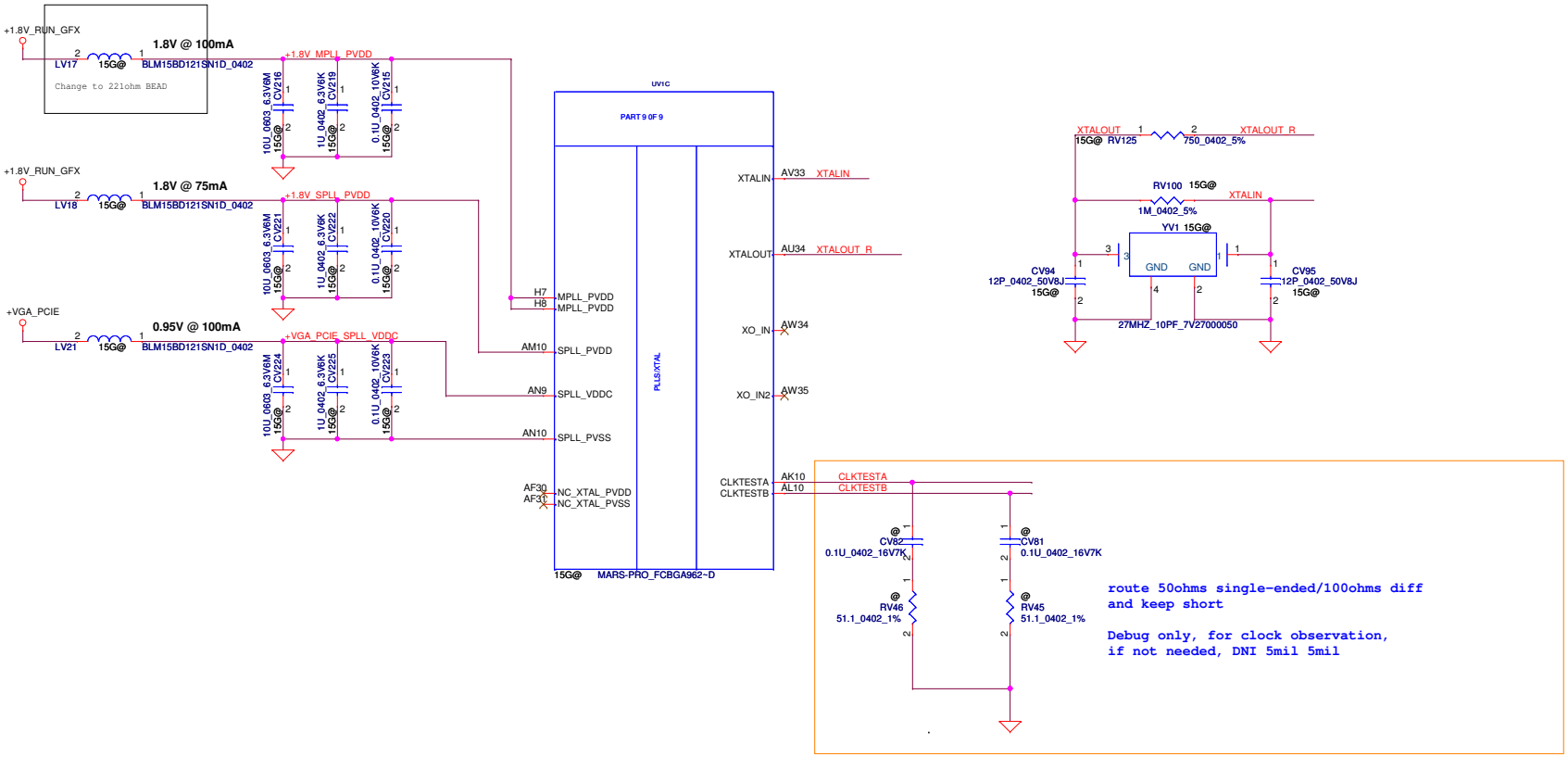


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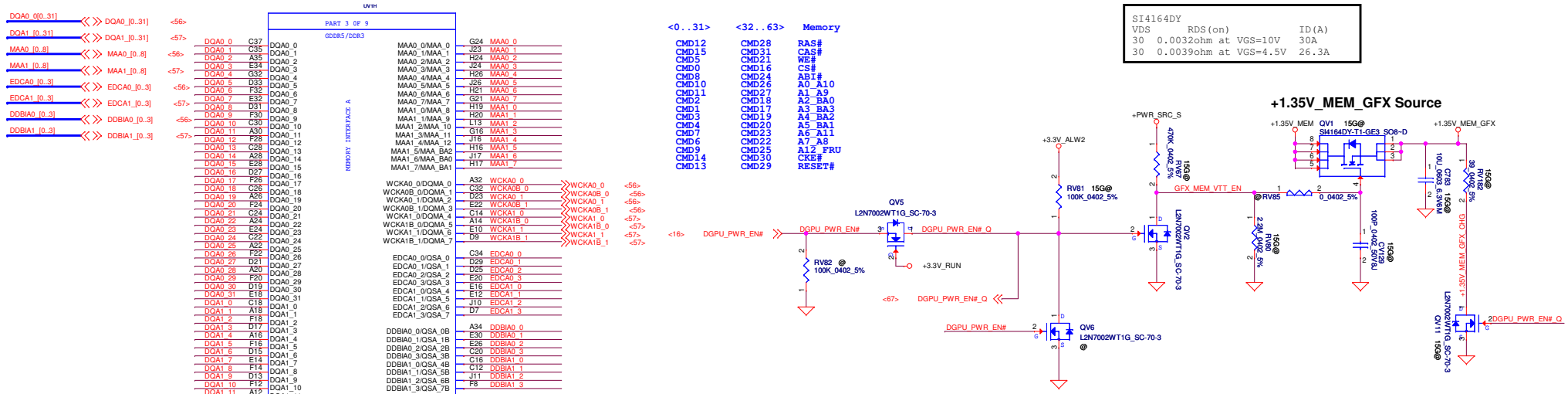
| | | |
|---|---|---|
| Title | MARX-PLL Power | |
| Size | Document Number LA-9411P | Rev 1.0 |
| Date: Wednesday, April 10, 2013 | Sheet 53 of 77 | |

## GDDR5 CMD Mapping Table

| <0..31> | <32..63> | Memory |
|---|---|---|
| CMD12 | CMD28 | RAS# |
| CMD15 | CMD31 | CAS# |
| CMD5 | CMD21 | WE# |
| CMD0 | CMD16 | CS# |
| CMD8 | CMD24 | ABI# |
| CMD10 | CMD26 | A0_A10 |
| CMD11 | CMD27 | A1_A9 |
| CMD2 | CMD18 | A2_BA0 |
| CMD1 | CMD17 | A3_BA3 |
| CMD3 | CMD19 | A4_BA2 |
| CMD4 | CMD20 | A5_BA1 |
| CMD7 | CMD23 | A6_A11 |
| CMD6 | CMD22 | A7_A8 |
| CMD9 | CMD25 | A12_FRU |
| CMD14 | CMD30 | CKE# |
| CMD13 | CMD29 | RESET# |

SI4164DY
VDS RDS(on) ID(A)
30 0.0032ohm at VGS=10V 30A
30 0.0039ohm at VGS=4.5V 26.3A

### +1.35V_MEM_GFX Source







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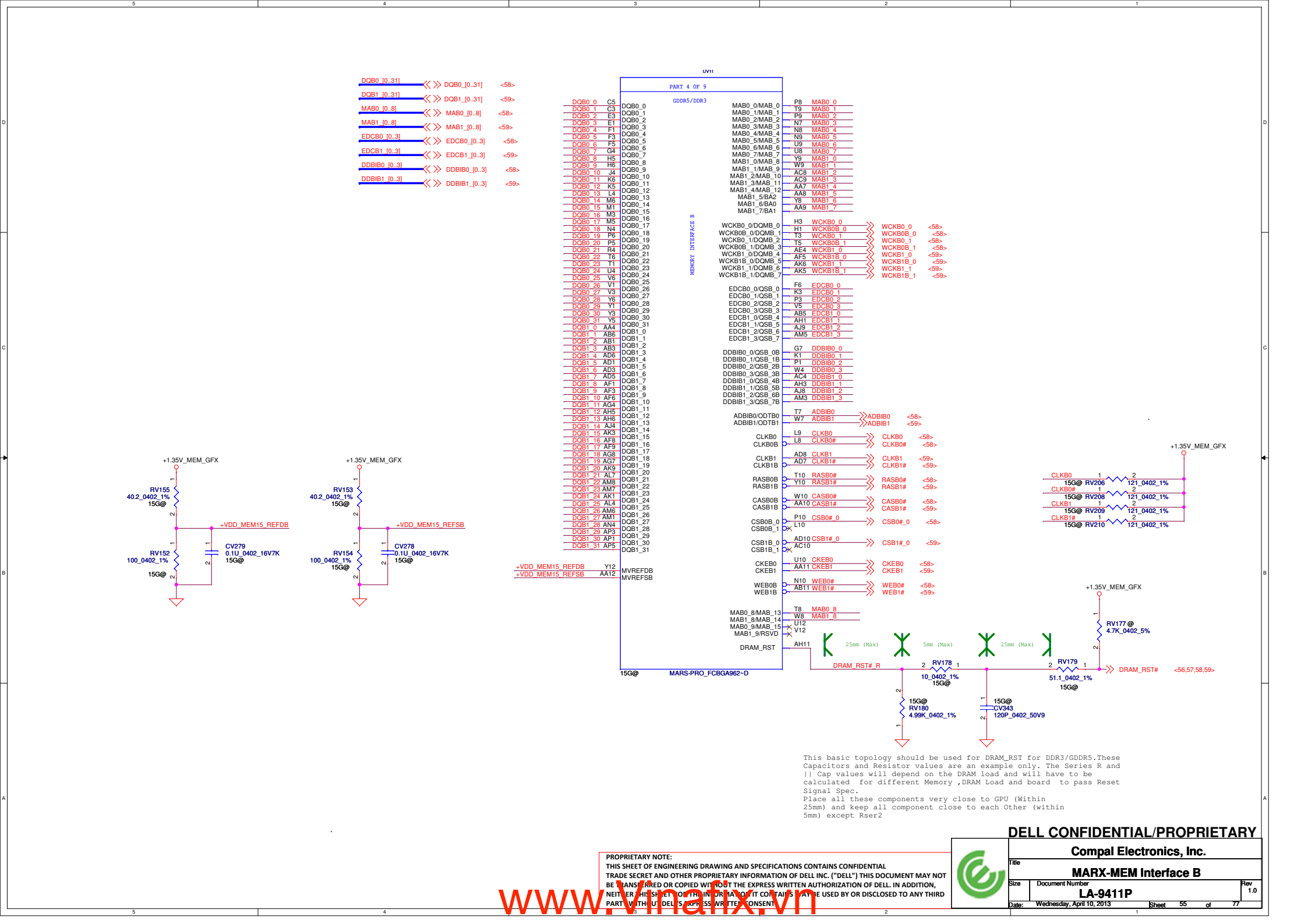
Title: MARX-MEM Interface A
Size: Document Number: LA-9411P
Rev: 1.0
Date: Wednesday, April 10, 2013 Sheet 54 of 77

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Compal Electronics, Inc.

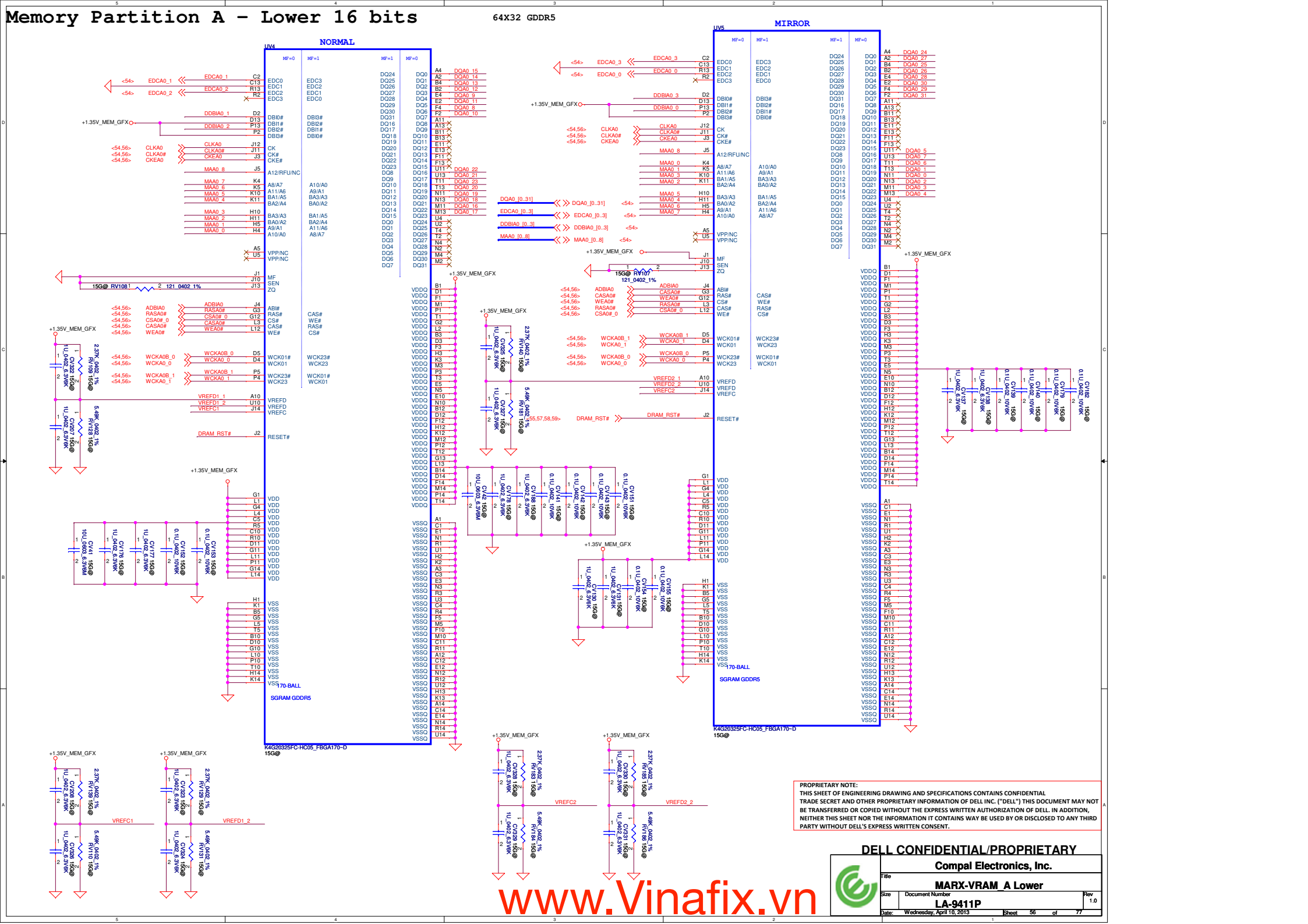
Title: MARX-MEM Interface B

Size | Document Number: LA-9411P | Rev: 1.0

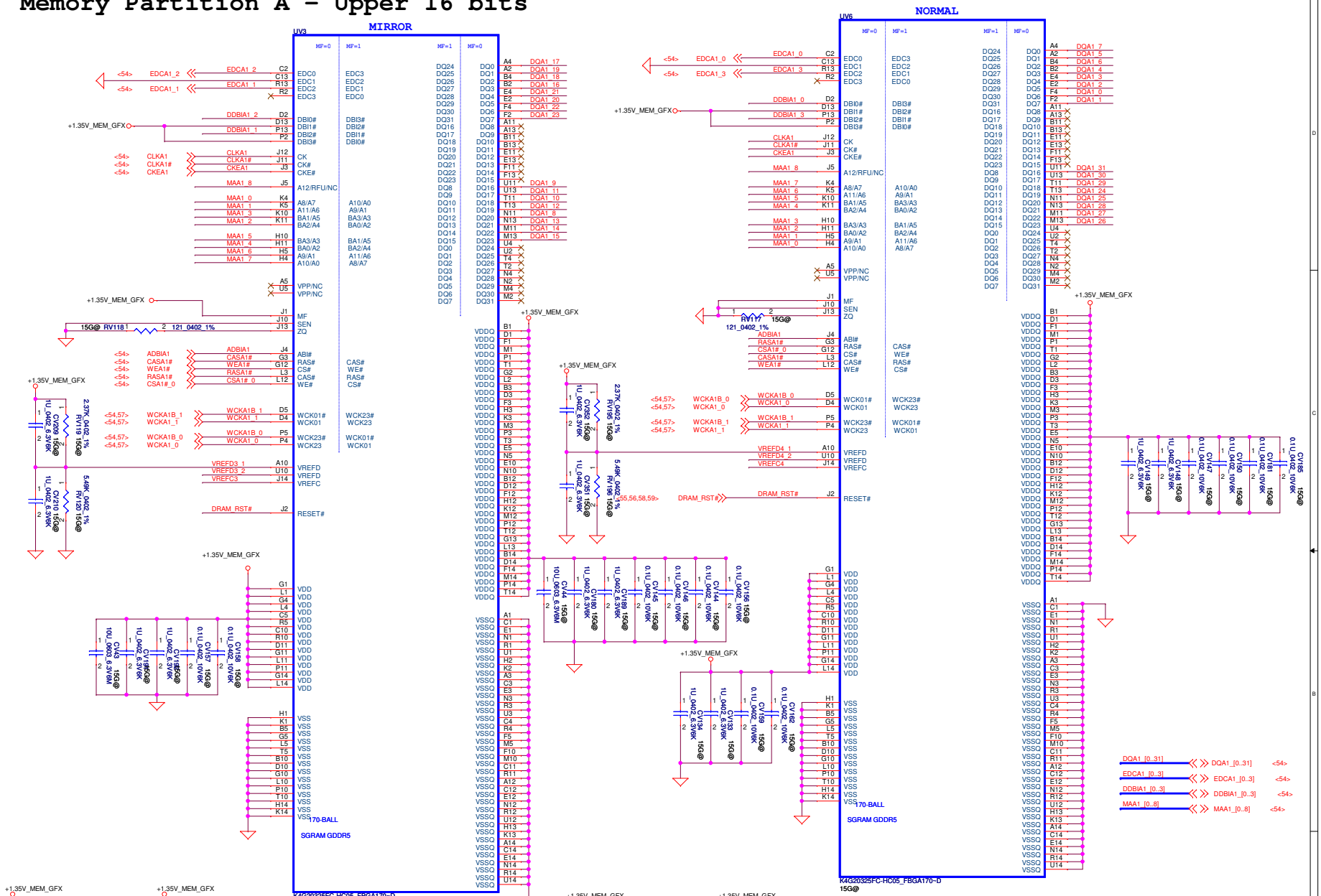
Date: Wednesday, April 10, 2013 | Sheet 55 of 77

# Memory Partition A – Lower 16 bits

64X32 GDDR5



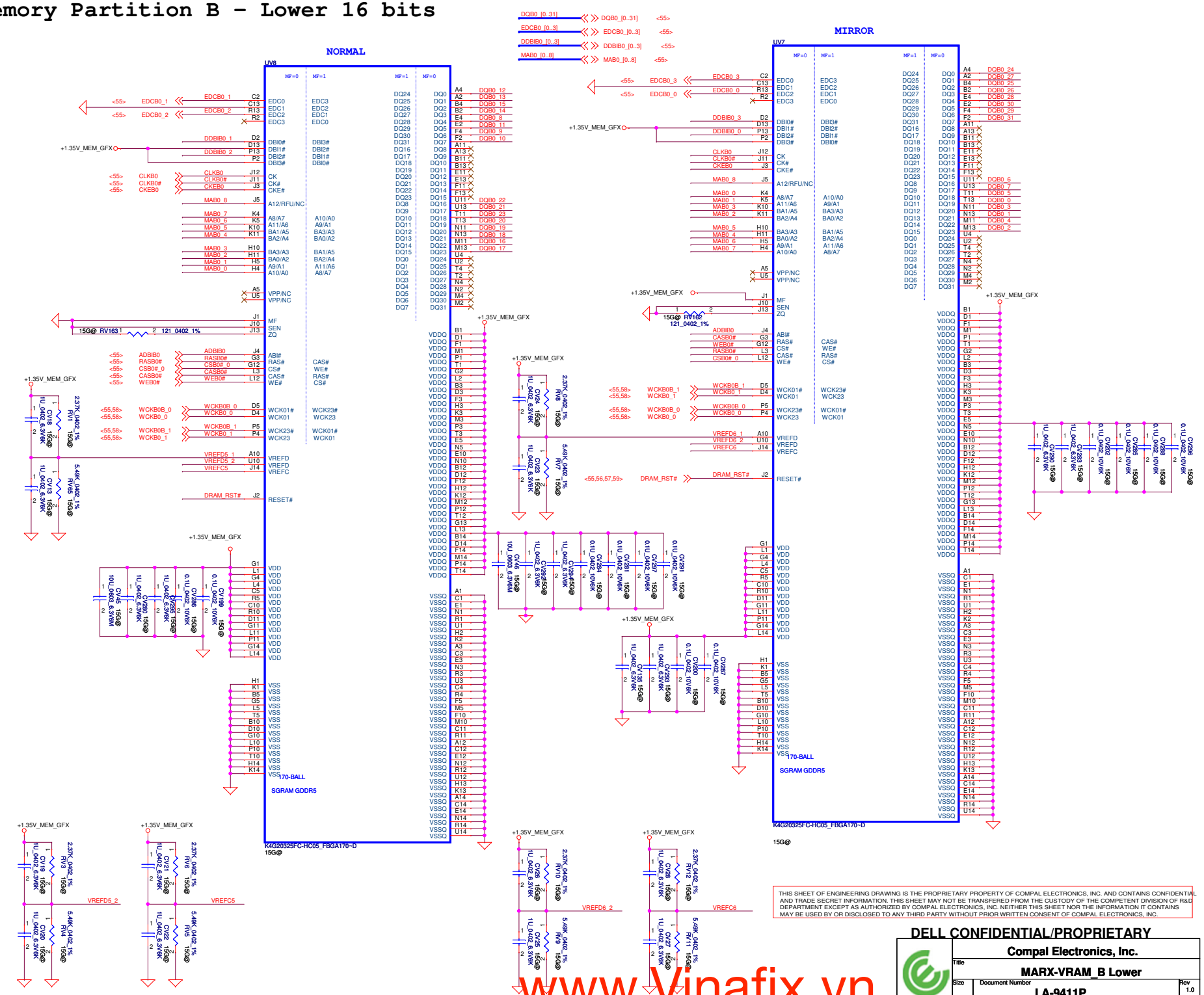
# Memory Partition A – Upper 16 bits






| | | |
|---|---|---|
| Compal Electronics, Inc. | | |
| Title: MARX-VRAM_A Upper | | |
| Size | Document Number: LA-9411P | Rev: 1.0 |
| Date: Wednesday, April 10, 2013 | Sheet 57 of 77 | |

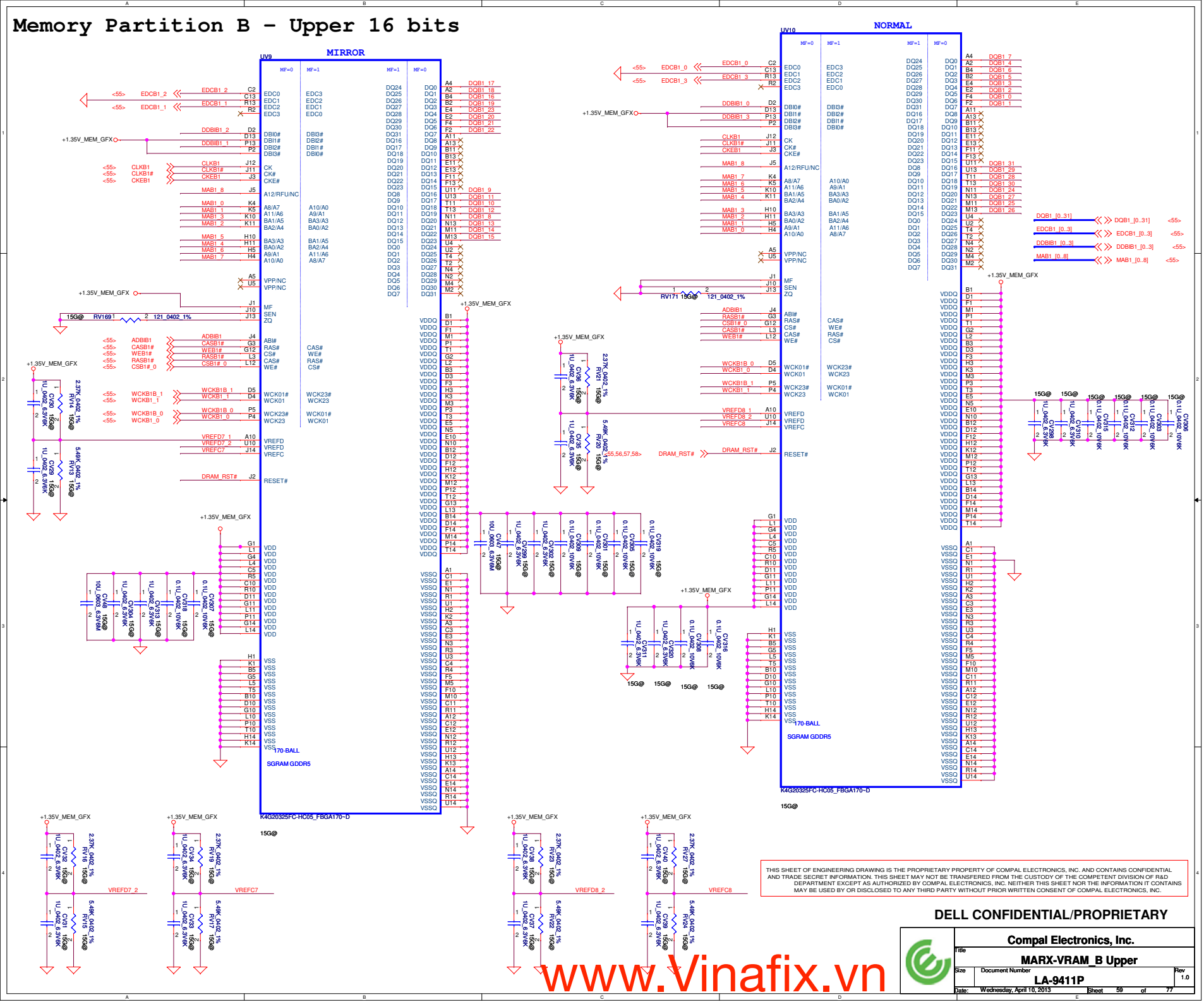
# Memory Partition B – Lower 16 bits





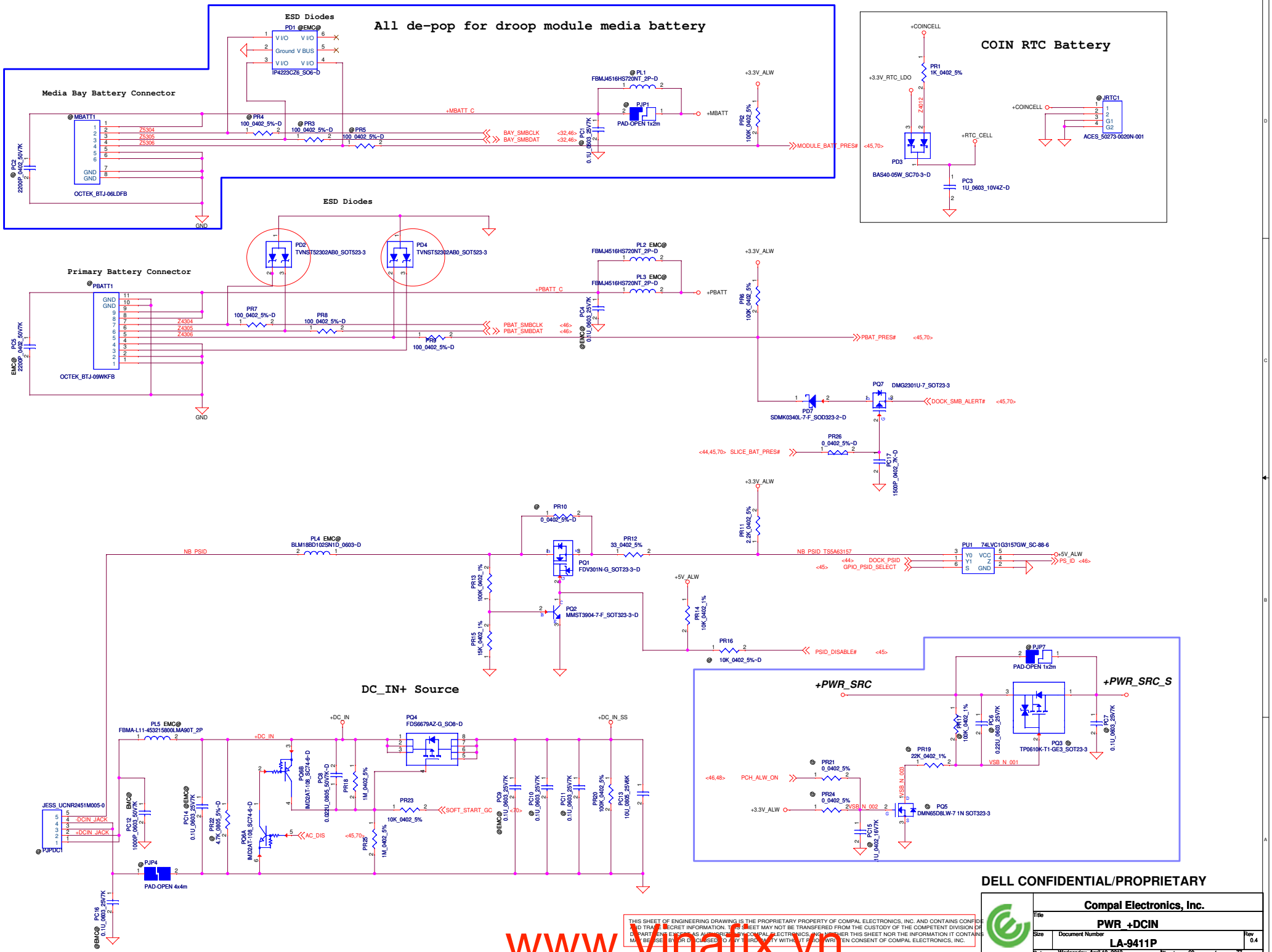

| | |
|---|---|
| Compal Electronics, Inc. | |
| Title | MARX-VRAM_B Lower |
| Size | Document Number: LA-9411P |
| Rev | 1.0 |
| Date: | Wednesday, April 10, 2013 |
| Sheet | 58 of 77 |

# Memory Partition B – Upper 16 bits



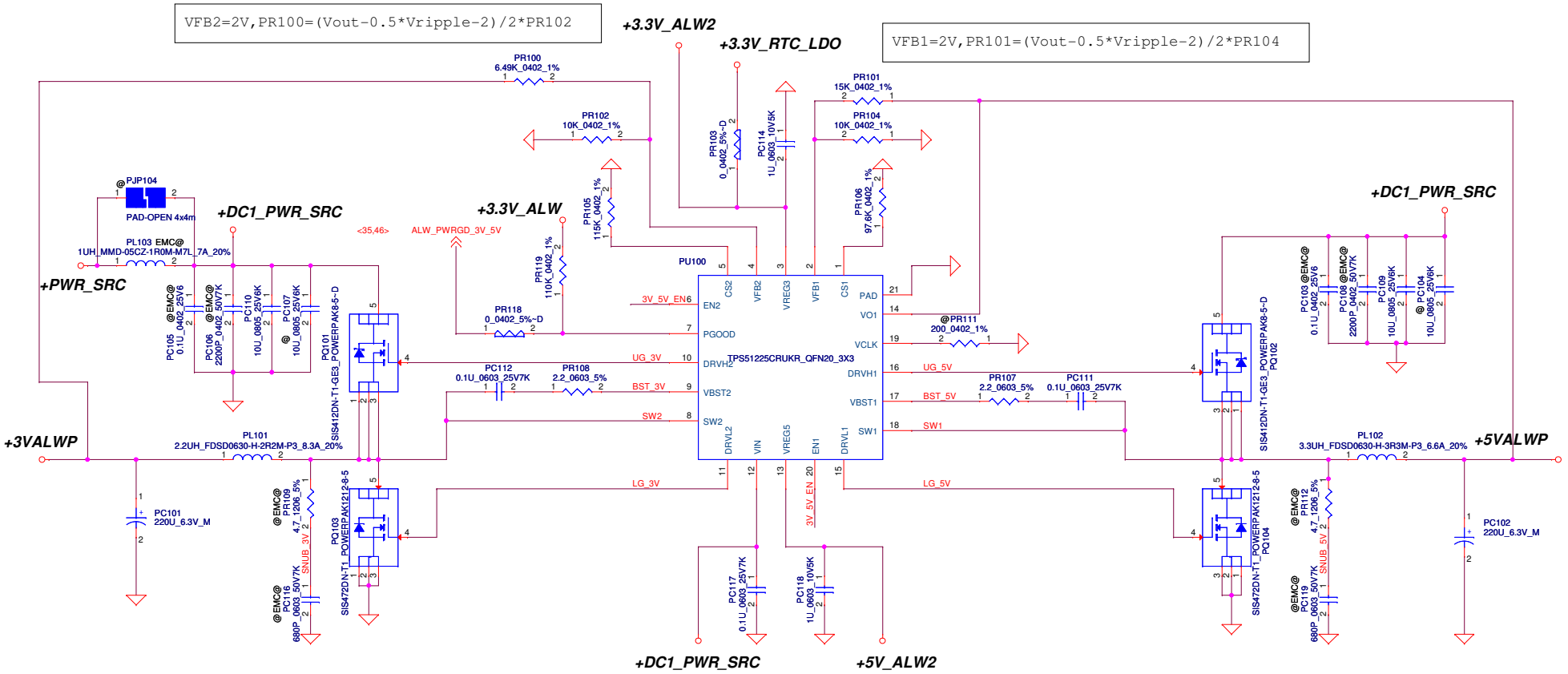



| | |
|---|---|
| Compal Electronics, Inc. | |
| Title | MARX-VRAM_B Upper |
| Size | Document Number: LA-9411P |
| Rev | 1.0 |
| Date: | Wednesday, April 10, 2013 |
| Sheet | 59 of 77 |






| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title: PWR_+DCIN | | | |
| Size | Document Number: LA-9411P | | Rev: 0.4 |
| Date: Wednesday, April 10, 2013 | Sheet 60 of 77 | | |




3VALWP
Ripple voltage -
Static load 3% / Dynamic load 5%
Frequency 350kHz
TDC 7.33A
Peak Current 10.48A
OCP current 12.57A

| | TYP | MAX |
|---|---|---|
| H/S Rds(on) | 24mohm , | 30mohm |
| L/S Rds(on) | 10.3mohm , | 12.4mohm |

Choke DCR Max:17mohm
Choke Ityp:8.3A / Isat:10.8A
Bulk cap ESR 15mohm

5VALWP
Ripple voltage -
Static load 3% / Dynamic load 5%
Frequency 300kHz
TDC 5.613A
Peak Current 8A
OCP current 9.6A

| | TYP | MAX |
|---|---|---|
| H/S Rds(on) | 24mohm , | 30mohm |
| L/S Rds(on) | 10.3mohm , | 12.4mohm |

Choke DCR Max:28mohm
Choke Ityp:6.6A / Isat:8.2A
Bulk cap ESR 15mohm

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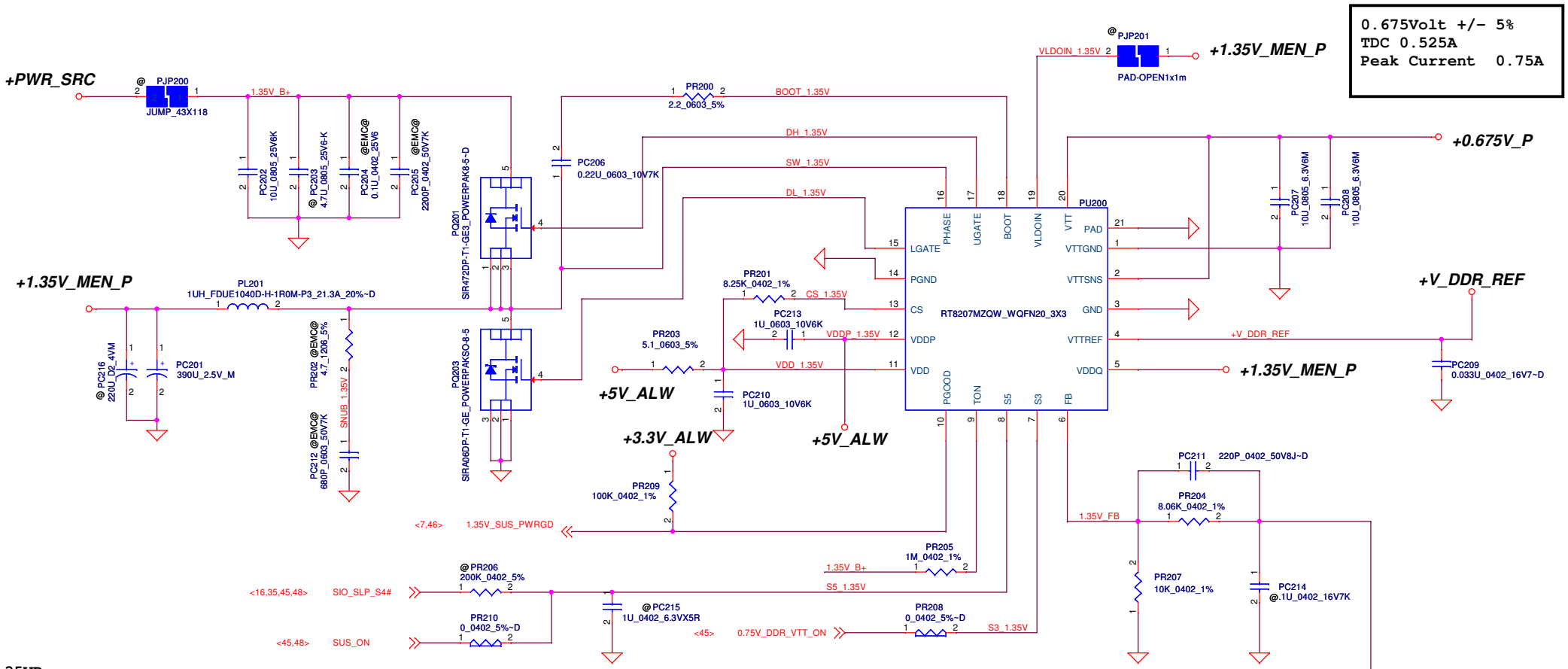
| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | Compal Electronics, Inc. |
| Issued Date | 2012/01/17 | Deciphered Date 2013/01/16 | Title: PWR_3VALWP/5VALWP |
| Size: B | Document Number: LA-9411P | | Rev: 0.4 |
| Date: Wednesday, April 10, 2013 | Sheet 61 of 77 | | |

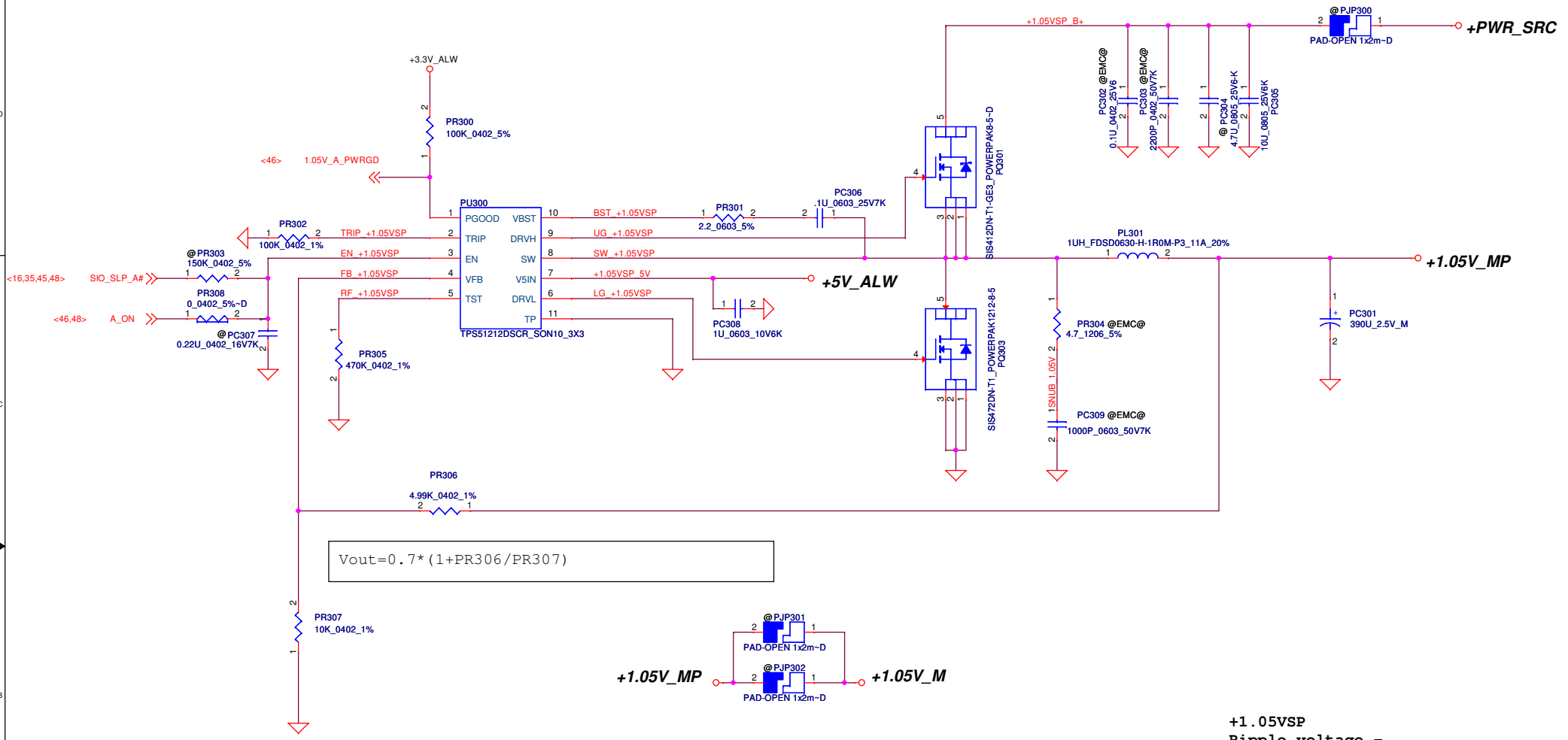





| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | Compal Electronics, Inc. |
| Issued Date | 2012/01/17 | Deciphered Date | 2013/01/16 |



| | | | |
|---|---|---|---|
| Title | PWR_1.35V/0.675VSP | | |
| Size | Document Number LA-9411P | | Rev 0.4 |
| Date: Wednesday, April 10, 2013 | Sheet 62 of 77 | | |




+1.05VSP
Ripple voltage -
Static load 3% / Dynamic load 5%
Frequency 290kHz
TDC 4.64A
Peak Current 6.5A
OCP current 7.8A

| | TYP | MAX |
|---|---|---|
| H/S Rds(on) | 24mohm , | 30mohm |
| L/S Rds(on) | 10.3mohm , | 12.4mohm |

Choke DCR 11mohm
Choke Ityp:11A / Isat:14.5A
Bulk cap ESR 10mohm

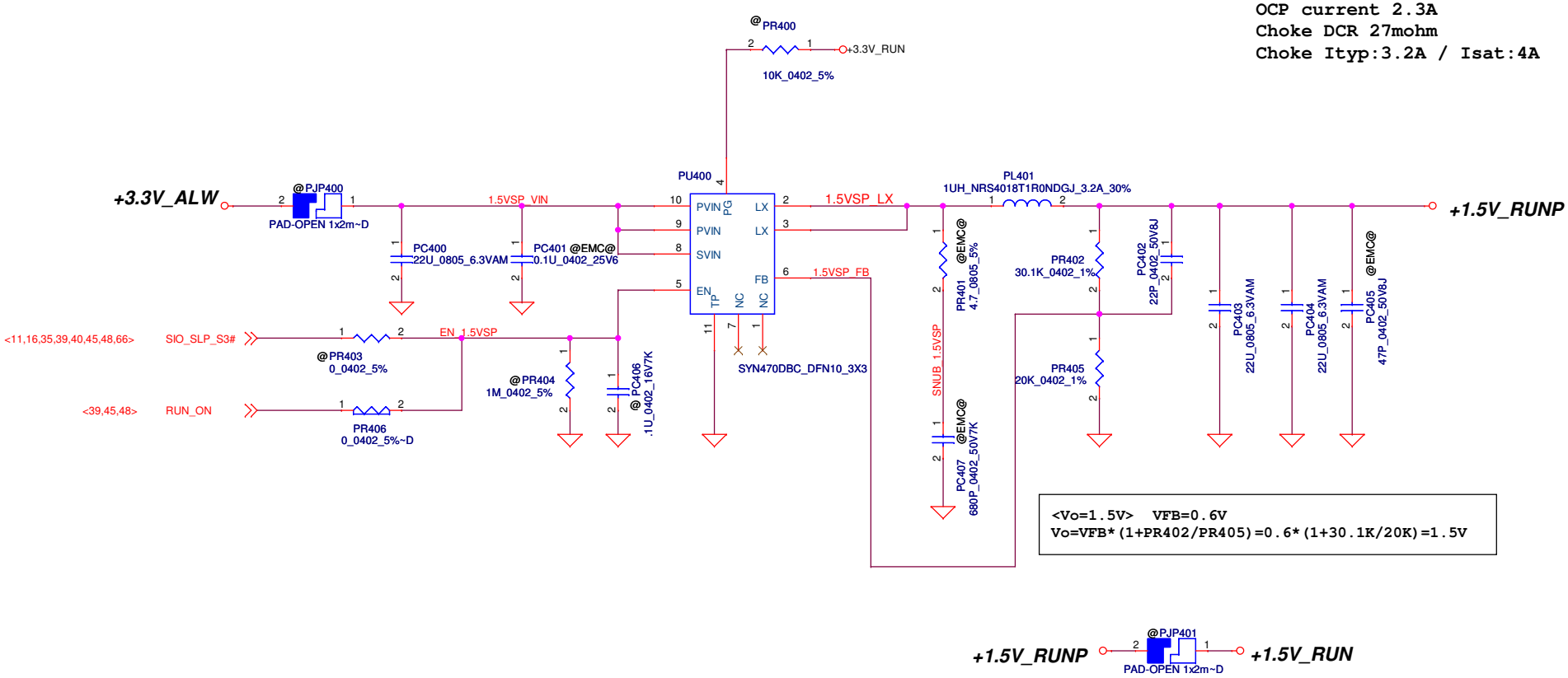


| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | Compal Electronics, Inc. |
| Issued Date | 2012/01/17 | Deciphered Date | 2013/01/16 |



Title: PWR_1.05VSP
Size: | Document Number: LA-9411P | Rev: 0.4
Date: Wednesday, April 10, 2013 | Sheet 63 of 77

+1.5VSP
Ripple voltage -
Static load 3% / Dynamic load 5%
Frequency 1MHz
TDC 1.329A
Peak Current 1.9A
OCP current 2.3A
Choke DCR 27mohm
Choke Ityp:3.2A / Isat:4A

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| | | |
|---|---|---|
| Compal Electronics, Inc. | | |
| Title: PWR_+1.5VSP | | |
| Size | Document Number: LA-9411P | Rev: 0.4 |
| Date: Wednesday, April 10, 2013 | Sheet 64 of 77 | |

PR507=21K, FW=400KHZ / VBOOT 1.7V

VCC_core (Base on PDDG rev 1.1)
TDC 27A
Peak Current 85A
DC Load line -1.5mV/A
Icc_Dyn_VID1 60A
OCP current 102A
Choke DCR 0.97m ohm
Choke Itype:19A / Isat:25A

Bulk cap 470u 4.5mohm *4
MLCC 10u *11 / 22u *19

| | TYP | MAX |
|---|---|---|
| H/S Rds(on) | :12.2mohm , | 15mohm |
| L/S Rds(on) | :2.75mohm , | 3.5mohm |

Local sense put on HW site





Compal Electronics, Inc.

Title: PWR_VCORE_ISL95812 for QC

Size: | Document Number: LA-9411P | Rev: 0.4

Date: Wednesday, April 10, 2013 | Sheet 65 of 77

Initial voltage is 0.85V

| VID4 | VID3 | VID2 | VID1 | VID0 | Vo |
|---|---|---|---|---|---|
| 0 | 1 | 1 | 0 | 1 | 1.175 |
| 0 | 1 | 1 | 1 | 0 | 1.15 |
| 0 | 1 | 1 | 1 | 1 | 1.125 |
| 1 | 0 | 0 | 0 | 0 | 1.1 |
| 1 | 0 | 0 | 0 | 1 | 1.075 |
| 1 | 0 | 0 | 1 | 0 | 1.05 |
| 1 | 0 | 0 | 1 | 1 | 1.025 |
| 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 0.975 |
| 1 | 0 | 1 | 1 | 0 | 0.95 |
| 1 | 0 | 1 | 1 | 1 | 0.925 |
| 1 | 1 | 0 | 0 | 0 | 0.9 |
| 1 | 1 | 0 | 0 | 1 | 0.875 |
| 1 | 1 | 0 | 1 | 0 | 0.85 |
| 1 | 1 | 0 | 1 | 1 | 0.825 |
| 1 | 1 | 1 | 0 | 0 | 0.8 |
| 1 | 1 | 1 | 0 | 1 | 0.775 |

VCC_GFXCORE
Frequency 300kHz
TDC 38A
Peak Current 57A
OCP current 68.4A

| | TYP | MAX |
|---|---|---|
| H/S Rds(on) | :12.2mohm , | 15mohm |
| L/S Rds(on) | :2.75mohm , | 3.5mohm |

Choke DCR 0.97mohm
Choke Itype:19A / Isat:25A

Bulk cap 470u 4.5mohm *4
MLCC 1u *30 / 10u *4

Layout Note:
Place near Phase1 Choke

OCP setting
Ri = PR659

ISL62883CHRTZ-TQFN40_5X5

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Compal Electronics, Inc.

Title: PWR_+GPU_CORE

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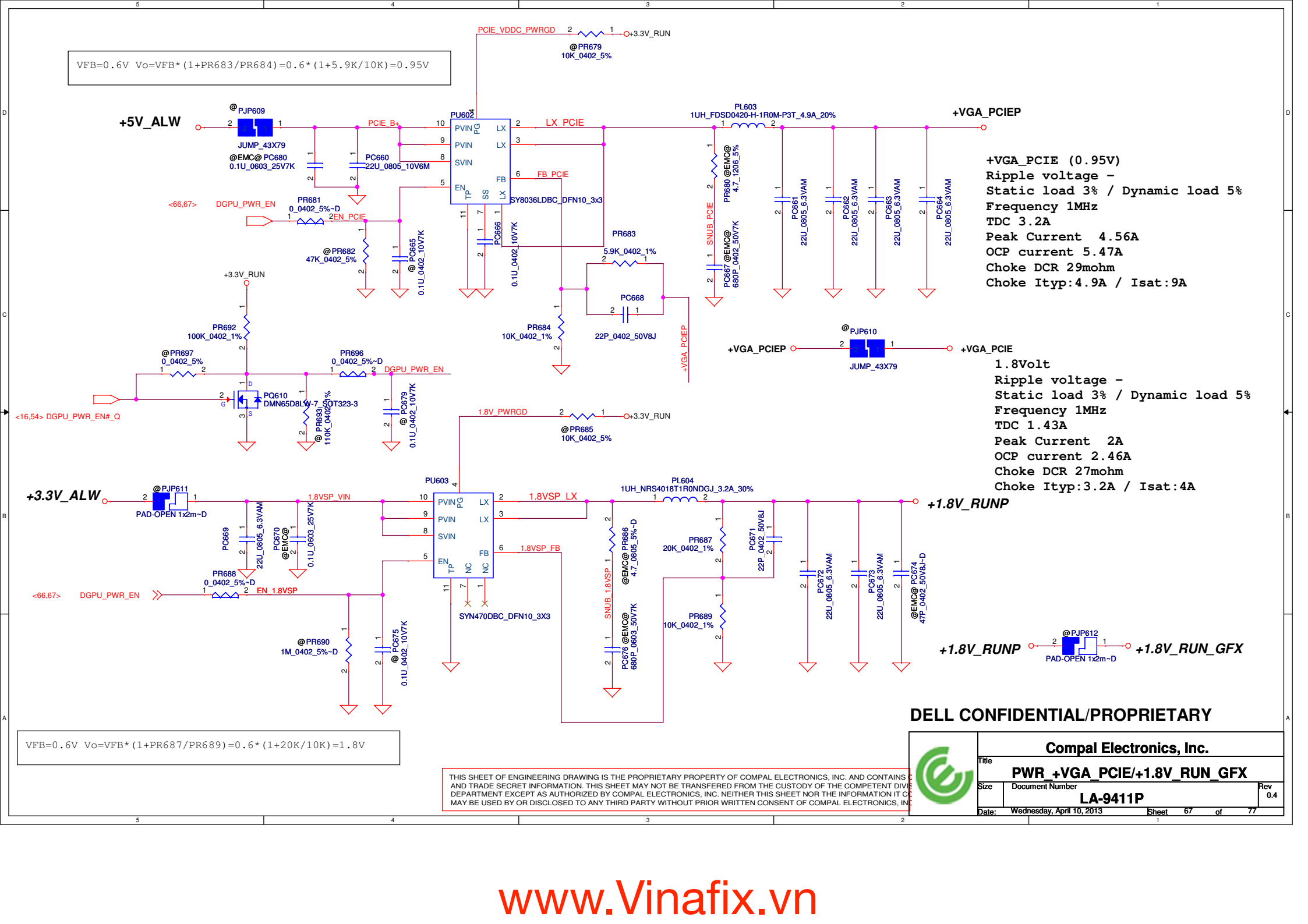
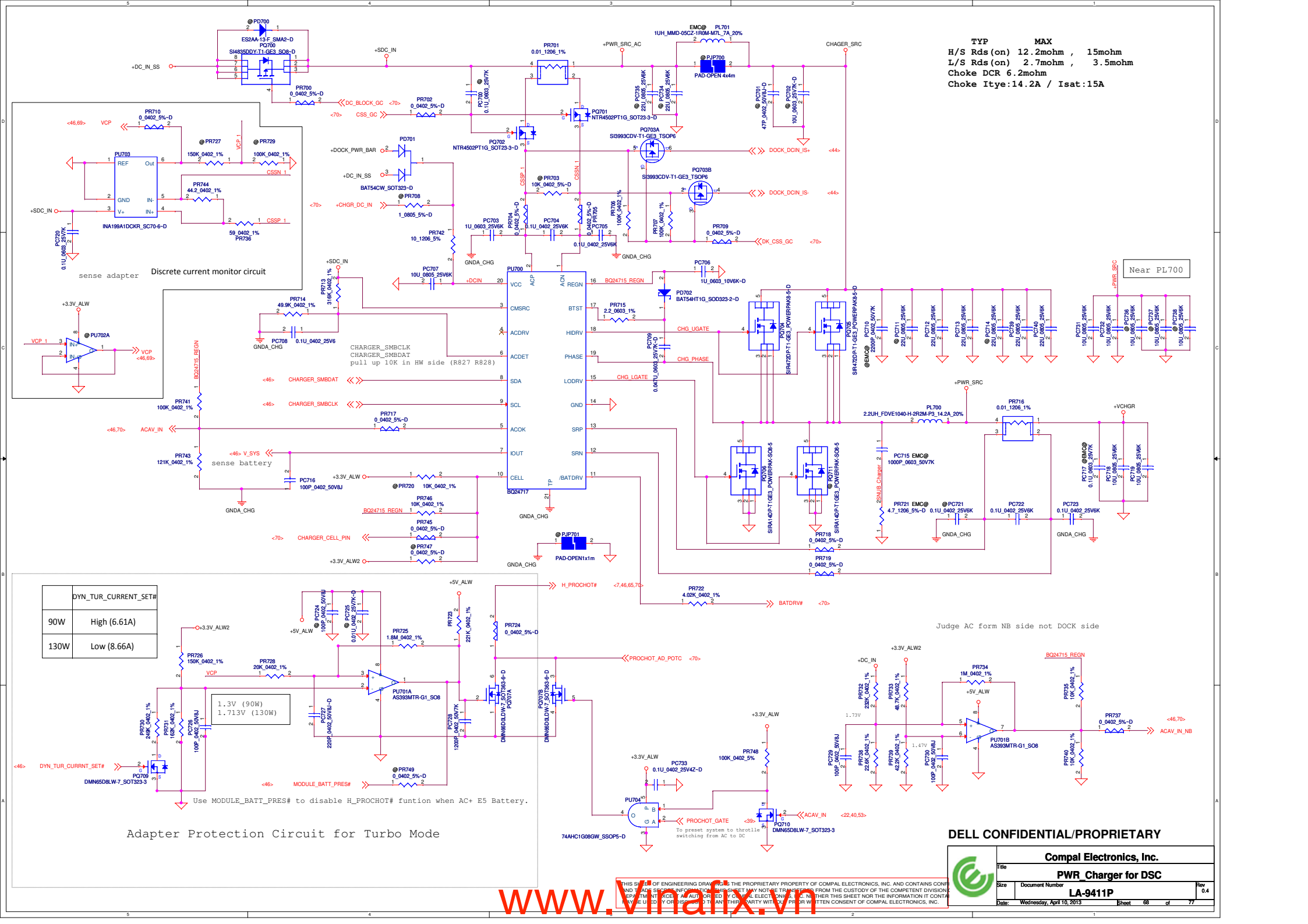
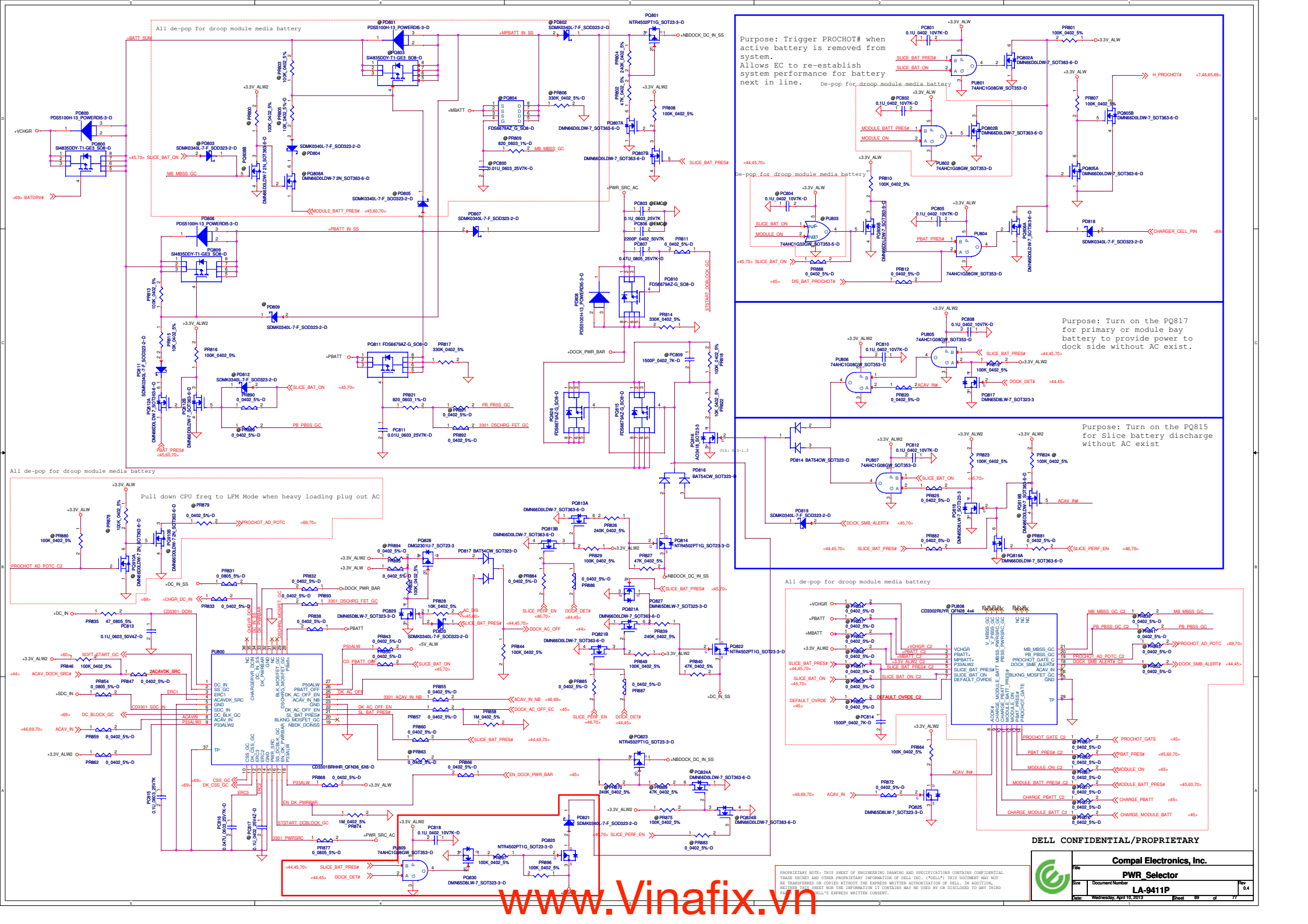
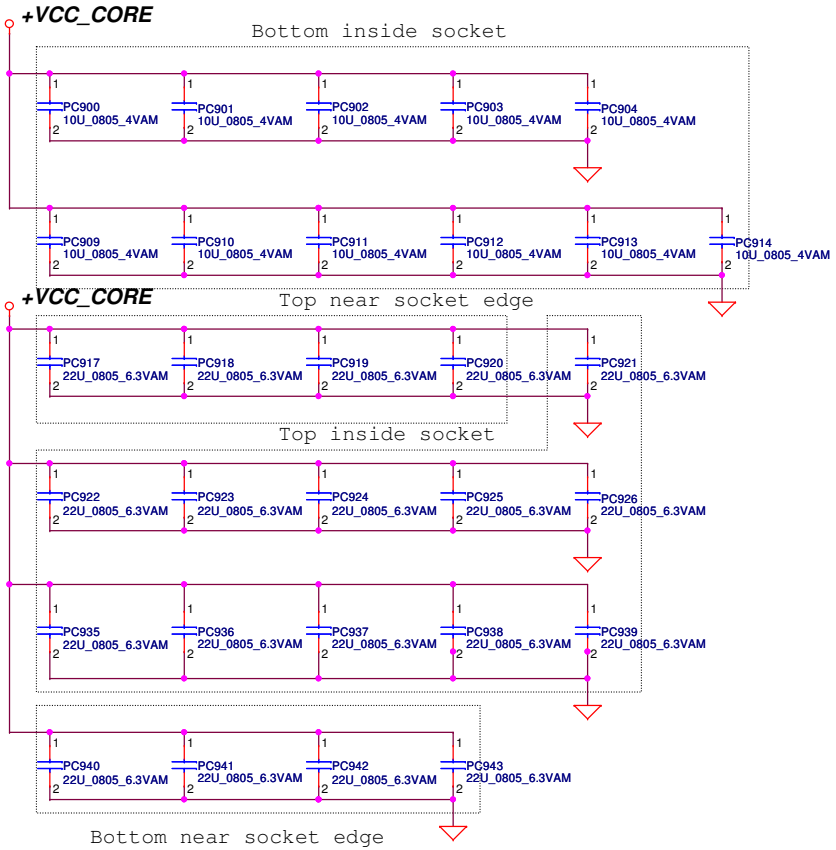


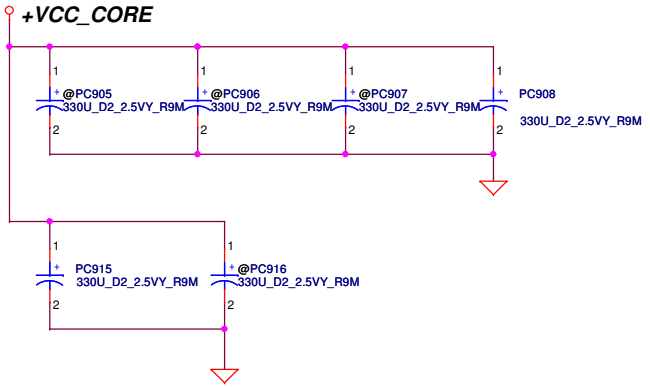


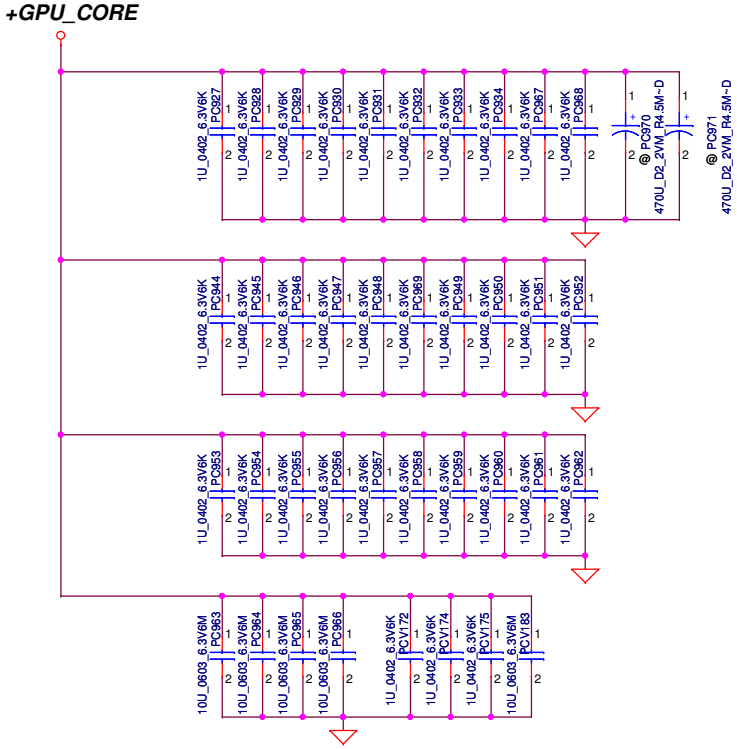

| | DYN_TUR_CURRENT_SET# |
|---|---|
| 90W | High (6.61A) |
| 130W | Low (8.66A) |



Based on PDDG rev 1.1 Table 5-1.

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Title: PWR_PROCESSOR DECOUPLING

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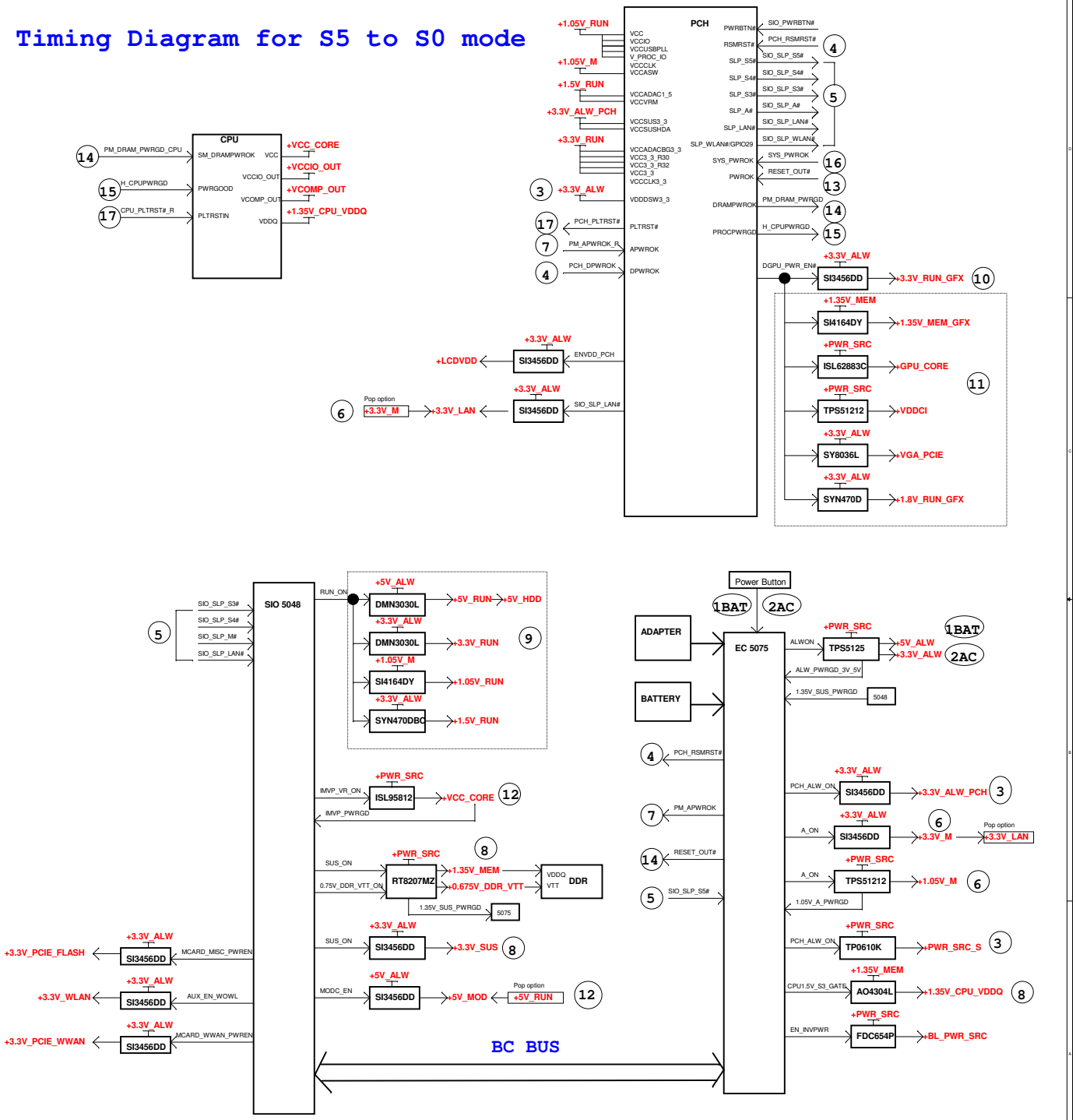
# Timing Diagram for S5 to S0 mode

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Power Sequence

LA-9411P

# Version Change List ( P. I. R. List )

| Item | Page# | Title | Date | Request Owner | Issue Description | Solution Description | Rev. |
|---|---|---|---|---|---|---|---|
| 1 | 7 | HW | 8/24/2012 | COMPAL | Change DRAMPWROK Pull up Power rail to Suspend | Base on EDS 1.0 (page124).<br>Change RC4 PM_DRAM_PWRGD pull up power rail to +3.3V_ALW_PCH. | X00(0.2) |
| 2 | 16 | HW | 8/24/2012 | COMPAL | Remove DGPU_HOLD_RST# double pull up. | Remove RH74 DGPU_HOLD_RST# pull up. | X00(0.2) |
| 3 | 20 | HW | 8/24/2012 | COMPAL | Remove mCARD_PCIE_SATA# double pull up. | Remove RH196 mCARD_PCIE_SATA# pull up. | X00(0.2) |
| 4 | 48 | HW | 8/27/2012 | COMPAL | Correct DC to DC interface Pull up power rail to +PWR_SRC_S | R905.1, R911.1, R917.1, R930.1, R906.1 and R912.1 change to +PWR_SRC_S | X00(0.2) |
| 5 | 13,14 | HW | 8/27/2012 | COMPAL | Follow DG DDR3L VREF_DQ Control as page120. it pull up power rail should be +1.35V_MEM | Modify RD19.1, RD22.1, RD15.1 net name to +1.35V_MEM. | X00(0.2) |
| 6 | 46,16 | HW | 8/30/2012 | COMPAL | Follow EDS page 131 as DSW rail | Modify AC_PRESENT R835.1 to +PCH_VCCDSW3_3<br>Add PCH_PCIE_WAKE# RH92.1 to +PCH_VCCDSW3_3<br>De-populate RH78 with +3.3V_ALW_PCH power rail | X00(0.2) |
| 7 | 46 | HW | 8/27/2012 | COMPAL | Correct GPU_SMBDAT,GPU_SMBCLK Pull up power rail to +3.3V_RUN | Modify GPU_SMBDAT R829,1,GPU_SMBCLK R822.1 to +3.3V_RUN | X00(0.2) |
| 8 | 33 | HW | 8/27/2012 | COMPAL | Change LANWAKE#_R Pull up power rail tO +3.3V_LAN | Modify R558.1 power rail to +3.3V_LAN | X00(0.2) |
| 9 | 46 | HW | 8/29/2012 | COMPAL | Modify THERMATRIP2# control by +VCCIO_OUT | Modify Q4.2 to +VCCIO_OUT. | X00(0.2) |
| 10 | 47 | HW | 8/27/2012 | COMPAL | Back E4 RSMRST RESET IC solution and add pull up at PCH_RSMRST#_Q | Modify U8 to RT9818A-44GU3<br>Add Pull up 8.2Kohm to +3.3V_ALW_PCH on PCH_RSMRST#_Q | X00(0.2) |
| 11 | 35 | HW | 8/27/2012 | COMPAL | Back E4 JUSH pin out | JUSH1 back to 20pins. | X00(0.2) |
| 12 | 51 | HW | 8/27/2012 | AMD | Modify GPU power net | +VDDCI change to +GPU_CORE power net | X00(0.2) |
| 13 | 48 | HW | 8/27/2012 | COMPAL | Correct +1.35V_CPU_VDDQ Discharge net name | Modify R926.2 Net name to +1.35V_CPU_VDDQ | X00(0.2) |
| 14 | 36 | HW | 8/27/2012 | COMPAL | Update OZ777 ES2 symbol | U38 OZ777FJ2LN_QFN48P_6X6 symbol updated | X00(0.2) |
| 15 | 38 | HW | 8/27/2012 | COMPAL | Replace U7 SATA Repeater and U95 SATA/PCIE SW by U7 ASM1467 SATA/PCIE Repeater. | Modify U7 circuit | X00(0.2) |
| 16 | 33,34 | HW | 9/4/2012 | COMPAL | LAN LED support unobtrusive mode on System board | Modify Q325,Q326 LAN LED control circuit between LAN SW MB and MB CONN. | X00(0.2) |
| 17 | 16 | HW | 8/27/2012 | COMPAL | Base on EDS 1.0 Page 124 Modify SIO_SLP_LAN# to DSW Power rail | Modify SIO_SLP_LAN# RH80.1 to +PCH_VCCDSW3_3 | X00(0.2) |
| 18 | 37 | HW | 8/27/2012 | COMPAL | Modify CPPE#, USB_MCARD1_DET# Pull up power rail to +3.3V_RUN | Modify CPPE# R737.2, USB_MCARD1_DET# R739.2 net name to +3.3V_RUN | X00(0.2) |
| 19 | 29 | HW | 8/28/2012 | DELL | Cost Down Concept | Replace(U21,U24)NOT Gate by(Q5, Q6)N-Channel MOSFET with Pull high resistor on CA_DET# | X00(0.2) |
| 20 | 30 | HW | 8/28/2012 | REALTEK | Codec AGND to DGND modify | Replace C981, C982, C983 0.1uf by R5,R6,R15 0ohm | X00(0.2) |
| 21 | 50 | ESD | 8/29/2012 | COMPAL | Reserve GPU_HOT# control by H_PROCHOT# | Reserve H_PROCHOT# with level shift circuit to control GPU_HOT# | X00(0.2) |

# Version Change List ( P. I. R. List )

| Item | Page# | Title | Date | Request Owner | Issue Description | Solution Description | Rev. |
|---|---|---|---|---|---|---|---|
| 22 | 24 | ME | 8/30/2012 | COMPAL | ME request | Change SW1 power switch to SN11100580L SKRBAAE010_4P~D | X00(0.2) |
| 23 | 45 | HW | 9/3/2012 | DELL | GPIO MAP2.4 | 1.Assign ECE5048_TX at 5048 GPIOE1/TXD<br>2.Remove 1.8V_RUN_PWRGD across X5 at 5048 GPIOK2 pin B10.<br>3.Move USB_PWR_SHR_EN# to GPIOK2 pin B10<br>4.Free up 5048 GPIOG3 (DYN_TURB_PWR_ALRT# ),de-populate R796 | X00(0.2) |
| 24 | 35 | HW | 9/4/2012 | COMPAL | Follow INTEL Check list 1.0 reserve JAPS1 pin4, 7 connection | 1.Reserve JAPS1 PIN4 of R23 SIO_SLP_S5# and R17 +3.3V_ALW_PCH<br>2.Reserve JAPS1 PIN7 of R24 +3.3V_ALW | X00(0.2) |
| 25 | 46 | HW | 9/18/2012 | COMPAL | Added a 0ohm at U51 VTR_ADC pin. | Added R839 0ohm between +3.3V_ALW and U51.A58 pin. | X01(0.3) |
| 26 | 47 | HW | 9/19/2012 | INTEL | Stuff RTC cell can't power on issue | Reserve R1636 pull down resistor on PCH_RSMRST#_Q. | X01(0.3) |
| 27 | 20,46 | HW | 9/24/2012 | COMPAL | GPIO MAP2.5 | 1.Remove POA_WAKE# at 5075 VCI_INT3# pin B68<br>2.Remove FP_POA_EN at 5048 GPIOL7/PWM5 pin A44.<br>3.Rename LANWAKE# to EC_WAKE# at 5048 GPIOL5/PWM2 pin B1.<br>4.Add LANWAKE# connect to 5075 pin B27<br>5.Reserve 0ohm between LANWAKE# and EC_WAKE# | X01(0.3) |
| 28 | 11 | HW | 9/24/2012 | COMPAL | HSW will internally power gate the VDDQ rail (+1.35V_CPU_VDDQ) | 1.De-populated the +1.35V_CPU_VDDQ DC to DC circuit<br>2.add these two PJP5, PJP6 4x4mm Jumper between +1.35V_CPU_VDDQ and +1.35V_MEM power net. | X01(0.3) |
| 29 | 46 | HW | 9/24/2012 | COMPAL | Follow CRB1.2 PECI circuit | De-populate PECI_EC_R C290 CAP. | X01(0.3) |
| 30 | 36 | HW | 9/24/2012 | COMPAL | O2 Request | Add C802 0.1uF cap on SD_CD#. | X01(0.3) |
| 31 | 30 | HW | 10/03/2012 | COMPAL | When no external power, it Sleeve will be floating mode and no reference GND. | Add AUD_NB_MUTE# to control Sleeve pin. | X01(0.3) |
| 32 | 16 | HW | 9/26/2012 | COMPAL | Follow CRB, PCH_DPWROK circuit | Add RH120 100Kohm PD and close to PCH site. | X01(0.3) |
| 33 | 32 | HW | 9/26/2012 | COMPAL | Follow EDS, Change USB30_SMI# (GPIO13) pull up power rail to +3.3V_ALW_PCH. | Change R514.1 to +3.3V_ALW_PCH | X01(0.3) |
| 34 | 38 | HW | 10/02/2012 | Asmedia | Asmedia ASM1467 spec modify | 1.Pin7 GND chage DE_A<br>2.Pin6 Reserved change to GND<br>3.Pin16 MOSEL change to Reserved<br>4.Pin17 DE_A change to MOSEL | X01(0.3) |
| 35 | 27 | HW | 9/26/2012 | COMPAL | Change EDP to LVDS converter solution to RTD2136R | 1.Change U27 P/N:SA000067100(S IC RTD2136R-CG QFN 48P DP/LVDS CTRL)<br>2.Remove R102,R103 0ohms<br>3.Remove R107 4.7Kohm<br>4.Add R108 4.7Kohm<br>5.Remove U26 CAT24C64WI-GT3_SO8 EEROM | X01(0.3) |
| 36 | 28 | HW | 10/02/2012 | COMPAL | Fix LCD T3 timing issue | Add R115 0ohm between LCD_ENVDD_CVT and U55.4 net to control +LCD_VDD power net. | X01(0.3) |
| 37 | 30 | HW | 10/04/2012 | COMPAL | Reserve Support universal jack | 1.C195,C196 4.7U_0603_6.3V6K~D<br>2.R198,R199 1K_0402_5%<br>3.R209,R210 4.7K_0402_5%~D<br>4.D11,D12 RB751VM-40TE-17_SOD323-2~D | X01(0.3) |
| 38 | 20,35 | HW | 10/05/2012 | COMPAL | GPIO MAP2.6 | 1.Add SMART_DET# on PCH GPIO15 and JUSH1 pin11.<br>2.Move EC_WAKE# from ECE5048[L]5 to MEC5075 GPIO52.<br>3.Add ECE5048_PWRGD to MEC5075 GPIO102<br>4.Add AND Gate of ECE5048_PWRGD, RUNPWROK to AND_PWRGD on ECE5048 A4 pin<br>5.Remove R842 pull up resistor | X01(0.3) |







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| Item | Page# | Title | Date | Request Owner | Issue Description | Solution Description | Rev. |
|---|---|---|---|---|---|---|---|
| 39 | 30 | HW | 10/08/2012 | COMPAL | Remove IDT& TI Audio codec co-lay circuit | Remove IDT& TI Audio codec co-lay circuit | X01(0.3) |
| 40 | 37 | HW | 10/08/2012 | COMPAL | Remove +1.5V_RUN power rail on JMINI3 card | 1.Remove +1.5V_RUN power rail on JMINI3 card of pin6, 28 and 48<br>2.Remove C619, C620 cap | X01(0.3) |
| 41 | 54 | HW | 10/11/2012 | COMPAL | Correct DGPU_PWR_EN# behavior | Add QV5 | X01(0.3) |
| 42 | 30 | HW | 10/11/2012 | REALTEK | Follow Realtek recommend circuit | 1.Change L91,92,93,94 to R41,42,43,44 0_0603_5%~D<br>2.Change C973,974,975,76 1000P_0402_50V8-J<br>3.Change R1680,1681,1682,1683 0_0402_5%~D | X01(0.3) |
| 43 | 11 | HW | 10/25/2012 | COMPAL | Follow CRB1.5 design | 1. De-populate 10UF CC26,CC27,CC28,CC29,CC30,CC31,CC32,CC33<br>2. De-populate 22UF CC41,CC37,CC42,CC43,CC38,CC44,CC39,CC45.CC46<br>3. De-populate 330UF CC34 | X01(0.3) |
| 44 | 11 | HW | 10/25/2012 | COMPAL | Support Deep SX mode | 1. De-populate RH79 0_0402<br>2. Populate R802 0_0402 | X01(0.3) |
| 45 | 30 | HW | 12/25/2012 | COMPAL | Follow Realtek recommend circuit | 1.Change R1658,R1095 to jump<br>2.Change R1119 ,R1120 to 100K<br>3.Change R1677 R1679 to 9.1 ohm<br>4.Remove R25 | X02(0.4) |
| 46 | 50 | HW | 12/25/2012 | COMPAL | Follow AMD recommend | Change GPU_HOT# pull high fomr 100K to 4.7K | X02(0.4) |
| 47 | 28 | HW | 12/25/2012 | COMPAL | Samsnug PANEL issue | Add pull down R1139 100K | X02(0.4) |
| 48 | 20 | HW | 12/25/2012 | COMPAL | TLS issue | Change RH229 fomr 200K to 1K | X02(0.4) |
| 49 | 46 | HW | 12/25/2012 | COMPAL | Follow DELL recommend | add 0ohm to short RUNPWROK and AND_PWRGD | X02(0.4) |
| 50 | 36 | HW | 12/25/2012 | COMPAL | Follow GPIO map rev 3.0C | SP_TPM_LPC_EN reserve PCH GPIO22 to control | X02(0.4) |
| 51 | 13,14 | HW | 12/25/2012 | COMPAL | Follow CRB1.5 DDR RAM M1&M3 circuit | Reserve circuit to control<br>1.+SA_DIMM1_VREFDQ ,+SA_DIMM2_VREFDQ<br>2.+SM_VREF_DIMM<br>3.DDR3_DRAMRST#_R | X02(0.4) |
| 52 | 30 | HW | 12/25/2012 | COMPAL | Follow ESD | Remove D83,D23,D8,D37,DE1&DE2 | X02(0.4) |
| 53 | 36 | HW | 03/28/2013 | COMPAL | Follow O2 recommend | add R493 on SD_CD# | A00(1.0) |





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| Item | Page# | Title | Date | Request Owner | Issue Description | Solution Description | Rev. |
|---|---|---|---|---|---|---|---|
| 1 | 66 | +GPU_CORE | 8/29 | AMD | GPU_CORE merged with one of AMD Chip power rail - VDDCI | Delete VDDCI Power rail page | X00 (0.2) |
| 2 | 60 | +DC_IN | 8/29 | Compal | ESD Team change solution | Change PD1 PD2 Solution | X00 (0.2) |
| 3 | 68 | Charger for DSC | 8/29 | Compal | SMBus connection is wrong | Swap net CHARGER_SMBDAT and CHARGER_SMBCLK | X00 (0.2) |
| 4 | 67 | +VGA_PCIE/ +1.8V_RUN_GFX | 8/29 | Compal | DGPU_PWR_EN signal pull high voltage net is wrong | Change PR692 Pin1 net from +3.3V_ALW to +3.3V_RUN | X00 (0.2) |
| 5 | 61 | 3VALWP/5VALWP | 8/29 | Compal | Find tune 3V/5V OCP setting | Change PR105 from 110k to 115k for 3.3V<br>Change PR106 from 82.5k to 86.6k for 5V | X00 (0.2) |
| 6 | 62 | 1.35V/0.675VSP | 8/29 | Compal | Change Enable signal from SIO_SLP_S4# to SUS_ON by HW request | Pop PR210 and depop PR206 | X00 (0.2) |
| 7 | 63 | 1.05VSP | 8/29 | Compal | Fint tune 1.05VSP OCP setting | Change PR302 from 64.9k to 68.1k | X00 (0.2) |
| 8 | 65 | VCORE_ISL95812 for QC | 8/29 | Compal | Fint tune DC loadline | Change PR537 from 2.55k to 2.37k | X00 (0.2) |
| 9 | 66 | +GPU_CORE | 8/29 | AMD | Adjust OCP setting for +GPU_CORE merge with VDDCI | Change PR659 from 787 to 1.37k | X00 (0.2) |
| 10 | 66 | +GPU_CORE | 8/29 | AMD | Adjust initial voltage from 1.125V to 0.85V | Pop PR602 PR604 PR608 PR605 PR610 PR612<br>Depop PR606 PR611 PR613 PR601 PR603 PR609 | X00 (0.2) |
| 11 | 65 | VCORE_ISL95812 for QC | 9/25 | Compal | Fint tune DC loadline | Change PR535 from 475ohm to 511ohm<br>Change PR537 from 2.37k to 2.55k | X01 (0.3) |
| 12 | 65 | VCORE_ISL95812 for QC | 9/25 | INTERSIL | Change schematic setting for new version IC (Rev3p0) | Change PR529 from 0 to 6.04k<br>Change PR512 from 21k to 16.9k<br>Change PR507 from 49.9k to 21k<br>Change PR509 from 34k to 3.24k | X01 (0.3) |
| 13 | 65 | VCORE_ISL95812 for QC | 9/25 | Compal | Fint tune IMON | Change PR521 from 90.9k to 100k | X01 (0.3) |
| 14 | 68 | Charger for DSC | 9/28 | TI | Schematic setting for charger IC | Change PR722 from 0 to 4.02k | X01 (0.3) |
| 15 | 69 | Selector | 9/28 | Compal | Can not power on with only slice battery | Add PD819 and DOCK_SMB_ALERT# control signal | X01 (0.3) |
| 16 | 69 | Selector | 9/28 | Compal | Turn on DOCK_PWR_BAR NVDC blocking MOSFET(PQ815) to charge and discharge slice battery | Add PR882 and SLICE_BAT_PRES# control signal to replace SLICE_PREF_EN EC signal | X01 (0.3) |
| 17 | 69 | Selector | 9/28 | Compal | Turn off DOCK_PWR_BAR NVDC blocking MOSFET(PQ815) when AC connect to other NB or DOCK | Add PR886 PR887 and DOCK_DET# control signal to replace SLICE_PREF_EN EC signal | X01 (0.3) |
| 18 | 60 | +DC_IN | 10/8 | Compal | Reserve circuit for droop module battery function | Reserve PQ7 PD7 PR26 PC17 location | X01 (0.3) |
| 19 | 69 | Selector | 10/8 | Compal | Reserve circuit for droop module battery function | Reserve PR888 PR890 PR892 location | X01 (0.3) |



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| Item | Page# | Title | Date | Request Owner | Issue Description | Solution Description | Rev. |
|---|---|---|---|---|---|---|---|
| 20 | 69 | Selector | 10/8 | Compal | Abnormal waveform in PBAT_PRES# when remove battery | Change PD811 and PD804 location | X01 (0.3) |
| 21 | 69 | Selector | 10/8 | Compal | Avoid voltage appearing at the docking connector when either slice battery or E-Dock is not connected to notebook | Add PQ826 | X01 (0.3) |
| 22 | 65 | VCORE_ISL95812 for QC | 10/8 | Compal | Remove the 1.05V_0.8V_PWROK connection by HW request | Delete PR517 | X01 (0.3) |
| 23 | 63 | 1.05VSP | 10/8 | Compal | Remove the 1.5V_RUN_PWRGD connection by HW request | Delete net 1.5V_RUN_PWRGD | X01 (0.3) |
| 24 | 68 | Charger for DSC | 10/11 | Compal | Reserve circuit for system throtlling switching from AC to DC if droop module battery function | Reserve PU704 PC733 PR748 PQ710 PQ708 location | X01 (0.3) |
| 25 | 60 | +DC_IN | 11/20 | Dell | Reserve module battery connector circuit for droop module battery function | De-pop MBATT1 PC2 PR4 PR3 PR5 PL1 PR2 PD1 PC1 PJP1 | X02 (0.4) |
| 26 | 60 | +DC_IN | 11/20 | Dell | Add Main battery control signal circuit for droop module battery function | Pop PQ7 (DMG2301U-7) PD7 (SDMK0340L-7-F) PC17 (1500pF) PR26 (0 ohm) | X02 (0.4) |
| 27 | 60 | +DC_IN | 11/20 | Compal | Reserve +PWR_SRC to +PWR_SRC_S Circuit by HW request | De-pop PQ3 PQ5 PR21 PC15 PR24 PR19 PR17 PC6 PC7 | X02 (0.4) |
| 28 | 60 | +DC_IN | 11/20 | Compal | Change EMI solution by EMI request | Delete PL6 PD6 and add PJP4 | X02 (0.4) |
| 29 | 68 | Charger for DSC | 11/20 | Dell | Add circuit for CPU freq to LFM mode when heavy loading plug out AC, because this function is built in module battery function controller IC - CD3302, droop module battery will not use CD3302 controller. | Pop PU704 (74AHC1G08GW) PC733 (0.1uF) PQ710 (DMN65D8LW-7) PR748 (100K) | X02 (0.4) |
| 30 | 68 | Charger for DSC | 11/20 | Compal | Use one dual N package part to replace two NPN Mosfet | Change PQ707 PQ708 from DMN65D8LW-7 to DMN66D0LDW-7 (PQ707A PQ707B) | X02 (0.4) |
| 31 | 69 | Selector | 11/20 | Dell | Reserve module battery circuit about trigger PROCHOT# when active battery is removed from system. | De-pop PU802 PC802 PU803 PC804 Pop PR888 (0 ohm) | X02 (0.4) |
| 32 | 69 | Selector | 11/20 | Dell | Reserve controller - CD3302 solution for droop module battery circuit | De-pop PU808 PR834 PR837 PR842 PR848 PR851 PR853 PR856 PC814 PR861 PR865 PR867 PR871 PR873 PR876 PR836 PR841 PR845 PR852 PQ910 PR880 PR878 PR879 | X02 (0.4) |
| 33 | 69 | Selector | 11/20 | Dell | Reserve mdoule battery charging and discharging path circuit | De-pop PQ808 PD803 PR800 PR803 PR805 PD804 PD805 PQ803 PD801 PQ804 PR809 PC800 PR806 PD802 PD809 | X02 (0.4) |
| 34 | 69 | Selector | 11/20 | Dell | Change battery control signal for droop module battery function | De-pop PD812 PR889 PR891 Pop PR890 (0 ohm) PR892 (0 ohm) | X02 (0.4) |
| 35 | 69 | Selector | 11/20 | Compal | Change Main source for EOL issue. | Change PQ801 PQ814 PQ822 PQ823 from FDN338P_G to NTR4502PT1G | X02 (0.4) |

# Version Change List ( P. I. R. List )



| Item | Page# | Title | Date | Request Owner | Issue Description | Solution Description | Rev. |
|---|---|---|---|---|---|---|---|
| 36 | 69 | Selector | 11/20 | Compal | Use one dual diode package part to replace two discrete diode part | Change PD810 PD814 PD813 PD816 PD815 PD817 from SDMK0340L-7-F to BAT54CW (PD814 PD816 PD817) | X02 (0.4) |
| 37 | 70 | PROCESSOR DECOUPLING | 11/20 | Compal | Move GPU Core output MLCC cap to power side by HW request | Change CV172 CV174 CV175 CV183 location to PCV172 PCV174 PCV175 PCV183 | X02 (0.4) |
| 38 | 68 | Charger for DSC | 11/20 | Compal | Change bootstrap resistor size | Change PR715 size from 0402 to 0603 | X02 (0.4) |
| 39 | 69 | Selector | 11/20 | Compal | Use one package part to replace dual n package part | Change PQ802 from DMN66D0LDW-7 to DMN65D8LW-7 | X02 (0.4) |
| 40 | 65 | VCORE_ISL95812 for QC | 12/25 | Compal | VCCIO_OUT 6KHz noise issue. Request by H.W. | Add PC548 (1uF) | X02 (0.4) |
| 41 | 65 | VCORE_ISL95812 for QC | 12/25 | INTERSIL | Fine tune Iout accuracy | Change PR535 from 511 Ohm to 470 Ohm.<br>Change PR521 from 100kOhm to 100kOhm.<br>Change PC500 from 0.01uF to 1000pF.<br>Change PC539,PC540,PC544 from 0.22uF to 0.022uF.<br>Change PR510,PR538,PR553 from 10kOhm to 100kOhm.<br>Add PR558 (4.3M Ohm) | X02 (0.4) |
| 42 | 68 | Charger for DSC | 12/25 | TI | For Input current sense stabilize | Change PC703 from 0.1uF to 1uF | X02 (0.4) |
| 43 | 68 | Charger for DSC | 12/25 | TI | Change cell pin pull high reference voltage from +3.3V_ALW to BQ24715_REGN | Depop PR720 and pop PR746 | X02 (0.4) |
| 44 | 60 | +DC_IN | 12/25 | Compal | GPIO net - AC_DIS# is high active. Corrent net name. | Change PQ6A pin.5 net name from AC_DIS# to AC_DIS. | X02 (0.4) |
| 45 | 69 | Selector | 12/25 | Compal | GPIO net - AC_DIS# is high active. Corrent net name. | Change PR828 pin1 net name from AC_DIS# to AC_DIS. | X02 (0.4) |
| 46 | 68 | Charger for DSC | 1/7 | Compal | Reserve input cap location for input voltage overshoot issue. This issue fix in PG1.3 | Reserve PC734 PC735 | X02 (0.4) |
| 47 | 68 | Charger for DSC | 1/7 | Compal | IAC peaks with VCORE EMI bead (PL504). reaches 8 A, triggers PROCHOT | Reserve PC736 PC737 PC738 | X02 (0.4) |
| 48 | 68 | Charger for DSC | 1/7 | DELL | AC+ E5 Battery will not active H_PROCHOT funtion | Add PR749 and EC signal | X02 (0.4) |
| 49 | 60 | +DC_IN | 2/6 | Compal | Change PD2 material by ESD team request. | Change PD2 material and add PD4. | X02 (0.5) |
| 50 | 69 | Selector | 2/6 | Compal | To avoid +DOCK_PWR_BAR leakage voltage when system only with main battery | Add PD821 PQ820 PR896 PR897 PQ830 PC818 PU809 | X02 (0.5) |