IV@ For UMA
EV@ For Pure Dis.
SP@ For special setting
SPI@ For Optimus & UMA special setting
SPE@ For Pure Dis.special setting
VA@ For Audio version A setting
VB@ For Audio version B setting
@3G For 3G setting
PIV@ For UMA Power
PEV@ For Pure Dis. Power

FH5 BLOCK DIAGRAM

01

GPU CORE PWR RT8204 P45	CHARGER ISL88731 P53
GPU IO PWR UP6111AQDD P46	3/5V SYS PWR RT8206 P52
Discharger/+3V_M P54	CPU CORE PWR ISL95831 P43~P44
+1.8V UP61111AQDD P51	CPU +1.05V_VTT UP61111AQDD P47
CPU iGPU_CORE RT8204 P45	PCH +1.05V UP61111AQDD P49
+0.85V ISL62871 P48	DDR3 PWR RT8207A P50

Fan Driver (PWM Type) P42

ALS (SM/BUS)

intel <MCH Processor>
SandyBridge 0.61
rPGA 988 (37.5mm X 37.5mm)
DDR SYSTEM MEMORY
FDI DMI P4~P7

DDR III
SO-DIMM 0
SO-DIMM 1
P14, 15

Dual Channel 1066/1333 MHz

PCIE X16 5GT/s

X'TAL 27.0MHz

nVIDIA GPU
N12P Fermi
Package GB2-128
Optimus (Muxless) P16~P22

FDI interface 2.7GT/s

X4 DMI interface 5GT/s

CRT R-SW P24 → CRT P24
LVDS Switchable P24 → LVDS P24
HDMI R-SW P24 → HDMI P24

INT_CRT
INT_LVDS
INT_HDMI

HDD (SATA) P25 — SATA0
ODD (SATA) P25 — SATA3

intel <PCH>
FDI DMI
SATA Gen3
SATA Gen2
iGFX Interfaces
RTC P9
X'TAL 32.768KHz
USB
CougarPoint 0.7
HDA
PCI-E
mBGA 989 (25mm X 25mm)
P8~P13
SPI LPC
X'TAL 25MHz

USB8 PCIE4 → NewCard USB8 P33

PCI-Express Gen2 5GT/s

USB CNNs USB0,1,2 P27
Bluetooth USB9 P27
CCD USB6 P24
CardReader RTS5138 USB5 P23
— USB 2.0

Azalia

PCIE6 → Realtek RTL8111E-GR P26 — X'TAL 25MHz
Transformer P26
RJ45 P26

PCIE1 → Mini Card WiFi USB3 P28 — USB3
PCIE2 → Mini Card 3G USB4 P28 — USB4
SIM Card Conn DB P28

Audio CODEC
RTL ALC269VB P30
HP Jack P30
MIC Jack P30
SPK P30
DMIC P24

Dual SPI ROM 4MB x1 (Basic ME+Braidwood) P9

WPCE791/FLASH
PECI3.0 P31
SPI ROM P31
Touch Pad P29
Keyboard P29
Light Sensor P33
Button on mechanical key P31

Note:
HM65 does not support USB 6 & 7
HM65 does not support SATA 2 & 3

Quanta Computer Inc.
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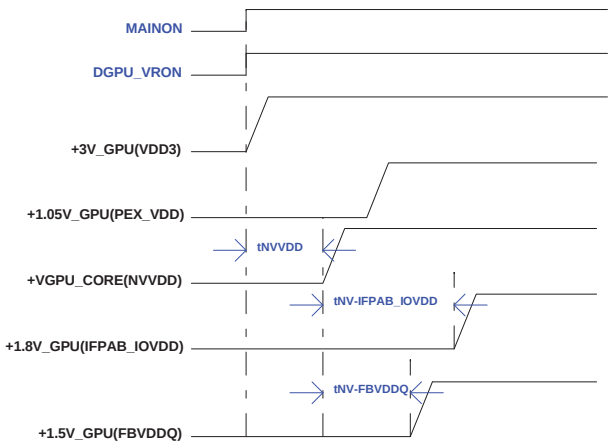
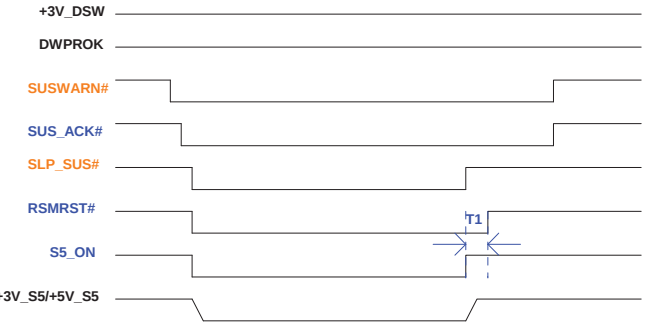
N12P-GE Power Up Sequence



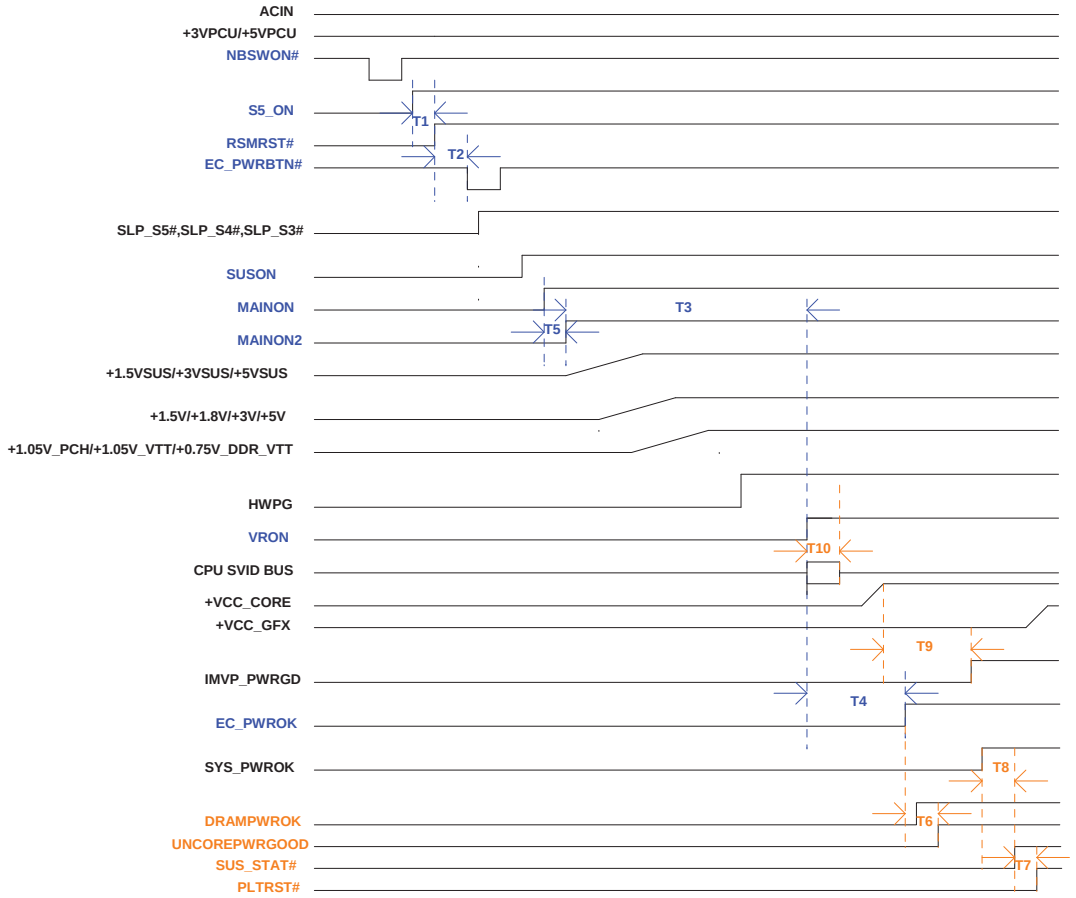
N12P-GE Power up Sequence
tNVVDD>0
tNV-IFPAB_IOVDD>0
tNV-FBVDDQ>0

Deep S4/S5 off-on Sequence



Deep S4/S5 Sequence
T1: S5_ON TO RSMRST# = 30ms (spec:mini 10ms)

MS15-UMA Power-ON Sequence



System Power Sequence
T1: S5_ON TO RSMRST# = 30ms (spec:mini 10ms)
T2: RSMRST# TO EC_PWRBTN# = 110ms (spec:mini 100ms)
T3: MAINON2 TO VRON = 110ms (spec:mini 99ms)
T4: VRON TO EC_PWROK = 10ms (HWPG NEED TO BE HIGH at that time)
T5: MAINON to MAINON2 =500us
T6: EC_PWROK to UNCOREPWRGOOD =2ms(Min)
T7: SUS_STAT# to PLTRST# =60us(Min)
T8: SYS_PWROK to SUS_STAT# =1ms(Min)
T9: +VCC_CORE to IMVP_PWRGD =5ms(Max)
T10: VRON to accept SVID command. =5ms(Max)

Quanta Computer Inc.
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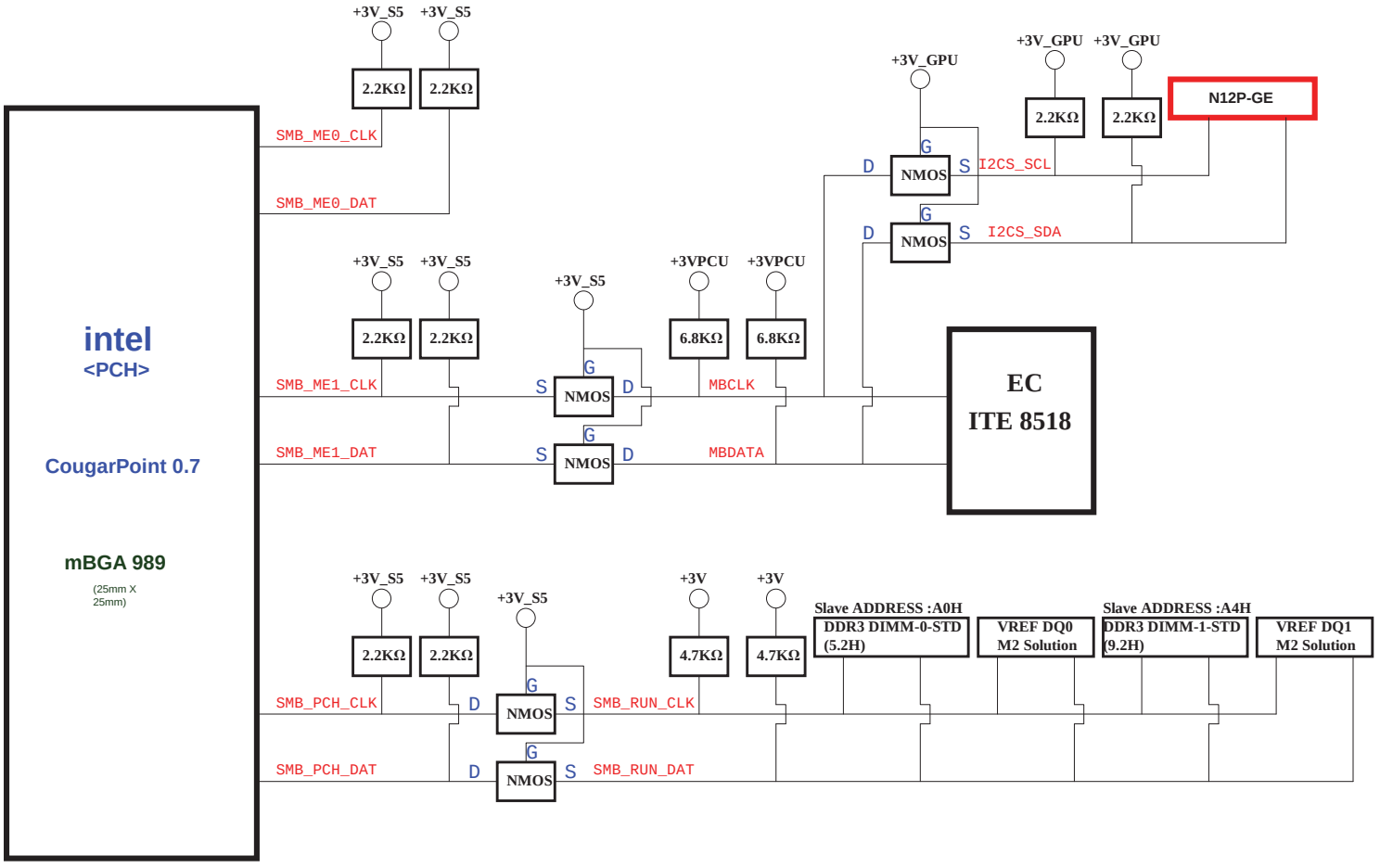
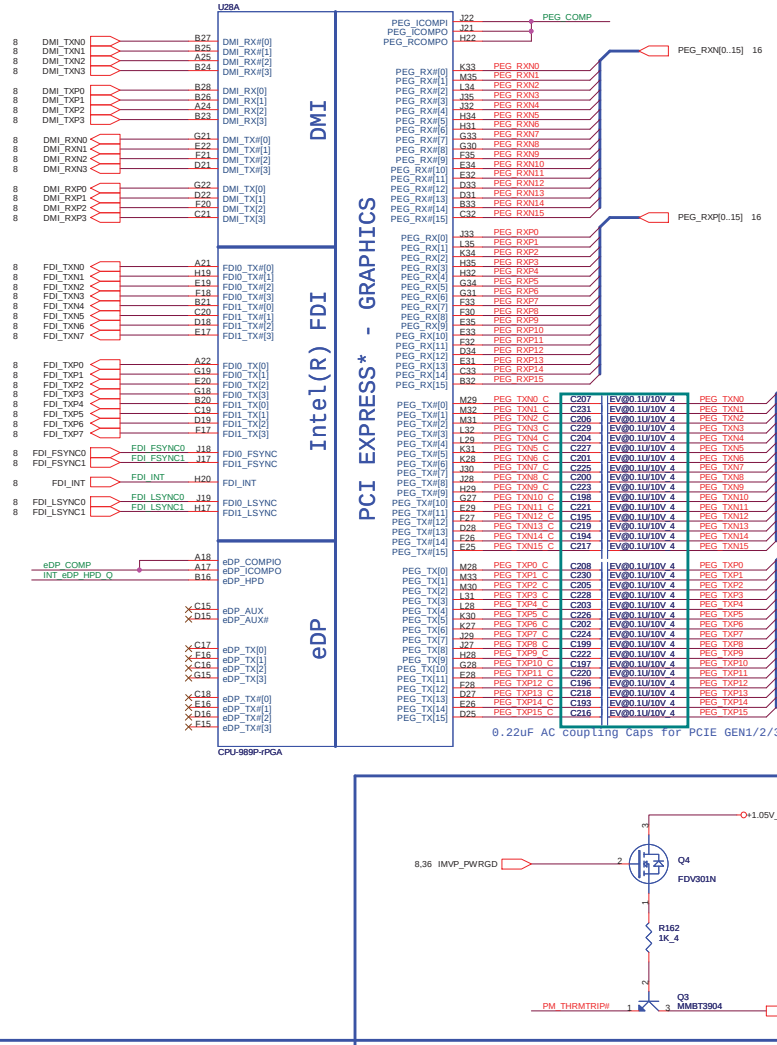


Quanta Computer Inc.
PROJECT : FH5

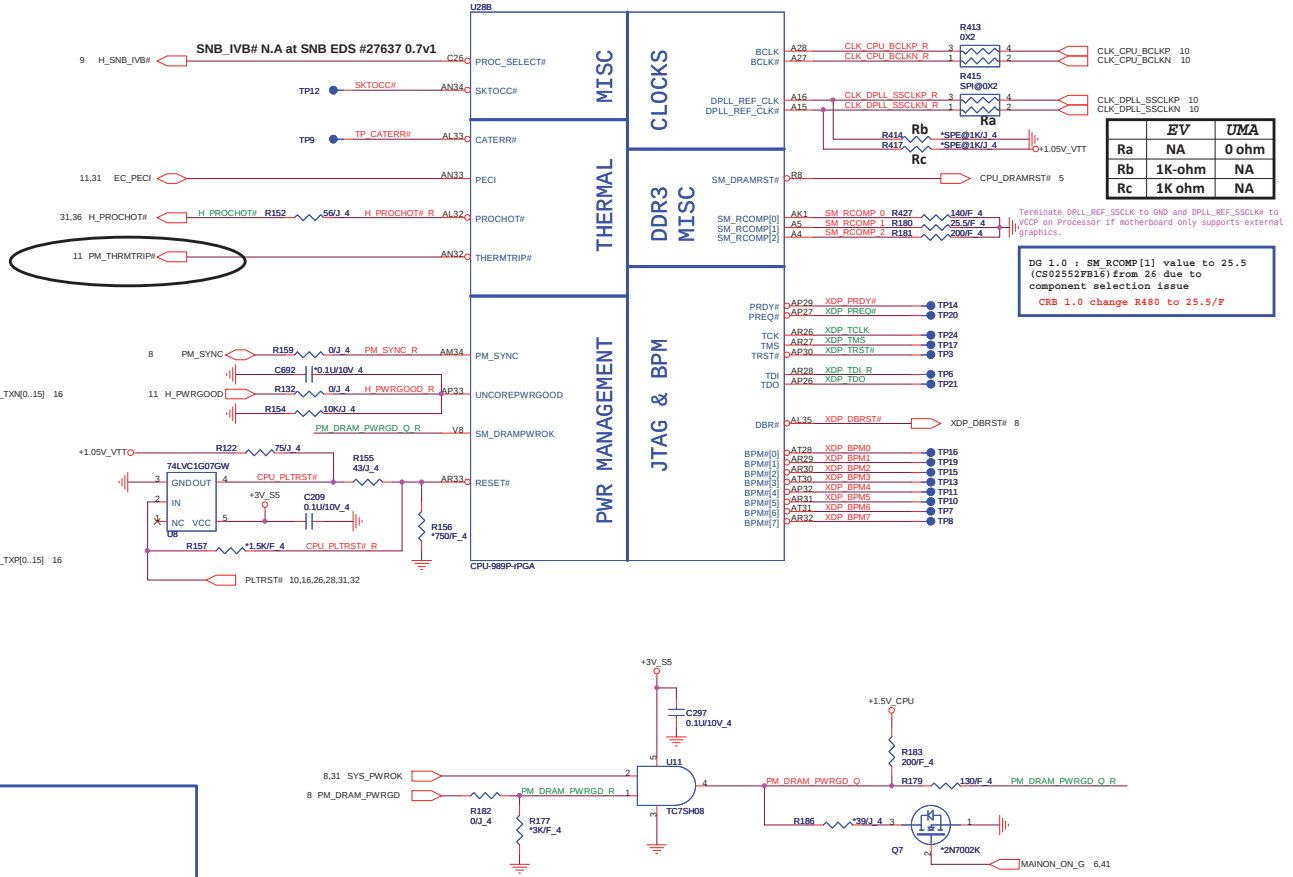
Size	Document Number	Rev
	SMBus Address	1A

Date: Monday, September 27, 2010 Sheet 3 of 41

Sandy Bridge Processor (DMI,PEG,FDI)

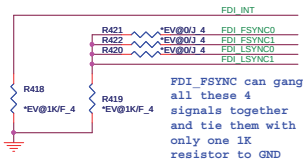


Sandy Bridge Processor (CLK,MISC,JTAG)



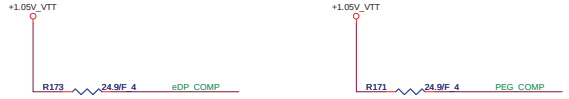
	EV	UMA
Ra	NA	0 ohm
Rb	1K-ohm	NA
Rc	1K ohm	NA

FDI Disabling (Discrete Only)



FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (DG V0.5 Ch2.2.9).

DP & PEG Compensation



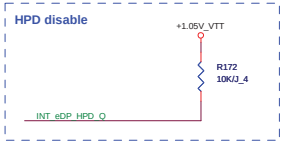
eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms

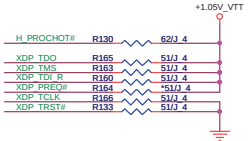
PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

eDP Hot-plug

CAD Note: Place PU resistor within 2 inches of CPU



Processor pull-up(CPU)



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Size | Document Number: Sandy Bridge 1/4 | Rev: 1A
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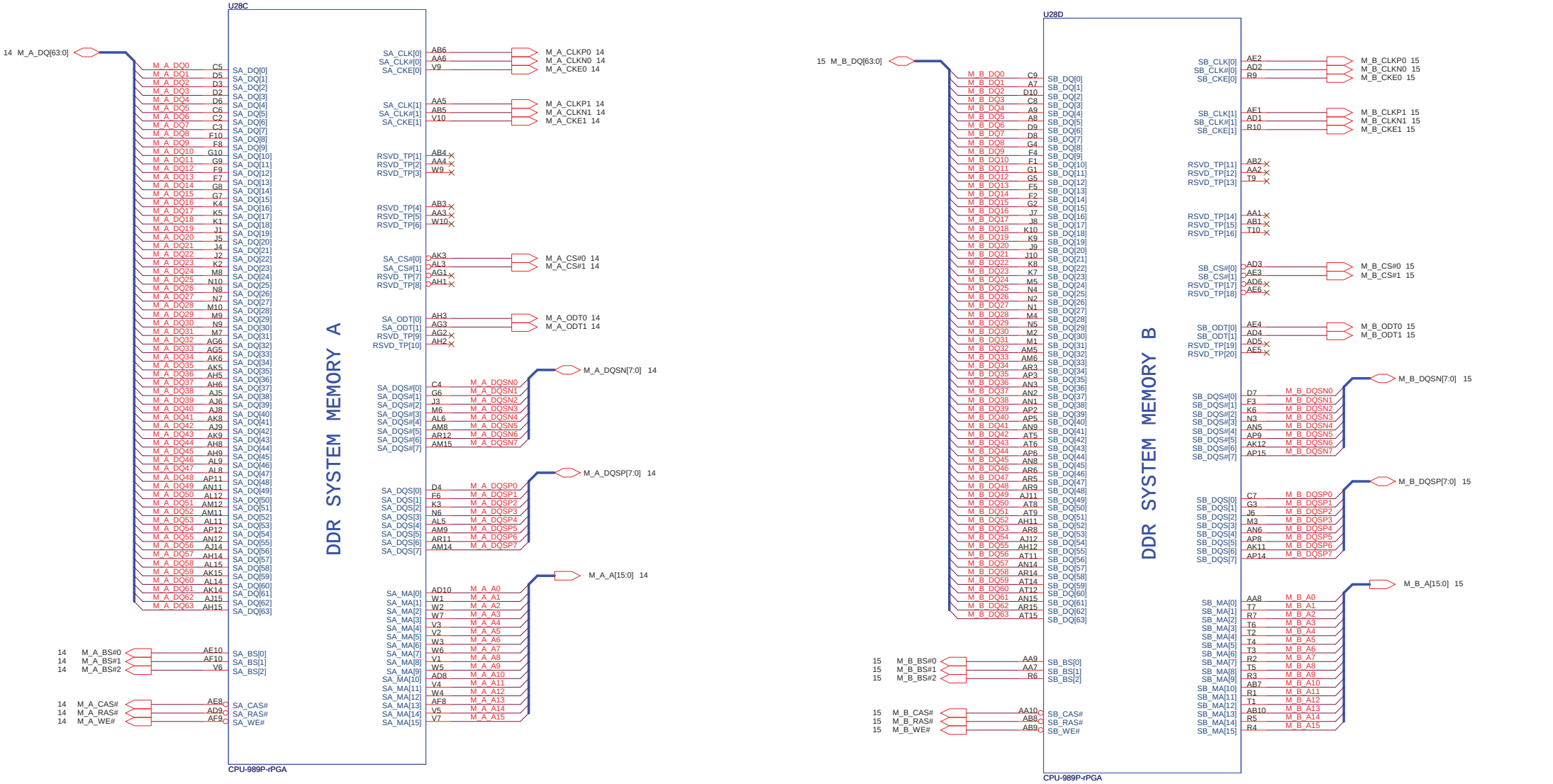
Sandy Bridge Processor (DDR3)



Quanta Computer Inc.			
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	Sandy Bridge 2/4		1A
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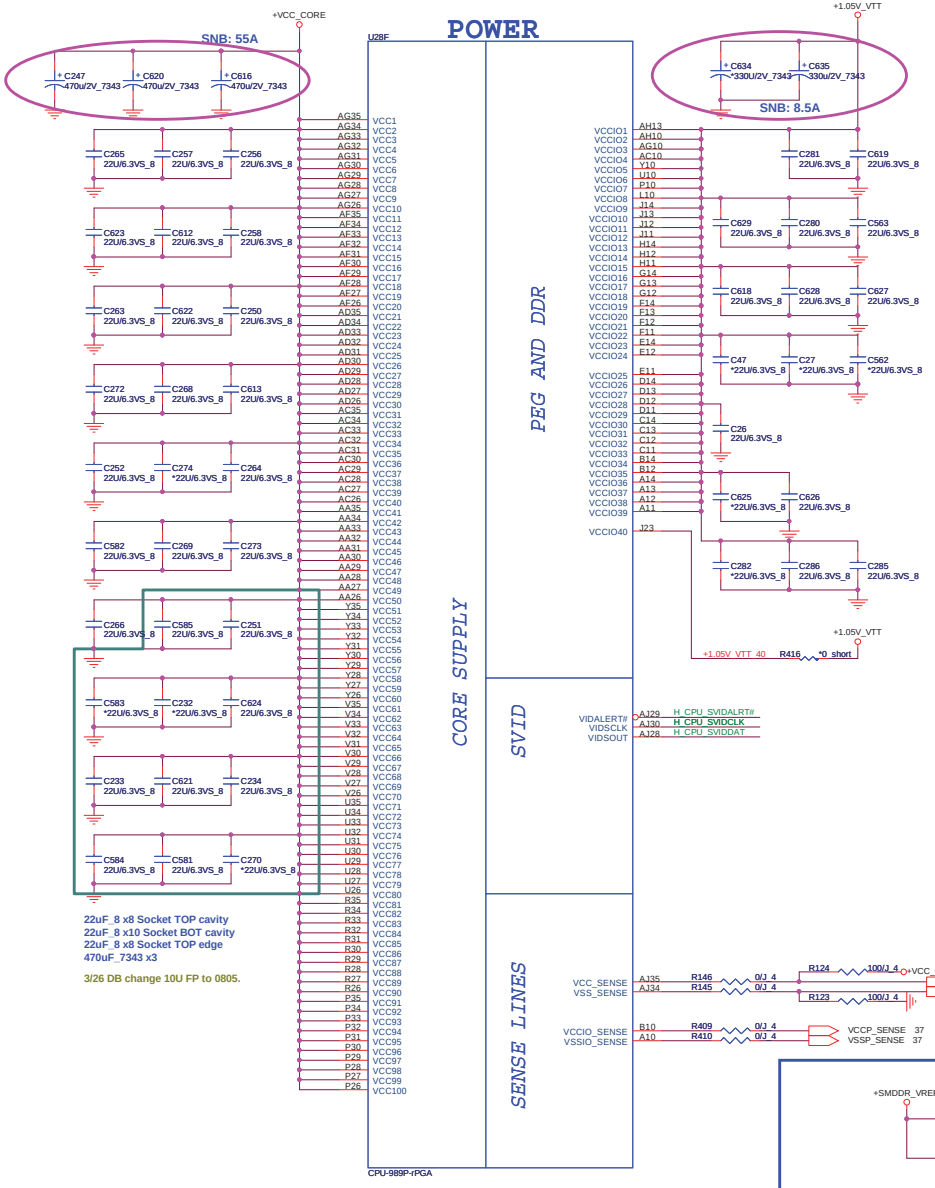
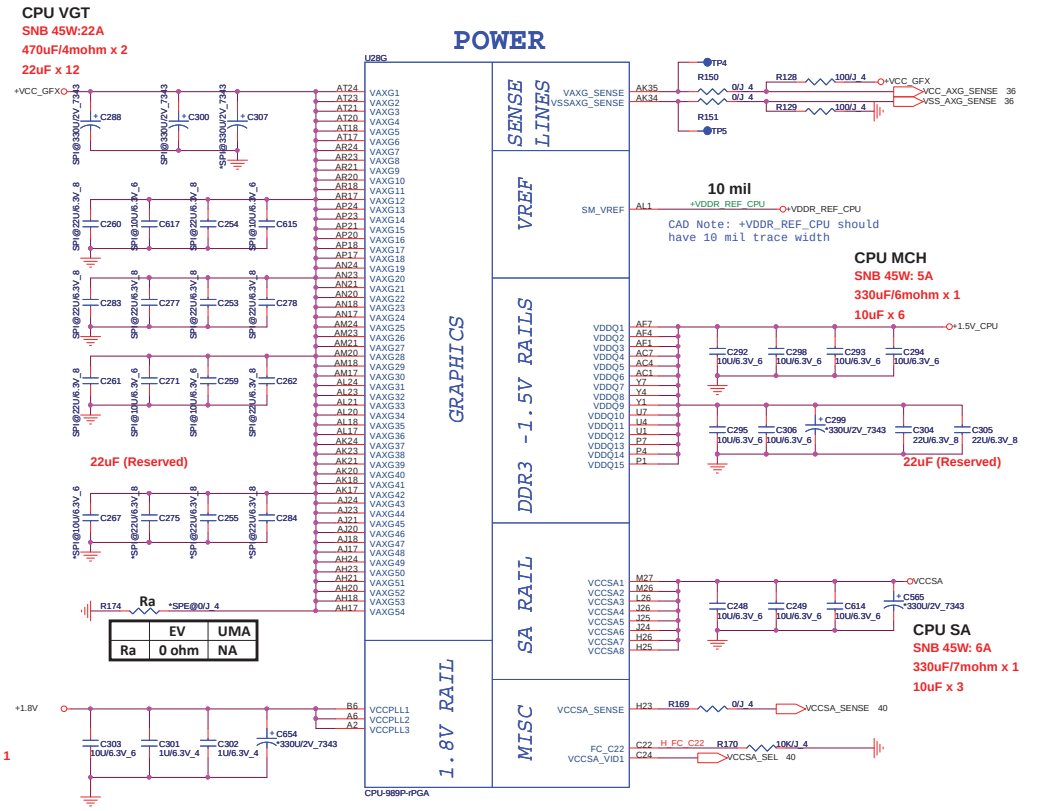
22uF_8 x7 Socket TOP cavity
22uF_8 x5 Socket BOT cavity
22uF_8 x2 Socket TOP cavity (no stuff)
22uF_8 x5 Socket BOT cavity (no stuff)
330uF_7343 x2

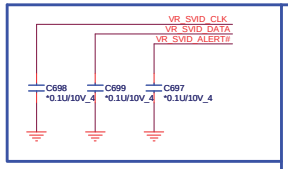
SPI@ For Optimus & UMA
SPE@ For Pure Dis.
SP@ For special setting

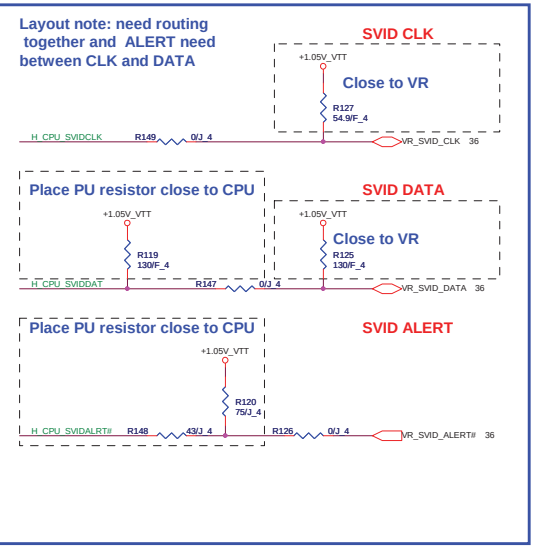
Sandy Bridge Processor (POWER)

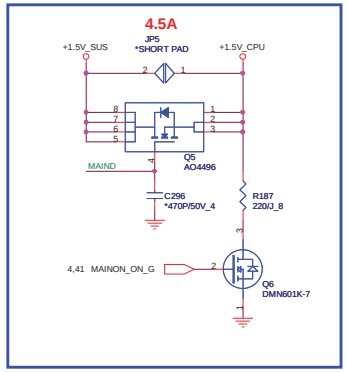


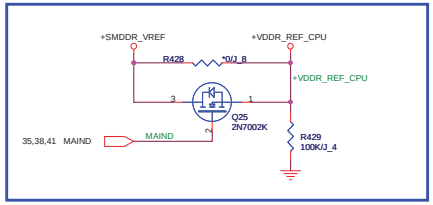
Sandy Bridge Processor (GRAPHIC POWER)











	EV	UMA
Ra	0 ohm	NA

Quanta Computer Inc.	
PROJECT : FH5	
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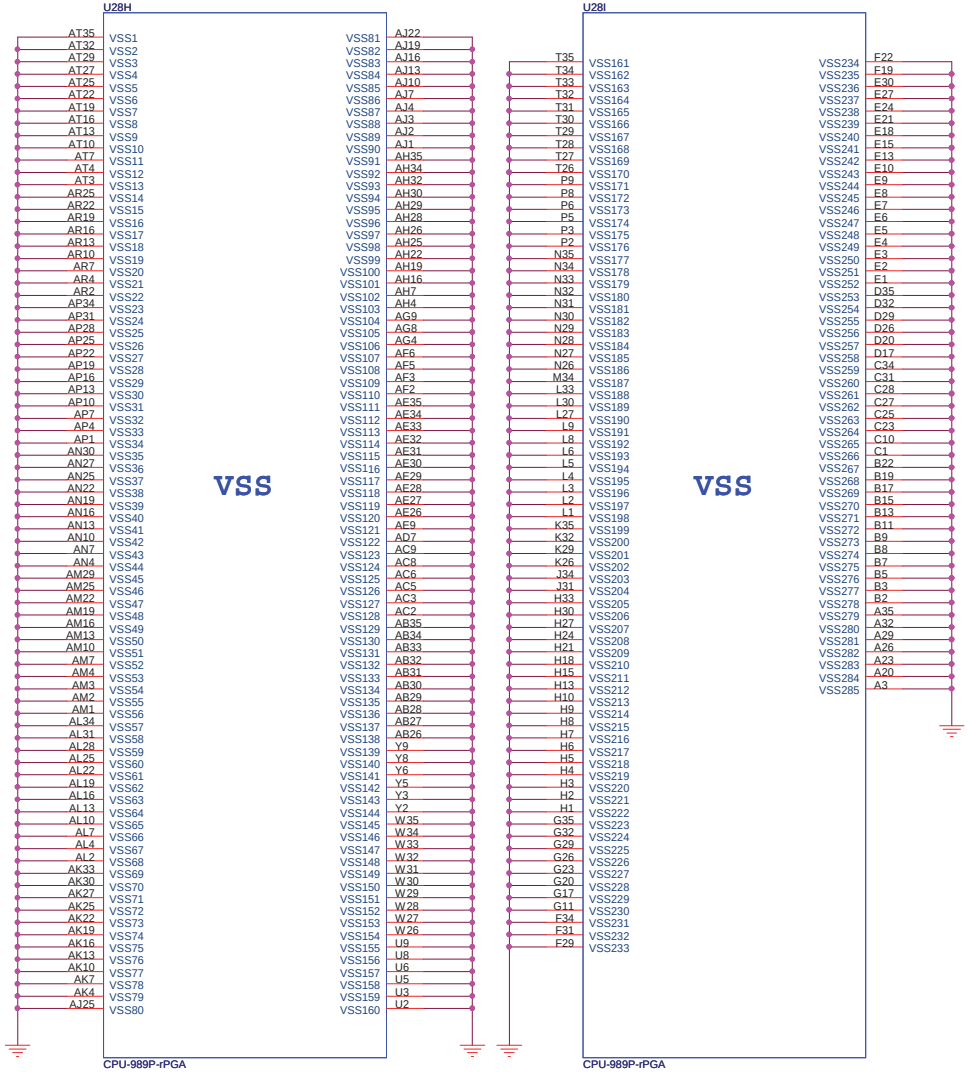
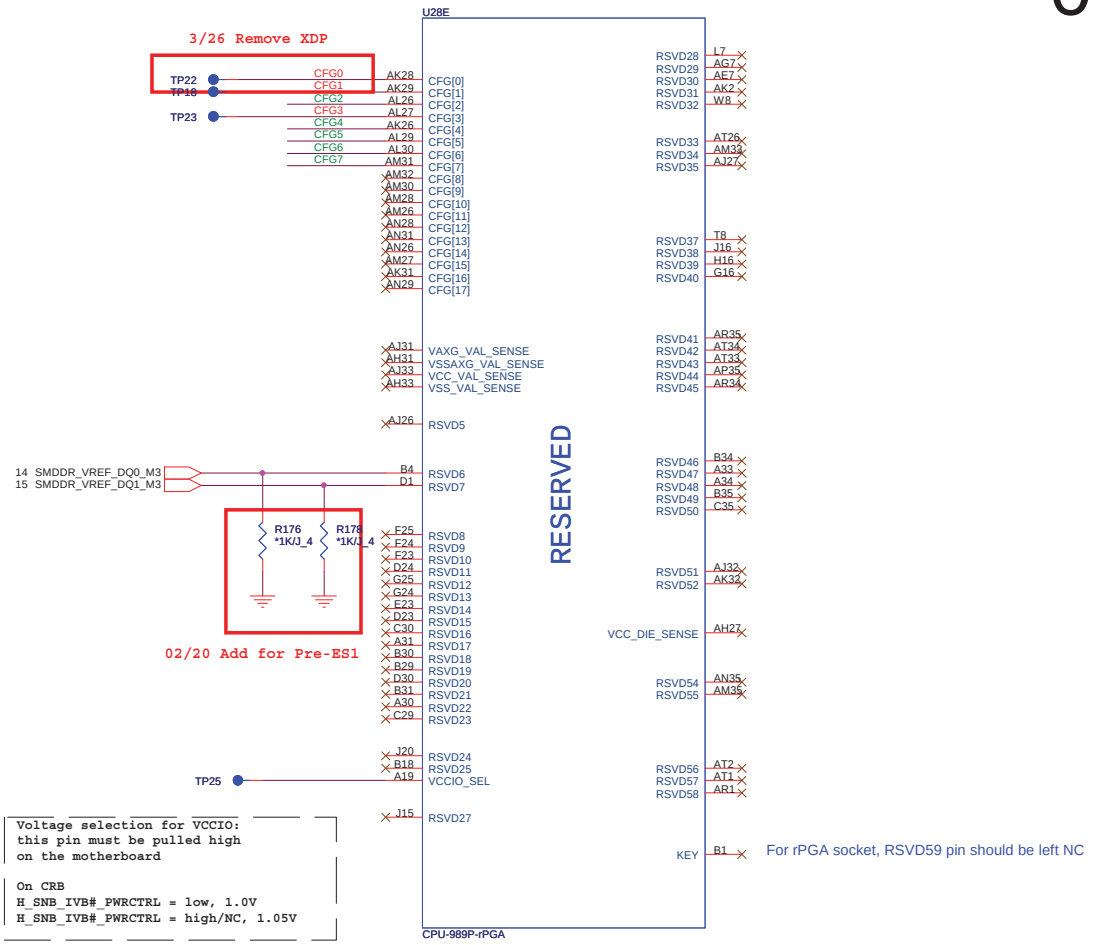
Sandy Bridge Processor (GND)



Sandy Bridge Processor (RESERVED, CFG)



For rPGA socket, RSVD59 pin should be left NC

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG3 PEG Static x4 Lane	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Quanta Computer Inc.
PROJECT : FH5

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	Sandy Bridge 4/4	1A
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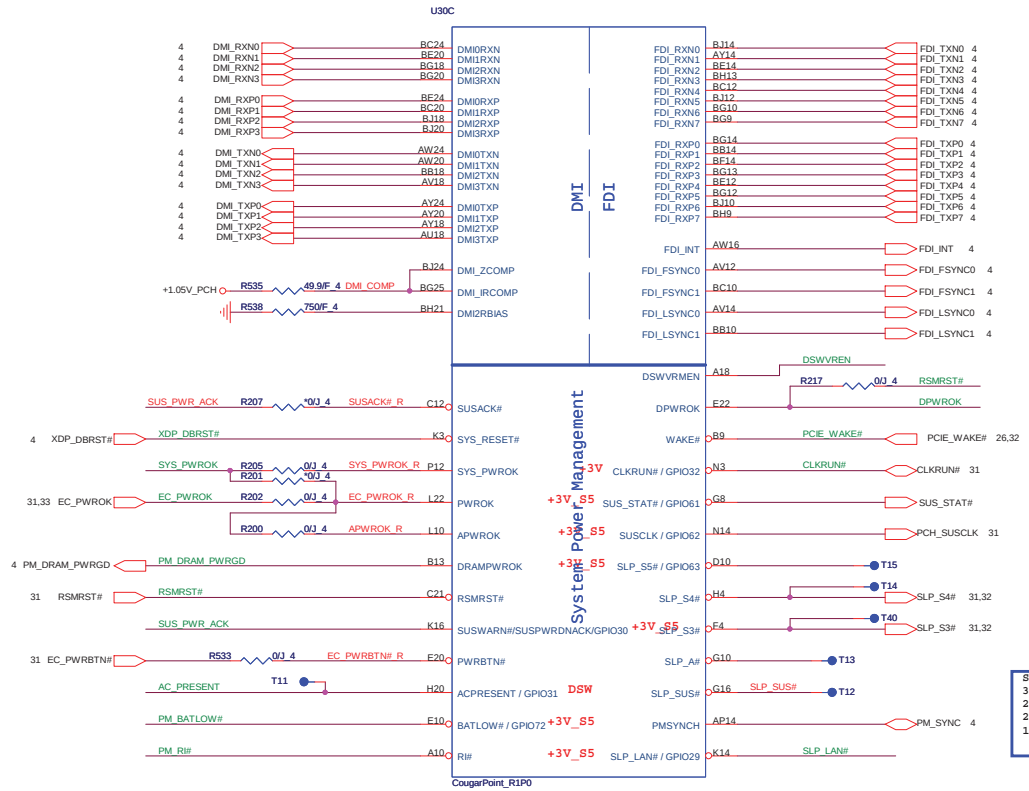
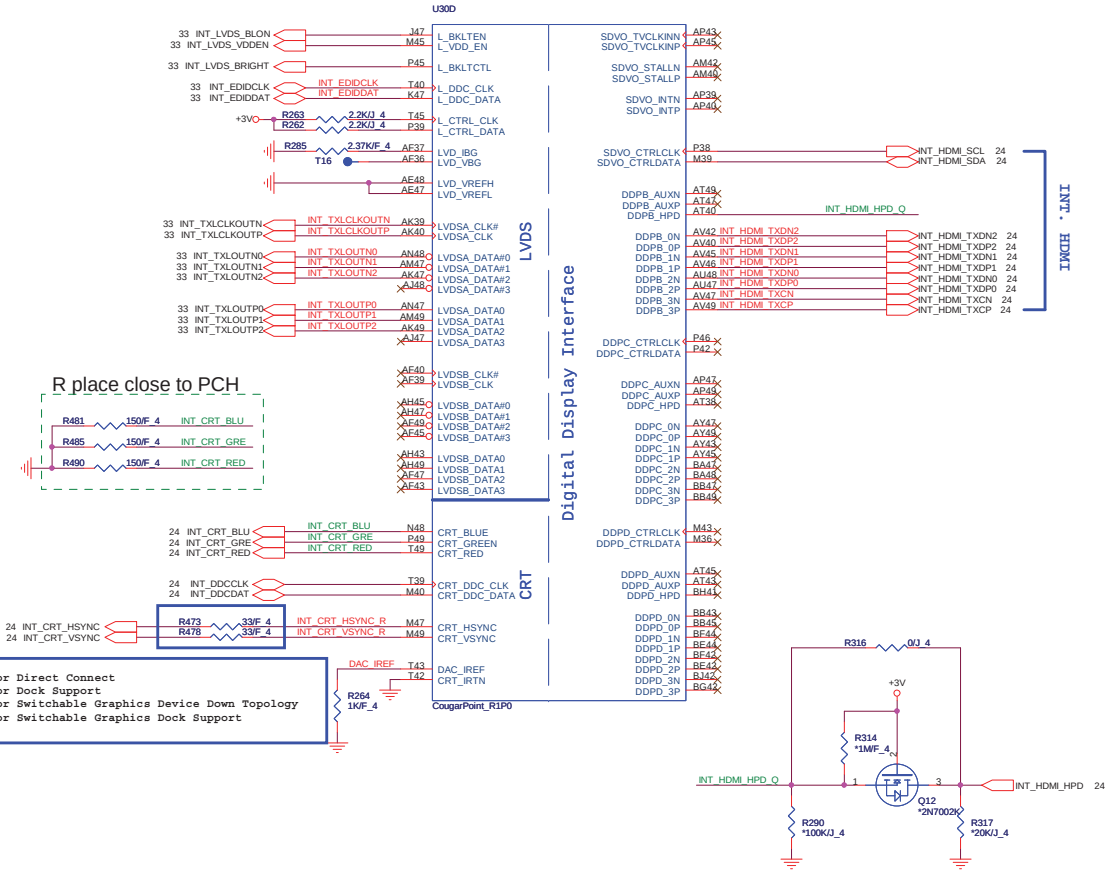
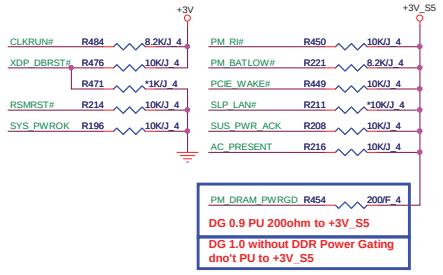
Cougar Point (DMI,FDI,PM)



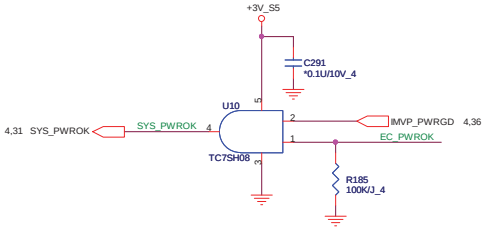
Cougar Point (LVDS,DDI)

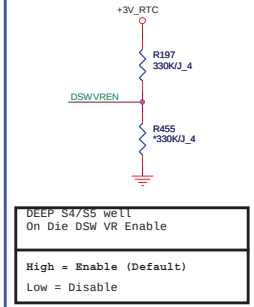


PCH Pull-high/low(CLG)

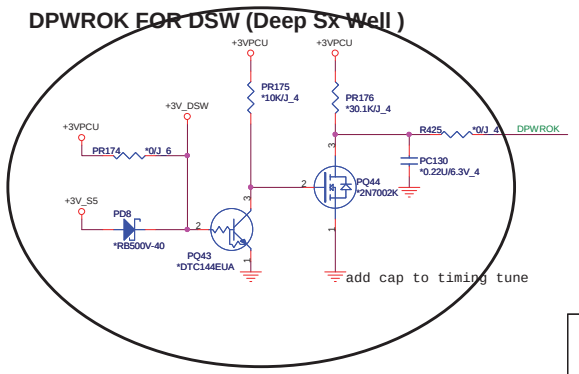


System PWR_OK(CLG)





DPWROK FOR DSW (Deep Sx Well)



Quanta Computer Inc.
PROJECT : FH5

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	Cougar Point 1/6	1A
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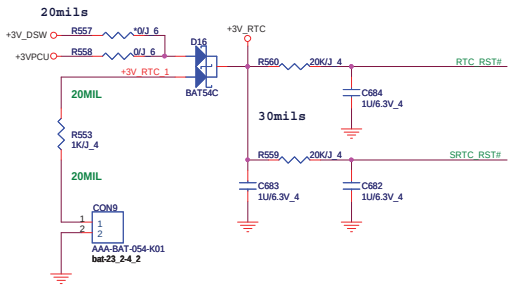
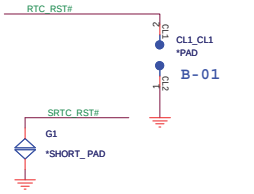
RTC Circuitry(RTC)

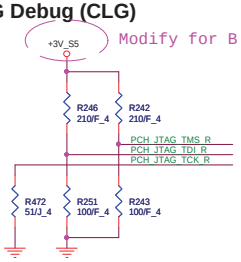


RESET JUMP (Near ROOM DOOR)

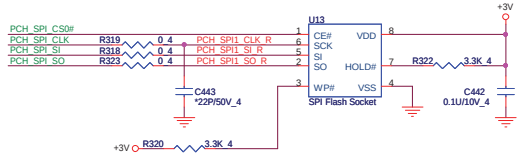


HDA Bus(CLG)

PCH JTAG Debug (CLG)



PCH SPI ROM(CLG)

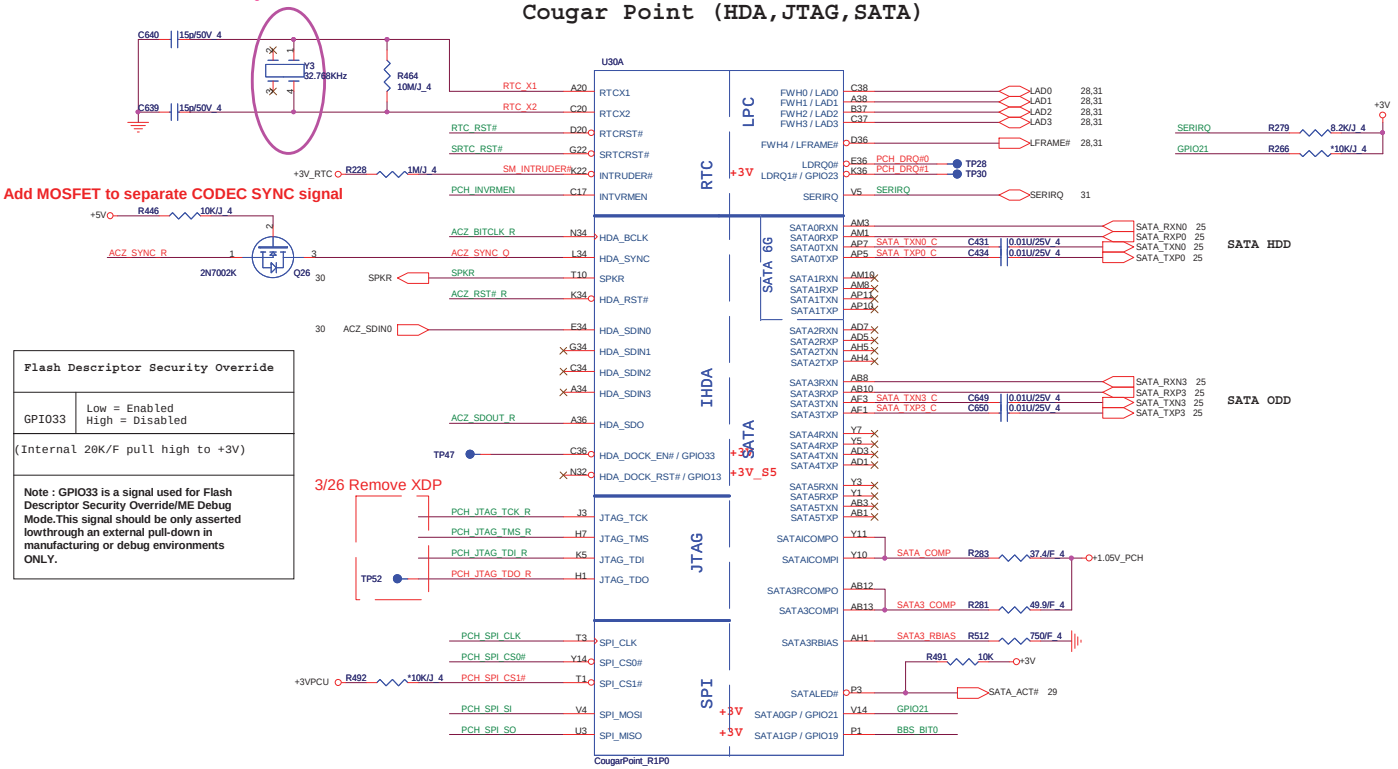


Vender	Size	P/N
EON	4MB	AKE39FN0Q00 (EN25F32-100HIP)
Winbond	4MB	AKE391P0N00 (W25Q32BVSSIG)
Socket		DG008000031

PCH2 (CLG)

Change SIZE 8/24

Cougar Point (HDA,JTAG,SATA)

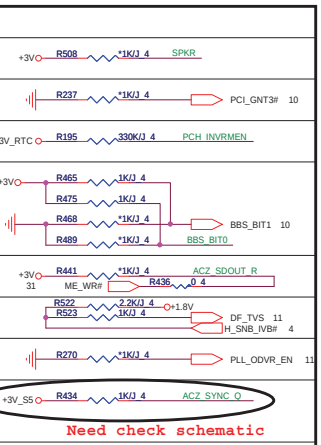


Flash Descriptor Security Override	
GPIO33	Low = Enabled High = Disabled
(Internal 20K/F pull high to +3V)	

Note : GPIO33 is a signal used for Flash Descriptor Security Override/ME Debug Mode.This signal should be only asserted lowthrough an external pull-down in manufacturing or debug environments ONLY.

PCH Strap Table

Pin Name	Strap description	Sampled	Configuration
SPKR	No reboot mode setting internal PD	PWROK	**0 = Default (weak pull-down 20K)** 1 = Setting to No-Reboot mode
GNT3# / GPIO55	Top-Block Swap Override internal PU	PWROK	0 = "top-block swap" mode **1 = Default (weak pull-up 20K)**
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1] internal PU	PWROK	GNT1# / GNT0# / Boot Location 1 / 1 / SPI * 0 / 0 / LPC
GPIO19	Boot BIOS Selection 0 [bit-0] internal PU	PWROK	
HDA_SDO	Flash Descriptor Security internal PD	RSMRST	**0 = Default (weak pull-up 20K)** 1 = Override
DF_TVS	DMI/FDI Termination voltage internal PD	PWROK	**0 = Set to Vss** **1 = Set to Vcc (weak pull-up 20K)**
GPIO28	On-die PLL Voltage Regulator internal PU	RSMRST#	0 = Disable **1 = Enable (Default)**
HDA_SYNC	On-Die PLL VR Voltage Select internal PD	RSMRST	**0 = Support by 1.8V (weak pull-down)** **1 = Support by 1.5V**
GPIO15	Intel ME Crypto Transport Layer Security (TLS) cipher suite internal PD	RSMRST	0 = Intel ME TLS with no confidentiality 1 = Intel ME TLS with confidentiality



Default weak pull-up on GNT0/1#
[Need external pull-down for LPC BIOS]

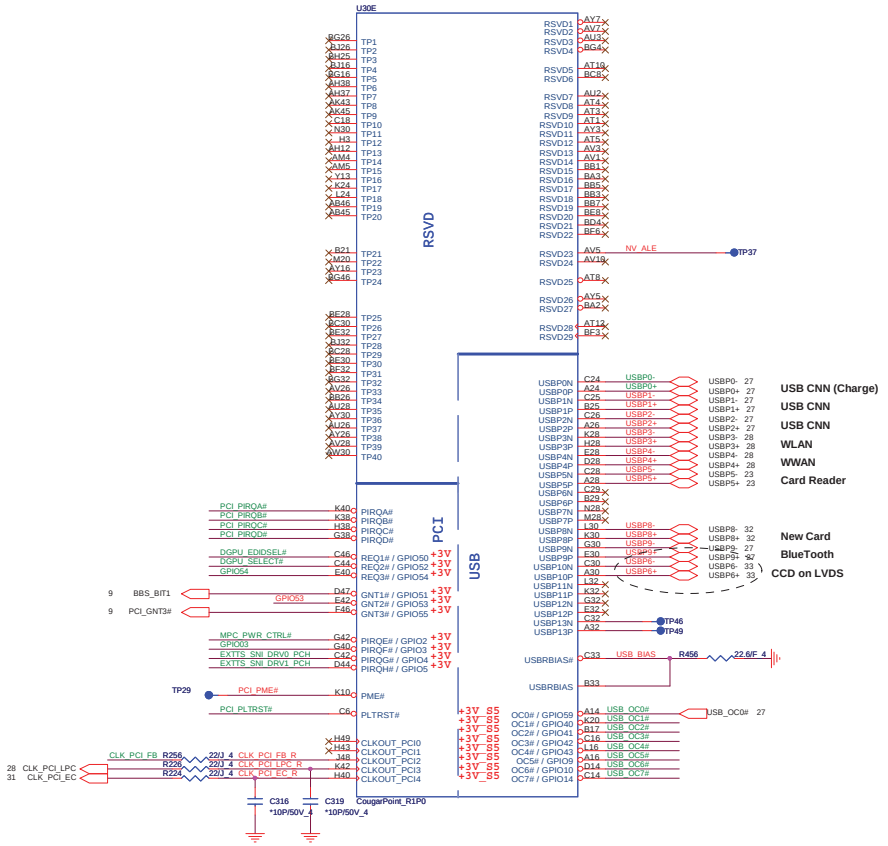
GNT[3:0]# functionality is not available on Mobile. Used as GPIO only.

Default weak pull-up on GNT0/1#
[Need external pull-down for LPC BIOS]

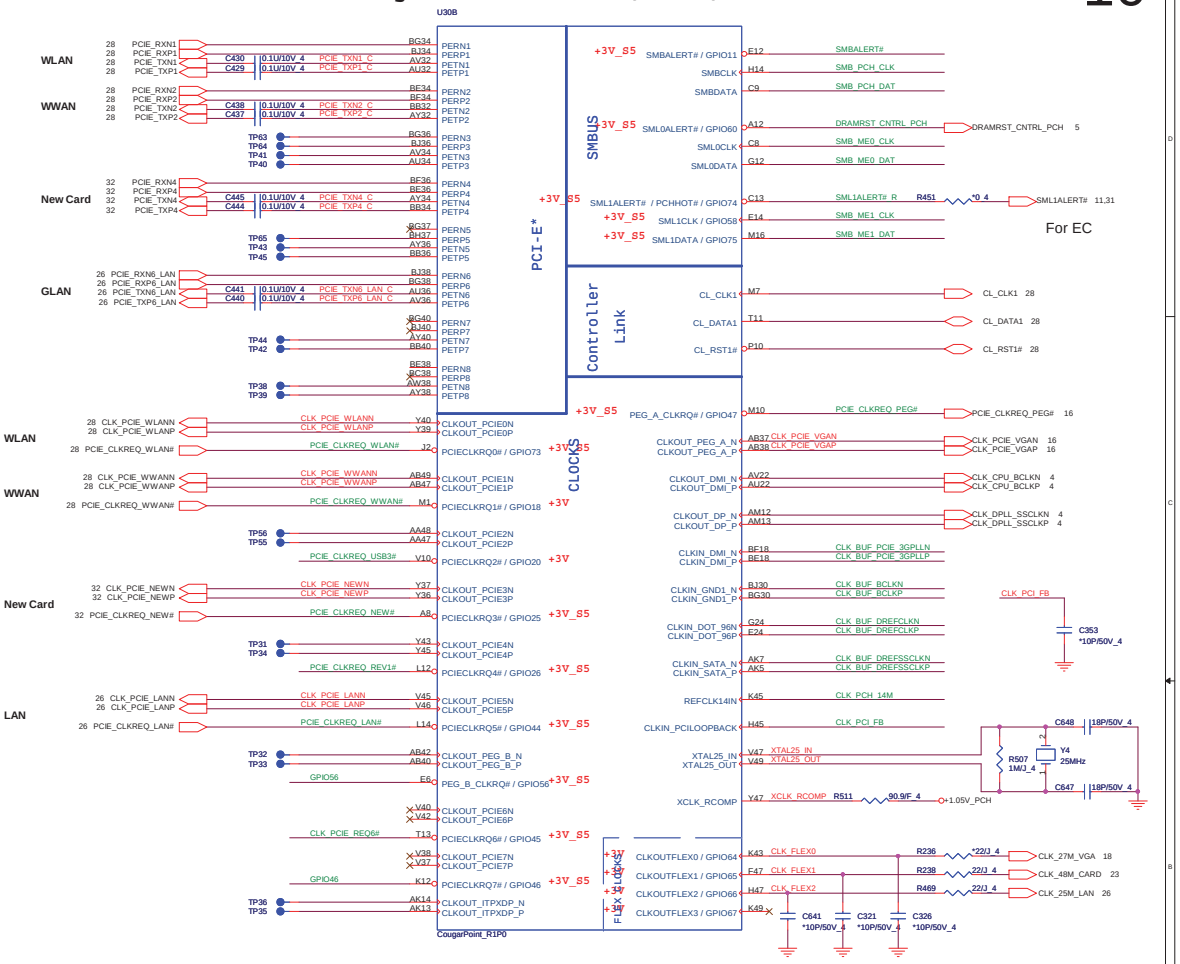
R8361 change to 1K ohm follow DG1.0 and chklist 1.0 It needs to be connected to PROC_SELECT with a 1K±5% pull-up resistor to PCH VCCPNAND rail and a 4.7K±5% series resistor.

New Add in CPT EDS Rev1.0 at 0316 , Needs to be pulled High for Huron River platform.

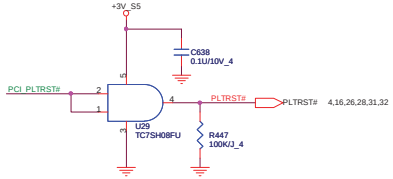
Cougar Point-M (PCI,USB,NVRAM)



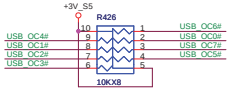
Cougar Point-M (PCI-E,SMBUS,CLK)

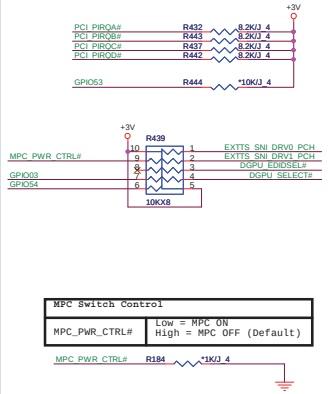


PLTRST#(CLG)

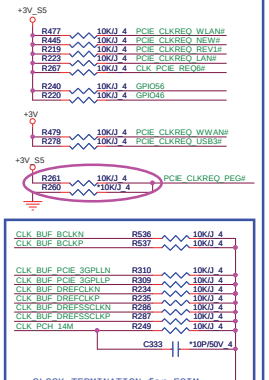


PCI/USBOC# Pull-up(CLG)

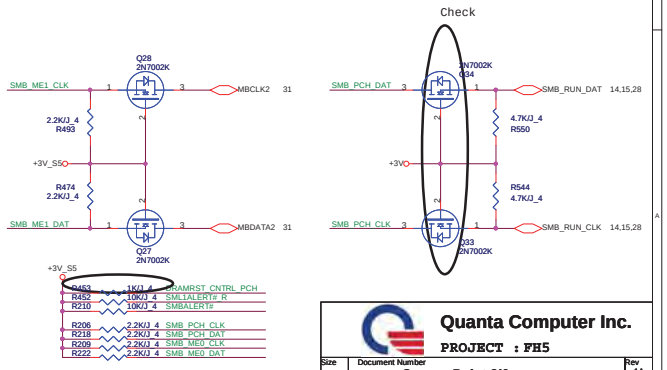




CLK_REQ/Strap Pin(CLG)



SMBus/Pull-up(CLG)



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Cougar Point (GPIO,VSS_NCTF,RSVD)

SGPIO

S_GPIO — R509 1K/J_4 — R510 *1K/J_4 — +3V

GPIO15

Intel ME Crypto Transport Layer Security (TLS) cipher suite internal PD

0 = Intel ME TLS with no confidentiality

1 = Intel ME TLS with confidentiality

U30F

	S_GPIO	T7	BMBUSY# / GPIO0 +3V	+3V	TACH4 / GPIO68 C40 BOARD_ID2
31 EC_EXT_SMI#	EC_EXT_SMI#	A42	TACH1 / GPIO1 +3V	+3V	TACH5 / GPIO69 B41 R461 1.5K/F_4
	BOARD_ID1	H36	TACH2 / GPIO6 +3V	+3V	TACH6 / GPIO70 C41 R462 1.5K/F_4 +3V
31 EC_EXT_SCI#	EC_EXT_SCI#	E38	TACH3 / GPIO7 +3V	+3V	TACH7 / GPIO71 A40 R460 1.5K/F_4
TP48	ICC_EN#	C10	GPIO8 +3V_S5		
TP27	LAN_DISABLE#	C4	LAN_PHY_PWR_CTRL / GPIO12	+3V_S5	
9 PCH_GPIO15		G2	GPIO15 +3V_S5		A20GATE P4 EC_A20GATE — EC_A20GATE 31
16 DGPU_HOLD_RST#		U2	SATA4GP / GPIO16 +3V		PECI AU16 R294 *0_4 — EC_PECI 4,31
16,31 GFXPG	GFXPG	D40	TACH0 / GPIO17 +3V		RCIN# P5 EC_RCIN# — EC_RCIN# 31
	BIOS_REC	T5	SCLOCK / GPIO22 +3V		PROCPWRGD AY11 — H_PWRGOOD 4
31 BIOS_WP#	+3V_S5 R239 1K/F_4	E8	GPIO24 / MEM_LED +3V_S5		THRMTRIP# AY10 PCH_THRMTRIP# R292 390/J_4 — PM_THRMTRIP# 4
	GPIO27	E16	GPIO27 DSW		INIT3_3V# T14
9 PLL_ODVR_EN		P8	GPIO28 +3V_S5		DF_TVS AY1 — DF_TVS 9
	STP_PCI#	K1	STP_PCI# / GPIO34 +3V		TS_VSS1 AH8
GPUCORE_ON	31,39,41 dGPU_VRON	K4	GPIO35 +3V		TS_VSS2 AK11
GPU_PWR_ON	41 dGPU_PWR_EN — dGPU_PWR_EN R274 EV@0_4 DMI_OVRVLTG	V8	SATA2GP / GPIO36 +3V		TS_VSS3 AH10
	dGPU_PRSNT# R501 EV@0_4 FDI_OVRVLTG	M5	SATA3GP / GPIO37 +3V		TS_VSS4 AK10
	MFG_MODE	N2	SLOAD / GPIO38 +3V		NC_1 P37
	BOARD_ID0	M3	SDATAOUT0 / GPIO39 +3V		
	TEST_SET_UP	V13	SDATAOUT1 / GPIO48 +3V		VSS_NCTF_15 BG2
10,31 SML1ALERT#	R498 0_4 CRIT_TEMP_REP#	V3	SATA5GP / GPIO49 +3V		VSS_NCTF_16 BG48
	SV_DET	D6	GPIO57 +3V_S5		VSS_NCTF_17 BH3
					VSS_NCTF_18 BH47
		A4	VSS_NCTF_1		VSS_NCTF_19 BJ4
		A44	VSS_NCTF_2		VSS_NCTF_20 BJ44
		A45	VSS_NCTF_3		VSS_NCTF_21 BJ45
		A46	VSS_NCTF_4		VSS_NCTF_22 BJ46
		A5	VSS_NCTF_5		VSS_NCTF_23 BJ5
		A6	VSS_NCTF_6		VSS_NCTF_24 BJ6
		B3	VSS_NCTF_7		VSS_NCTF_25 C2
		B47	VSS_NCTF_8		VSS_NCTF_26 C48
		BD1	VSS_NCTF_9		VSS_NCTF_27 D1
		BD49	VSS_NCTF_10		VSS_NCTF_28 D49
		BE1	VSS_NCTF_11		VSS_NCTF_29 E1
		BE49	VSS_NCTF_12		VSS_NCTF_30 E49
		BF1	VSS_NCTF_13		VSS_NCTF_31 F1
		BF49	VSS_NCTF_14		VSS_NCTF_32 F49

GPIO — CPU/MISC — NCTF

CougarPoint_R1P0

Muxed with STP_PCI#
If not used, 8.2-kΩ to 10-kΩ pull-up to +V3.3S.

Un-multiplexed. Can be configured as wake input to allow wakes from Deep Sleep.
If not used then use 8.2-kΩ to 10-kΩ pull-down to GND.

GPIO Pull-up/Pull-down(CLG)

+3V_S5
- LAN_DISABLE# R229 10K/J_4
- PLL_ODVR_EN R496 10K/J_4
- ICC_EN# R448 *10K/J_4

+3V
- EC_EXT_SMI# R463 10K/J_4
- EC_EXT_SCI# R433 10K/J_4
- STP_PCI# R480 10K/J_4
- EC_A20GATE R259 10K/J_4
- EC_RCIN# R258 10K/J_4
- GFXPG R431 *10K/J_4
- CRIT_TEMP_REP# R497 10K/J_4
- dGPU_PWR_EN R280 10K/J_4

GPIO27 — R225 10K/J_4

SATA[3:2]GP/GPIO[37:36] internal Pull-down 20K
SATA2GP/GPIO36 (FDI_OVRVLTG) & SATA3GP/GPIO37 (DMI_OVRVLTG)
Sampled at Rising edge of PWROK.
Weak internal pull-down. (weak internal pull-down is disabled after PLTRST# de-asserts)
NOTE: This signal should NOT be pulled high when strap is sampled

R506 *100K/J_4 FDI_OVRVLTG R500 *1K/J_4 +3V

FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage

DMI_OVRVLTG R282 *200K/F_4 +3V

DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

BIOS_REC R272 10K/J_4 R271 *1K/J_4 +3V

BIOS RECOVERY	High = Disable (Default) Low = Enable

SV_SET_UP
High = Strong (Default)

TEST_SET_UP — R430 10K/J_4 R435 *1K/J_4 +3V

MFG-TEST

MFG_MODE — R482 10K/J_4 R488 *1K/J_4 +3V

+3V_S5 — R231 *10K/J_4 — SV_DET — R233 100K/J_4

[ID0:D1]	0:0	0:1	1:0	1:1
Fuction	UMA	Optimus (Hynix)	Optimus (Samsung)	Rev.
Board ID2	reserve	PD		

+3V
- R250 *SP@10K/J_4 BOARD_ID0 R245 SP@10K/J_4
- R190 SP@10K/J_4 BOARD_ID1 R189 *SP@10K/J_4
- R458 SP@10K/J_4 BOARD_ID2 R459 *SP@10K/J_4

	EV	UMA
Stuff	Ra	Rb

+3V — R504 SPE@10K/J_4 — DGPU_PRSNT# — R505 *SPI@100K/J_4

Ra Rb

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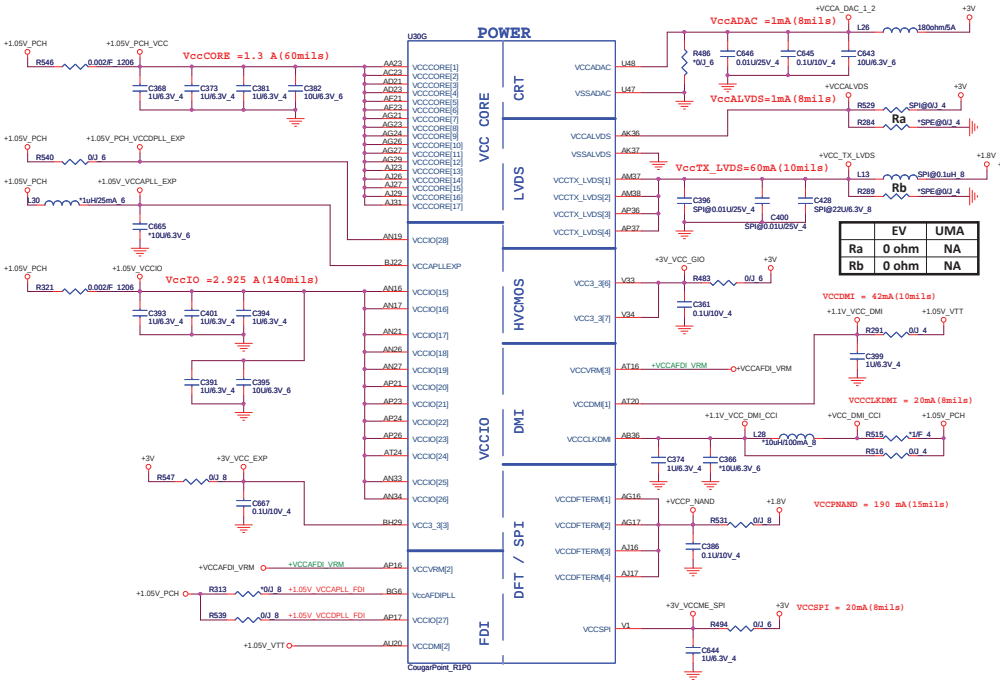
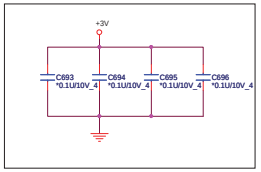
PCH5(CLG)

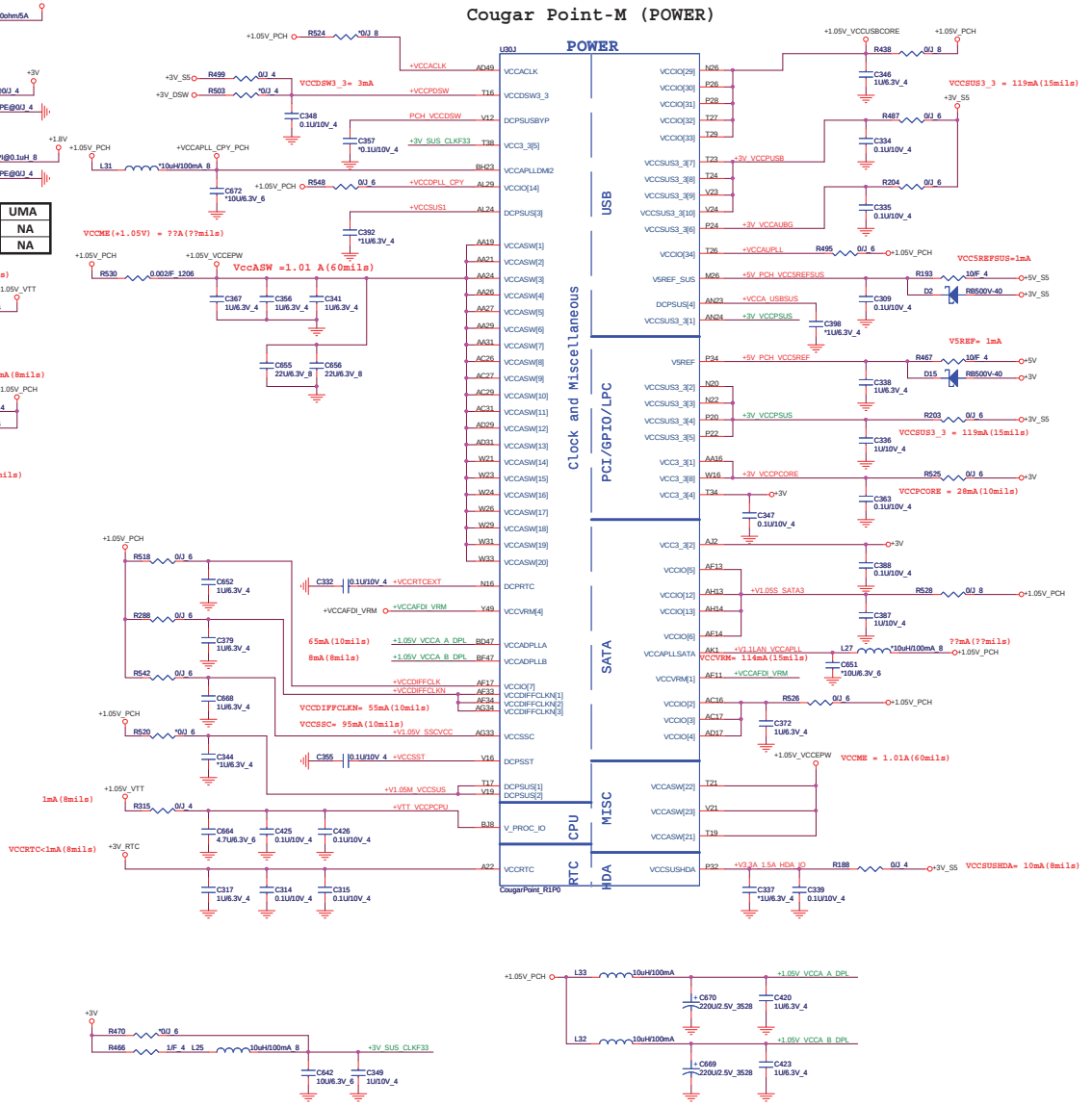
COUGAR POINT (POWER)



	EV	UMA
Ra	0 ohm	NA
Rb	0 ohm	NA



Cougar Point-M (POWER)



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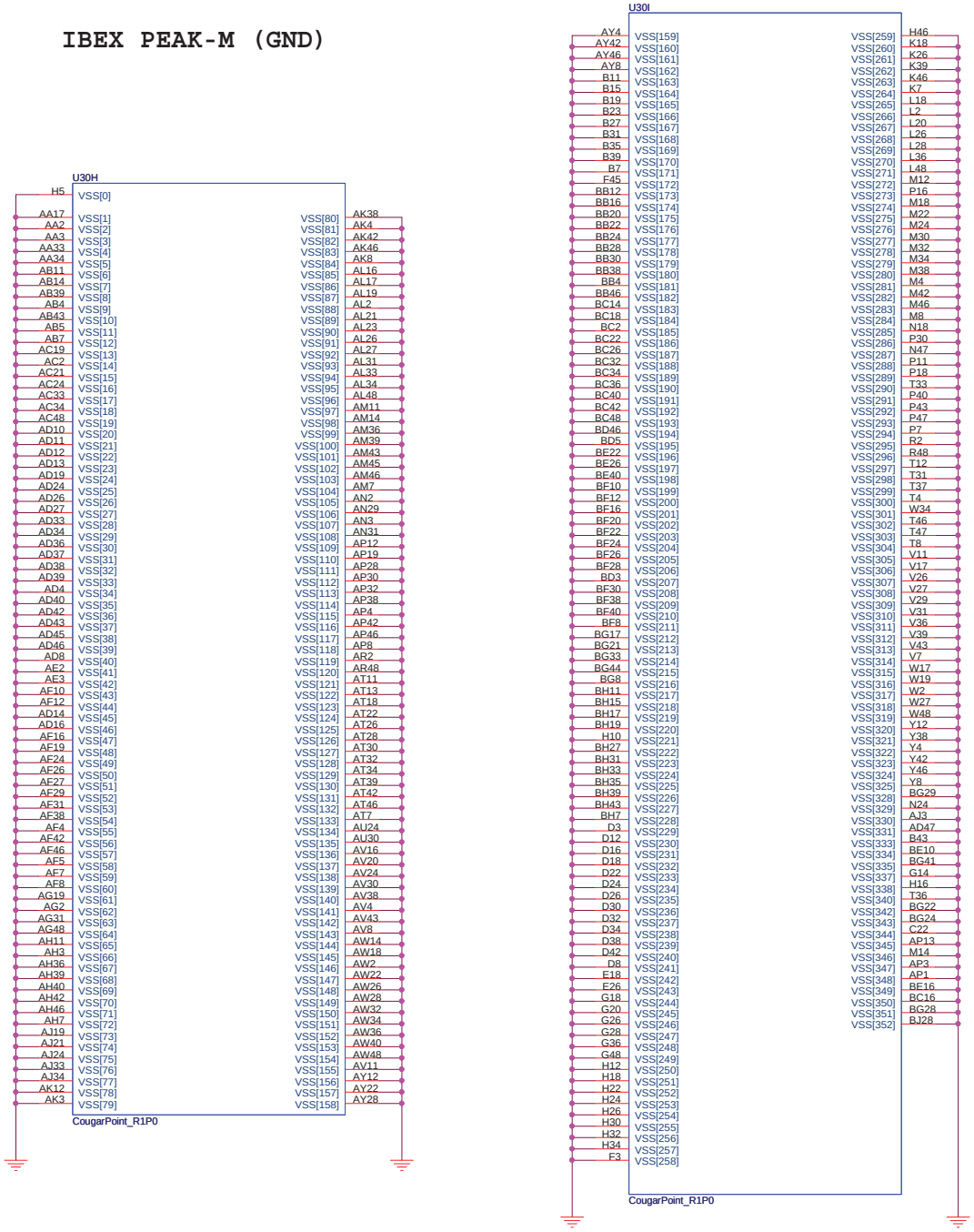
IBEX PEAK-M (GND)



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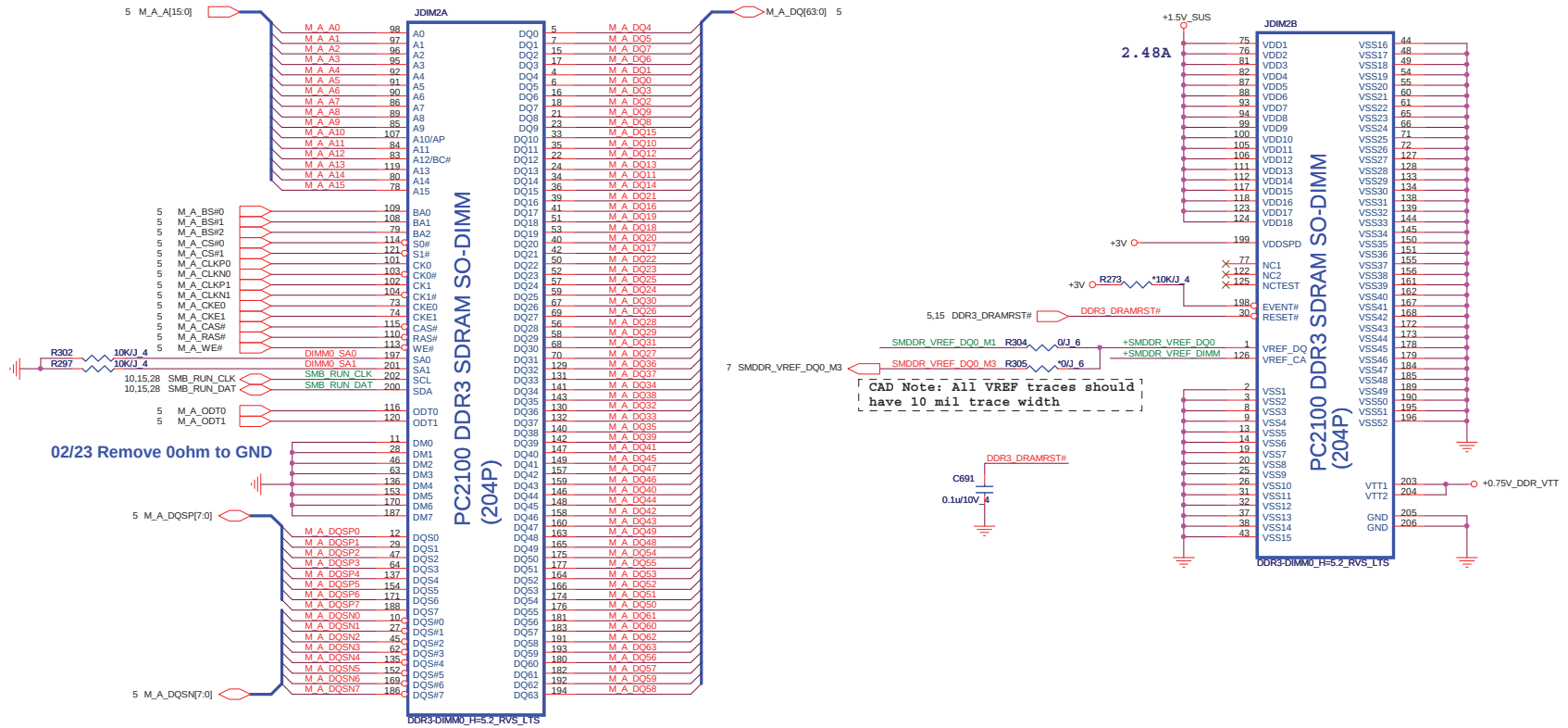
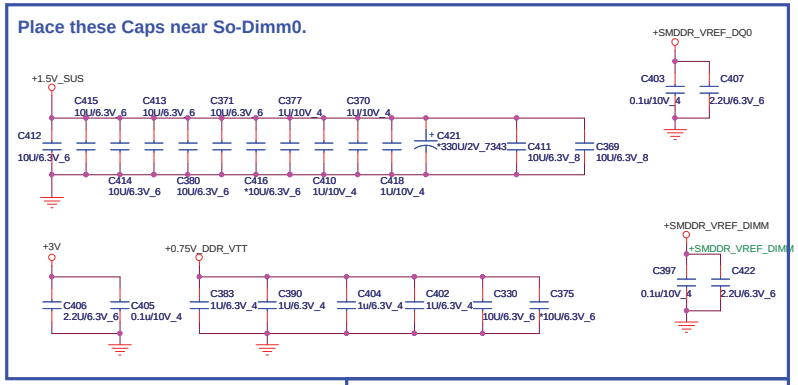
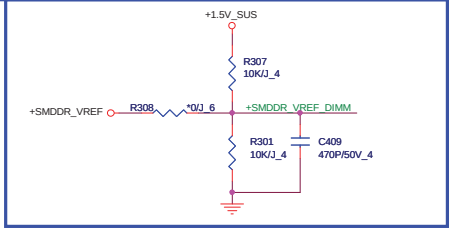
DDR_STD(DDR)



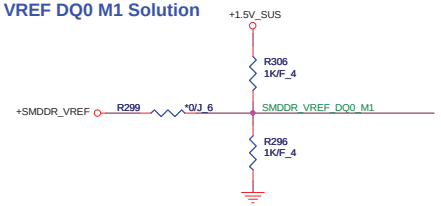
02/23 Remove 0ohm to GND

Place these Caps near So-Dimm0.





VREF DQ0 M1 Solution



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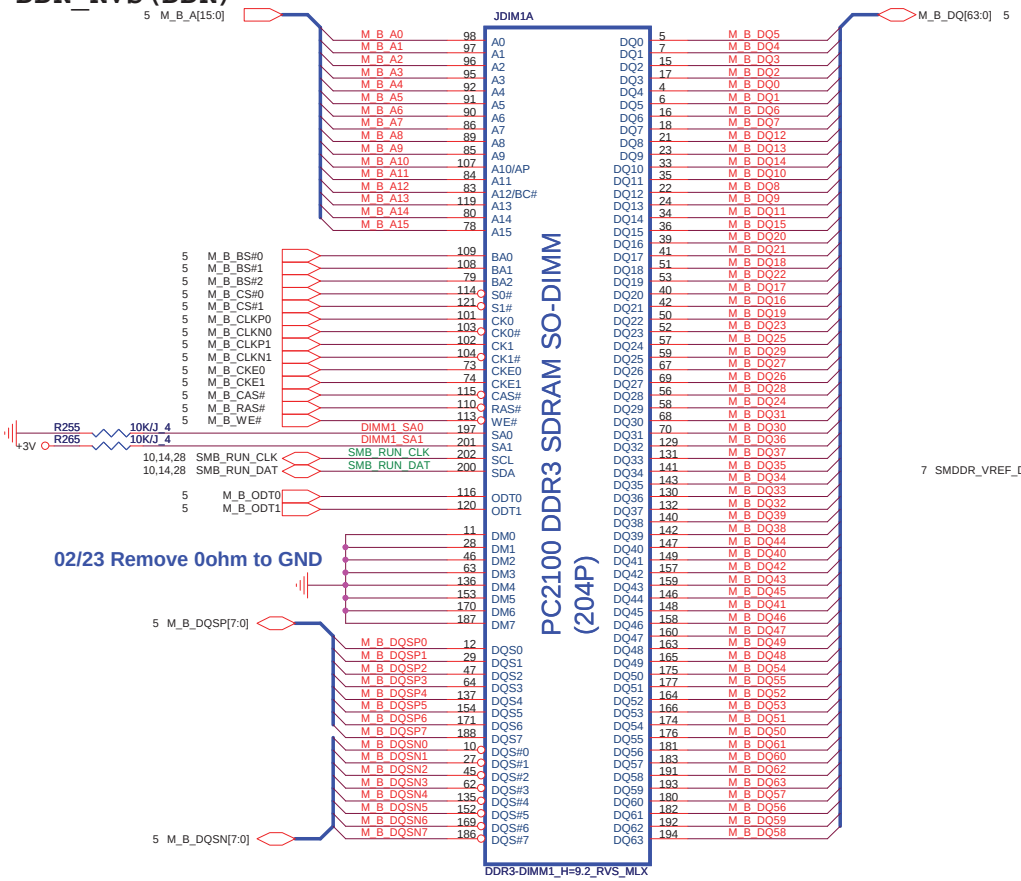
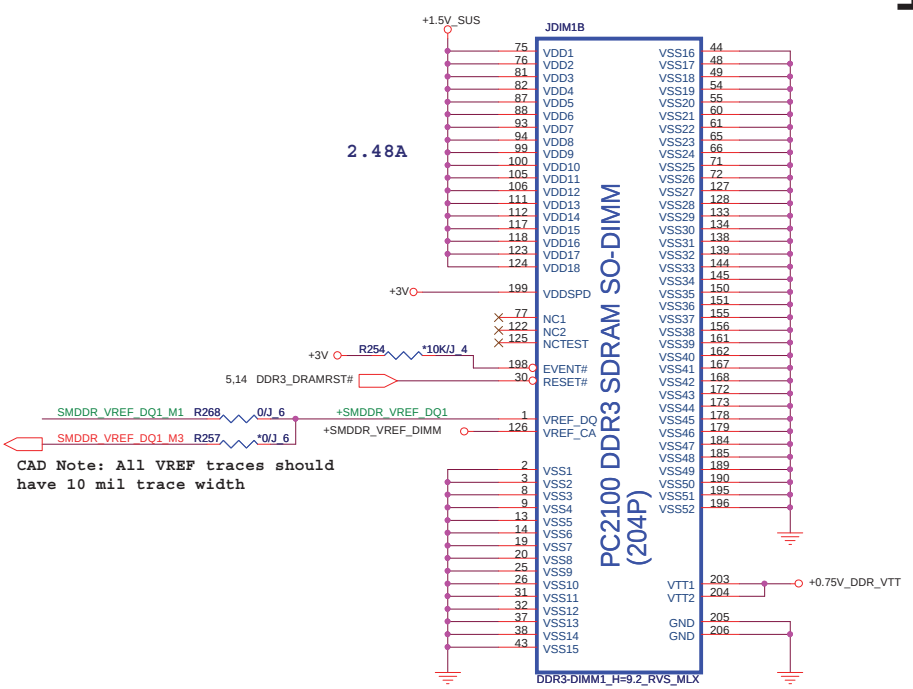
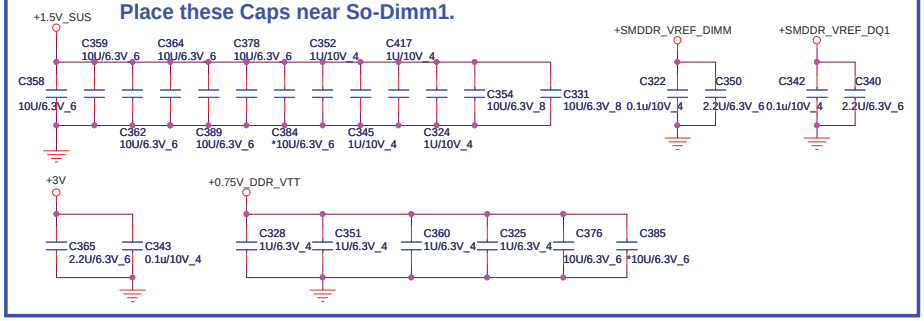
DDR_RVS (DDR)

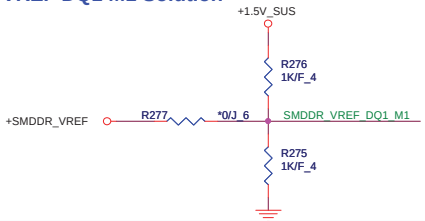




Place these Caps near So-Dimm1.



VREF DQ1 M1 Solution



	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080

Standard 8H type:DDR-C-2013310-204p-1

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PEX_IOVDD+PEX_IOVDDQ+PEX_PLLVDD >2.2A

2000mA

+1.05V_GPU

PLACE NEAR BALLS

C97 *EV@0.1U/10V_4
C73 EV@0.1U/10V_4
C114 EV@0.1U/10V_4
C122 EV@1U/6.3V_4
C28 EV@1U/6.3V_4
C24 EV@4.7U/6.3V_6
C516 EV@10U/6.3V_8
C17 EV@22U/6.3V_8

PLACE NEAR BGA

AK16 AK17 AK21 AK24 AK27

+1.05V_GPU

PLACE NEAR BALLS

C84 *EV@0.1U/10V_4
C23 EV@0.1U/10V_4
C125 EV@0.1U/10V_4
C131 EV@1U/6.3V_4
C134 EV@1U/6.3V_4
C71 EV@4.7U/6.3V_6
C18 EV@10U/6.3V_8
C517 EV@22U/6.3V_8

PLACE NEAR BGA

AG11 AG12 AG13 AG15 AG16 AG17 AG18 AG22 AG23 AG24 AG25 AG26 AJ14 AJ15 AJ19 AJ21 AJ22 AJ24 AJ25 AJ27 AK18 AK20 AK23 AK26 AL16

120mA

+3V_GPU

PLACE NEAR BGA

C95 EV@4.7U/6.3V_6
C81 EV@1U/6.3V_4

PLACE NEAR BALLS

C79 EV@0.1U/10V_4
C76 EV@0.1U/10V_4
C98 EV@0.1U/10V_4

J10 J11 J12 J13 J9

39 VGPU_VCC_SENSE
39 VGPU_VSS_SENSE

AD20 D35 P7 AD19 E35 R7

120mA 120-ohm / ESR=0.18

+1.05V_GPU L9 EV@BLM18AG121SN1D

PLACE NEAR BGA

C61 EV@4.7U/6.3V/X7R_6
C68 EV@1U/6.3V/X7R_4
C75 *EV@1U/6.3V_4
C78 *EV@1U/6.3V_4

+PEX_PLLVDD AG14

PLACE NEAR BALLS

C55 EV@0.1U/10V/X7R_4

120mA

+3V_GPU L6 EV@0_6 +PEX_SVDD_3V3 AG19 F7
+1.05V_GPU L10 *EV@0_6

PLACE NEAR BALLS

C56 EV@0.1U/10V_4
C42 EV@4.7U/6.3V_6

U23A
fcbga973-nvidia-n12p-ge
COMMON

PEX_IOVDD_1 PEX_IOVDD_2 PEX_IOVDD_3 PEX_IOVDD_4 PEX_IOVDD_5

PEX_IOVDDQ_1 PEX_IOVDDQ_2 PEX_IOVDDQ_3 PEX_IOVDDQ_4 PEX_IOVDDQ_5 PEX_IOVDDQ_6 PEX_IOVDDQ_7 PEX_IOVDDQ_8 PEX_IOVDDQ_9 PEX_IOVDDQ_10 PEX_IOVDDQ_11 PEX_IOVDDQ_12 PEX_IOVDDQ_13 PEX_IOVDDQ_14 PEX_IOVDDQ_15 PEX_IOVDDQ_16 PEX_IOVDDQ_17 PEX_IOVDDQ_18 PEX_IOVDDQ_19 PEX_IOVDDQ_20 PEX_IOVDDQ_21 PEX_IOVDDQ_22 PEX_IOVDDQ_23 PEX_IOVDDQ_24 PEX_IOVDDQ_25

VDD33_1 VDD33_2 VDD33_3 VDD33_4 VDD33_5

VDD_SENSE
NC_9/ VDD_SENSE
NC_16/ VDD_SENSE

GND_SENSE
NC_10/ GND_SENSE
NC_17/ GND_SENSE

PEX_PLLVDD

PEX_CAL_PD_VDDQ/ PEX_SVDD_3V3
NC_12/ PEX_SVDD_3V3

PEX_CAL_PU_GND/ NC
NC_1 NC_2 NC_3 NC_4 NC_5 NC_6 NC_7 NC_8 NC_11 NC_13 NC_14 NC_15 NC_18 NC_19

PCI EXPRESS

PEX_RX0 PEX_RX0* PEX_RX1 PEX_RX1* PEX_RX2 PEX_RX2* PEX_RX3 PEX_RX3* PEX_RX4 PEX_RX4* PEX_RX5 PEX_RX5* PEX_RX6 PEX_RX6* PEX_RX7 PEX_RX7* PEX_RX8 PEX_RX8* PEX_RX9 PEX_RX9* PEX_RX10 PEX_RX10* PEX_RX11 PEX_RX11* PEX_RX12 PEX_RX12* PEX_RX13 PEX_RX13* PEX_RX14 PEX_RX14* PEX_RX15 PEX_RX15*

AP17 AN17 AN19 AP19 AR19 AR20 AP20 AN20 AN22 AP22 AR22 AR23 AP23 AN23 AN25 AP25 AR25 AR26 AP26 AN26 AN28 AP28 AR28 AR29 AP29 AN29 AN31 AP31 AR31 AR32 AR34 AP34

PEG_TXP15 4 PEG_TXN15 4 PEG_TXP14 4 PEG_TXN14 4 PEG_TXP13 4 PEG_TXN13 4 PEG_TXP12 4 PEG_TXN12 4 PEG_TXP11 4 PEG_TXN11 4 PEG_TXP10 4 PEG_TXN10 4 PEG_TXP9 4 PEG_TXN9 4 PEG_TXP8 4 PEG_TXN8 4 PEG_TXP7 4 PEG_TXN7 4 PEG_TXP6 4 PEG_TXN6 4 PEG_TXP5 4 PEG_TXN5 4 PEG_TXP4 4 PEG_TXN4 4 PEG_TXP3 4 PEG_TXN3 4 PEG_TXP2 4 PEG_TXN2 4 PEG_TXP1 4 PEG_TXN1 4 PEG_TXP0 4 PEG_TXN0 4

PEX_TX0 PEX_TX0* PEX_TX1 PEX_TX1* PEX_TX2 PEX_TX2* PEX_TX3 PEX_TX3* PEX_TX4 PEX_TX4* PEX_TX5 PEX_TX5* PEX_TX6 PEX_TX6* PEX_TX7 PEX_TX7* PEX_TX8 PEX_TX8* PEX_TX9 PEX_TX9* PEX_TX10 PEX_TX10* PEX_TX11 PEX_TX11* PEX_TX12 PEX_TX12* PEX_TX13 PEX_TX13* PEX_TX14 PEX_TX14* PEX_TX15 PEX_TX15*

AL17 PEG_RXP15_C C80
AM17 PEG_RXN15_C C89
AM18 PEG_RXP14_C C109
AM19 PEG_RXN14_C C102
AL19 PEG_RXP13_C C113
AK19 PEG_RXN13_C C108
AL20 PEG_RXP12_C C106
AM20 PEG_RXN12_C C112
AM21 PEG_RXP11_C C120
AM22 PEG_RXN11_C C123
AL22 PEG_RXP10_C C124
AK22 PEG_RXN10_C C127
AL23 PEG_RXP9_C C129
AM23 PEG_RXN9_C C137
AM24 PEG_RXP8_C C128
AM25 PEG_RXN8_C C136
AL25 PEG_RXP7_C C130
AK25 PEG_RXN7_C C138
AL26 PEG_RXP6_C C143
AM26 PEG_RXN6_C C145
AM27 PEG_RXP5_C C144
AM28 PEG_RXN5_C C147
AL28 PEG_RXP4_C C160
AK28 PEG_RXN4_C C153
AK29 PEG_RXP3_C C162
AL29 PEG_RXN3_C C157
AM29 PEG_RXP2_C C165
AM30 PEG_RXN2_C C168
AM31 PEG_RXP1_C C167
AM32 PEG_RXN1_C C170
AN32 PEG_RXP0_C C171
AP32 PEG_RXN0_C C173

EV@0.1U/10V_4

PEG_RXP15 4 PEG_RXN15 4 PEG_RXP14 4 PEG_RXN14 4 PEG_RXP13 4 PEG_RXN13 4 PEG_RXP12 4 PEG_RXN12 4 PEG_RXP11 4 PEG_RXN11 4 PEG_RXP10 4 PEG_RXN10 4 PEG_RXP9 4 PEG_RXN9 4 PEG_RXP8 4 PEG_RXN8 4 PEG_RXP7 4 PEG_RXN7 4 PEG_RXP6 4 PEG_RXN6 4 PEG_RXP5 4 PEG_RXN5 4 PEG_RXP4 4 PEG_RXN4 4 PEG_RXP3 4 PEG_RXN3 4 PEG_RXP2 4 PEG_RXN2 4 PEG_RXP1 4 PEG_RXN1 4 PEG_RXP0 4 PEG_RXN0 4

PEX_REFCLK PEX_REFCLK* AR16 AR17 CLK_PCIE_VGAP 10 CLK_PCIE_VGAN 10

PEX_TSTCLK_OUT PEX_TSTCLK_OUT* AJ17 PEX_TSTCLK R89 *EV@200/J_4 ?? R90 1 2 EV@100K/J_4
AJ18 PEX_TSTCLK#

PEX_RST* AM16 VGA_RST# R87 EV@0/J_4 GPU_RST# GPU_RST# 31

PEX_CLKREQ* AR13 PEX_CLKREQ# R401 EV@10K/J_4 +3V_GPU

PEX_TERMP AG21 PEX_TERMP R94 EV@2.49K/F_4

TESTMODE AP35 TESTMODE R110 EV@10K/J_4

R61 EV@10K_4
R60 EV@40.2K/F_4

Ffor N12P-GE, they can be unstuffed by default

GPU RST#

+3V

C59 EV@0.1U/10V_4

4,10,26,28,31,32 PLTRST#
11 DGPU_HOLD_RST#

R55 EV@100K/J_4

U3 EV@TC7SH08FU

GPU_RST#

GPU all PWROK

+3V +3V_GPU

R396 EV@10K_4
R397 EV@10K_4

GFXPG GFXPG 11,31

Q24 EV@MMBT3904

+1.5V_GPU R386 EV@10K_4

*EV@1000P/50V/X7R_4@NC C515

Q23 EV@PDTC143TT

+3V_GPU

R385 *EV@10K/J_4 +3V

PCIE_CLKREQ_PEG# 10

R383 EV@10K/J_4

GFXPG R384 *EV@10K/F_4

Q22 EV@DTC144EUA

PEX_CLKREQ#

Q21 EV@DTC144EUA

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U23B
fcbga973-nvidia-n12p-ge
COMMON

U23C
fcbga973-nvidia-n12p-ge
COMMON

MEMORY I/F A

MEMORY I/F C

5500mA

+1.5V_GPU

POP For Debug only
Place close to ball

30-ohm ESR=0.01-ohm
EV@BLM18AG331SN1D

100mA

+1.05V_GPU

15mils width

Check

PLACE NEAR BGA

PLACE NEAR BALLS

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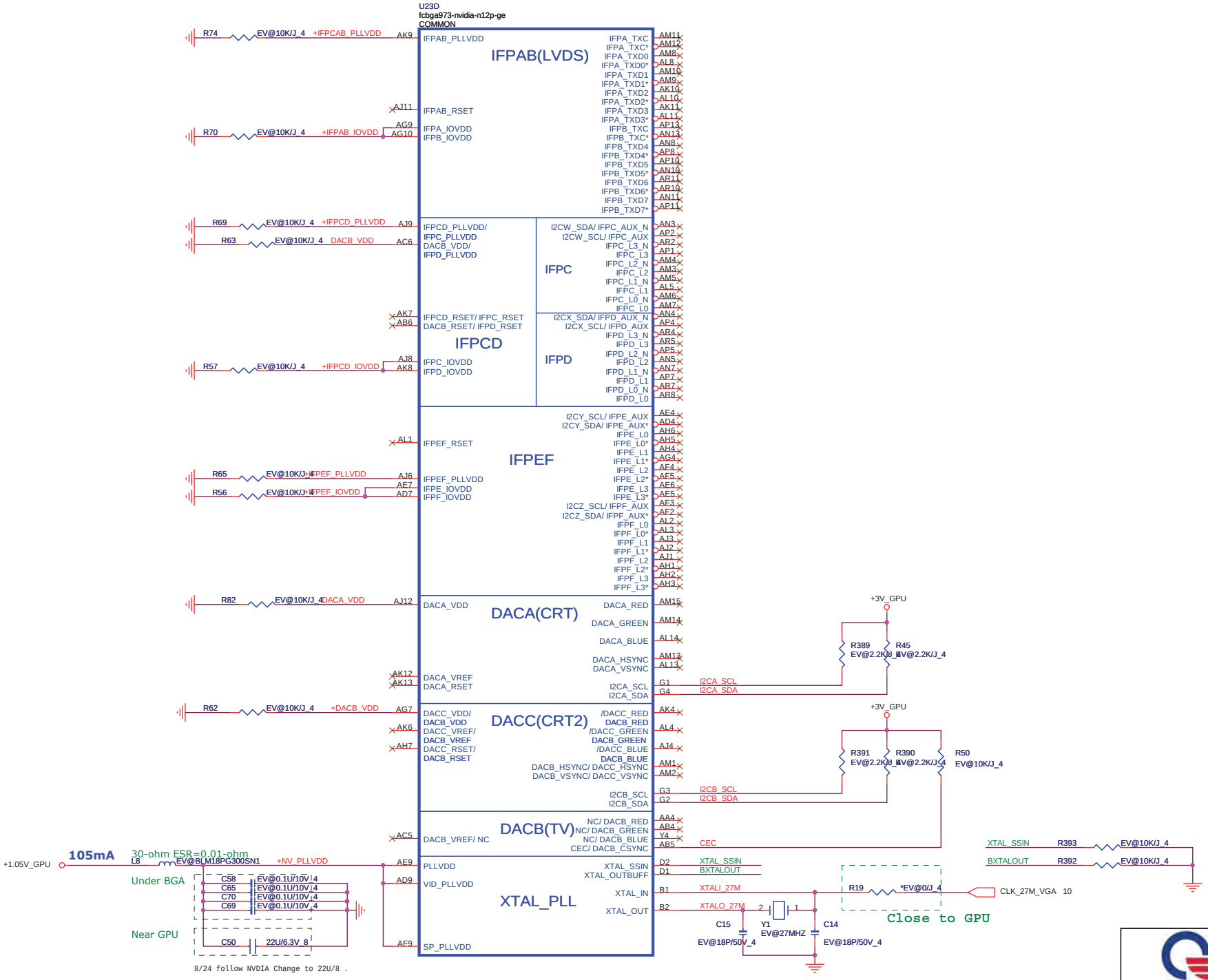

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Size	Document Number: N12P-GE (DISPLAY) 3/5	Rev: 1A
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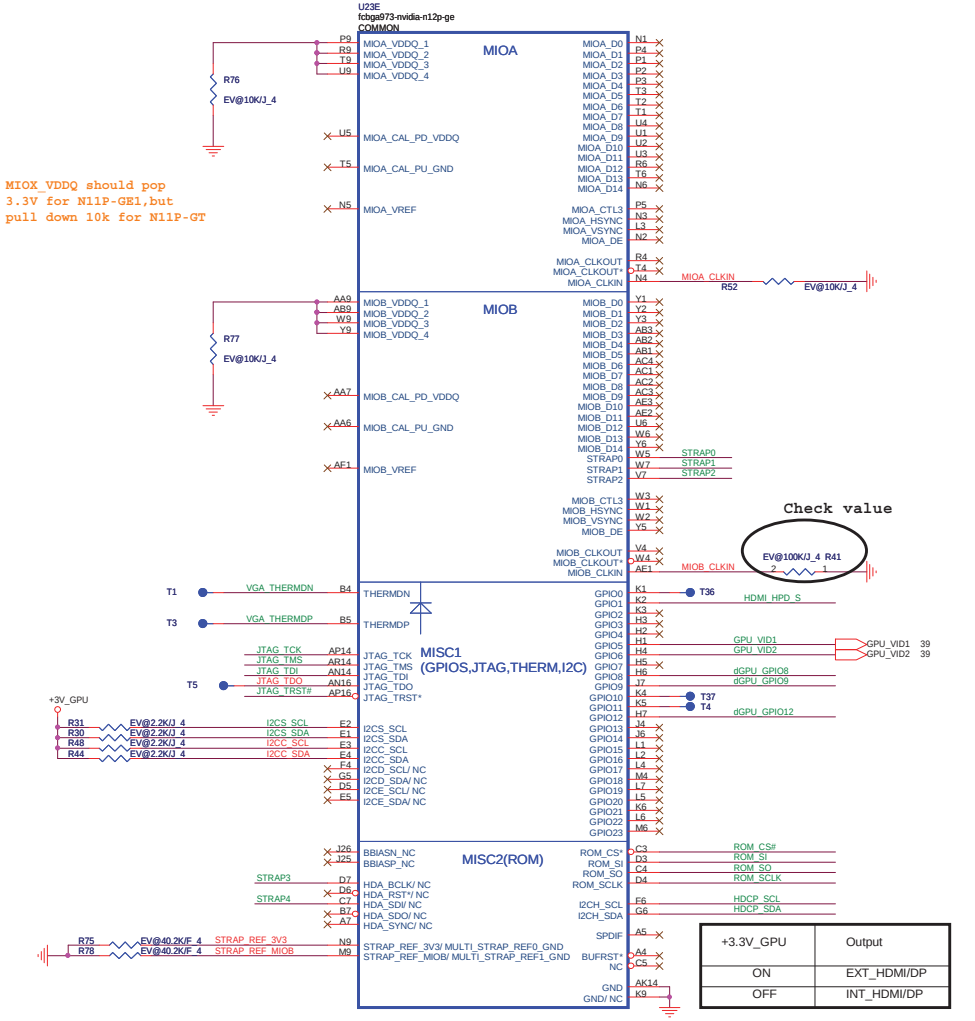
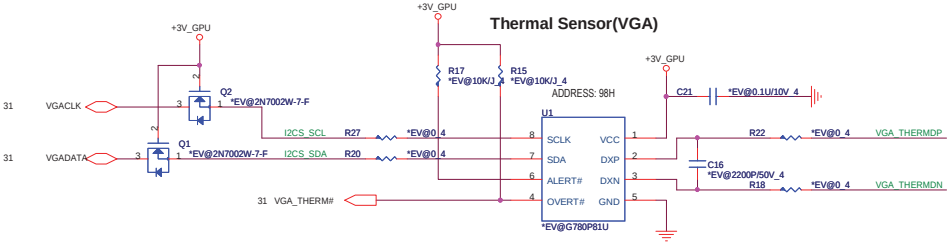


+3.3V_GPU	Output
ON	EXT_HDMI/DP
OFF	INT_HDMI/DP



	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	1010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	0011
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	0101
STRAP3	SOR_EXPOSED[3]	SOR_EXPOSED[2]	SOR_EXPOSED[1]	SOR_EXPOSED[0]	TBD
STRAP4	Reserve	Reserve	PCI_MAX_SPEED	DP_PLL_VDD3	TBD

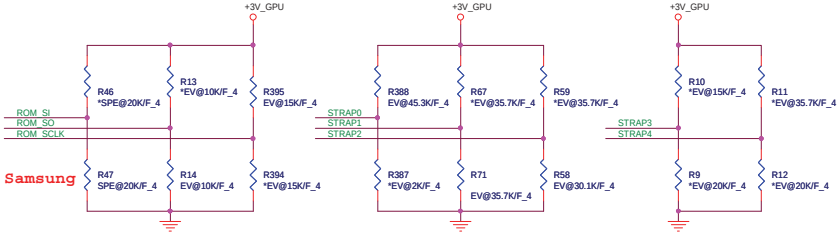
	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

VRAM Configuration Table

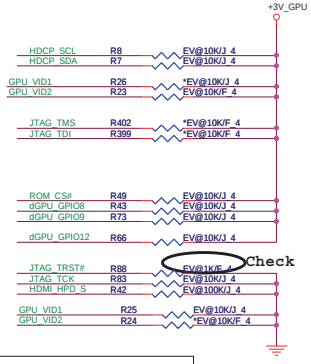
RAMCFG [3:0]	DESCRIPTION	Quanta PN(Q buy)	Quanta PN(W buy)	Vendor PN
* 0x3(0011)	900MHz 512MB(64M*16) Samsung	AKD5LGHT500		K4W1G1646E-HC11
0x2(0010)	900MHz 512MB(64M*16) Hynix	AKD5LZWTW01	AKD5LZWTW00	H5TQ1G63BFR-11C
0x6(0110)	800MHz 1GB(128M*16) Hynix	AKD5MGGTW00	AKD5MGGTW01	H5TQ2G63BFR-12C
0x7(0111)	800MHz 1GB(128M*16) Samsung	AKD5MGGT501	AKD5MGGT502	K4W2G1646B-HC12

4.99K/F_4 ==> CS24992FB26
10K/F_4 ==> CS31002FB26
15K/F_4 ==> CS31502FB24
20K/F_4 ==> CS32002FB29
30.1K/F_4 ==> CS33012FB18
35.7K/F_4 ==> CS33572FB13
45.3K/F_4 ==> CS34532FB18

ROM_SI Strap Bit for RAM Mapping



N11P-GE1 DevID is 0x0DFE, so pull up
ROM_SCLK with 15Kohm and STRAP2
pull up 35Kohm



GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	N/A	
3	OUT	N/A	
4	OUT	N/A	
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

NV VID Table for N12P-GE

GPU_VID1	GPU_VID2	+VGPU_CORE
0	0	0.825V
1	0	0.9V
0	1	0.95V
1	1	TBD

Modify 8/18

Quanta Computer Inc.
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	N12P-GE (GPIO&STRAPS)4/5	1A

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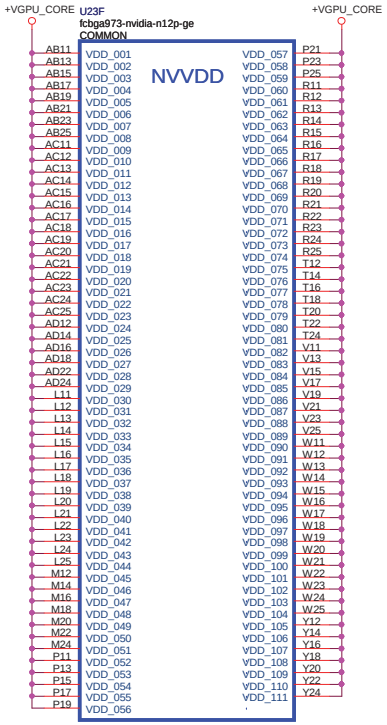

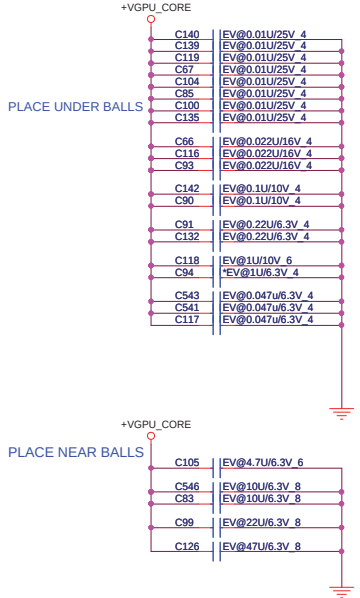

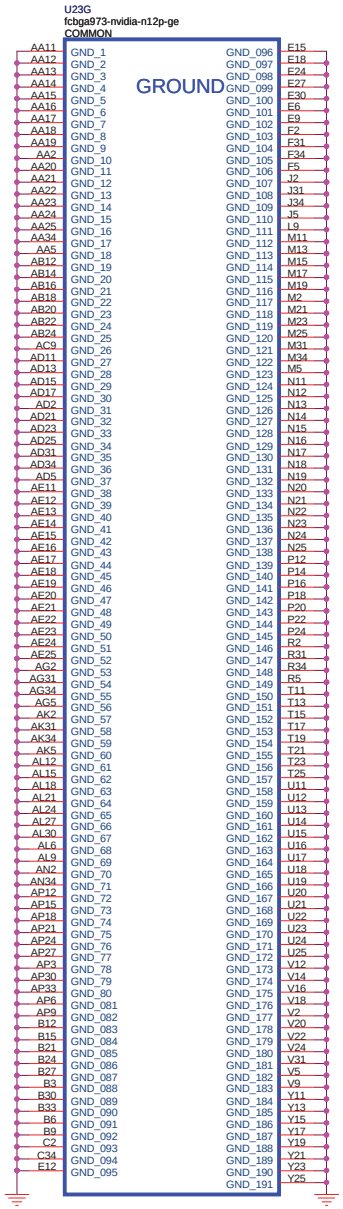

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	N12P-GE(POWER&THM)5/5	1A
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17 VMA_DQ[63..0]
17 VMA_DM[7..0]
17 VMA_WDQS[7..0]
17 VMA_RDQS[7..0]

CHANNEL A: 512MB/1024MB DDR3

U7 / U27 / U6 / U26 — 96-BALL SDRAM DDR3 SPE@K4W1G1646E-HC11

Should be 240 Ohms +-1%

R114 EV@240/F_4 (U7)
R412 EV@240/F_4 (U27)
R138 EV@240/F_4 (U6)
R408 EV@240/F_4 (U26)

+1.5V_GPU

R142 EV@1.33K/F_4 — VREFC_VMA1 — R141 EV@1.33K/F_4 — C240 EV@0.01U/25V_4
R144 EV@1.33K/F_4 — VREFD_VMA1 — R143 EV@1.33K/F_4 — C241 EV@0.01U/25V_4
C594 *EV@10U/6.3V_6
R140 EV@1.33K/F_4 — VREFC_VMA3 — R139 EV@1.33K/F_4 — C237 EV@0.01U/25V_4
R136 EV@1.33K/F_4 — VREFD_VMA3 — R137 EV@1.33K/F_4 — C236 EV@0.01U/25V_4

3/22 Change R1/R2/C values for VREF

Placement has to be close to VRAM

R135 EV@162/F_4 — VMA_CLKP0
R134 EV@162/F_4 — VMA_CLKP1
VMA_CLKN0
VMA_CLKN1

+1.5V_GPU decoupling:
C593 C602 C214 C523 C601 C243 C40 C182 — EV@1U/6.3V_4
C603 C610 C592 C238 — EV@0.1U/10V_4
C599 C596 C595 C181 C212 C588 C35 — EV@1U/6.3V_4
C606 C607 C580 C609 — EV@0.1U/10V_4
C590 C246 C598 C591 C239 C604 C188 — EV@1U/6.3V_4
C210 C245 C600 C608 — EV@0.1U/10V_4
C192 C605 C235 C579 C242 C597 C524 — EV@1U/6.3V_4
C244 C577 C211 C611 — EV@0.1U/10V_4

GE1 FOR 243 BUT GT/E REQUIRE CHECK FAE

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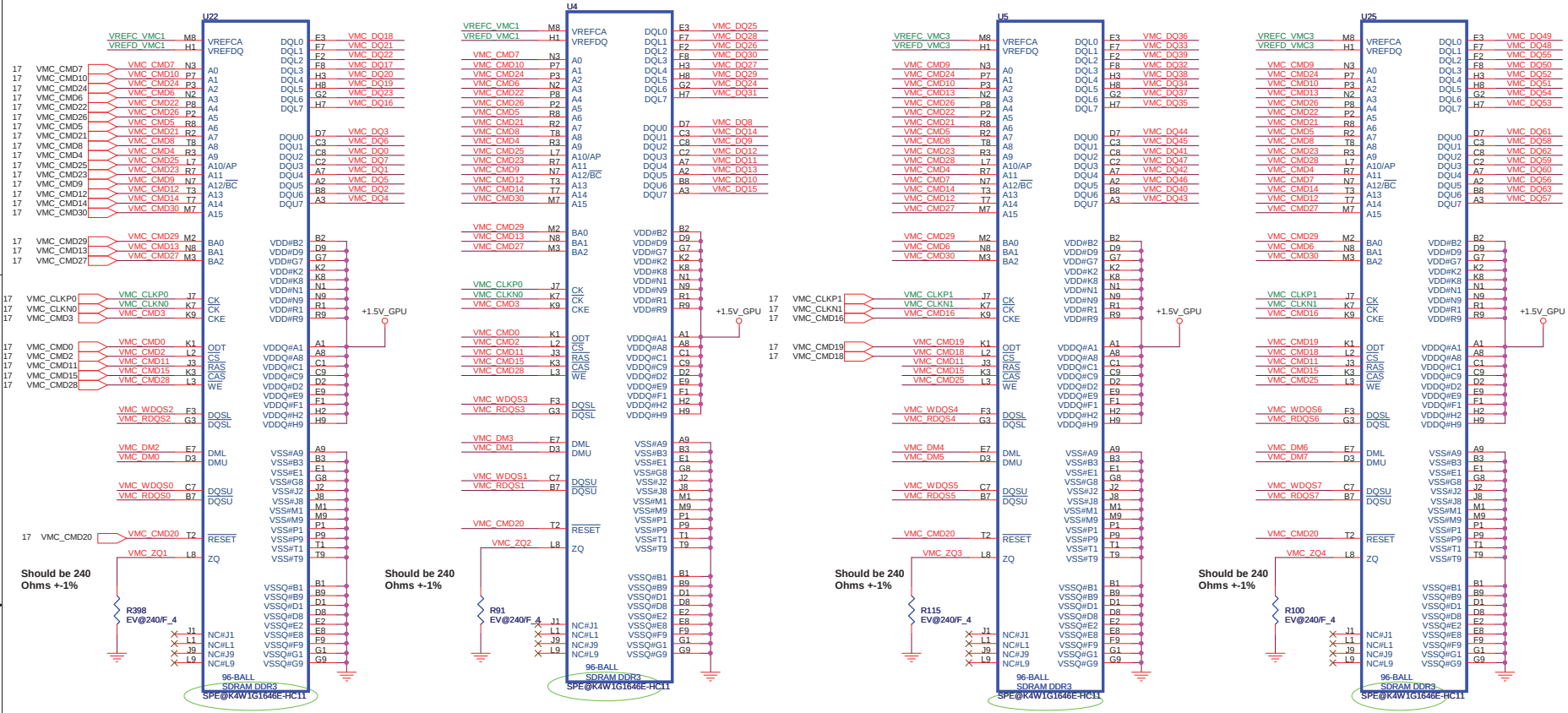
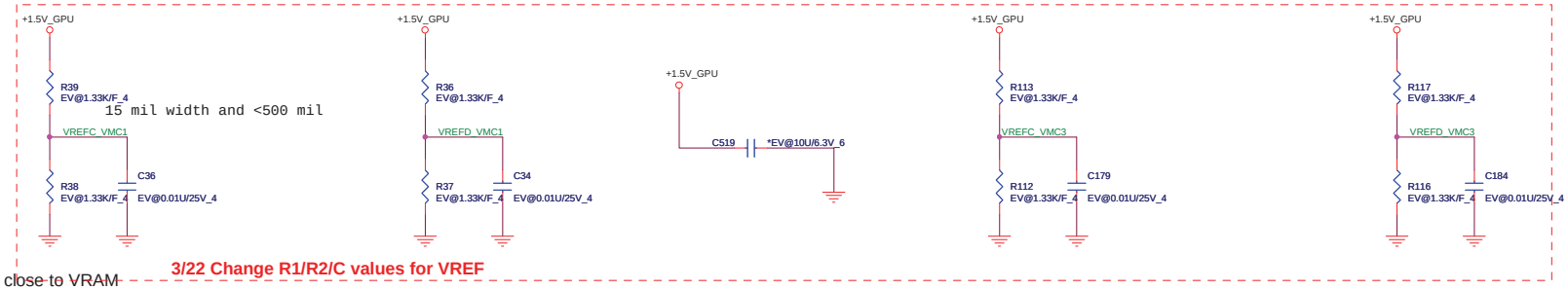
CHANNEL B: 512MB/1024MB DDR3

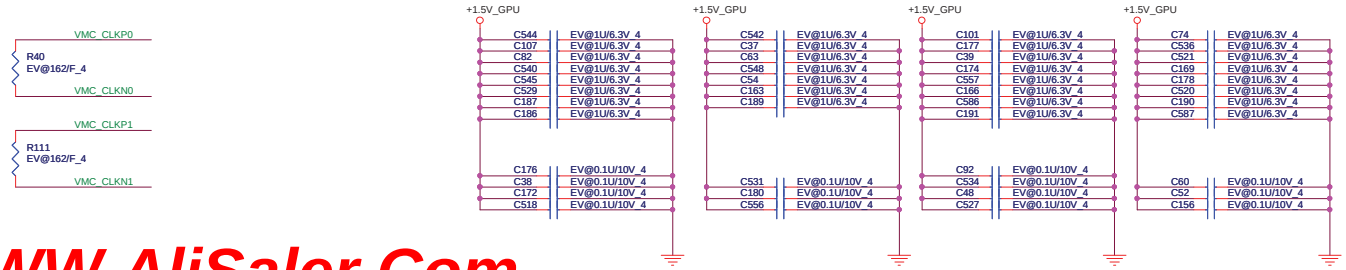
17 VMC_DQ[63..0]
17 VMC_DM[7..0]
17 VMC_WDQS[7..0]
17 VMC_RDQS[7..0]





Placement has to be close to VRAM

3/22 Change R1/R2/C values for VREF



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	N12P-GE VRAM-2	1A

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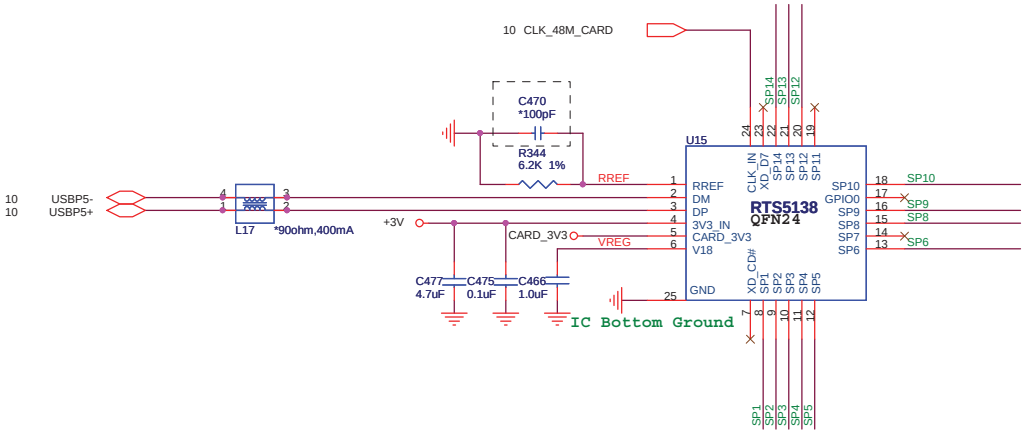
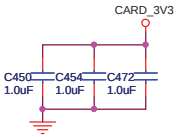
RST5138 SIDO

SD/SDHC CARD READER



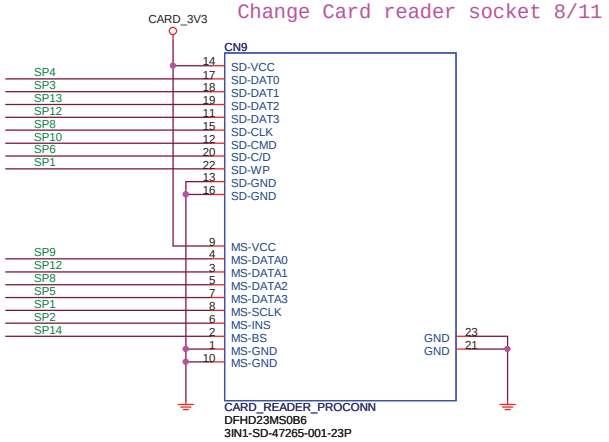


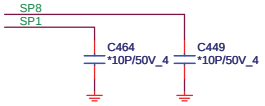
Share Pin

Share Pin	XD	MS	SD
SP1	XDR/B#	MS_CLK	SD_WP
SP2	XD_RE#	MS_INS#	
SP3	XD_CE#		SD_D1
SP4	XD_CLE	MS_D7	SD_D0
SP5	XD_ALE	MS_D3	SD_D7
SP6	XD_WE#		SD_CD#
SP7	XD_WP	MS_D6	SD_D6
SP8	XD_D0	MS_D2	SD_CLK
SP9	XD_D1	MS_D0	SD_D5
SP10	XD_D2		SD_CMD
SP11	XD_D3	MS_D4	SD_D4
SP12	XD_D4	MS_D1	SD_D3
SP13	XD_D5	MS_D5	SD_D2
SP14	XD_D6	MS_BS	

SD/MS CONNDETOR

Change Card reader socket 8/11





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	Card Reader RST5138	3G

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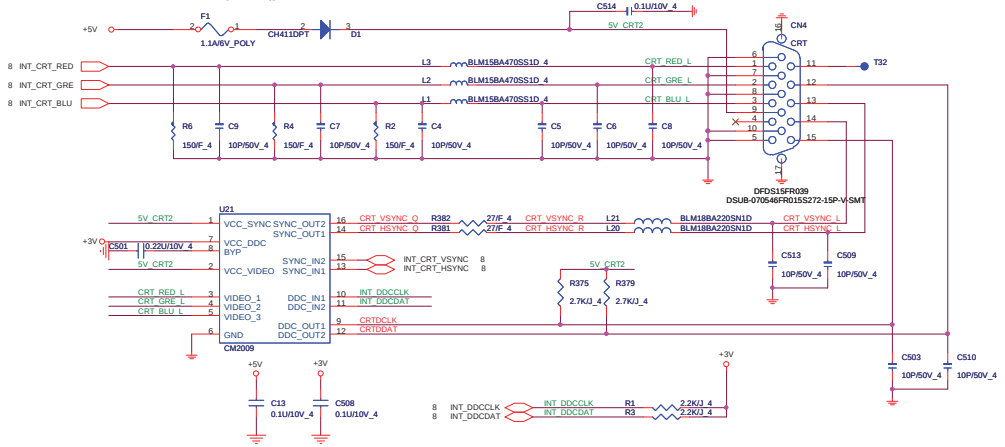
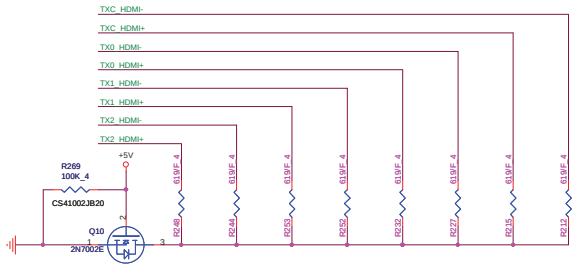
CRT CONN/DDC LEVEL SHIFT

40mils

TBD CN5500 FOOTPRINT

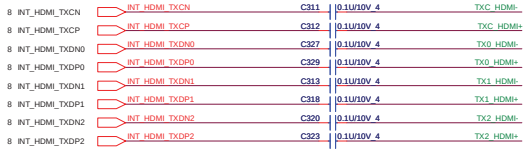


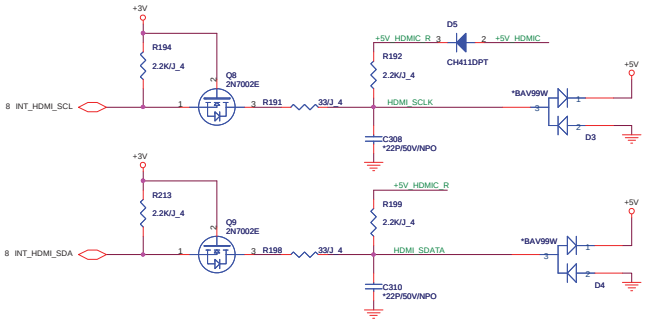


PLACE PULL DOWN RESISTORS CLOSE TO DIFFERENTIAL PAIRS CONNECTED TO SOLID GROUND FLOOD WHICH IS CONTROLLED BY THE FET
AVOID STUBS TO ALL DIFFERENTIAL TRACES

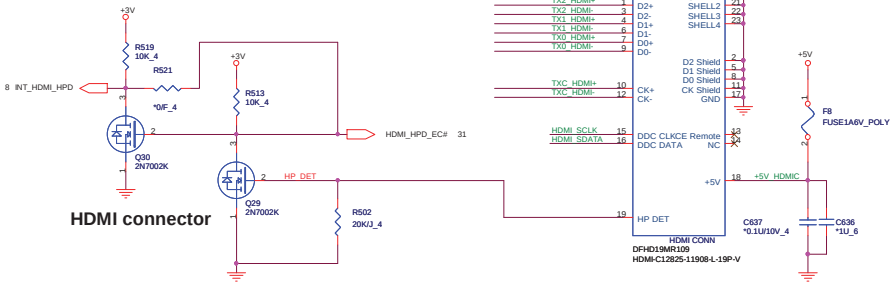
INT-HDMI

PLACE AC CAP CLOSE TO CONNECTOR





HDMI CONN



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	CRT CONN/HDMI	1A

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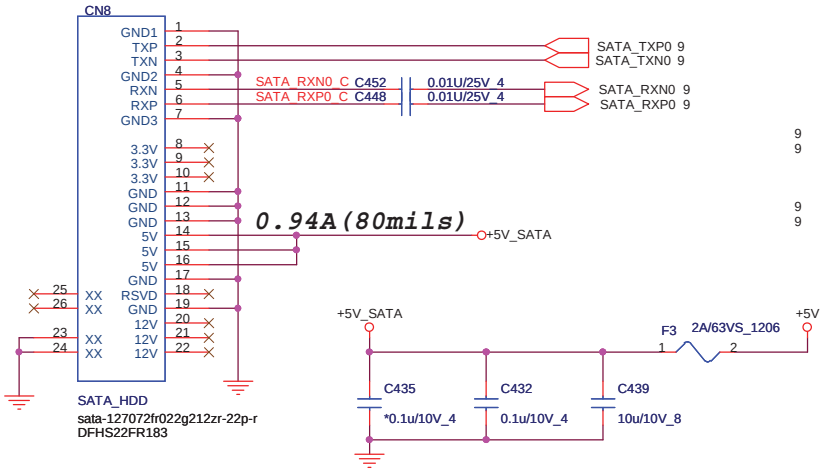
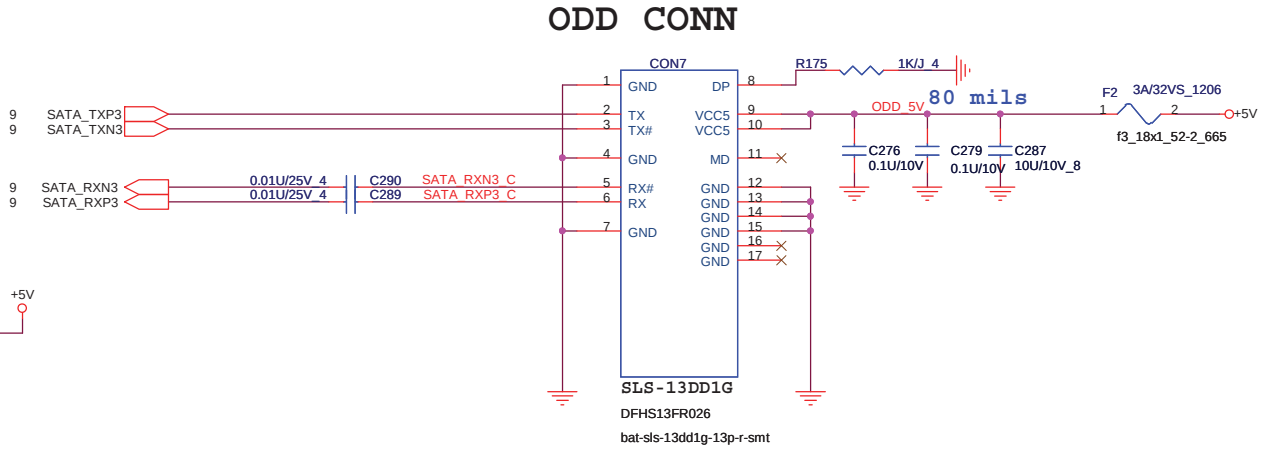
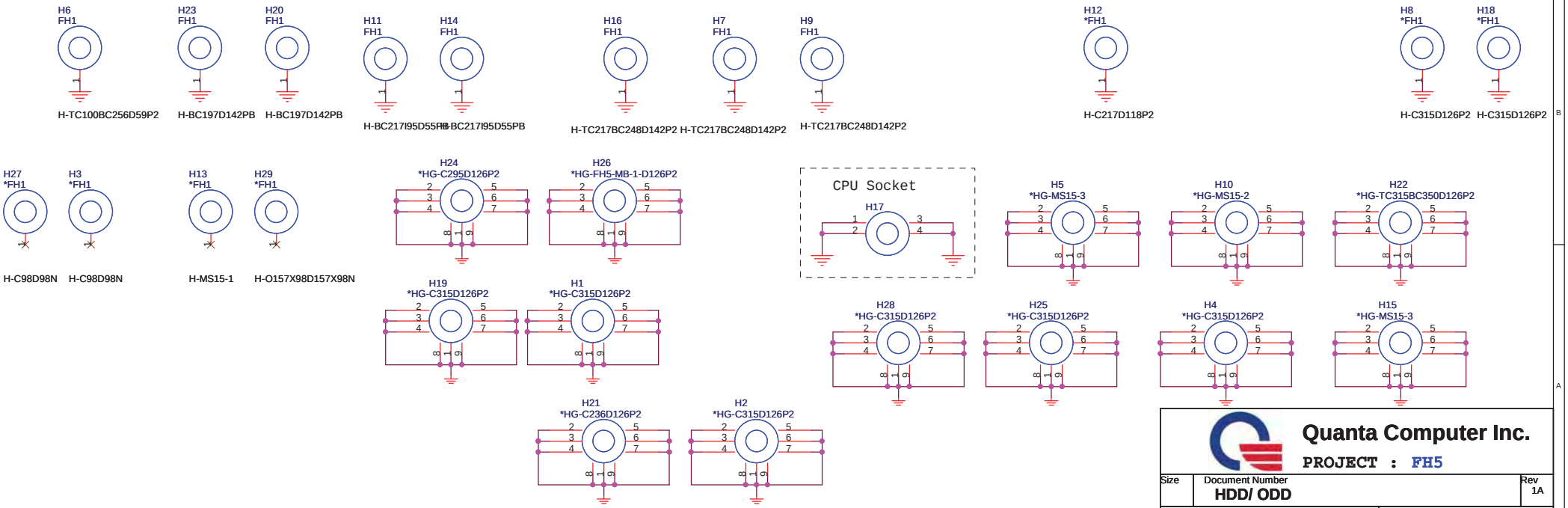
2.5" SATA HDD



SATA ODD





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	HDD/ ODD	1A
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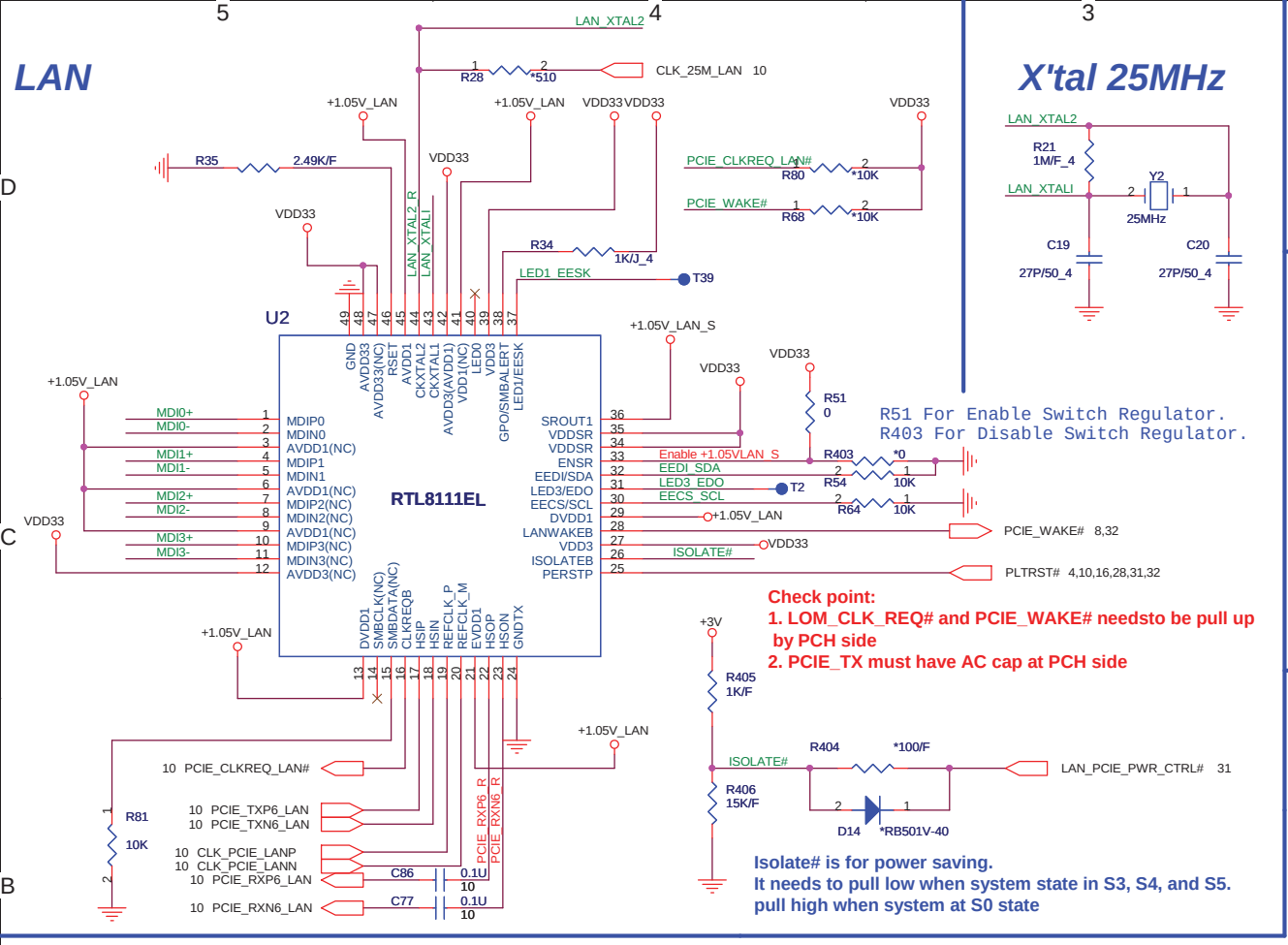
LAN



R51 For Enable Switch Regulator.
R403 For Disable Switch Regulator.

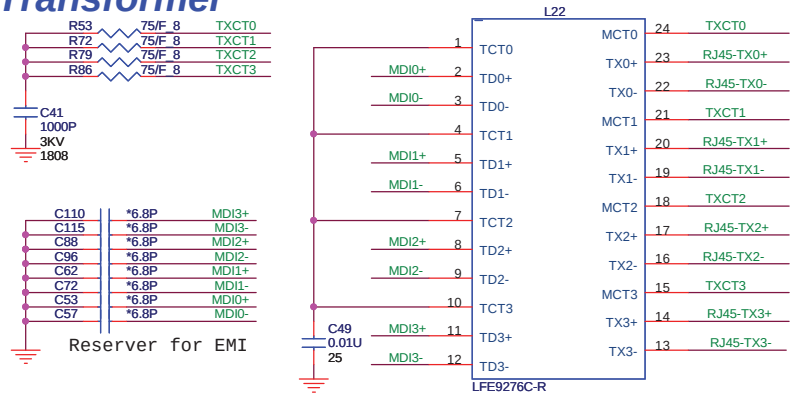
Check point:
1. LOM_CLK_REQ# and PCIE_WAKE# needsto be pull up by PCH side
2. PCIE_TX must have AC cap at PCH side

Isolate# is for power saving.
It needs to pull low when system state in S3, S4, and S5.
pull high when system at S0 state

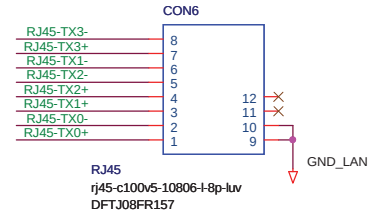
X'tal 25MHz

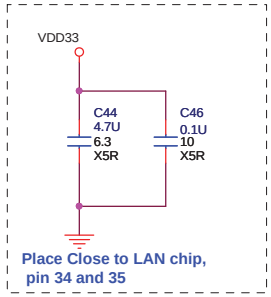
LAN EEPROM(DEL)

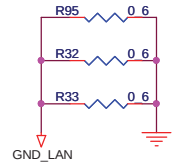
Transformer



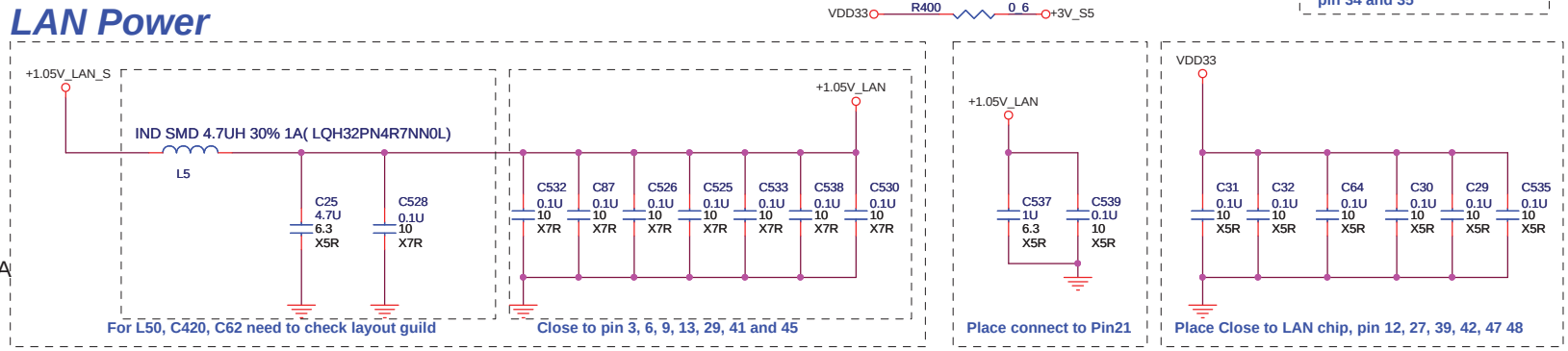
RJ45







LAN Power



REQ by layout

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	LAN_RTL8111E-GR/RJ45	1A
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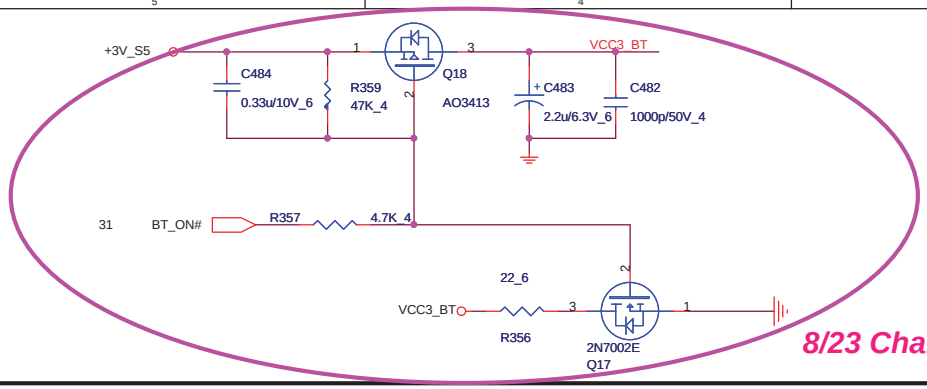
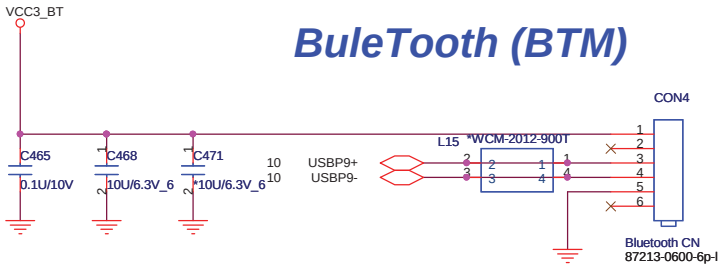
BuleTooth (BTM)

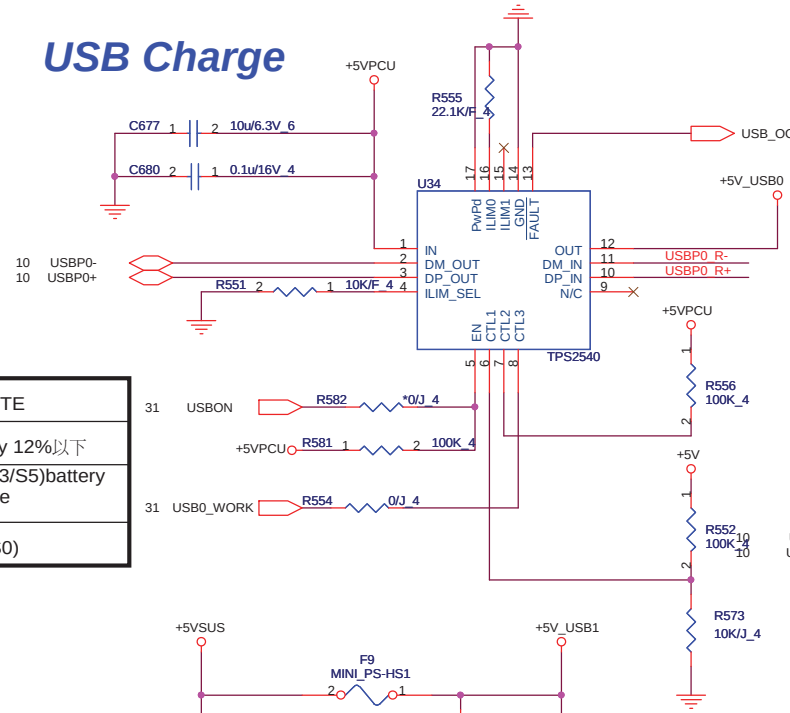


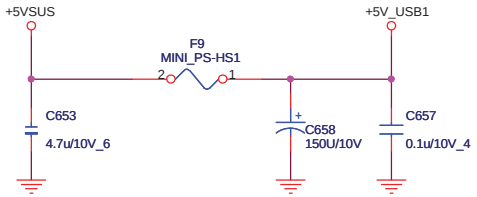
8/23 Change BT on circuit.

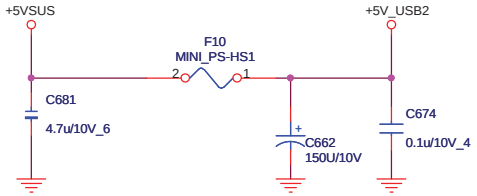


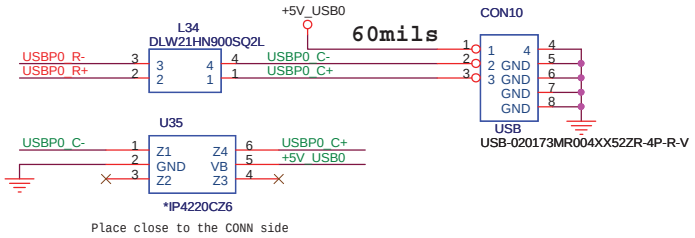
USB Connector

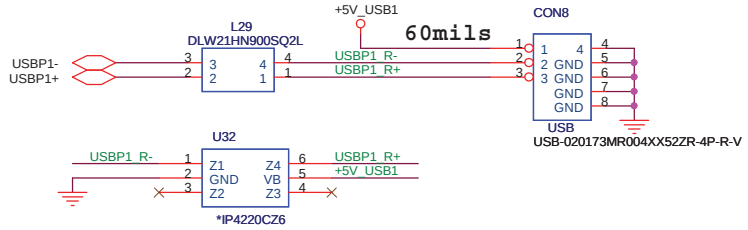
USB Charge

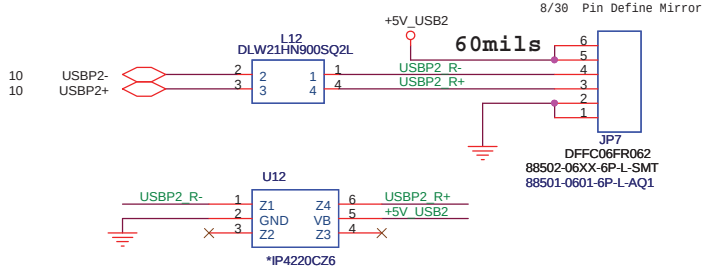












	CTL1	CTL2	CTL3	NOTE
ES(PG1.1)	0	1	0	SDP(S3/S5)battery 12%以下
	0	1	1	DCP, Auto-detect(S3/S5)battery 12%以上 or AC mode
	1	1	0	SDP(S0)

USB0_WORK	Mode
Low - S5 - 1.8A	DCP, Auto-detect
High - S0/S3 - 1.5A USB wake up with S3	CDP, BC Spec 1.1 == PCH HOST

	R321	mA	
OC limitation	100k ohm	480	
	22.1k ohm	2171	Applied Now

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	USB/BLUE TOOTH	1A
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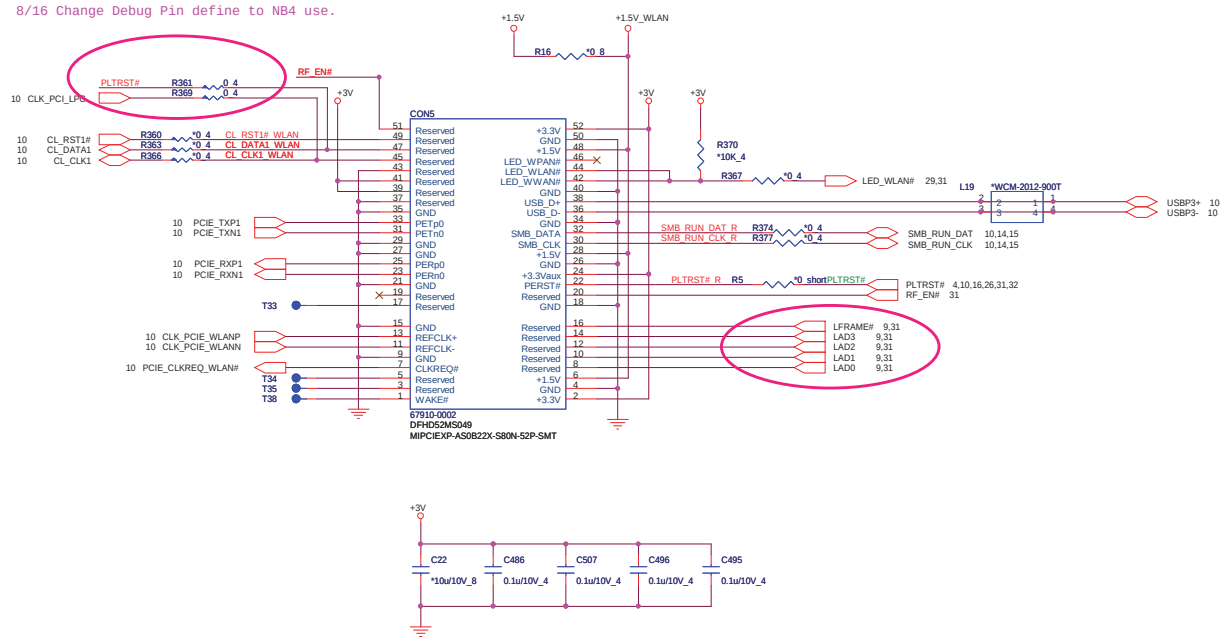
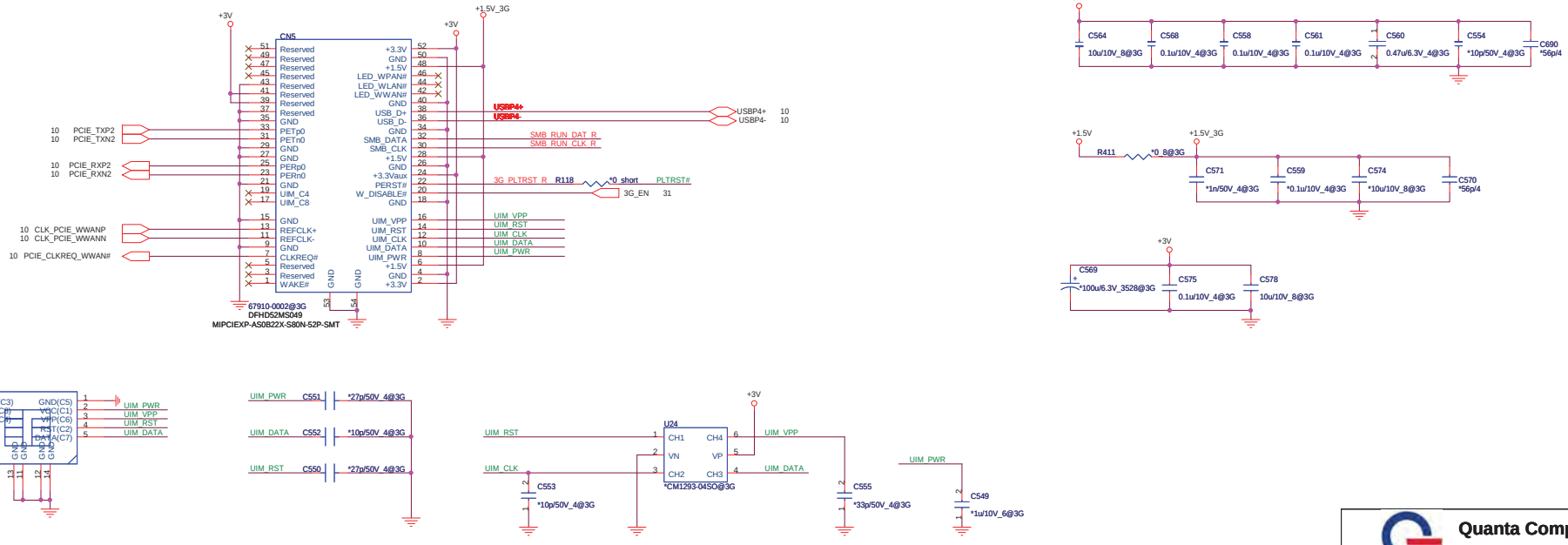
MINI CARD (WLAN)



Mini Card2-3G(MNC)



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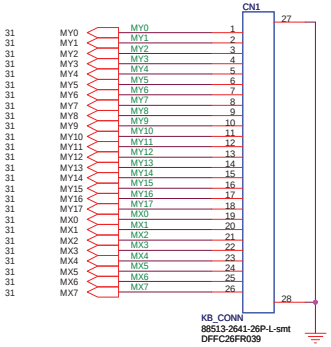
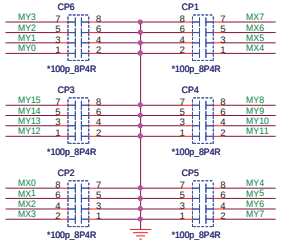
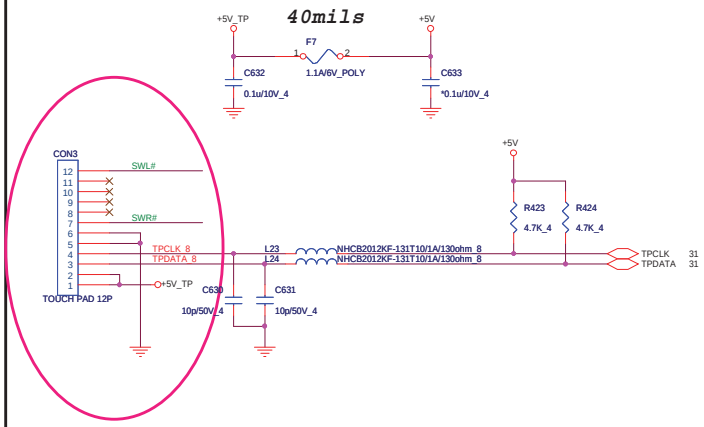
Keyboard(KBC)



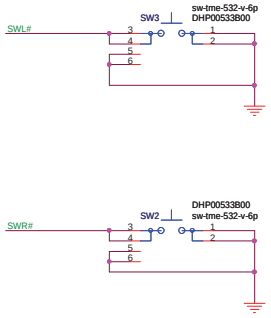
For EMI Reserve Caps for debug



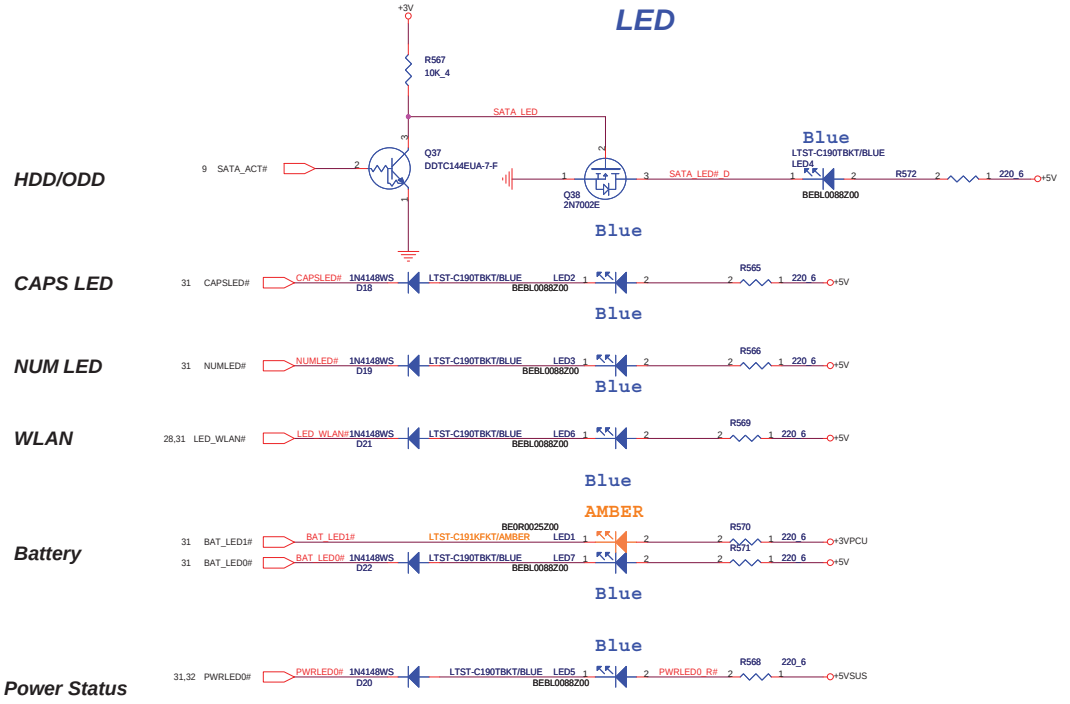
Touch Pad



8/23 Change TP to 12 pin conn.



LED



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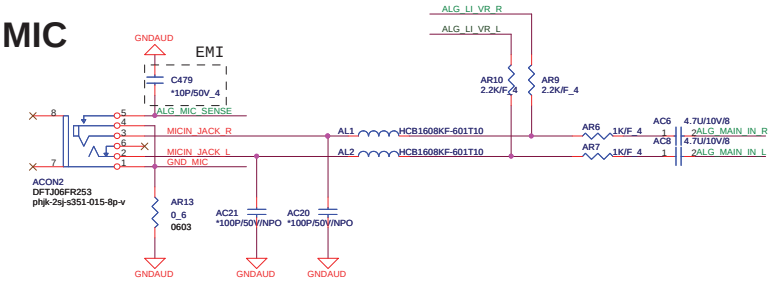
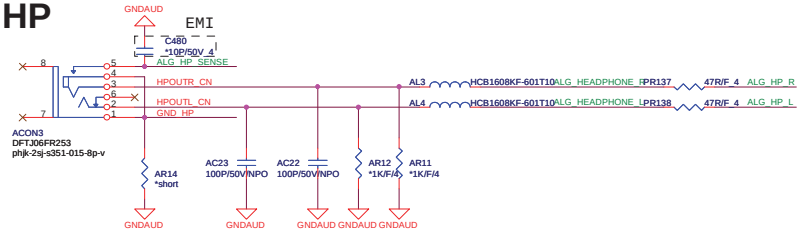
Codec ALC269-VB

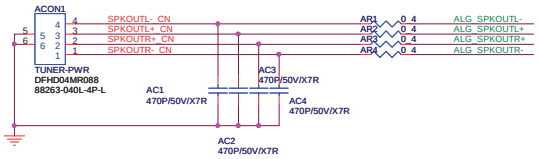
MIC



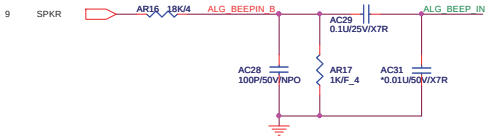
HP



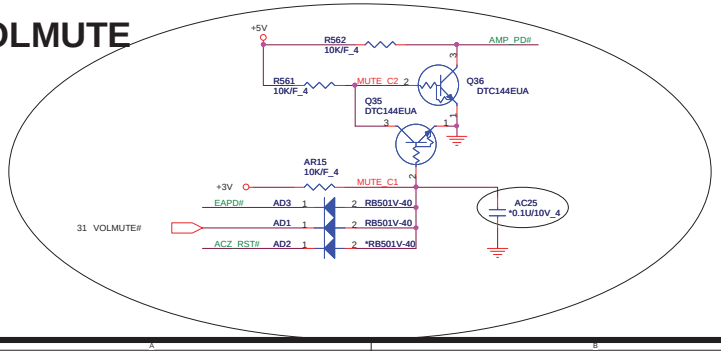
SPKR



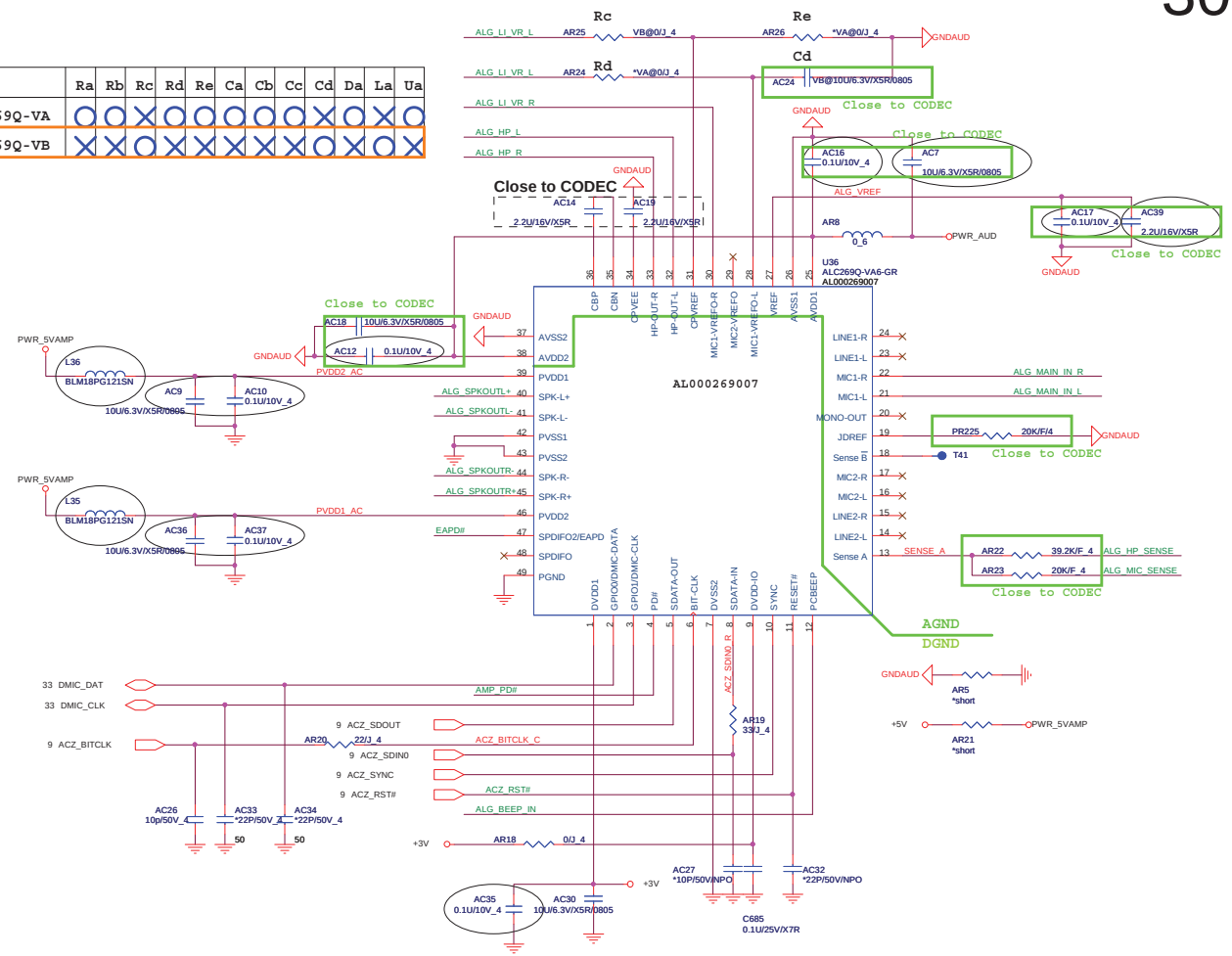
BEEP

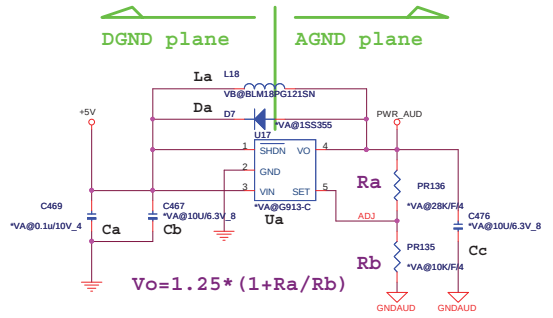


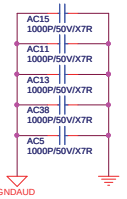
VOLMUTE



U23	Ra	Rb	Rc	Rd	Re	Ca	Cb	Cc	Cd	Da	La	Ua
ALC269Q-VA	O	O	X	O	O	O	O	O	X	O	X	O
ALC269Q-VB	X	X	O	X	X	X	X	X	O	X	O	X







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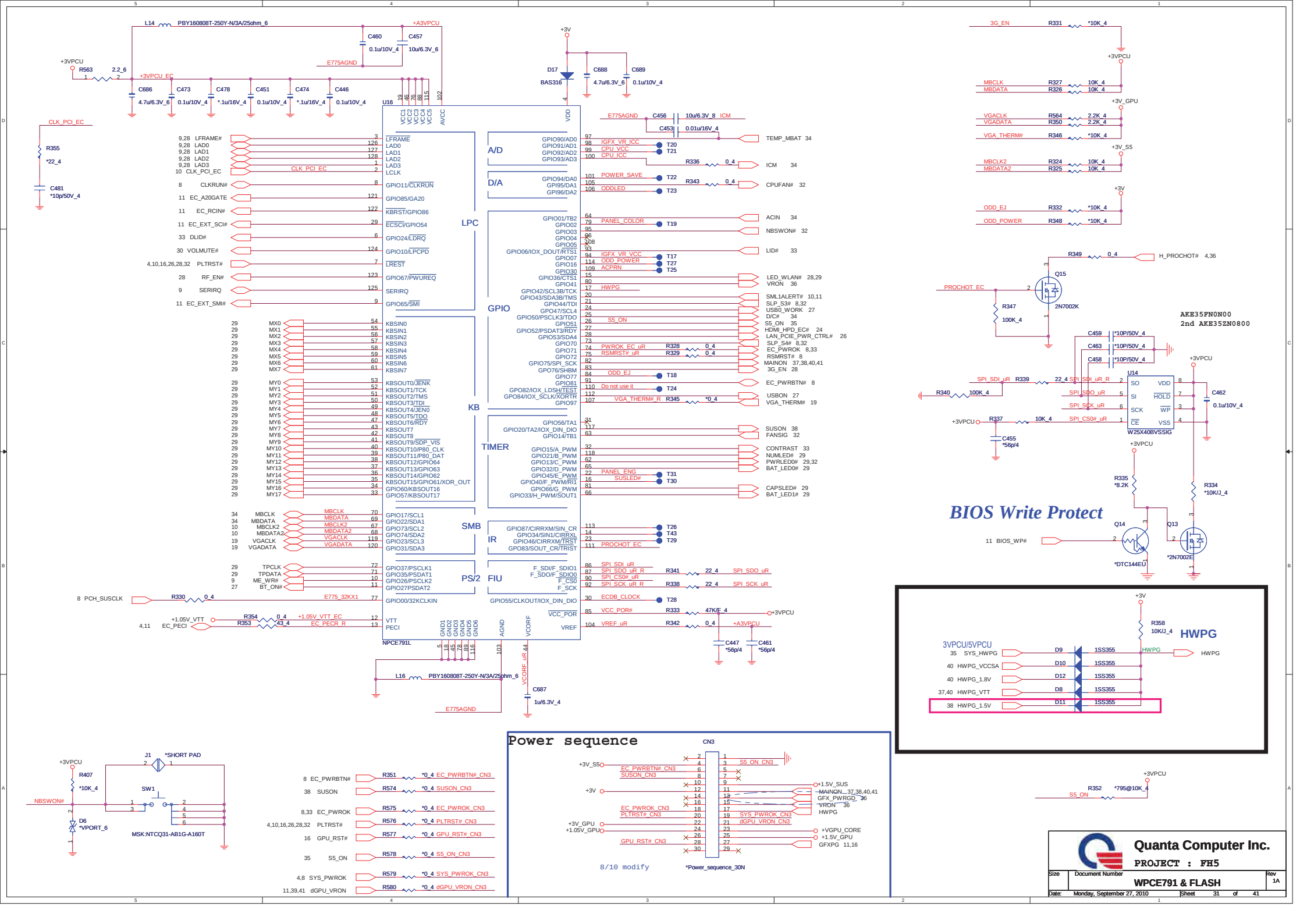
L14 PBY160808T-250Y-N/3A/25ohm_6
+A3VPCU
C460 0.1u/10V_4
C457 10u/6.3V_6
E775AGND
+3VPCU
R563 2.2_6
+3VPCU_EC
C686 4.7u/6.3V_6
C473 0.1u/10V_4
C478 *.1u/16V_4
C451 0.1u/10V_4
C474 *.1u/16V_4
C446 0.1u/10V_4
U16
VCC1 VCC2 VCC3 VCC4 VCC5 AVCC VDD
CLK_PCI_EC
R355 *22_4
C481 *10p/50V_4
9,28 LFRAME#
9,28 LAD0
9,28 LAD1
9,28 LAD2
9,28 LAD3
10 CLK_PCI_EC
8 CLKRUN#
11 EC_A20GATE
11 EC_RCIN#
11 EC_EXT_SCI#
33 DLID#
30 VOLMUTE#
4,10,16,26,28,32 PLTRST#
28 RF_EN#
9 SERIRQ
11 EC_EXT_SMI#
LPC
GPIO
KB
SMB
PS/2
A/D
D/A
FIU
IR
TIMER
MX0 MX1 MX2 MX3 MX4 MX5 MX6 MX7
MY0 MY1 MY2 MY3 MY4 MY5 MY6 MY7 MY8 MY9 MY10 MY11 MY12 MY13 MY14 MY15 MY16 MY17
MBCLK MBDATA MBCLK2 MBDATA2 VGACLK VGADATA
TPCLK TPDATA ME_WR# BT_ON#
8 PCH_SUSCLK
R330 0_4
E775_32KX1
+1.05V_VTT
4,11 EC_PECI
R354 0_4
R353 43_4
+1.05V_VTT_EC
EC_PECR_R
NPCE791L
GND1 GND2 GND3 GND4 GND5 GND6 AGND VCORF
L16 PBY160808T-250Y-N/3A/25ohm_6
VCORF_uR_44
C687 1u/6.3V_4
E775AGND
+3V
D17 BAS316
C688 4.7u/6.3V_6
C689 0.1u/10V_4
E775AGND C456 10u/6.3V_8_ICM
C453 0.01u/16V_4
TEMP_MBAT 34
IGFX_VR_ICC T20
CPU_VCC T21
CPU_ICC
R336 0_4
ICM 34
POWER_SAVE T22
R343 0_4
CPUFAN# 32
ODDLED T23
ACIN 34
PANEL_COLOR T19
NBSWON# 32
LID# 33
IGFX_VR_VCC T17
ODD_POWER T27
ACPRN T25
LED_WLAN# 28,29
VRON 36
HWPG
SML1ALERT# 10,11
SLP_S3# 8,32
USB0_WORK 27
D/C# 34
S5_ON
S5_ON 35
HDMI_HPD_EC# 24
LAN_PCIE_PWR_CTRL# 26
SLP_S4# 8,32
PWROK_EC_uR R328 0_4
EC_PWROK 8,33
RSMRST#_uR R329 0_4
RSMRST# 8
MAINON 37,38,40,41
3G_EN 28
ODD_EJ T18
EC_PWRBTN# 8
Do not use it T24
USBON 27
VGA_THERM# R345 *0_4
VGA_THERM# 19
SUSON 38
FANSIG 32
CONTRAST 33
NUMLED# 29
PWRLED0# 29,32
BAT_LED0# 29
PANEL_ENG T31
SUSLED# T30
CAPSLED# 29
BAT_LED1# 29
SPI_SDI_uR
SPI_SDO_uR R341 22_4 SPI_SDO_uR
SPI_CS0#_uR
SPI_SCK_uR_R R338 22_4 SPI_SCK_uR
ECDB_CLOCK T28
VCC_POR# R333 47K/F_4 +3VPCU
VREF_uR R342 0_4 +A3VPCU
PROCHOT_EC T26 T43 T29
C447 *56p/4
C461 *56p/4
3G_EN R331 *10K_4
+3VPCU
MBCLK R327 10K_4
MBDATA R326 10K_4
+3V_GPU
VGACLK R564 2.2K_4
VGADATA R350 2.2K_4
VGA_THERM# R346 *10K_4
+3V_S5
MBCLK2 R324 10K_4
MBDATA2 R325 10K_4
+3V
ODD_EJ R332 *10K_4
ODD_POWER R348 *10K_4
R349 0_4 H_PROCHOT# 4,36
Q15 2N7002K
PROCHOT_EC
R347 100K_4
AKE35FN0N00
2nd AKE35ZN0800
C459 *10P/50V_4
C463 *10P/50V_4
C458 *10P/50V_4
U14
SPI_SDI_uR R339 22_4 SPI_SDI_uR_R
SPI_SDO_uR
SPI_SCK_uR
SPI_CS0#_uR
R340 100K_4
R337 10K_4
C455 *56p/4
SO SI SCK CE VDD HOLD WP VSS
W25X40BVSSIG
C462 0.1u/10V_4
BIOS Write Protect
11 BIOS_WP#
Q14 Q13 *2N7002E
*DTC144EU
R335 *8.2K
R334 *10K/J_4
+3V
R358 10K/J_4
HWPG
3VPCU/5VPCU
35 SYS_HWPG
40 HWPG_VCCSA
40 HWPG_1.8V
37,40 HWPG_VTT
38 HWPG_1.5V
D9 D10 D12 D8 D11
1SS355
HWPG
J1 *SHORT PAD
R407 *10K_4
NBSWON#
SW1
D6 *VPORT_6
MSK:NTCQ31-AB1G-A160T
8 EC_PWRBTN#
38 SUSON
8,33 EC_PWROK
4,10,16,26,28,32 PLTRST#
16 GPU_RST#
35 S5_ON
4,8 SYS_PWROK
11,39,41 dGPU_VRON
R351 *0_4 EC_PWRBTN#_CN3
R574 *0_4 SUSON_CN3
R575 *0_4 EC_PWROK_CN3
R576 *0_4 PLTRST#_CN3
R577 *0_4 GPU_RST#_CN3
R578 *0_4 S5_ON_CN3
R579 *0_4 SYS_PWROK_CN3
R580 *0_4 dGPU_VRON_CN3
Power sequence
CN3
+3V_S5
EC_PWRBTN#_CN3
SUSON_CN3
+3V
EC_PWROK_CN3
PLTRST#_CN3
+3V_GPU
+1.05V_GPU
GPU_RST#_CN3
S5_ON_CN3
+1.5V_SUS
MAINON 37,38,40,41
GFX_PWRGD 36
VRON 36
HWPG
SYS_PWROK_CN3
dGPU_VRON_CN3
+VGPU_CORE
+1.5V_GPU
GFXPG 11,16
8/10 modify
*Power_sequence_30N
+3VPCU
R352 *795@10K_4
S5_ON
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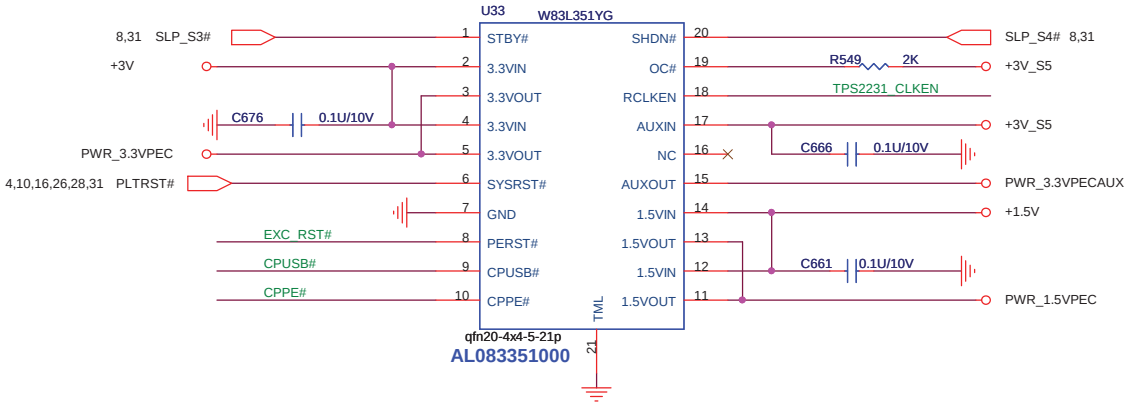
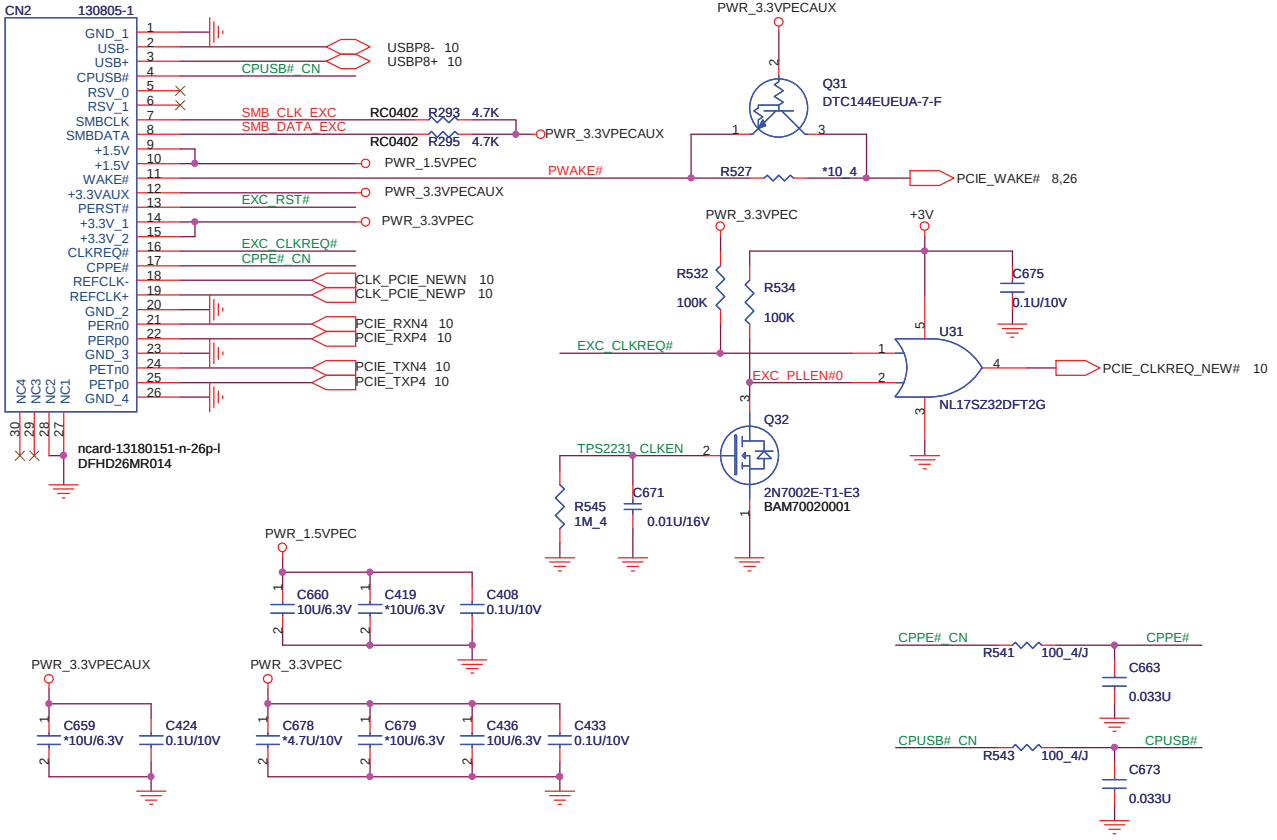
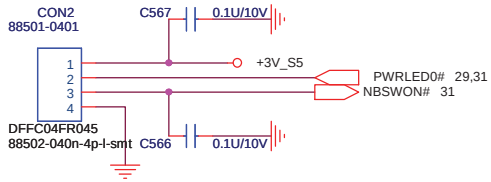
NEW CARD

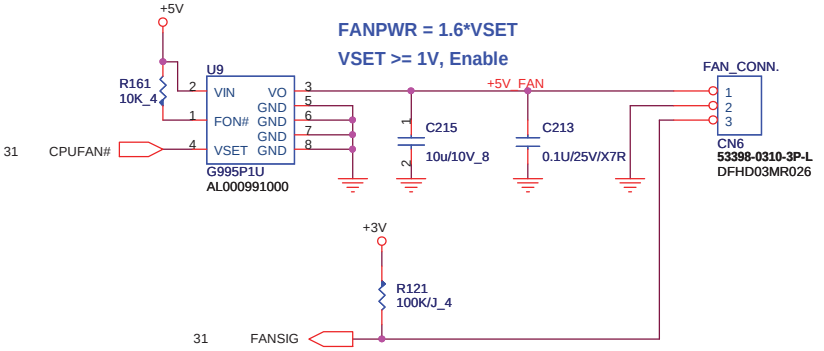




PW BOARD CON



CPU FAN CTRL



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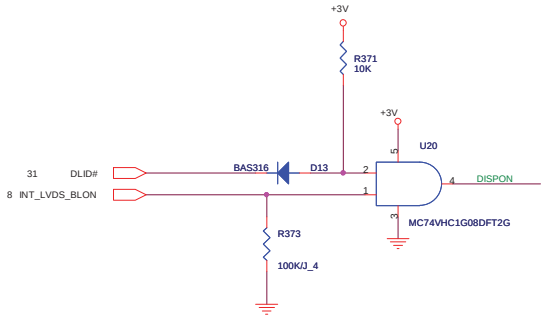
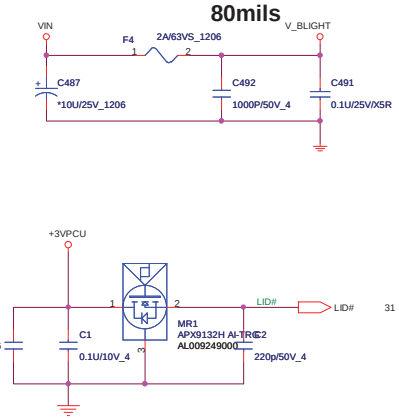
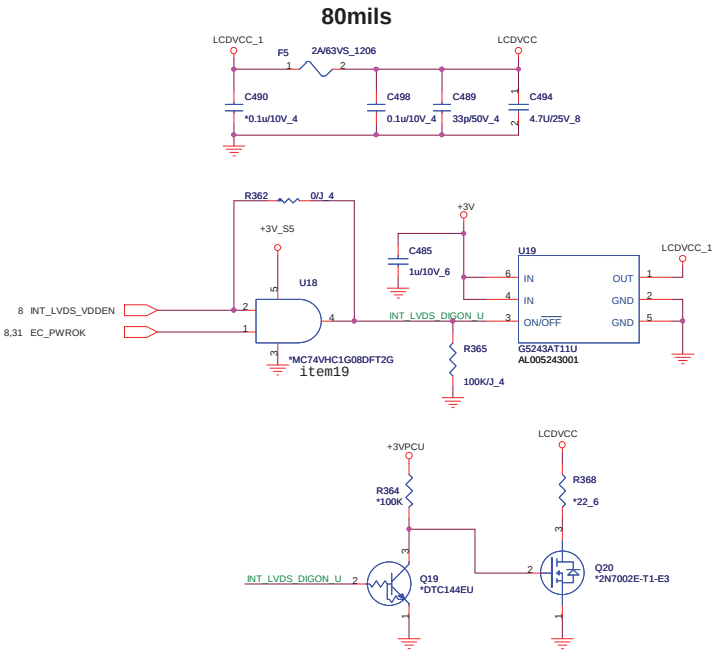
BACKLIGHT Control(LVDS)



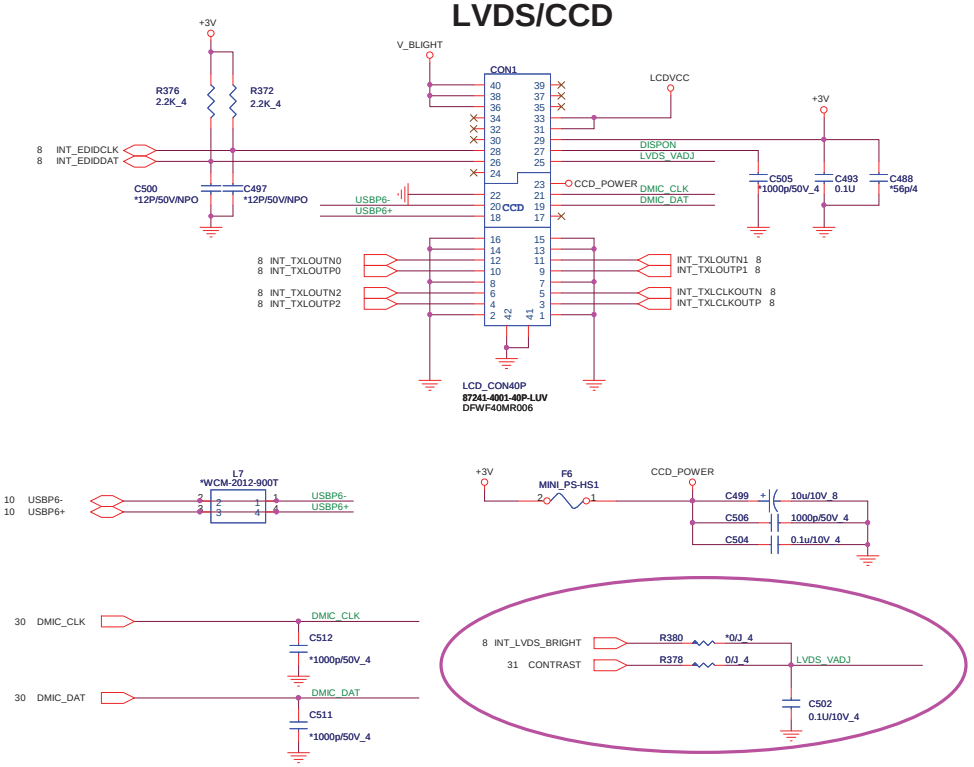
BACKLIGHT POWER

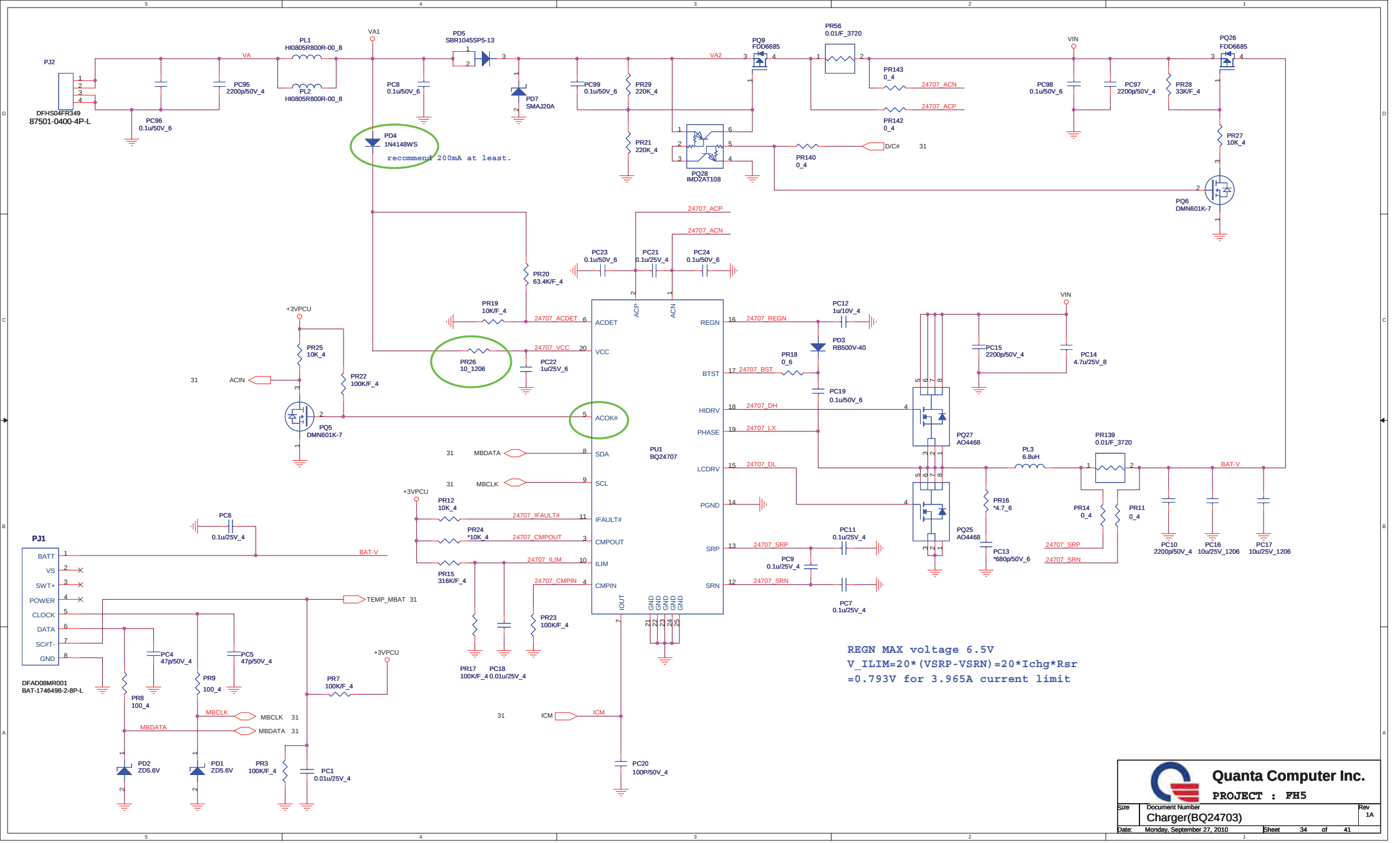


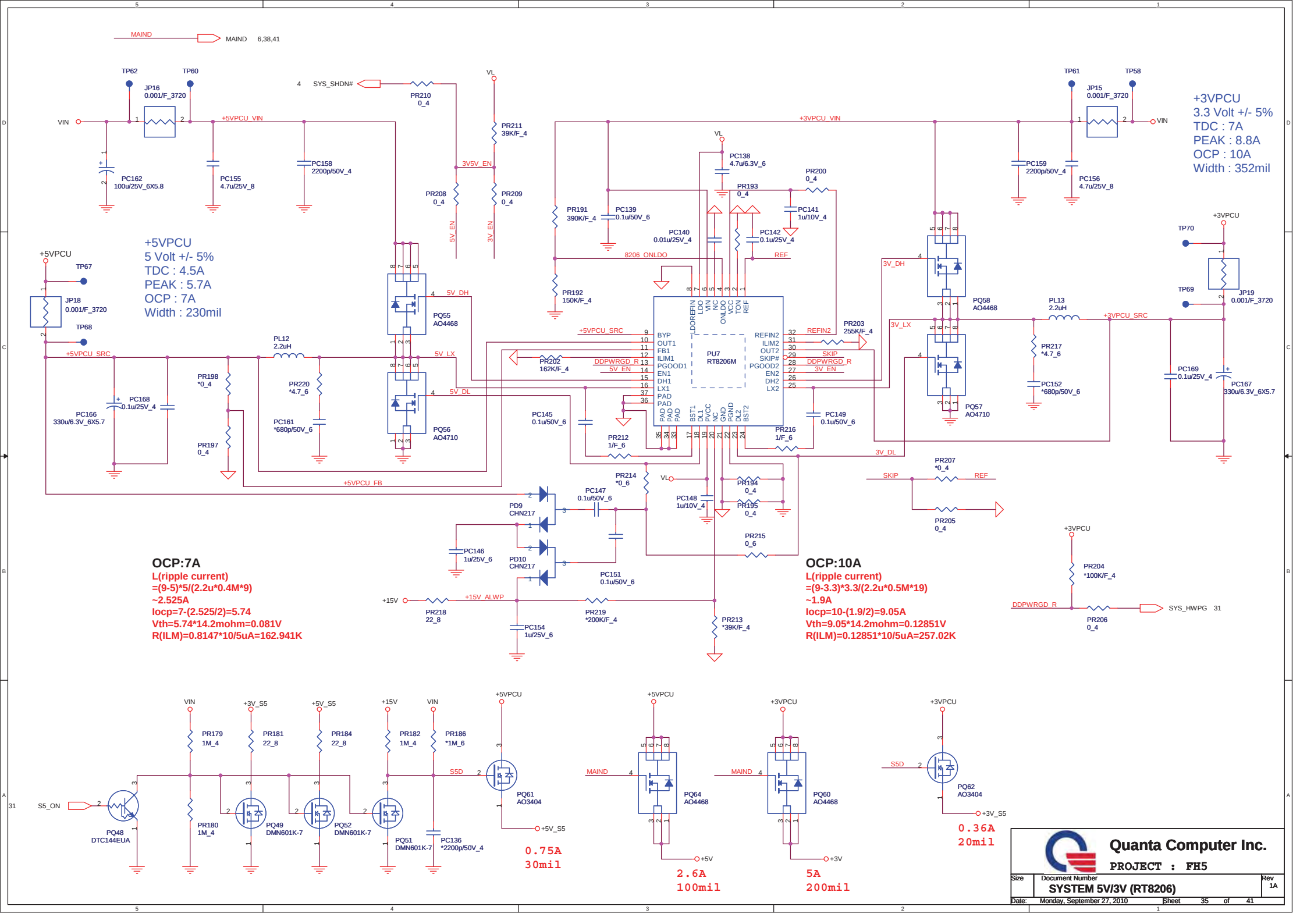
LED Panel POWER SWITCH(LVDS)



LVDS/CCD






MAIND
MAIND 6,38,41
+5VPCU
5 Volt +/- 5%
TDC : 4.5A
PEAK : 5.7A
OCP : 7A
Width : 230mil
+3VPCU
3.3 Volt +/- 5%
TDC : 7A
PEAK : 8.8A
OCP : 10A
Width : 352mil
PU7
RT8206M
8206_ONLDO
+5VPCU_VIN
+3VPCU_VIN
+5VPCU_SRC
+3VPCU_SRC
+5VPCU_FB
SYS_SHDN#
3V5V_EN
5V_EN
3V_EN
DDPWRGD_R
REFIN2
SKIP
REF
5V_DH
5V_LX
5V_DL
3V_DH
3V_LX
3V_DL
+15V_ALWP
SYS_HWPG 31
OCP:7A
L(ripple current)
=(9-5)*5/(2.2u*0.4M*9)
~2.525A
Iocp=7-(2.525/2)=5.74
Vth=5.74*14.2mohm=0.081V
R(ILM)=0.8147*10/5uA=162.941K
OCP:10A
L(ripple current)
=(9-3.3)*3.3/(2.2u*0.5M*19)
~1.9A
Iocp=10-(1.9/2)=9.05A
Vth=9.05*14.2mohm=0.12851V
R(ILM)=0.12851*10/5uA=257.02K
0.75A
30mil
2.6A
100mil
5A
200mil
0.36A
20mil
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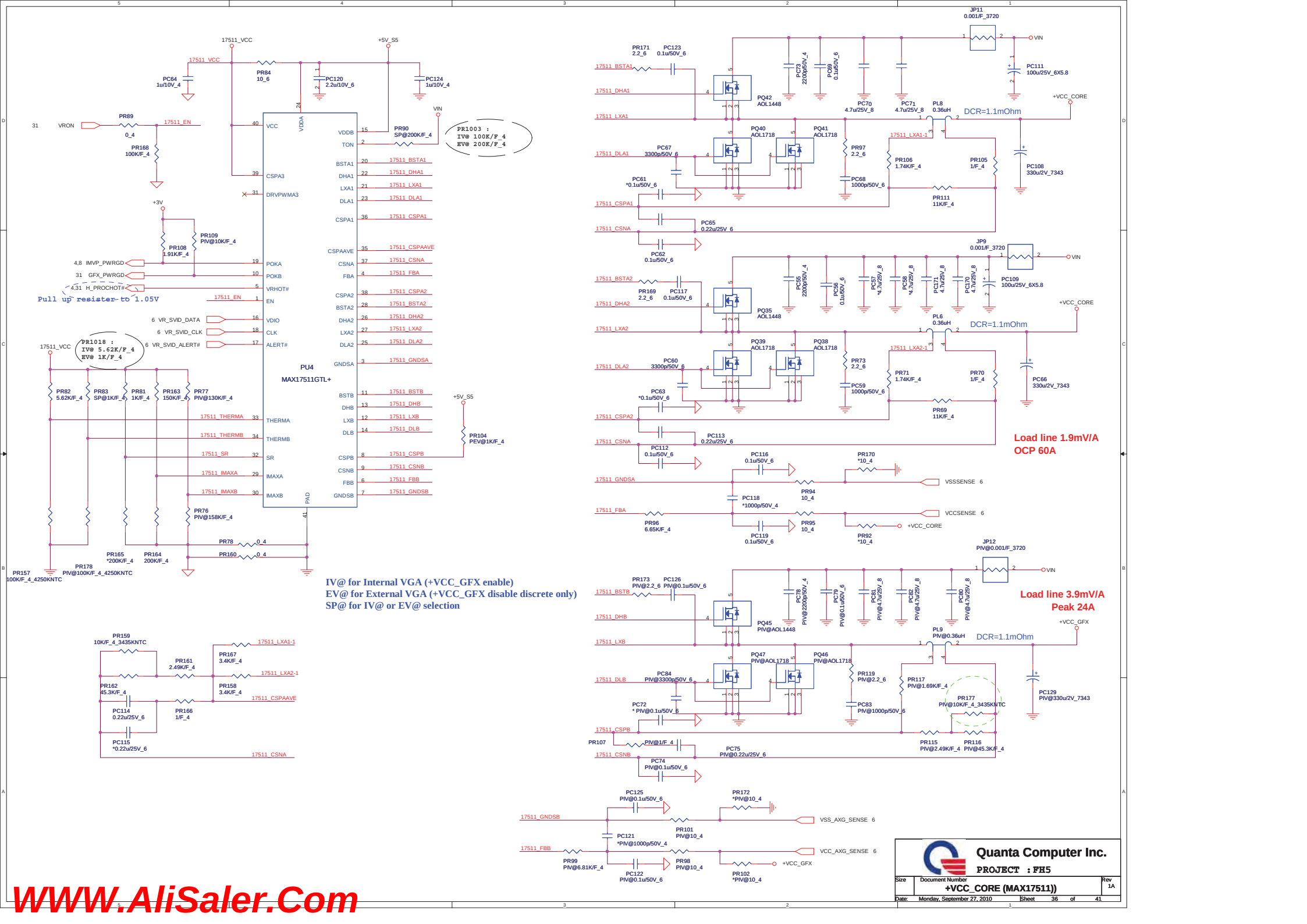

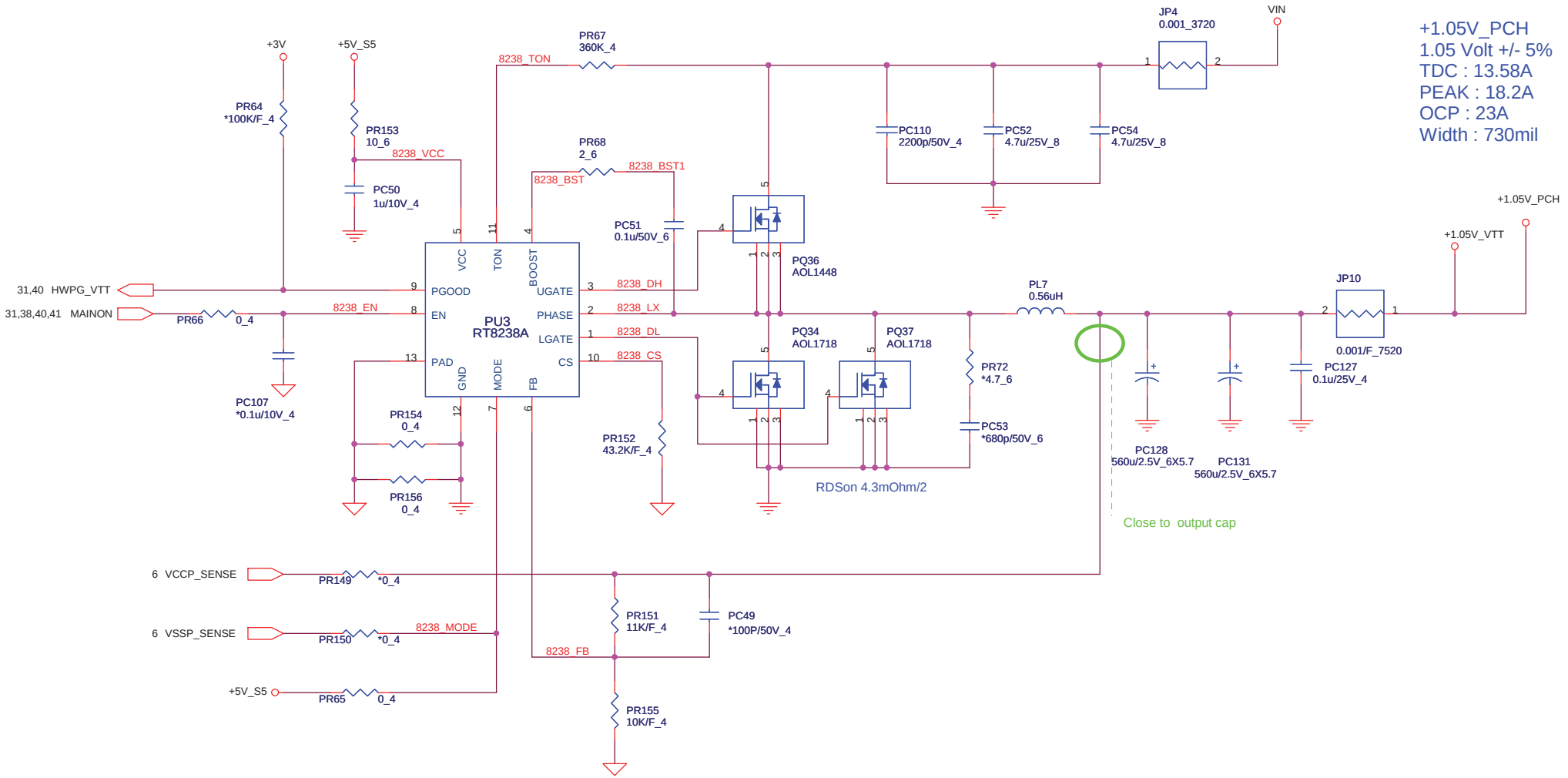
+1.05V_PCH
1.05 Volt +/- 5%
TDC : 13.58A
PEAK : 18.2A
OCP : 23A
Width : 730mil
JP4
0.001_3720
VIN
+3V
+5V_S5
PR64
*100K/F_4
PR153
10_6
8238_VCC
PC50
1u/10V_4
PR67
360K_4
8238_TON
PR68
2_6
8238_BST
8238_BST1
PC51
0.1u/50V_6
PC110
2200p/50V_4
PC52
4.7u/25V_8
PC54
4.7u/25V_8
PU3
RT8238A
VCC
TON
BOOST
PGOOD
UGATE
EN
PHASE
PAD
LGATE
GND
MODE
FB
CS
31,40 HWPG_VTT
31,38,40,41 MAINON
PR66
0_4
8238_EN
8238_DH
8238_LX
8238_DL
8238_CS
PQ36
AOL1448
PQ34
AOL1718
PQ37
AOL1718
PL7
0.56uH
PR72
*4.7_6
PC53
*680p/50V_6
PC107
*0.1u/10V_4
PR154
0_4
PR156
0_4
PR152
43.2K/F_4
RDSon 4.3mOhm/2
Close to output cap
PC128
560u/2.5V_6X5.7
PC131
560u/2.5V_6X5.7
JP10
0.001/F_7520
PC127
0.1u/25V_4
+1.05V_VTT
+1.05V_PCH
6 VCCP_SENSE
PR149
*0_4
6 VSSP_SENSE
PR150
*0_4
8238_MODE
+5V_S5
PR65
0_4
PR151
11K/F_4
PC49
*100P/50V_4
8238_FB
PR155
10K/F_4
Current limit =10uA*Rth/RDSon
VOUT=(1+R1/R2)*0.5
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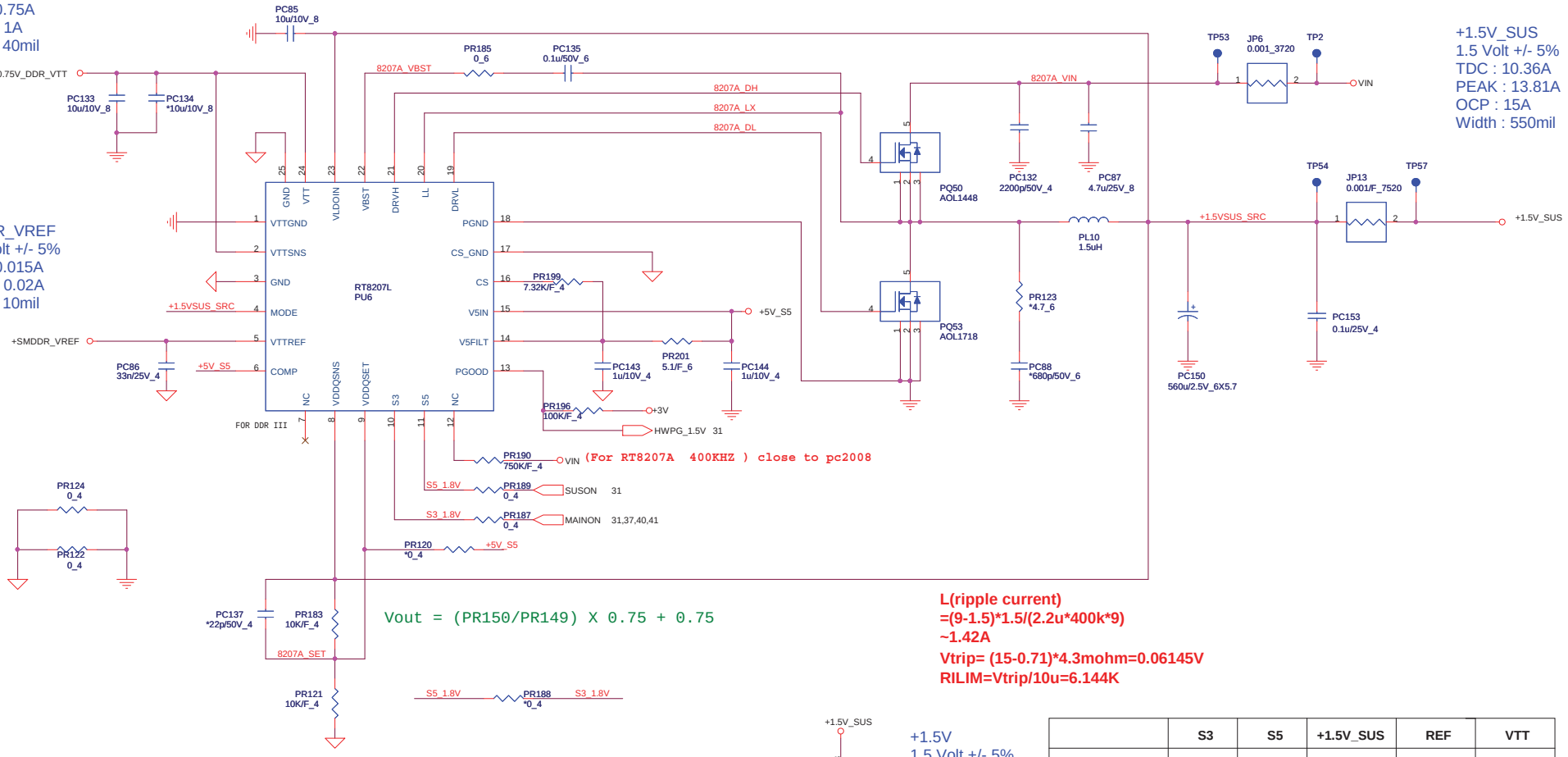
[PWM]

+0.75V_DDR_VTT
0.75 Volt +/- 5%
TDC : 0.75A
PEAK : 1A
Width : 40mil

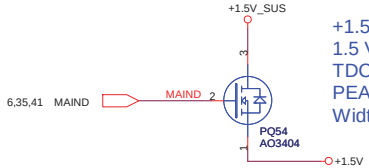
SMDDR_VREF
0.75 Volt +/- 5%
TDC : 0.015A
PEAK : 0.02A
Width : 10mil



Vout = (PR150/PR149) X 0.75 + 0.75

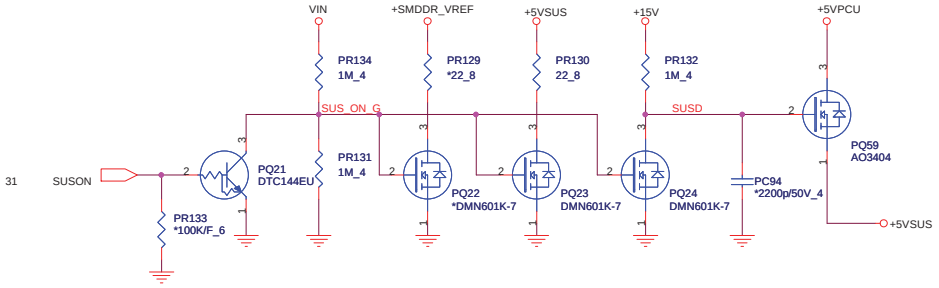
L(ripple current)
=(9-1.5)*1.5/(2.2u*400k*9)
~1.42A
Vtrip= (15-0.71)*4.3mohm=0.06145V
RILIM=Vtrip/10u=6.144K

+1.5V_SUS
1.5 Volt +/- 5%
TDC : 10.36A
PEAK : 13.81A
OCP : 15A
Width : 550mil



+1.5V
1.5 Volt +/- 5%
TDC : 0.5A
PEAK : 0.65A
Width : 25mil

	S3	S5	+1.5V_SUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF



TDC : 1.125A
PEAK : 1.5A
Width : 60mil

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	DDR 1.5V(TPS51116)	1A
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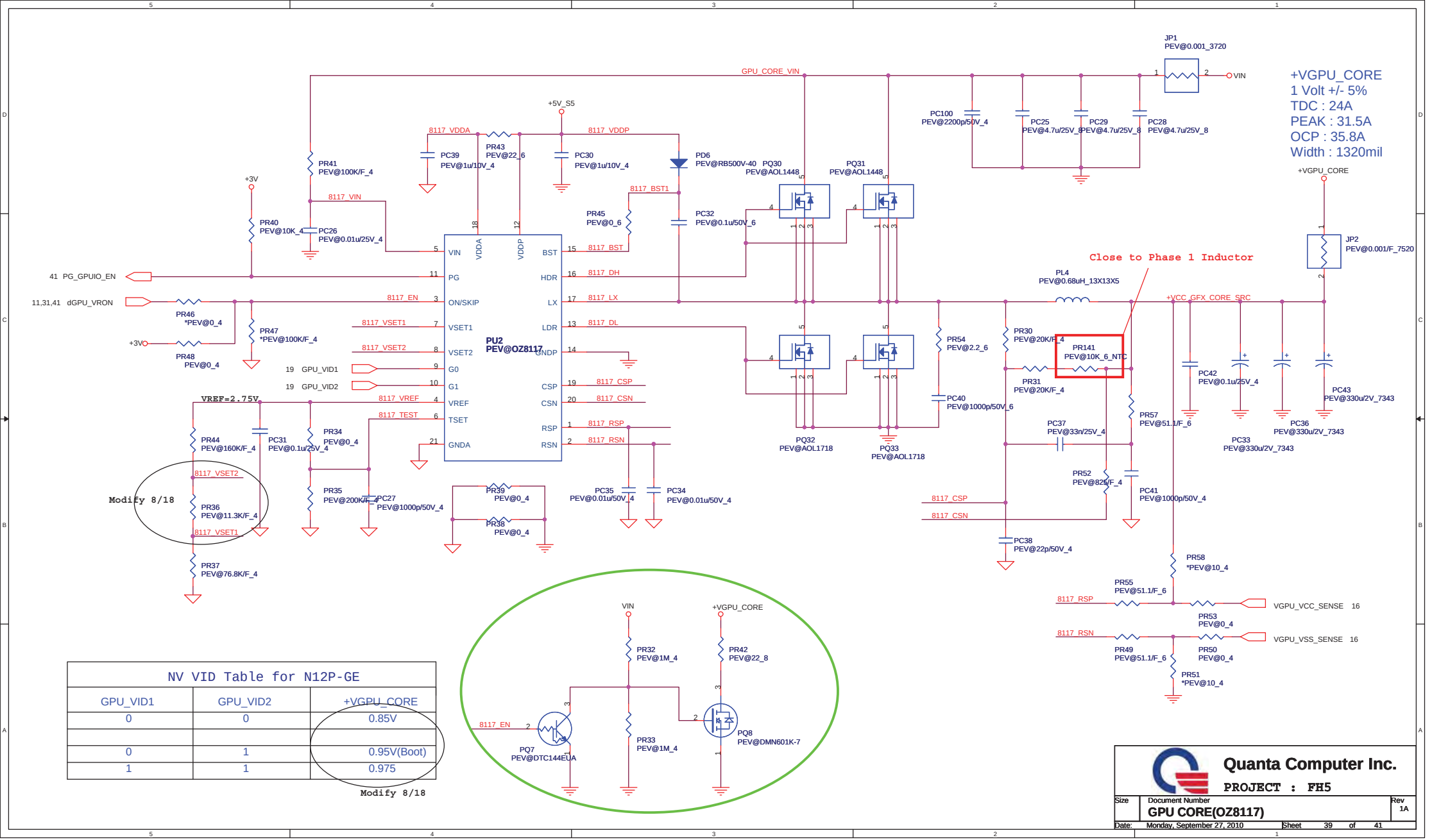

NV VID Table for N12P-GE

GPU_VID1	GPU_VID2	+VGPU_CORE
0	0	0.85V
0	1	0.95V(Boot)
1	1	0.975

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	GPU CORE(OZ8117)	1A

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VID0	VID1	VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

VCCSA
0.9 Volt +/- 5%
TDC : 4.2A
PEAK : 6A
Width : 240mil

JP3 0.001/F_3720 +3V
PC44 0.1u/25V_4
PC101 10u/10V_8
PC102 10u/10V_8
+5V_S5
PC103 2.2u/10V_6
51461_DRV
PR59 0_6
PC104 1u/10V_4
51461_FILT
+3V
PR144 100K/F_4
31 HWPG_VCCSA
31,37 HWPG_VTT
PR147 0_4
PC46 *0.1u/25V_4
6 VCCSA_SEL
51461_EN
PR145 1K_4
TPS51461 PU5
VIN VIN VIN PGND PGND PGND
V5DRV V5FILT PGOOD EN VID0 VID1
BST SW SW SW SW SW Pad
MODE GND VREF COMP SLEW VOUT
PC48 0.1u/50V_6
51461_BST
51461_SW
PL5 1uH_7X7X3
VCCSA
JP8 0.001/F_3720
PC106 0.1u/25V_4
PR148 100_4
PC105 560u/2.5V_6X5.7
51461_VOUT
VCCSA_SENSE 6
PR146 0_4
PR63 *0_4
PC45 0.22u/25V_6
PR62 7.15K/F_4
PC47 0.01u/25V_4
51461_MODE
51461_VREF
51461_COMP
51461_SLEW
PR60 0_4
PR61 0_4

VCCSA_SEL	VCCSA
1	0.8V
0	0.9V

default 0.9V

+1.8V
1.8 Volt +/- 5%
TDC : 1.34A
PEAK : 1.78A
Width : 71mil

+3VPCU
TP1 TP66
JP17 0.001_3720
PC165 10u/10V_8
PC93 0.1u/10V_4
PU8 TPS51117RGYR-GP_4
VIN VIN VIN EN VSNS COMP RT/CLK SS
PH PH PH BOOT PWRGD GND GND AGND
835_PH
835_EN
54418-1.8_VFB
835_COMP
835_RTCLK
835_SS
PR224 0_4
MAINON
PR127 *100K/F_4
PC91 1000p/50V_4
PR222 8.06K/F_4
PC92 *100P/50V_4
PR125 182K/F_4
PC90 0.01u/25V_4
PC164 2700p/50V_4
PR221 0_6
PC163 0.1u/50V_6
PL11 1uH_7X7X3
+1.8V
TP26
JP14 0.001_3720
TP59
R1
PR126 100K/F_4
PC160 0.1u/10V_4
PC89 10u/10V_8
PC157 10u/10V_8
HWPG_1.8V 31
PR223 100K/F_4
+3V
R2
PR128 78.7K/F_4
V0=0.8*(R1+R2)/R2
MAINON 31,37,38,41

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	VCCSA(TPS51461)/+1.8V(HPA00835)	1A
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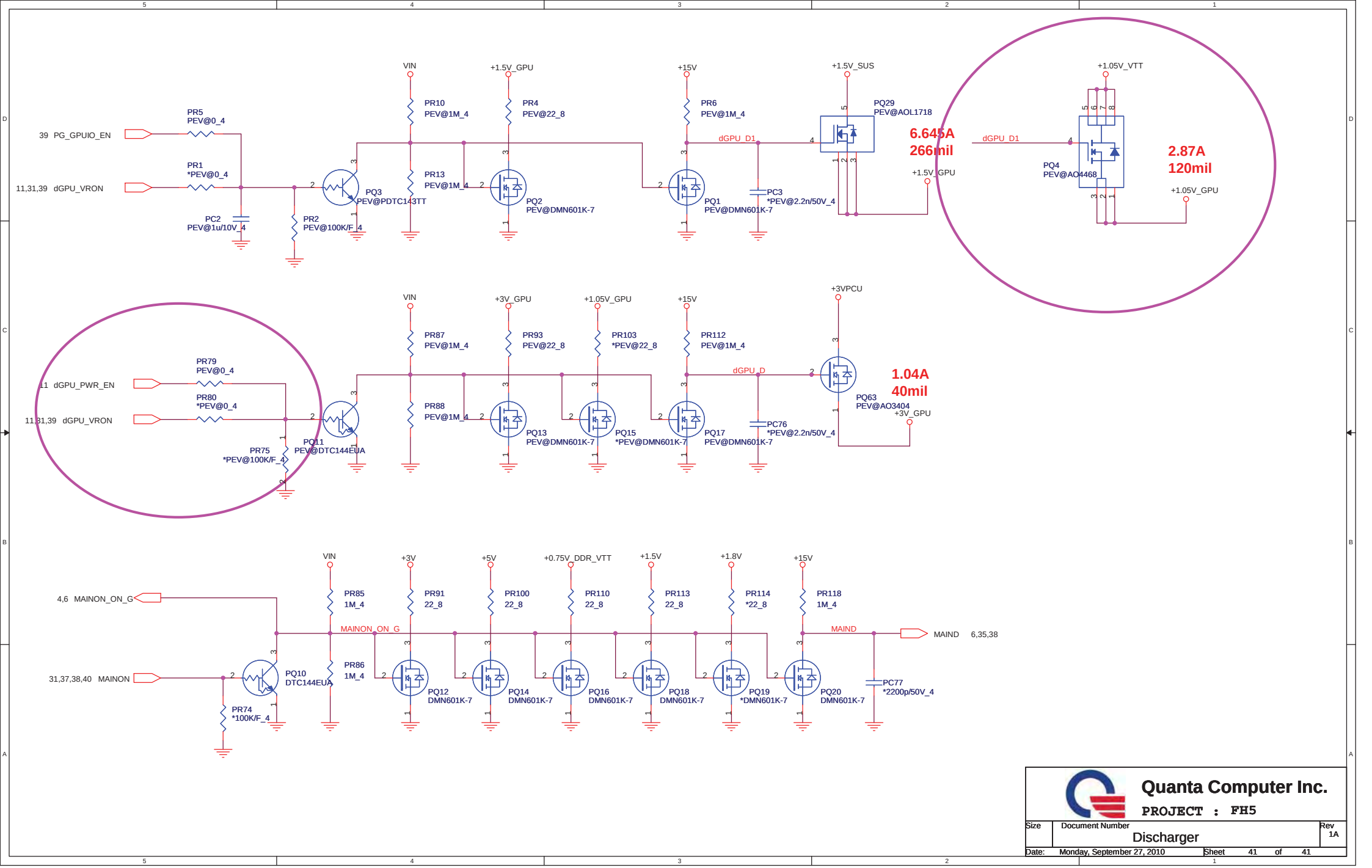

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	Discharger	1A
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Model

FH5 MB

CHANGE LIST

REV	
B	page 33: Change +VIN to VIN. 2010/09/20 page 30 : Del Q16 ,R351. page 10 : Add Q27 and Q28. page 26 : Change CON6 RJ45 Conn to DFTJ08FR157.
	2010/09/22 page 10: Change USB port6 ot port10.
	2010/09/22 page 31 : Del CN3 Netname ,NBSWON#, SLP_S3# ,+VCC_GFX,+VCC_CORE,H_PWRGOOD, RSMRST#, SLP_S4# ,SUS_STAT#. page 31 : Reserve R351 ,R574-R580 for Power sequence resistor. page 31 : Reserve C692 for H_PWRGOOD. page 9: Change JTAG VCC +3VPCU to +3V_S5.
	2010/09/23 page 31 : Change CON2 VCC from +3V to +3V_S5. page 12 : Reserve C693,C694,C695,C696 for ESD. Page36 : PC61、PC63 change value from *1000p/50V_4 (CH21006JB10) to *0.1u/50V_6 (CH41006K911) Page36 : PC62、PC112、PC116、PC119 change value from 1000p/50V_4 (CH21006JB10) to 0.1u/50V_6 (CH41006K911) Page36 : PC72 change value from *PIV@1000p/50V_4 (CH21006JB10) to * PIV@0.1u/50V_6 (CH41006K911) Page36 : PC74、PC122、PC125 change value from PIV@1000p/50V_4 (CH21006JB10) to PIV@0.1u/50V_6 (CH41006K911) Page38 : PR190 changes value from 620K/F_4 (CS46202FB00) to 750K/F_4 (CS47502FB14) Page39 : PR44 changes value from PEV@169K/F_4 (CS41692FB12) to PEV@160K/F_4 (CS41602FB00) Page39 : PR36 changes value from PEV@21.5K/F_4 (CS32152FB17) to PEV@11.3K/F_4 (CS31132FB07) Page39 : PR37 changes value from PEV@82K/F_4 (CS38202FB14) to PEV@76.8K/F_4 (CS37682FB00) page36 :PL6、PL8、PL9 change footprint from CHOKE-ETQP4LR36WFC-4P-SMT to CHOKE-PCMB104T-R45MN-4P-SMT page06 Reserve C697,C698,C699 for VID.
	2010/09/24 page06 Del R28 , add R21,C19,C20,Y2 , use cystal to provide 25M CLK. page36 Del PC57,PC58 ,ADD PC170,171,PC78,PC73,PC55 for C state issue. page38 CHange PR199 to 7.32K_4(CS27322FB12), change 1.5V_SUS OCP value.
	2010/09/27 Page39 : PL4 change P/B from CV+68^0MZ00 to DC+68Z0M001 Page24 : C4,C5,C6,C7,C8,C9 change from2.2P/50V_4 to 10P/50V_4(CH01006JB08). page 27 : Change U34 Ctrl 1 ~3 behavior,add R554 , R581,del R582.
3C	

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	Change list	1A

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DOC NO.					
PROJECT MODEL :	FH5	APPROVED BY:		DATE:	2010/09/20
PART NUMBER:		DRAWING BY:		REVISON:	1A