

J361Y-SB Rev_V3.06(06/16/2005)

91.3H801.001

Sheet

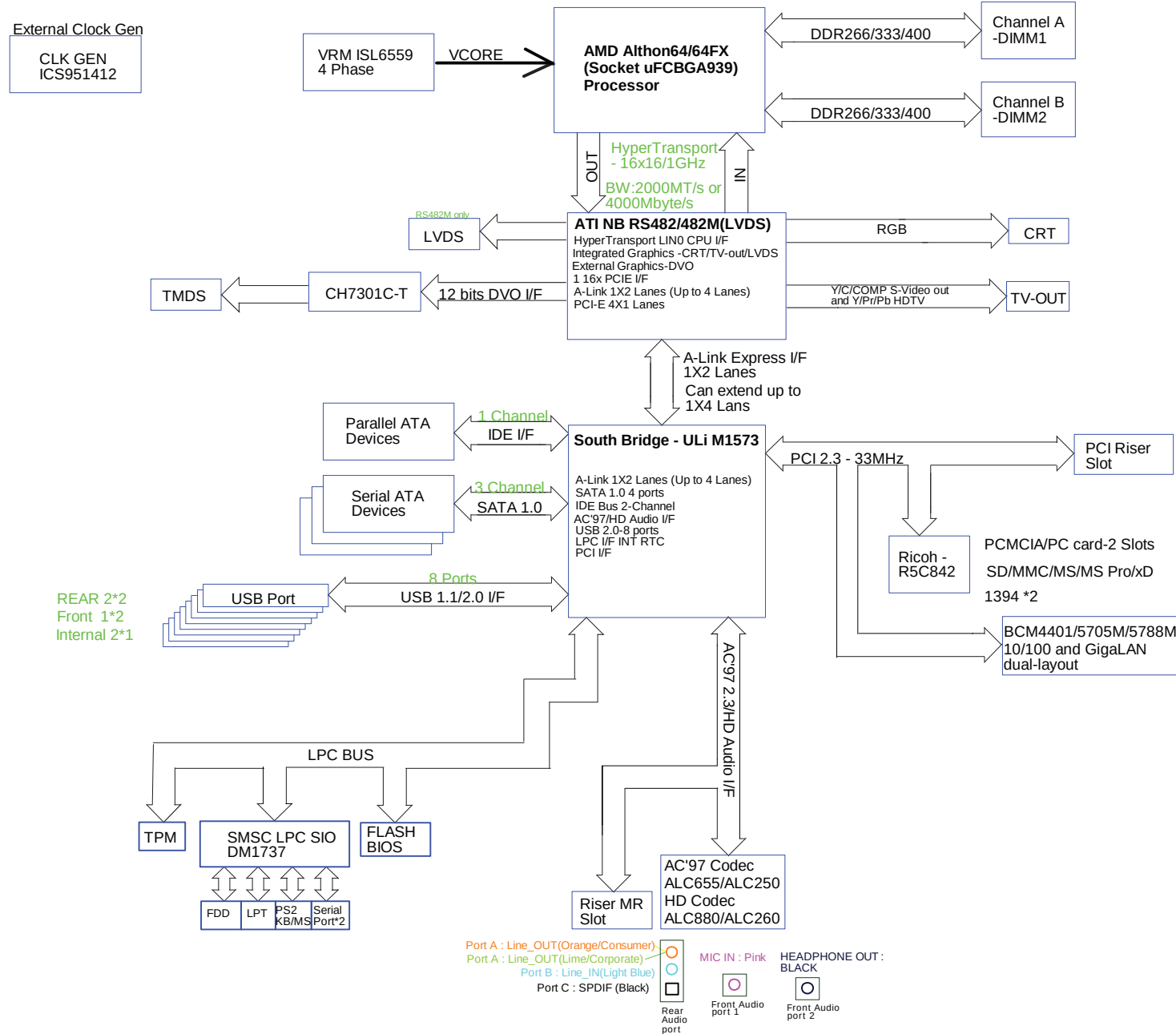
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Sheet 25	IDE and SATA CONN

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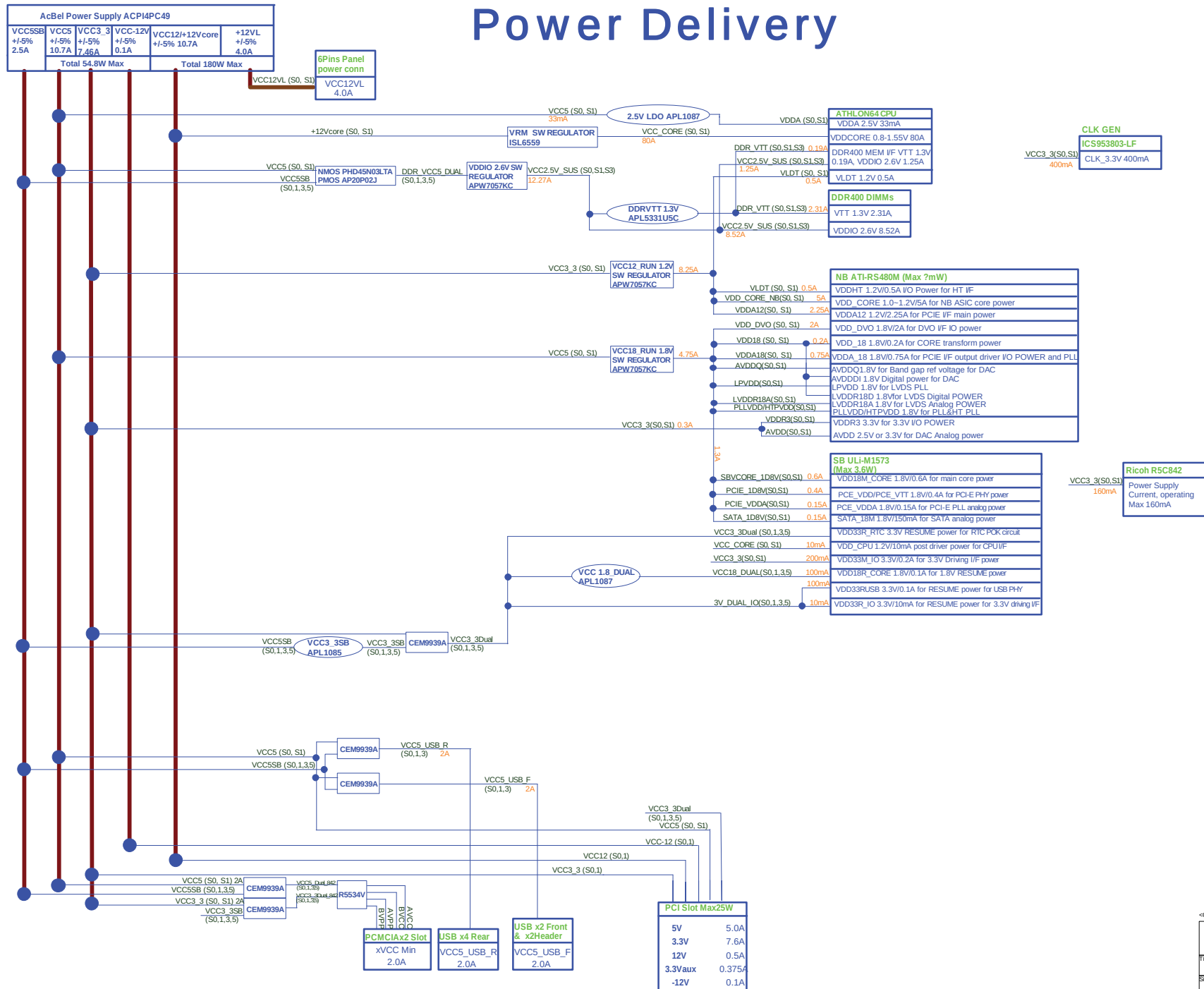
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Sheet 28	SIO DM1737 & FDD Conn
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Sheet 33	R5C842-MDIO I/F and CB I/F
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Sheet 35	MS/SD/xD CARD Conn
Sheet 36	PCI Riser Slot
Sheet 37	LAN
Sheet 38	AUDIO CODEC
Sheet 39	AUDIO CONN
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Sheet 45	VCC18_RUN & VCC12_RUN
Sheet 46	VCC_Core(ISL6559)
Sheet 47	PWR Sequence controller
Sheet 48	ATX 24Pin conn
Sheet 49	Screw Hole
Sheet 50	CLK MAP

		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
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Block Diagram



Power Delivery



PME event output

PCI

Device	IDSEL	GNTJ/REQJ	IRQ	Active Status
R5C842	AD21	PREQJ3PGNTJ3	PIRQJD,A,B,C	LOW
PCI RISER	AD19 AD20	PREQJ0PGNTJ0 PREQJ1PGNTJ1	PIRQJAB,C,D PIRQJB,C,D,A	LOW
PCI LAN	AD22	PREQJ4PGNTJ4	PIRQJE	LOW

SMSC DM1737

GPIO #	Mux Function	GPIO Function	I/O	POWER	Active Status
GP10	RST_IDE*		0	MAIN (VCC)	Low
GP11	PCIRST_OUT1	LAN_DISJ	0	AUX (VTR)	Low/Default high
GP12			0	AUX (VTR)	
GP13		SLP_S1_S5_L*	0	AUX (VTR)	Low@S0/ S1/ S3 / High@S4/ S5
GP14	PCIRST_OUT4	SUSLED*	0	AUX (VTR)	Low
GP21	KBDATA		I	MAIN (VCC)	
GP22	KBCLK		I	MAIN (VCC)	
GP27			I	MAIN (VCC)	
GP32	MSDATA		I	MAIN (VCC)	
GP33	MSCLK		I	MAIN (VCC)	
GP36	KBRST*		I	MAIN (VCC)	Low
GP37	A20GATE		I	MAIN (VCC)	
GP40			0	MAIN (VCC)	
GP42	IO_PMES3#		0	AUX (VTR)	PME event output
GP43	IO_PMES5#		0	AUX (VTR)	PME event output
GP50	RI*2		I	MAIN (VCC)	
GP51	DCD*2		I	MAIN (VCC)	
GP52	RXD2		I	MAIN (VCC)	
GP53	TXD2		I	MAIN (VCC)	
GP54	DSR*2		I	MAIN (VCC)	
GP55	RTS*2		I	MAIN (VCC)	
GP56	CTS*2		I	MAIN (VCC)	
GP57	DTR*2		I	MAIN (VCC)	
GP60		TVLED*	0	AUX (VTR)	High / push-pull
GP61		LCDONJ_SIO	0	AUX (VTR)	Low/ S5 wake up event

ATI RS482/482M

GPIO #	Mux Function	GPIO Function	I/O	POWER	Active Status
DFT_GPIO0			I	VDDR3	
DFT_GPIO1	LOAD_ROM_STRAPS#		I	VDDR3	Low
DFT_GPIO2		TV_SWITCH	0	VDDR3	1:0-Video
DFT_GPIO3		D_PLUGDET	I	VDDR3	0:SDV/Video connected 1: HDTV_unconnected
DFT_GPIO4			I	VDDR3	
DFT_GPIO5	LOAD_MEM_STRAPS#		I	VDDR3	Low

ULi M1573

GPIO #	Mux Function	GPIO Function	I/O	POWER	Active Status
RUNGPI00		IDE_P	I	VDD33M_IO	High
RUNGPI01			0	VDD33M_IO	LOW
RUNGPI02				VDD33M_IO	
RUNGPI03		MO_DET	I	VDD33M_IO	0: M0 connected 1: M0 unconnected
RUNGPI18	ACB_BITCLK	BOARD_ID_0	I	VDD33M_IO	
RUNGPI11	VOL_UP#	BOARD_ID_1	I	VDD33M_IO	
RUNGPI12	VOL_DOWN#	BOARD_ID_2	I	VDD33M_IO	
RUNGPI13	VOL_MUTE#	BOARD_ID_3	I	VDD33M_IO	
RUNGPI9	CLKRUN#	CRT_TMDS_DISJ	0	VDD33M_IO	HIGH
RUNGPO[13]	CPUHI#	Blueled*	0	VDD33M_IO	HIGH
RUNGPO[16]	IGNNE#	Blueled02*	0	VDD33M_IO	HIGH
RUNGPO[19]	NMI	HDDLED	0	VDD33M_IO	HIGH
RUNGPO[21]	SMI#	Blueled03*	0	VDD33M_IO	HIGH
SATA_GPIO		LCD_VID0	I	VDD33M_IO	
SATA_GPI1		LCD_VID1	I	VDD33M_IO	
SATA_GPI2		LCD_VID2	I	VDD33M_IO	
SATA_GPI3			I	VDD33M_IO	
SATA_GP00			0	VDD33M_IO	LOW
SATA_GP01		FlashROM_WP	0	VDD33M_IO	High/Default LOW
SATA_GP02			0	VDD33M_IO	LOW
SATA_GP03		PWRLED*	0	VDD33M_IO	LOW
RSMGPI00		USBPWR_Ctrl	0	VDD33R_IO	Consumer: S3->H, S4/S5->L Corporate: S3/S4->H, S5->L
RSMGPI01		ACPILED*	0	VDD33R_IO	HIGH
RSMGPI02		ACPI_S3	0	VDD33R_IO	S3:High
RSMGPI03		842HWSPNDJ	0	VDD33R_IO	High
RSMGPI10	SMBALERT#	IO_PMES3#	I	VDD33R_IO	PME event input
RSMGPI1[0]	SLPBTN#	IO_PMES5#	I	VDD33R_IO	PME event input

<Core Design>

		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title GPIO Table			
Size Custom	Document Number J361Y RS482+M1573		Rev 1A
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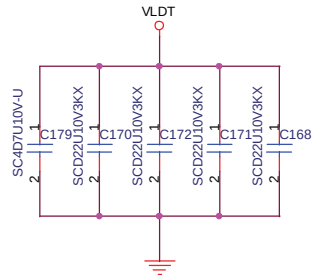
Rev. Notes

DATE	Rev	Description	Page
3/10	SA_V1.0	Release Schematic	
	SA_V1.1	Add Board_ID [3..0] setting	22
		Add PIRQ[EH] pull high	36
		Add CN41	28
		HW strapping setting	13,21,22,23
		Modify Front HP OUT Mute circuit	39
		Two copper pure for VTT fill - at least 100mils wide/Change DDR_VTT_CPU as DDR_VTT	7,8
		Modify Net REFCLK0_1 and REFCLK0_2	24
3/14		Connect ASIC8M_CPU_RST to LDTREST#	47
		Change R92 to 2.4k ohm	17
		Modify DVO_IDCKN and DVO_IDCKP	17
		Modify TMDs HotPlug circuit	17
		Modify TV-out I2C circuit	18
3/15		Modify VDD_DVO power for RS482 revA11	15
		Modify DVO_VREF circuit	17
3/15	SA_V1.2	Change L33	22
		Modify VRM Circuit (Vendor suggestion)	46
		Change M1573 HW strapping resistors to 1K ohm	21
		Change R536 and R538 to 1K ohm and change R554 to 5.1K (Vendor suggestion)	46
		Modify SB4NB POWER Good circuit	47
3/16	SA_V1.3	Modify DLINE circuit	18
		Modify TMDs Hot plug circuit	15
3/16	SA_V1.4	Move R664 and R697 to Page17. Delete R665 and R666	13,17,19
		Delete R669 and R670	18
		Delete TC86	32
		Modify DLINE circuit	18
		Change M1573 to RevA1D	20-23
		Add LAN Disable circuit	37
3/19	SA_V1.5	Delete TC39 for Extra 4 CPU FANSINK screw hole	46
		Change C763 to a small size	40
		Modify FJ's checklist items	
3/21	SA_V1.6	SWAP USB Port	26
	SA_V1.7	SMBCLK and SMBDATA (SIO Page)	28
		Modify SUSLED* circuit	41
		Change R74 and R75 to 8.25k and 82.5 ohm (ATI_PA_RS4X0F4.pdf)	14
		Modify N8_RST* circuit	20
3/22	SA_V1.8	Modify LAN Disable circuit	37
3/23	SA_V1.9	Add 6559 Common Ground	46
	SA_V1.10	Change PCIRST circuit from VCC3_3DUAL driven to VCC3_3S8	
		USE CLKRUN# of M1573(RUNGPO9) to disable CR1 and TMDs	
		Modify GPIO arrangement	
		Add another pair of SM bus dedicate for CLK GEN and DDR	
3/24	SA_V1.11	Net Swap	
3/25	SA_V1.12	Add Two capacitors for EMI	38
	SA_V1.13	Change Q70 to 3904 NPN BJT	42
3/30	SA_V1.16	Rename Reference and swap nets	
3/31	SA_V1.17	Connect H7 to AGND	
4/06	SA_V1.18	Add CLOCK MAP	50

NOTE :

DATE	Rev	Description	Page
0422	Sb_V2.0	Modify All SA PIR rework items and FJ GFX Feedback	
0426	Sb_V2.1	Modify R554 and R744 and FJ GFX Feedback ver.0427	47
0427		Swap ACZ_SDIN0 and ACZ_SDINI at Sb side	23
	Sb_V2.2	L_O_R can't be connected with Mute_LG	39
		Add R746/R747/R748	23
		Change C267 to 0.015uF and R418 to 60.4 ohm	44
		Add R749	27
		Modify LAN_RSTJ signal	37
		Remove JF2 and around circuit	21
		Change Pin assignment of CN99	40
		Modify LCD PWRON circuit	37
		Add USB ESD IC	26
		Add COMMON GND for SW regulator	44,45
		Change TC35 to Z20JF	
0505	Sb_V2.3	Add common ground near VRD low side MOS	46
		Modify SUSLED circuit	41
		Modify FAN tach circuit	41
		Modify GPIO assignment for LED function	
		Modify PCI Riser IOSEL	36
		Add FlashRom write protect function	
		Add Two more GPIO pin for Io_PMECS# and Io_PMeSS#	
0508	Sb_V2.5	Modify USBPWR control circuit	32
		Modify SUSLED circuit	41
		Modify TVON_Plug circuit	41
		Modify All LED circuit	41
		Modify BIOS write protection circuit	27
		Add a pull-up resistor on Mute#	40
		Change R557 to 100K ohm	
0509	Sb_V2.6	Modify VDDA_2.5V_CPU Enable circuit	08
		1394 port 0 and port1 swap	
0510	Sb_V2.7	Remove Q73 and ACZ_RST_CRL*	40
		Modify All LED circuit	41
		Modify USB POWER controller circuit	42
		Add two 1K ohm between VCC5_USB_F/VCC5USB_R* and GND	42
		Remove D31 and R517. Then change R518 from 1k-ohm to 0ohm and unmount as default.	29
		[ESD for DDC]	17/19
0511	Sb_V2.8	Add SLP_S4_H to control USB power	23/42
		Change R775.1 to VCC5	08
		Modify TVON_PLUSE3.jpg	28/41
	Sb_V2.9	Change Q65 to 2N7002 and remove R769	41
	Sb_V2.10	USE CRT_TMDS_DisJ to do mute function	40
		Change BOM option for Audio function	40
		Reserve 3.3V pull-up for Fansink	41
0512	Sb_V2.11	Modify VLD1_EN circuit	45
		Modify USB power control circuit	42
0513	Sb_V2.12	Unmount R8	41
0517	Sb_V2.13	Change Q105 to FET(2N7002)	40
		Change Board ID	21
		Consumer M/B: Board_ID[3..0] = "0001"	
		Corporate M/B: Board_ID[3..0] = "1000"	
		Small Qty M/B: Board_ID[3..0] = "0010"	
		Change C67 to X7R	16
		Change R512 for Consumer/LCDPC , Change R508 for Corporate	29
		Change C98 and C413 to X5R	32 26
		mount C691 and C692	24
		R13 R14 change to 1Kohm , RN1 change to 1K ohm	28
		U58 U59 U60 change to 83.01293.0AE	26
0524		R129 unmount, L66 change to 63.R0004.151	32 38
0525		R59 R777 change to 0 ohm, Q103 Q15 change to 2N7002	41

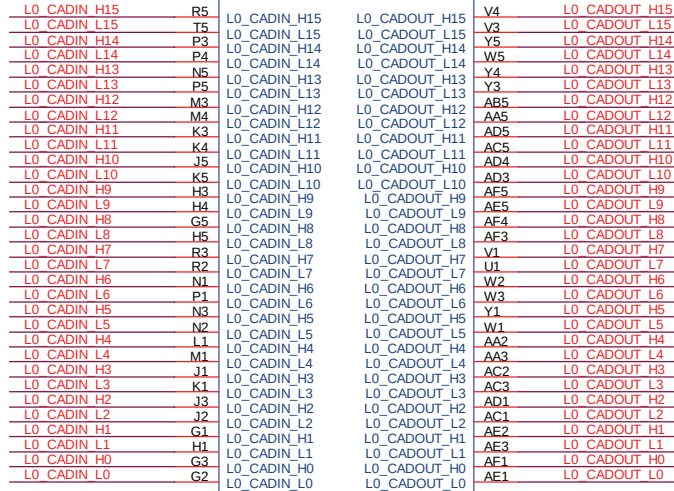
Processor HyperTransport Interface



At least 200mils for pure
and 20mils to pin

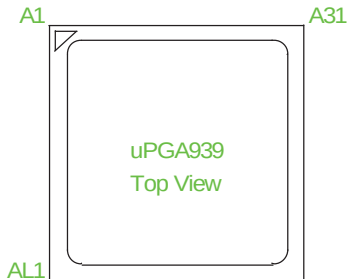
At least 100mils to Capacitor
and 20mils to pin

12 L0_CADIN_L[0..15] >> L0_CADIN_L[0..15]
12 L0_CADIN_H[0..15] >> L0_CADIN_H[0..15]
20/5/5/20 1"<x<12"



L0_CADOUT_H[0..15] >> L0_CADOUT_H[0..15] 12
L0_CADOUT_L[0..15] >> L0_CADOUT_L[0..15] 12
20/5/5/20 1"<x<12"

12 L0_CLKIN_H1 >> L0_CLKIN_H1 12
12 L0_CLKIN_L1 >> L0_CLKIN_L1 12
12 L0_CLKIN_H0 >> L0_CLKIN_H0 12
12 L0_CLKIN_L0 >> L0_CLKIN_L0 12
12 L0_CTLIN_H0 >> L0_CTLIN_H0 12
12 L0_CTLIN_L0 >> L0_CTLIN_L0 12
20/5/5/20 1"<x<12"



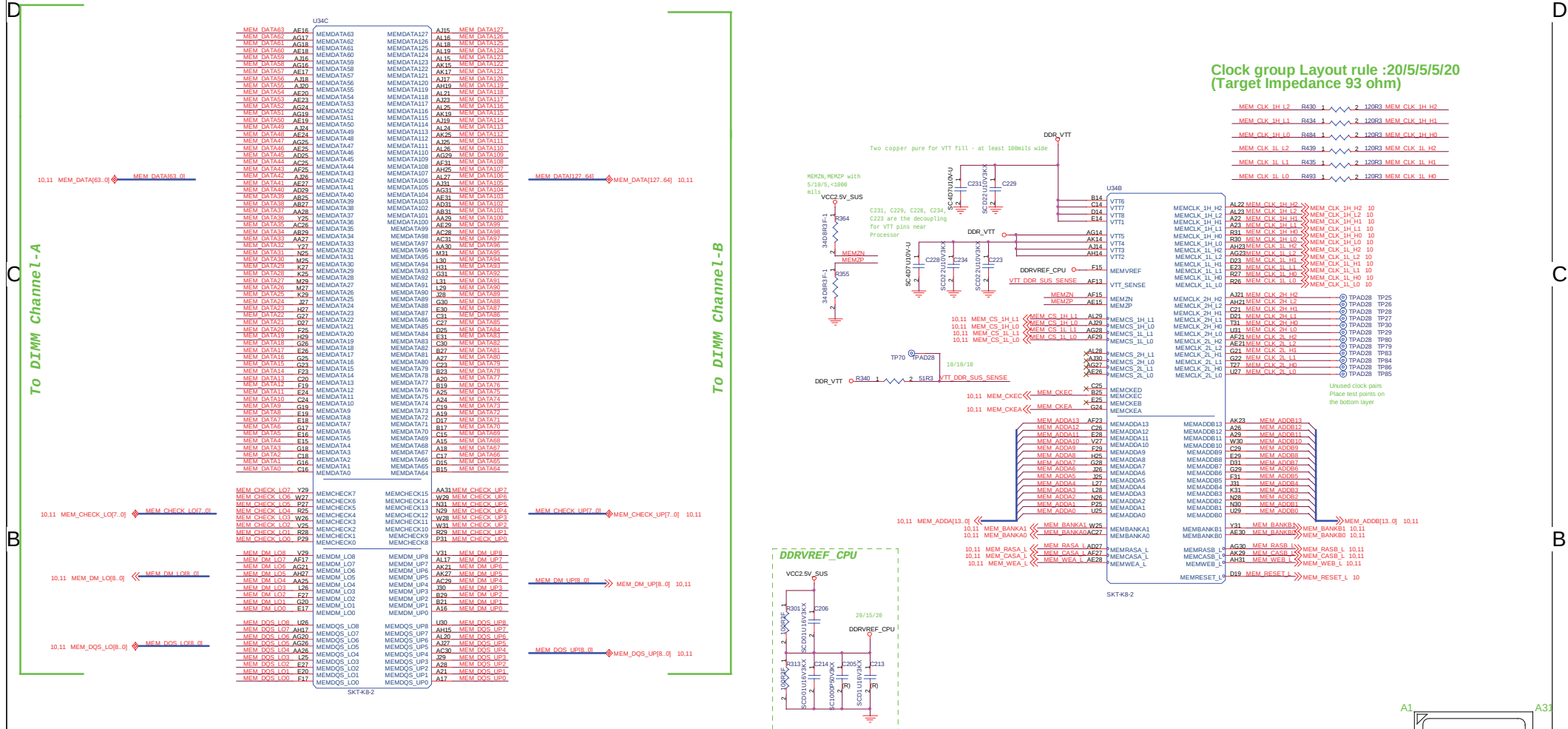
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wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title Althon64/64FX HT I/F		
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Processor DDR Memory Interface



Data/DIMM/CHECK group Layout rule : (Target Impedance 45 ohm)

Break in/out : 15/15/15

Motherboard trace routing : 10/10/10

DQS group Layout rule : (Target Impedance 35 ohm)

Break in/out : 20/5/20

Motherboard trace routing : 20/15/20

Address/Command group Layout rule : (Target Impedance 45 ohm)

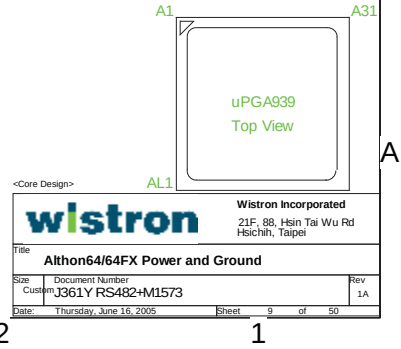
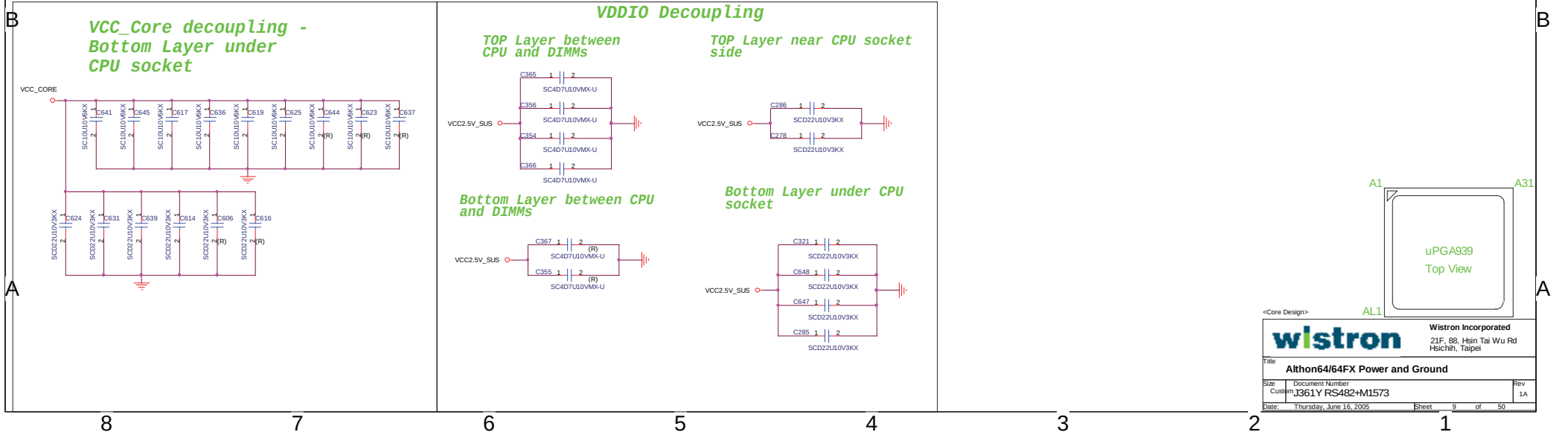
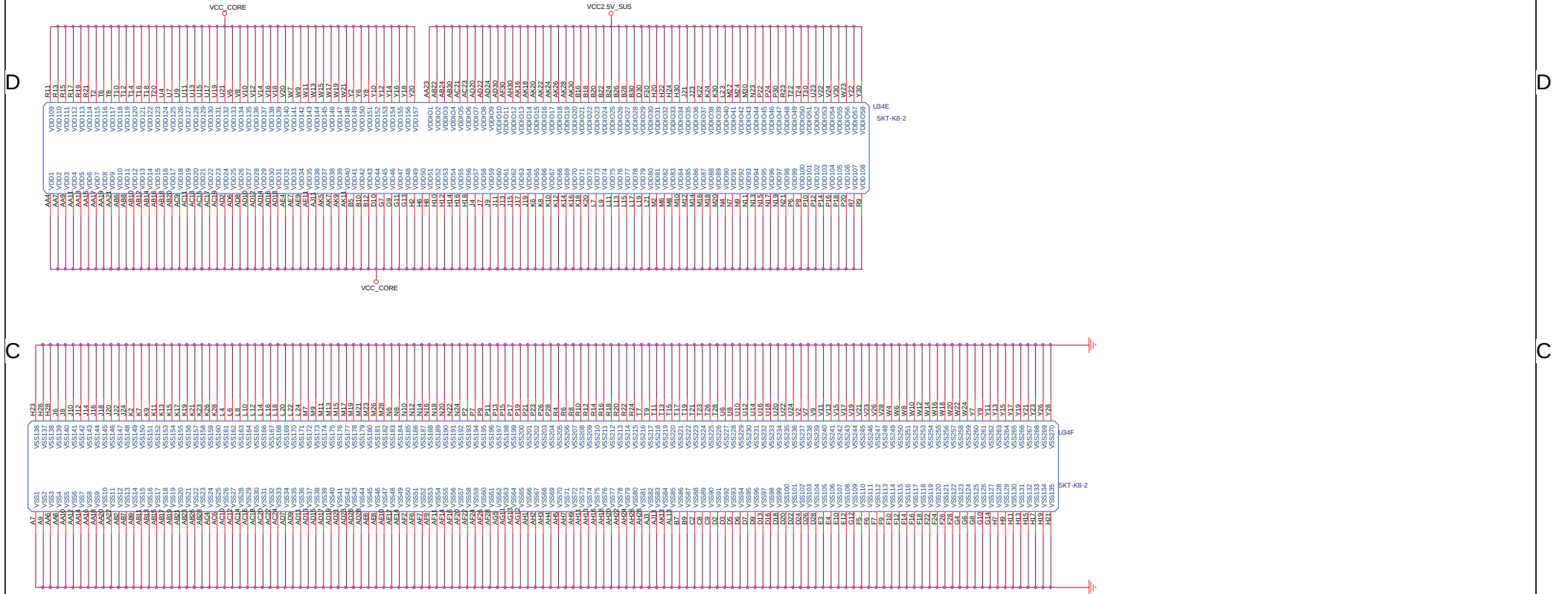
Break in/out : 15/15/15

Motherboard trace routing : 10/10/10

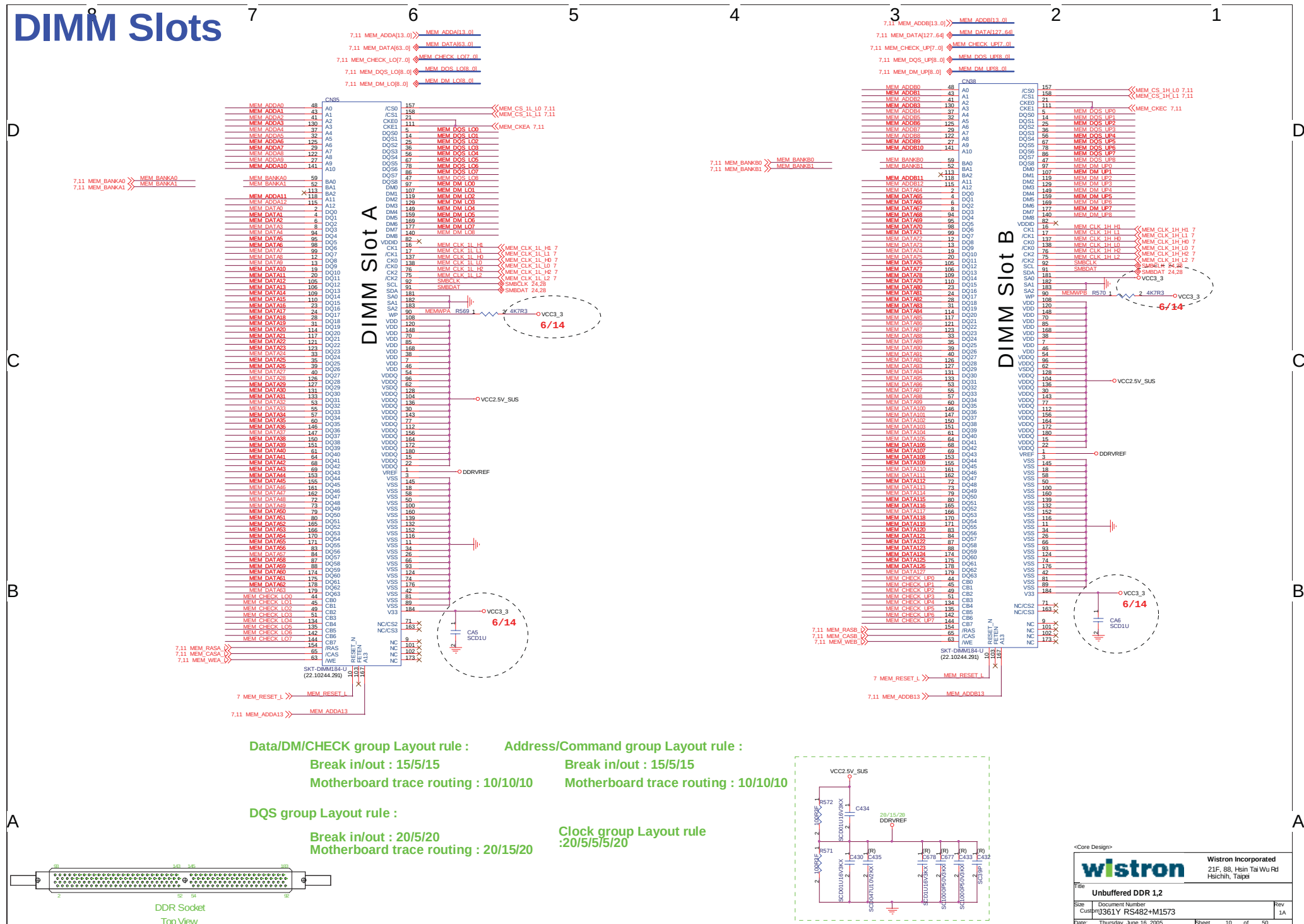
D



Processor POWER & Ground



DIMM Slots



DDR Termination

Data/DMA/CHECK group Layout rule :
Break in/out : 15/5/15
Motherboard trace routing : 10/10/10

DQS group Layout rule :
Break in/out : 20/5/20
Motherboard trace routing : 20/15/20

Address/Command group Layout rule :
Break in/out : 15/5/15
Motherboard trace routing : 10/10/10

Channel A

Channel B

Place between CPU and DIMMs

Place at either end of VTT island

Wistron

Wistron Incorporated
21F., 88, Hei Tai Wu Rd
Foshin, Taipei

DDR termination

Sum : Document Number
Custno361Y RS462-M1573

Date : Thursday, April 16, 2009

Rev : 1A

Address/Command group Layout rule :
Break in/out : 15/5/15
Motherboard trace routing : 10/10/10

Place between CPU and DIMMs

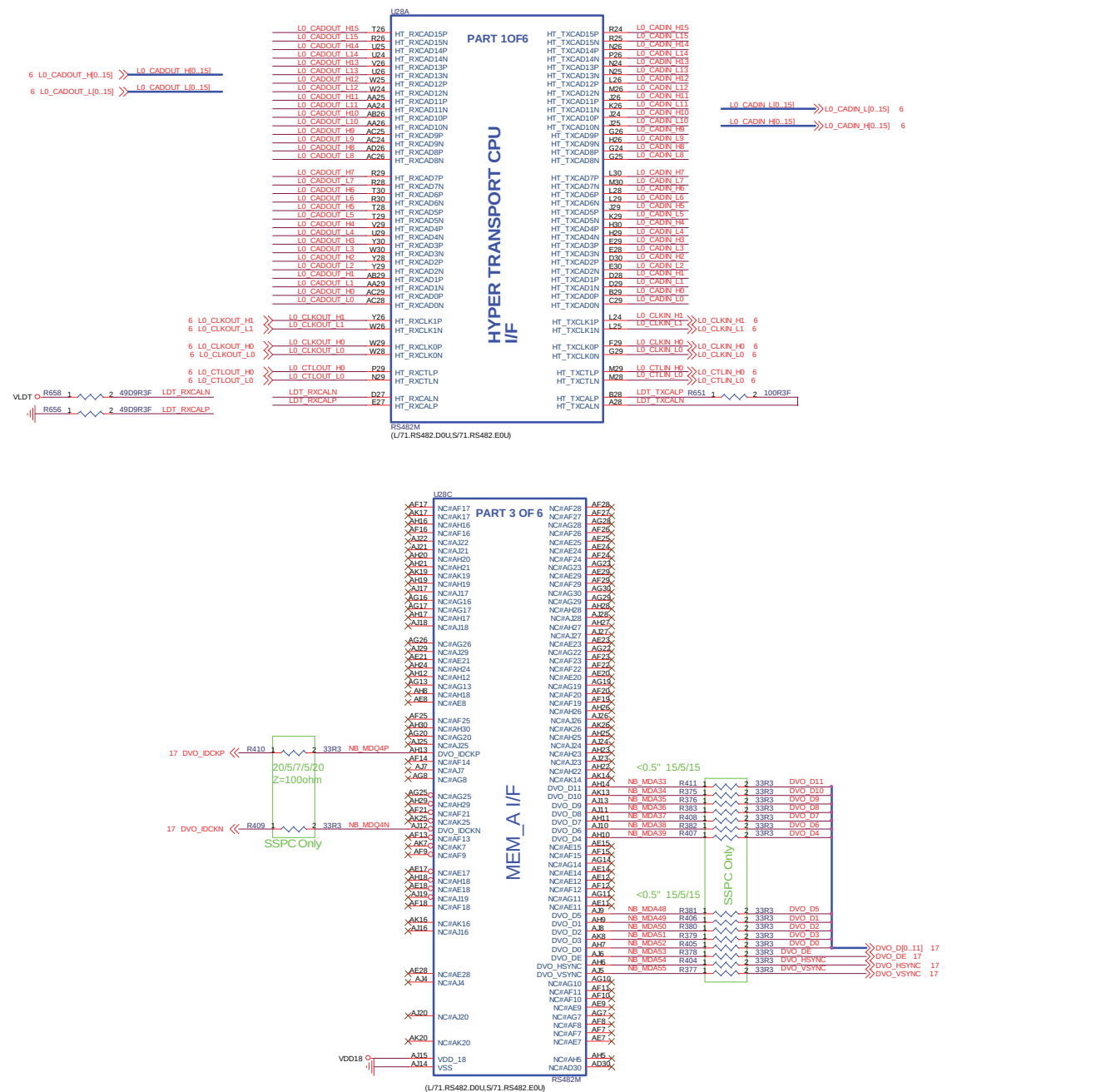
Place at either end of VTT island

<Core Design>		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
wistron			
Title DDR termination			
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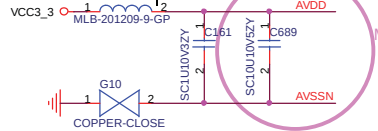
RS482 ver.A12    PB_P/N 71.RS482.E0U
RS482 ver.A12    LF_P/N 71.RS482.B0U
RS482M ver.A12   PB_P/N 71.RS482.D0U
RS482M ver.A12   LF_P/N 71.RS482.C0U

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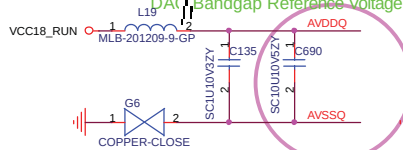
NB/RS482M DAC/LVDS/CLK/PM

Dedicated for DAC POWER



Modify 0506

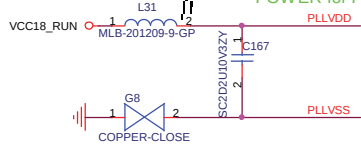
DAC Bandgap Reference Voltage



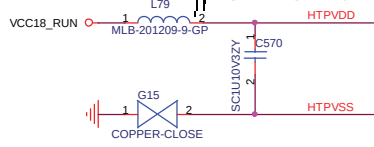
Guard Trace for TV-out and RGB signals

10/10/10

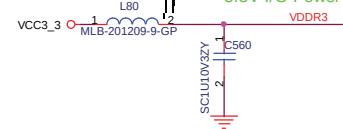
POWER for PLL



POWER for HT I/F PLL



3.3V I/O Power



HW Strapping Setting

DFT_GPIO1(LOAD_ROM_STRAPS#): High-not connected EEPROM (Default)
Low-load strap values from EEPROM

DFT_GPIO2(HT_Width_Override): High-8 bit link (default)
Low-for testing only

DFT_GPIO[4..3](Overrides HT Freq): 11-200MHz(Default)

DFT_GPIO5(LOAD_MEM_STRAPS#): 0-capture DVO pins for debug bus straps.
1-Use Default Values

NOTE: Provide access to STRAP_DATA and I2C_SCL pins is MANDATORY.

1-Use Default Values

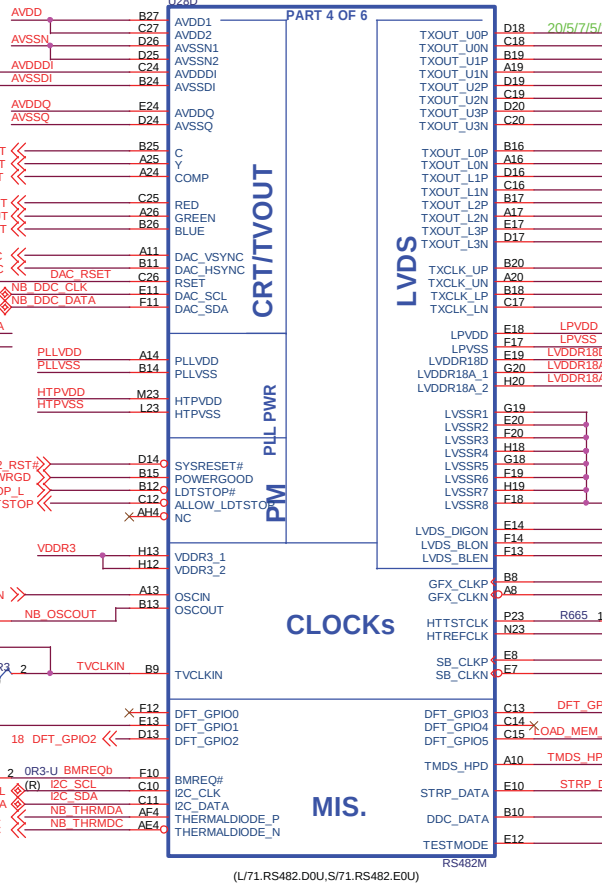
1-Use Default Values

1-Use Default Values

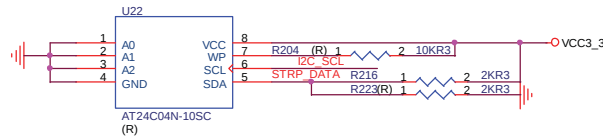
1-Use Default Values

1-Use Default Values

1-Use Default Values



(U71.RS482.D0U,S71.RS482.E0U)



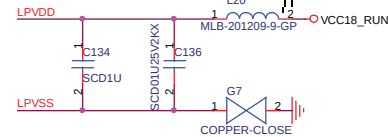
AT24C04N-10SC (R)

LVDS

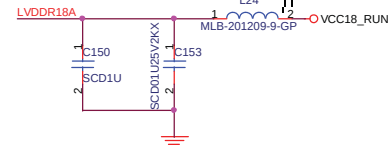
CLOCKS

MIS.

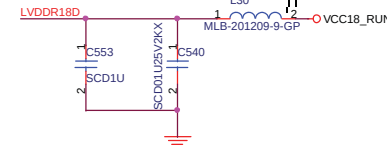
For LVDS PLL



For LVDS Analog power



For LVDS Digital power

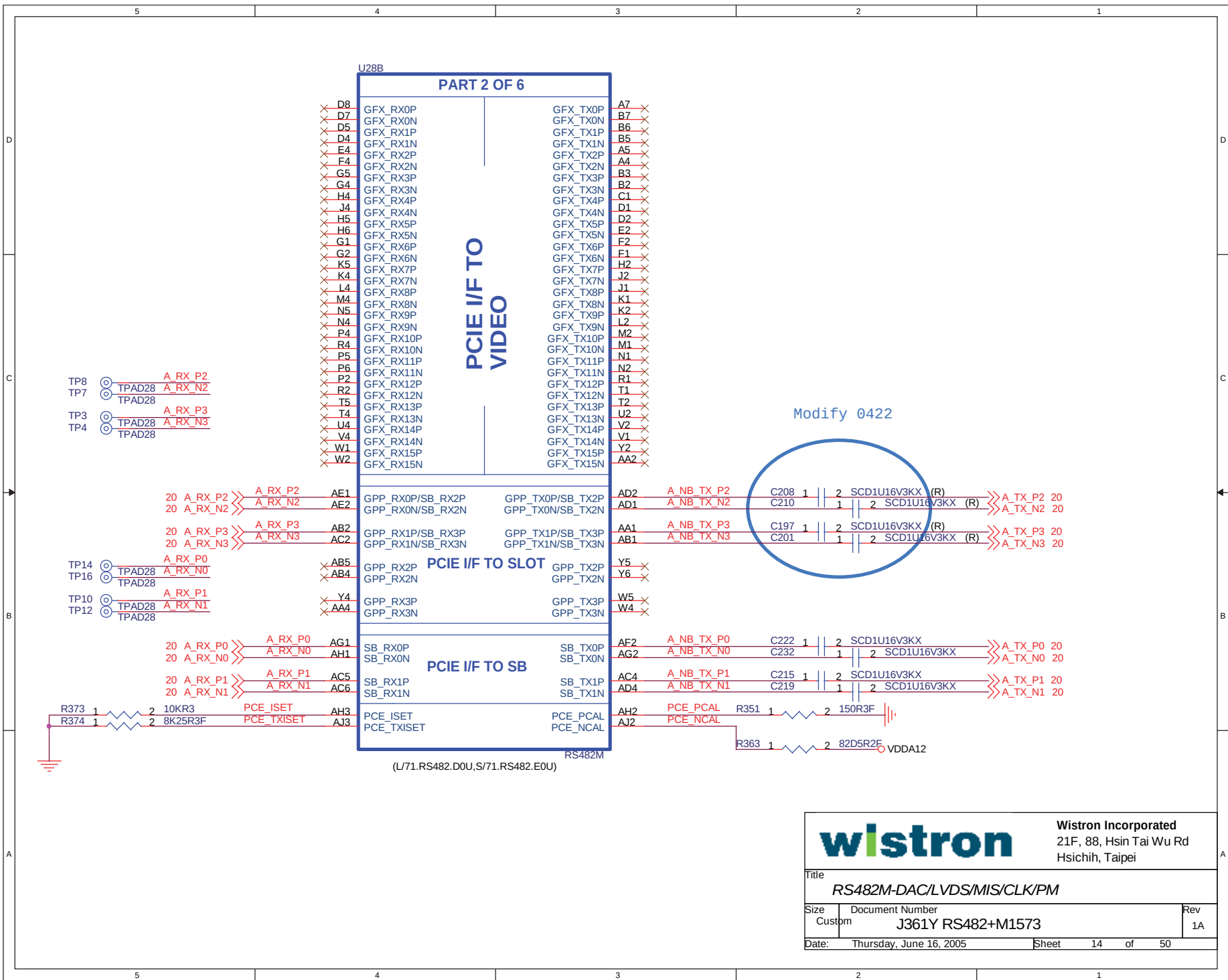


PCIE 16X diff CLK

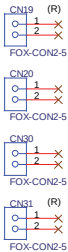
HT 66MHz Ref Clk

A-Link diff CLK

		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title <i>RS482M-DAC/LVDS/MIS/CLK/PM</i>			
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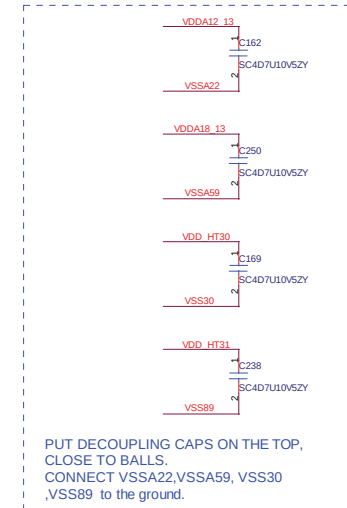
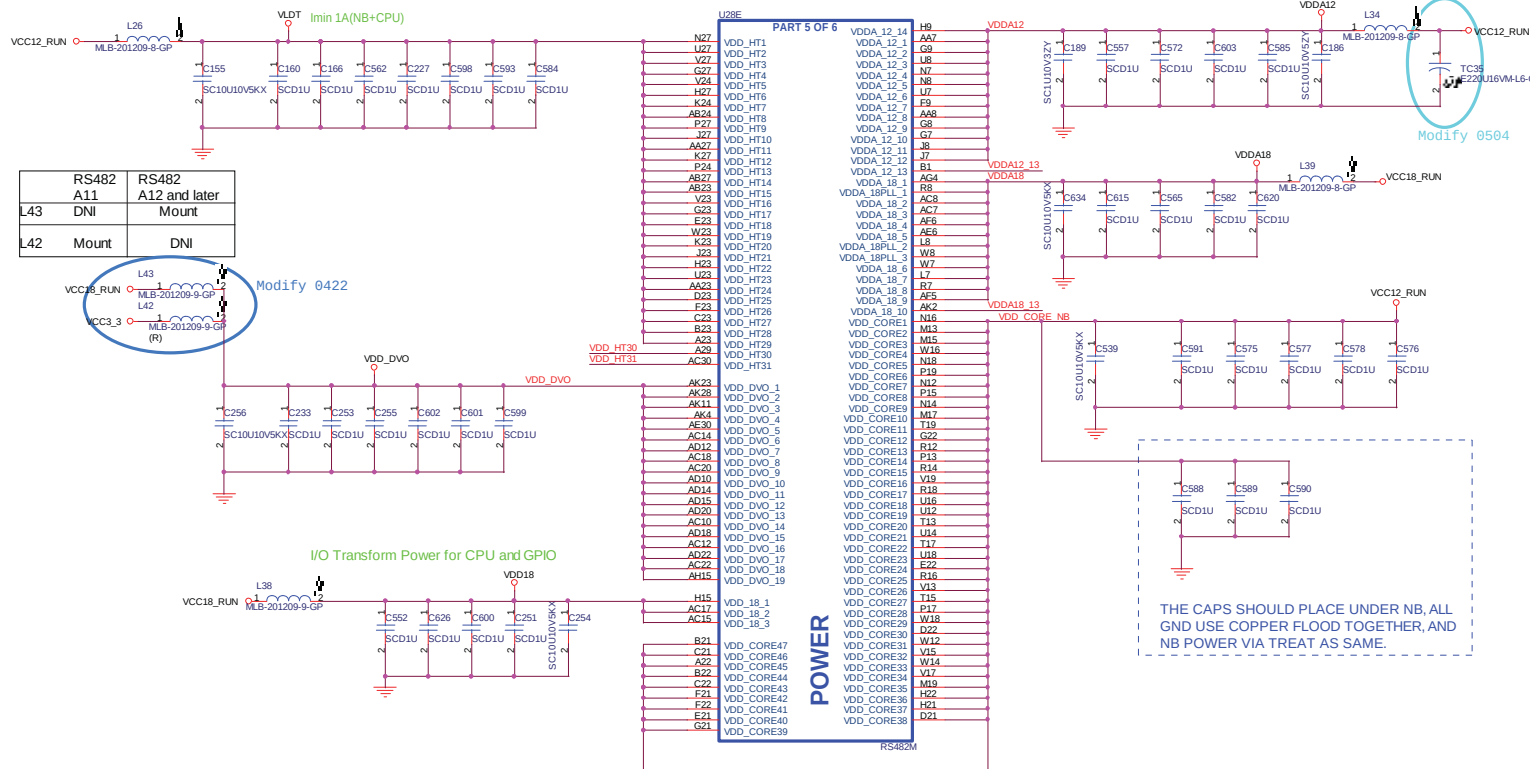


NB Heat Sink Clip



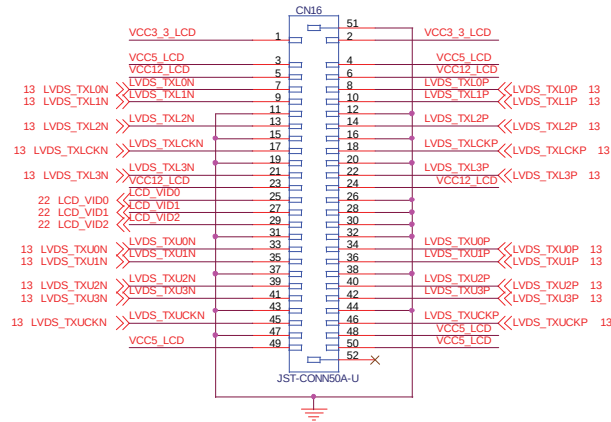
NB RS482M POWER STATES

Power	Signal	S0	S1	S3	S4/S5	G3
VDDHT		ON	ON	OFF	OFF	OFF
VDDR, VDDRCK		ON	ON	ON	OFF	OFF
VDD18		ON	ON	OFF	OFF	OFF
VDDC		ON	ON	OFF	OFF	OFF
VDDA18		ON	ON	OFF	OFF	OFF
VDDA12		ON	ON	OFF	OFF	OFF
AVDD		ON	ON	OFF	OFF	OFF
AVDDDI		ON	ON	OFF	OFF	OFF
PLLVD		ON	ON	OFF	OFF	OFF
HTPVDD		ON	ON	OFF	OFF	OFF
VDDR3		ON	ON	OFF	OFF	OFF
LPVDD		ON	ON	OFF	OFF	OFF
LVDDR18D		ON	ON	OFF	OFF	OFF
LVDDR18A		ON	ON	OFF	OFF	OFF



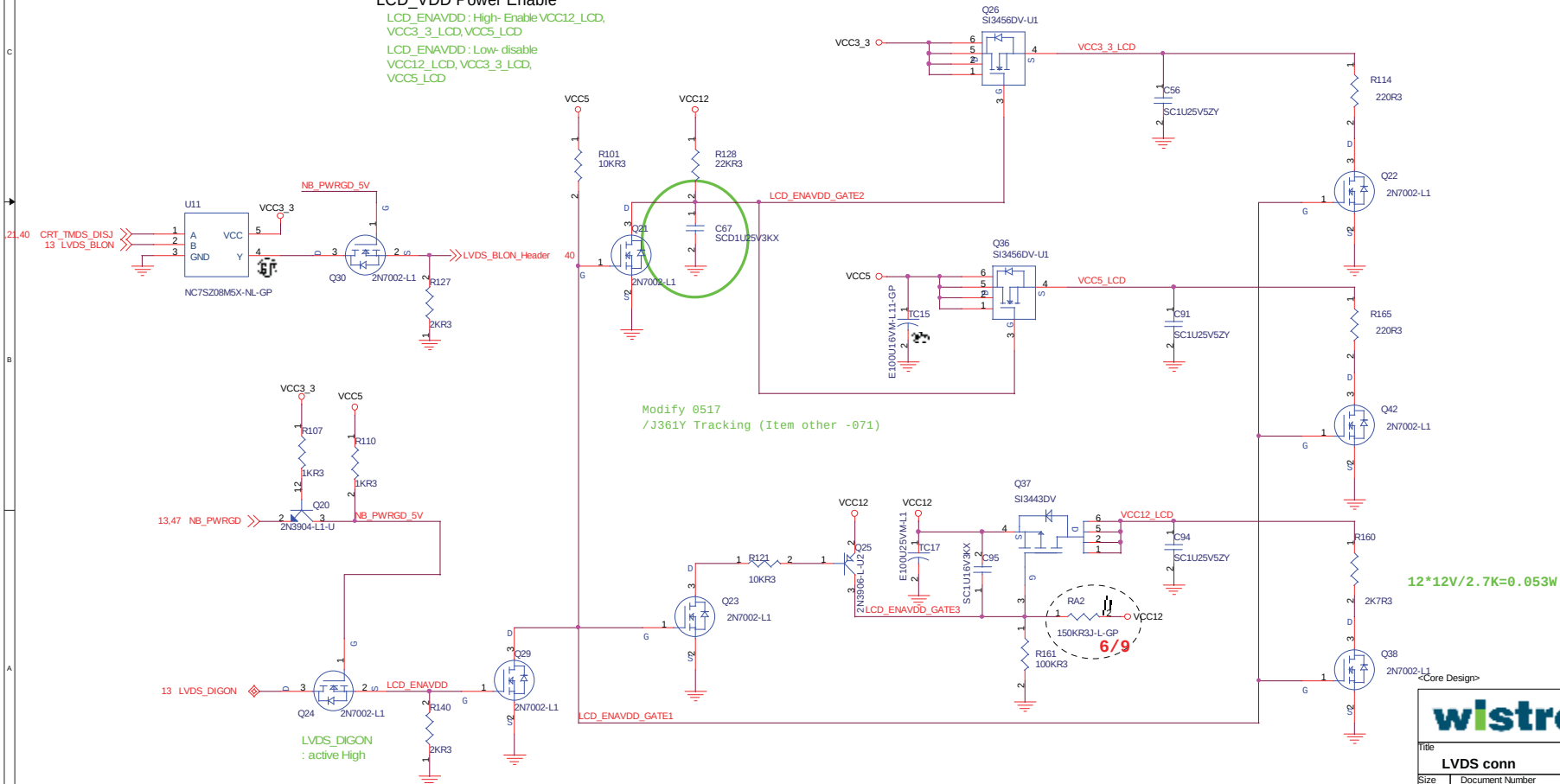
THE CAPS SHOULD PLACE UNDER NB, ALL GND USE COPPER FLOOD TOGETHER, AND NB POWER VIA TREAT AS SAME.

LVDS header (LCDPC Only)



LCD_VDD Power Enable

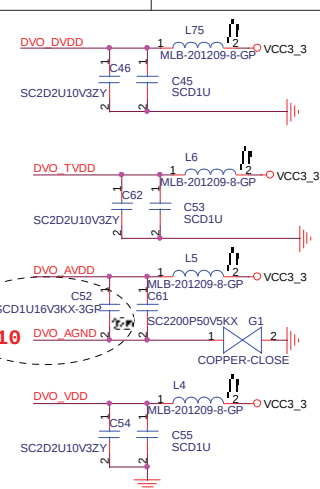
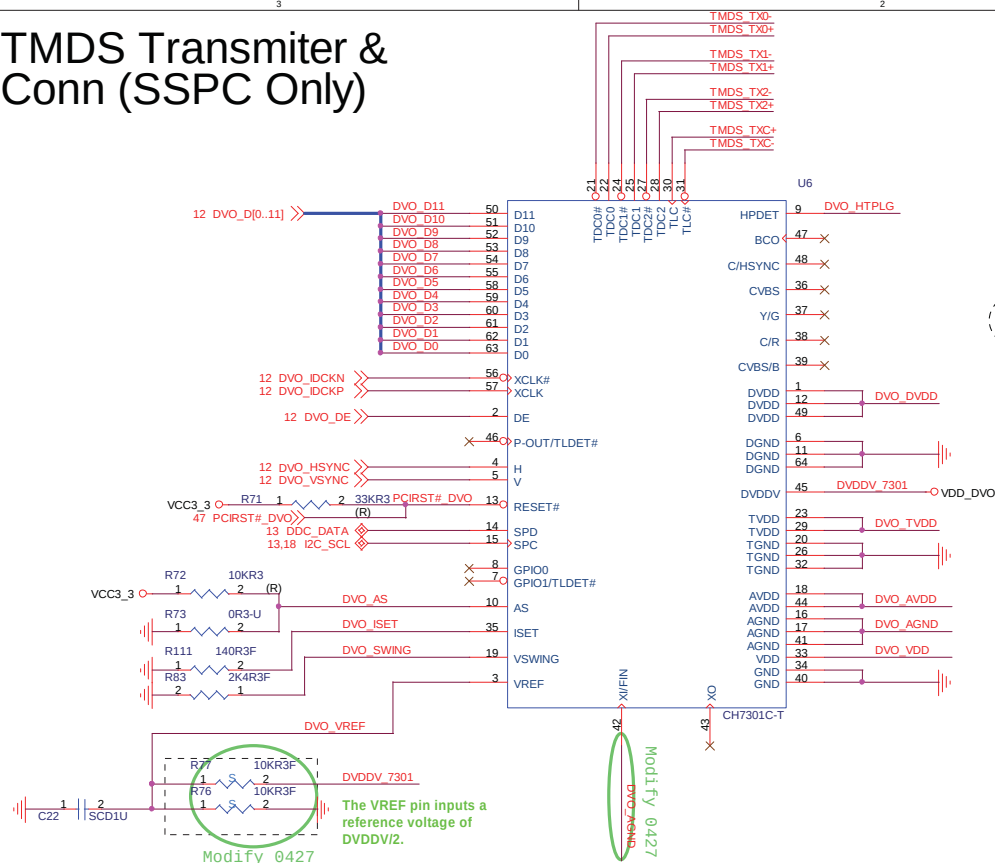
LCD_ENAVDD : High- Enable VCC12_LCD,
VCC3_3_LCD, VCC5_LCD
LCD_ENAVDD : Low- disable
VCC12_LCD, VCC3_3_LCD,
VCC5_LCD



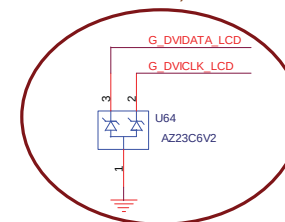
12*12V/2.7K=0.053W

		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title LVDS conn			
Size	Document Number J361Y RS482+M1573		Rev 1A
Custom			
Date:	Thursday, June 16, 2005	Sheet	16 of 50

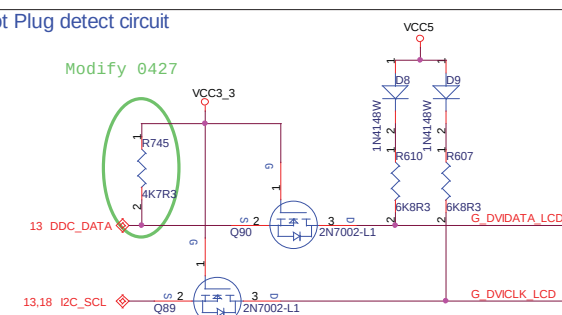
TMD5 Transmitter & Conn (SSPC Only)



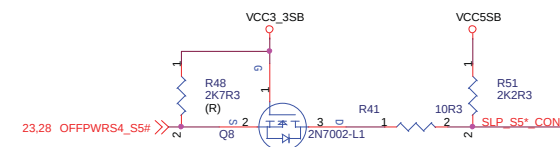
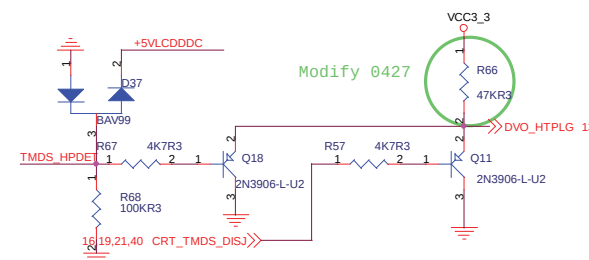
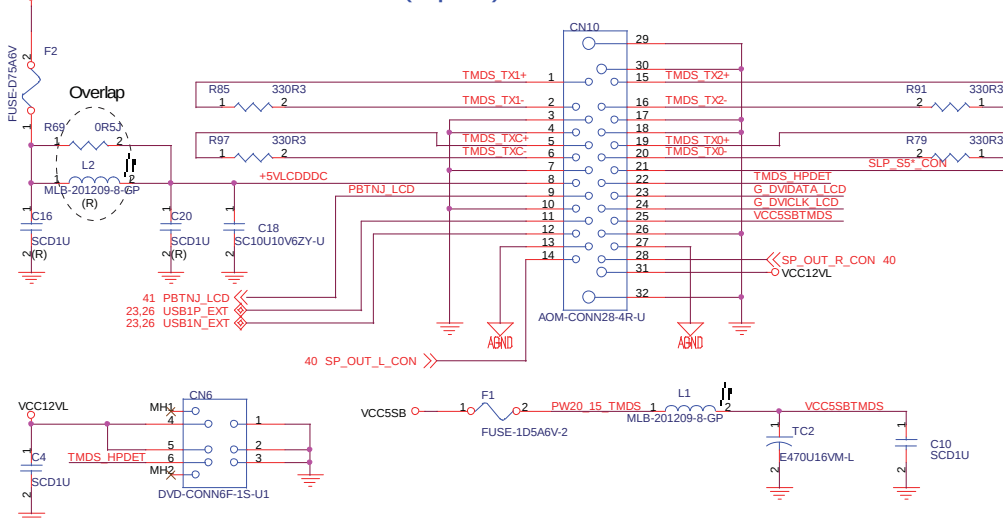
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Modify 0510
/J361Y_Tracking (Item
other-064)
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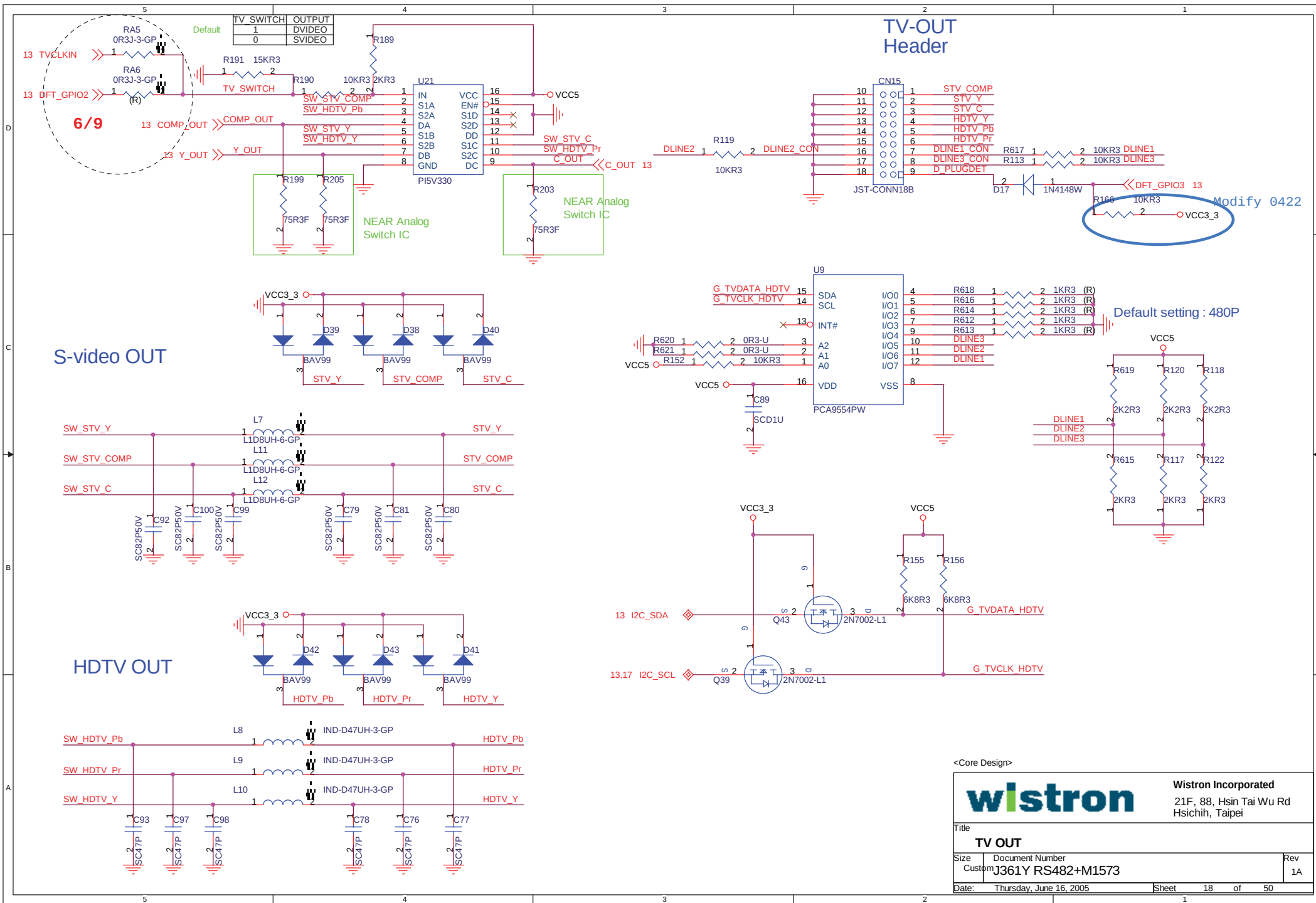


Hot Plug detect circuit



TMDS Conn & PS conn (6 pins)

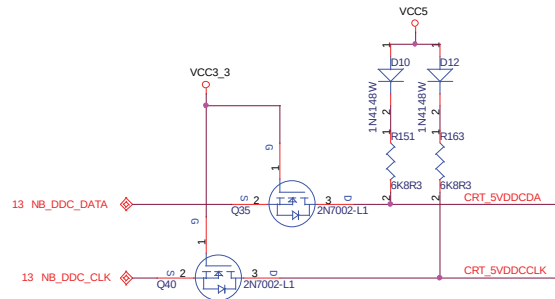
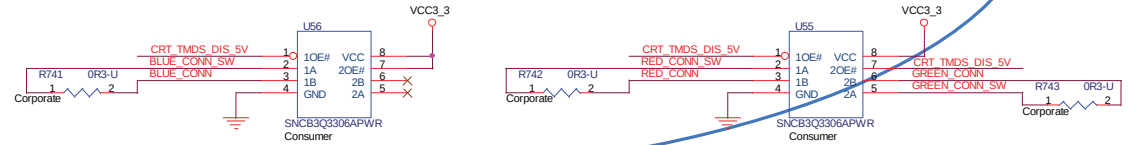
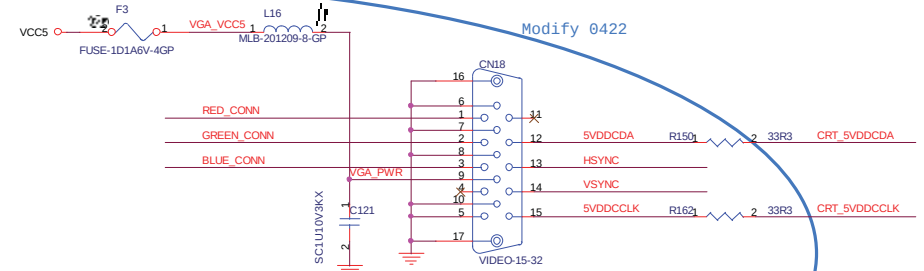
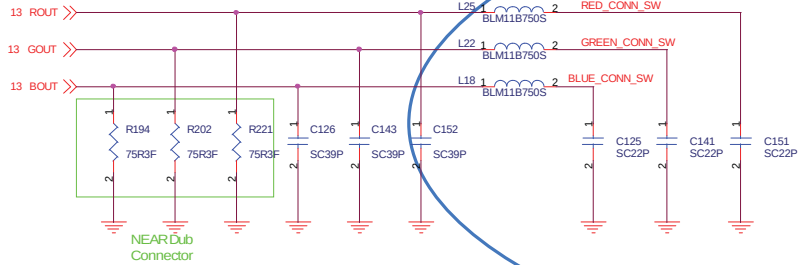




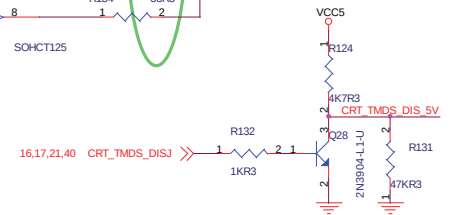
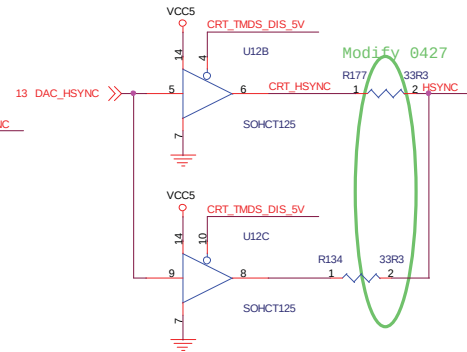
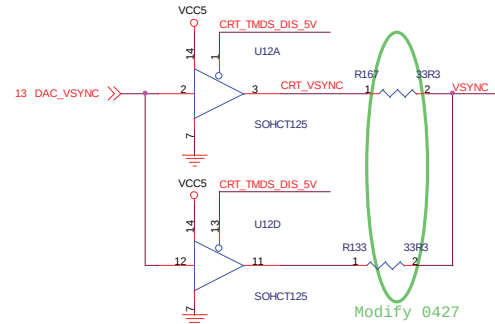
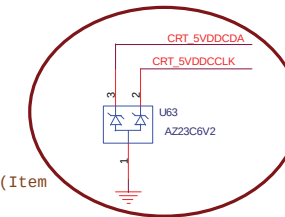
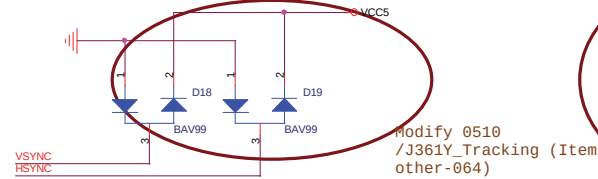
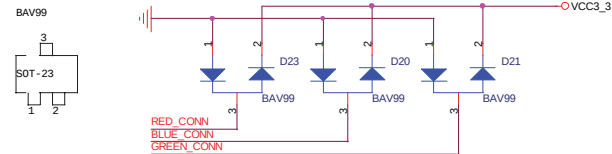
Video Filter & CRT CONN

Z=37.5ohm
20/12/20

Z=75ohm
20/4/20



ESD PROTECTION



<Core Design>



Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title

VGA CONN

Size

Customer

Document Number

J361Y RS482+M1573

Rev

1A

Date

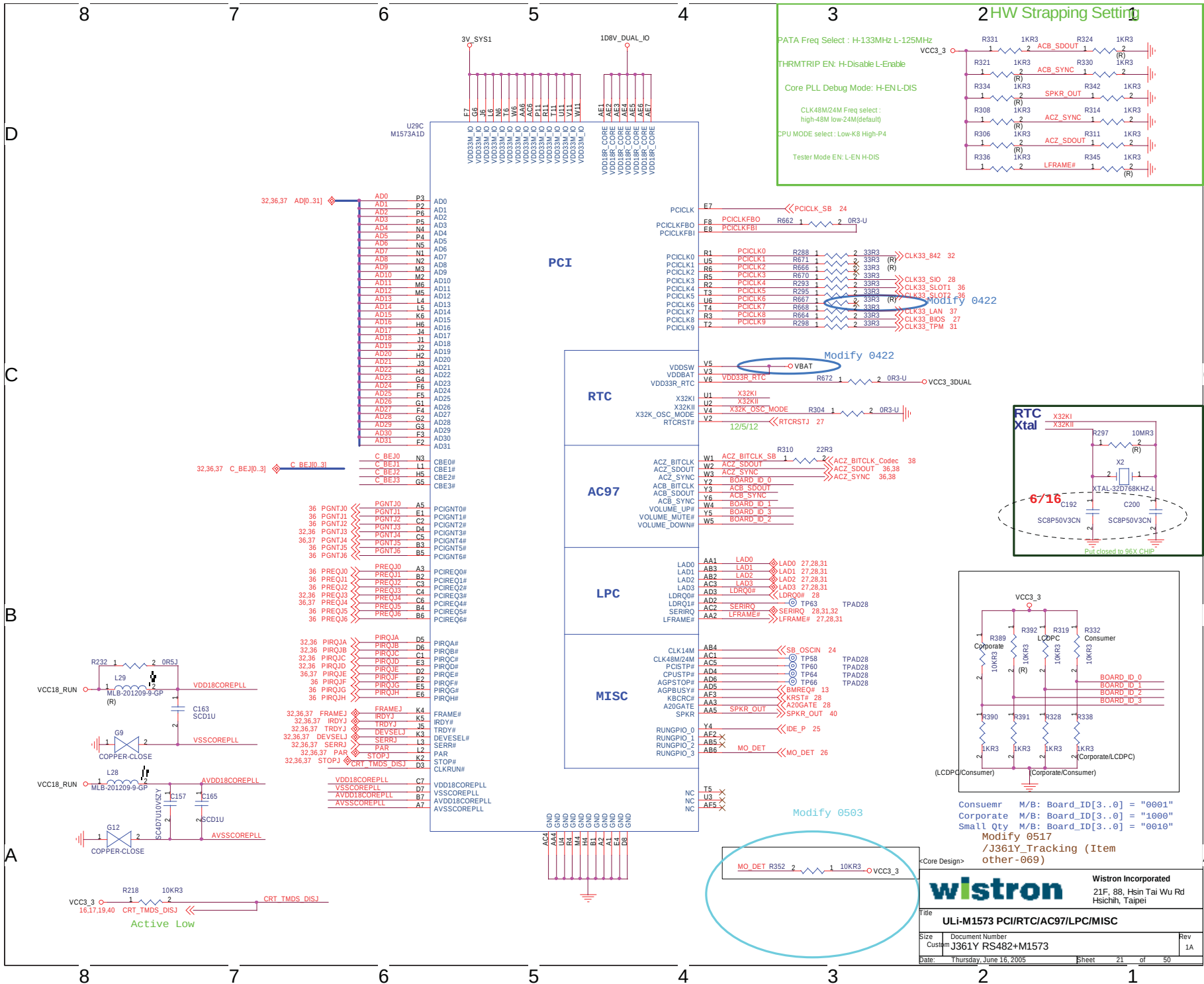
Thursday, June 16, 2005

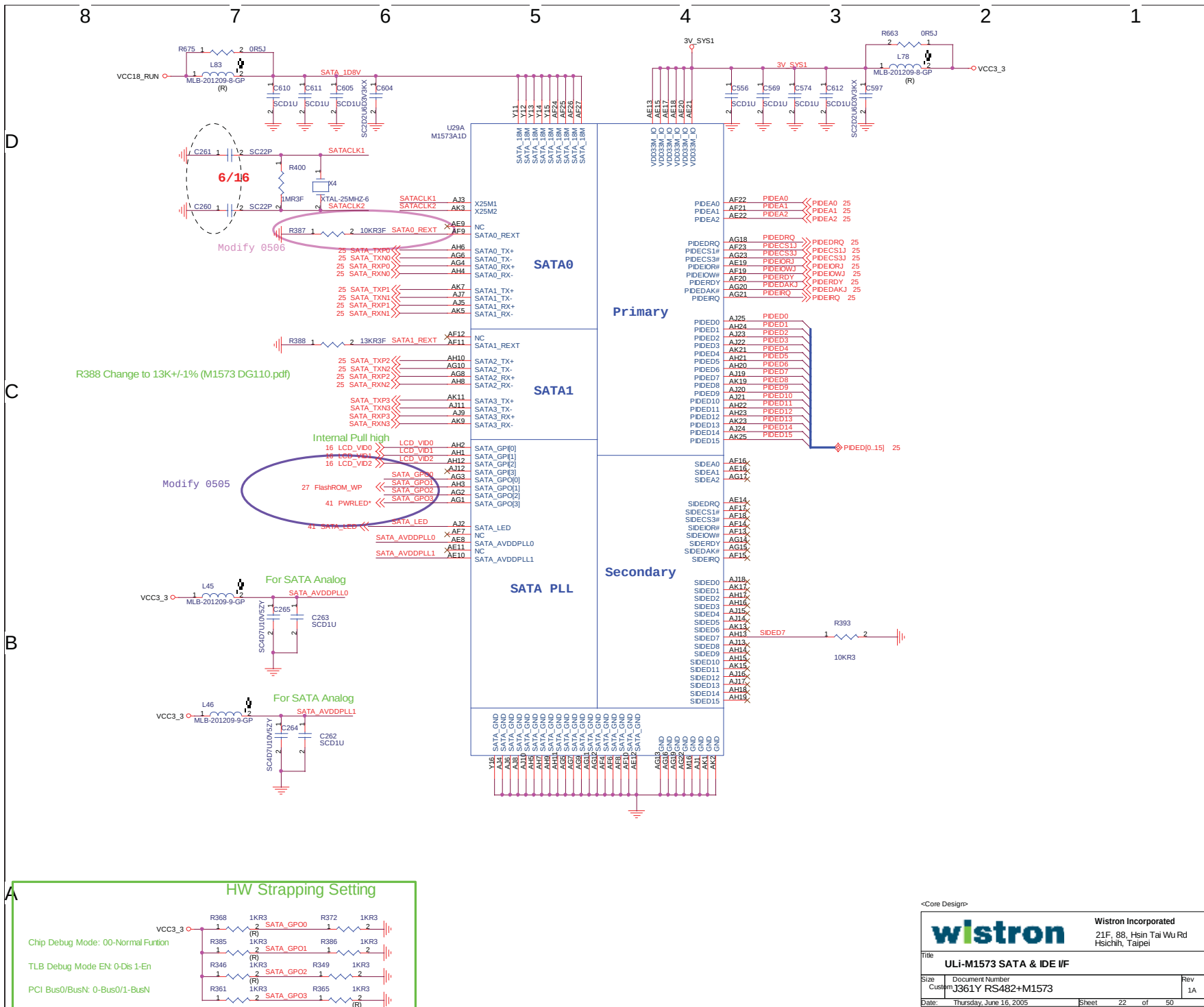
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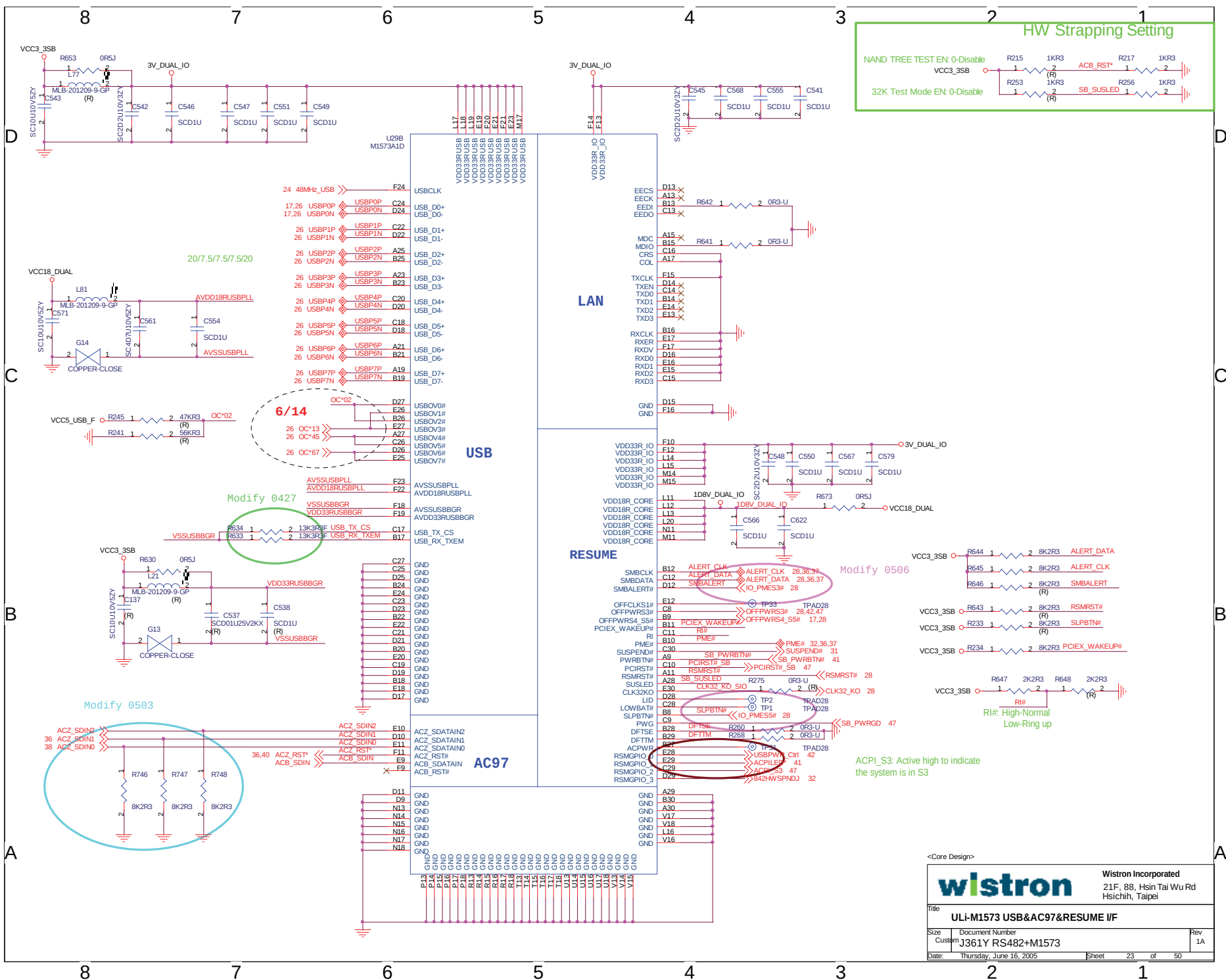
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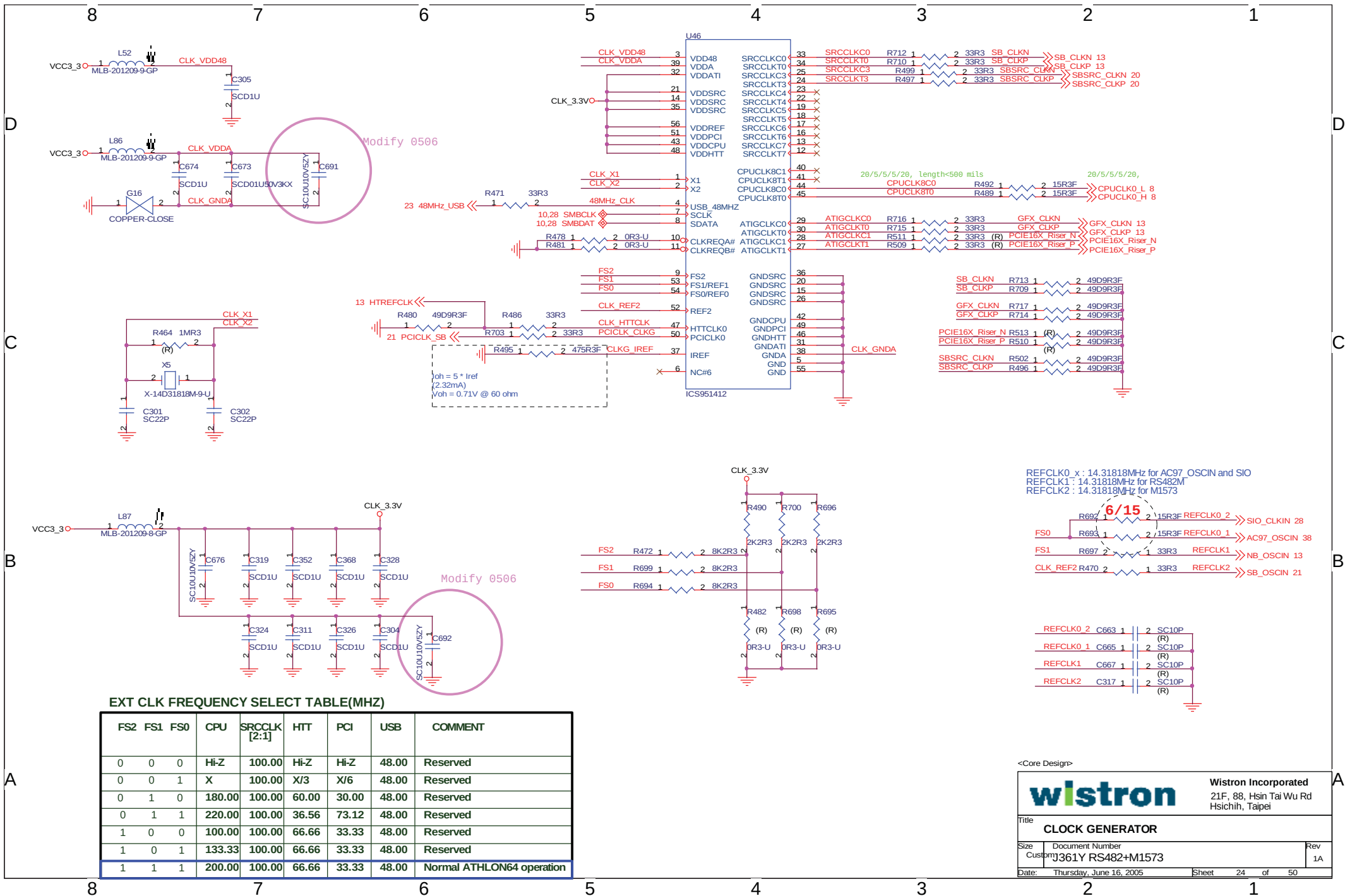
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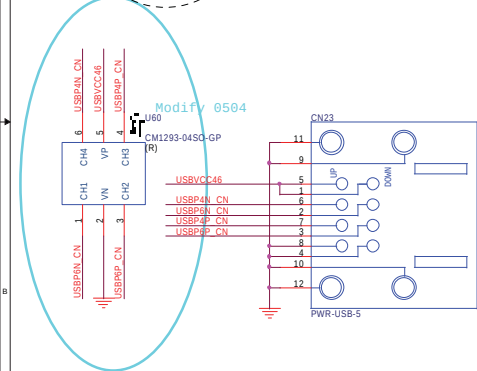
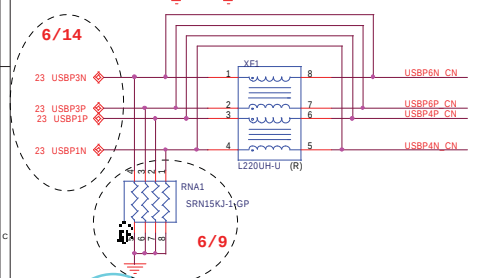
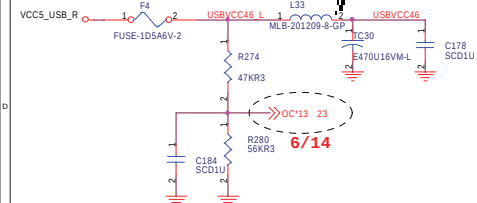




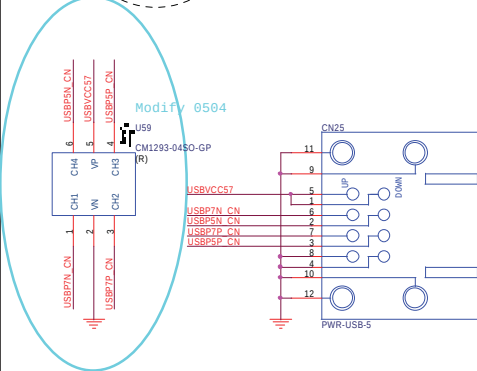
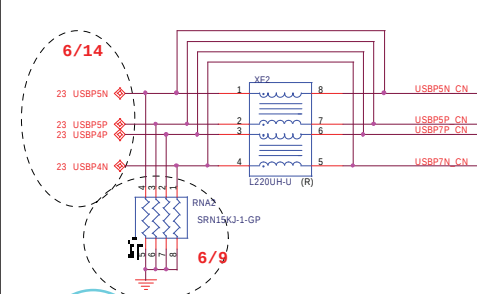
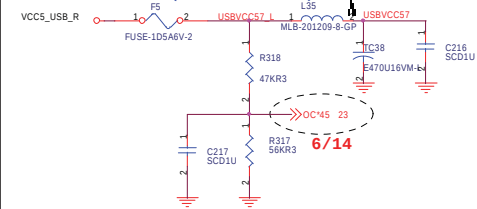


USB CONN

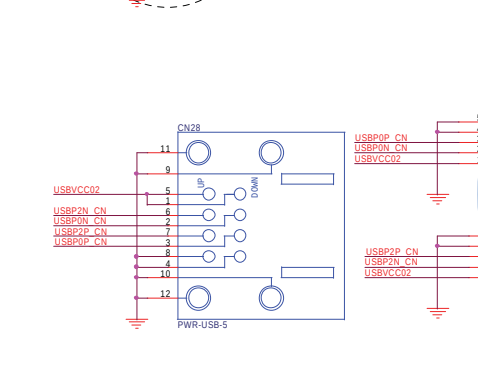
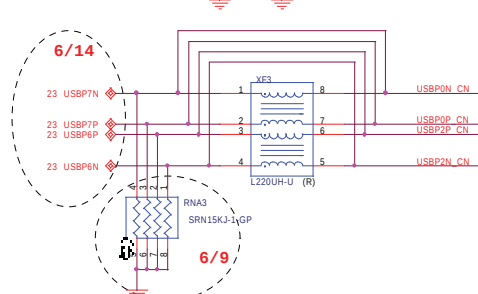
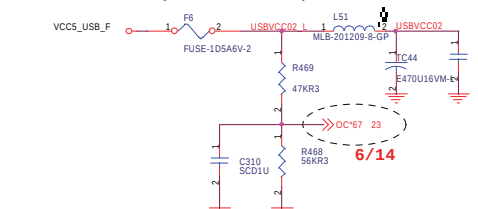
Rear USB CONN 1(Port 4 and Port6)



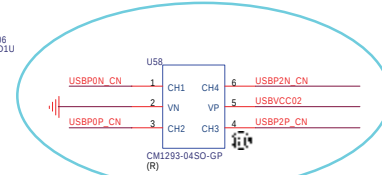
Rear USB CONN 2(Port5 and Port7)



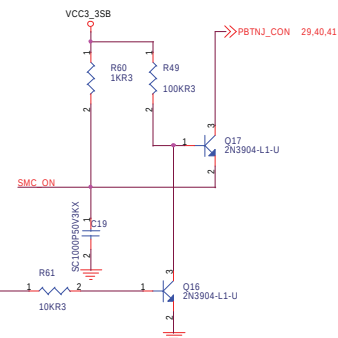
Front USB CONN(Port 0 and Port2)



Modify 0504

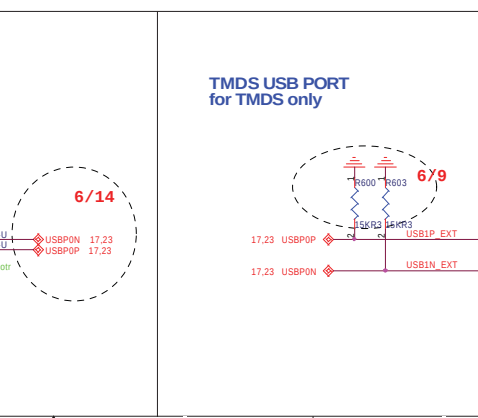
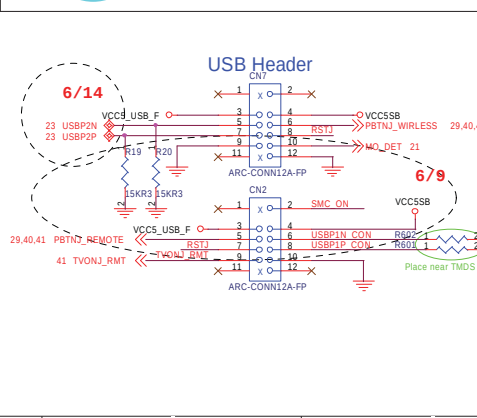
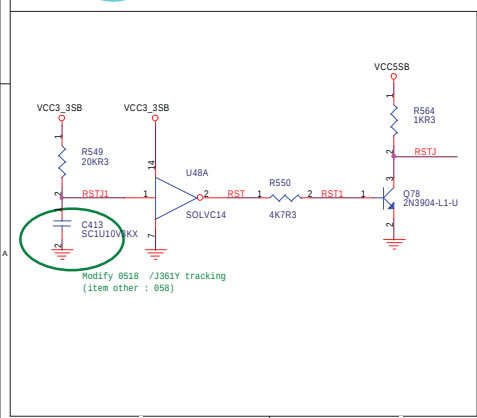


SMART CARD CIRCUIT

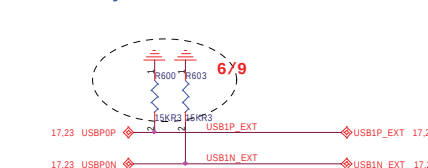


SLP S1 S5 L*:
High@S4,S5

USB Layout Rule : 20/7.5/7.5/7.5/20



TMDS USB PORT for TMDS only



<Core Design>

		Wistron Incorporated	
		21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title			
USB CNT			
Size	Document Number		Rev
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[illegible]

BIOS SCOKET P/N : 62.10061.001

RTC Battery

Close to Uli M1573

Modify 0422

I(R627) must be less than 4.566uA

Battery P/N-23.20023.L01 200MAH BT1 CR2032-1

Modify 0508

JP1	COMS setup
1-2	NORMAL (Default)
2-3	CLEAR CMOS

<Core Design>



Wistron Incorporated

21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title

BIOS/Battery RTC

Size

Document Number
J361Y RS482+M1573

Rev
1A

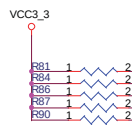
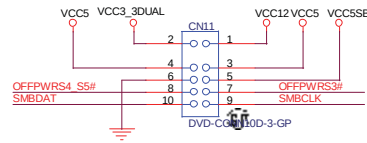
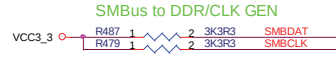
Date:

Thursday, June 16, 2005

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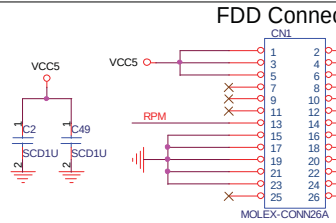
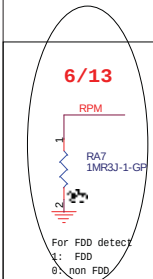
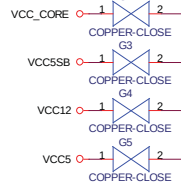
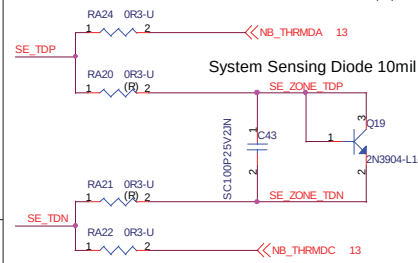
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SIO SMSC DM1737/FDD Header

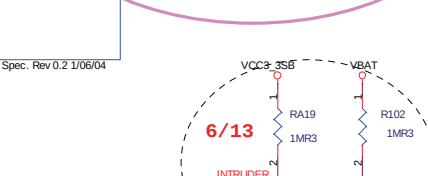
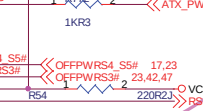
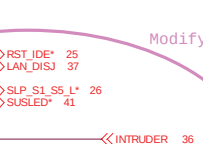
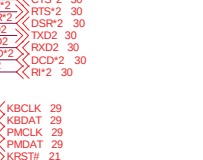
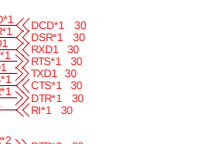
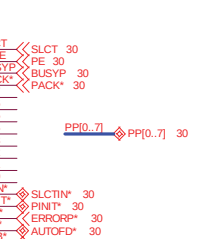
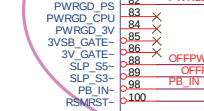
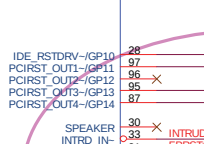
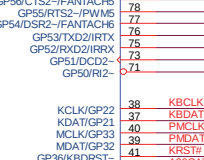
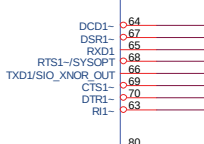
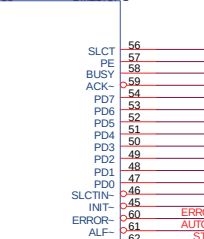
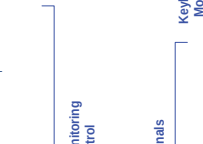
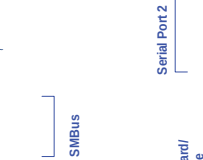
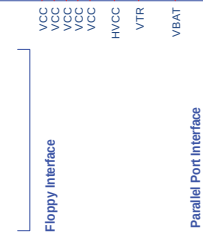
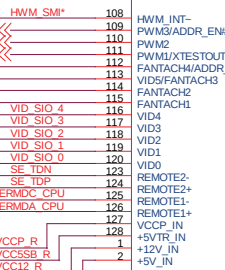
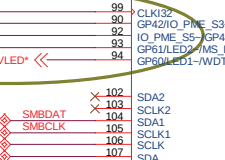
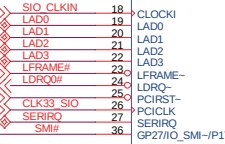
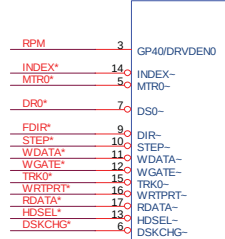
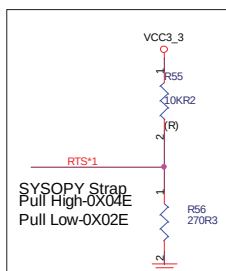
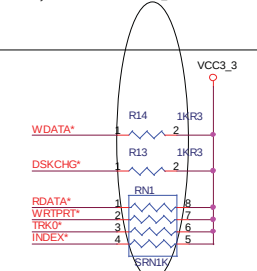


Modify 0512 /J361Y
Tracking (Item: other051)
23 CLK32 KO

If 32.768KHz clk isn't used by SIO, then it needs pull-low externally.

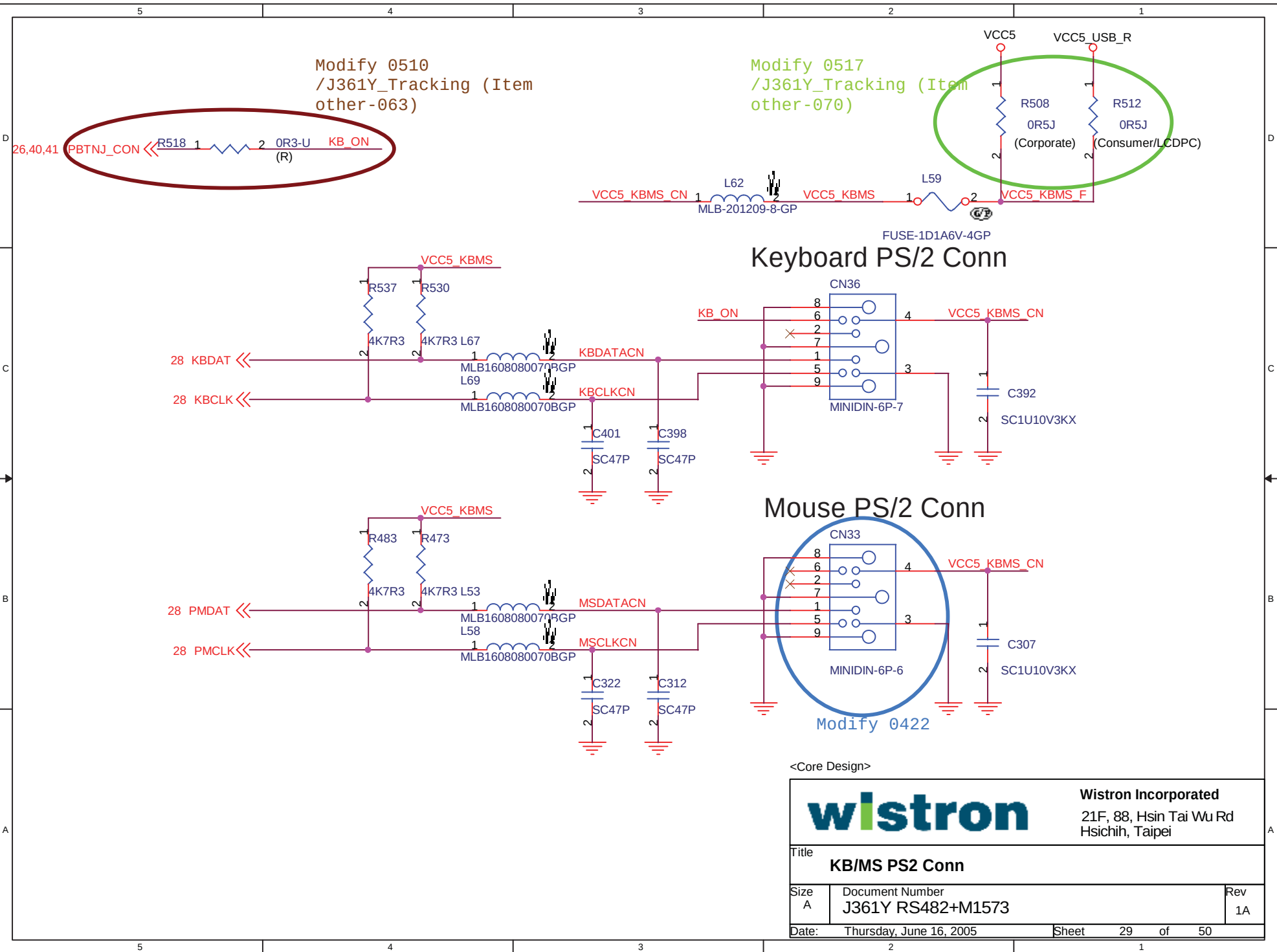


Modify 0519 / follow UPF05_P4 mode



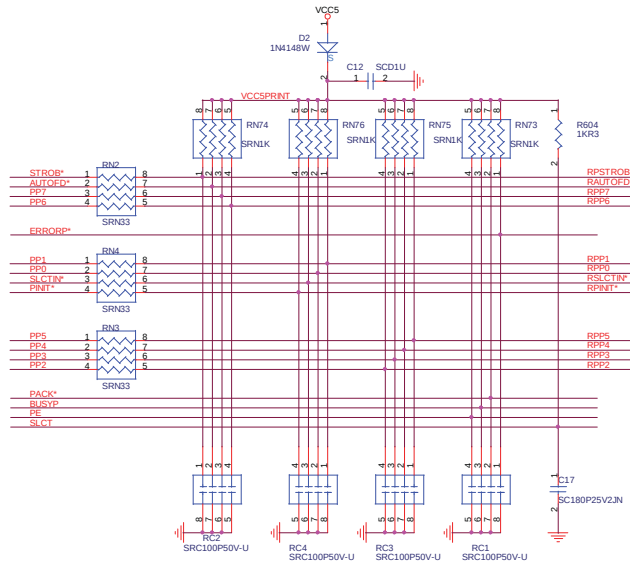
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Title: SIO DM1737 & FDD Conn			
Size	Document Number	Rev	
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Date:	Thursday, June 16, 2005	Sheet	28 of 50

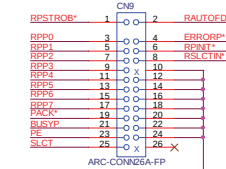


Parallel Port

28 PP0..7) PP0..7
28 STROB* STROB*
28 AUTOFD* AUTOFD*
28 ERRORP* ERRORP*
28 PNT* PNT*
28 SLCTIN* SLCTIN*
28 PACK* PACK*
28 BUSYP* BUSYP*
28 PE PE
28 SLCT SLCT

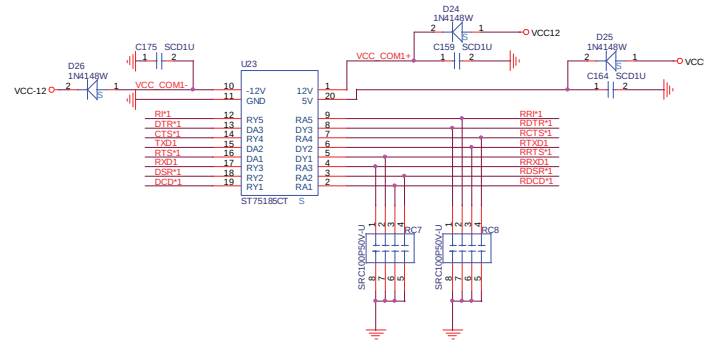


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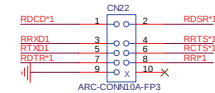


Serial Port 1

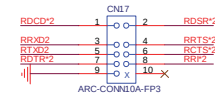
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28 RP1 RP1
28 CTS*1 CTS*1
28 DTR*1 DTR*1
28 RTS*1 RTS*1
28 DSR*1 DSR*1
28 TXD1 TXD1
28 RXD1 RXD1



COM1 Header

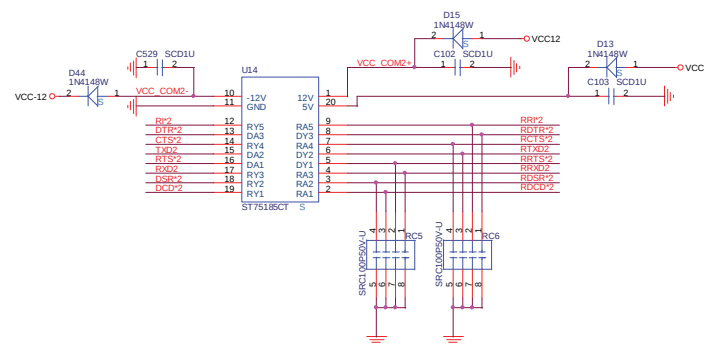


COM2 Header



Serial Port 2

28 DCD*2 DCD*2
28 RP2 RP2
28 CTS*2 CTS*2
28 DTR*2 DTR*2
28 RTS*2 RTS*2
28 DSR*2 DSR*2
28 TXD2 TXD2
28 RXD2 RXD2

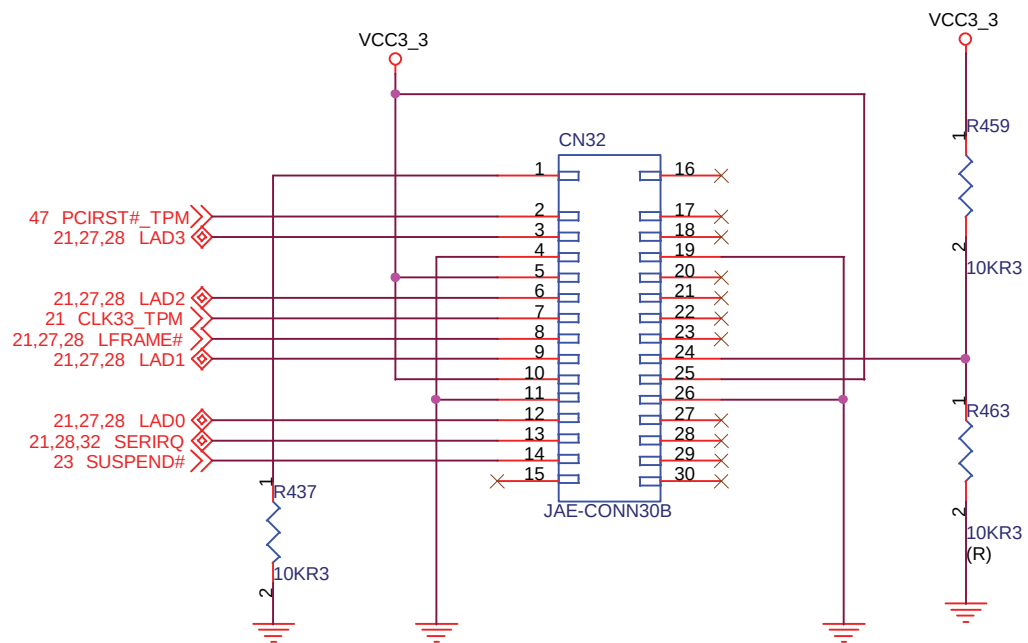


<Core Design>

wistron

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Hsichih, Taipei

COM/PRINTER PORT		
Size	Document Number	Rev
C	J361Y-RS482-M1573	1A
Date	Thursday, June 16, 2005	Sheet 30 of 50



<Core Design>



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Hsichih, Taipei

Title

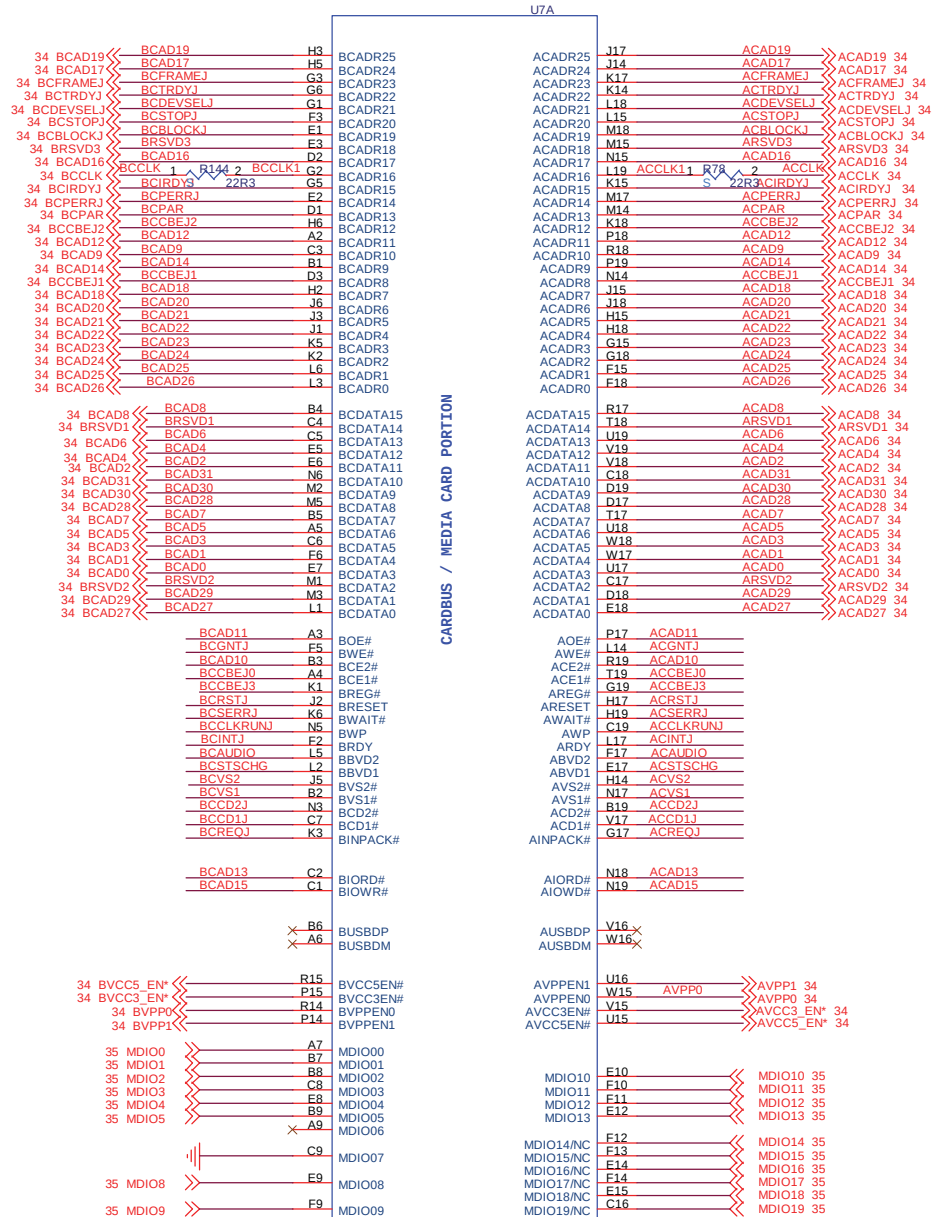
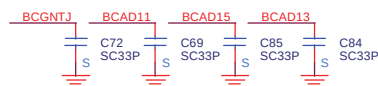
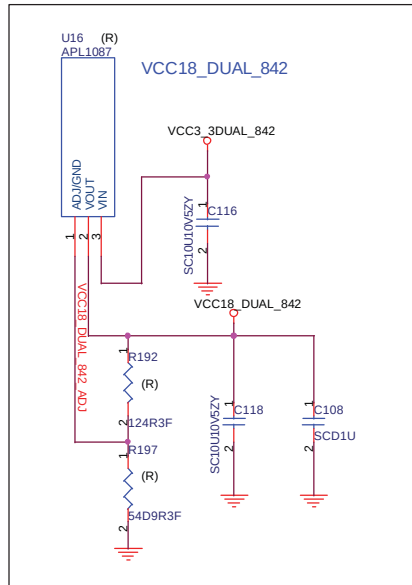
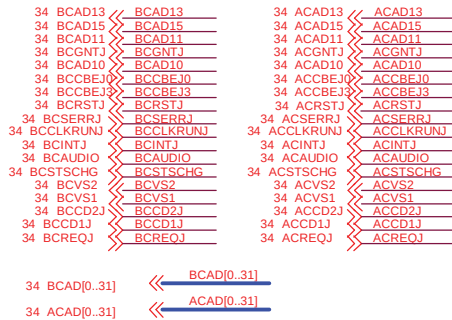
TPM Header

Size
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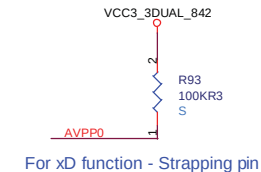
Document Number
J361Y RS482+M1573

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1A

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R5C842-1-GP

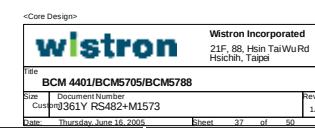


For xD function - Strapping pin

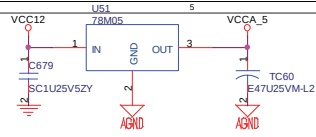
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		Title Ricoh R5C842-MDIO I/F and CB I/F	
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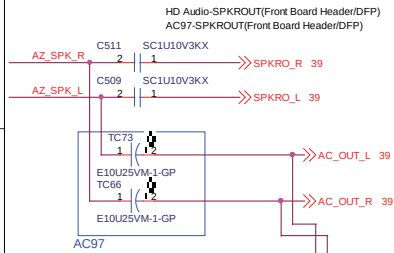


PREQJ4/PGNTJ4
IDSEL:AD22
PIRQJF

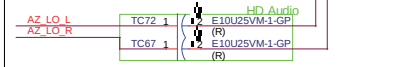
AC97 Audio Codec :ALC250/ALC655 HD Audio Codec: ALC260/ALC880



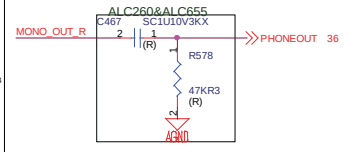
Pin 35,36 :
AC97->HPOUT/SPKOUT/LINEOUT
HD_Audio->SPKROUT



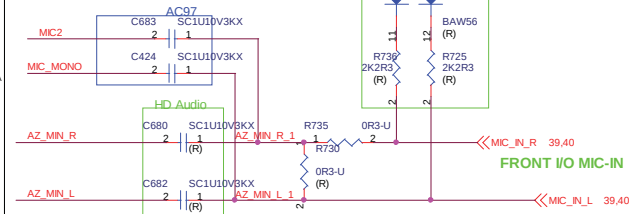
Pin 39,41 : HD_Audio->LineOUT(REAR)



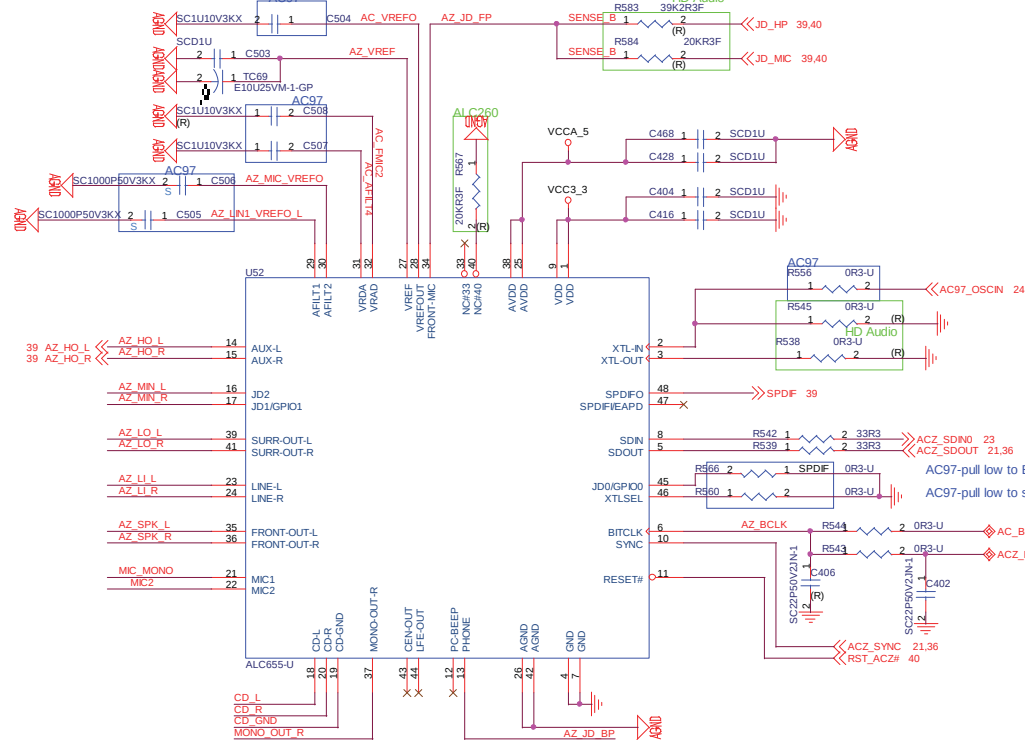
Pin 37 : Riser PHONEOUT



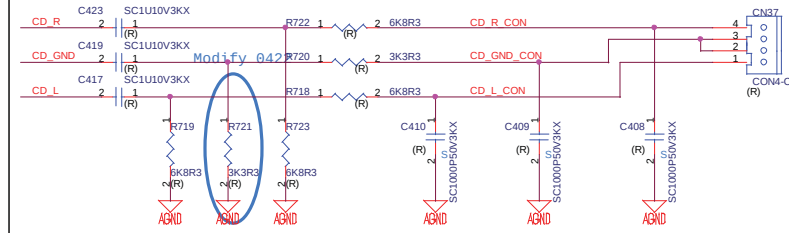
Pin 16,17 :HD_Audio->MIC2 IN



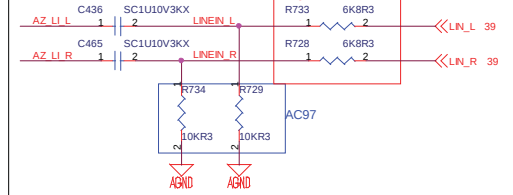
Pin 34 : HD_Audio->SENSEB



Pin 18,19,20 : CD-in

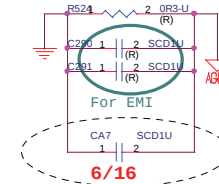
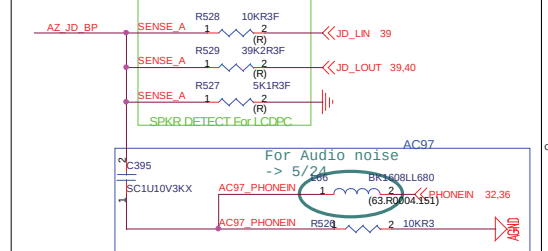


Pin 23,24 : LINE_IN(REAR)



Pin 13 :
AC97->PHONEIN

HD_Audio->SENSE A



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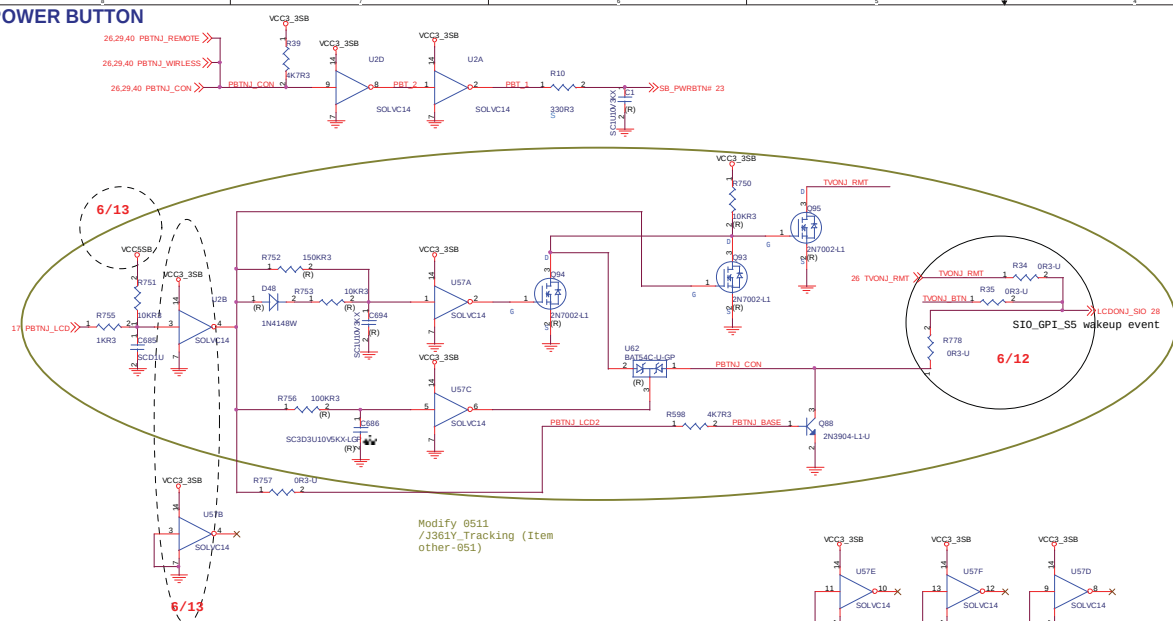
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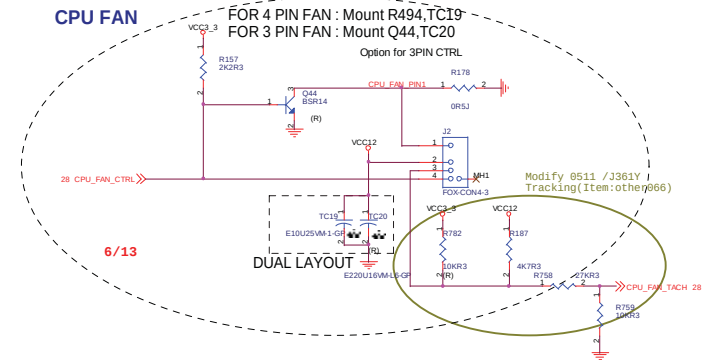
AC97



POWER BUTTON

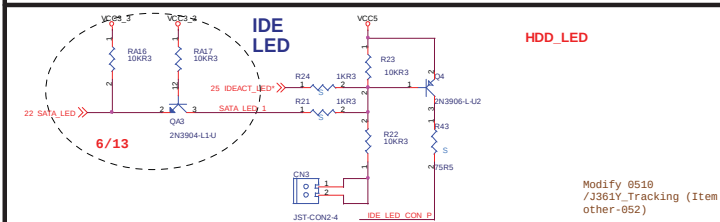


CPU FAN



IDE LED

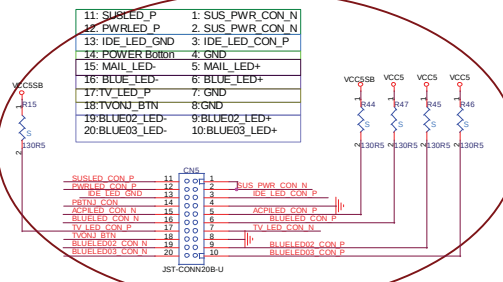
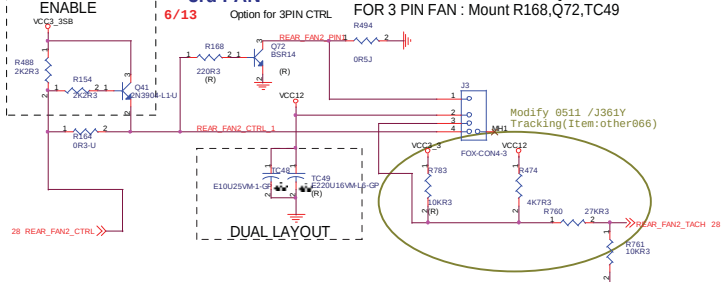
HDD_LED



SMBUS ADD ENABLE

3rd FAN

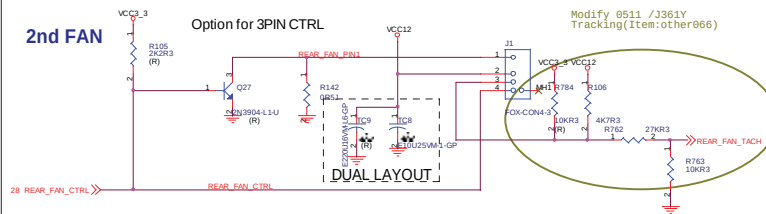
FOR 4 PIN FAN : Mount R154,Q41,TC48,R178,R164
FOR 3 PIN FAN : Mount R168,Q72,TC49



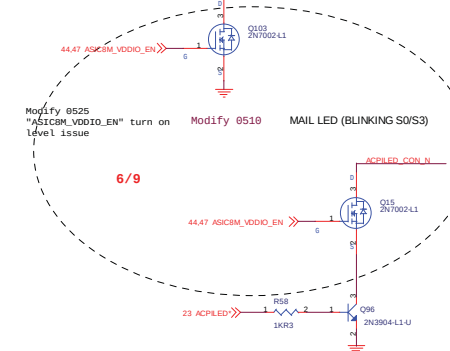
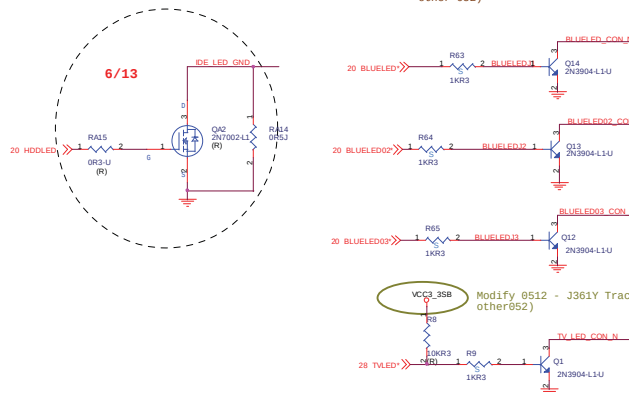
2nd FAN

Option for 3PIN CTRL

Modify 0511 /J361Y Tracking(Item:other966)

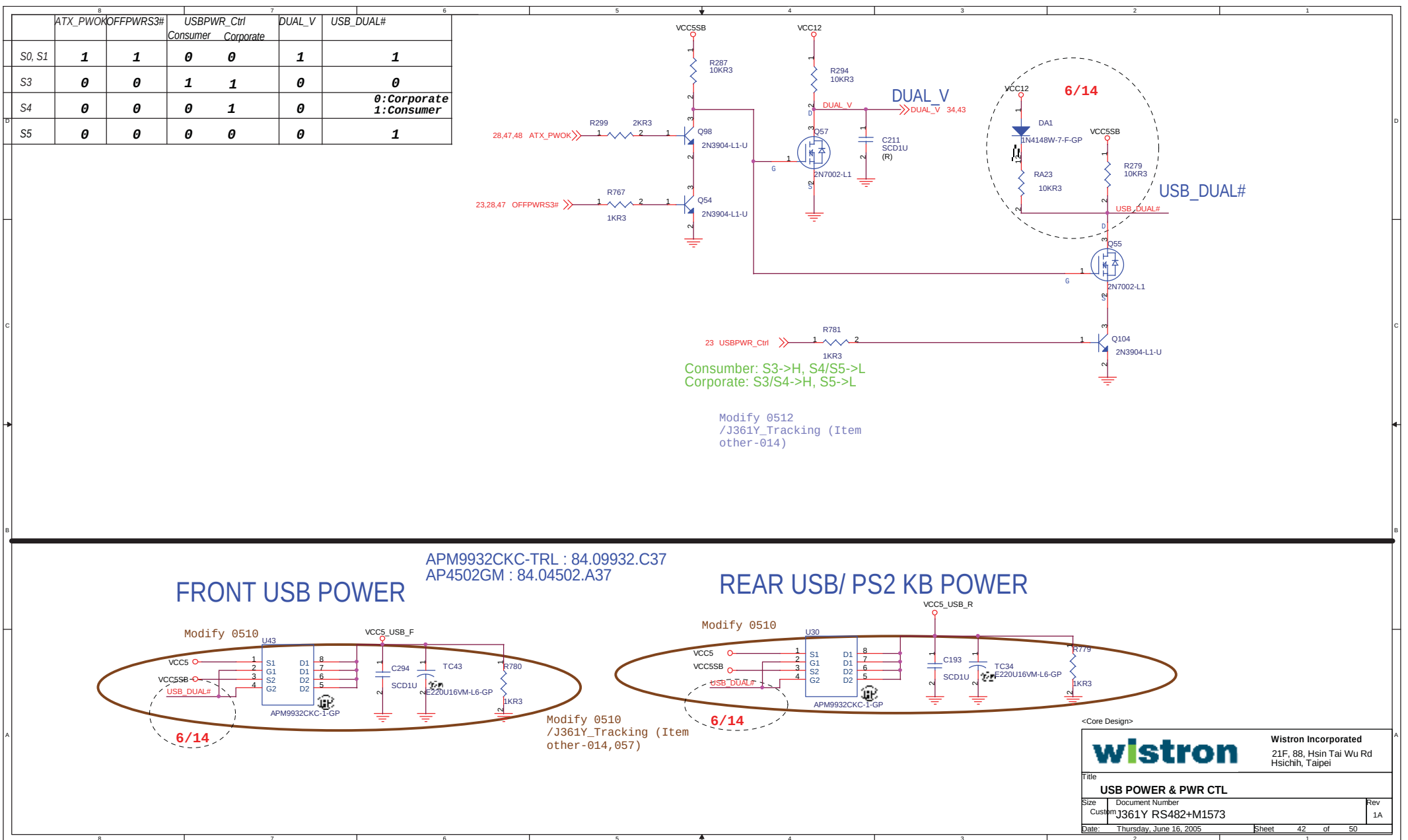


FOR 4 PIN FAN : Mount R142,TC8
FOR 3 PIN FAN : Mount R105, Q27,TC9

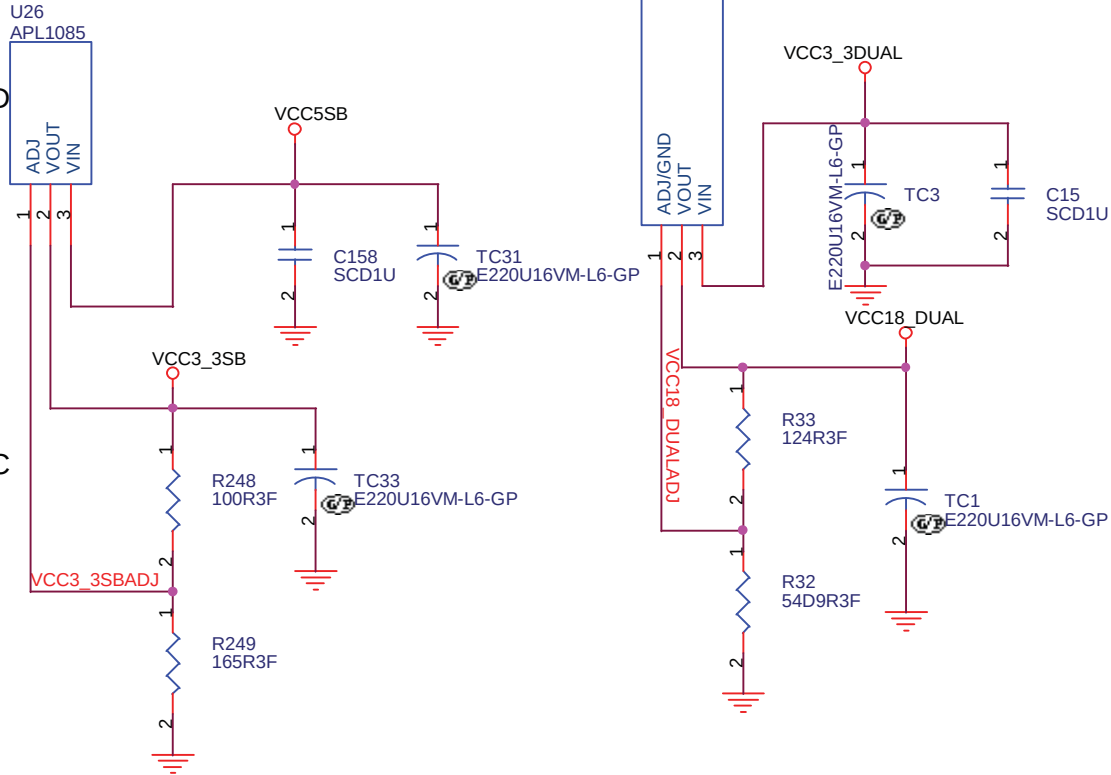


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File		21F_88_Hsin Tai Wu R3	
Size		Hsichih, Taipei	
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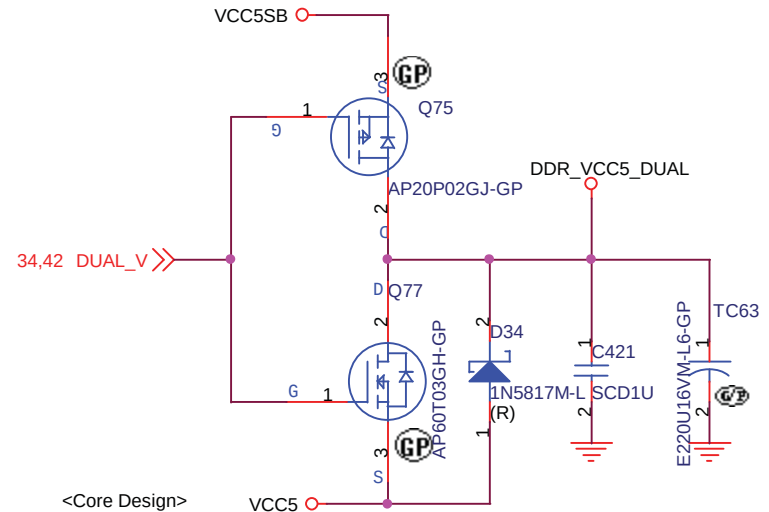


VCC3_3SB



VCC1.8_DUAL for SB Resume Power

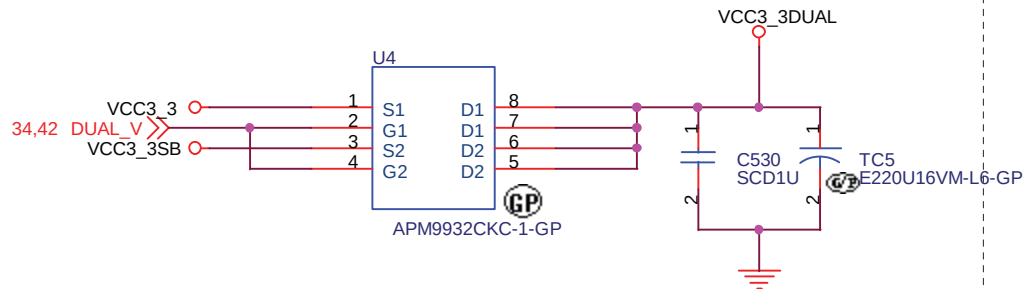
DDR_VCC5_DUAL FOR DDR & Card bus



VCC3 3 DUAL

APM9932CKC-TRL : 84.09932.C37

AP4502GM : 84.04502.A37



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Hsichih, Taipei

Title

Dual 5V, 3.3V, 1.8V, and 3.3VSB

Size

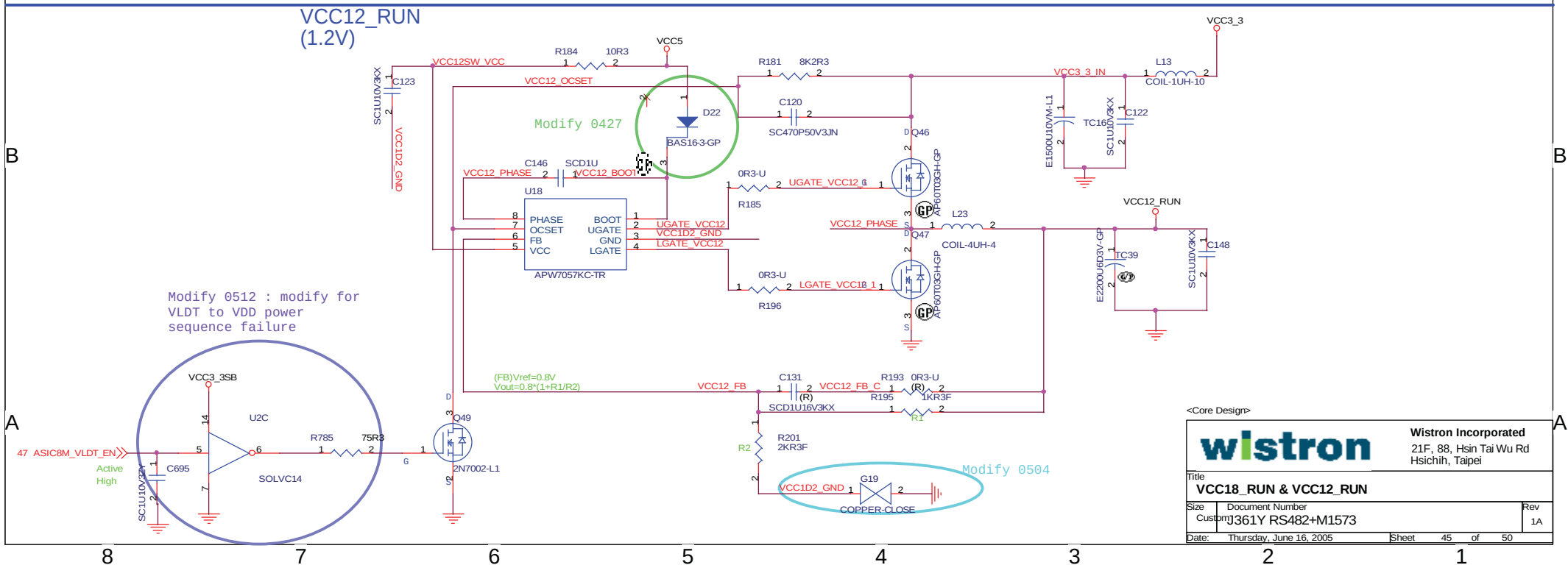
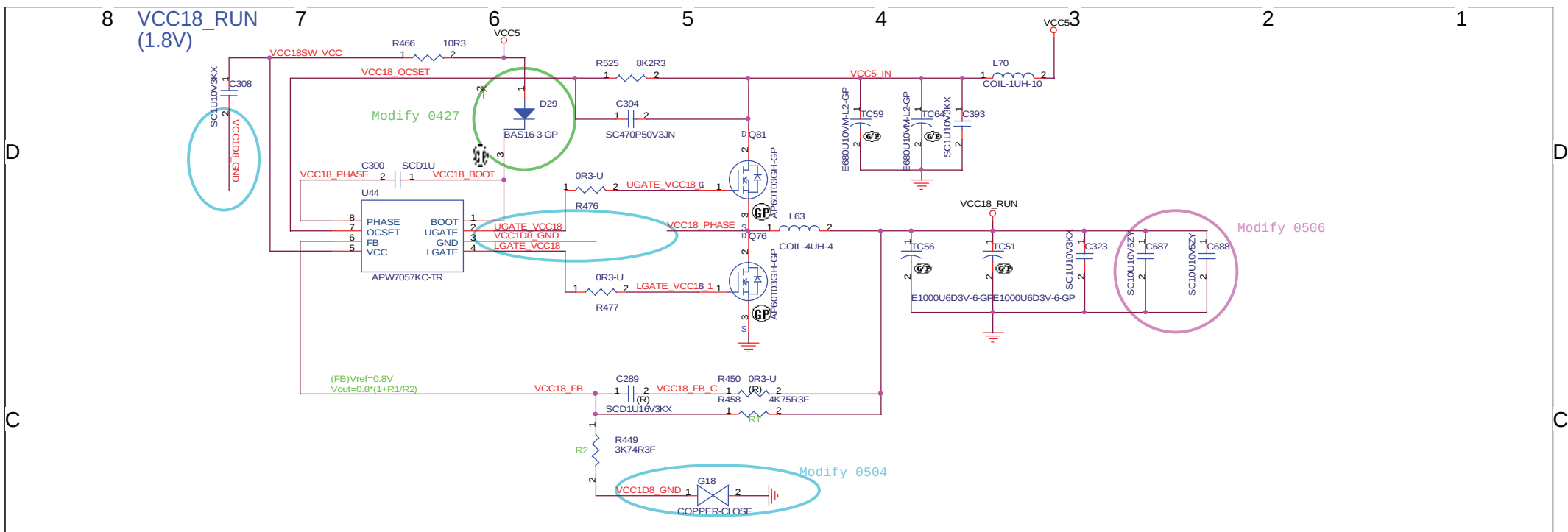
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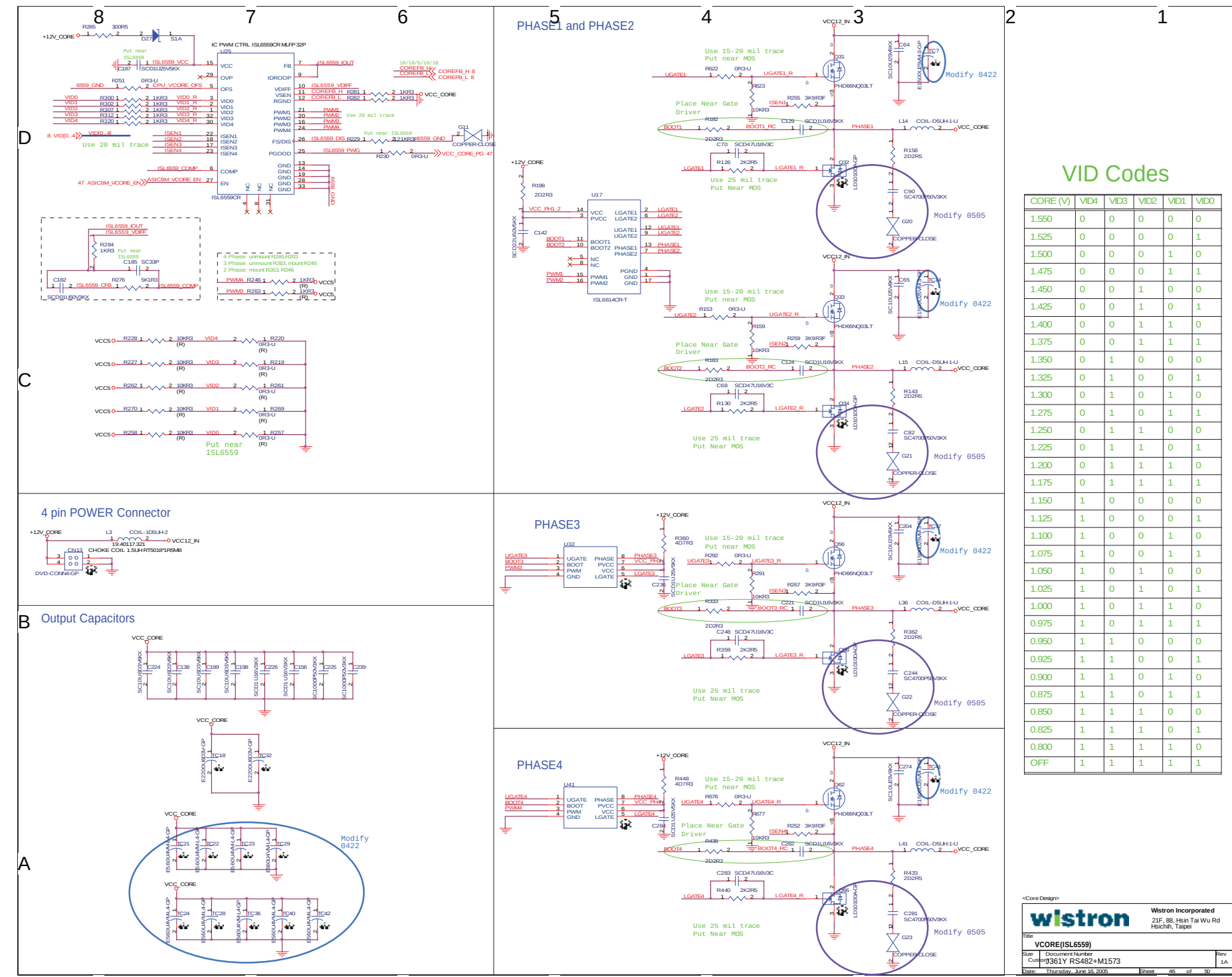
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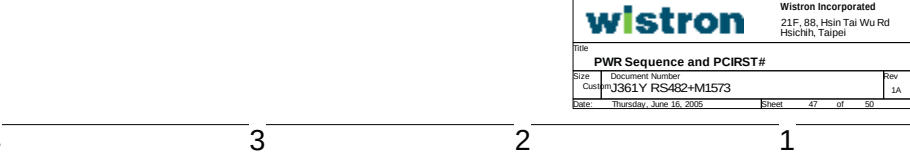
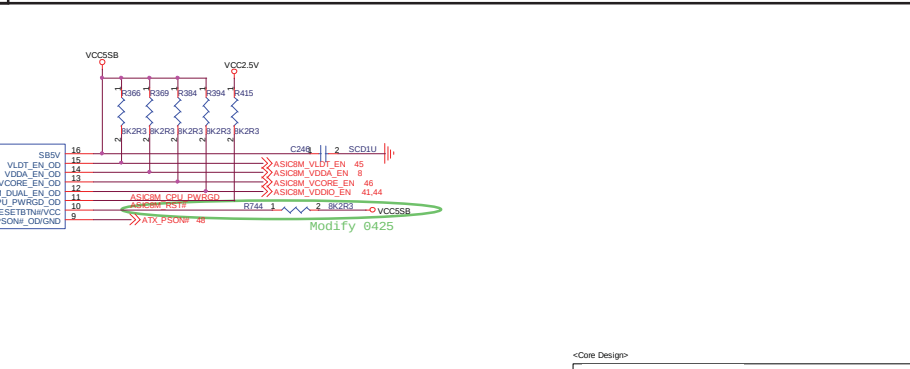
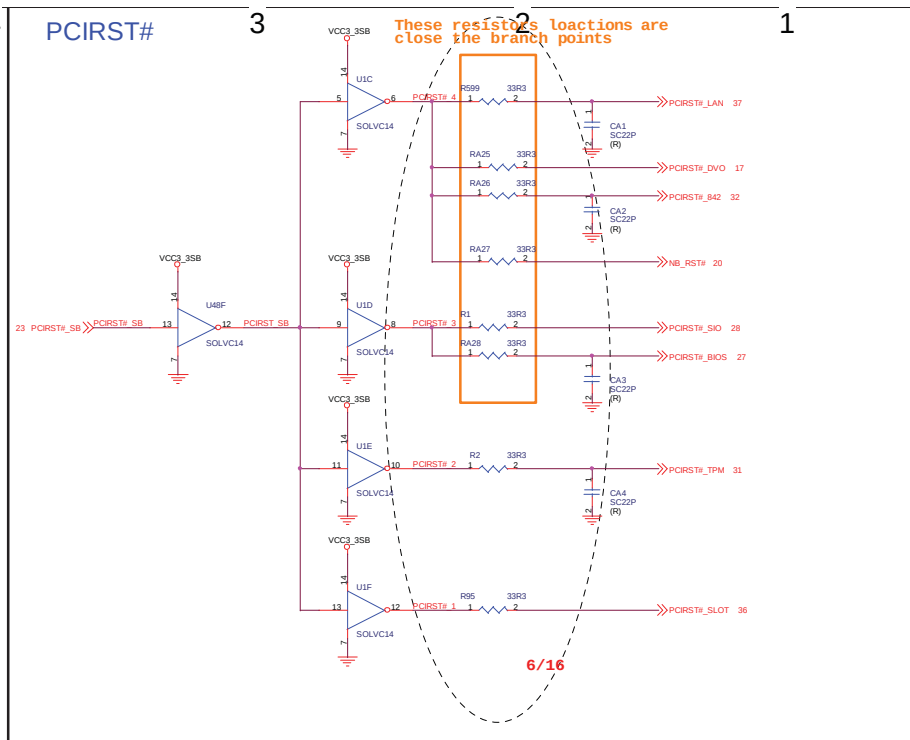
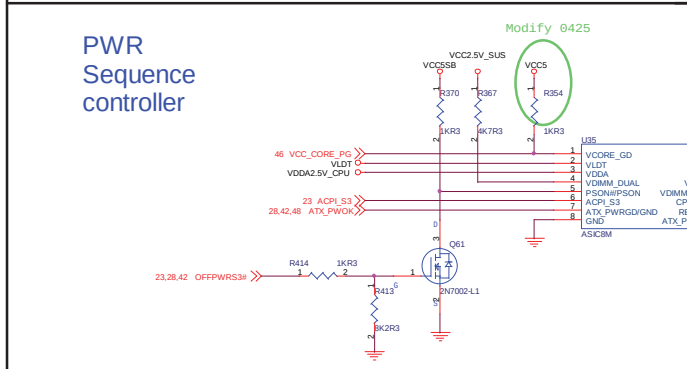
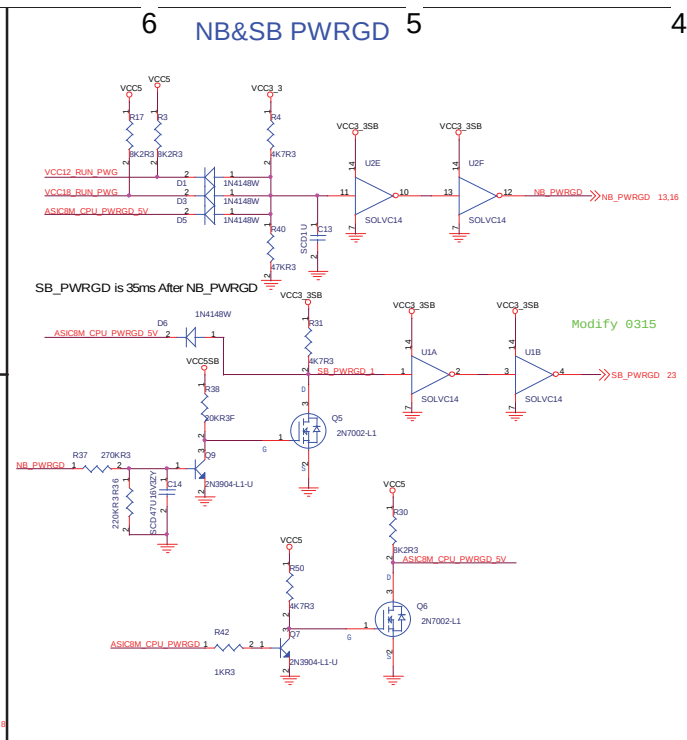
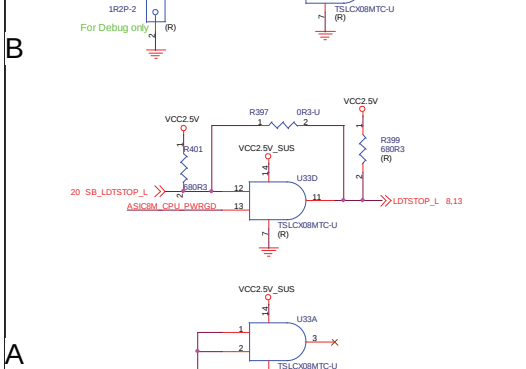
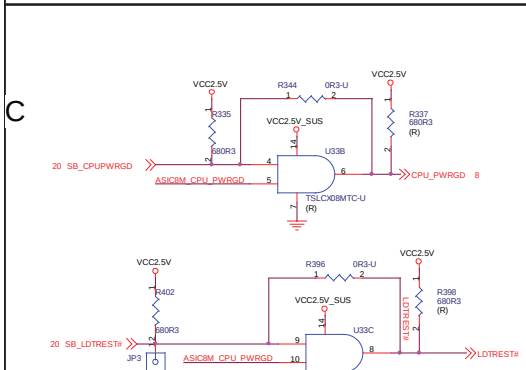
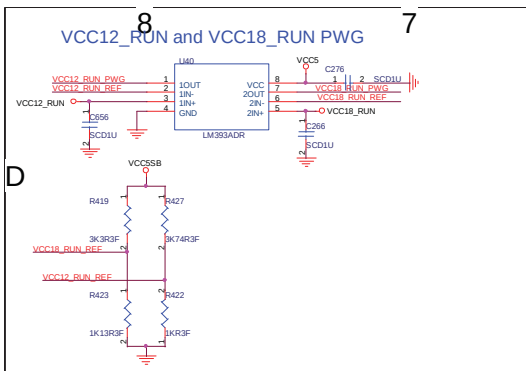
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ATX PWR CONN

ATX 24Pin Power Plane Schematic:

- Power Planes:** VCC12, VCC5, VCC3_3, VCC5SB, VCC-12, VCC3_3.
- Decoupling Capacitors:**
 - C32, C63, C57, C58, C59, C287, C31 (SCD1U).
 - TC4, TC6, TC11 (E1000U6D3V-6-GP).
- Connectors:**
 - CN14 (FOX-CONN24F-1-U):** 24-pin connector with pins 1-12 connected to VCC12, VCC5, VCC3_3, VCC5SB, VCC-12, VCC3_3, and pins 13-24 connected to VCC5SB, VCC-12, VCC3_3, VCC5, VCC12, VCC5.
 - CNA2 (DAVID-CONN20B-GP consumer):** 20-pin connector with pins 1-10 connected to VCC12, VCC5, VCC3_3, VCC5SB, VCC-12, VCC3_3, and pins 11-20 connected to VCC5SB, VCC-12, VCC3_3, VCC5, VCC12, VCC5.
- ATX PWR CONN Pinout:**
 - PIN 1: VCC12
 - PIN 2: VCC5
 - PIN 3: VCC3_3
 - PIN 4: VCC5SB
 - PIN 5: VCC-12
 - PIN 6: VCC3_3
 - PIN 7: VCC12
 - PIN 8: VCC5
 - PIN 9: VCC3_3
 - PIN 10: VCC5SB
 - PIN 11: VCC-12
 - PIN 12: VCC3_3
 - PIN 13: VCC5SB
 - PIN 14: VCC-12
 - PIN 15: VCC3_3
 - PIN 16: VCC5
 - PIN 17: VCC12
 - PIN 18: VCC5
 - PIN 19: VCC3_3
 - PIN 20: VCC5SB
 - PIN 21: VCC-12
 - PIN 22: VCC3_3
 - PIN 23: VCC5
 - PIN 24: VCC12
- ATX PWR CONN Pinout:**
 - PIN 1: VCC12
 - PIN 2: VCC5
 - PIN 3: VCC3_3
 - PIN 4: VCC5SB
 - PIN 5: VCC-12
 - PIN 6: VCC3_3
 - PIN 7: VCC12
 - PIN 8: VCC5
 - PIN 9: VCC3_3
 - PIN 10: VCC5SB
 - PIN 11: VCC-12
 - PIN 12: VCC3_3
 - PIN 13: VCC5SB
 - PIN 14: VCC-12
 - PIN 15: VCC3_3
 - PIN 16: VCC5
 - PIN 17: VCC12
 - PIN 18: VCC5
 - PIN 19: VCC3_3
 - PIN 20: VCC5SB
 - PIN 21: VCC-12
 - PIN 22: VCC3_3
 - PIN 23: VCC5
 - PIN 24: VCC12

OVERLAP with CN14

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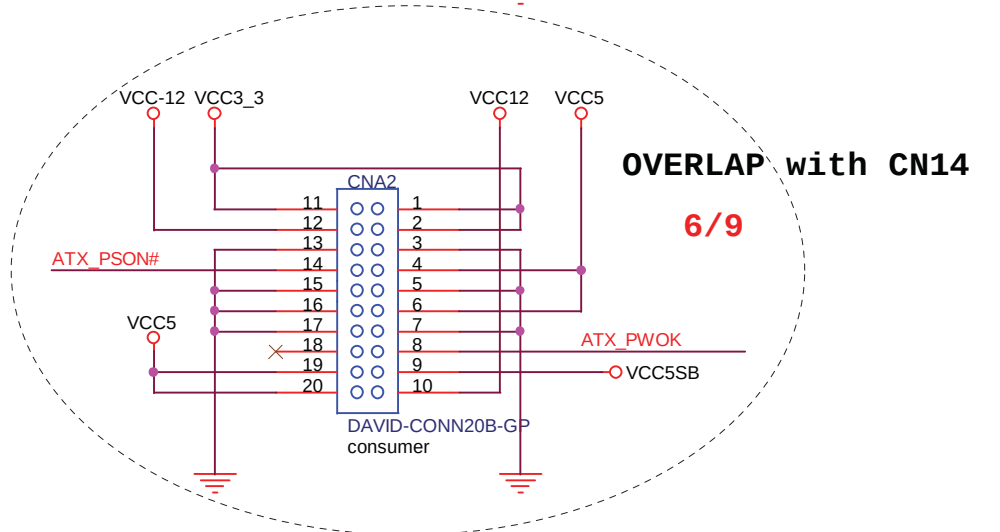
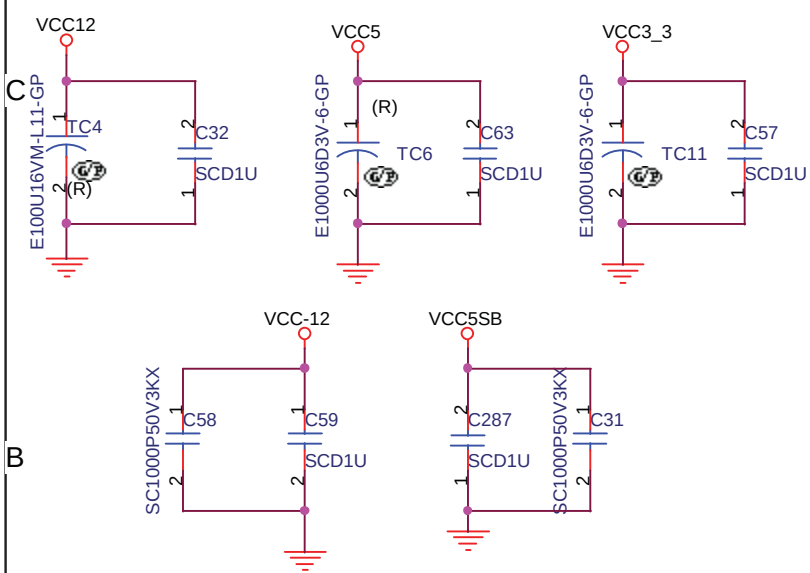
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Hsichih, Taipei

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ATX 24Pin conn

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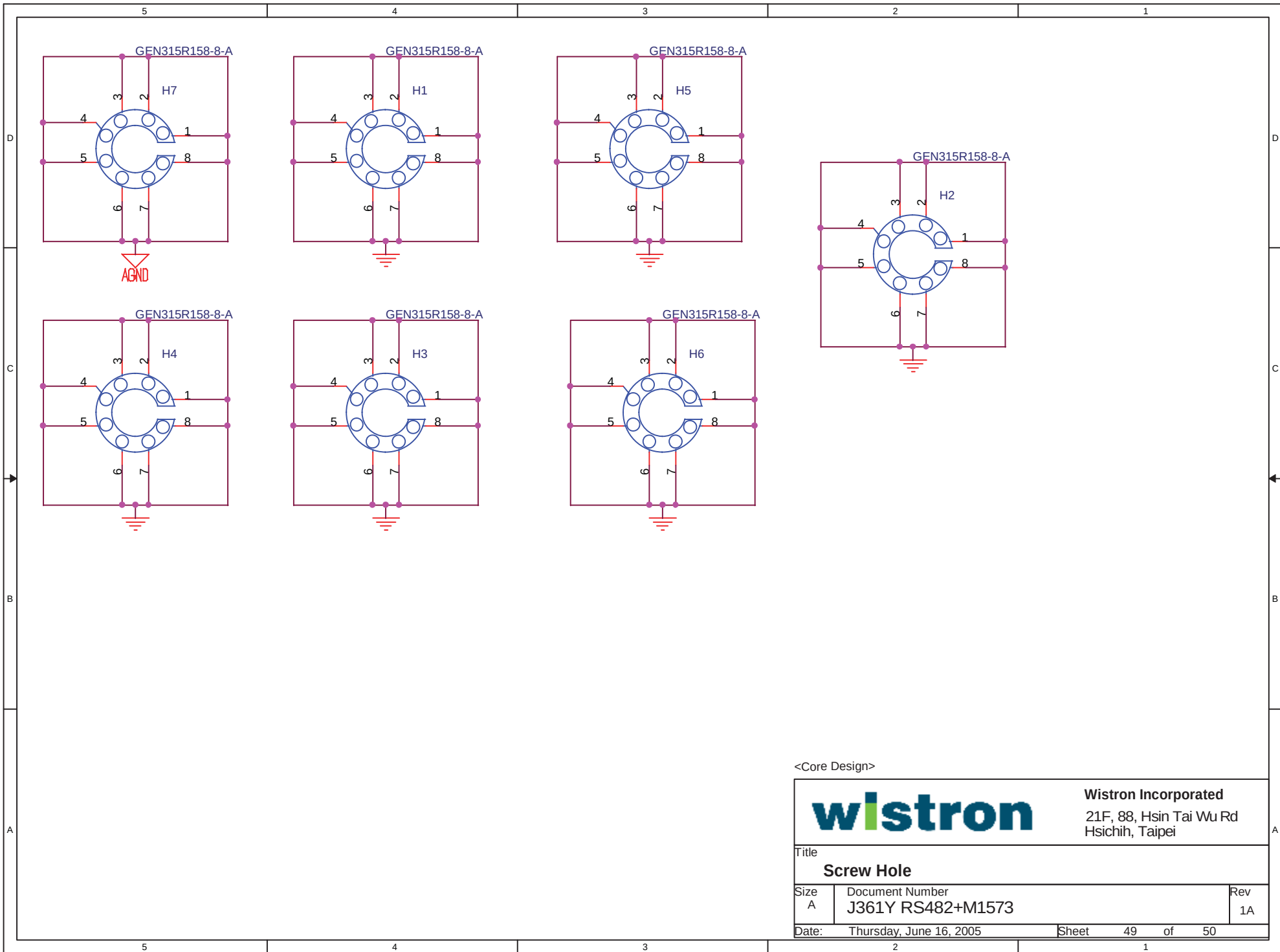
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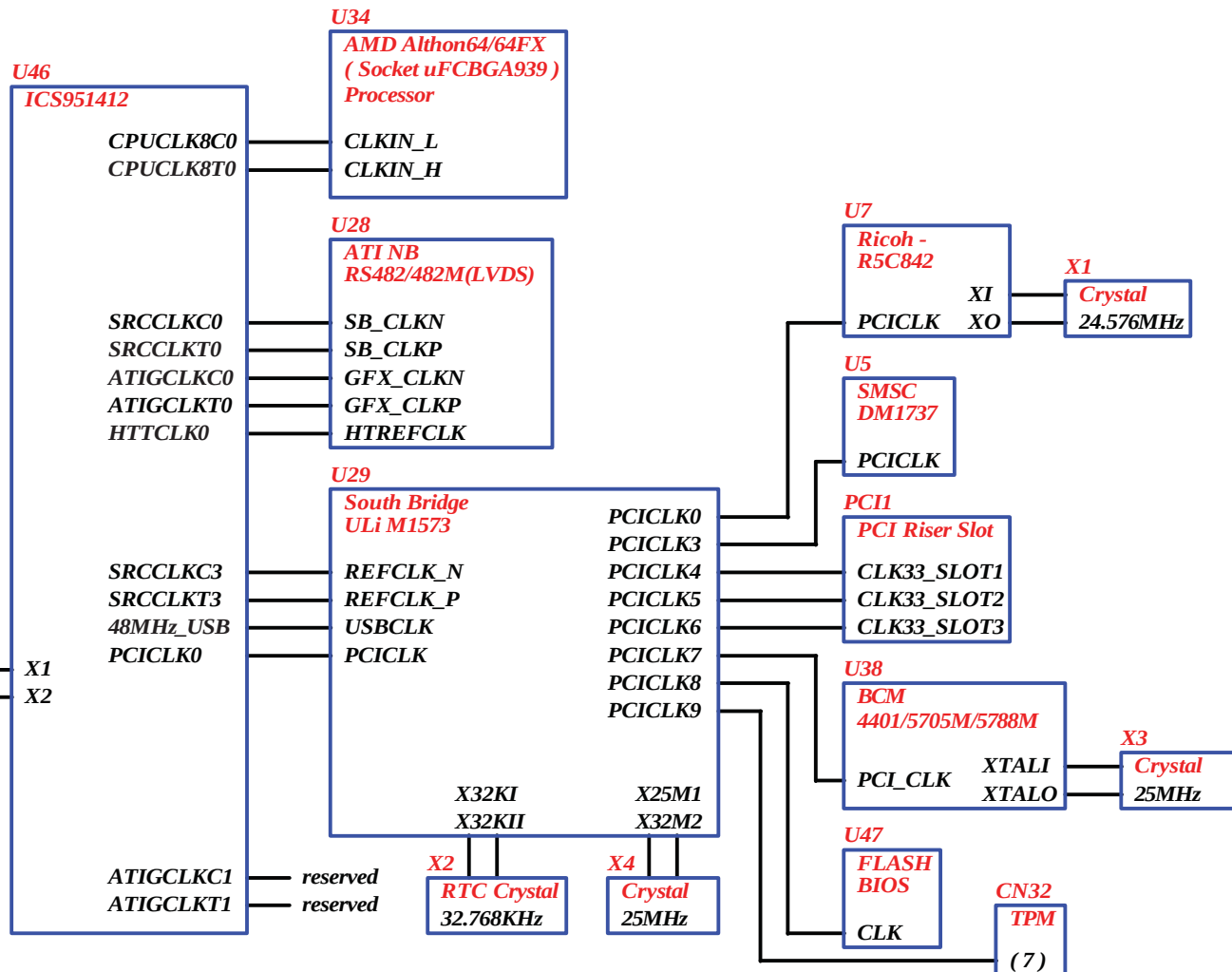


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ATX 24Pin conn			
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EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

ATIGCLK Divider Selection

ATIG_Div(3:0)	ATIGCLK(1:0) (MHz)
1 0 0 0	100.00
0 0 1 1	114.29
TBD	133.33
0 0 1 0	160.00

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CLOCK MAP

Size

Document Number

Rev

Custom

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1A

Date:

Thursday, June 16, 2005

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