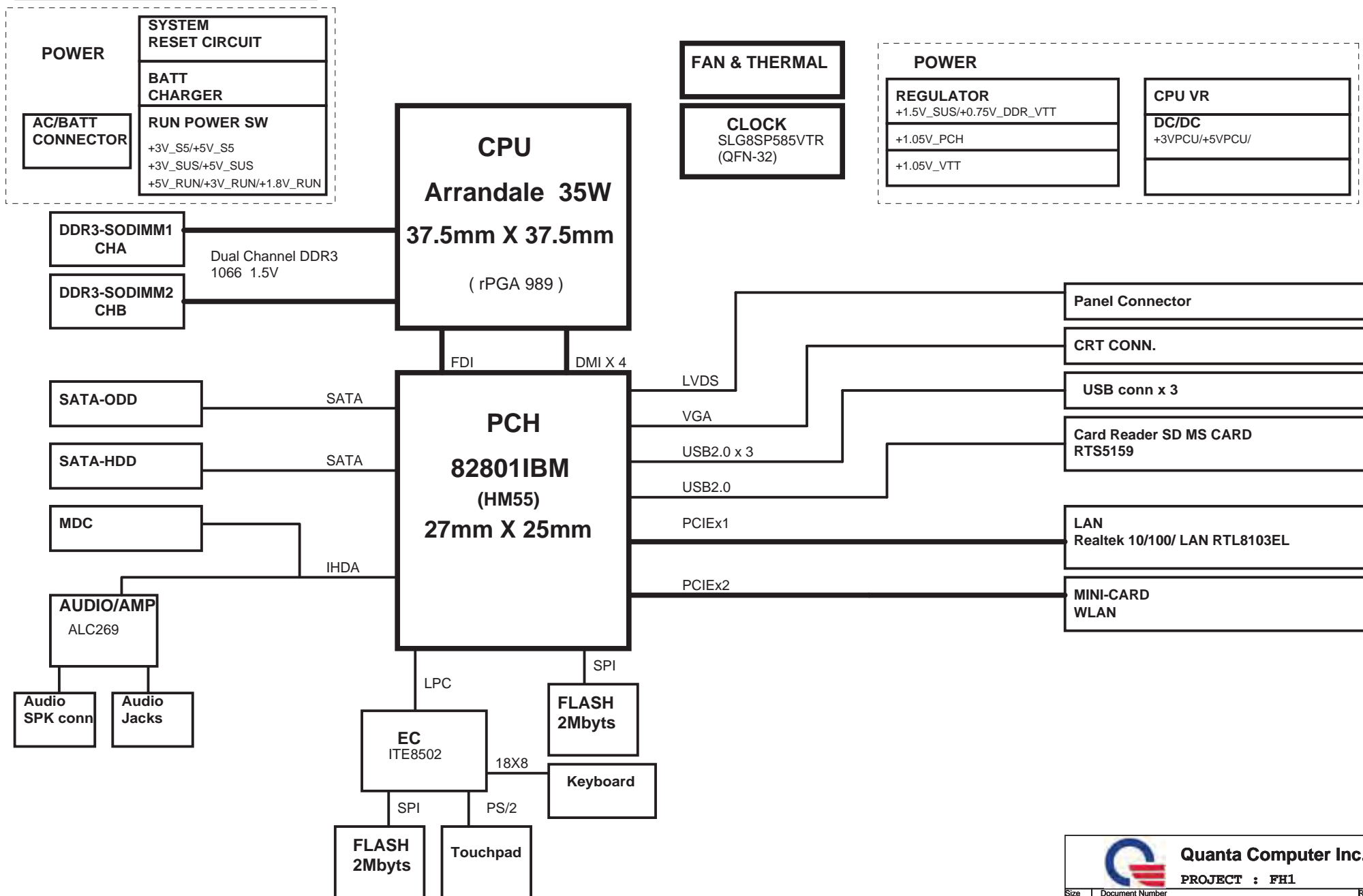


Intel Calpella BLOCK DIAGRAM

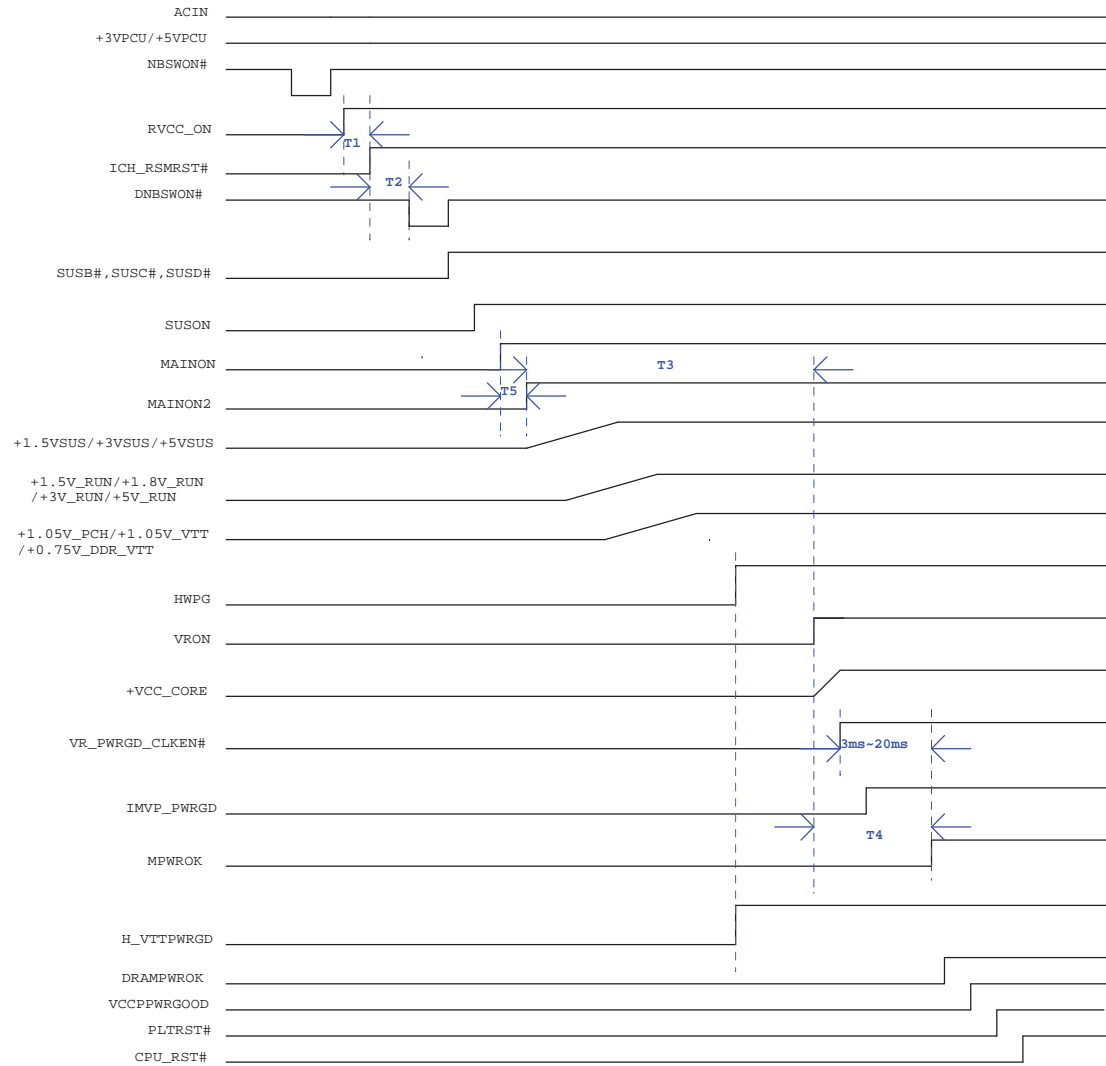
Intel Calpella Arrandale UMA

01




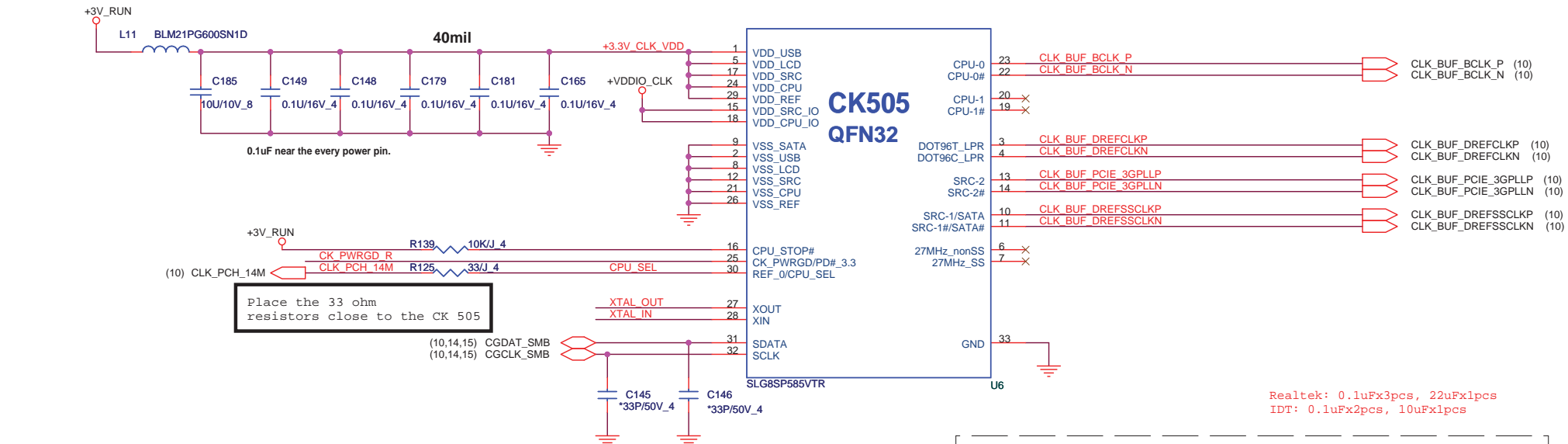
PAGE	DESCRIPTION
01	Schematic Block Diagram
02	Front Page
03	Clock Generator
04-07	Arrandale
08-13	Ibex Peak-M
14-15	DDRIII SO-DIMM(204P)
16	LCD/CCD CONN
17	CRT CONN
18	Card Reader (RTS5159)
19	LAN RTL8103EL/RJ45
20	HDD/ODD/HOLE
21	USB/BLUE TOOTH
22	MINI-Card (WLAN)/ XDP
23	KB/TOUCH PAD/LED
24	CODEC (ALC269)
25	EC_ ITE8502
26	FAN/SW CON/MDC
27	+5V/+3V (RT8206B)
28	+1.05V/+1.8V (RT8204C)
29	CPU Core (ADP3212)
30	+1.05V_VTT (VT358)
31	UMA GPU CORE (RT8152C)
32	DDR3 (RT8207)
33	DISCHARGE/3VS5/5VS5/LAN
34	CHARGER (ISL88731)
35	Clock Distribution
36	Power Tree
37	SMBUS Address

Power Sequence



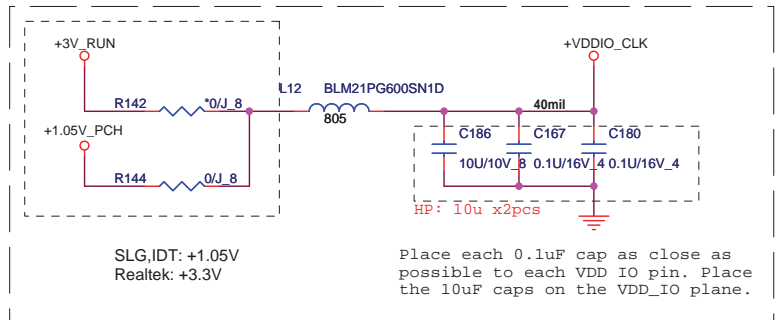
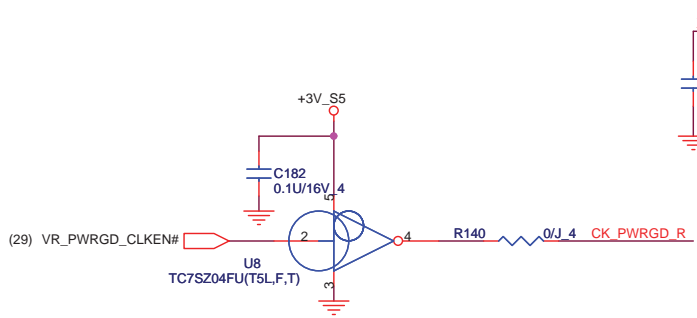
T1: RVCCON TO RSMRST# = 30ms (spec:mini 10ms)
 T2: RSMRST# TO-DNBSWON = 110ms (spec:mini 100ms)
 T3: MAINON2 TO VRON = 110ms (spec:mini 99ms)
 T4: VRON TO MPWROK = 10ms (HWPG NEED TO BE HIGH at that time)
 Note: IMVP_CLK_EN# (inverted) assertion to SYS_PWROK/PCH_PWROK assertion.
 SPEC:3ms~20ms
 T5: MAINON to MAINON2 =500us


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Place the 33 ohm resistors close to the CK 505

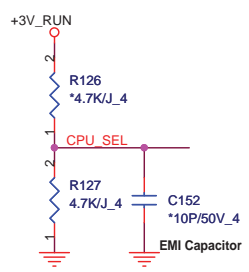
Realtek: 0.1uF x 3pcs, 22uF x 1pcs
IDT: 0.1uF x 2pcs, 10uF x 1pcs



SLG, IDT: +1.05V
Realtek: +3.3V

Place each 0.1uF cap as close as possible to each VDD IO pin. Place the 10uF caps on the VDD_IO plane.

+VDDIO_CLK:
SLG date sheet (V0.2) P15: Min 1.05V, Max 3.465V.
Realtek date sheet (V1.2) P11: Min 1.05V, Max 3.3V.
IDT date sheet (V0.7) P10: Min 0.9975V, Max 3.465V.

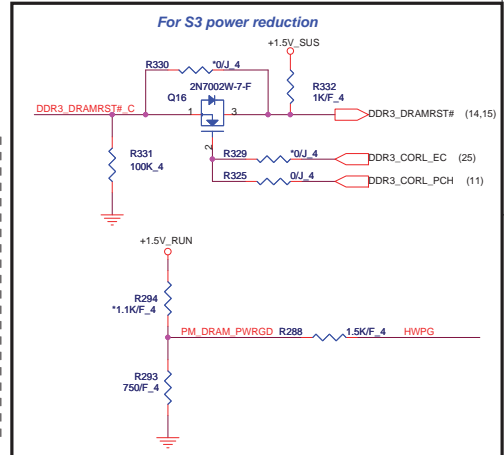
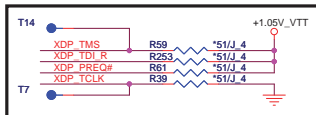
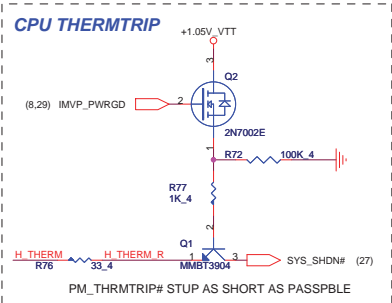
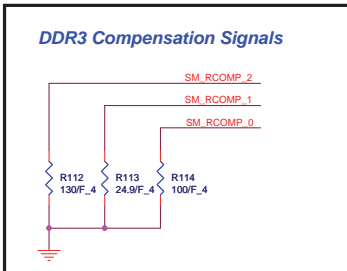
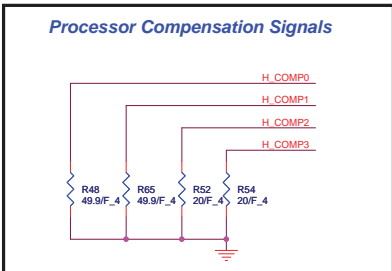
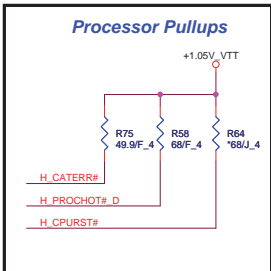
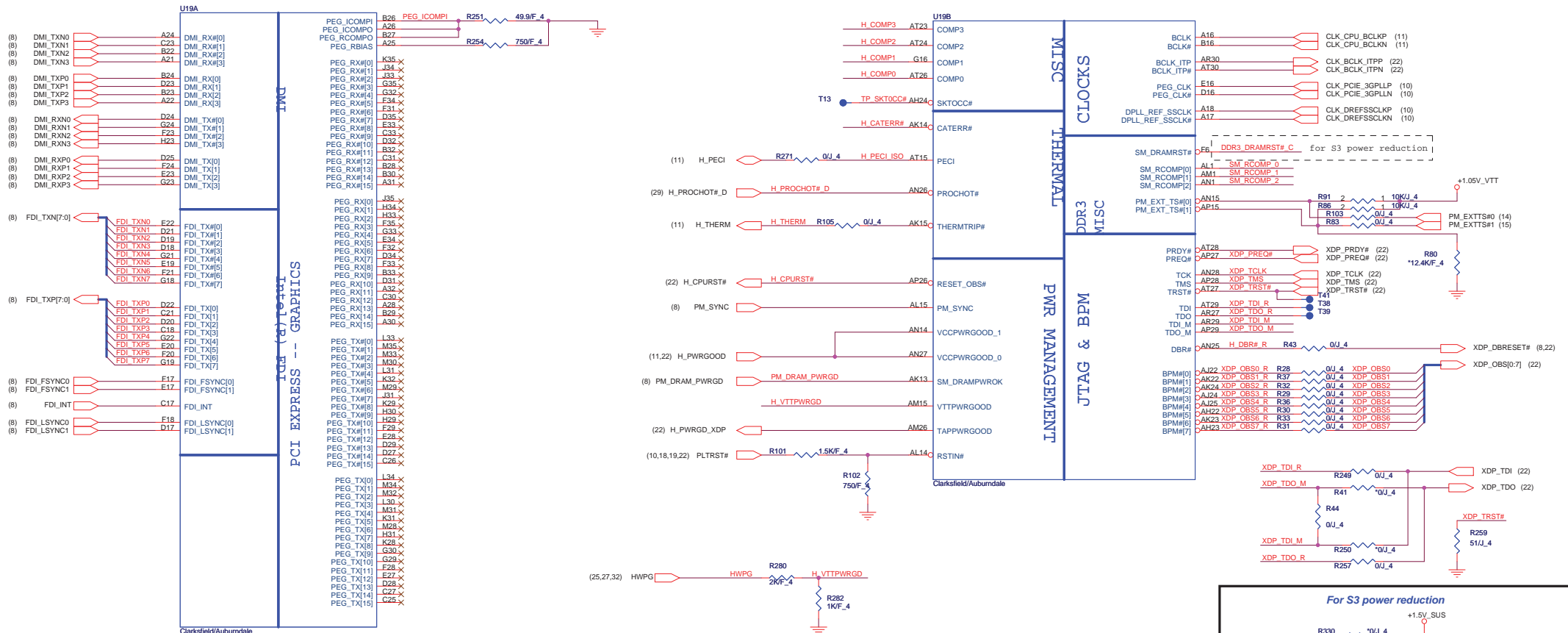


PIN 30	CPU_0	CPU_1
0 (default)	133MHz	133MHz
1 (0.7V-1.5V)	100MHz	100MHz

CPU_SEL:
SLG date sheet (V0.2) P15:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
Realtek date sheet (V1.2) P11:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
IDT date sheet (V0.7) P10:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.

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Size	Document Number	Rev 1A
Clock Generator		
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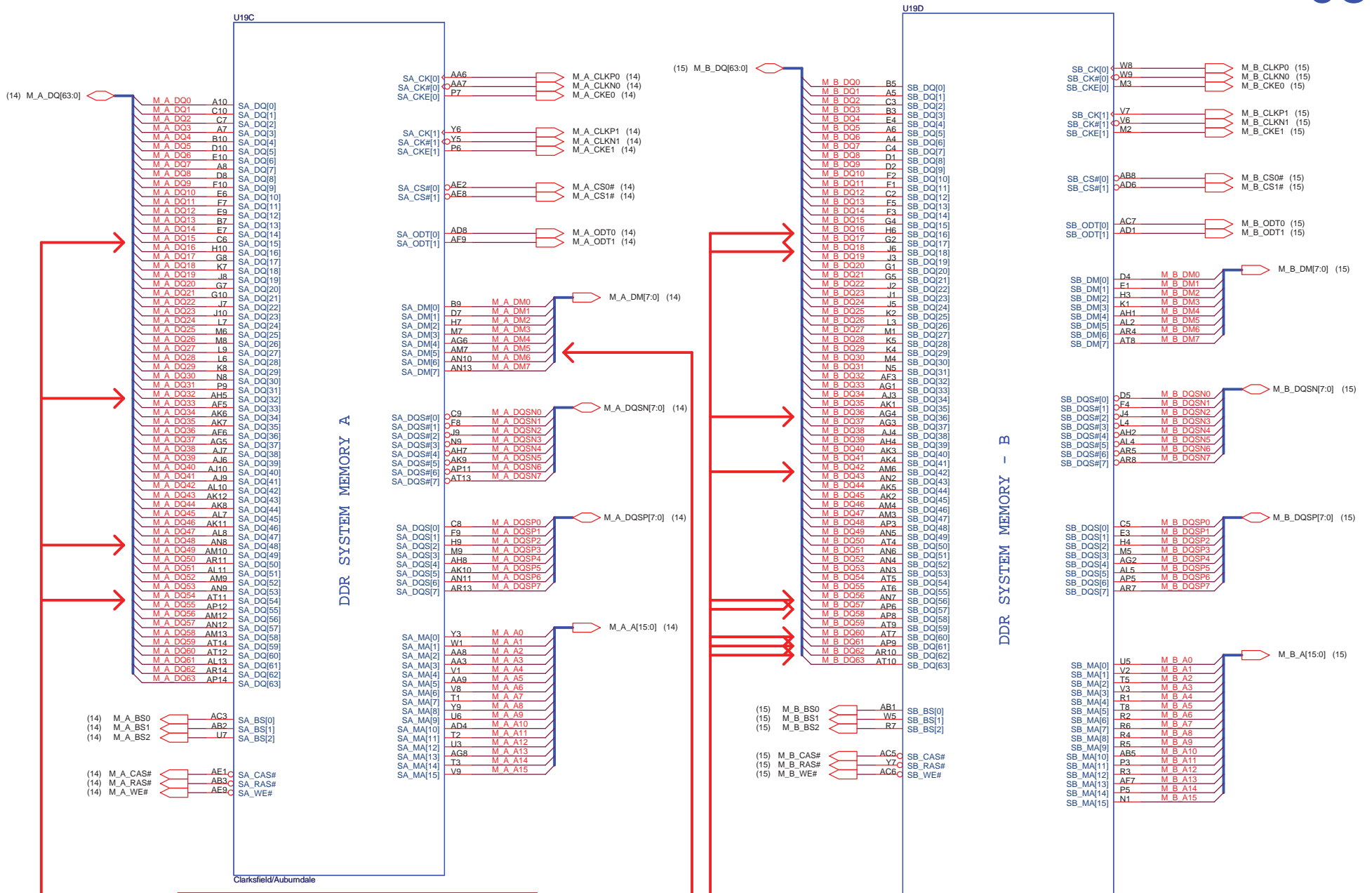


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	ARRANDALE I/4	1A
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ARRANDALE PROCESSOR (DDR3)

05



Channel A DQ[15,32,48,54], DM[5]
Requires minimum 12mils spacing
with all other signals, including data signals.

Channel B DQ[16,18,36,42,56,57,60,61,62]
Requires minimum 12mils spacing
with all other signals, including data signals.

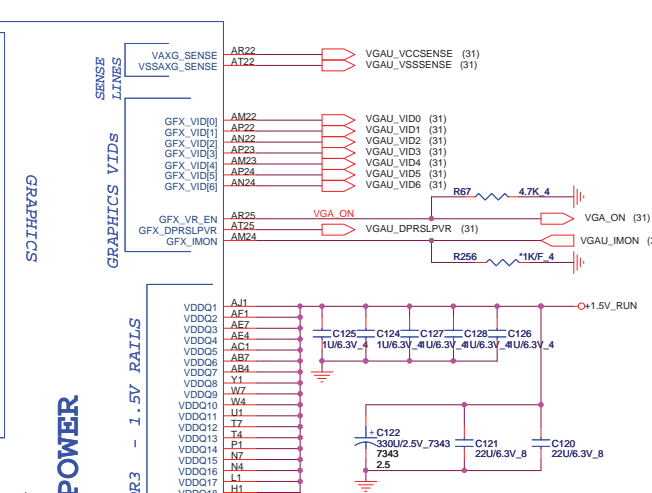
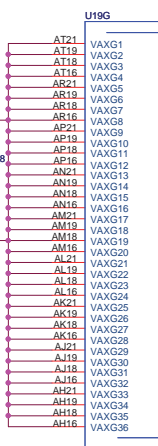
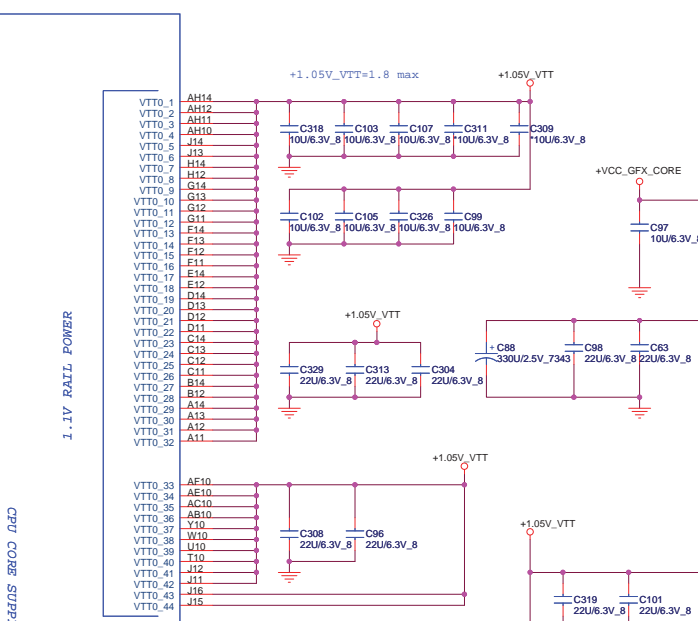
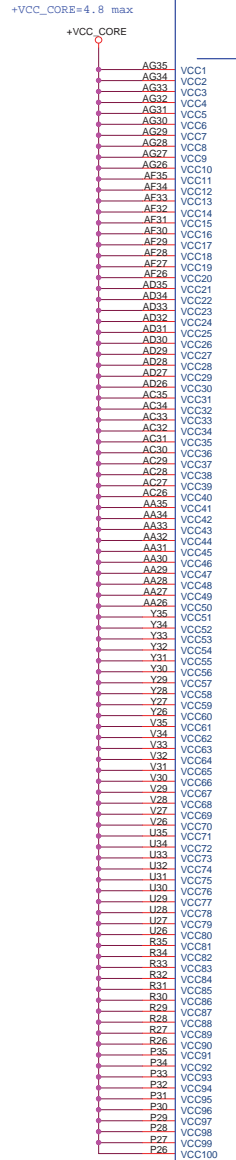
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PROJECT : FHL

Size Document Number
ARRANDALE 2/4 Rev 1A

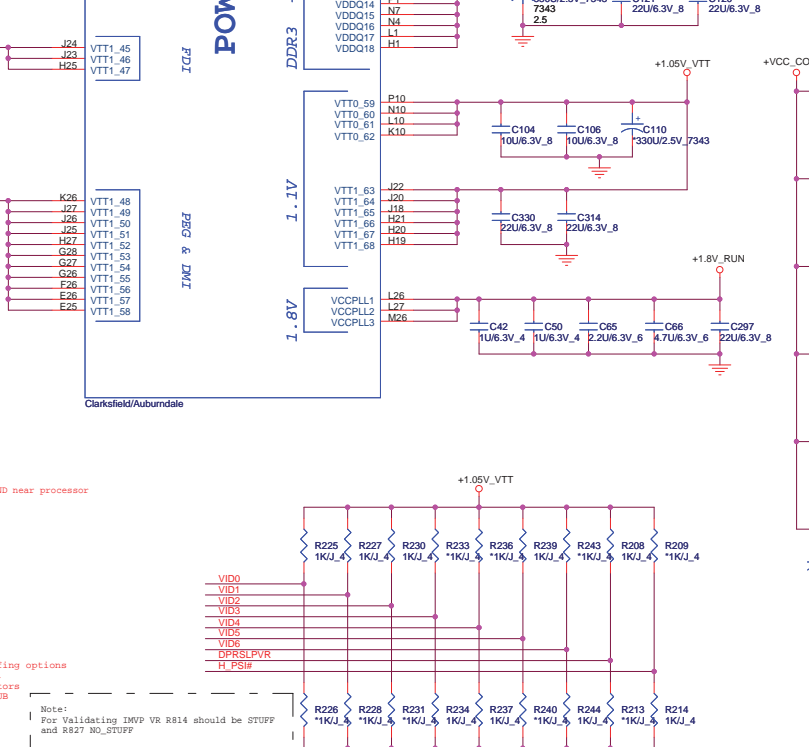
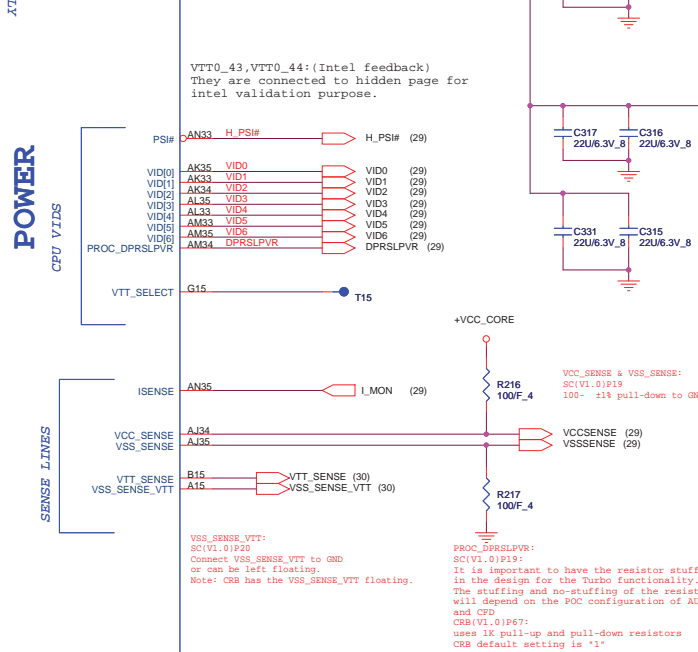
Date: Friday, October 05, 2009 Sheet 5 of 37

ARRANDALE PROCESSOR (GRAPHICS POWER)

CPU Core Power



For S3 power reduction
 Check to ensure that 4 switching caps per SODIMM connector between SODIMM 1.5V and GND are placed as close as possible to the connectors - caps should be evenly distributed between the connectors



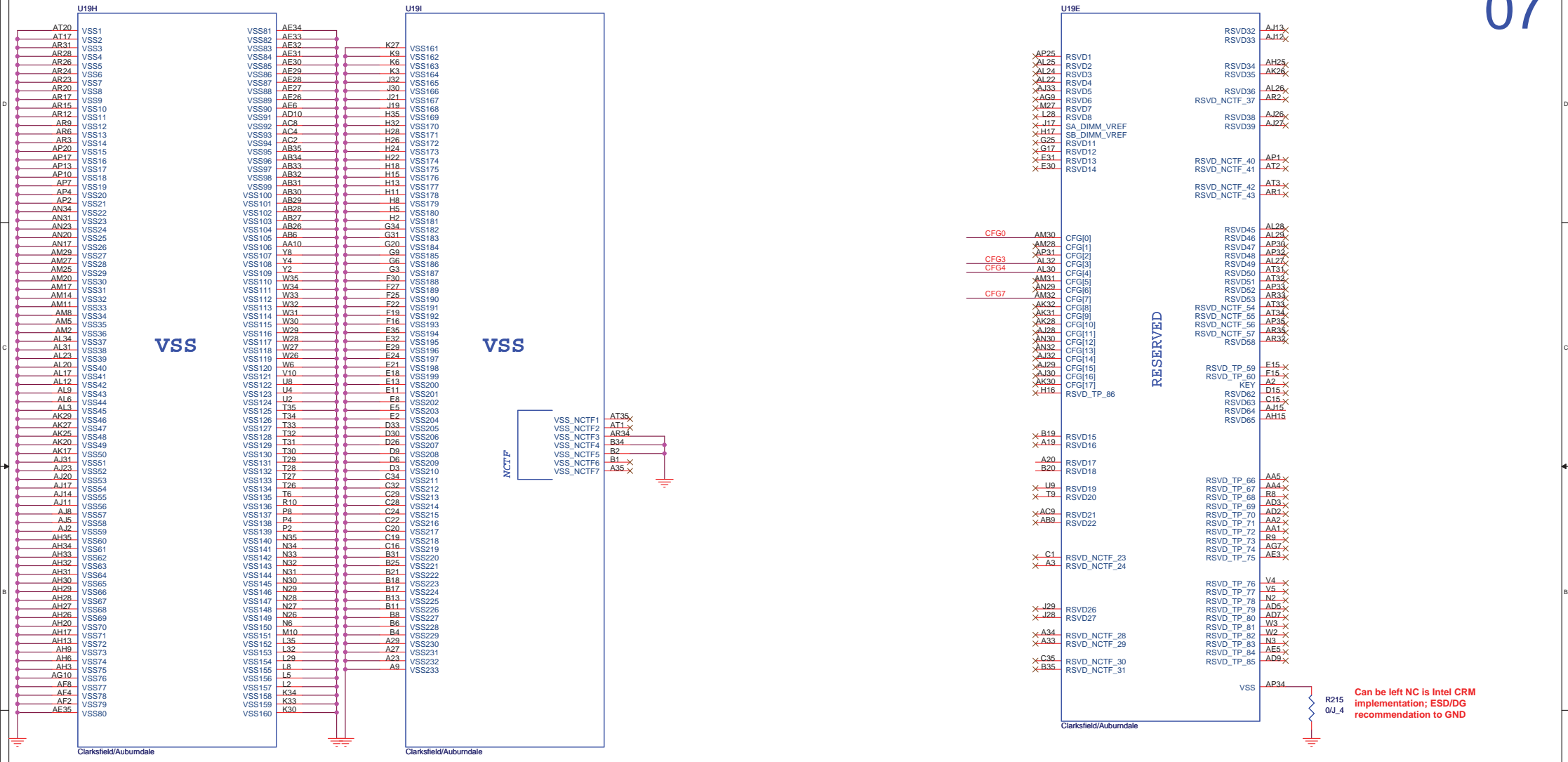
AUBURDALE/CLARKSFIELD PROCESSOR (POWER)

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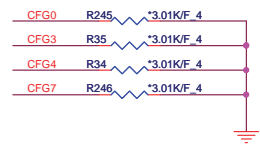
Size	Document Number	Rev
	ARRANDALE 3/4	1A
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ARRANDALE PROCESSOR (GND)

ARRANDALE PROCESSOR (RESERVED, CFG)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.



	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

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PROJECT : FH1

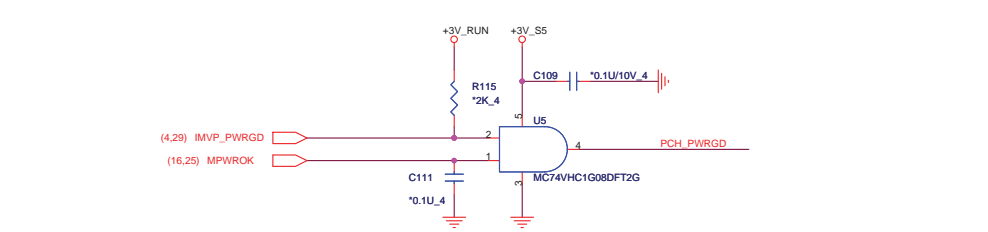
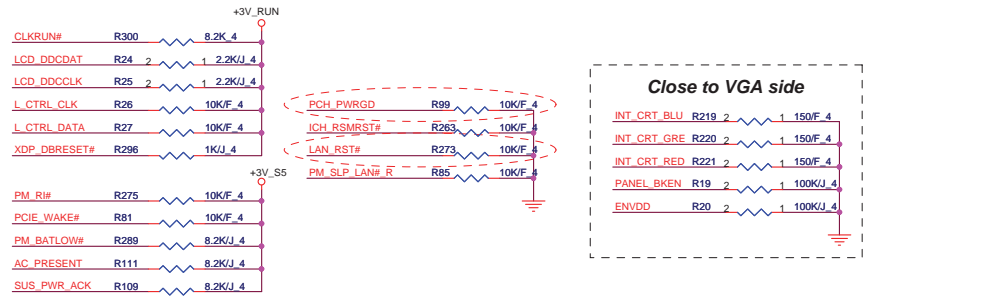
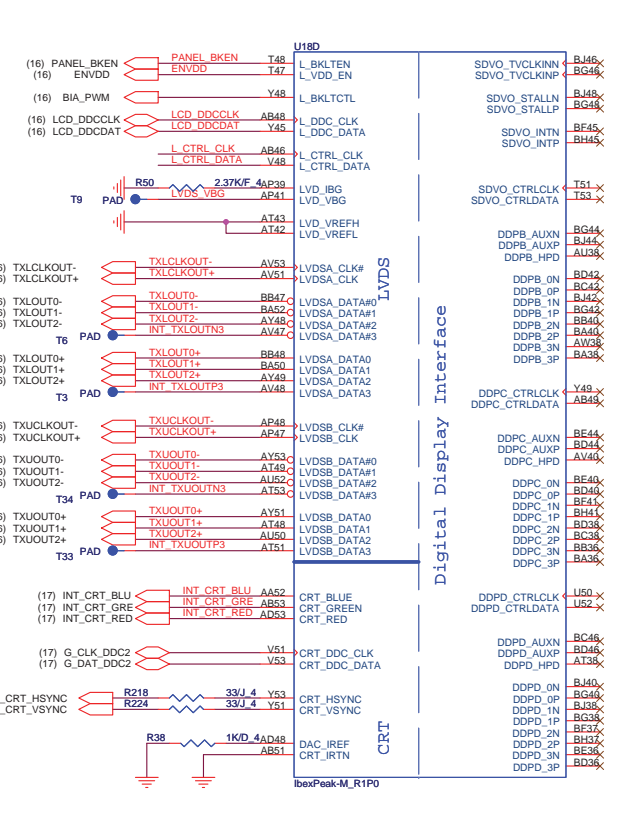
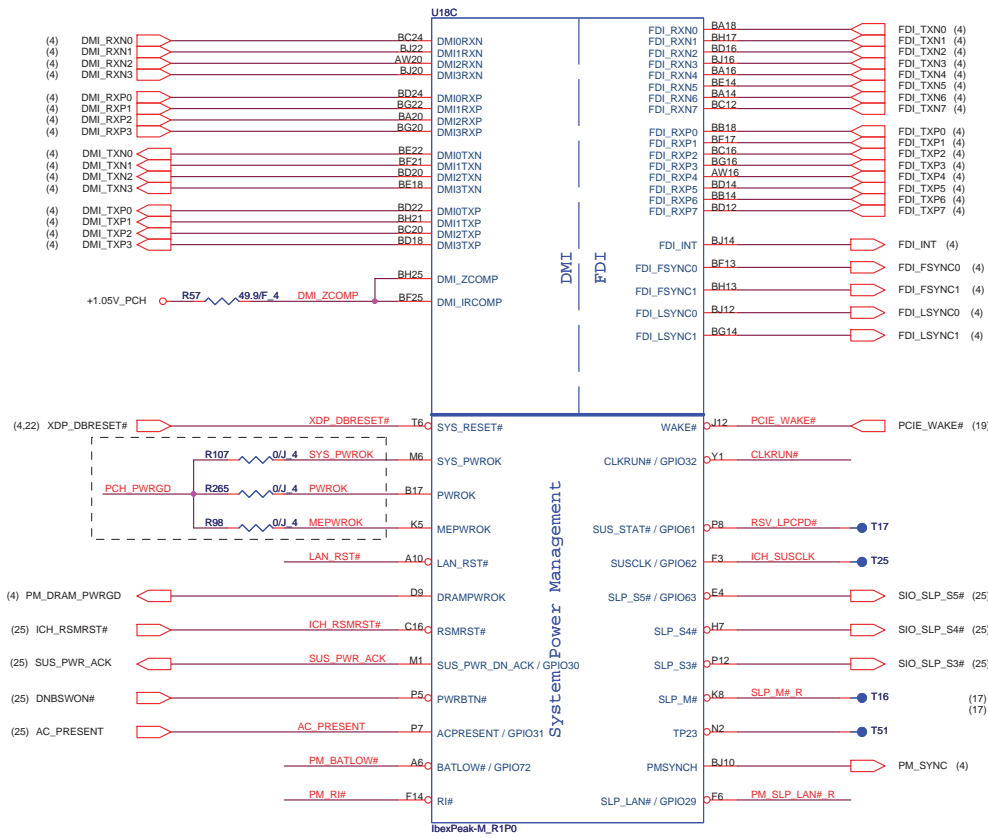
Size: Document Number: Rev 1A
ARRANDALE 4/4

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Can be left NC is Intel CRM implementation; ESD/DG recommendation to GND

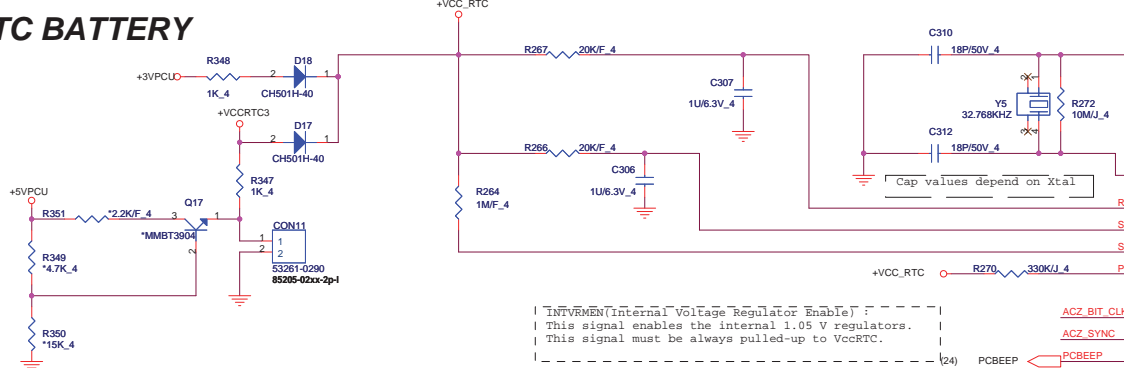
IBEX PEAK-M (DMI,FDI,GPIO)

IBEX PEAK-M (LVDS,DDI)



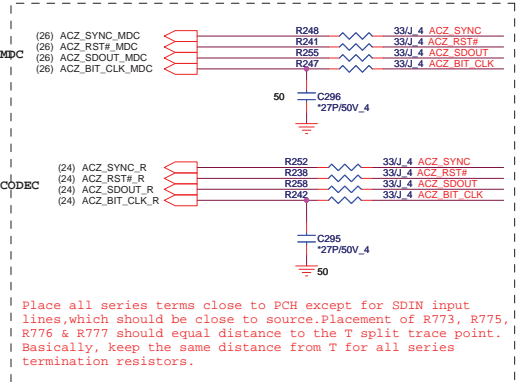
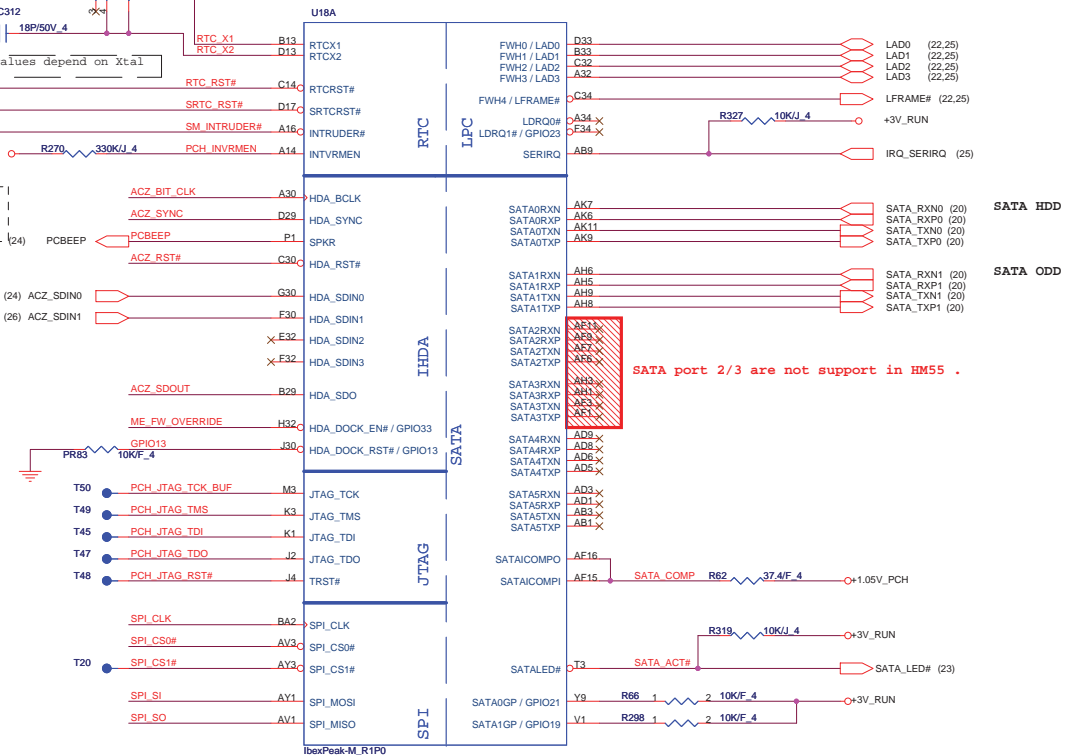
Digital Display Interface

RTC BATTERY

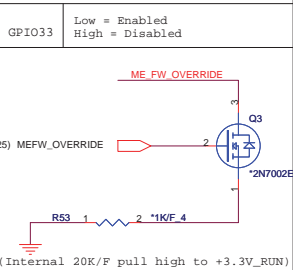


INTRMVEN (Internal Voltage Regulator Enable) : This signal enables the internal 1.05 V regulators. This signal must be always pulled-up to VccRTC.

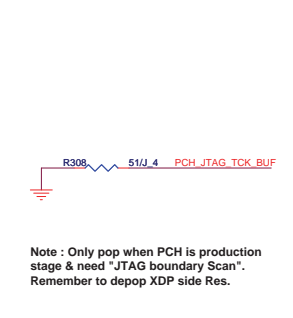
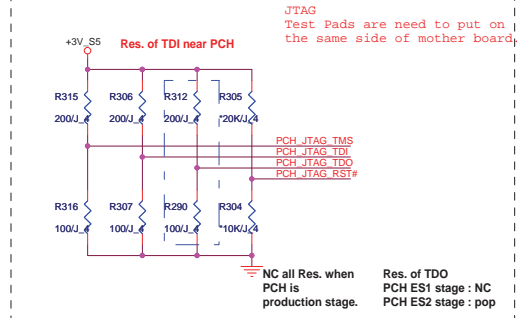
IBEX PEAK-M (HDA, JTAG, SATA)



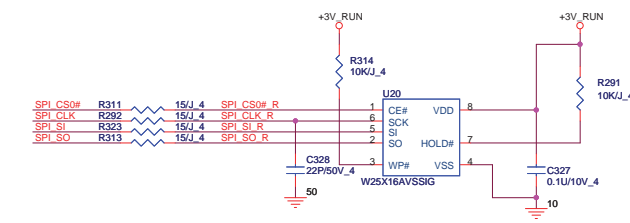
Flash Descriptor Security Override



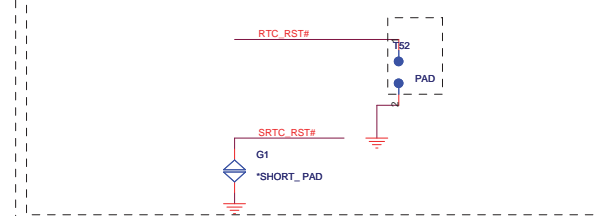
Note : GPIO13 is a signal used for Flash Descriptor Security Override/ME Debug Mode. This signal should be only asserted low through an external pull-down in manufacturing or debug environments ONLY.



For PCH 32Mbit (4M Byte)

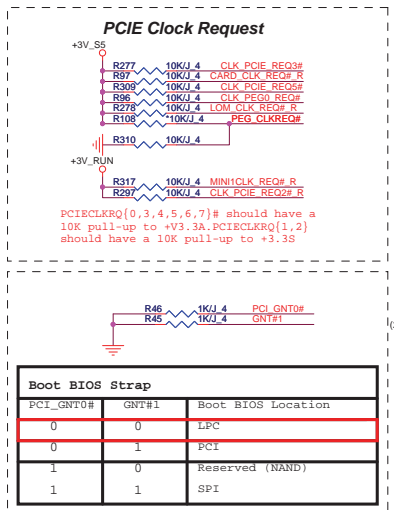
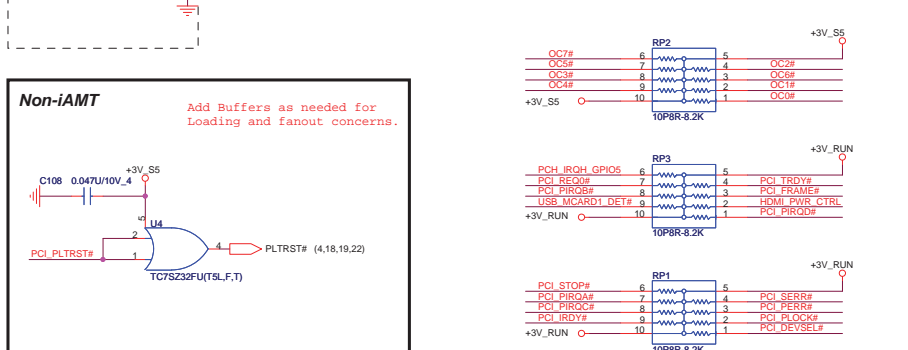
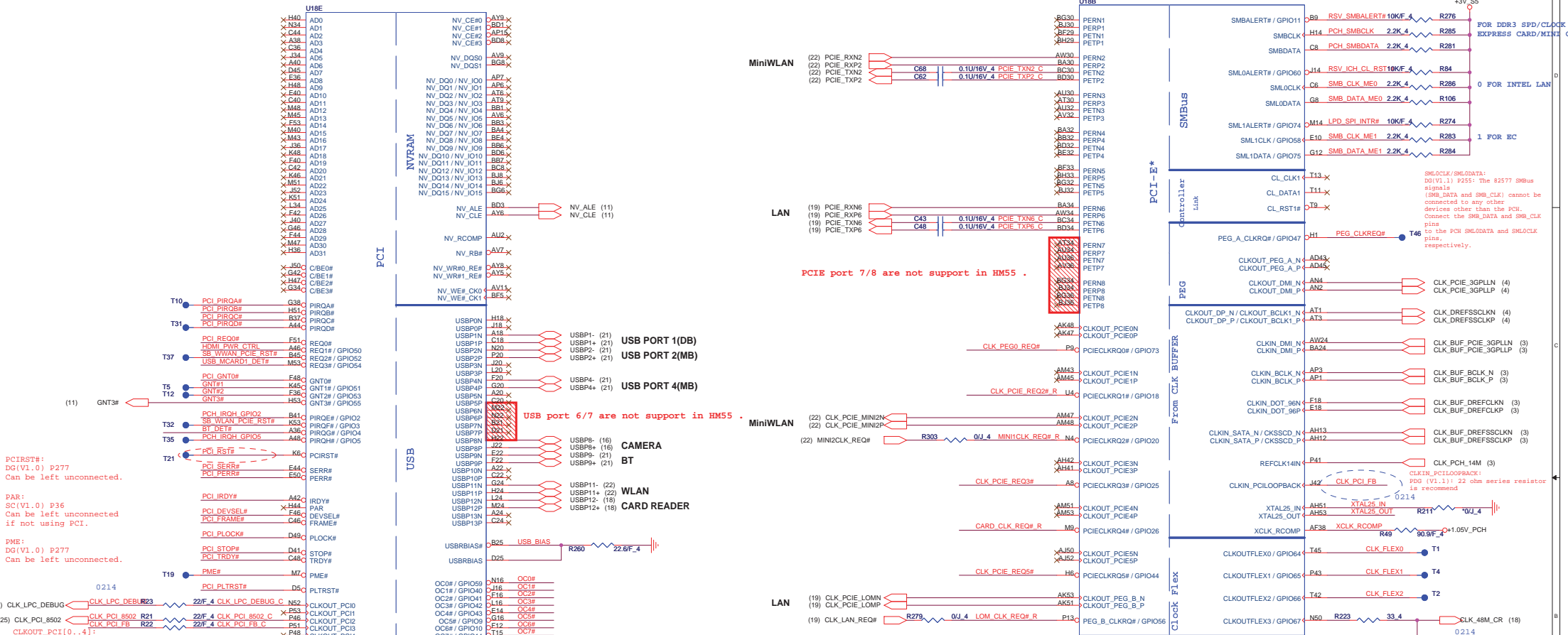


RESET JUMP (Near ROOM DOOR)

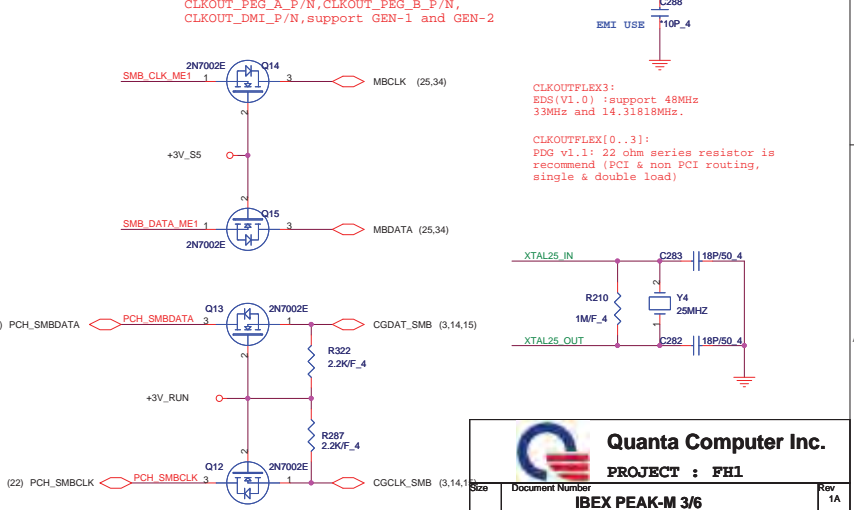


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IBEX PEAK-M 2/6
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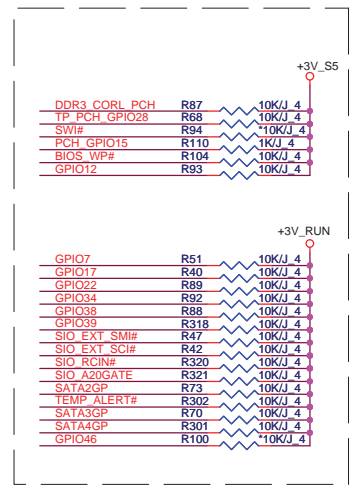
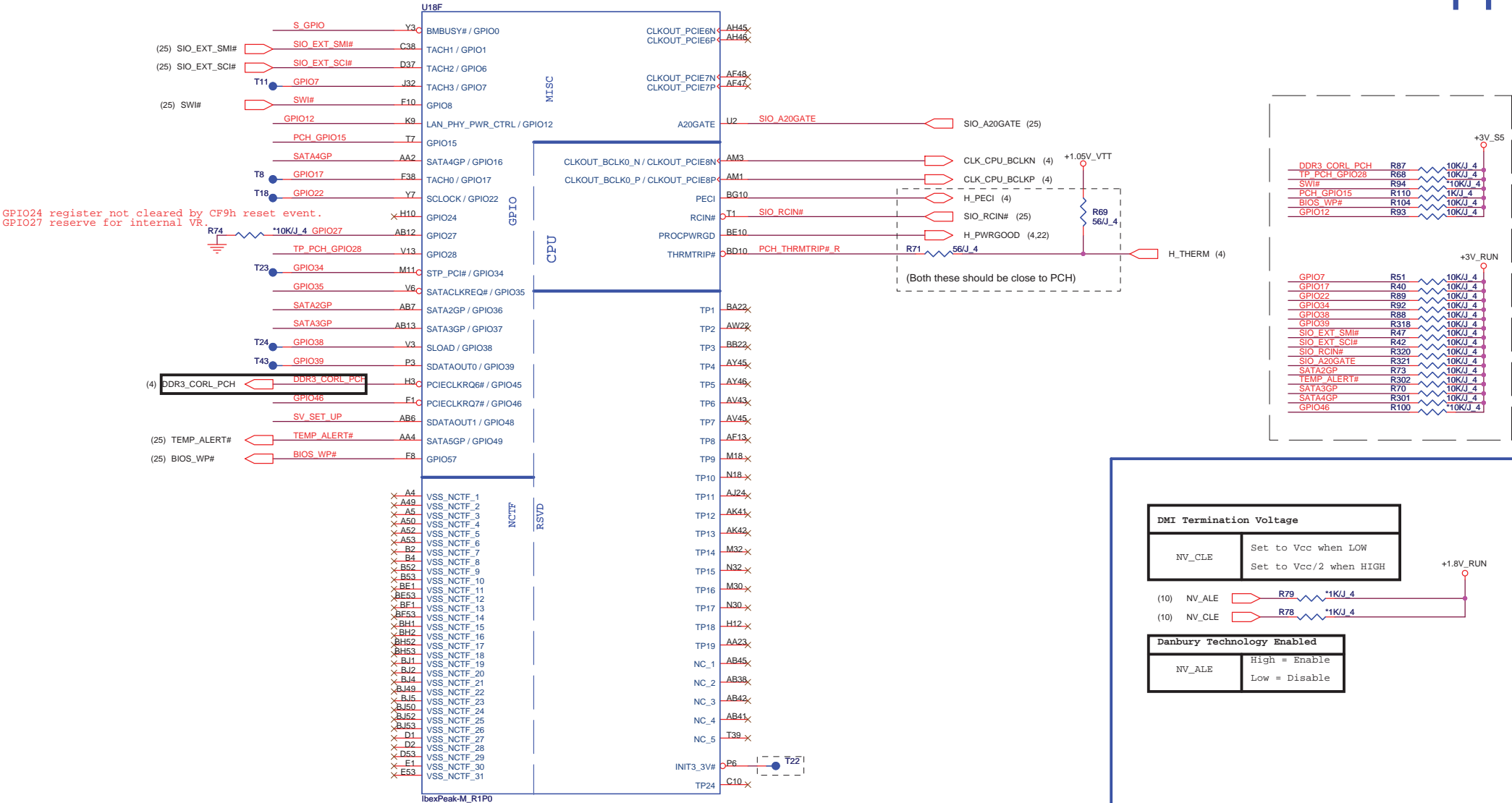
Place TX DC blocking caps close PCH.



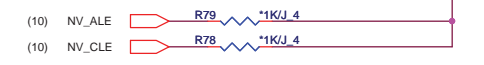
PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	PCI
1	0	Reserved (NAND)
1	1	SPI



IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW
	Set to Vcc/2 when HIGH



Danbury Technology Enabled	
NV_ALE	High = Enable
	Low = Disable

A16 swap override Strap/Top-Block Swap Override jumper

GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default
-------	---

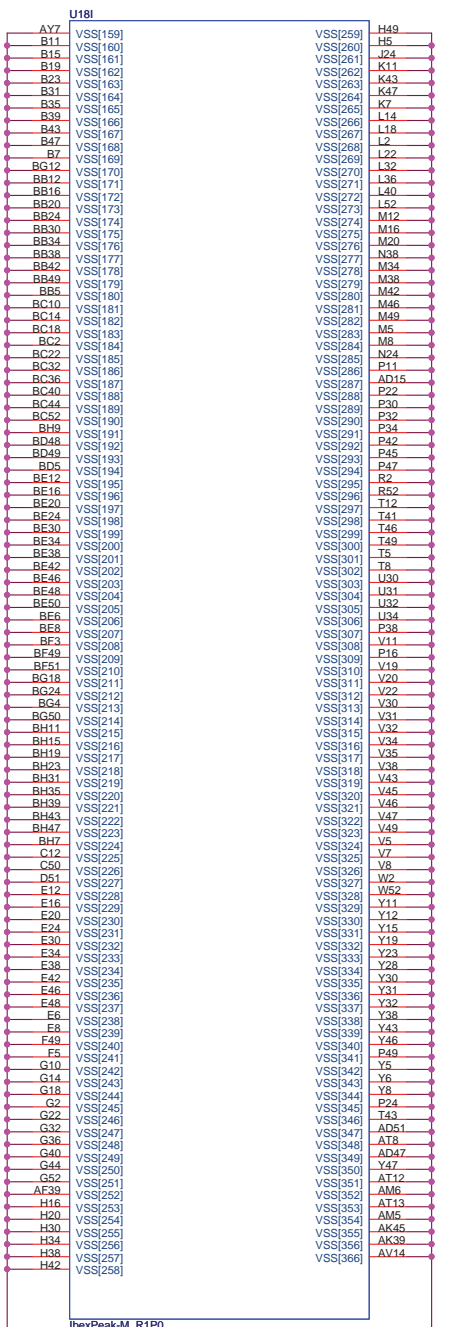
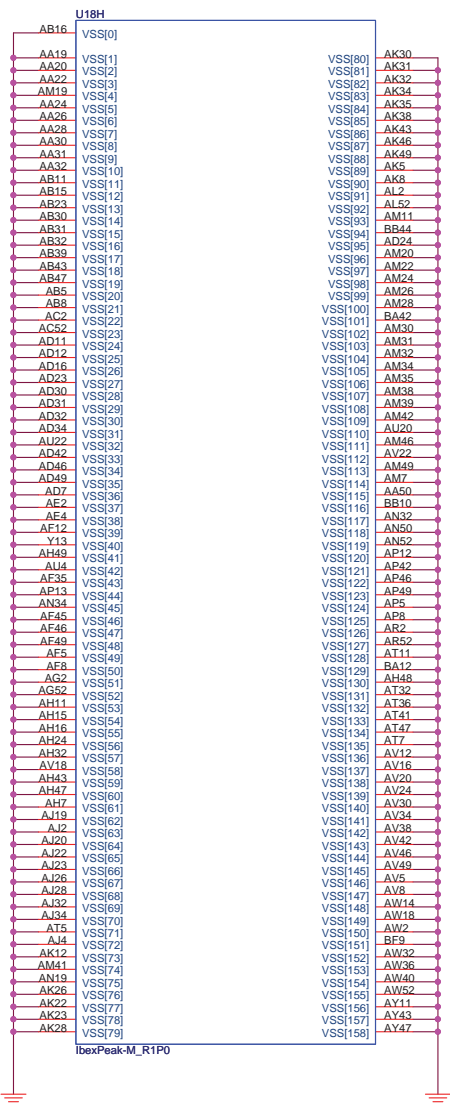
Integrated Clock Chip Enable
(Reserve to validate for future platforms)


RSV_WOL_EN (GPIO8)	Enable when sampled low Disable when sampled high
--------------------	--

SV_SET_UP	1-X High = Strong (Default)
-----------	-----------------------------

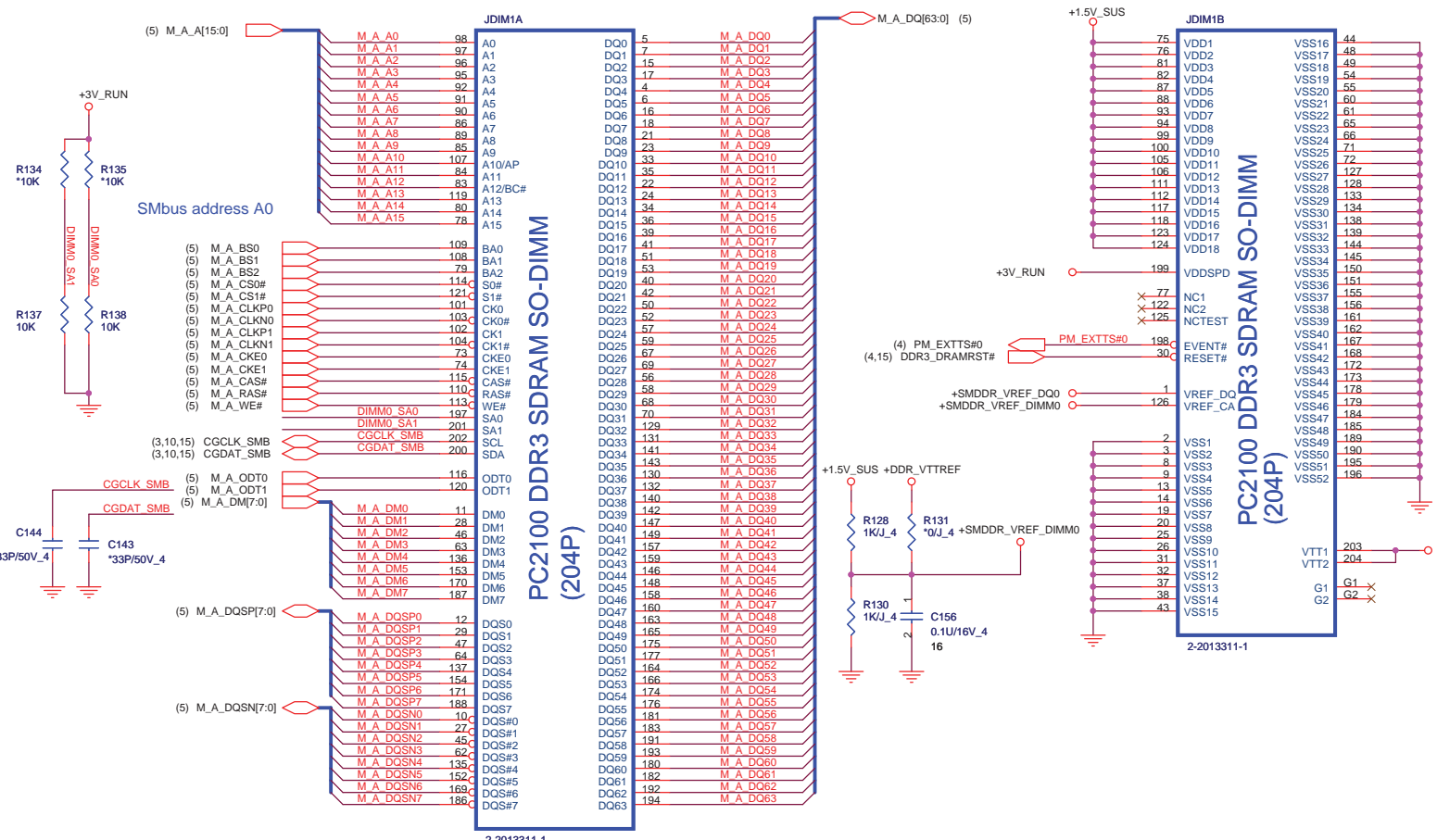
BMBUSY#: (Intel feedback)
Follow CRB checklist, 1K is for intel BIOS validation purpose.

IBEX PEAK-M (GND)



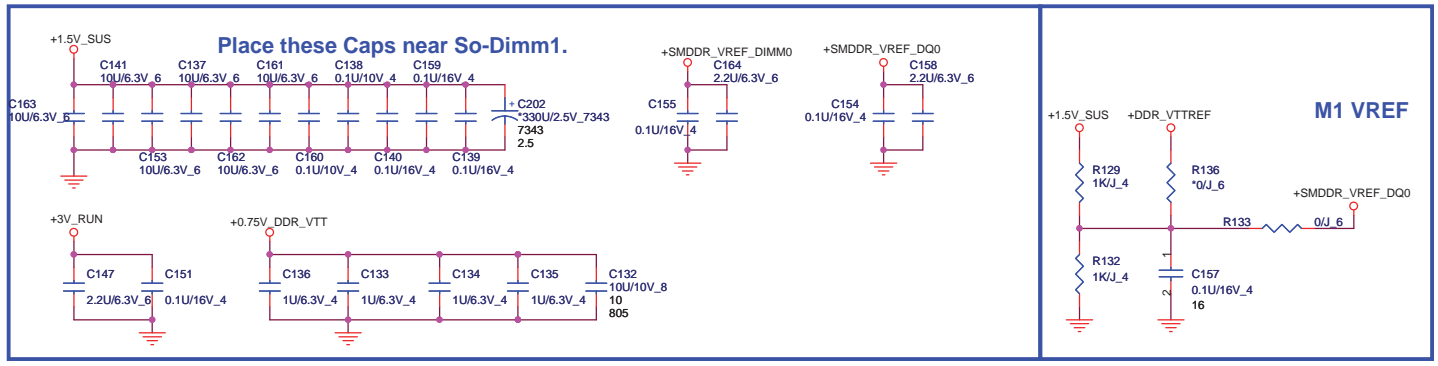
 **Quanta Computer Inc.**
PROJECT : FH1

Size	Document Number	Rev
	IBEX PEAK-M 6/6	1A
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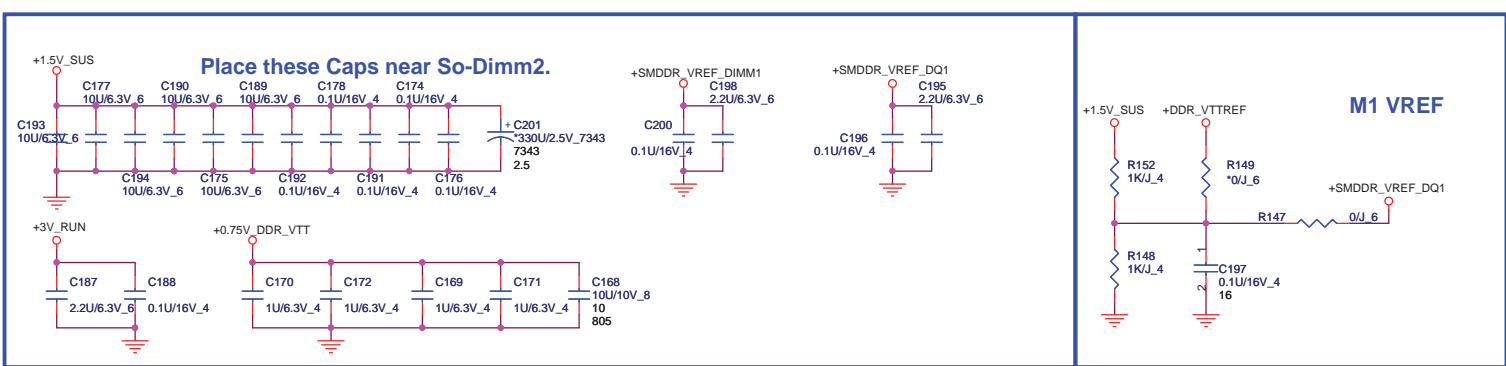
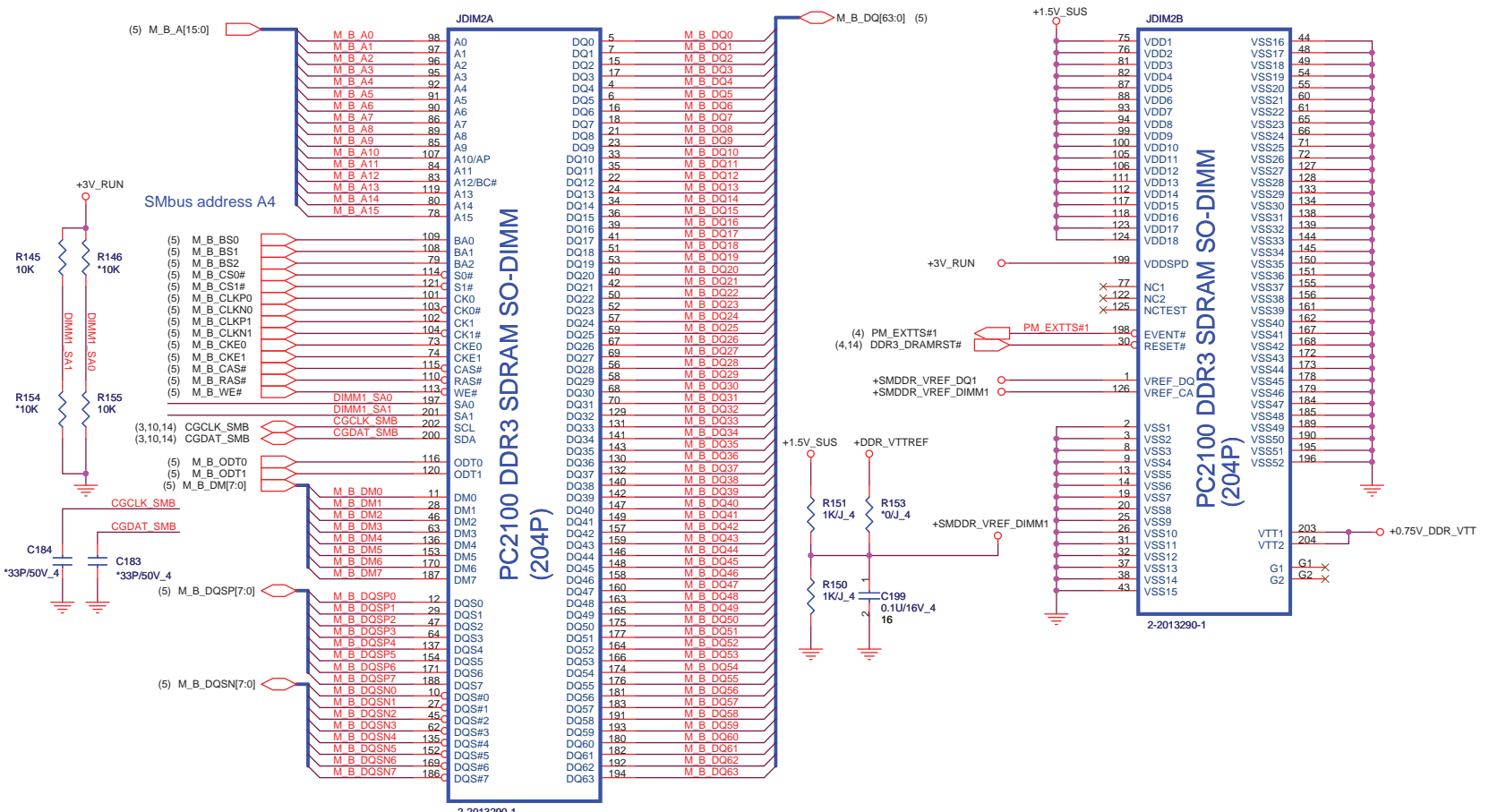
Intel is requesting that customers implement all methods (M1 and M2 and M3 described below) to generate and control Reference voltage for Data/Strobe inputs (VREFDQ) on Clarksfield based platforms. For fine tuning of the VREFDQ levels to optimize the voltage and timing margins.

M1: Fixed voltage resistor divider or DDR Voltage Regulator drives the Vref
M2: A set of Digital potentiometers and op amps are added on the motherboard (one pair for each channel). This circuit is controlled by SMBUS (SMB_CLK & SMB_DATA) on PCH.
M3: Intel investigating future processor VREF_DQ generation to replace M1 and M2. This would require routing processor signal balls J17 and H17 to SO-DIMM connectors directly.

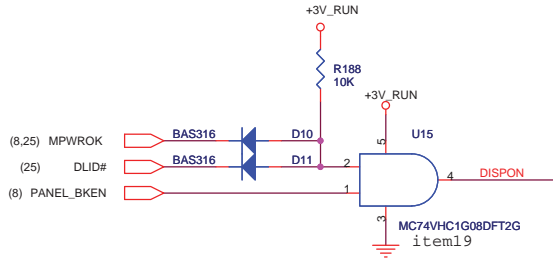


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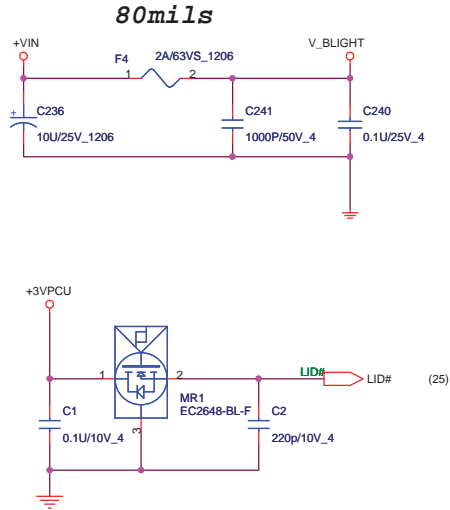
Size	Document Number	Rev
	DDR3 DIMM-1	1A
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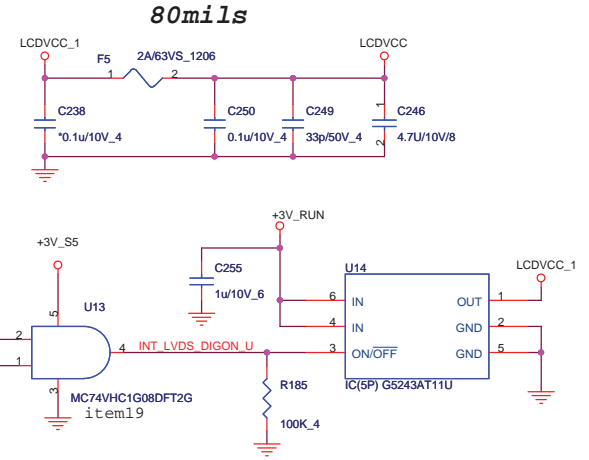
Backlight Control(LDS)



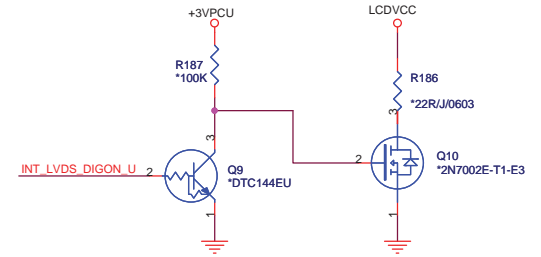
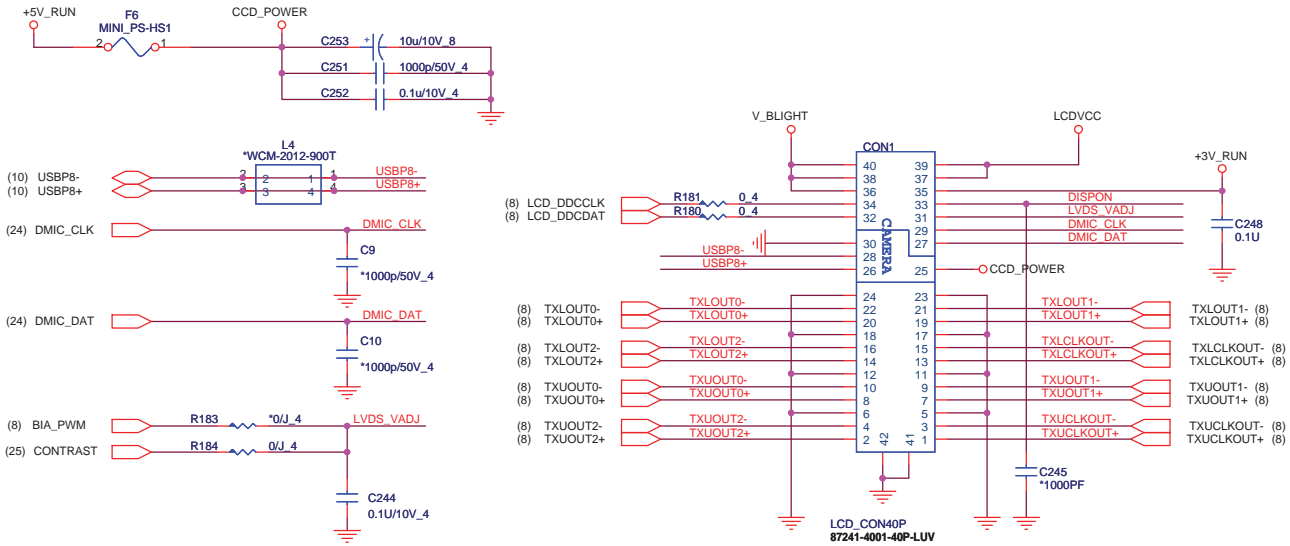
BACKLIGHT POWER




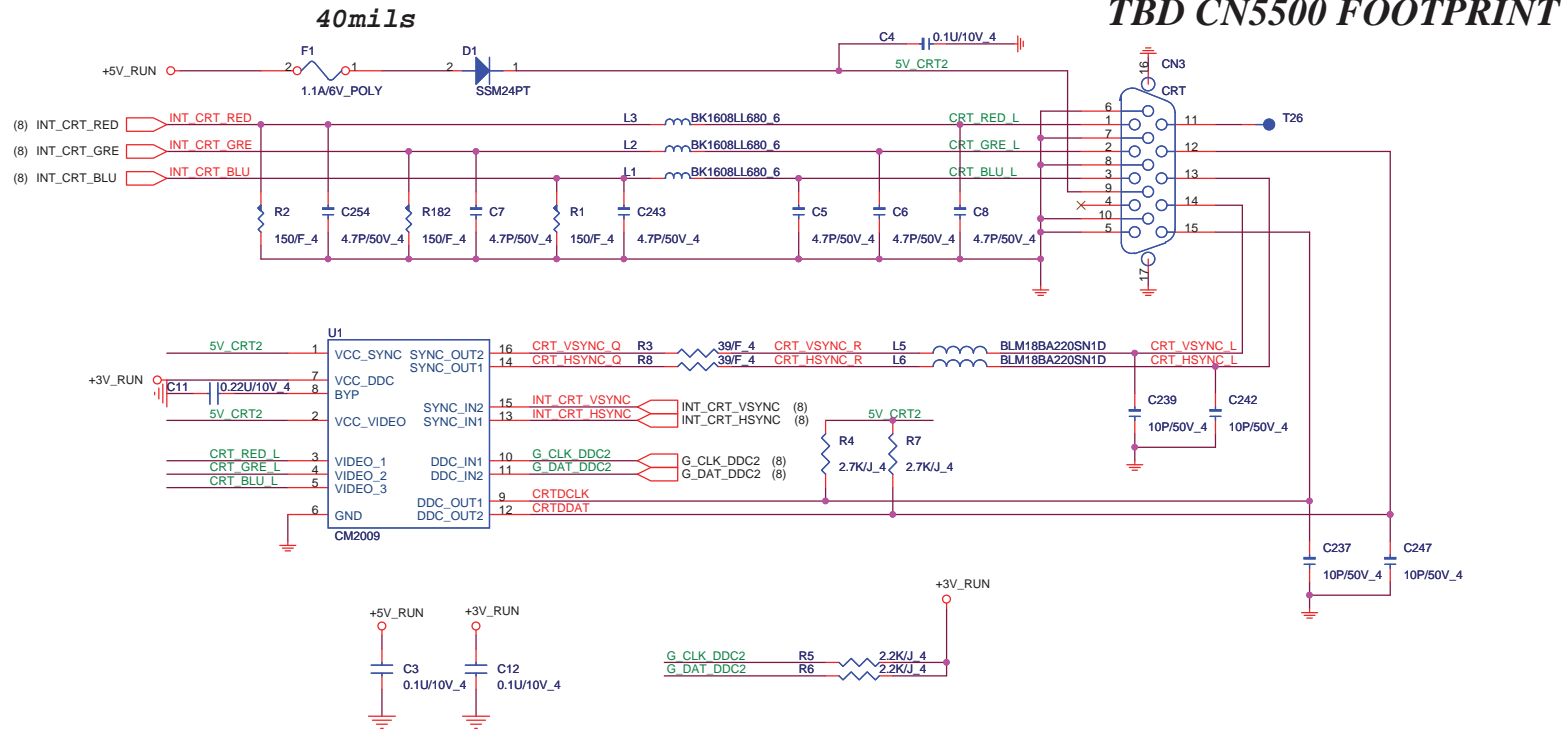
LED Panel POWER SWITCH(LVDS) 16



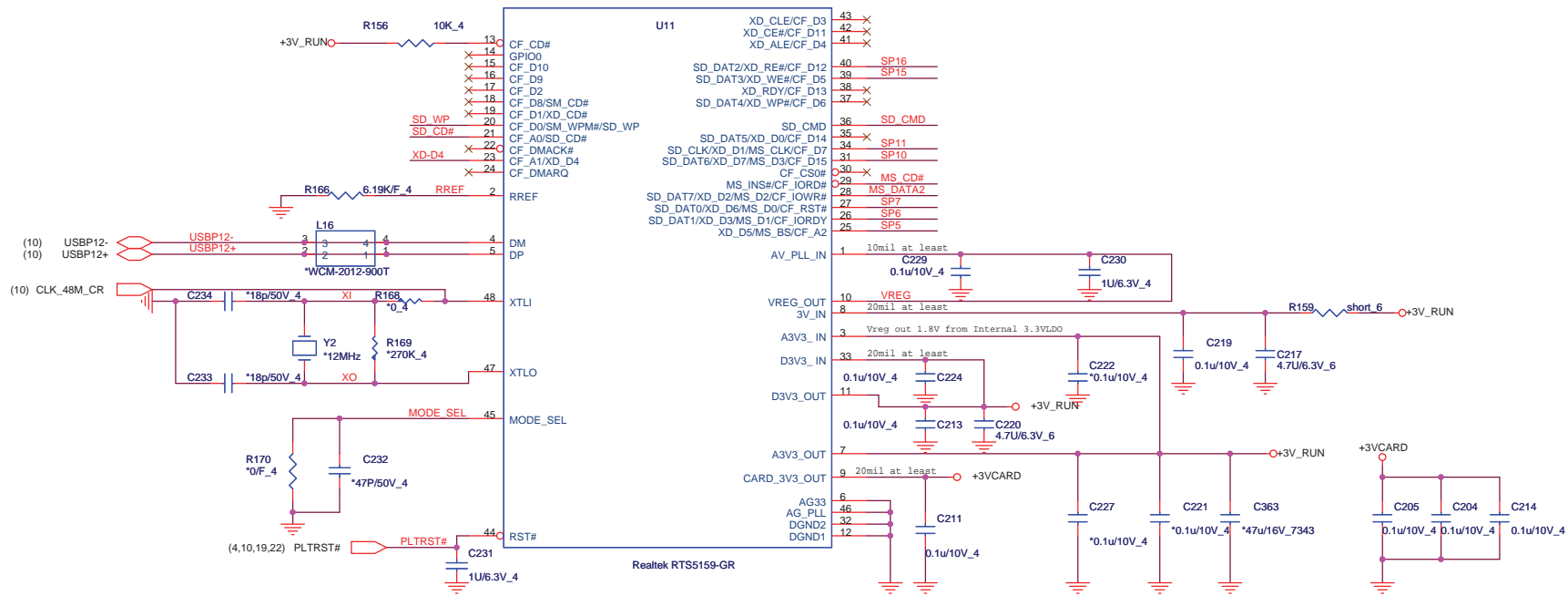
LVDS/CCD



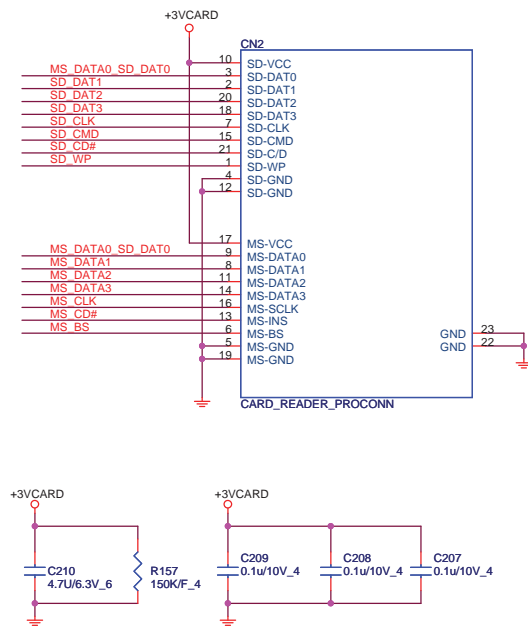
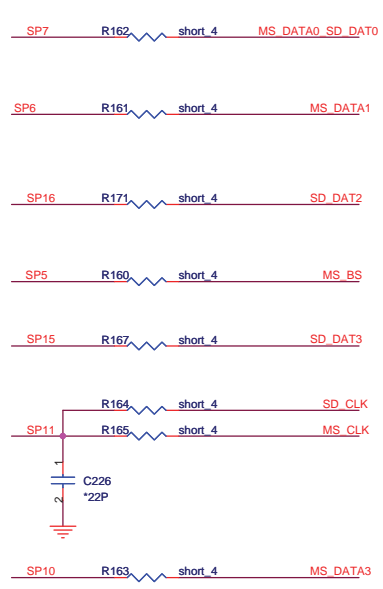
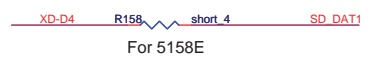
 Quanta Computer Inc. PROJECT : FH1		
Size	Document Number	Rev
	LCD/LED Panel/CCD	1A
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Card Reader

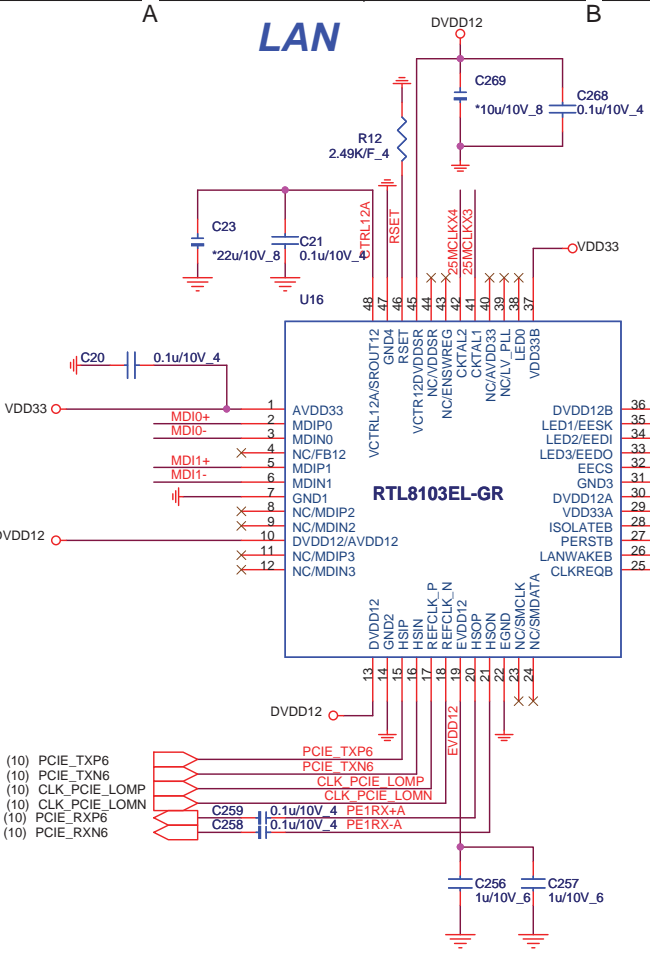


As close U8203 pin9 as possible



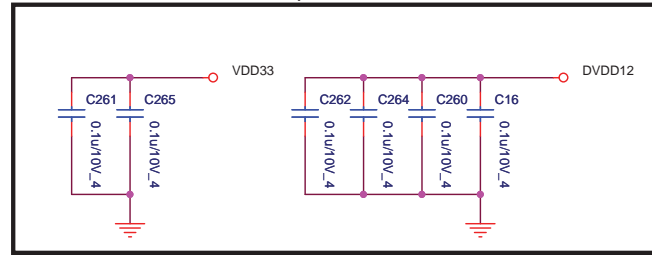
Quanta Computer Inc.
PROJECT : FH1
Card Reader RTS5159

Size	Document Number	Rev
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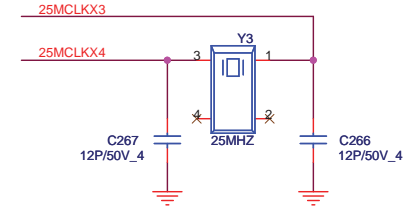


- (10) PCIE_TXP6
- (10) PCIE_TXN6
- (10) CLK_PCIE_LOMP
- (10) CLK_PCIE_LOMN
- (10) PCIE_RXP6
- (10) PCIE_RXN6

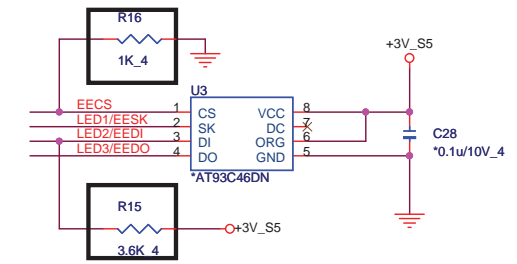
Placement close to LAN chip



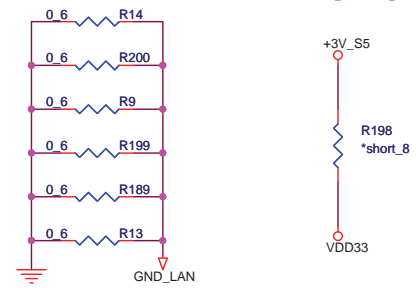
X'tal 25MHz



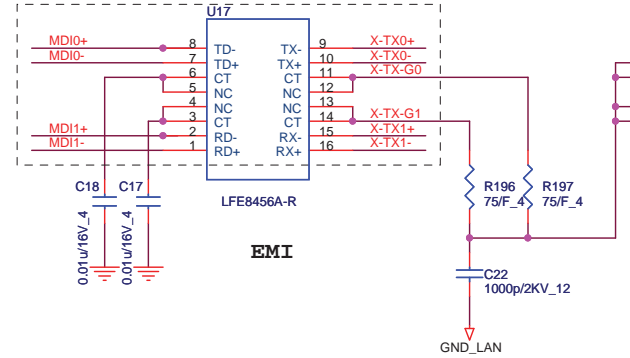
LAN EEPROM



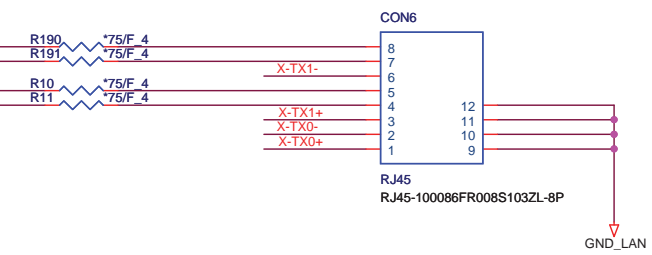
LAN Power



10/100 Transformer signal swap



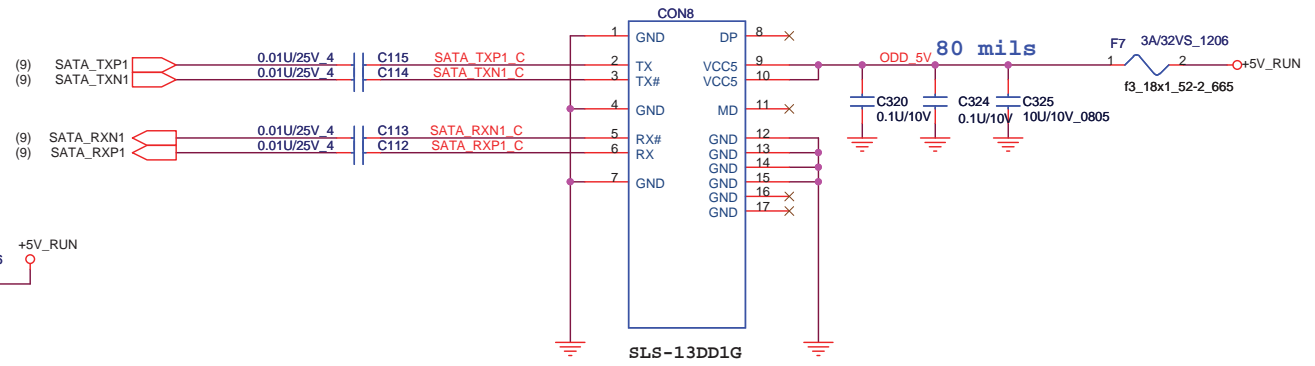
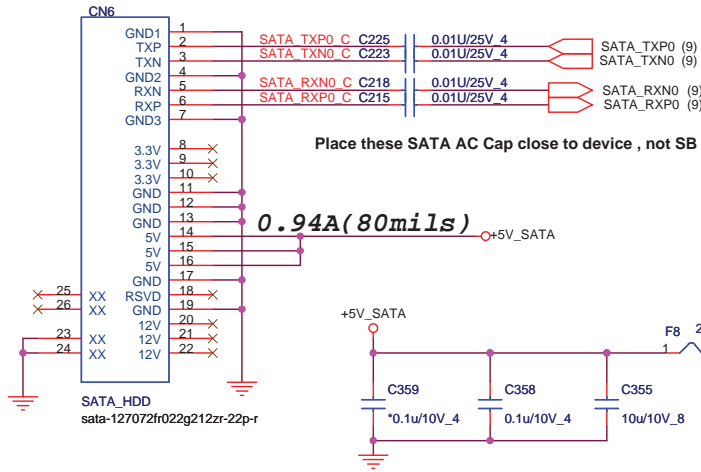
RJ45



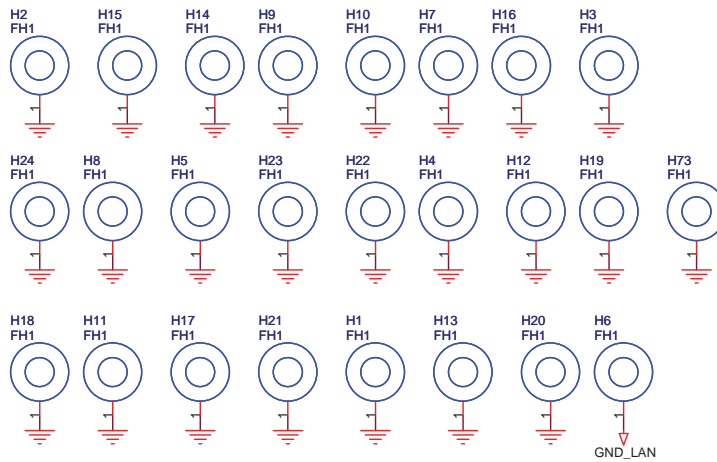
Quanta Computer Inc.

PROJECT : FH1

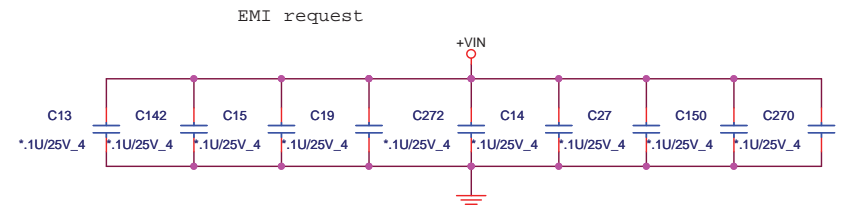
Size	Document Number	Rev 1A
LAN_RTL8103EL/RJ45		
Date: Friday, October 09, 2009	Sheet 19 of 37	



Hole

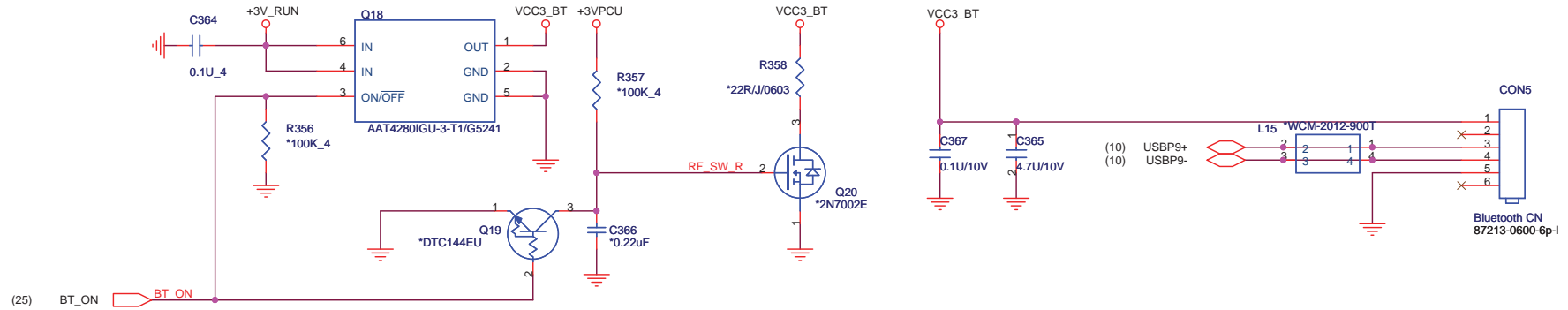


Decoupling Cap

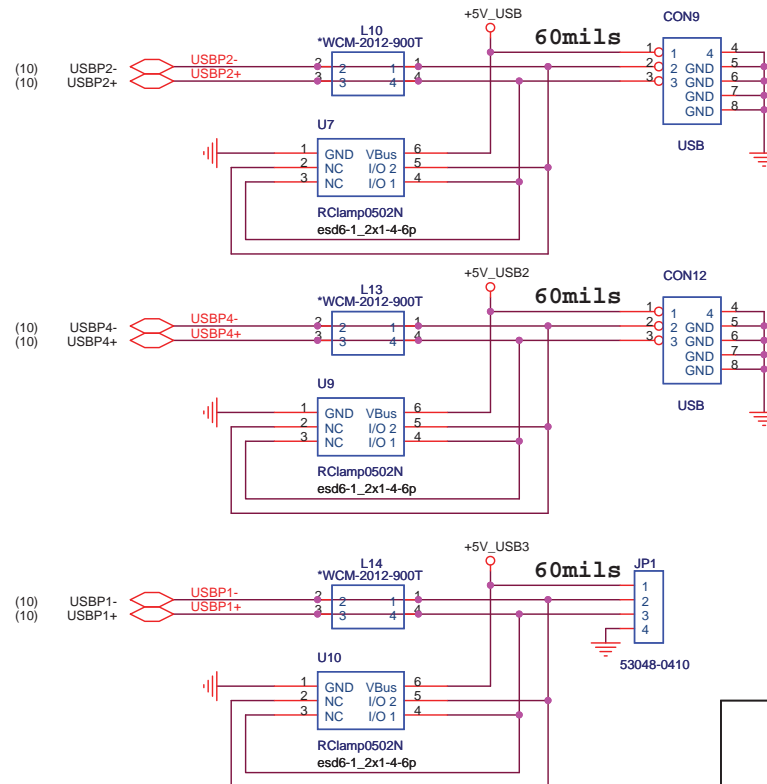
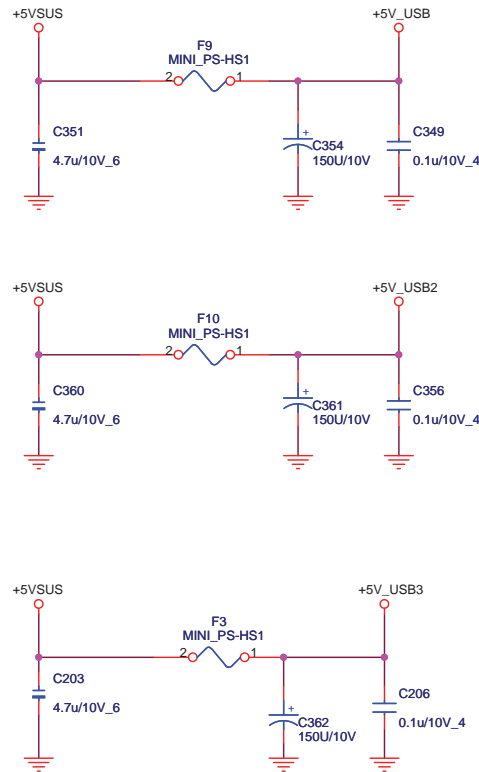


Quanta Computer Inc.
PROJECT : FH1

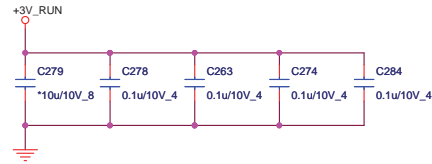
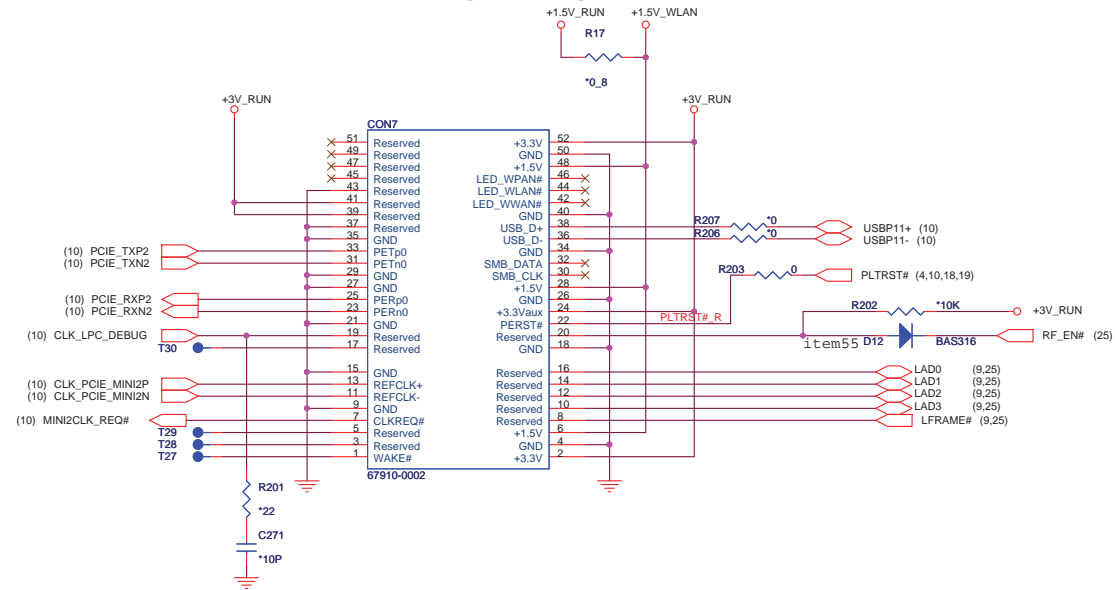
Size	Document Number	Rev
	HDD/ ODD/HOLE	1A
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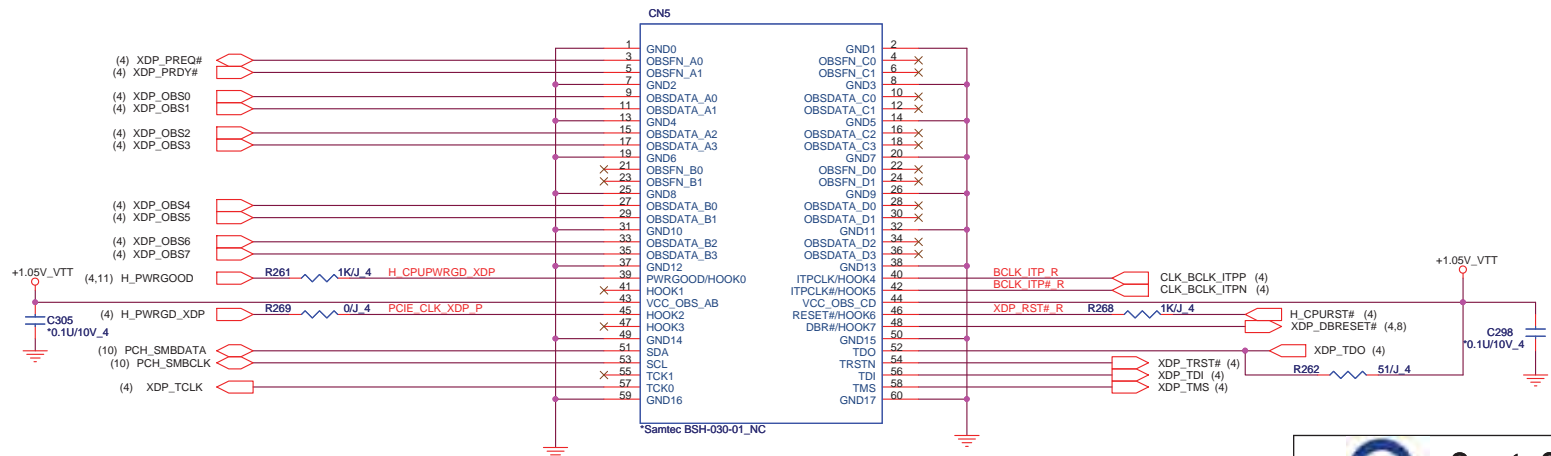
USB Connector



MINI CARD (WLAN)



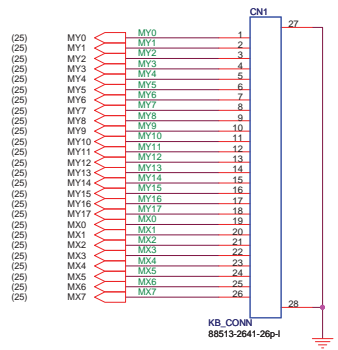
XDP



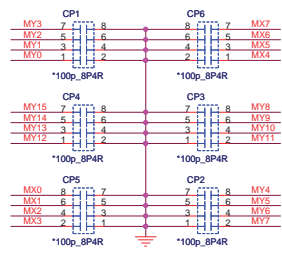
It is for debug. request vevdeer provide 200 pcs sample.

		Quanta Computer Inc. PROJECT : FH1	
		Size: _____ Document Number: MINI CARD(WLAN)/XDP Date: Friday, October 09, 2009	Rev: 1A Sheet 22 of 37

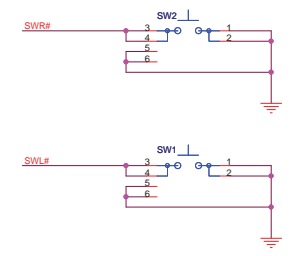
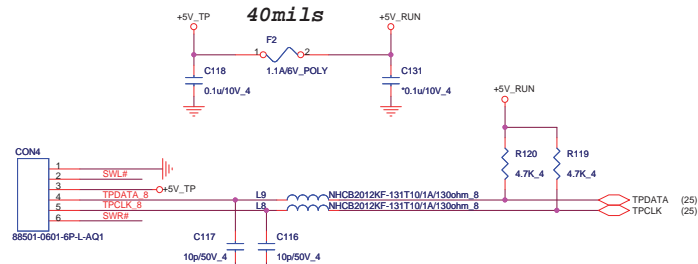
Keyboard(KBC)



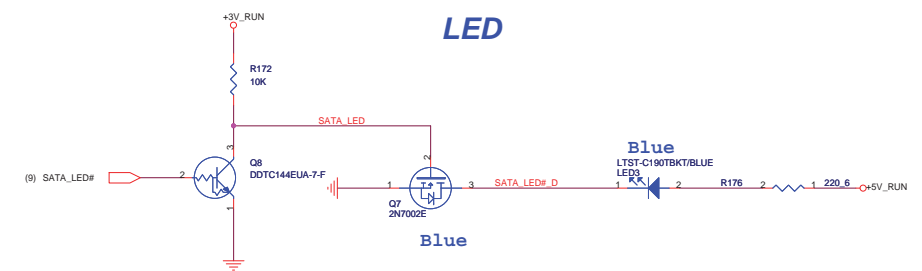
For EMI Reserve Caps for debug



Touch Pad



HDD/ODD



CAPS LED



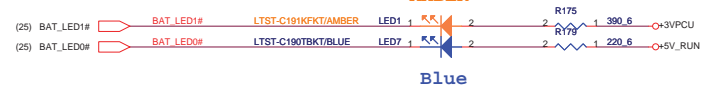
NUM LED



WLAN



Battery

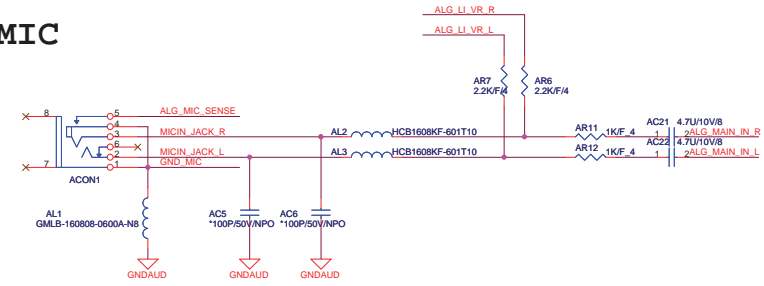


Power Status

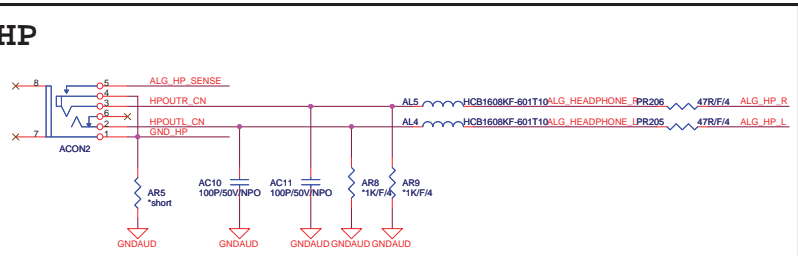


Codec ALC269

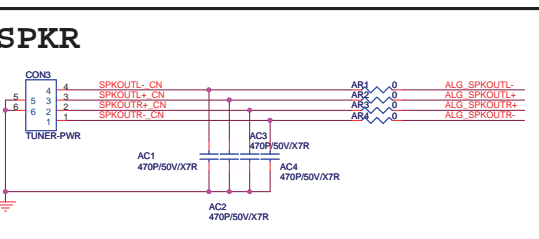
MIC



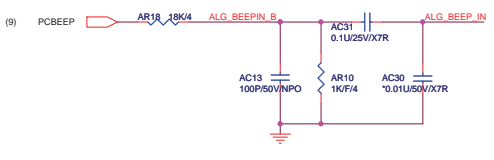
HP



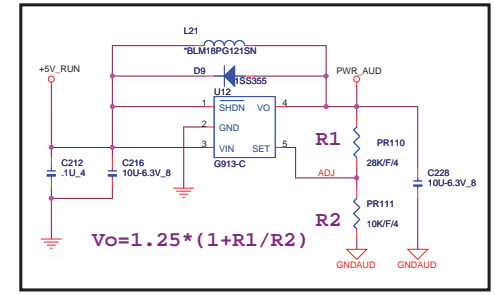
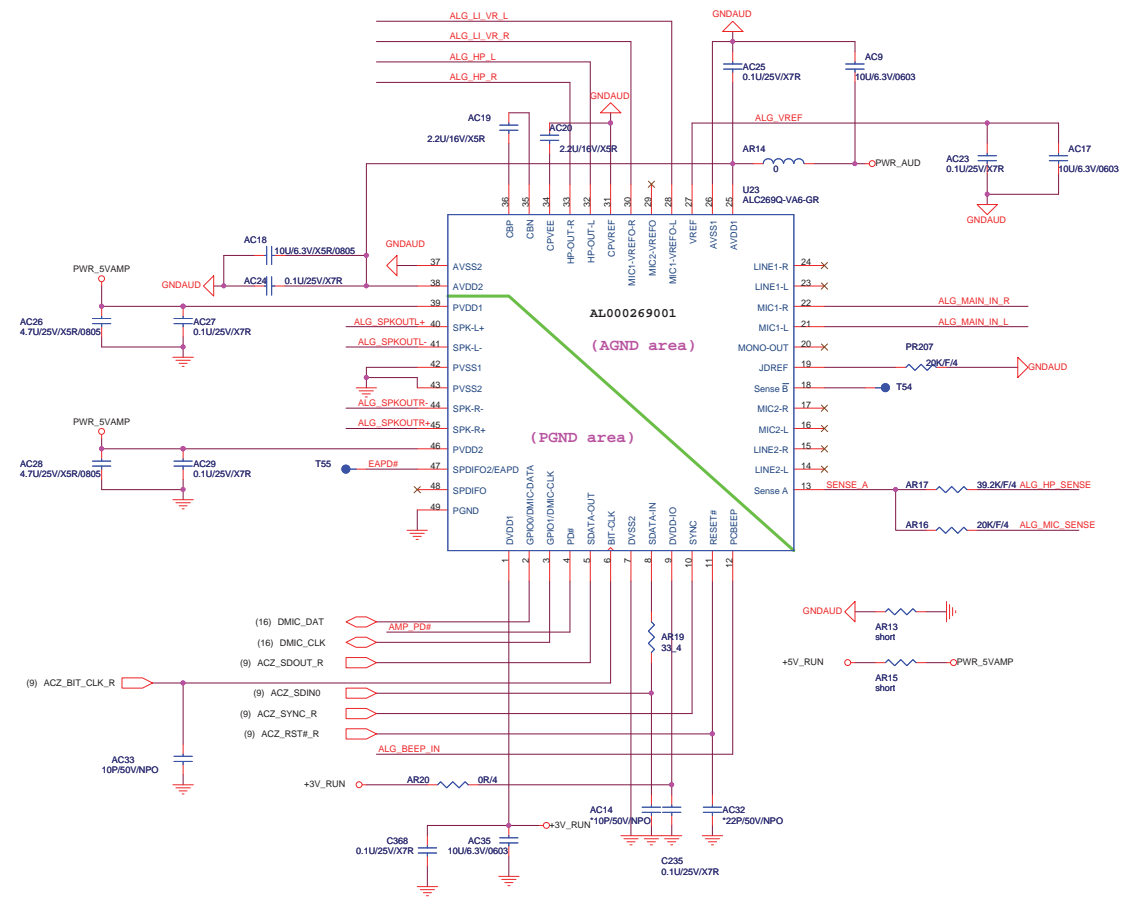
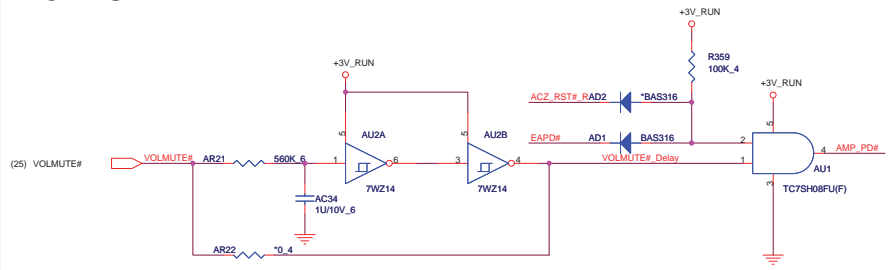
SPKR



BEEP

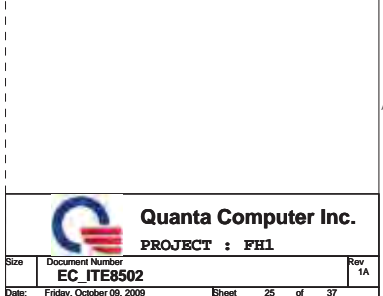
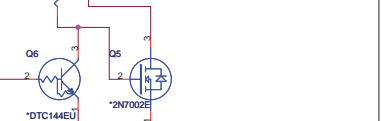
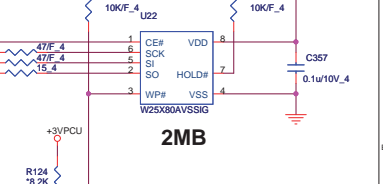
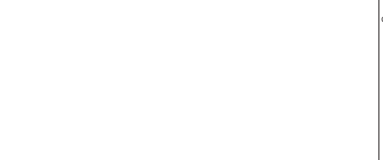
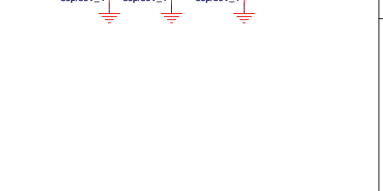
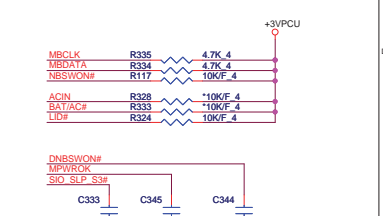
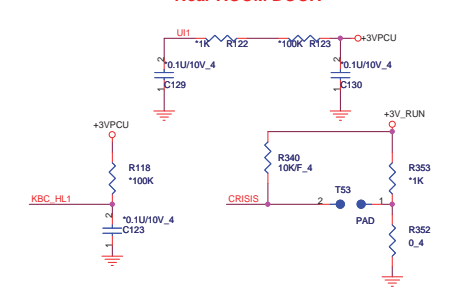
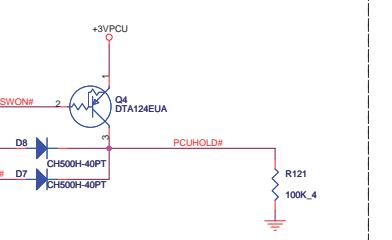
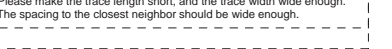
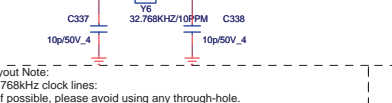
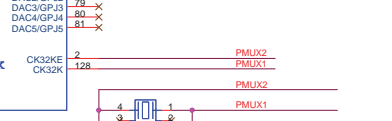
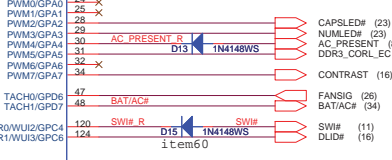
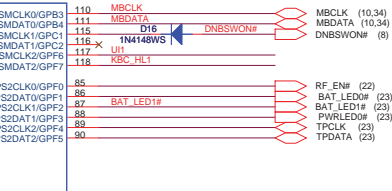
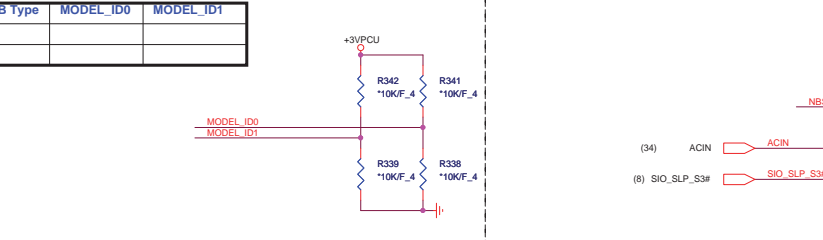
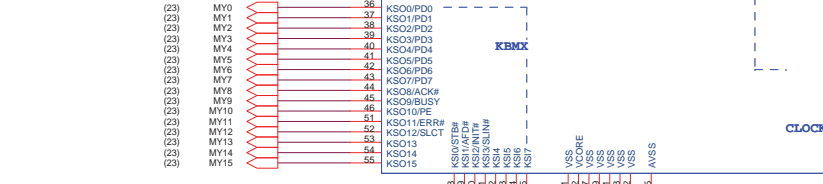
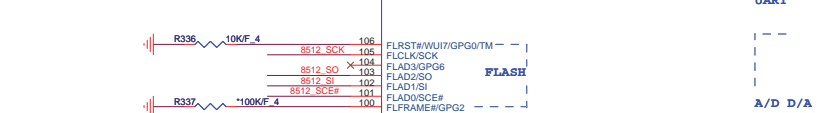
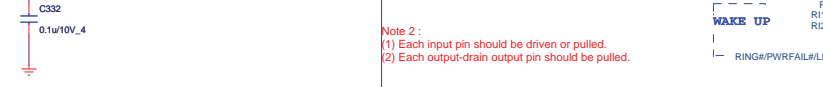
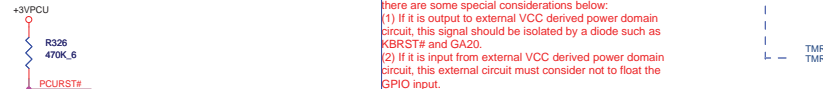
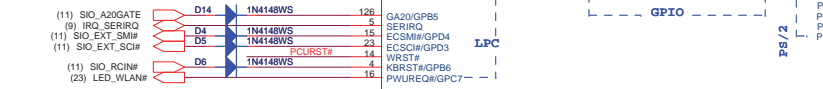
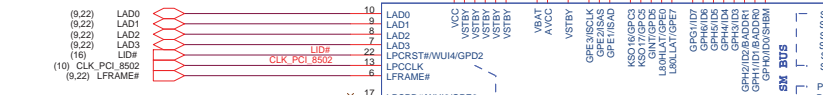
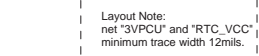
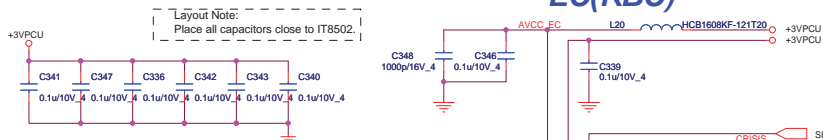


VOLMUTE



Quanta Computer Inc.
PROJECT : FH1
CODEC (ALC269)
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EC(KBC)

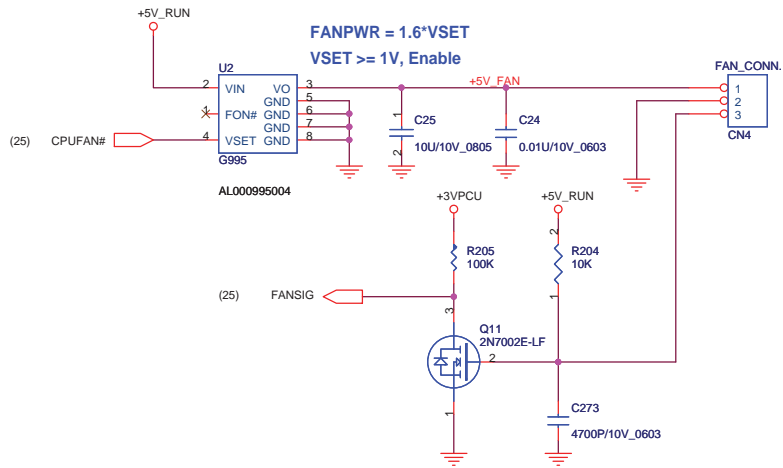


Layout Note:

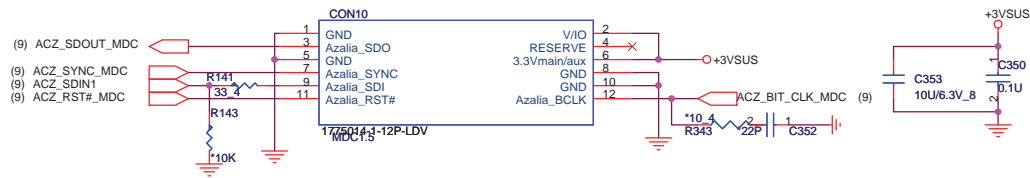
- a. 32.768kHz clock lines:
- b. If possible, please avoid using any through-hole.
- c. Please make the trace length short, and the trace width wide enough.
- d. The spacing to the closest neighbor should be wide enough.

MB Type	MODEL_ID0	MODEL_ID1

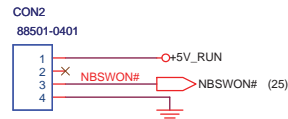
CPU FAN CTRL



MDC



SW BOARD CON



Quanta Computer Inc.
PROJECT : FHL

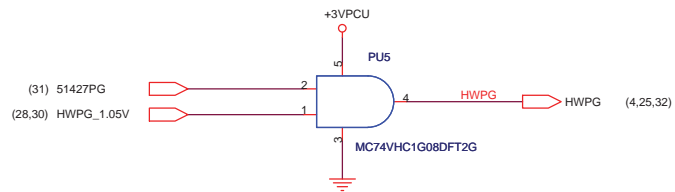
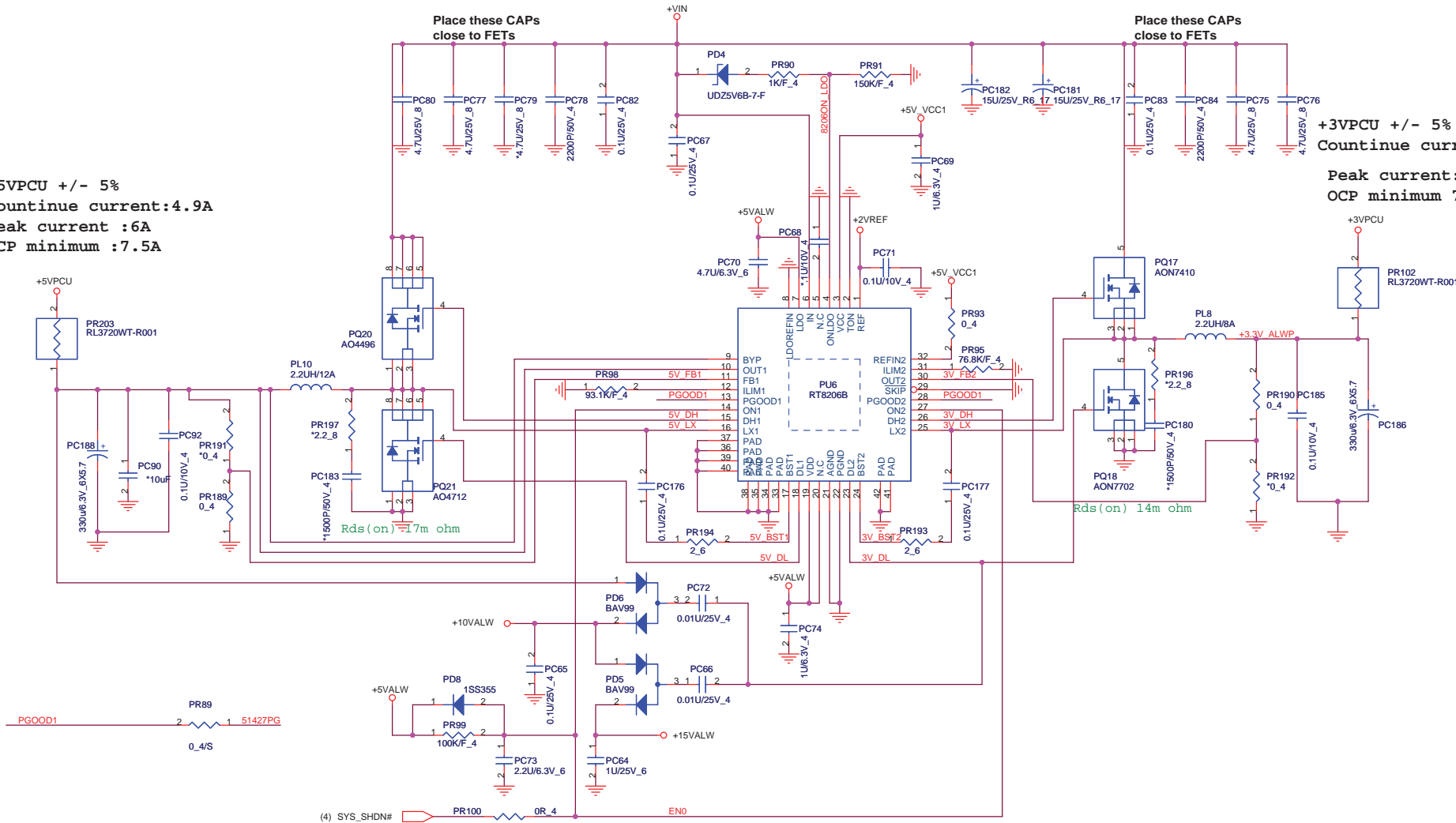
Size	Document Number	Rev
	FAN/SW CON/MDC	1A
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Place these CAPs close to FETs

Place these CAPs close to FETs

+5VPCU +/- 5%
 Countinue current:4.9A
 Peak current :6A
 OCP minimum :7.5A

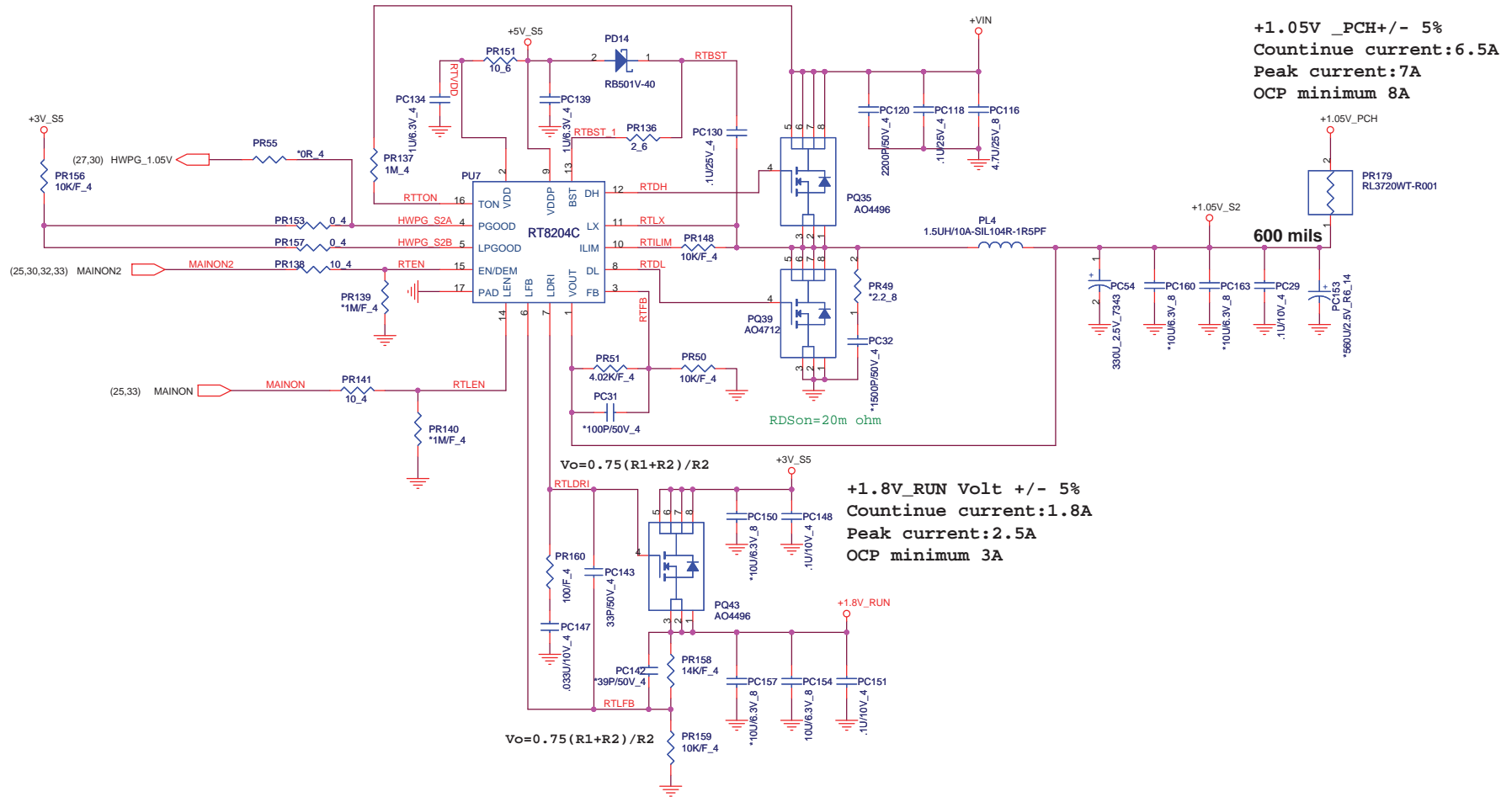
+3VPCU +/- 5%
 Countinue current:5.1A
 Peak current:6A
 OCP minimum 7.5A




Quanta Computer Inc.
PROJECT : FH1
+5V/+3V (RT8206B)

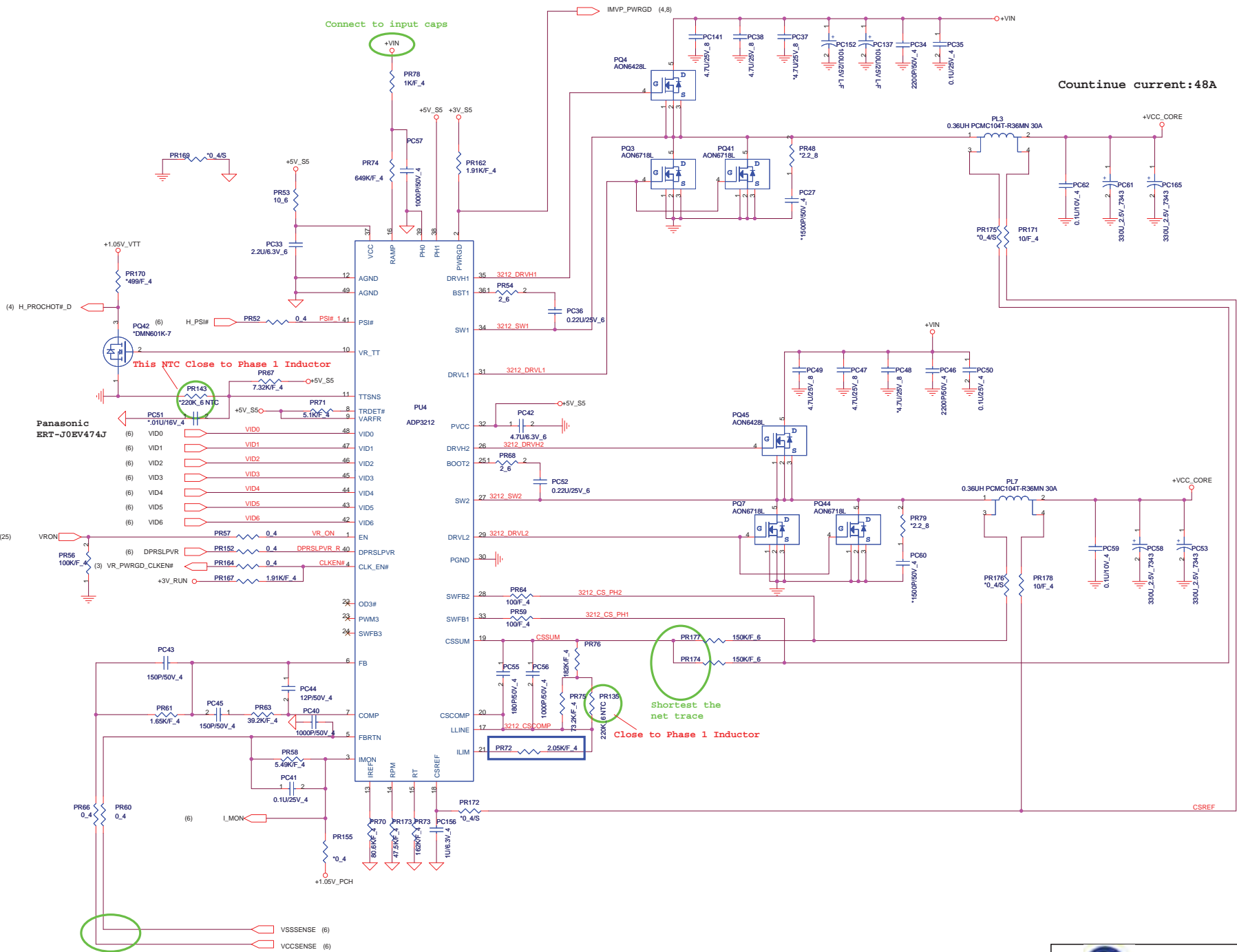
Size	Document Number	Rev
		1A

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 **Quanta Computer Inc.**
PROJECT : FHL

Size	Document Number	Rev
	+1.05V/+1.8V (RT8204C)	1A
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Continue current: 48A

Connect to input caps

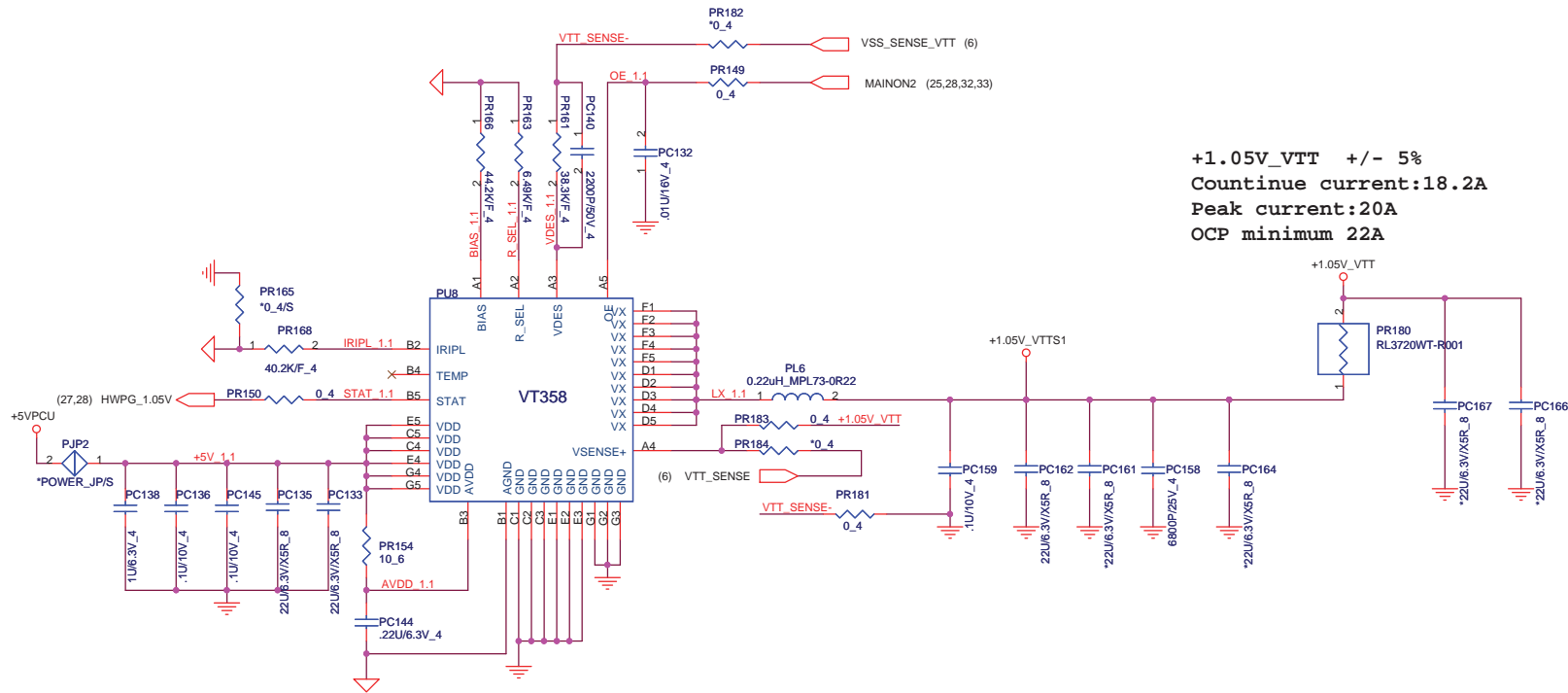
This NTC Close to Phase 1 Inductor

Shortest the net trace


Close to Phase 1 Inductor

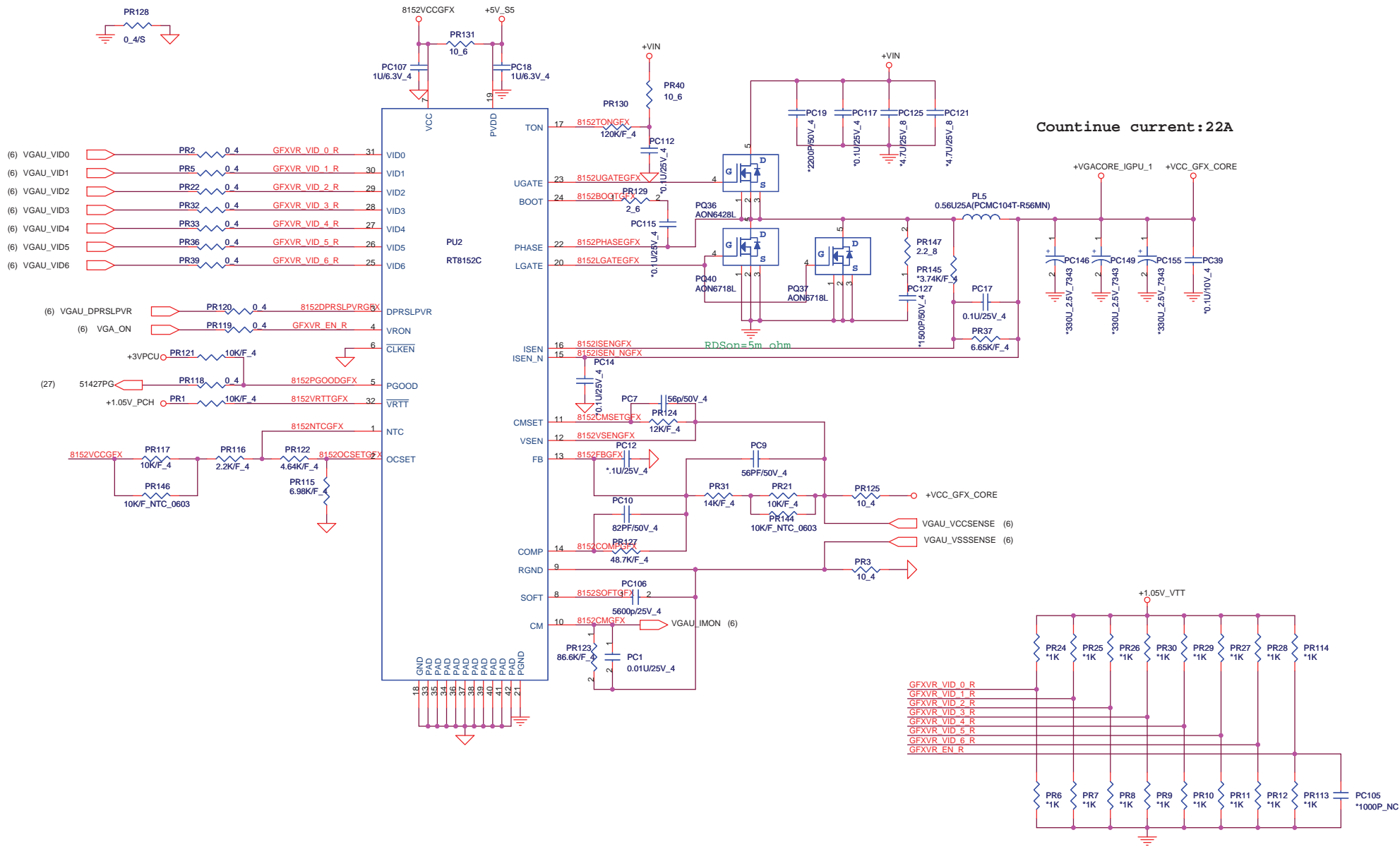
Quanta Computer Inc.
PROJECT : FH1

Size	Document Number	Rev
	CPU Core (ADP3212)	1A
Date: Friday, October 09, 2009	Sheet 29 of 37	

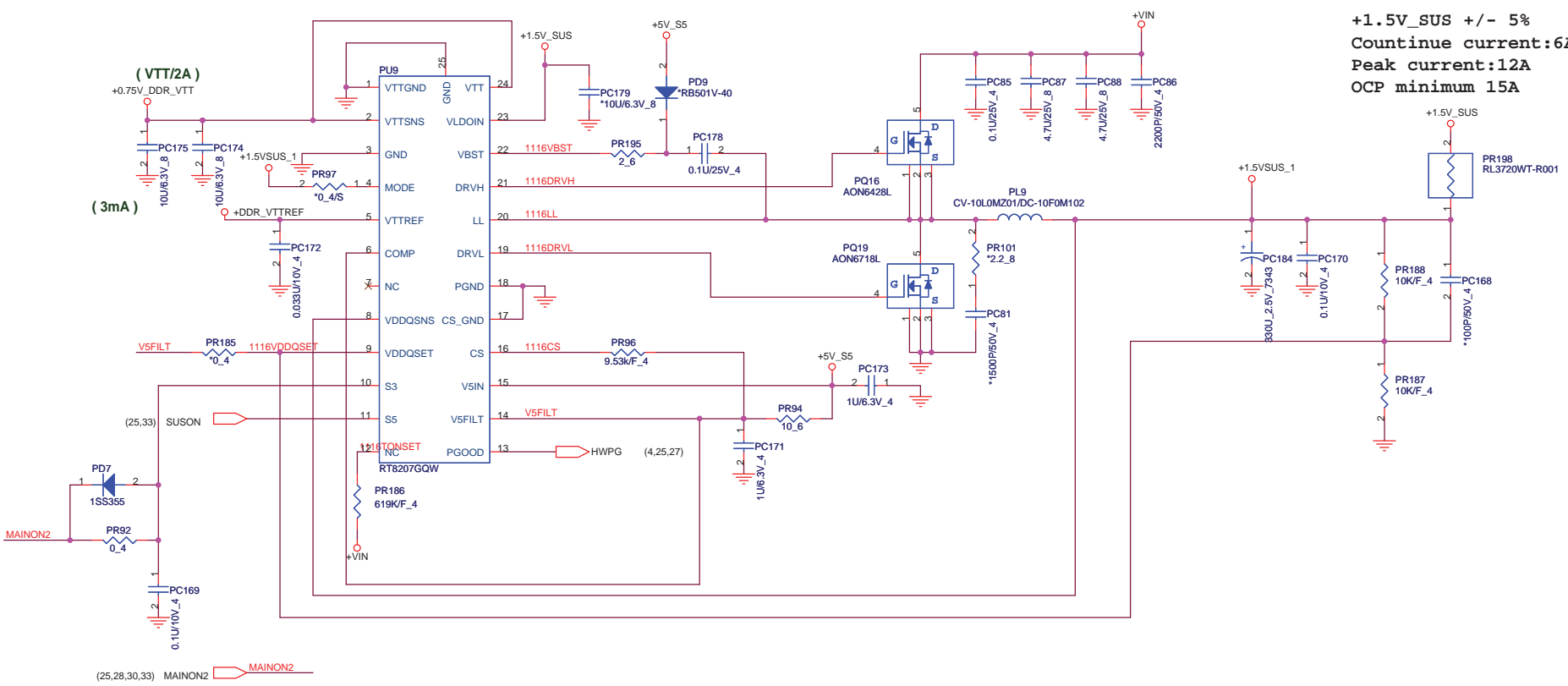


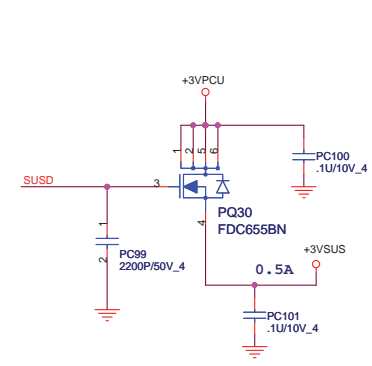
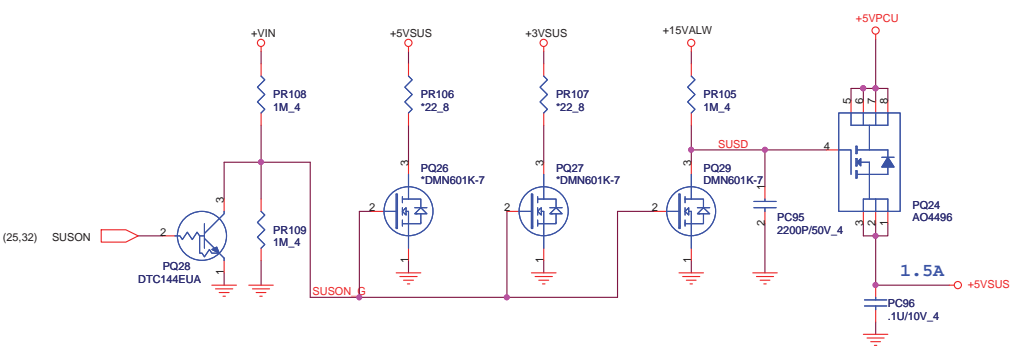
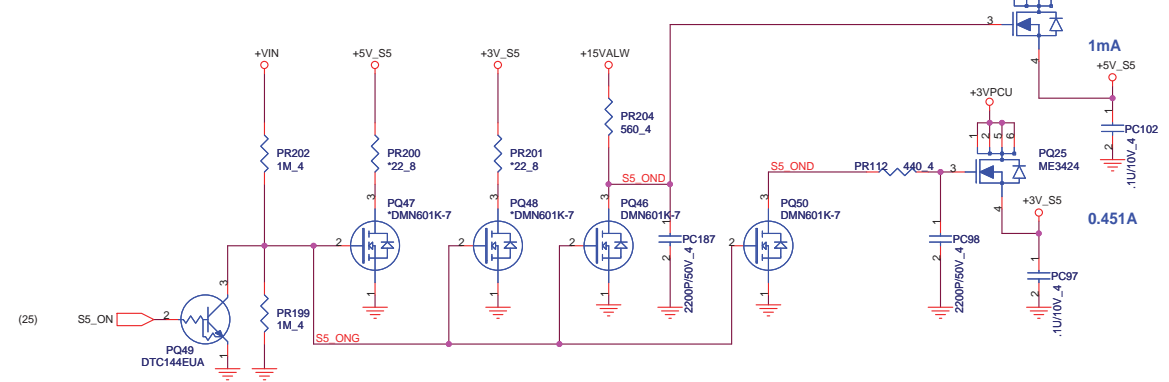
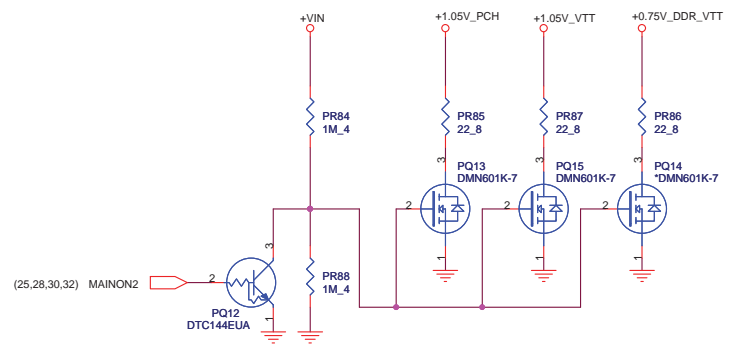
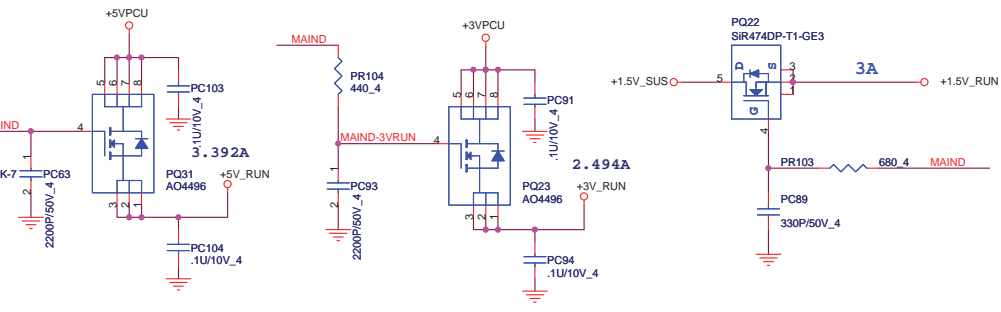
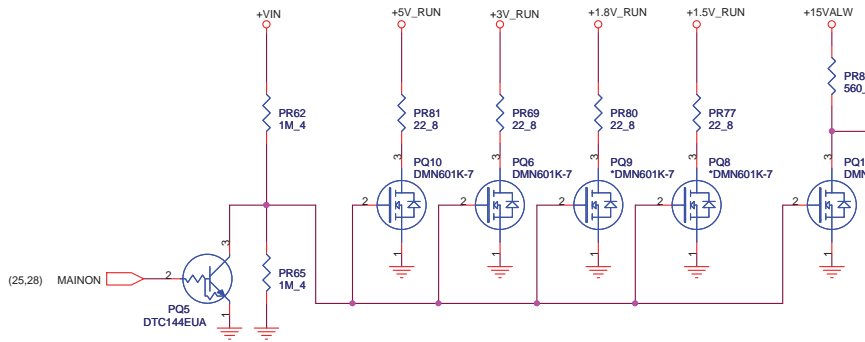
+1.05V_VTT +/- 5%
Countinue current:18.2A
Peak current:20A
OCP minimum 22A

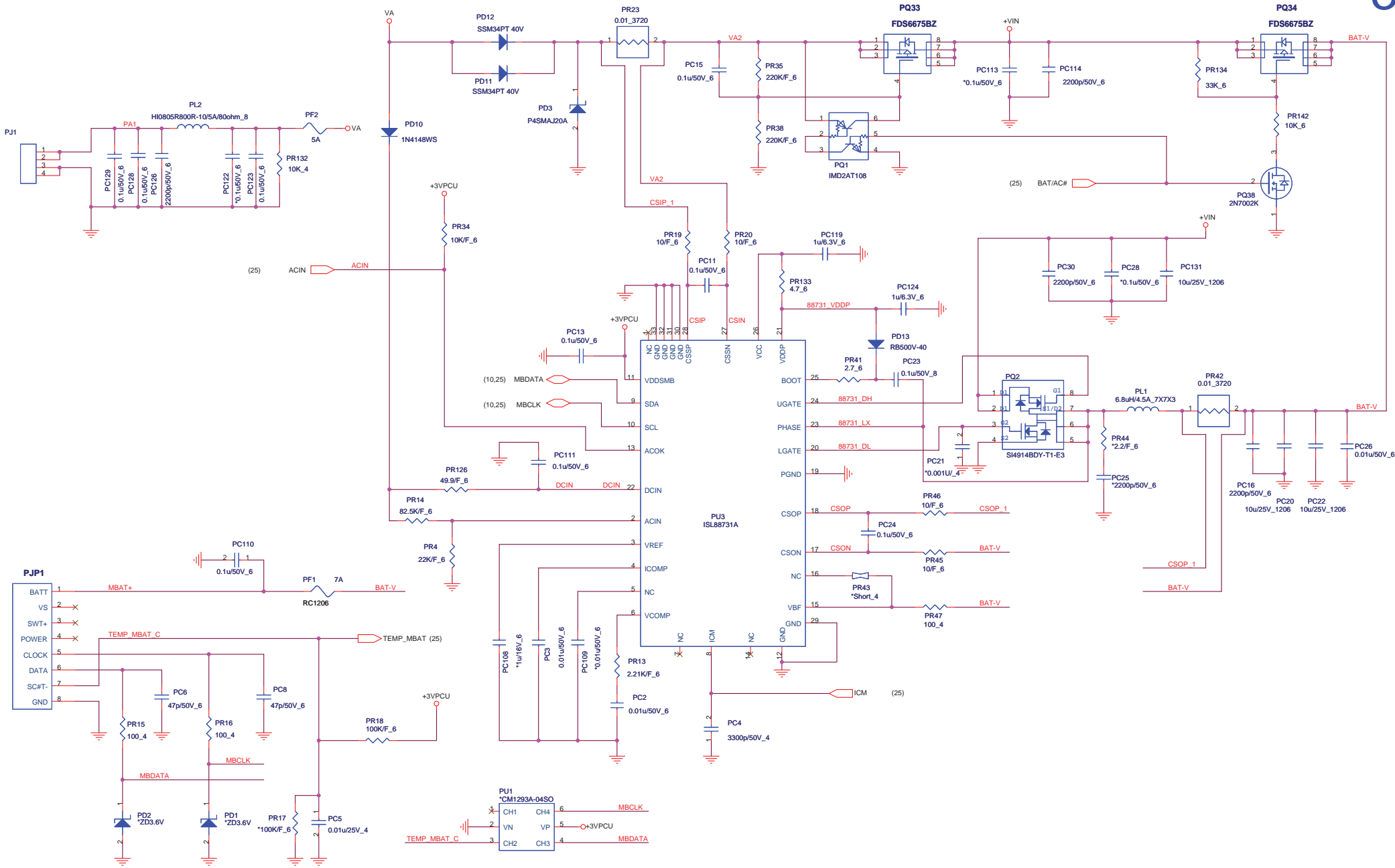
 Quanta Computer Inc. PROJECT : FHL		Size	Document Number	Rev	
		+1.05V_VTT (VT358)			1A
Date:	Friday, October 09, 2009	Sheet	30	of	37



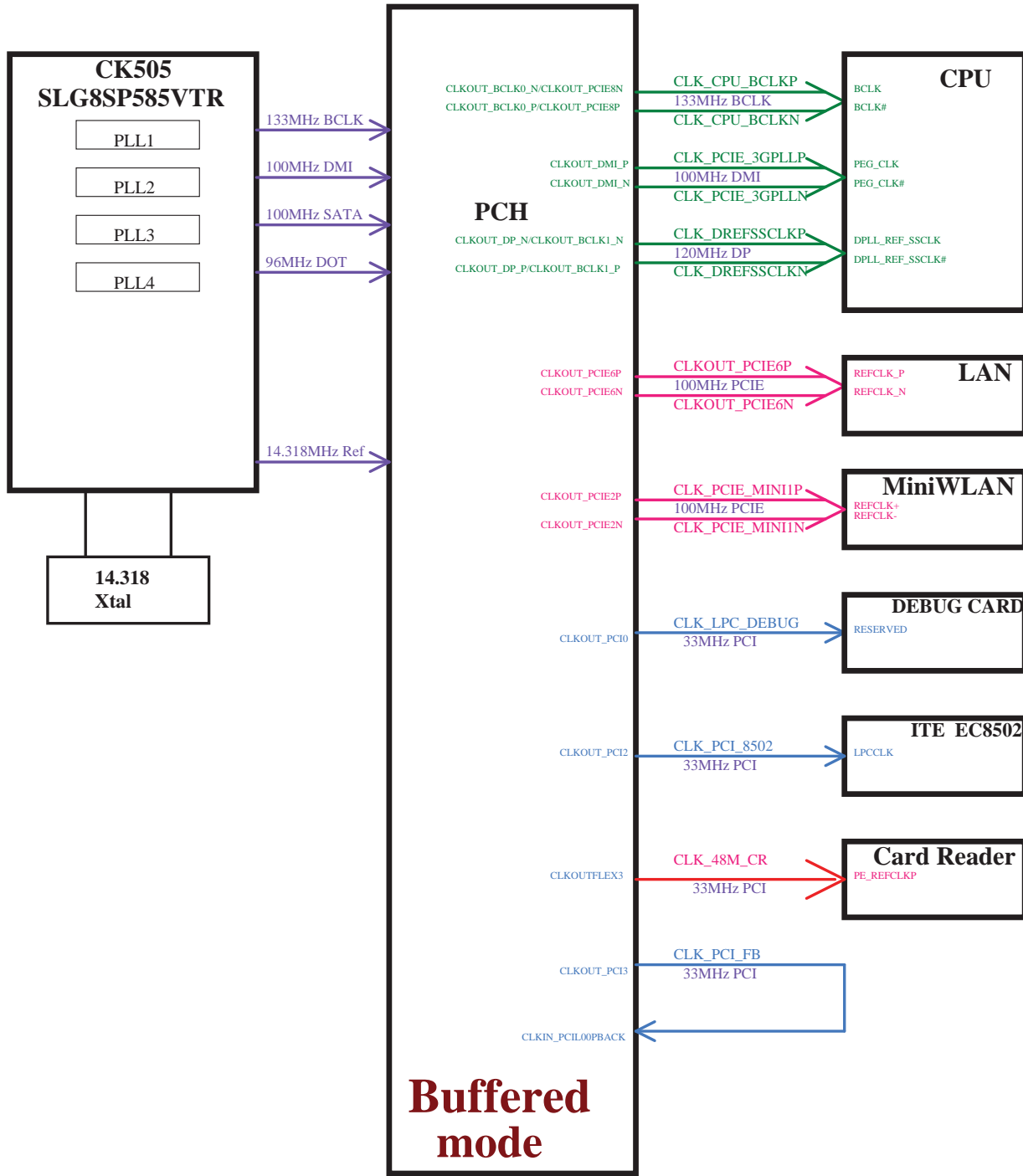
+1.5V_SUS +/- 5%
Continue current:6A
Peak current:12A
OCP minimum 15A







Quanta Computer Inc.		
PROJECT : FH1		
Size	Document Number	Rev
	CHARGER (ISL88731)	1A
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Power Tree Table

