Intel Calpella BlOCK DIAGRAM

INTEL DISCRETE SYSTEM DIAGRAM 01

FAN & THERMAL

CLOCK
SLG8SP585VTR
(QFN-32)

POWER

REGULATOR
+1.5V_SUS/+0.75V_DDR_VTT
+1.05V_PCH
+1.05V_VTT

CPU VR
DC/DC
+3VPCU/+5VPCU/

POWER

SYSTEM RESET CIRCUIT
BATT CHARGER
RUN POWER SW
+3V_S5/+5V_S5
+3V_SUS/+5V_SUS
+5V_RUN/+3V_RUN/+1.8V_RUN

AC/BATT CONNECTOR

CPU
Arrandale 35W
37.5mm X 37.5mm
(rPGA 989)

PCI-E x16

AMD
PARK-LP
23mm X 23mm
TDP 8W
(S3)

CRT
LVDS

CRT
LVDS

DDR3-SODIMM1 CHA
DDR3-SODIMM2 CHB
Dual Channel DDR3
1066 1.5V

DDR3 800MHz

VRAM
64Mx16x2,32bit

DMI X 4

PCH
82801IBM
(HM55)
27mm X 25mm

SATA-ODD
SATA-HDD
SATA

USB conn x 3
Card Reader SD MS CARD
RTS5159
USB2.0 x 3
USB2.0

LAN
Realtek 10/100/ LAN RTL8103EL
PCIEx1

MINI-CARD
WLAN
PCIEx2

IHDA
AUDIO/AMP
ALC269
Audio SPK conn
Audio Jacks

LPC
EC
ITE8502

SPI
FLASH
2Mbyts

18X8
Keyboard

SPI
FLASH
2Mbyts

PS/2
Touchpad

Quanta Computer Inc.
PROJECT : FH1A

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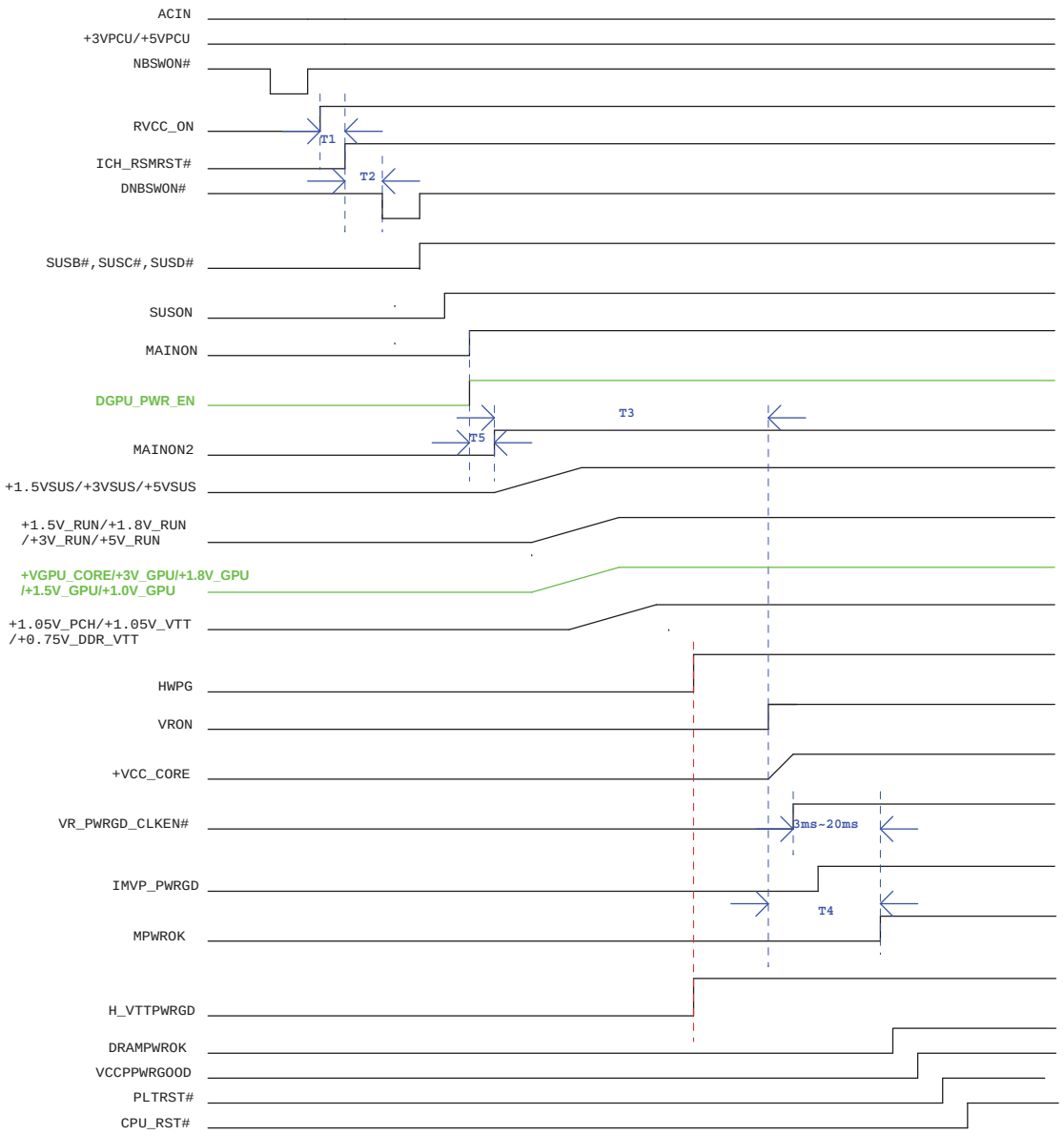
Power Sequence



T1: RVCCON TO RSMRST# = 30ms (spec:mini 10ms)
T2: RSMRST# TO-DNBSWON = 110ms (spec:mini 100ms)
T3: MAINON2 TO VRON = 110ms (spec:mini 99ms)
T4: VRON TO MPWROK = 10ms (HWPG NEED TO BE HIGH at that time)
Note: IMVP_CLK_EN# (inverted) assertion to SYS_PWROK/PCH_PWROK assertion.
SPEC:3ms~20ms
T5: MAINON to MAINON2 =500us

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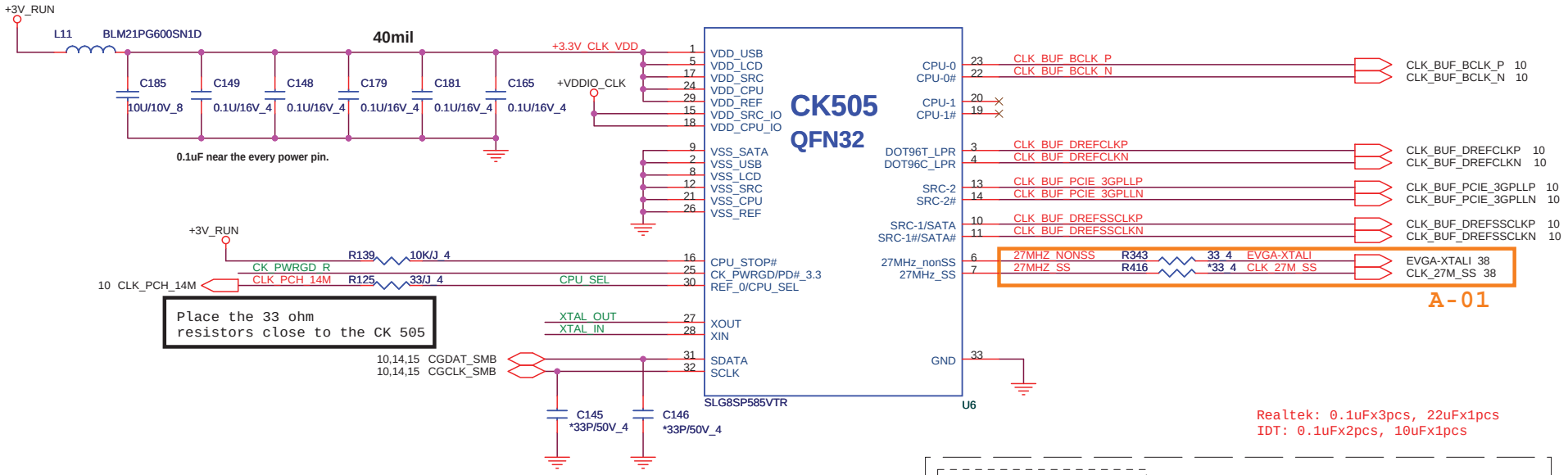
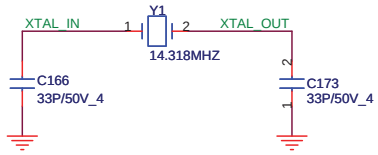
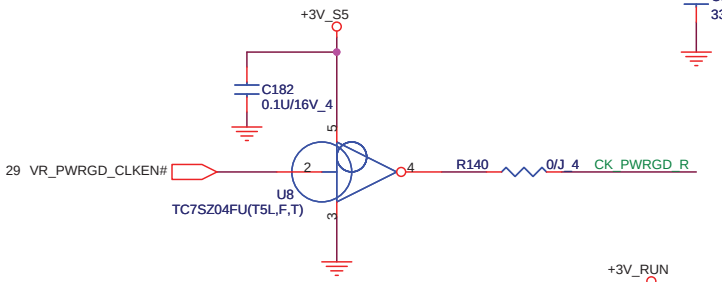
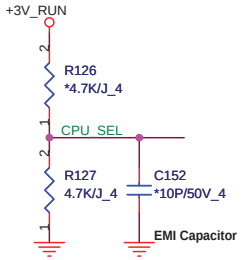




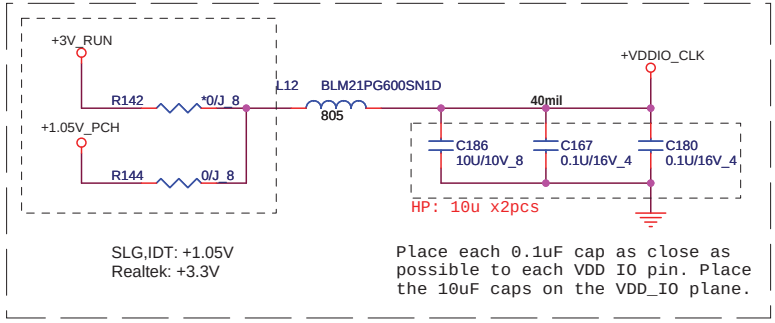




PIN 30	CPU_0	CPU_1
0(default)	133MHz	133MHz
1(0.7V-1.5V)	100MHz	100MHz

CPU_SEL:
SLG date sheet (V0.2) P15:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
Realtek date sheet(V1.2) P11:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
IDT date sheet(V0.7) P10:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.

Realtek: 0.1uFx3pcs, 22uFx1pcs
IDT: 0.1uFx2pcs, 10uFx1pcs



+VDDIO_CLK:
SLG date sheet (V0.2) P15: Min 1.05V,Max3.465V
Realtek date sheet(V1.2) P11: Min 1.05V,Max 3.3V
IDT date sheet(V0.7) P10: Min 0.9975V,Max 3.465V

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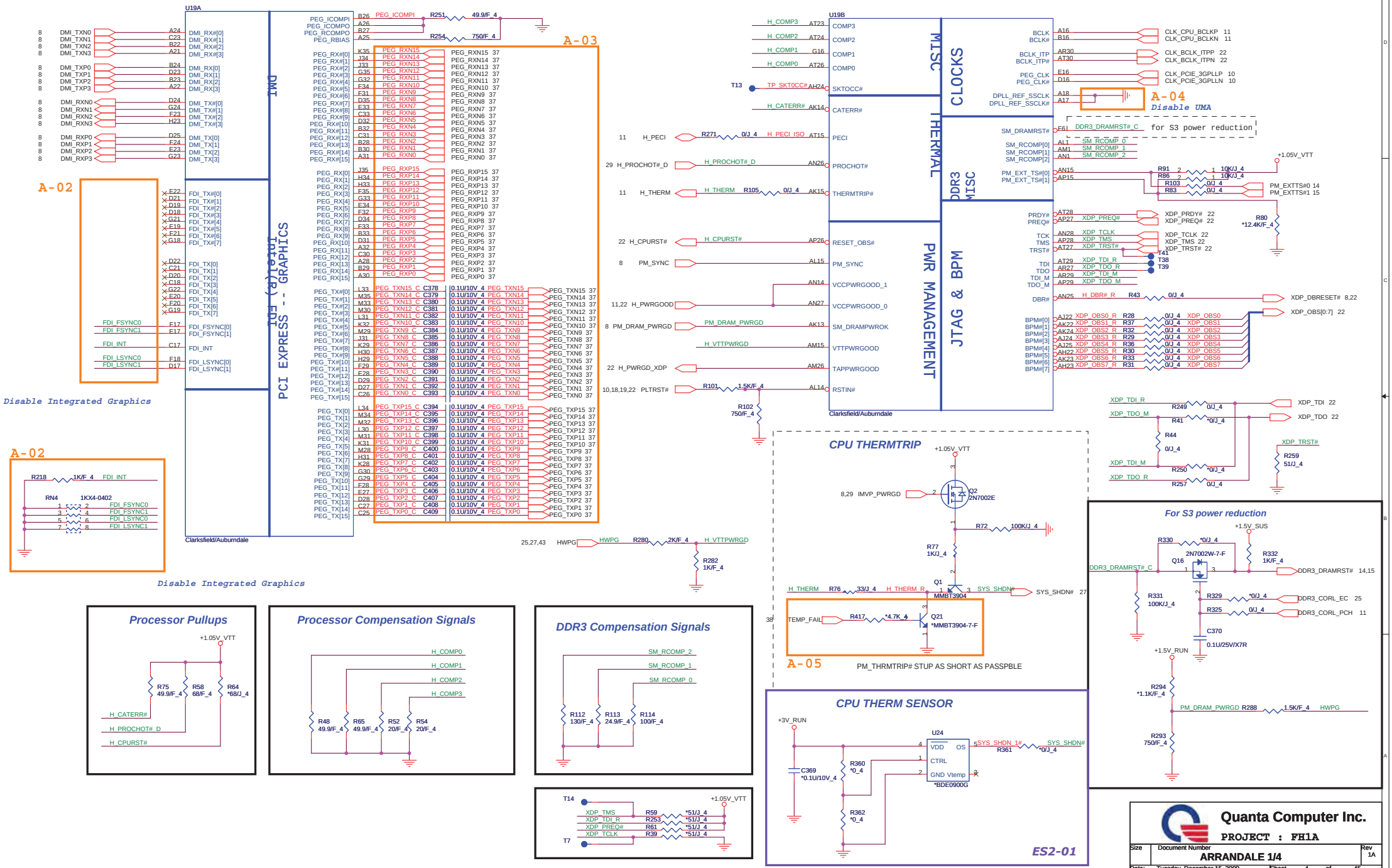

Quanta Computer Inc.

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	ARRANDALE 1/4	1A

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ARRANDALE PROCESSOR (DDR3)

05

U19C

DDR SYSTEM MEMORY A

14 M_A_DQ[63:0]

M_A_DQ0 A10 SA_DQ[0]
M_A_DQ1 C10 SA_DQ[1]
M_A_DQ2 C7 SA_DQ[2]
M_A_DQ3 A7 SA_DQ[3]
M_A_DQ4 B10 SA_DQ[4]
M_A_DQ5 D10 SA_DQ[5]
M_A_DQ6 E10 SA_DQ[6]
M_A_DQ7 A8 SA_DQ[7]
M_A_DQ8 D8 SA_DQ[8]
M_A_DQ9 F10 SA_DQ[9]
M_A_DQ10 E6 SA_DQ[10]
M_A_DQ11 E7 SA_DQ[11]
M_A_DQ12 E9 SA_DQ[12]
M_A_DQ13 B7 SA_DQ[13]
M_A_DQ14 E7 SA_DQ[14]
M_A_DQ15 C6 SA_DQ[15]
M_A_DQ16 H10 SA_DQ[16]
M_A_DQ17 G8 SA_DQ[17]
M_A_DQ18 K7 SA_DQ[18]
M_A_DQ19 J8 SA_DQ[19]
M_A_DQ20 G7 SA_DQ[20]
M_A_DQ21 G10 SA_DQ[21]
M_A_DQ22 J7 SA_DQ[22]
M_A_DQ23 J10 SA_DQ[23]
M_A_DQ24 L7 SA_DQ[24]
M_A_DQ25 M6 SA_DQ[25]
M_A_DQ26 M8 SA_DQ[26]
M_A_DQ27 L9 SA_DQ[27]
M_A_DQ28 L6 SA_DQ[28]
M_A_DQ29 K8 SA_DQ[29]
M_A_DQ30 N8 SA_DQ[30]
M_A_DQ31 P9 SA_DQ[31]
M_A_DQ32 AH5 SA_DQ[32]
M_A_DQ33 AF5 SA_DQ[33]
M_A_DQ34 AK6 SA_DQ[34]
M_A_DQ35 AK7 SA_DQ[35]
M_A_DQ36 AF6 SA_DQ[36]
M_A_DQ37 AG5 SA_DQ[37]
M_A_DQ38 AJ7 SA_DQ[38]
M_A_DQ39 AJ6 SA_DQ[39]
M_A_DQ40 AJ10 SA_DQ[40]
M_A_DQ41 AJ9 SA_DQ[41]
M_A_DQ42 AL10 SA_DQ[42]
M_A_DQ43 AK12 SA_DQ[43]
M_A_DQ44 AK8 SA_DQ[44]
M_A_DQ45 AL7 SA_DQ[45]
M_A_DQ46 AK11 SA_DQ[46]
M_A_DQ47 AL8 SA_DQ[47]
M_A_DQ48 AN8 SA_DQ[48]
M_A_DQ49 AM10 SA_DQ[49]
M_A_DQ50 AR11 SA_DQ[50]
M_A_DQ51 AL11 SA_DQ[51]
M_A_DQ52 AM9 SA_DQ[52]
M_A_DQ53 AN9 SA_DQ[53]
M_A_DQ54 AT11 SA_DQ[54]
M_A_DQ55 AP12 SA_DQ[55]
M_A_DQ56 AM12 SA_DQ[56]
M_A_DQ57 AN12 SA_DQ[57]
M_A_DQ58 AM13 SA_DQ[58]
M_A_DQ59 AT14 SA_DQ[59]
M_A_DQ60 AT12 SA_DQ[60]
M_A_DQ61 AL13 SA_DQ[61]
M_A_DQ62 AR14 SA_DQ[62]
M_A_DQ63 AP14 SA_DQ[63]

14 M_A_BS0 AC3 SA_BS[0]
14 M_A_BS1 AB2 SA_BS[1]
14 M_A_BS2 U7 SA_BS[2]

14 M_A_CAS# AE1 SA_CAS#
14 M_A_RAS# AB3 SA_RAS#
14 M_A_WE# AE9 SA_WE#

SA_CK[0] AA6 M_A_CLKP0 14
SA_CK#[0] AA7 M_A_CLKN0 14
SA_CKE[0] P7 M_A_CKE0 14

SA_CK[1] Y6 M_A_CLKP1 14
SA_CK#[1] Y5 M_A_CLKN1 14
SA_CKE[1] P6 M_A_CKE1 14

SA_CS#[0] AE2 M_A_CS0# 14
SA_CS#[1] AE8 M_A_CS1# 14

SA_ODT[0] AD8 M_A_ODT0 14
SA_ODT[1] AF9 M_A_ODT1 14

SA_DM[0] B9 M_A_DM0
SA_DM[1] D7 M_A_DM1
SA_DM[2] H7 M_A_DM2
SA_DM[3] M7 M_A_DM3
SA_DM[4] AG6 M_A_DM4
SA_DM[5] AM7 M_A_DM5
SA_DM[6] AN10 M_A_DM6
SA_DM[7] AN13 M_A_DM7
M_A_DM[7:0] 14

DM signals are not present on Clarkfield processor. All DM signal can be left as NC on Clarkfield and connect directly to GND on So-DIMM side for Clarkfield design only

SA_DQS#[0] C9 M_A_DQSN0
SA_DQS#[1] F8 M_A_DQSN1
SA_DQS#[2] J9 M_A_DQSN2
SA_DQS#[3] N9 M_A_DQSN3
SA_DQS#[4] AH7 M_A_DQSN4
SA_DQS#[5] AK9 M_A_DQSN5
SA_DQS#[6] AP11 M_A_DQSN6
SA_DQS#[7] AT13 M_A_DQSN7
M_A_DQSN[7:0] 14

SA_DQS[0] C8 M_A_DQSP0
SA_DQS[1] F9 M_A_DQSP1
SA_DQS[2] H9 M_A_DQSP2
SA_DQS[3] M9 M_A_DQSP3
SA_DQS[4] AH8 M_A_DQSP4
SA_DQS[5] AK10 M_A_DQSP5
SA_DQS[6] AN11 M_A_DQSP6
SA_DQS[7] AR13 M_A_DQSP7
M_A_DQSP[7:0] 14

SA_MA[0] Y3 M_A_A0
SA_MA[1] W1 M_A_A1
SA_MA[2] AA8 M_A_A2
SA_MA[3] AA3 M_A_A3
SA_MA[4] V1 M_A_A4
SA_MA[5] AA9 M_A_A5
SA_MA[6] V8 M_A_A6
SA_MA[7] T1 M_A_A7
SA_MA[8] Y9 M_A_A8
SA_MA[9] U6 M_A_A9
SA_MA[10] AD4 M_A_A10
SA_MA[11] T2 M_A_A11
SA_MA[12] U3 M_A_A12
SA_MA[13] AG8 M_A_A13
SA_MA[14] T3 M_A_A14
SA_MA[15] V9 M_A_A15
M_A_A[15:0] 14

Clarksfield/Auburndale

Channel A DQ[15,32,48,54], DM[5]
Requires minimum 12mils spacing
with all other signals, including data signals.

U19D

DDR SYSTEM MEMORY - B

15 M_B_DQ[63:0]

M_B_DQ0 B5 SB_DQ[0]
M_B_DQ1 A5 SB_DQ[1]
M_B_DQ2 C3 SB_DQ[2]
M_B_DQ3 B3 SB_DQ[3]
M_B_DQ4 E4 SB_DQ[4]
M_B_DQ5 A6 SB_DQ[5]
M_B_DQ6 A4 SB_DQ[6]
M_B_DQ7 C4 SB_DQ[7]
M_B_DQ8 D1 SB_DQ[8]
M_B_DQ9 D2 SB_DQ[9]
M_B_DQ10 F2 SB_DQ[10]
M_B_DQ11 F1 SB_DQ[11]
M_B_DQ12 C2 SB_DQ[12]
M_B_DQ13 F5 SB_DQ[13]
M_B_DQ14 F3 SB_DQ[14]
M_B_DQ15 G4 SB_DQ[15]
M_B_DQ16 H6 SB_DQ[16]
M_B_DQ17 G2 SB_DQ[17]
M_B_DQ18 J6 SB_DQ[18]
M_B_DQ19 J3 SB_DQ[19]
M_B_DQ20 G1 SB_DQ[20]
M_B_DQ21 G5 SB_DQ[21]
M_B_DQ22 J2 SB_DQ[22]
M_B_DQ23 J1 SB_DQ[23]
M_B_DQ24 J5 SB_DQ[24]
M_B_DQ25 K2 SB_DQ[25]
M_B_DQ26 L3 SB_DQ[26]
M_B_DQ27 M1 SB_DQ[27]
M_B_DQ28 K5 SB_DQ[28]
M_B_DQ29 K4 SB_DQ[29]
M_B_DQ30 M4 SB_DQ[30]
M_B_DQ31 N5 SB_DQ[31]
M_B_DQ32 AF3 SB_DQ[32]
M_B_DQ33 AG1 SB_DQ[33]
M_B_DQ34 AJ3 SB_DQ[34]
M_B_DQ35 AK1 SB_DQ[35]
M_B_DQ36 AG4 SB_DQ[36]
M_B_DQ37 AG3 SB_DQ[37]
M_B_DQ38 AJ4 SB_DQ[38]
M_B_DQ39 AH4 SB_DQ[39]
M_B_DQ40 AK3 SB_DQ[40]
M_B_DQ41 AK4 SB_DQ[41]
M_B_DQ42 AM6 SB_DQ[42]
M_B_DQ43 AN2 SB_DQ[43]
M_B_DQ44 AK5 SB_DQ[44]
M_B_DQ45 AK2 SB_DQ[45]
M_B_DQ46 AM4 SB_DQ[46]
M_B_DQ47 AM3 SB_DQ[47]
M_B_DQ48 AP3 SB_DQ[48]
M_B_DQ49 AN5 SB_DQ[49]
M_B_DQ50 AT4 SB_DQ[50]
M_B_DQ51 AN6 SB_DQ[51]
M_B_DQ52 AN4 SB_DQ[52]
M_B_DQ53 AN3 SB_DQ[53]
M_B_DQ54 AT5 SB_DQ[54]
M_B_DQ55 AT6 SB_DQ[55]
M_B_DQ56 AN7 SB_DQ[56]
M_B_DQ57 AP6 SB_DQ[57]
M_B_DQ58 AP8 SB_DQ[58]
M_B_DQ59 AT9 SB_DQ[59]
M_B_DQ60 AT7 SB_DQ[60]
M_B_DQ61 AP9 SB_DQ[61]
M_B_DQ62 AR10 SB_DQ[62]
M_B_DQ63 AT10 SB_DQ[63]

15 M_B_BS0 AB1 SB_BS[0]
15 M_B_BS1 W5 SB_BS[1]
15 M_B_BS2 R7 SB_BS[2]

15 M_B_CAS# AC5 SB_CAS#
15 M_B_RAS# Y7 SB_RAS#
15 M_B_WE# AC6 SB_WE#

SB_CK[0] W8 M_B_CLKP0 15
SB_CK#[0] W9 M_B_CLKN0 15
SB_CKE[0] M3 M_B_CKE0 15

SB_CK[1] V7 M_B_CLKP1 15
SB_CK#[1] V6 M_B_CLKN1 15
SB_CKE[1] M2 M_B_CKE1 15

SB_CS#[0] AB8 M_B_CS0# 15
SB_CS#[1] AD6 M_B_CS1# 15

SB_ODT[0] AC7 M_B_ODT0 15
SB_ODT[1] AD1 M_B_ODT1 15

SB_DM[0] D4 M_B_DM0
SB_DM[1] F1 M_B_DM1
SB_DM[2] H3 M_B_DM2
SB_DM[3] K1 M_B_DM3
SB_DM[4] AH1 M_B_DM4
SB_DM[5] AL2 M_B_DM5
SB_DM[6] AR4 M_B_DM6
SB_DM[7] AT8 M_B_DM7
M_B_DM[7:0] 15

DM signals are not present on Clarkfield processor. All DM signal can be left as NC on Clarkfield and connect directly to GND on So-DIMM side for Clarkfield design only

SB_DQS#[0] D5 M_B_DQSN0
SB_DQS#[1] F4 M_B_DQSN1
SB_DQS#[2] J4 M_B_DQSN2
SB_DQS#[3] L4 M_B_DQSN3
SB_DQS#[4] AH2 M_B_DQSN4
SB_DQS#[5] AL4 M_B_DQSN5
SB_DQS#[6] AR5 M_B_DQSN6
SB_DQS#[7] AR8 M_B_DQSN7
M_B_DQSN[7:0] 15

SB_DQS[0] C5 M_B_DQSP0
SB_DQS[1] E3 M_B_DQSP1
SB_DQS[2] H4 M_B_DQSP2
SB_DQS[3] M5 M_B_DQSP3
SB_DQS[4] AG2 M_B_DQSP4
SB_DQS[5] AL5 M_B_DQSP5
SB_DQS[6] AP5 M_B_DQSP6
SB_DQS[7] AR7 M_B_DQSP7
M_B_DQSP[7:0] 15

SB_MA[0] U5 M_B_A0
SB_MA[1] V2 M_B_A1
SB_MA[2] T5 M_B_A2
SB_MA[3] V3 M_B_A3
SB_MA[4] R1 M_B_A4
SB_MA[5] T8 M_B_A5
SB_MA[6] R2 M_B_A6
SB_MA[7] R6 M_B_A7
SB_MA[8] R4 M_B_A8
SB_MA[9] R5 M_B_A9
SB_MA[10] AB5 M_B_A10
SB_MA[11] P3 M_B_A11
SB_MA[12] R3 M_B_A12
SB_MA[13] AF7 M_B_A13
SB_MA[14] P5 M_B_A14
SB_MA[15] N1 M_B_A15
M_B_A[15:0] 15

Clarksfield/Auburndale

Channel B DQ[16,18,36,42,56,57,60,61,62]
Requires minimum 12mils spacing
with all other signals, including data signals.

Quanta Computer Inc.

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	ARRANDALE 2/4	1A
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CPU Core Power

+VCC_CORE=4.8 max

ARRANDALE PROCESSOR (GRAPHICS POWER)

U19F

+VCC_CORE

AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26 AF35 AF34 AF33 AF32 AF31 AF30 AF29 AF28 AF27 AF26 AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26 AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26 AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26 V35 V34 V33 V32 V31 V30 V29 V28 V27 V26 U35 U34 U33 U32 U31 U30 U29 U28 U27 U26 R35 R34 R33 R32 R31 R30 R29 R28 R27 R26 P35 P34 P33 P32 P31 P30 P29 P28 P27 P26
VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

1.1V RAIL POWER

CPU CORE SUPPLY

+1.05V_VTT=1.8 max

+1.05V_VTT

VTT0_1 VTT0_2 VTT0_3 VTT0_4 VTT0_5 VTT0_6 VTT0_7 VTT0_8 VTT0_9 VTT0_10 VTT0_11 VTT0_12 VTT0_13 VTT0_14 VTT0_15 VTT0_16 VTT0_17 VTT0_18 VTT0_19 VTT0_20 VTT0_21 VTT0_22 VTT0_23 VTT0_24 VTT0_25 VTT0_26 VTT0_27 VTT0_28 VTT0_29 VTT0_30 VTT0_31 VTT0_32
AH14 AH12 AH11 AH10 J14 J13 H14 H12 G14 G13 G12 G11 F14 F13 F12 F11 E14 E12 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11

C318 10U/6.3V_8 C103 10U/6.3V_8 C107 10U/6.3V_8 C311 10U/6.3V_8 C309 *10U/6.3V_8
C102 10U/6.3V_8 C105 10U/6.3V_8 C326 10U/6.3V_8 C99 10U/6.3V_8
C329 22U/6.3V_8 C313 22U/6.3V_8 C304 22U/6.3V_8
C308 22U/6.3V_8 C96 22U/6.3V_8

VTT0_33 VTT0_34 VTT0_35 VTT0_36 VTT0_37 VTT0_38 VTT0_39 VTT0_40 VTT0_41 VTT0_42 VTT0_43 VTT0_44
AF10 AF10 AC10 AB10 Y10 W10 U10 T10 J12 J11 J16 J15

VTT0_43,VTT0_44:(Intel feedback)
They are connected to hidden page for
intel validation purpose.

POWER

CPU VIDS

PSI# AN33 H_PSI# → H_PSI# 29

VID[0] AK35 VID0
VID[1] AK33 VID1
VID[2] AK34 VID2
VID[3] AL35 VID3
VID[4] AL33 VID4
VID[5] AM33 VID5
VID[6] AM35 VID6
PROC_DPRSLPVR AM34 DPRSLPVR
VID0 29 VID1 29 VID2 29 VID3 29 VID4 29 VID5 29 VID6 29 DPRSLPVR 29

VTT_SELECT G15 → H_VTTVID1 30

SENSE LINES

ISENSE AN35 → I_MON 29

VCC_SENSE AJ34 → VCCSENSE 29
VSS_SENSE AJ35 → VSSSENSE 29

VTT_SENSE B15 → VTT_SENSE 30
VSS_SENSE_VTT A15 → VSS_SENSE_VTT 30

VSS_SENSE_VTT:
SC(V1.0)P20
Connect VSS_SENSE_VTT to GND
or can be left floating.
Note: CRB has the VSS_SENSE_VTT floating.

+VCC_CORE

R216 100/F_4
R217 100/F_4

VCC_SENSE & VSS_SENSE:
SC(V1.0)P19
100- ±1% pull-down to GND near processor

PROC_DPRSLPVR:
SC(V1.0)P19:
It is important to have the resistor stuffing options in the design for the Turbo functionality. The stuffing and no-stuffing of the resistors will depend on the POC configuration of AUB and CFD
CRB(V1.0)P67:
uses 1K pull-up and pull-down resistors
CRB default setting is "1"

A-06

U19G

VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36
AT21 AT19 AT18 AT16 AR21 AR19 AR18 AR16 AP21 AP19 AP18 AP16 AN21 AN19 AN18 AN16 AM21 AM19 AM18 AM16 AL21 AL19 AL18 AL16 AK21 AK19 AK18 AK16 AJ21 AJ19 AJ18 AJ16 AH21 AH19 AH18 AH16

GRAPHICS

VTT1_45 VTT1_46 VTT1_47
J24 J23 H25

PDI

VTT1_48 VTT1_49 VTT1_50 VTT1_51 VTT1_52 VTT1_53 VTT1_54 VTT1_55 VTT1_56 VTT1_57 VTT1_58
K26 J27 J26 J25 H27 G28 G27 G26 F26 E26 E25

PEG & DMI

POWER

SENSE LINES

VAXG_SENSE AR22
VSSAXG_SENSE AT22

GRAPHICS VIDs

GFX_VID[0] AM22
GFX_VID[1] AP22
GFX_VID[2] AN22
GFX_VID[3] AP23
GFX_VID[4] AM23
GFX_VID[5] AP24
GFX_VID[6] AN24

GFX_VR_EN AR25
GFX_DPRSLPVR AT25
GFX_IMON AM24

R220 1K/F_4

A-06
Disable UMA

DDR3 - 1.5V RAILS

VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9 VDDQ10 VDDQ11 VDDQ12 VDDQ13 VDDQ14 VDDQ15 VDDQ16 VDDQ17 VDDQ18
AJ1 AF1 AE7 AE4 AC1 AB7 AB4 Y1 W7 W4 U1 T7 T4 P1 N7 N4 L1 H1

+1.5V_RUN

C125 1U/6.3V_4 C124 1U/6.3V_4 C127 1U/6.3V_4 C128 1U/6.3V_4 C126 1U/6.3V_4
C122 330U/2.5V_7343 7343 2.5
C121 22U/6.3V_8
C120 22U/6.3V_8

1.1V

VTT0_59 VTT0_60 VTT0_61 VTT0_62
P10 N10 L10 K10

+1.05V_VTT

C104 10U/6.3V_8 C106 10U/6.3V_8 C110 *330U/2.5V_7343

VTT1_63 VTT1_64 VTT1_65 VTT1_66 VTT1_67 VTT1_68
J22 J20 J18 H21 H20 H19

C330 22U/6.3V_8 C314 22U/6.3V_8

1.8V

VCCPLL1 VCCPLL2 VCCPLL3
L26 L27 M26

+1.8V_RUN

C42 1U/6.3V_4 C50 1U/6.3V_4 C65 2.2U/6.3V_6 C66 4.7U/6.3V_6 C297 22U/6.3V_8

+VCC_CORE

C281 22U/6.3V_8 C54 22U/6.3V_8 C302 22U/6.3V_8 C52 22U/6.3V_8 C53 22U/6.3V_8 C291 22U/6.3V_8
C276 22U/6.3V_8 C38 22U/6.3V_8 C59 22U/6.3V_8 C58 22U/6.3V_8 C280 22U/6.3V_8 C285 22U/6.3V_8
C79 10U/6.3V_8 C56 10U/6.3V_8 C36 10U/6.3V_8 C81 10U/6.3V_8 C55 10U/6.3V_8 C299 10U/6.3V_8
C301 10U/6.3V_8 C300 10U/6.3V_8 C286 10U/6.3V_8 C80 10U/6.3V_8 C35 10U/6.3V_8 C82 10U/6.3V_8
C57 10U/6.3V_8 C37 10U/6.3V_8 C78 10U/6.3V_8 C303 10U/6.3V_8
C277 *470U/6.3V_7343 C90 *470U/6.3V_7343

+1.05V_VTT

R225 1K/J_4 R227 1K/J_4 R230 1K/J_4 R233 1K/J_4 R236 1K/J_4 R239 1K/J_4 R243 1K/J_4 R208 1K/J_4 R209 1K/J_4
R226 1K/J_4 R228 1K/J_4 R231 1K/J_4 R234 1K/J_4 R237 1K/J_4 R240 1K/J_4 R244 1K/J_4 R213 1K/J_4 R214 1K/J_4

VID0 VID1 VID2 VID3 VID4 VID5 VID6 DPRSLPVR H_PSI#

Note:
For Validating IMVP VR R814 should be STUFF and R827 NO_STUFF

For S3 power reduction

Check to ensure that 4 stitching caps per SODIMM connector between SODIMM 1.5V and GND are placed as close as possible to the connectors – caps should be evenly distributed between the connectors

Clarksfield/Auburndale

AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

Quanta Computer Inc.
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	ARRANDALE 3/4	1A
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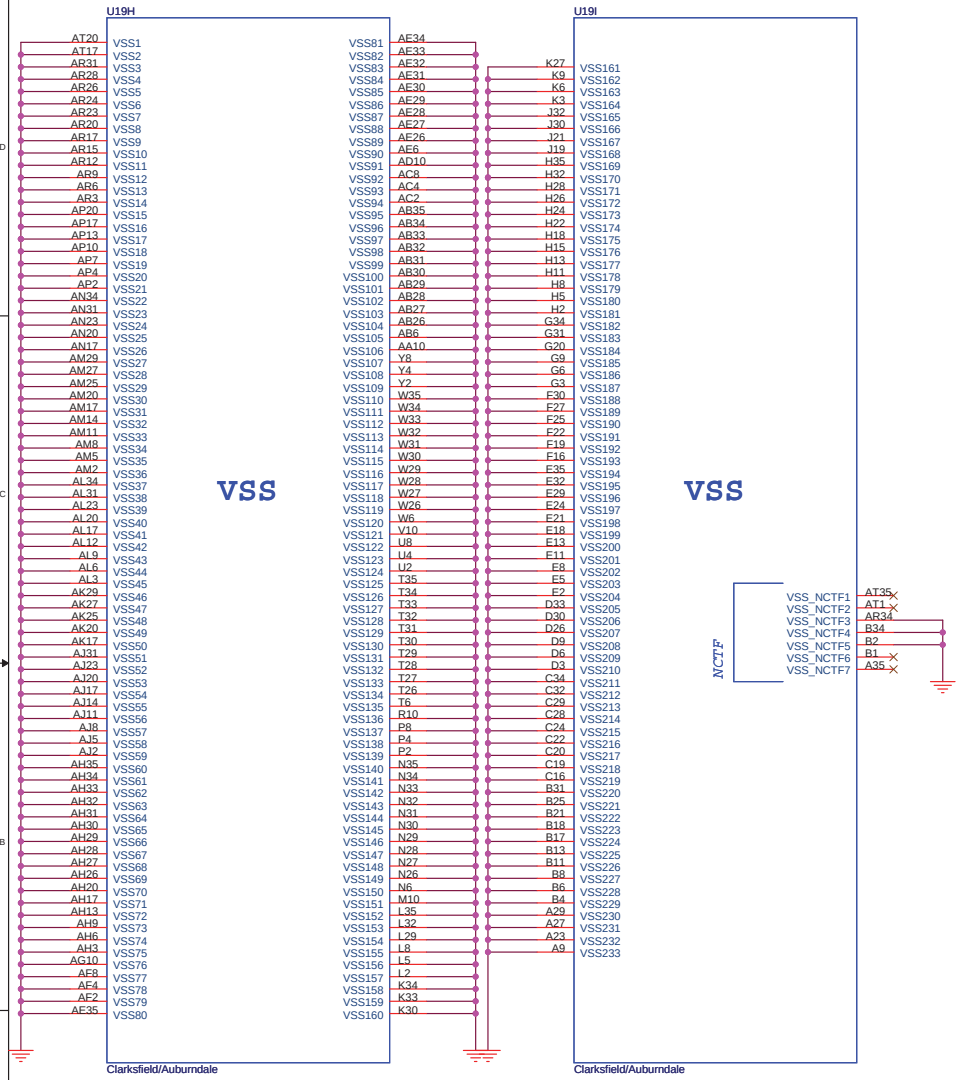
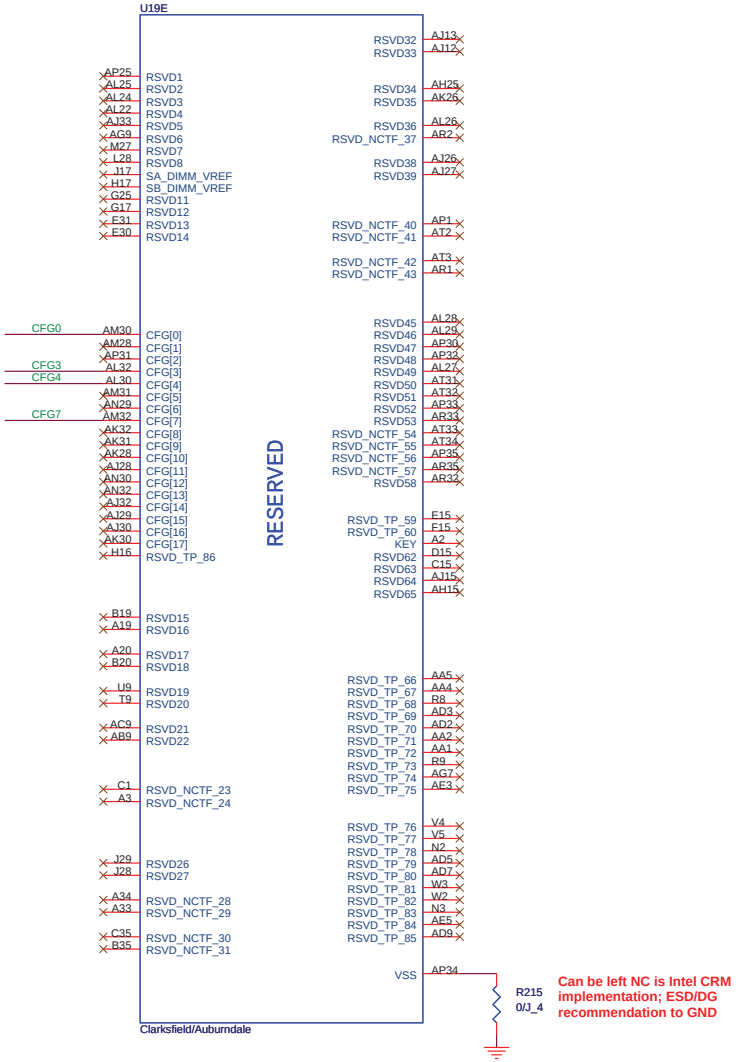
ARRANDALE PROCESSOR (GND)



ARRANDALE PROCESSOR(RESERVED, CFG)



Can be left NC is Intel CRM implementation; ESD/DG recommendation to GND

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

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PROJECT : FH1A

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	ARRANDALE 4/4	1A

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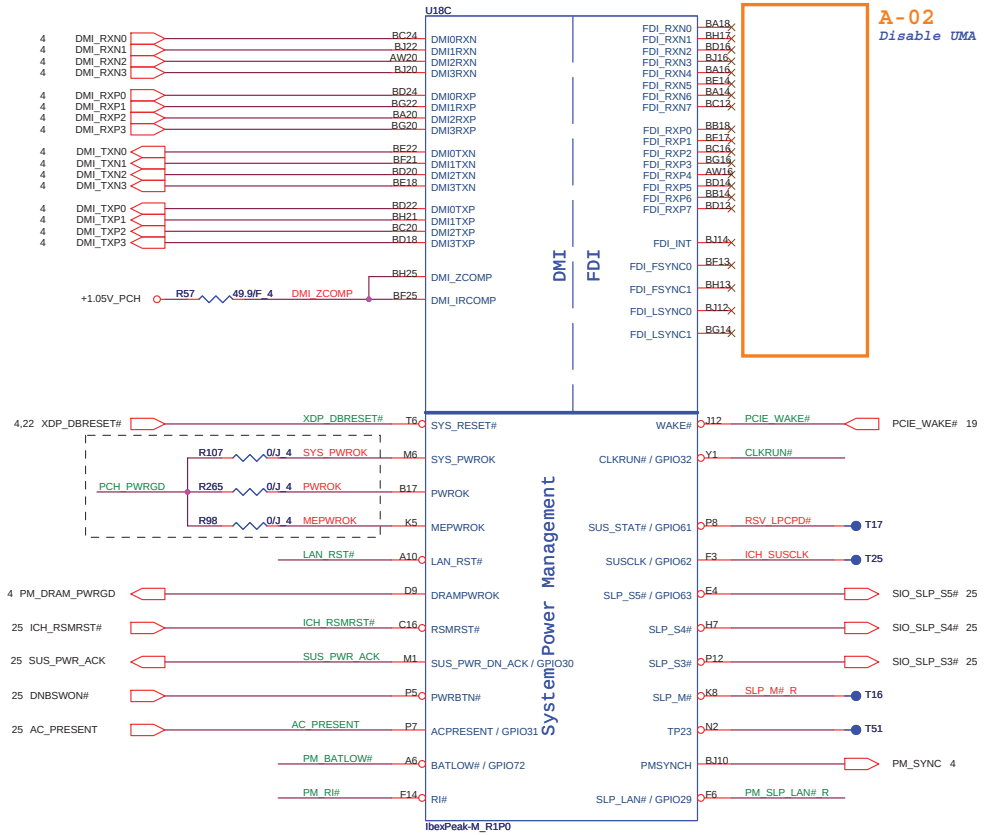
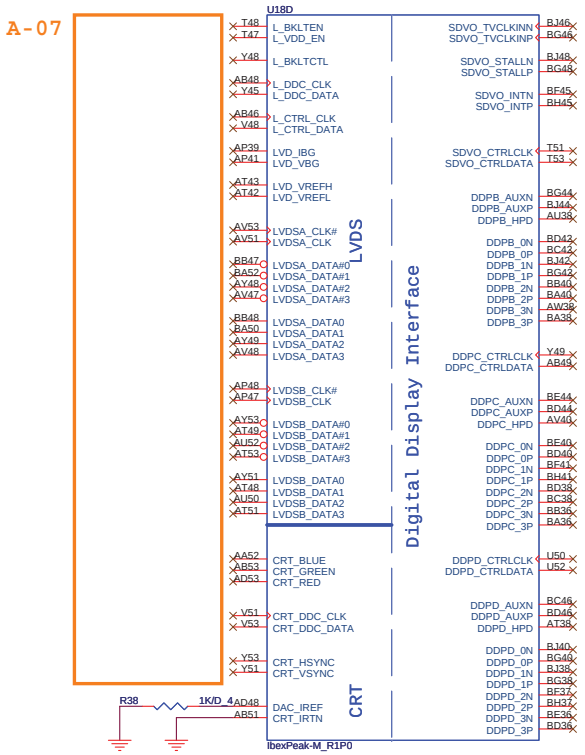
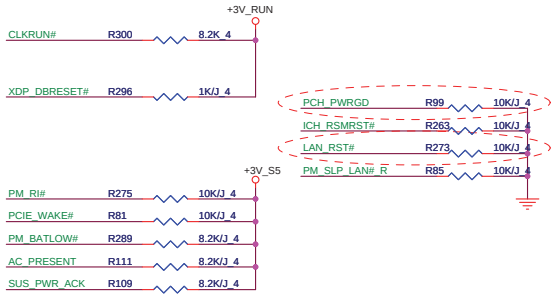
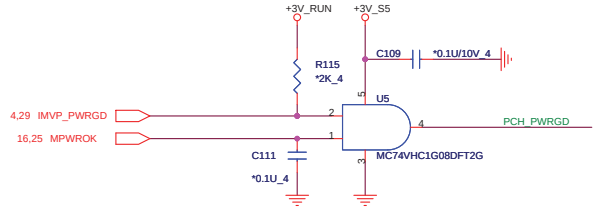
IBEX PEAK-M (DMI,FDI,GPIO)



IBEX PEAK-M (LVDS,DDI)







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PROJECT : FH1A

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	IBEX PEAK-M 1/6	1A
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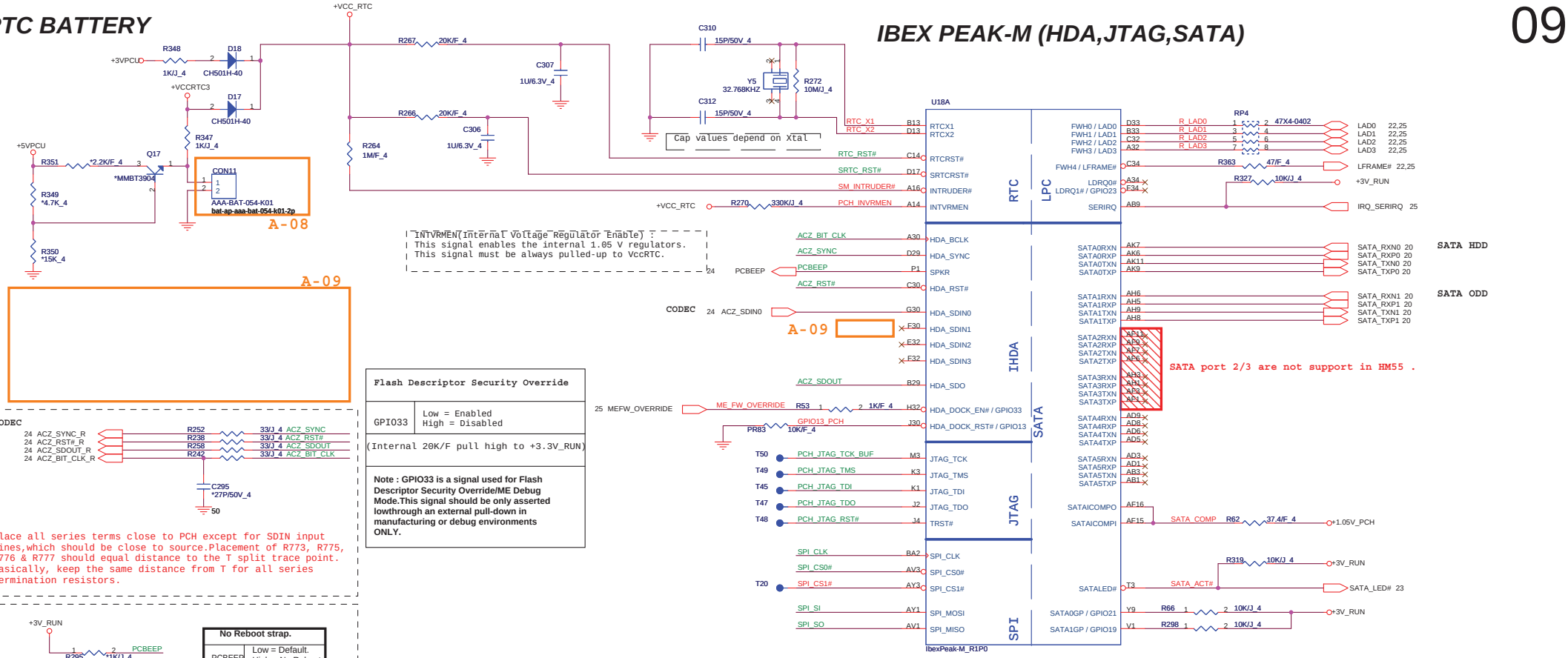
RTC BATTERY

IBEX PEAK-M (HDA,JTAG,SATA)

09

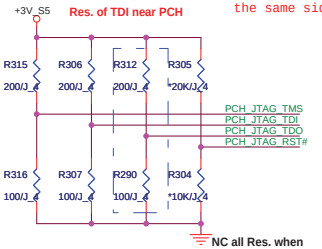


Flash Descriptor Security Override	
GPIO33	Low = Enabled High = Disabled
(Internal 20K/F pull high to +3.3V_RUN)	

Note : GPIO33 is a signal used for Flash Descriptor Security Override/ME Debug Mode.This signal should be only asserted lowthrough an external pull-down in manufacturing or debug environments ONLY.

Place all series terms close to PCH except for SDIN input lines,which should be close to source.Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

No Reboot strap.	
PCBEEP	Low = Default. High = No Reboot.



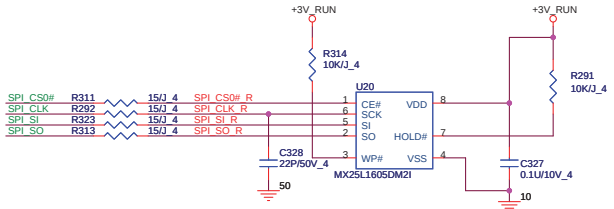
JTAG
Test Pads are need to put on the same side of mother board.

NC all Res. when PCH is production stage.

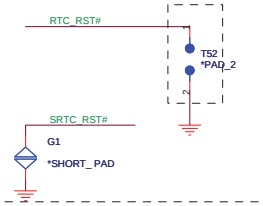
Res. of TDO
PCH ES1 stage : NC
PCH ES2 stage : pop

Note : Only pop when PCH is production stage & need "JTAG boundary Scan". Remember to depop XDP side Res.

For PCH 32Mbit (4M Byte)



RESET JUMP (Near ROOM DOOR)



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	IBEX PEAK-M 2/6	1A

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IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (PCI-E,SMBUS,CLK)

Place TX DC blocking caps close PCH.

PCIE port 7/8 are not support in HM55 .

USB port 6/7 are not support in HM55 .

USB PORT 1(DB)
USB PORT 2(MB)
USB PORT 4(MB)
CAMERA
BT
WLAN
CARD READER

PCIRST#:
DG(V1.0) P277
Can be left unconnected.

PAR:
SC(V1.0) P36
Can be left unconnected
if not using PCI.

PME:
DG(V1.0) P277
Can be left unconnected.

CLKOUT_PCI[0..4]:
22 ohm series resistor is recommend
(single & double load) on PDG v1.1

OC0#~OC7#:
DG(V1.0)P214
Pin Default Port Mapping
OC0# Port0,Port1
OC1# Port2,Port3
OC2# Port4,Port5

CLKOUT_PEG_A_P/N,CLKOUT_PEG_B_P/N,
CLKOUT_DMI_P/N,support GEN-1 and GEN-2

CLKOUTFLEX3:
EDS(V1.0) :support 48MHz
33MHz and 14.31818MHz.

CLKOUTFLEX[0..3]:
PDG v1.1: 22 ohm series resistor is
recommend (PCI & non PCI routing,
single & double load)

Reserve capacitor pads for improving WWAN.

Non-iAMT

Add Buffers as needed for Loading and fanout concerns.

PCIE Clock Request

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +V3.3A.PCIECLKRQ{1,2} should have a 10K pull-up to +3.3S

Boot BIOS Strap

PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	PCI
1	0	Reserved (NAND)
1	1	SPI

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Size: Document Number: IBEX PEAK-M 3/6 Rev 1A
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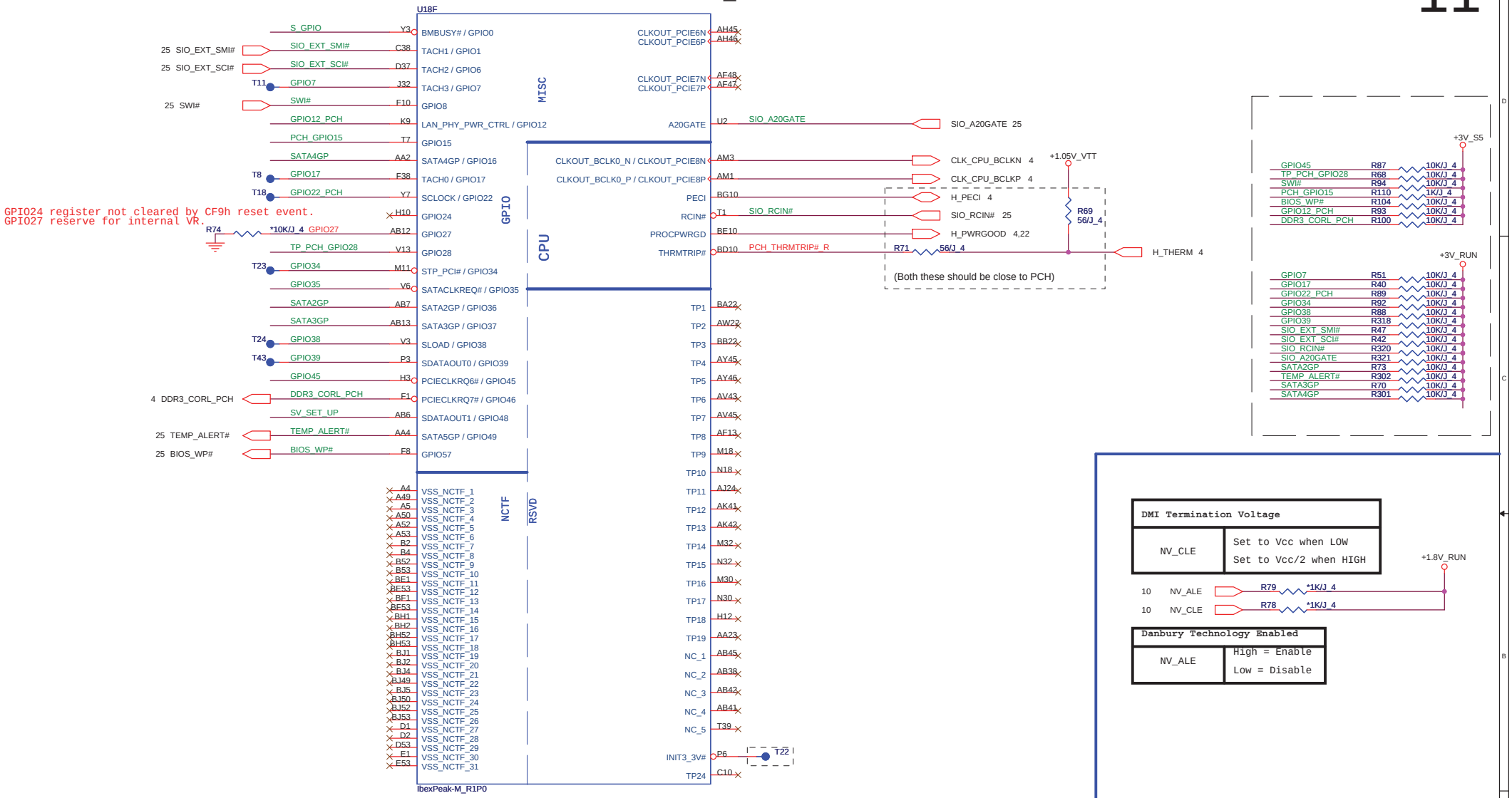
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

+1.8V_RUN

10 NV_ALE R79 *1K/J_4

10 NV_CLE R78 *1K/J_4

Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

R82 10K/J_4 GPIO35

R222 *1K/J_4 GNT3# 10

A16 swap override Strap/Top-Block Swap Override jumper	
GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

R95 *1K/J_4 SWI#

Integrated Clock Chip Enable (Reserve to validate for future platforms)	
RSV_WOL_EN (GPIO8)	Enable when sampled low Disable when sampled high

+3V_RUN

S_GPIO R299 10K/J_4

SV_SET_UP R90 10K/J_4

SV_SET_UP	1-X High = Strong (Default)

BMBUSY#:
If not used, require a weak pull-up (8.2- KΩ to 10 kΩ) to Vcc3_3.
CRB(V1.0)P28: it has 1K PU and 100 ohm on this net for validation purpose.

BMBUSY#:(Intel feedback)
Follow CRB checklist, 1K is for intel BIOS validation purpose.

Quanta Computer Inc.

PROJECT : FH1A

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	IBEX PEAK-M 4/6	1A
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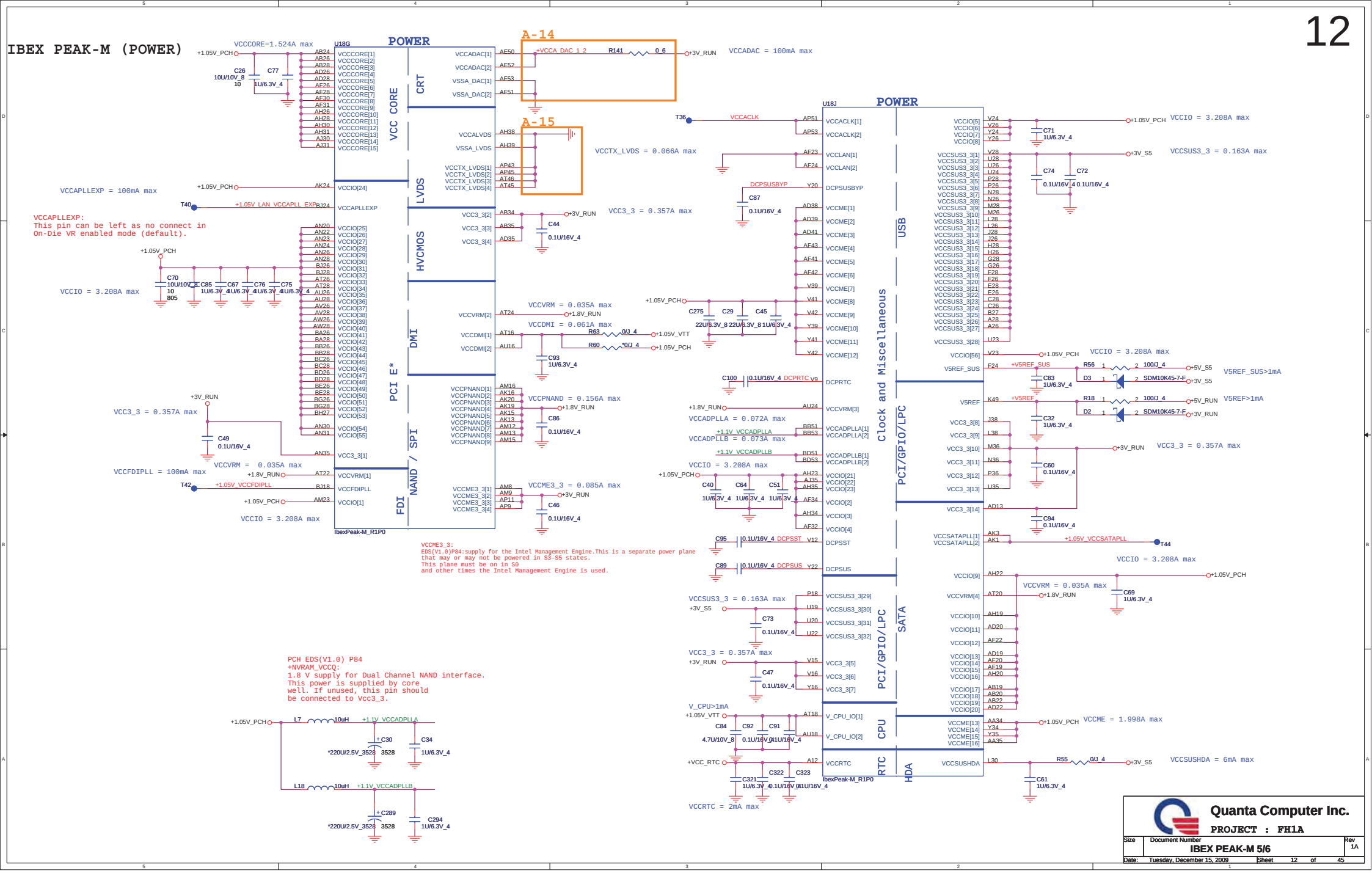
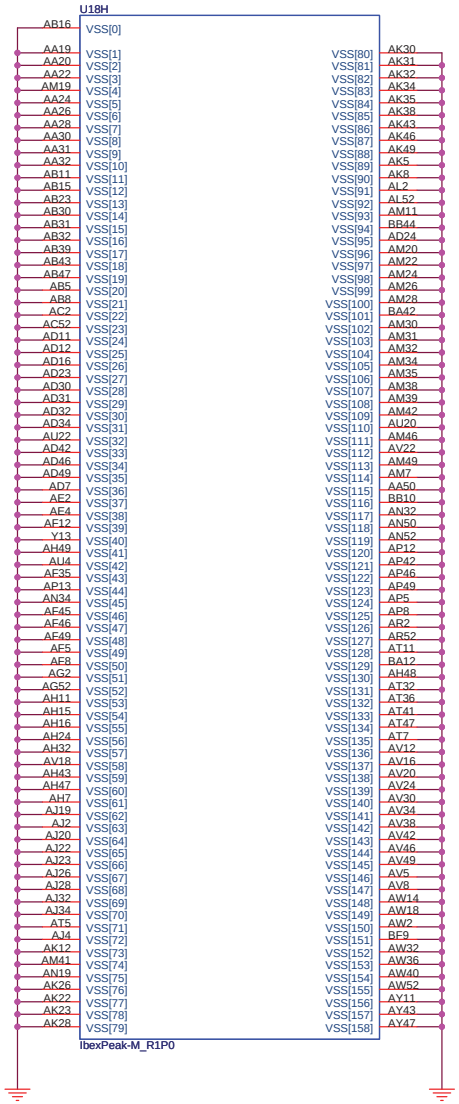
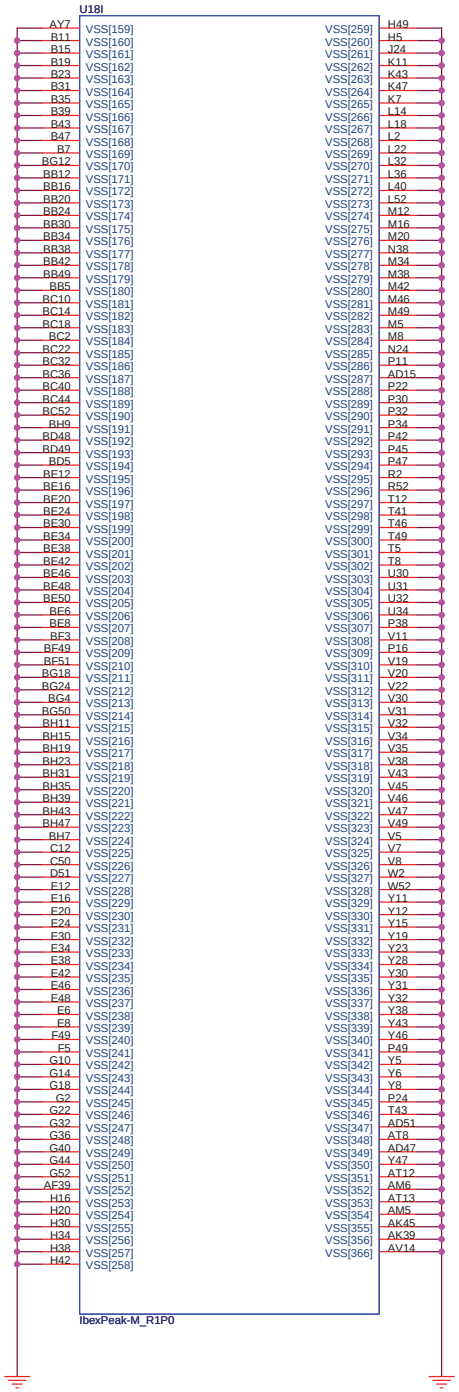
IBEX PEAK-M (POWER)



IBEX PEAK-M (GND)





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PROJECT : FH1A

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	IBEX PEAK-M 6/6	1A

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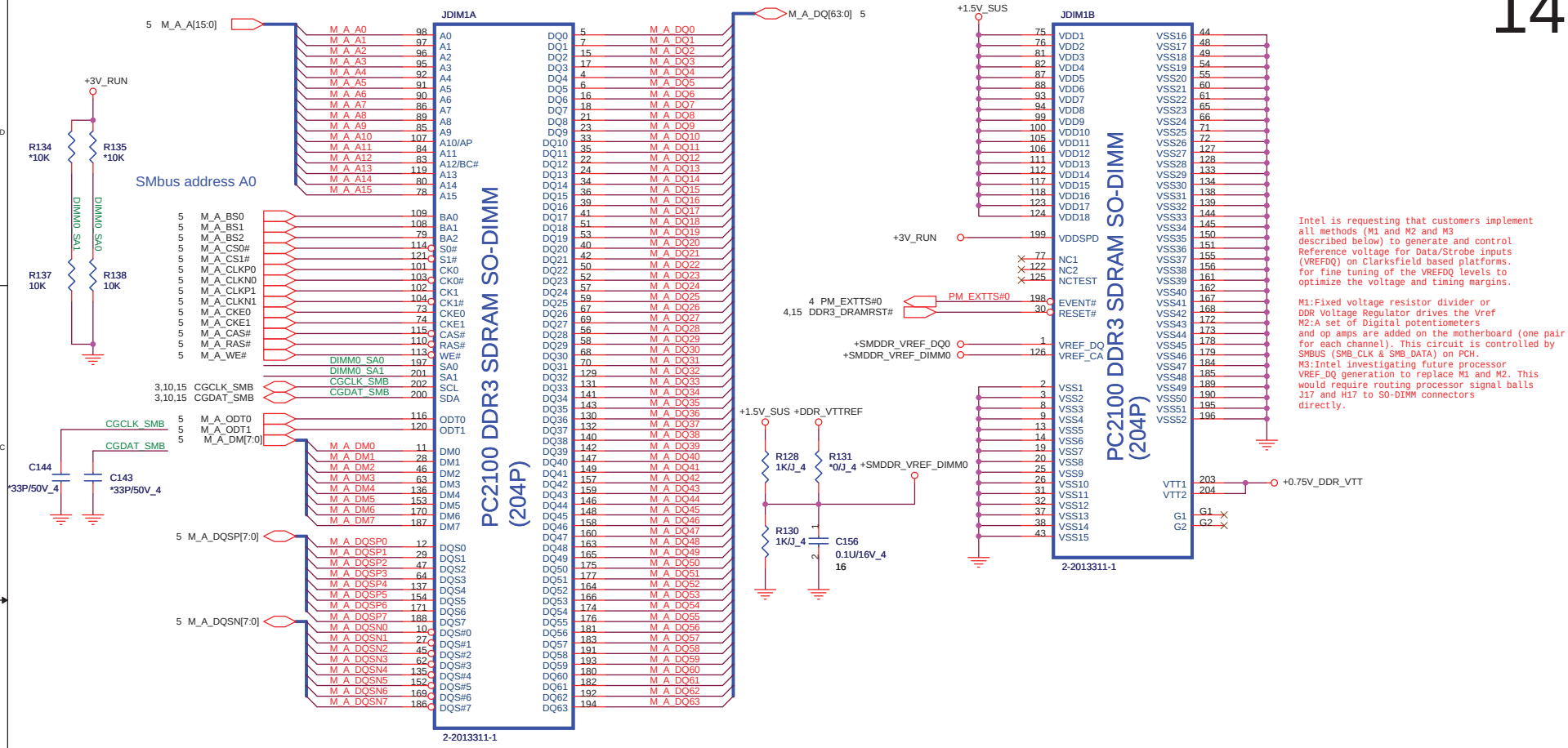
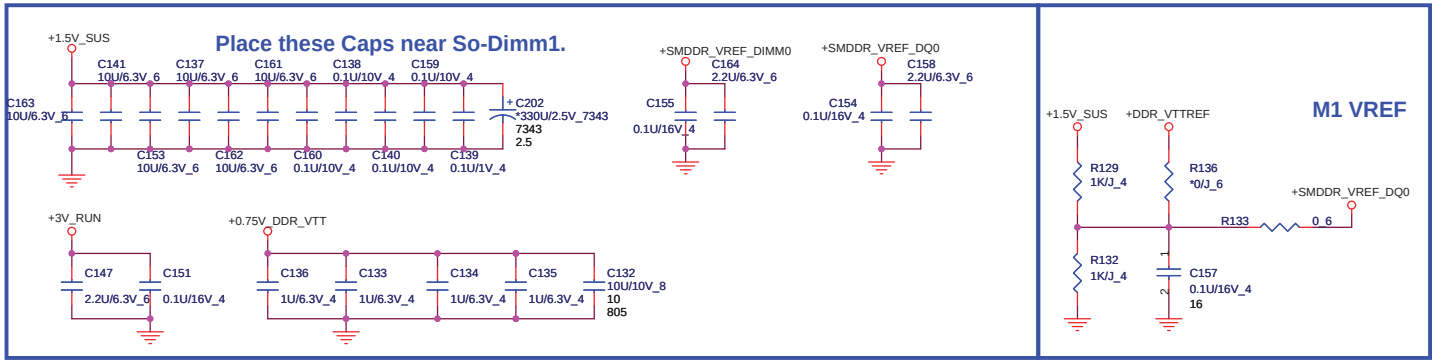


Intel is requesting that customers implement all methods (M1 and M2 and M3 described below) to generate and control Reference voltage for Data/Strobe inputs (VREFDQ) on Clarksfield based platforms. for fine tuning of the VREFDQ levels to optimize the voltage and timing margins.

M1:Fixed voltage resistor divider or DDR Voltage Regulator drives the Vref
M2:A set of Digital potentiometers and op amps are added on the motherboard (one pair for each channel). This circuit is controlled by SMBUS (SMB_CLK & SMB_DATA) on PCH.
M3:Intel investigating future processor VREF_DQ generation to replace M1 and M2. This would require routing processor signal balls J17 and H17 to SO-DIMM connectors directly.



Quanta Computer Inc.

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Size	Document Number	Rev
	DDR3 DIMM-1	1A
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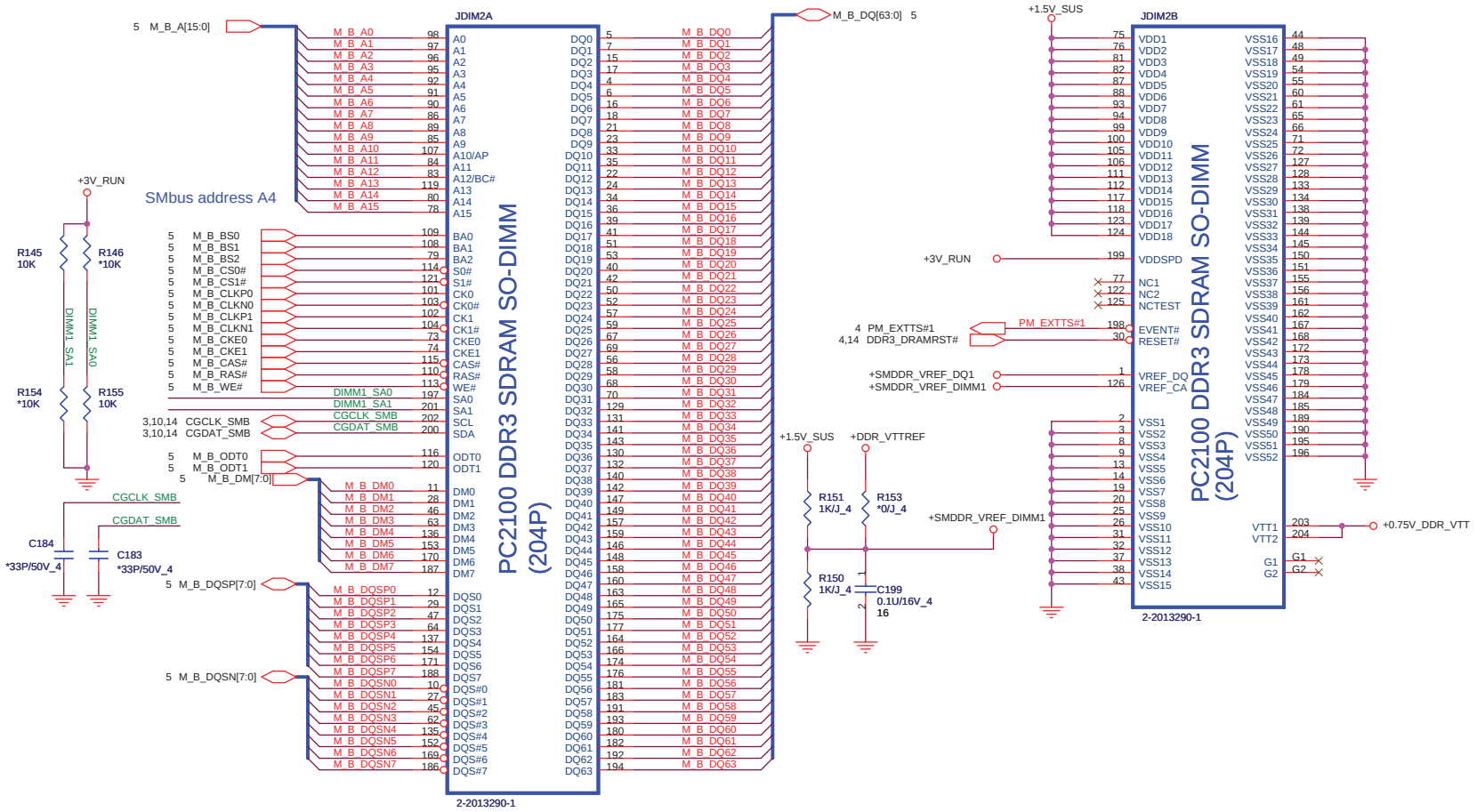

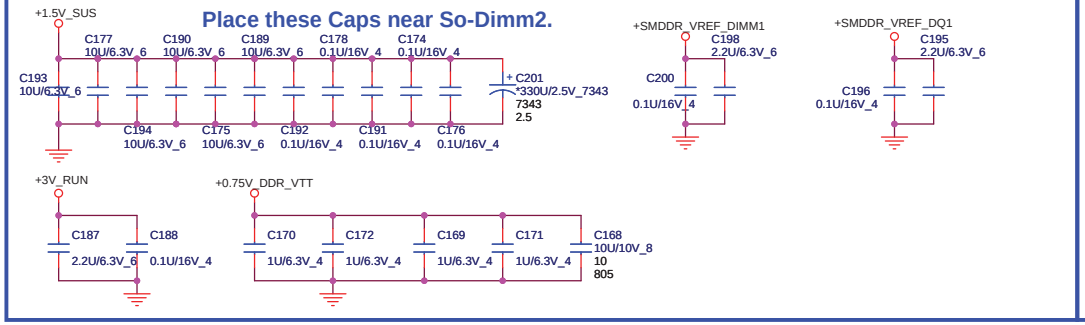

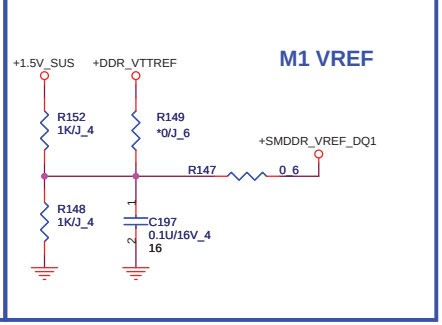

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	DDR3 DIMM-2	1A
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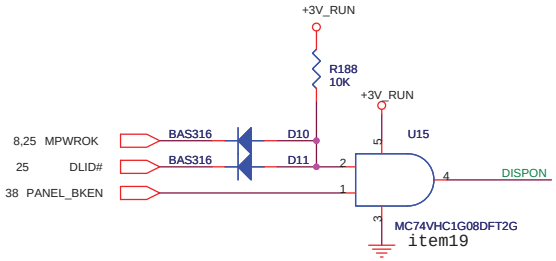
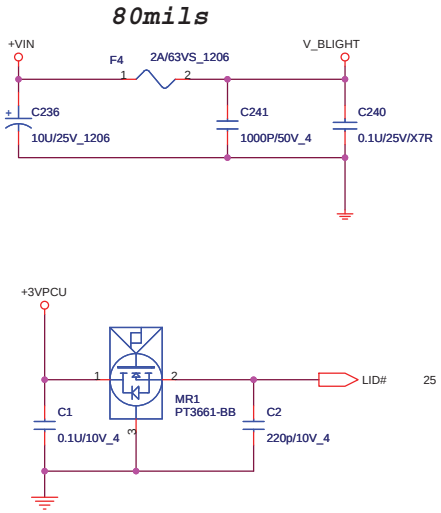
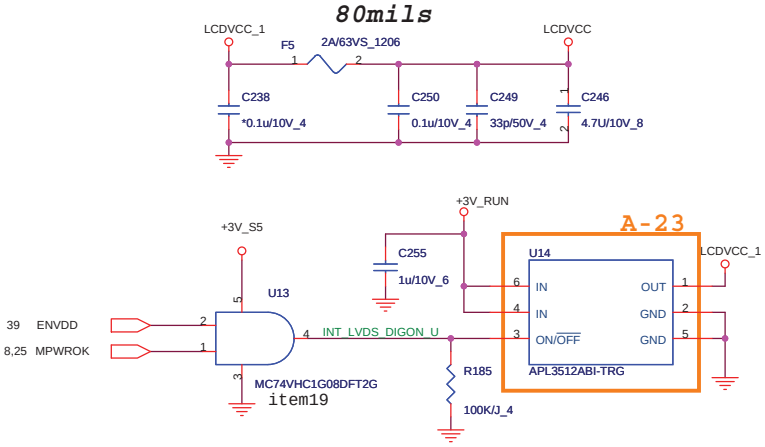
Backlight Control(LDS)

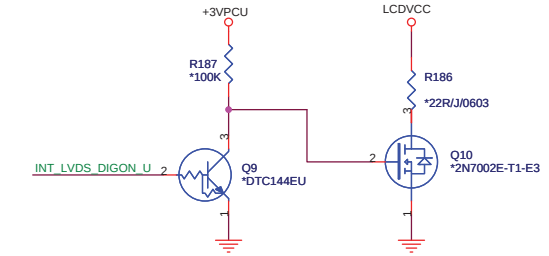


BACKLIGHT POWER

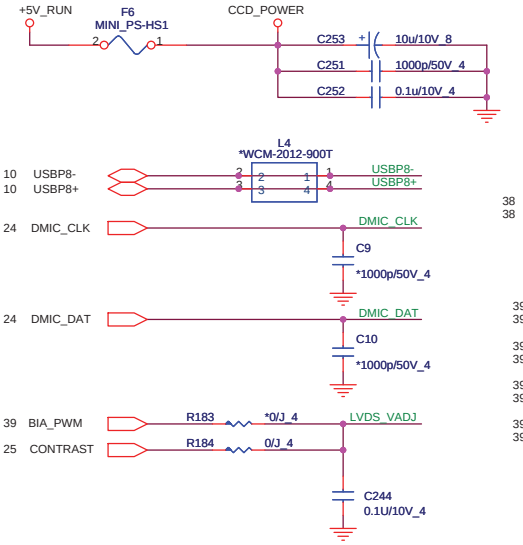


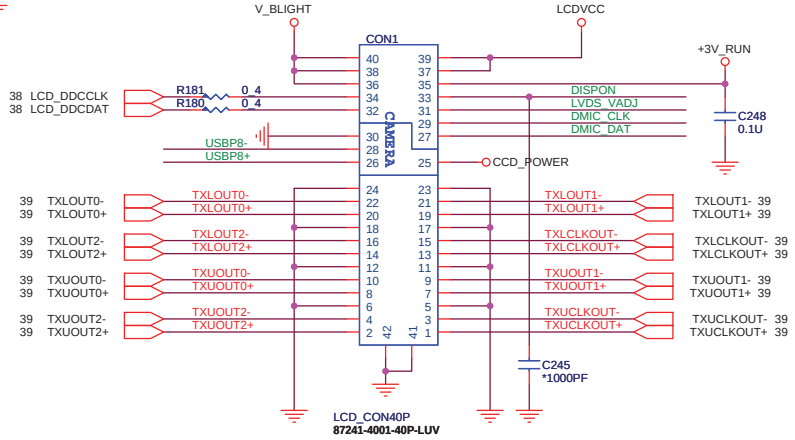
LED Panel POWER SWITCH(LVDS)





LVDS/CCD





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Size	Document Number	Rev
	LCD/LED Panel/CCD	1A
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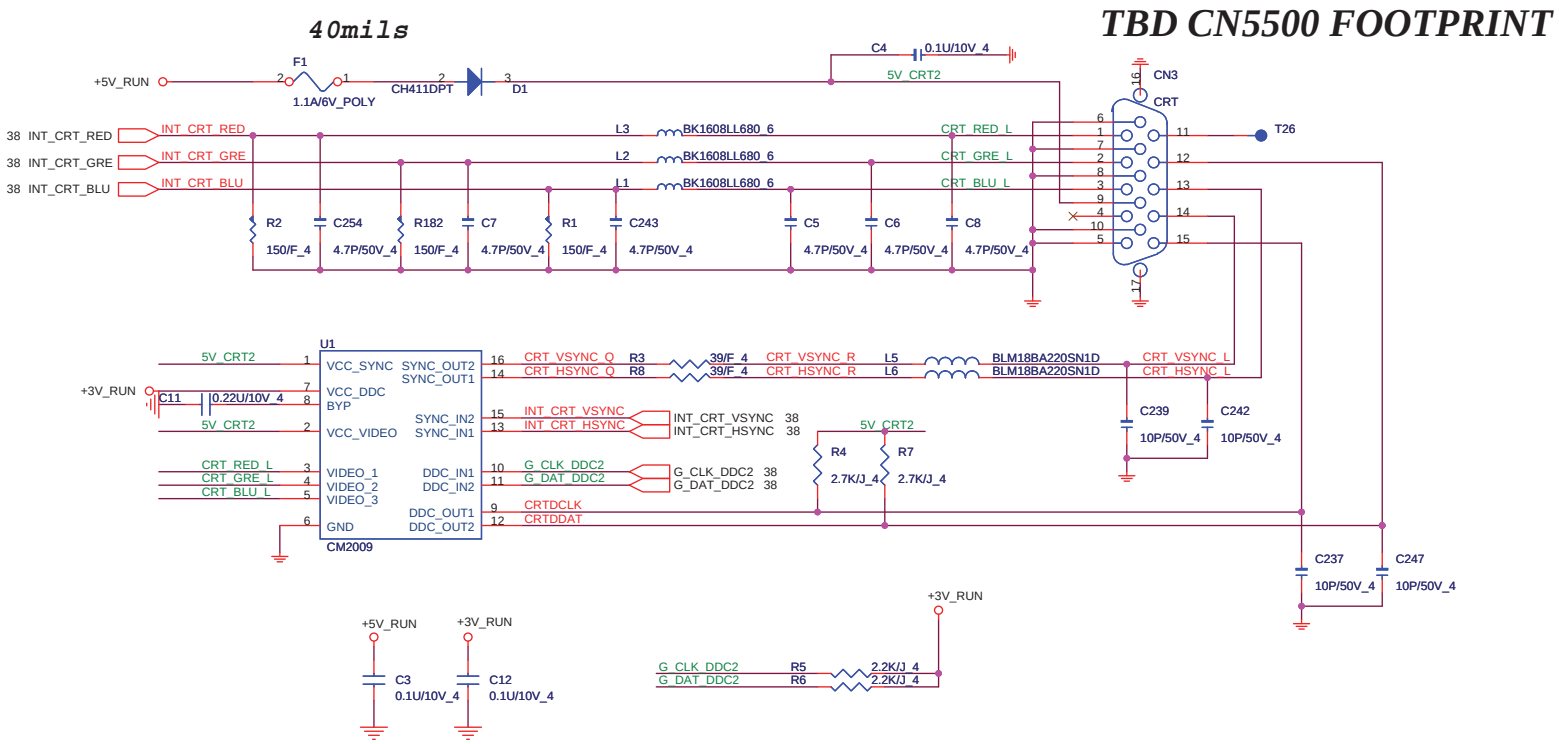
CRT CONN/DDC LEVEL SHIFT



Quanta Computer Inc.		
PROJECT : FH1A		
Size	Document Number: CRT CONN/DDC LEVEL SHIFT	Rev: 1A
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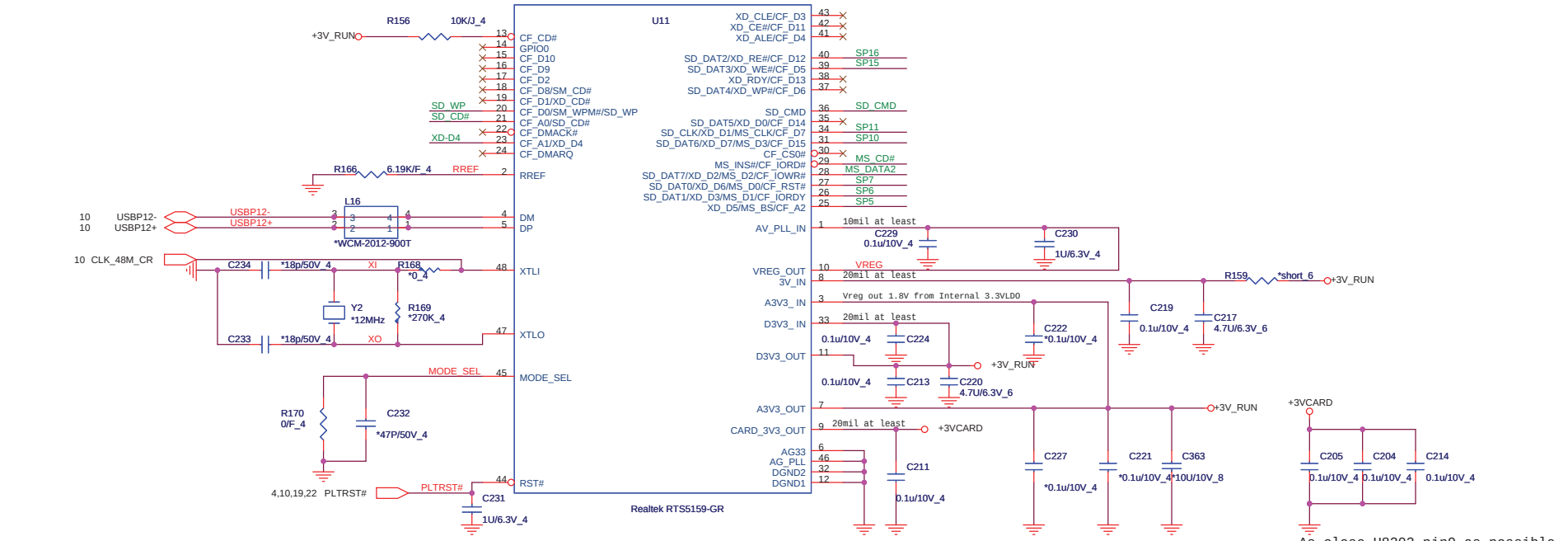
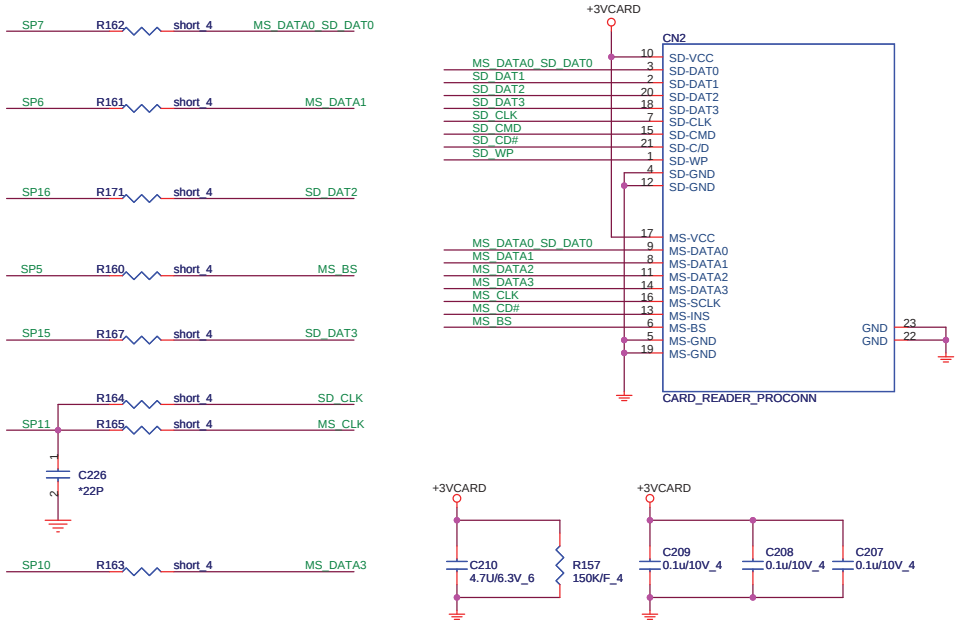
Card Reader



As close U8203 pin9 as possible

XD-D4 R158 short_4 SD_DAT1

For 5158E



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PROJECT : FH1A

Size	Document Number	Rev
	Card Reader RTS5159	1A
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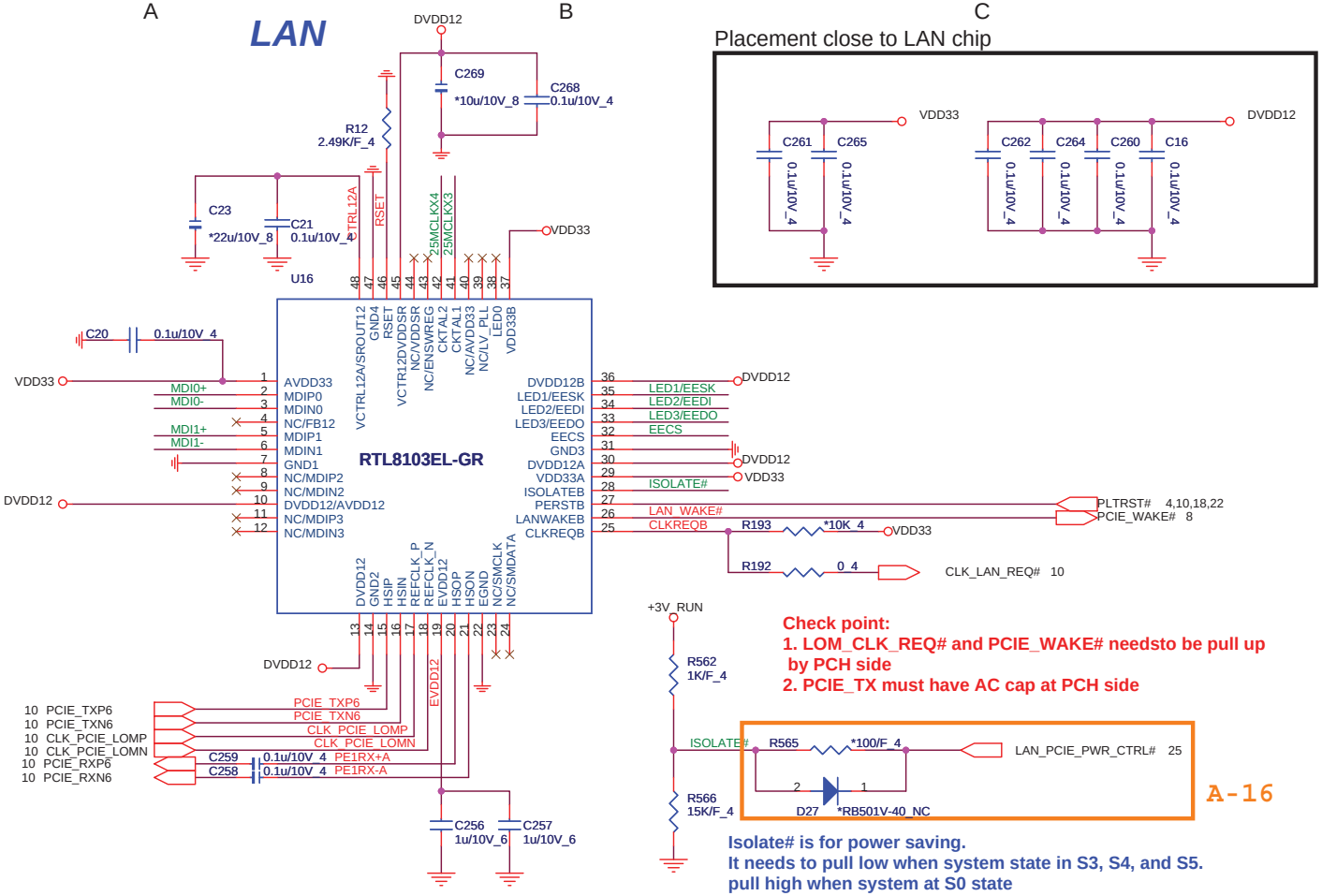
LAN



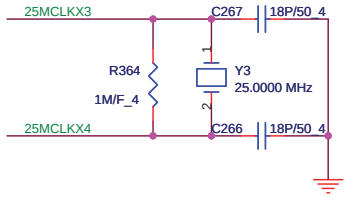
Placement close to LAN chip

Check point:
1. LOM_CLK_REQ# and PCIE_WAKE# needsto be pull up by PCH side
2. PCIE_TX must have AC cap at PCH side

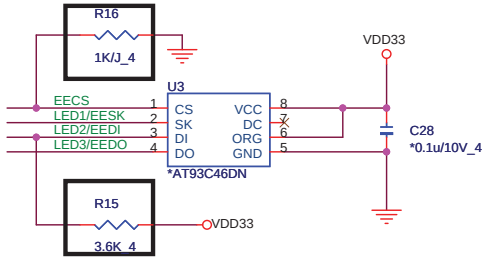
A-16

Isolate# is for power saving.
It needs to pull low when system state in S3, S4, and S5.
pull high when system at S0 state

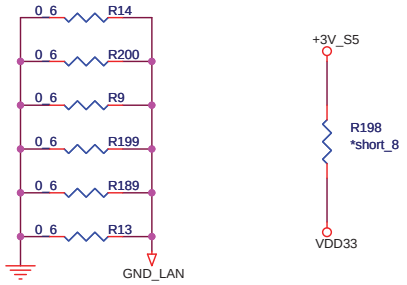
X'tal 25MHz



LAN EEPROM

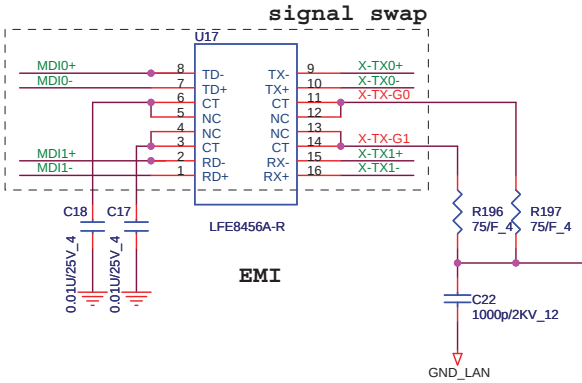


LAN Power

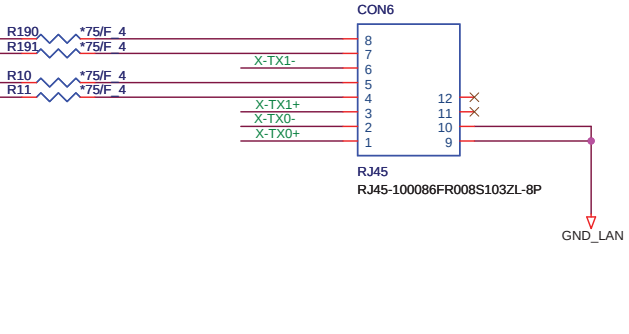


10/100 Transformer

signal swap



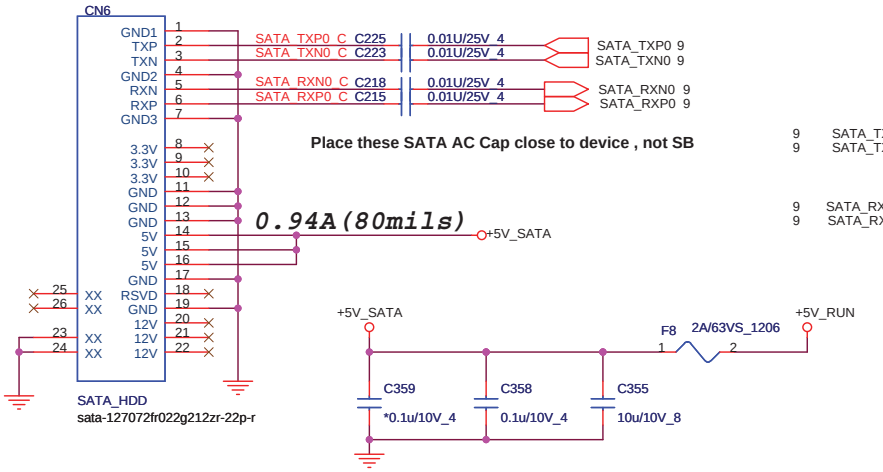
RJ45



Quanta Computer Inc.		
PROJECT : FH1A		
Size	Document Number: LAN_RTL8103EL/RJ45	Rev 1A
Date: Tuesday, December 08, 2009	Sheet 19 of 45	

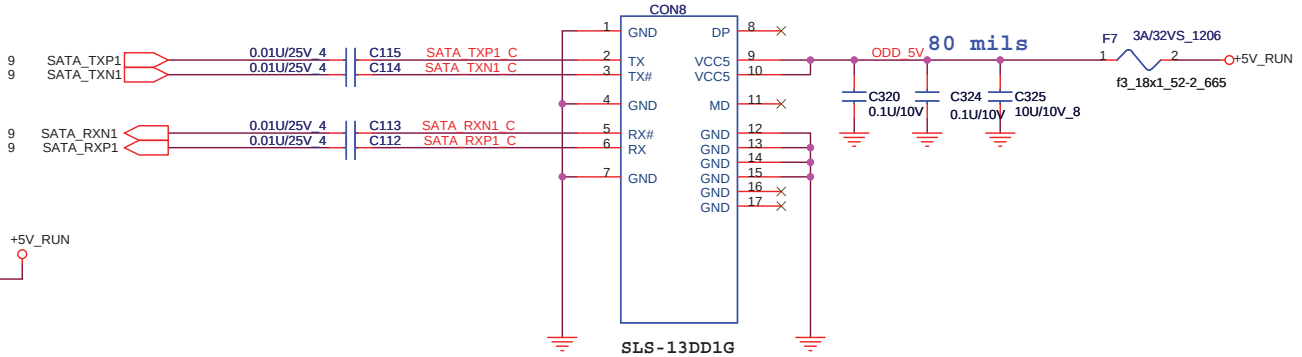
REQ by layout

2.5" SATA HDD



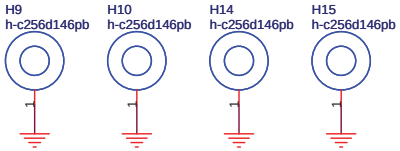
SATA ODD

ODD CONN

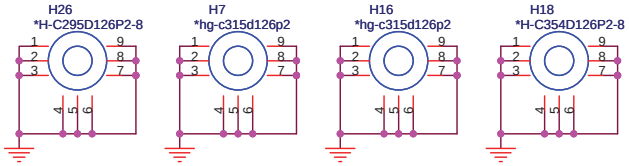


Hole

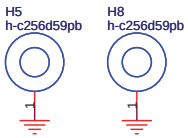
CPU Nut



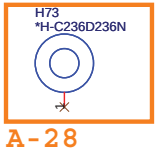
Hole for ESD

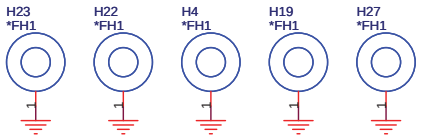


MINI CARD



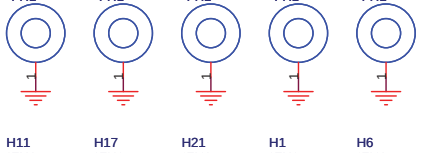
Antenna Hole

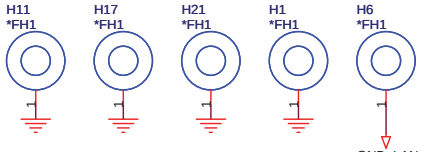




Thermal Module

VGA Nut

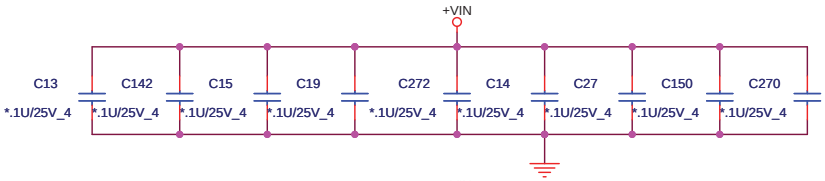


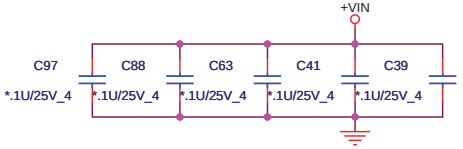


Fan Hole

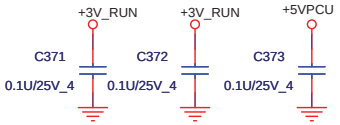
Decoupling Cap

EMI request





EMI(Decoupling Cap)



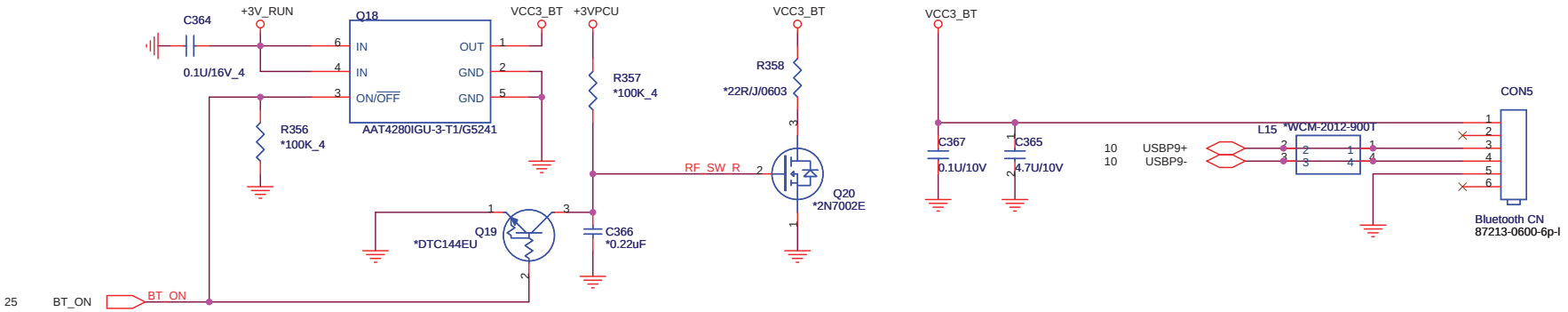
Quanta Computer Inc.

PROJECT : FH1A

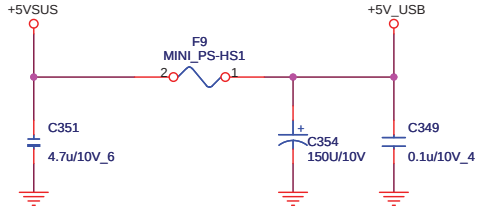
Size	Document Number	Rev
	HDD/ ODD/HOLE	1A

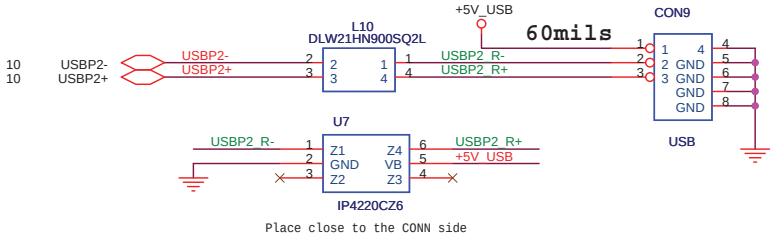
Date: Tuesday, December 15, 2009 Sheet 20 of 45

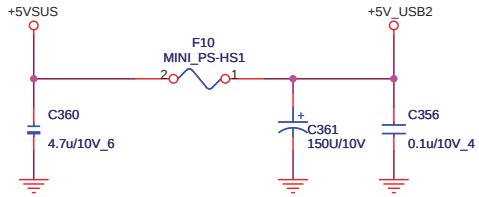
BuleTooth (BTM)

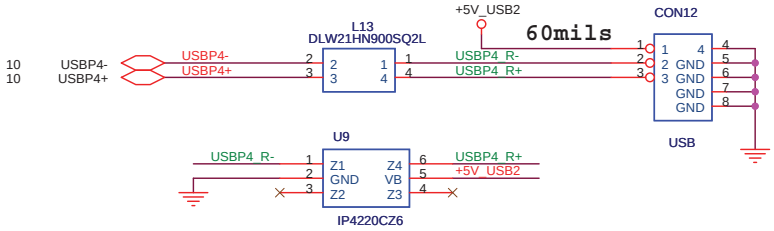


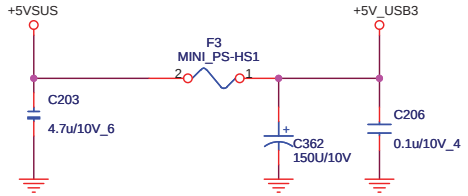
USB Connector

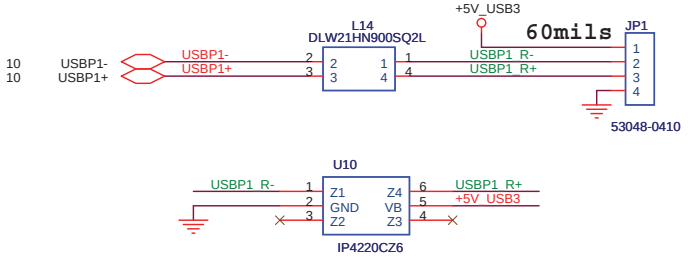










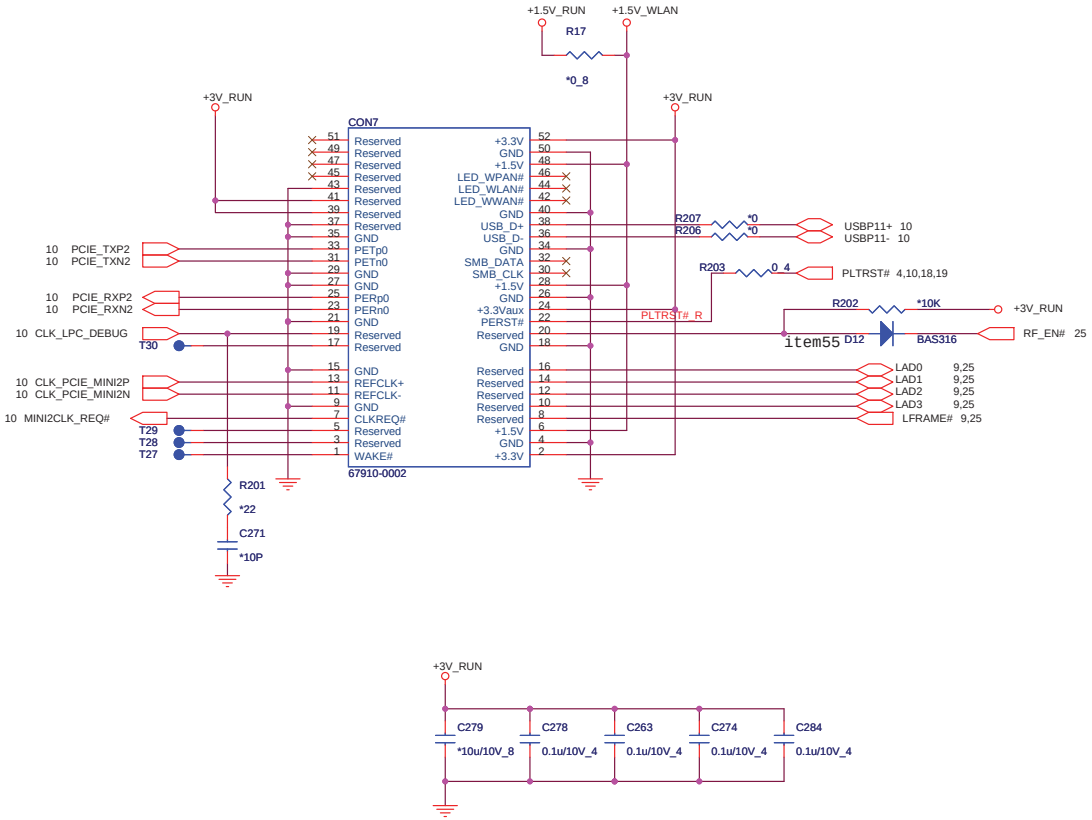


Quanta Computer Inc.

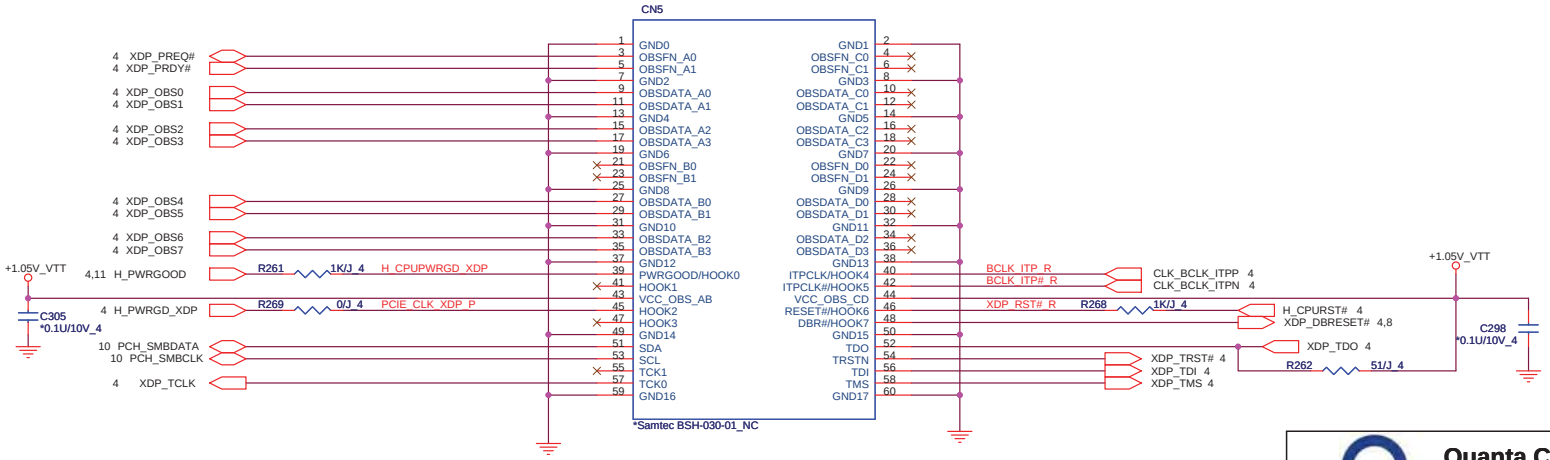
PROJECT : FH1A

Size	Document Number	Rev
	USB/BLUE TOOTH	1A
Date: Monday, December 07, 2009	Sheet 21 of 45	

MINI CARD (WLAN)



XDP



It is for debug. requesst vendeer provide 200 pcs sample.

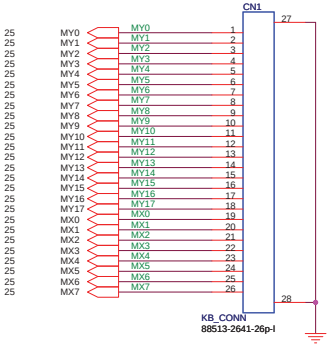
Quanta Computer Inc.

PROJECT : FH1A

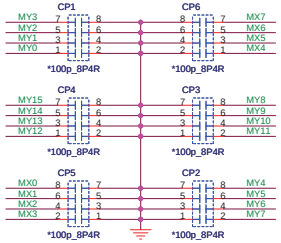
Size	Document Number	Rev
	MINI CARD(WLAN)/XDP	1A

Date: Monday, December 07, 2009 Sheet 22 of 45

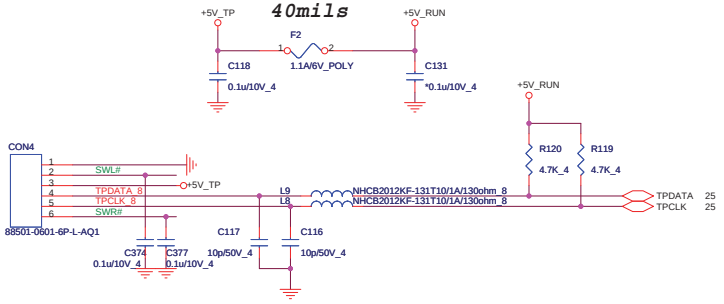
Keyboard(KBC)

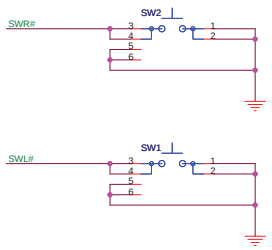


For EMI Reserve Caps for debug

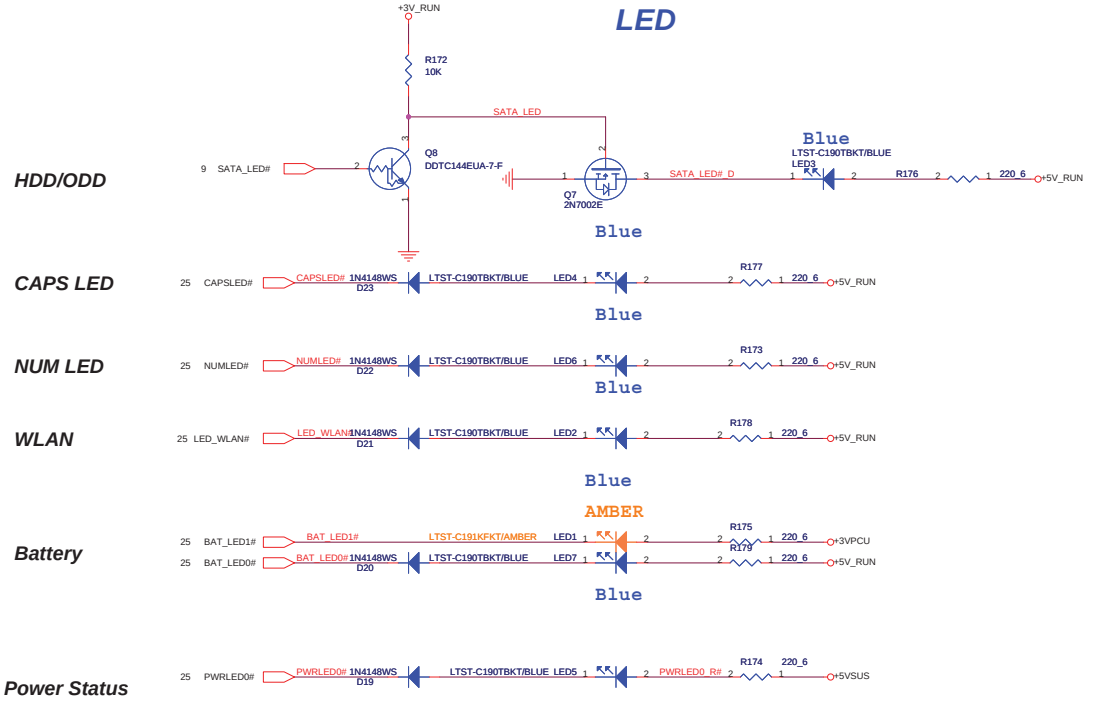


Touch Pad





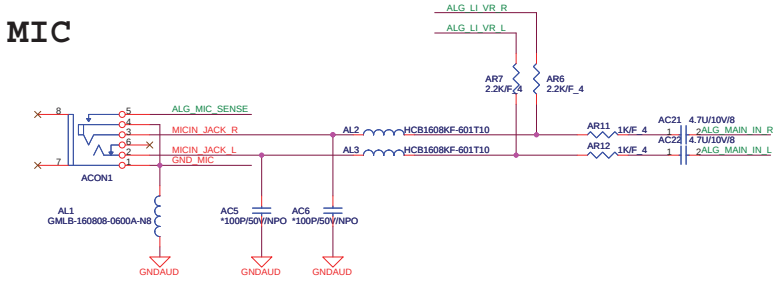
LED



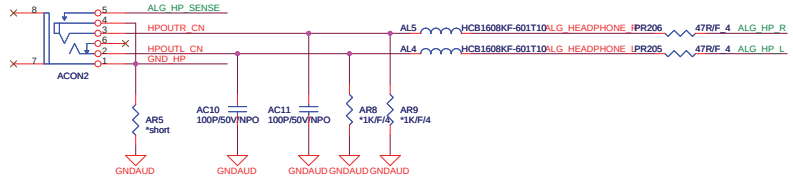
Quanta Computer Inc.	
PROJECT : FH1A	
Size	Document Number: KB/TOUCH PAD/LED — Rev: 1A
Date: Monday, December 07, 2009	Sheet 23 of 45

Codec ALC269 A-18

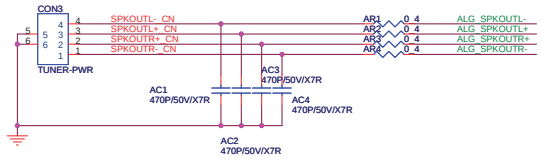
MIC



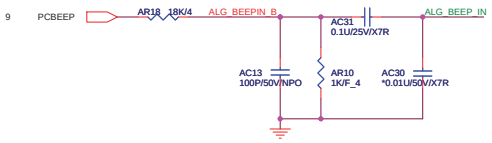
HP



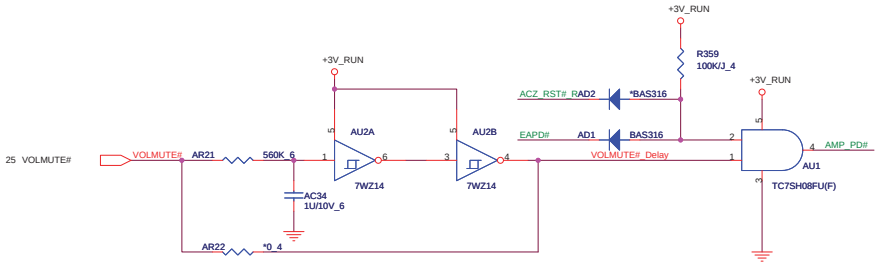
SPKR



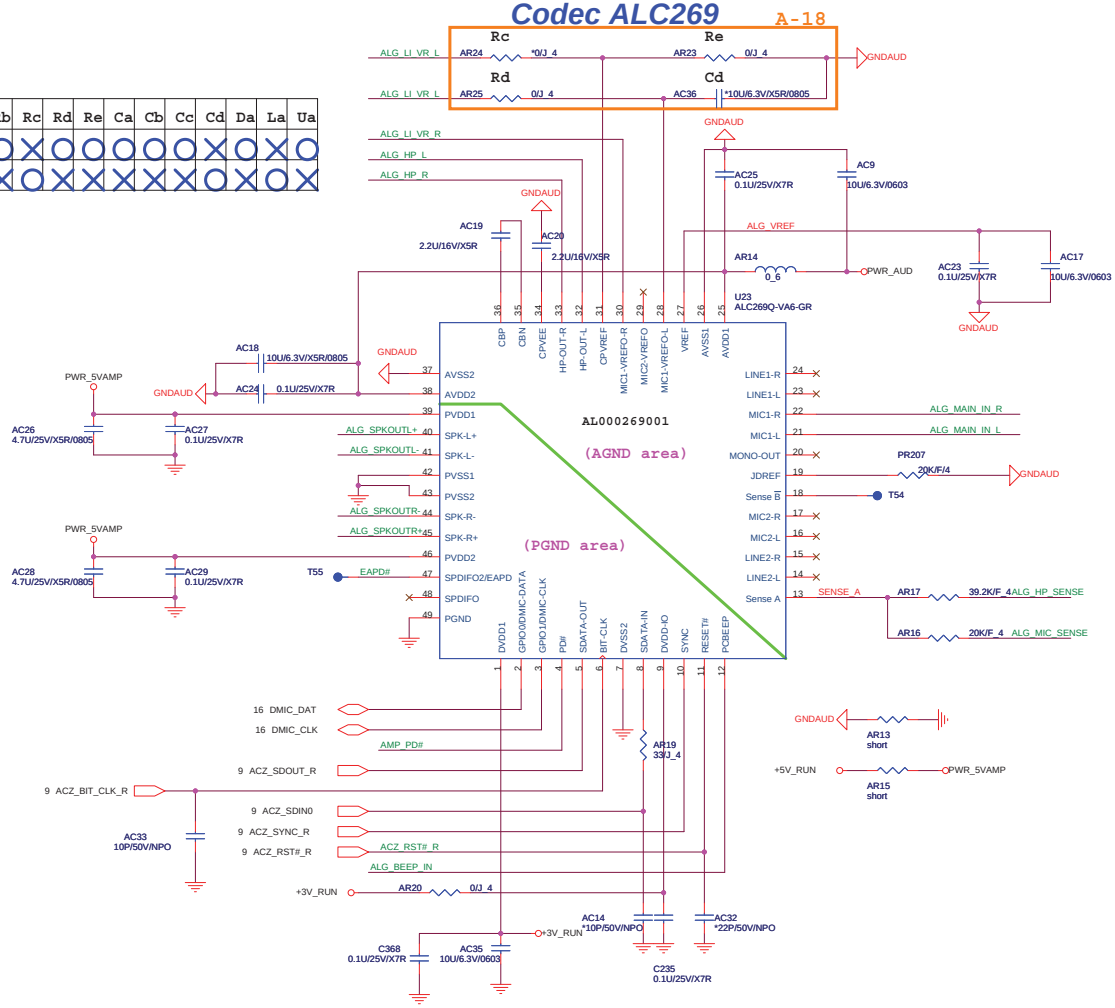
BEEP

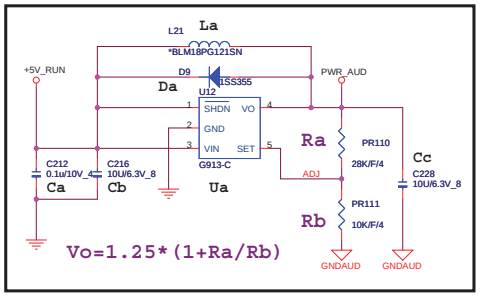


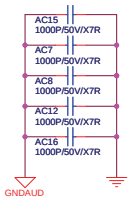
VOLMUTE



U23	Ra	Rb	Rc	Rd	Re	Ca	Cb	Cc	Cd	Da	La	Ua
ALC269Q-VA	O	O	X	O	O	O	O	O	X	O	X	O
ALC269Q-VB	X	X	O	X	X	X	X	X	O	X	O	X







Quanta Computer Inc.

PROJECT : FH1A

Size	Document Number	Rev
	CODEC (ALC269)	1A

Date: Monday, December 07, 2009 Sheet 24 of 45

EC(KBC)

IT8502

Layout Note:
Place all capacitors close to IT8502.

Layout Note:
net "3VPCU" and "RTC_VCC" minimum trace width 12mils.

Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.

Layout Note:
32.768kHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.

For Charger, Battery

For VGA Thermal Sensor, PCH

BIOS Write Protect

2MB

Near ROOM DOOR

MB Type	MODEL_ID
FH1	Low (R365)
FH1A	High (R353)

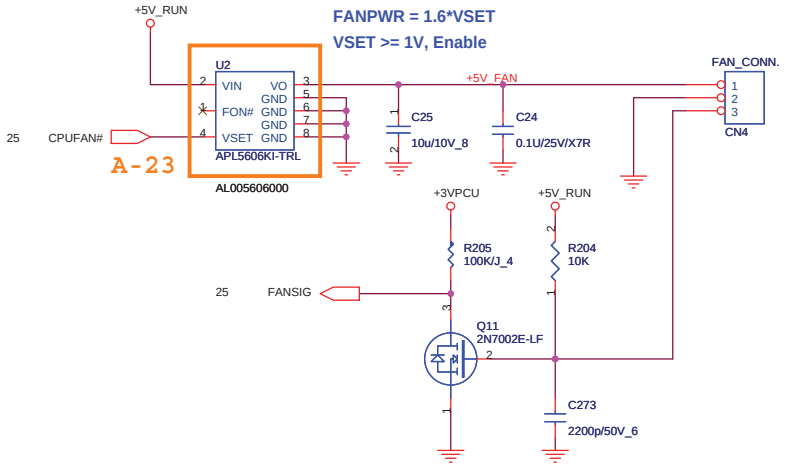
PCBA Rev.	MODEL_ID0	MODEL_ID1
C	Low	Low
D	High	Low
E	Low	High
F	High	High

Quanta Computer Inc.
PROJECT : FH1A

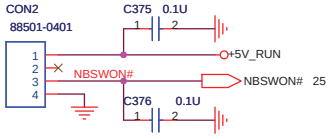
Size	Document Number	Rev
	EC_ITE8502	1A

Date: Tuesday, December 15, 2009 Sheet 25 of 45

CPU FAN CTRL



SW BOARD CON



Quanta Computer Inc.

PROJECT : FH1A

Size	Document Number	Rev
	FAN/SW CON	1A
Date: Tuesday, December 15, 2009	Sheet 26 of 45	

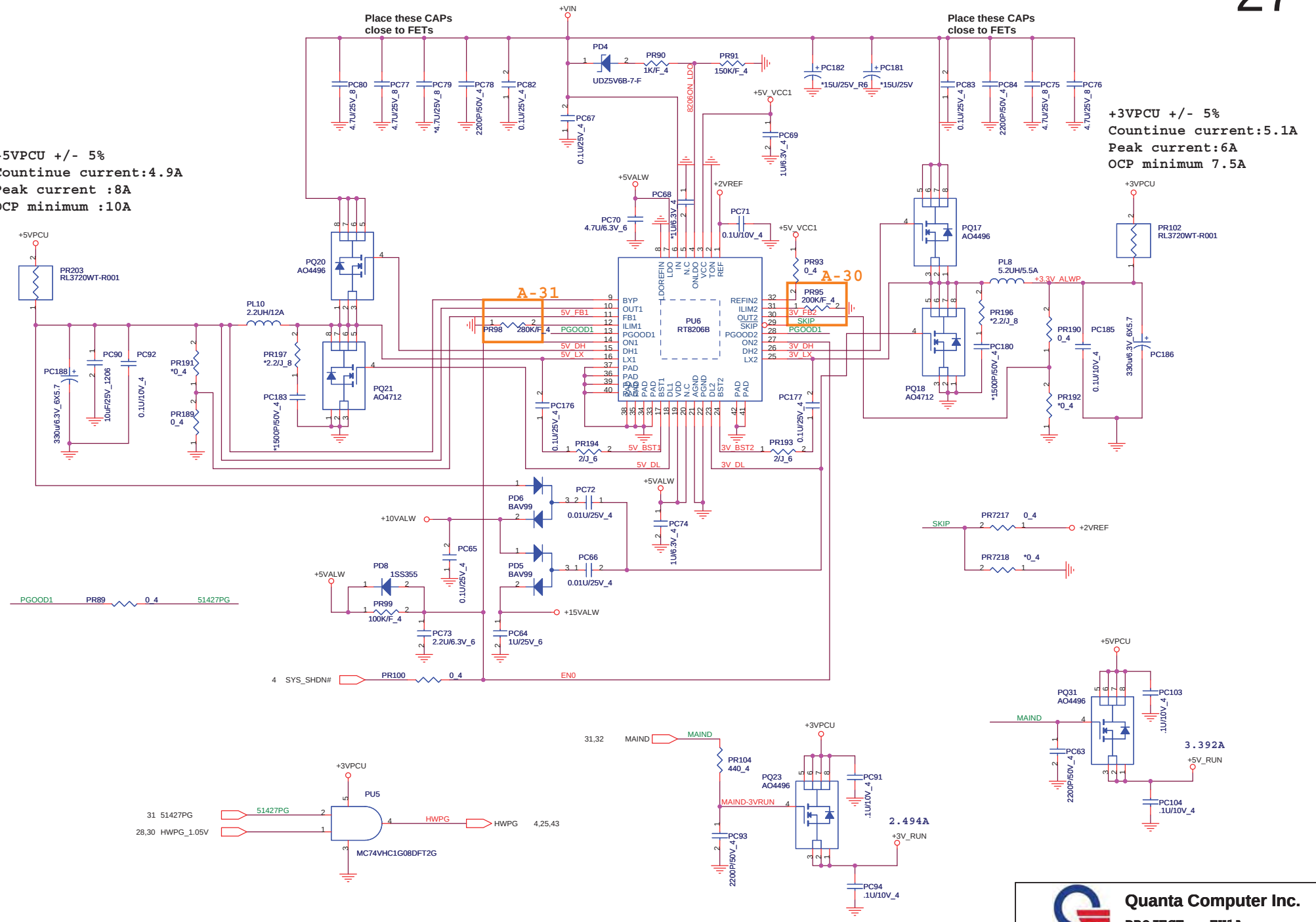
DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

+5VPCU +/- 5%
Countinue current:4.9A
Peak current :8A
OCP minimum :10A

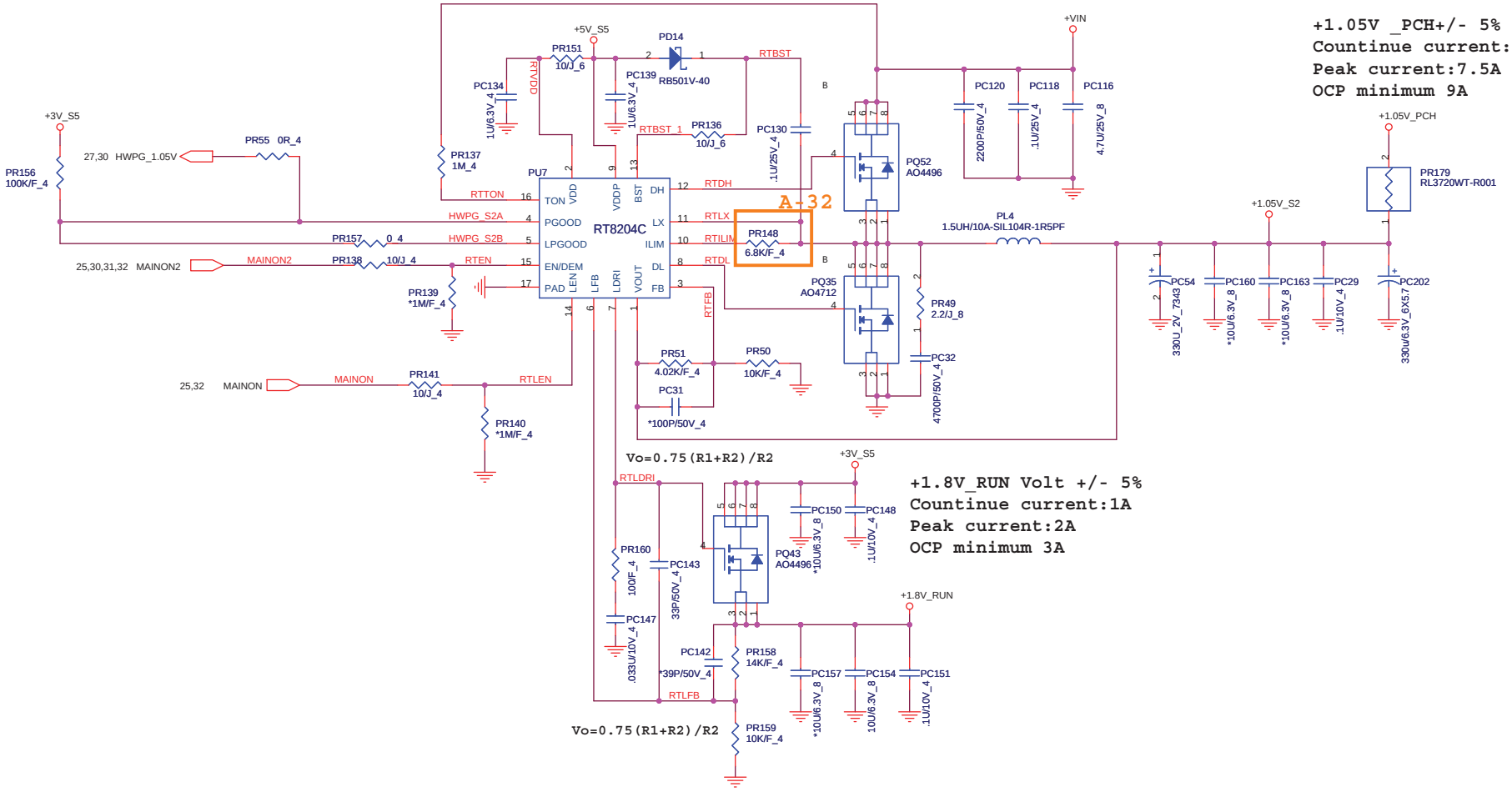
+3VPCU +/- 5%
Countinue current:5.1A
Peak current:6A
OCP minimum 7.5A

Place these CAPs close to FETs

Place these CAPs close to FETs



Quanta Computer Inc.		
PROJECT : FH1A		
Size	Document Number: +5V/+3V (RT8206B)	Rev: 1A
Date: Friday, December 11, 2009	Sheet 27 of 45	

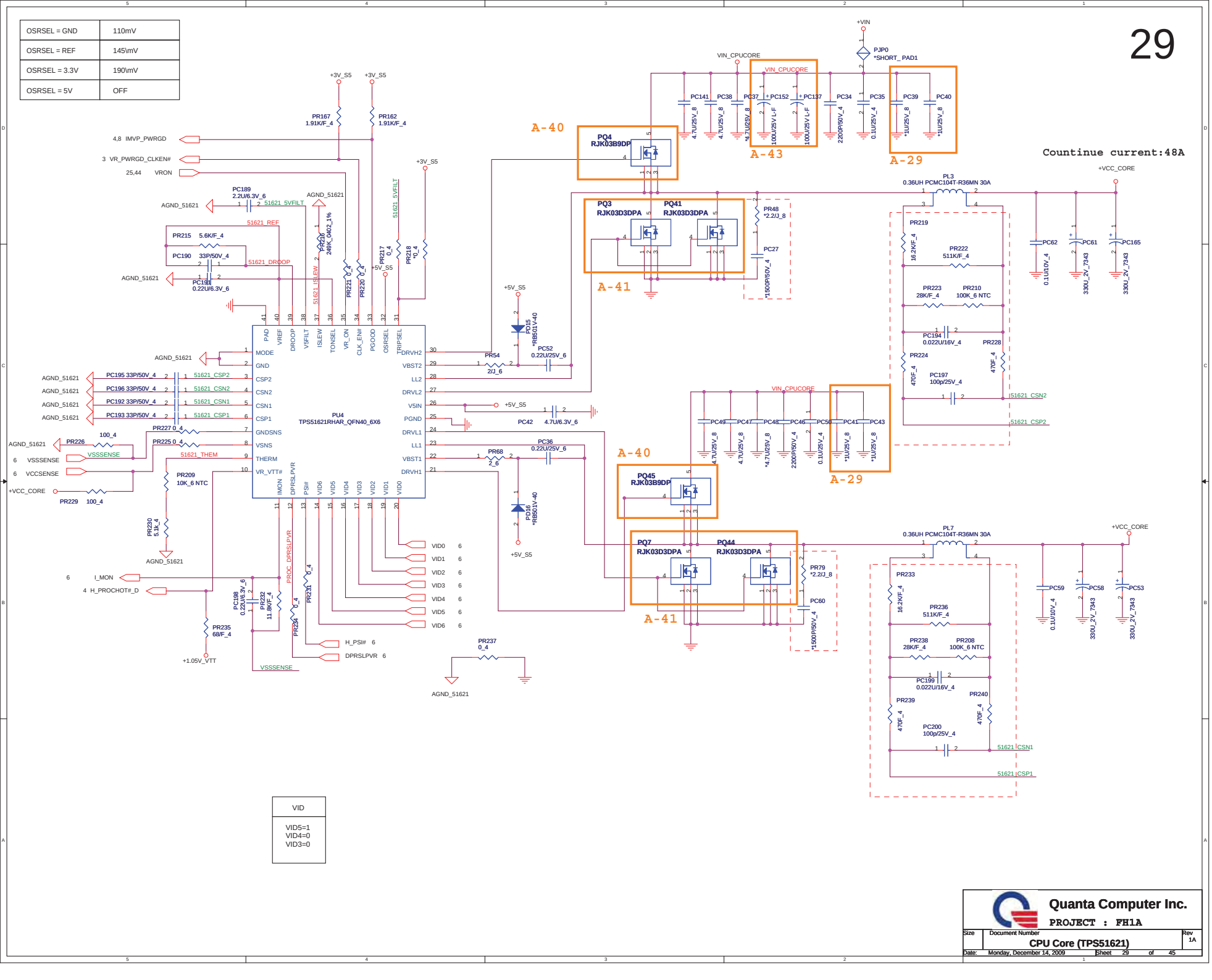


Quanta Computer Inc.

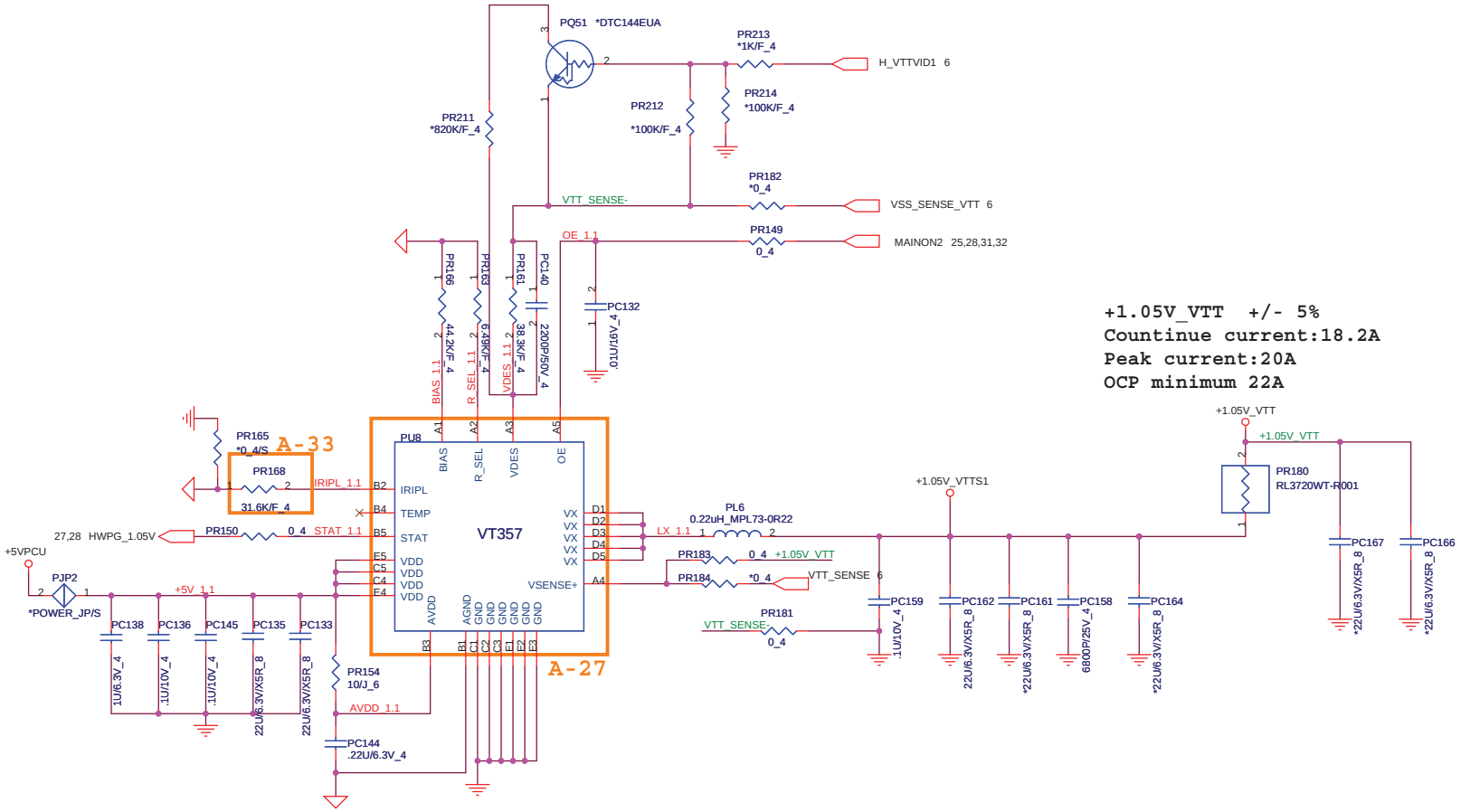
PROJECT : FH1A

Size	Document Number	Rev
	+1.05V/+1.8V (RT8204C)	1A
Date: Friday, December 11, 2009	Sheet 28 of 45	

OSRSEL = GND	110mV
OSRSEL = REF	145\mV
OSRSEL = 3.3V	190\mV
OSRSEL = 5V	OFF



Quanta Computer Inc.	
PROJECT : FH1A	
Size	Document Number: CPU Core (TPS51621) — Rev 1A
Date: Monday, December 14, 2009	Sheet 29 of 45



+1.05V_VTT +/- 5%
Countinue current:18.2A
Peak current:20A
OCP minimum 22A

Quanta Computer Inc.		
PROJECT : FH1A		
Size	Document Number: +1.05V_VTT (VT358)	Rev: 1A
Date: Friday, December 11, 2009	Sheet 30 of 45	

+1.5V_SUS +/- 5%
Countinue current:4A
Peak current:8A
OCP minimum 12A

(VTT/1A)
(20mA)

PU9 RT8207GQW
PD9 *RB501V-40
PD7 *1SS355
PQ42 AO4496
PQ50 AO4712
PQ22 AOL1448
PL9 CV-10L0MZ01/DC-10F0M102

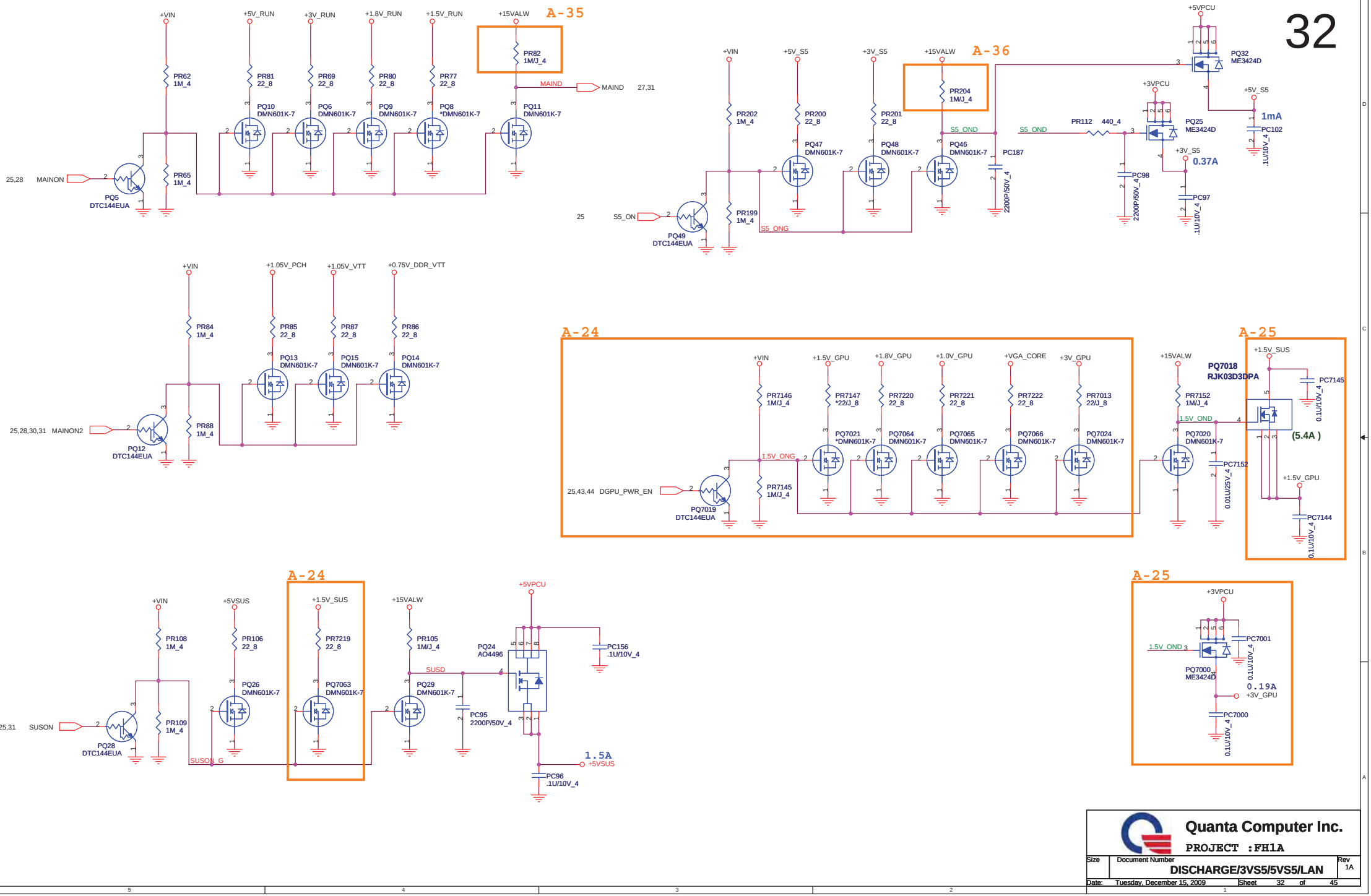
A-34
B
3A

DIS_MODE
Tracking discharge : VDDQ
Non tracking discharge : GND
No discharge : VCC5

Quanta Computer Inc.
PROJECT : FH1A

Size	Document Number	Rev
	DDR3 (RT8207)	1A

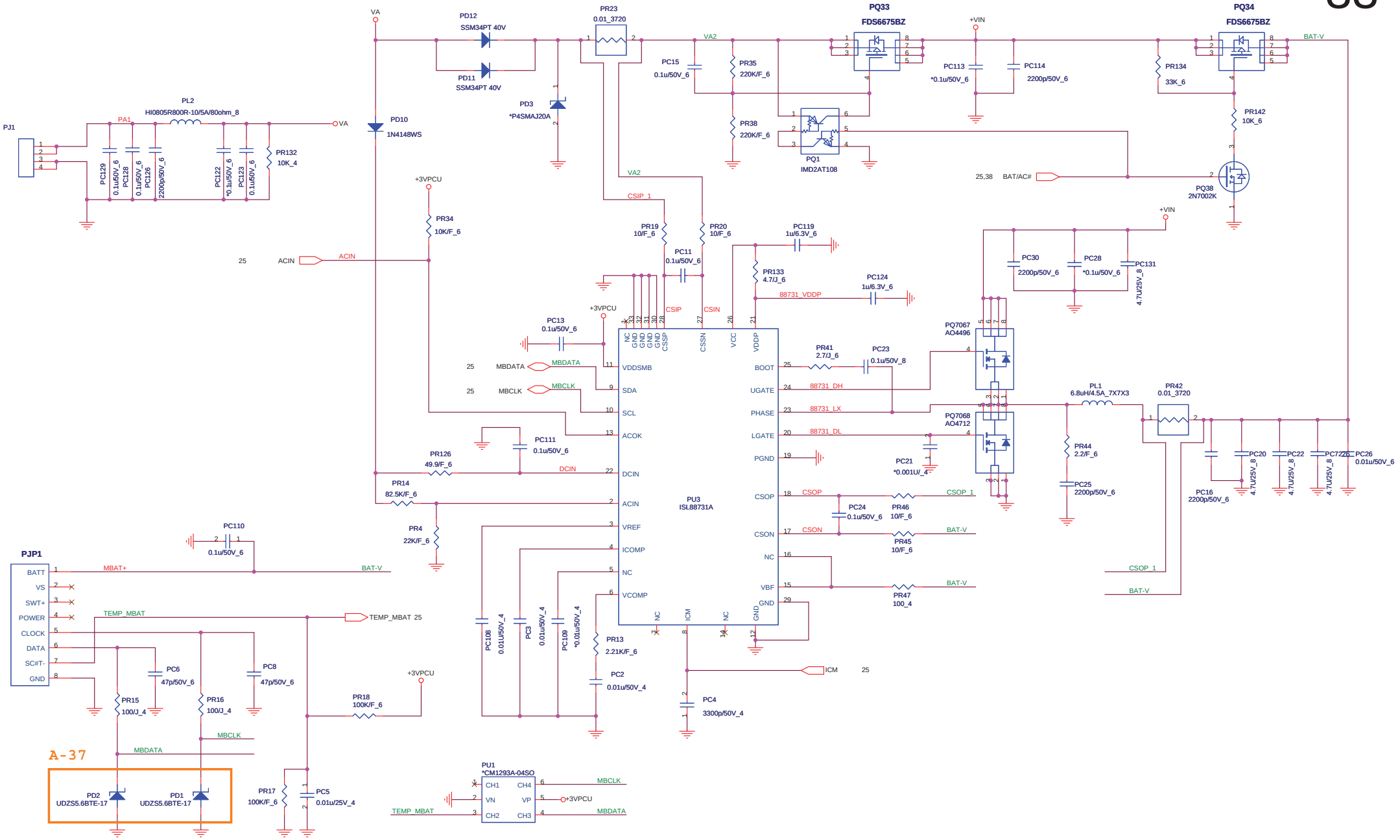
Date: Friday, December 11, 2009 Sheet 31 of 45



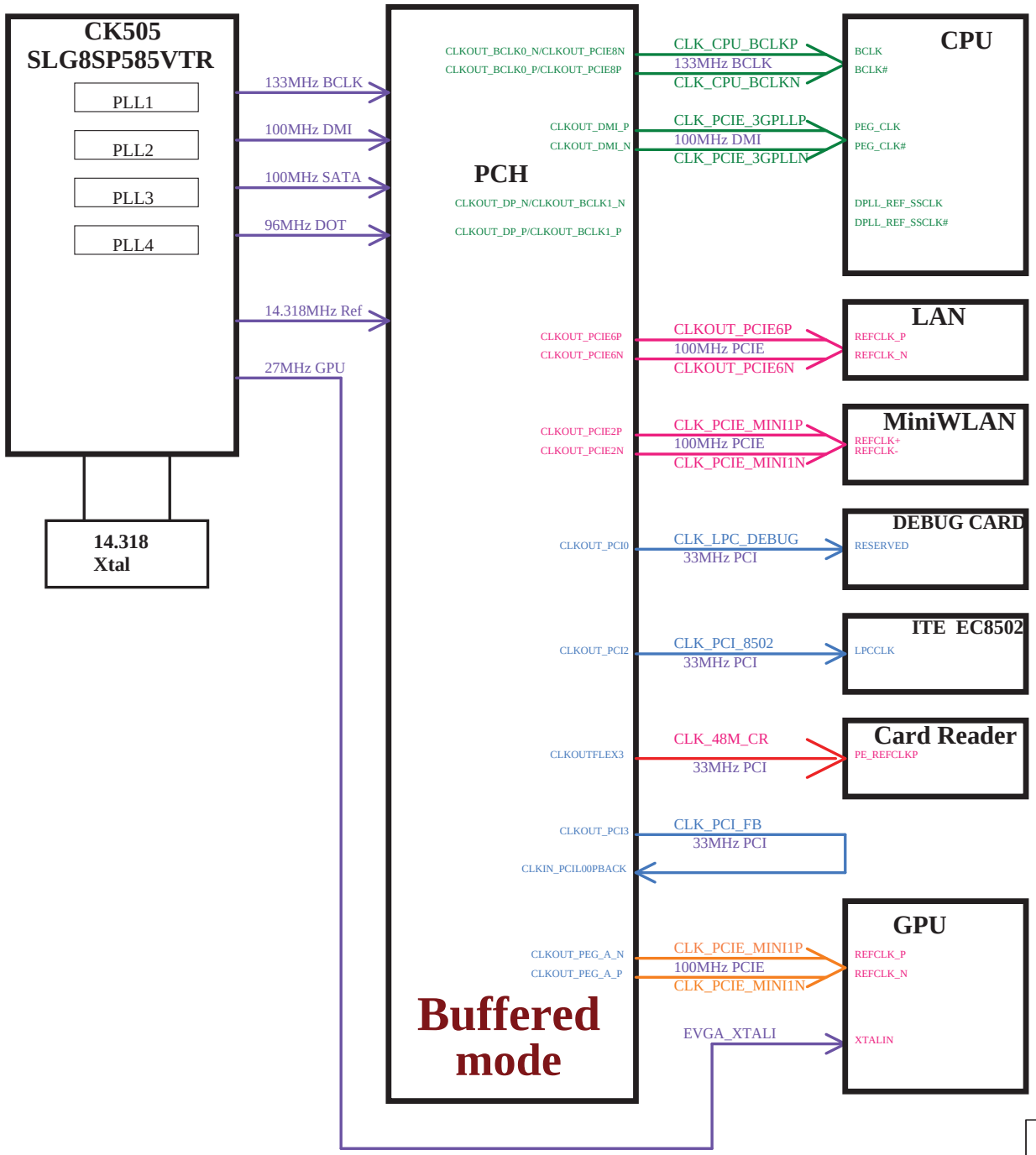
Quanta Computer Inc.

PROJECT :FH1A

Size	Document Number	Rev
	DISCHARGE/3VS5/5VS5/LAN	1A
Date: Tuesday, December 15, 2009	Sheet 32 of 45	



Quanta Computer Inc.		
PROJECT : FH1A		
Size	Document Number: CHARGER (ISL88731)	Rev: 1A
Date: Friday, December 11, 2009	Sheet 33 of 45	

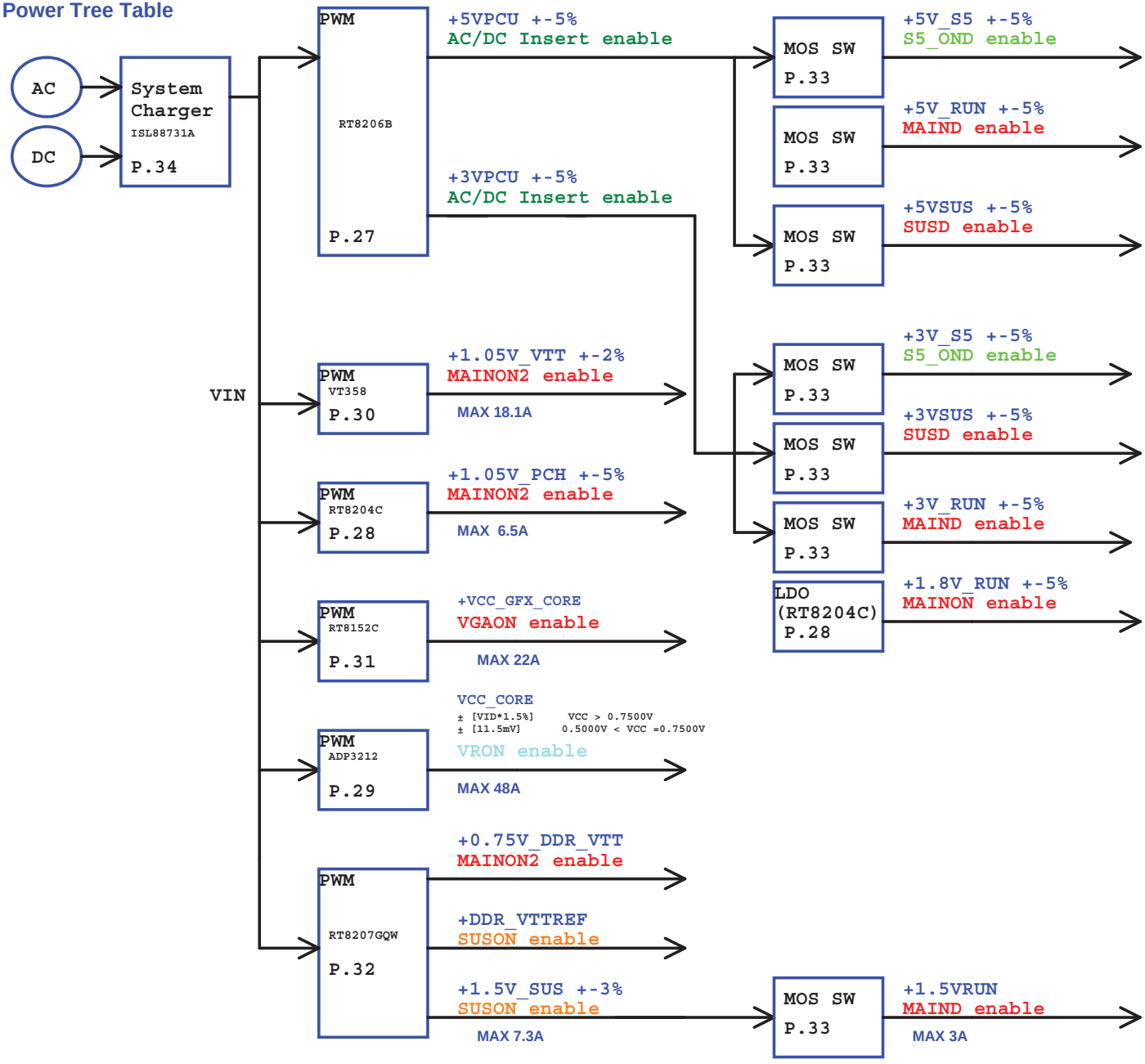


Quanta Computer Inc.
PROJECT : FH1A

Size	Document Number	Rev
	Clock Distribution	1A

Date: Friday, December 04, 2009 Sheet 34 of 45

Power Tree Table



Quanta Computer Inc.

PROJECT : FH1A

Size	Document Number	Rev
	Power Tree	1A

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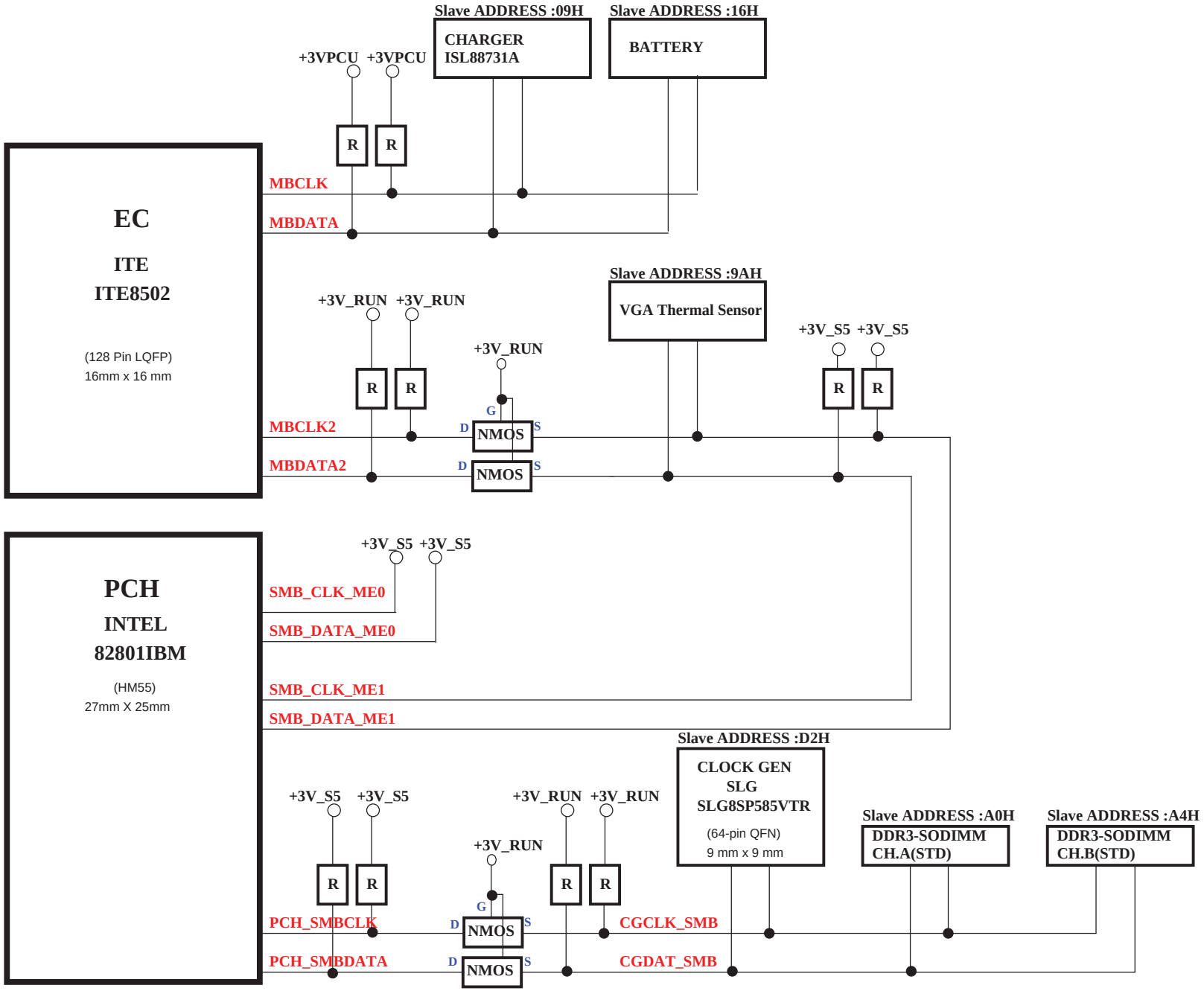

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PROJECT : FH1A

Size	Document Number	Rev
	SM BUS	1A
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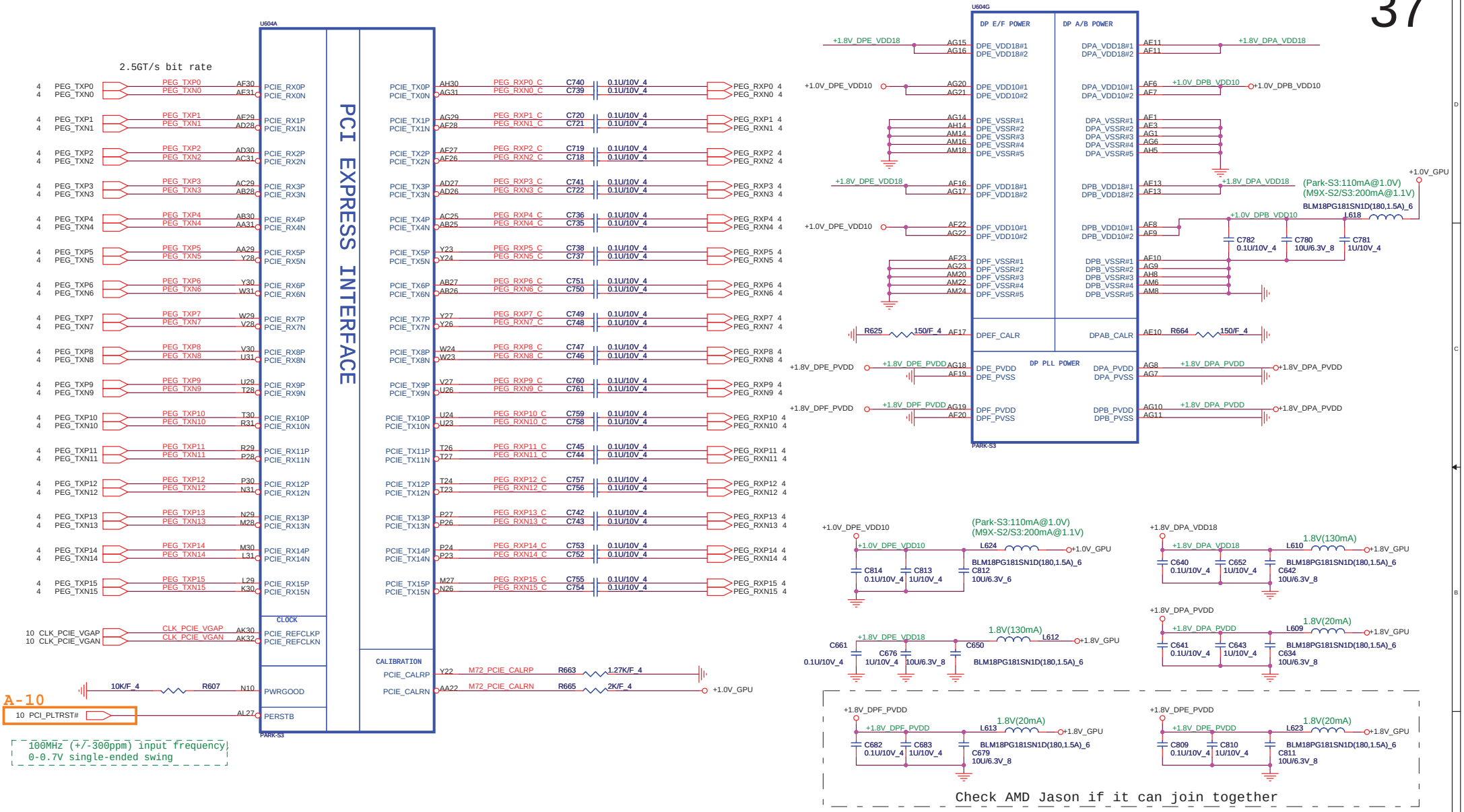

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PROJECT : FH1A

Size	Document Number	Rev
	PARK_PCIE_Interface	1A

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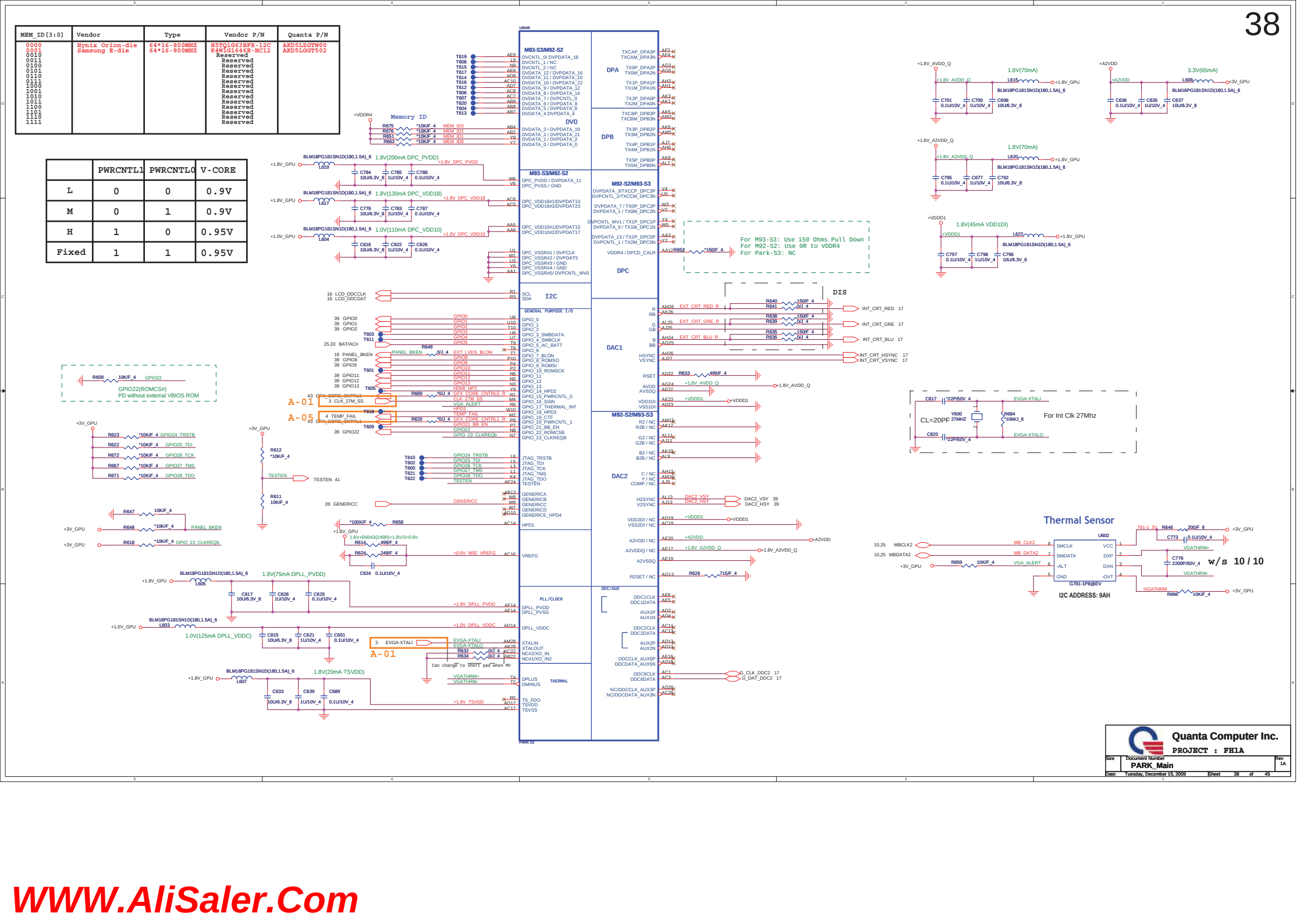
MEM_ID[3:0]	Vendor	Type	Vendor P/N	Quanta P/N
0000	Hynix Orion-die	64*16-800MHZ	H5TQ1G63BFR-12C	AKD5LZGTW00
0001	Samsung E-die	64*16-800MHZ	K4W1G1646E-HC12	AKD5LGGT502
0010			Reserved	
0011			Reserved	
0100			Reserved	
0101			Reserved	
0110			Reserved	
0111			Reserved	
1000			Reserved	
1001			Reserved	
1010			Reserved	
1011			Reserved	
1100			Reserved	
1101			Reserved	
1110			Reserved	
1111			Reserved	

	PWRCNTL1	PWRCNTL0	V-CORE
L	0	0	0.9V
M	0	1	0.9V
H	1	0	0.95V
Fixed	1	1	0.95V



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Size | Document Number: PARK_Main | Rev: 1A
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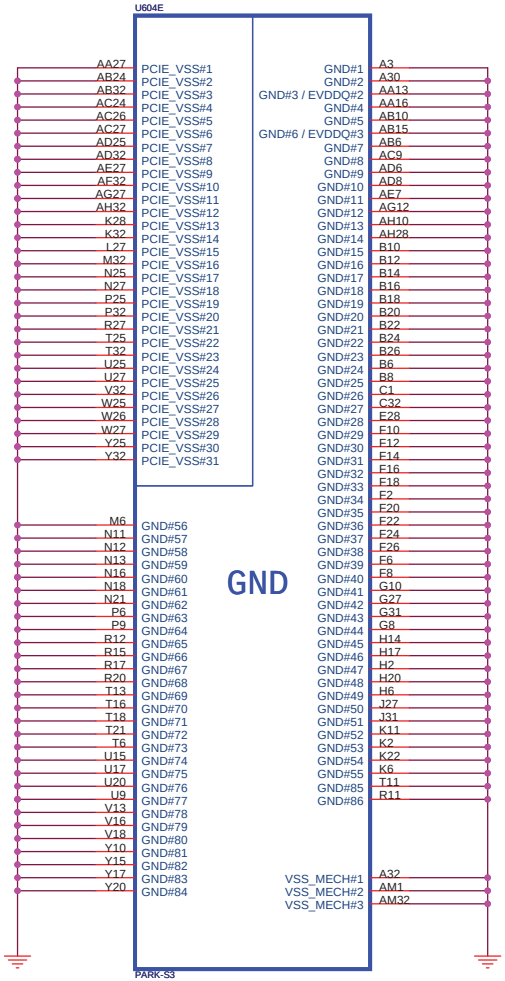
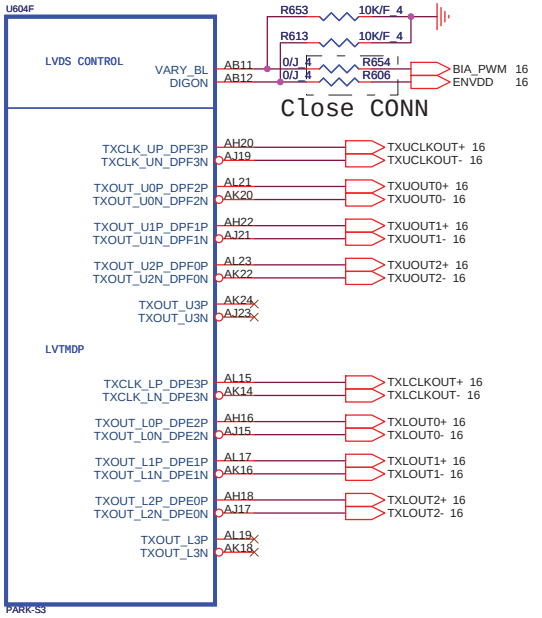
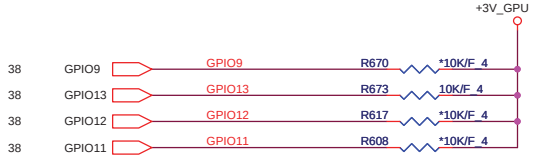






CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	**Transmitter Power Savings Enable** 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	**PCI Express Transmitter De-emphasis Enable** 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

AMD RESERVED CONFIGURATION STRAPS

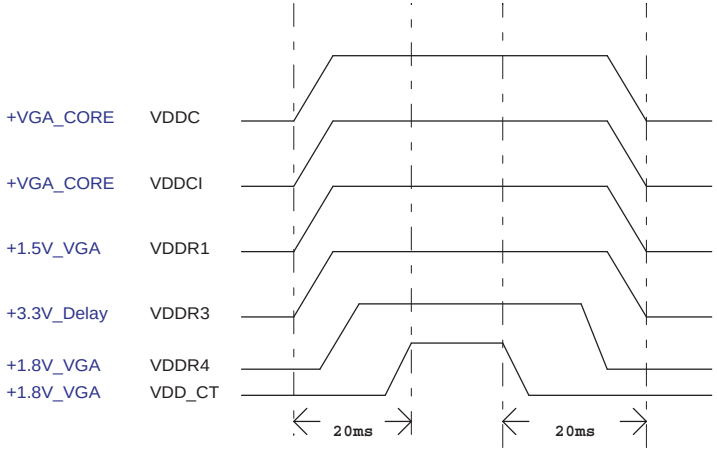
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO21_BB_EN

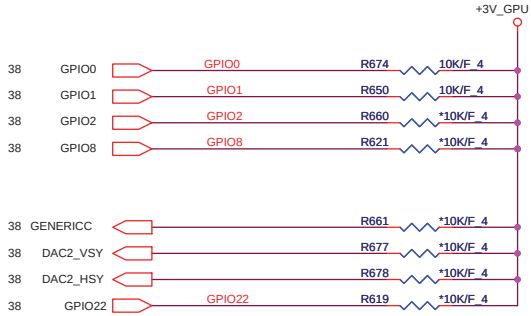
Power Up/Down Sequence



Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.



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Size	Document Number	Rev
	PARK_GND / LVDS/ Straps	1A
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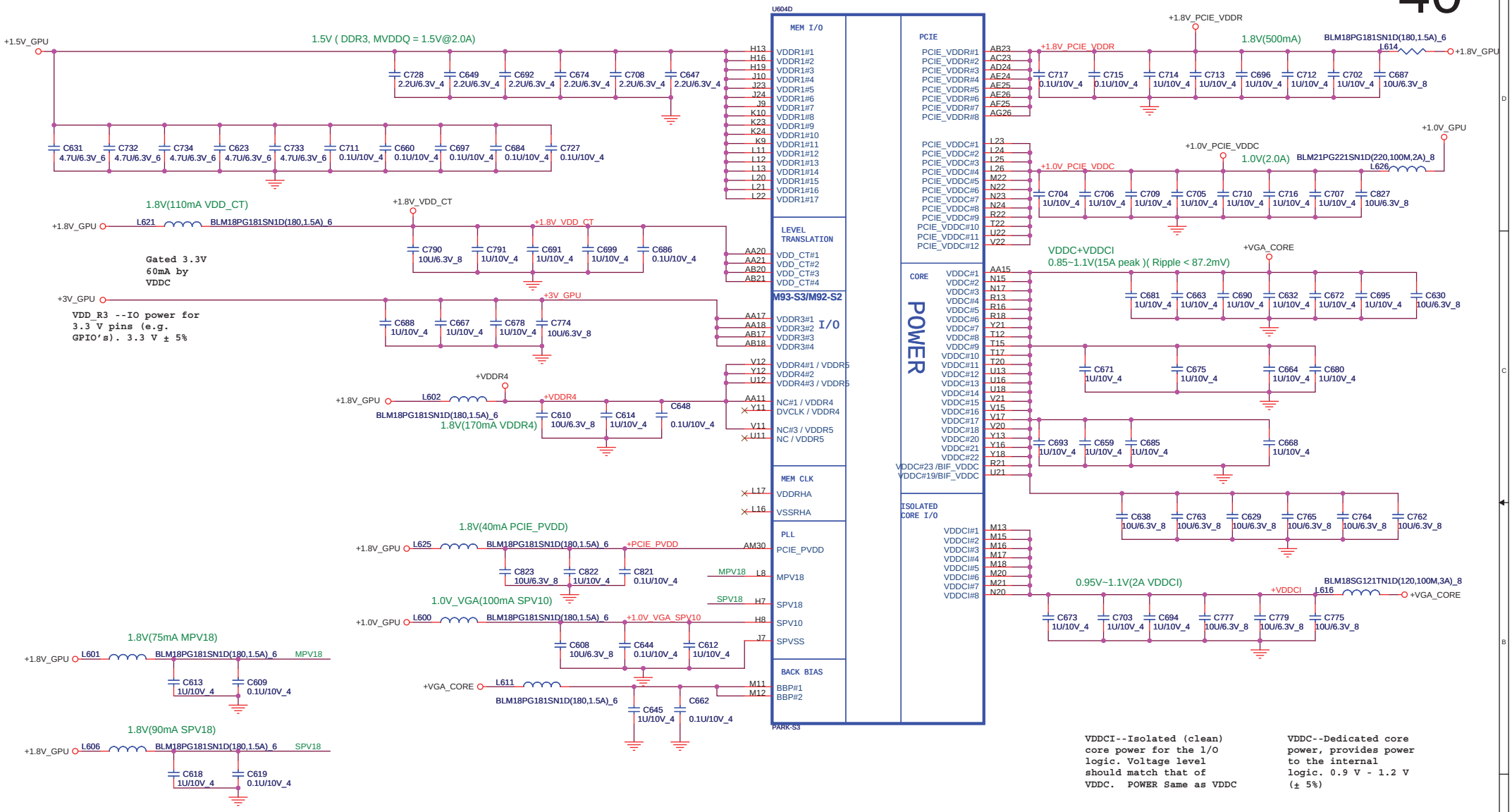
PCIE_VDDR--PCI-E I/O power. 1.8 V ± 5%



VDDRH_1 & VDDRH_2 --Dedicated power pins for memory clock pads for each channel. Should have the same voltage level as VDDR1.

VDDCI--Isolated (clean) core power for the I/O logic. Voltage level should match that of VDDC. POWER Same as VDDC

VDDC--Dedicated core power, provides power to the internal logic. 0.9 V - 1.2 V (± 5%)

PCIE_VDDC--PCI-E Digital Power Supply (Either 1.0 V or 1.1 V) 1.0 V -5% to 1.1 V +5%

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PROJECT : FH1A

Size	Document Number	Rev
	PARK_Power_and_NC	1A
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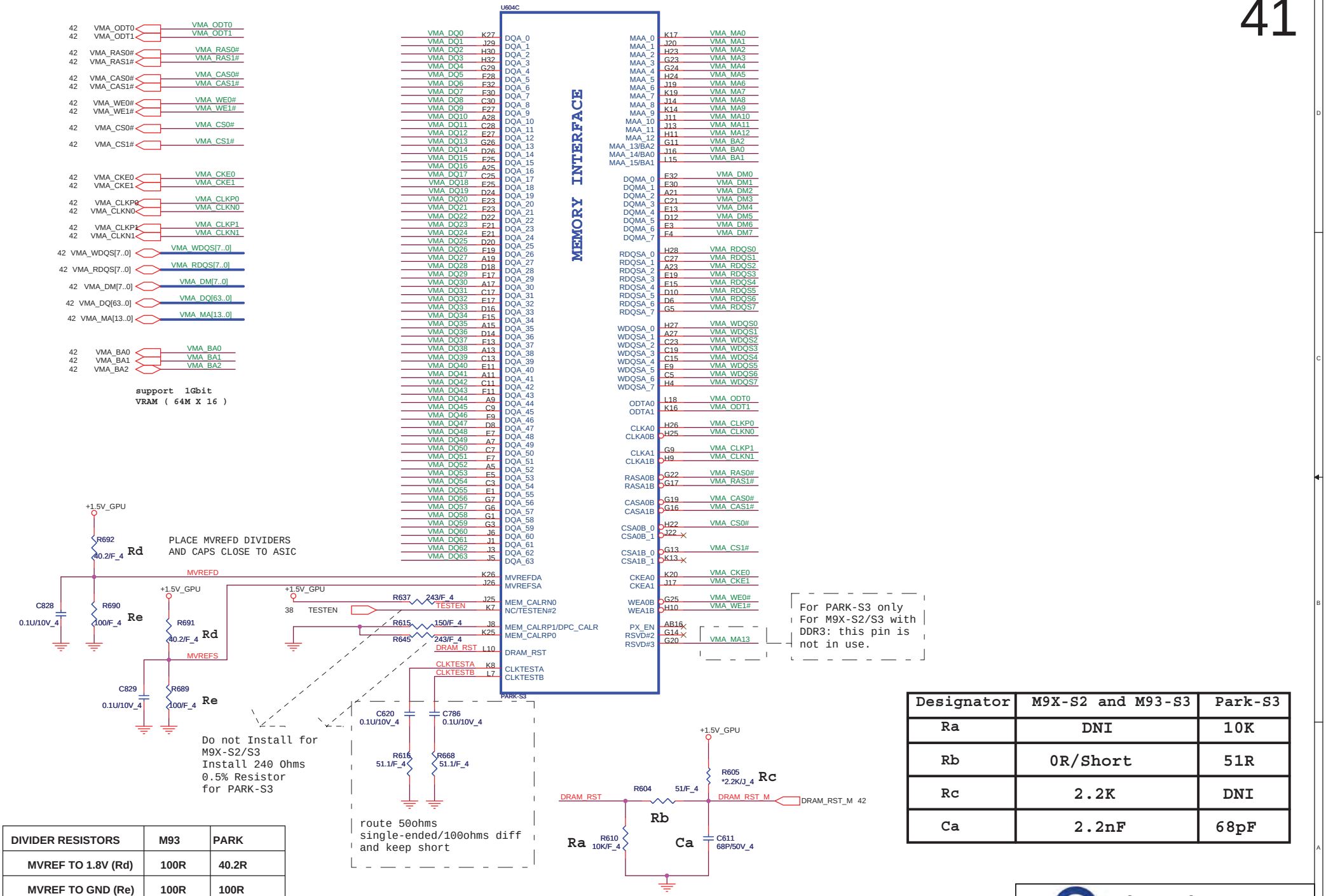

DIVIDER RESISTORS	M93	PARK
MVREF TO 1.8V (Rd)	100R	40.2R
MVREF TO GND (Re)	100R	100R

Designator	M9X-S2 and M93-S3	Park-S3
Ra	DNI	10K
Rb	0R/Short	51R
Rc	2.2K	DNI
Ca	2.2nF	68pF

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Size	Document Number	Rev
	PARK/MEM_Interface	1A
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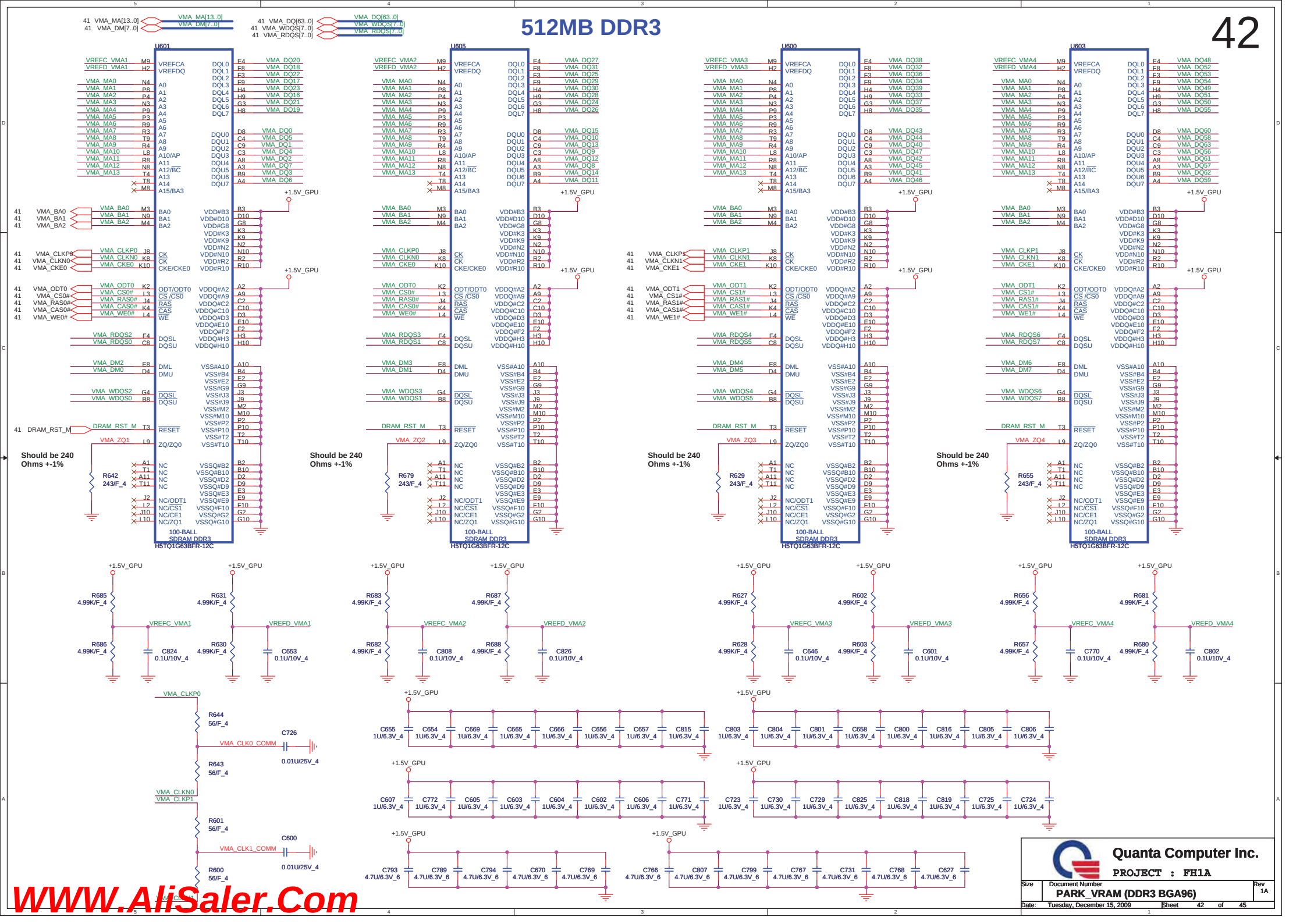
512MB DDR3



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Size	Document Number	Rev
	PARK_VRAM (DDR3 BGA96)	1A

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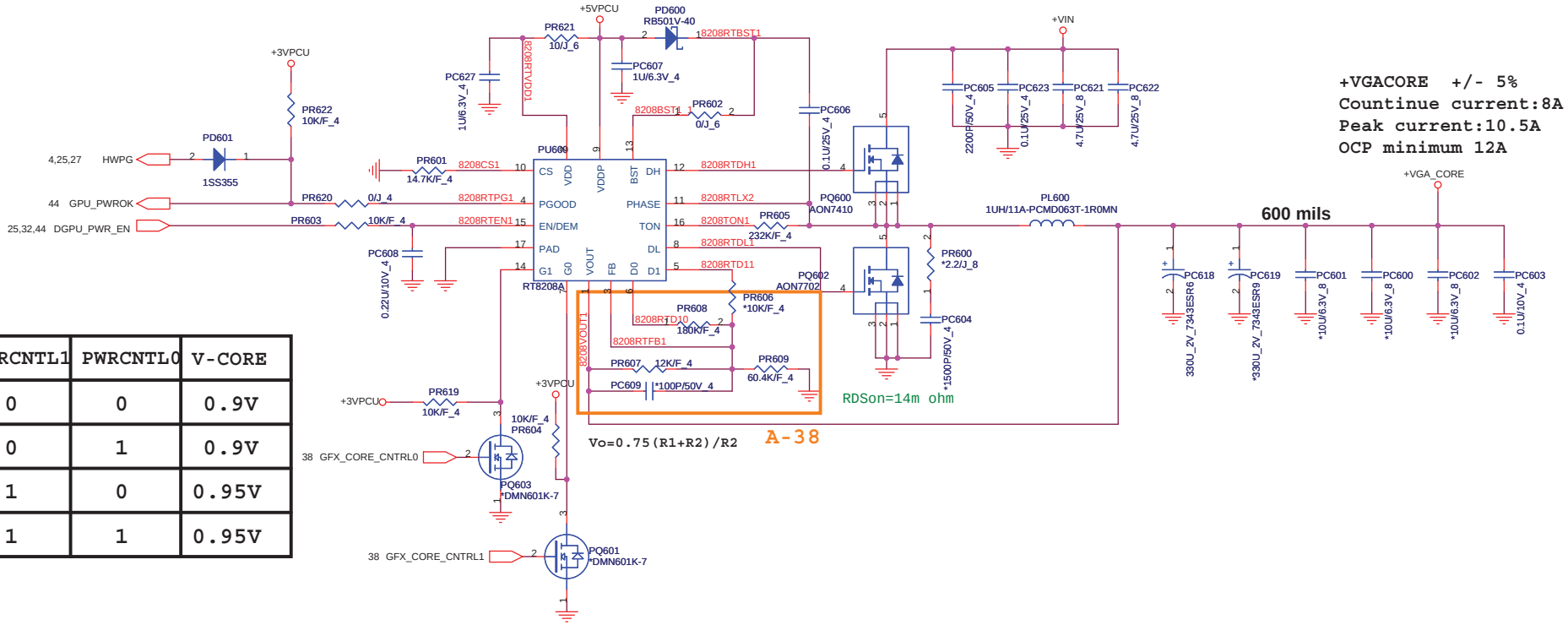
VGA Core



	PWRCNTL1	PWRCNTL0	V-CORE
L	0	0	0.9V
M	0	1	0.9V
H	1	0	0.95V
Fixed	1	1	0.95V

Quanta Computer Inc.

PROJECT : FH1A

Size	Document Number	Rev
	+VGACORE (RT8208/1.8V)	1A

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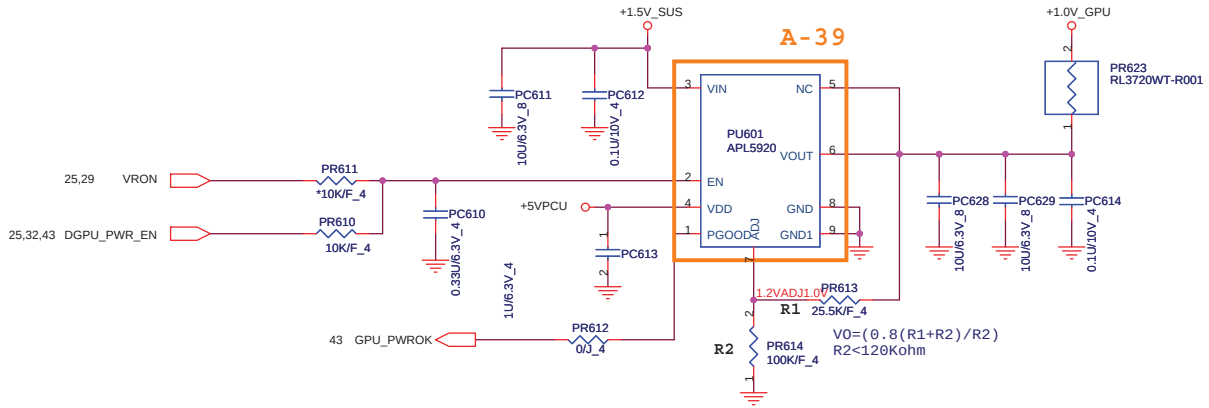
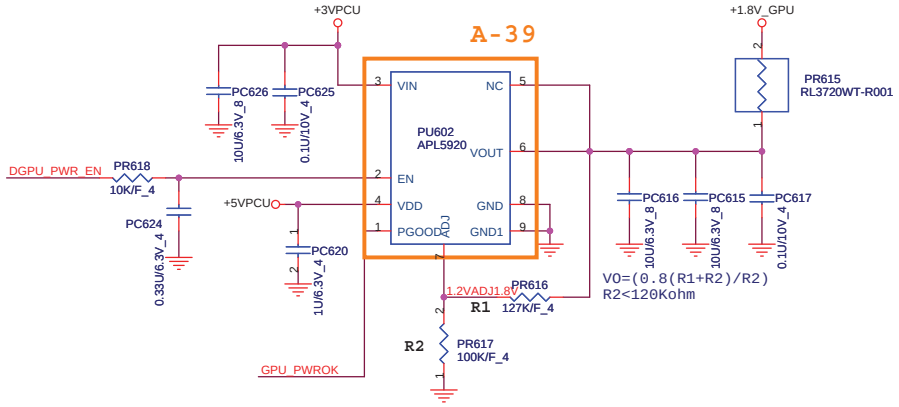
+1.0V +/- 5%
Countinue current:2A
Peak current:3A



+1.8V +/- 5%
Countinue current:1.2A
Peak current:3A



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Size	Document Number	Rev
	DDR3 (RT8207)	1A
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Change List

A-01 PAGE 3,38 : Add EVGA-XTALI and CLK_27M_SS, and stuff R343, nonstuff R416 for providing 27MHz clock.
A-02 PAGE 4,8 : NC FDI_TX[7:0]/FDI_TX#[7:0], and FDI_INT,FDI_FSYNC0/1,FDI_LSYNC0/1 connect to GND for disable UMA setting.
A-03 PAGE 4,37 : Add PEG_RXN[15:0],PEG_RXP[15:0],PEG_TXN[15:0],PEG_TXP[15:0] to connect to Park LP PCIE I/F
A-04 PAGE 4,10 : DPLL_REF_SSCLK/DPLL_REF_SSCLK# pull down and NC in PCH side for Disable UMA setting.
A-05 PAGE 4,38 : Reserve TEMP_FAIL circuit for GPU thermal detect signal control.
A-06 PAGE 6 : VAXG_SENSE,VSSAXG_SENSE,GFX_VID[6:0],GFX_VR_EN,GFX_DPRSLPVR to be NC, VAXG connect to GND, and IMON pull down via R220 10Kohm for Disable UMA
A-07 PAGE 8 : LVDS/CRT signals in PCH side to be NC
A-08 PAGE 9 : RTC Battery Connect CON11 change from Cable type to Socket type(PN : DFHS02FS027)
A-09 PAGE 9,26 : Remove MDC circuit
A-10 PAGE 10,37 : PCI_PLTRST# connect to Park LP PinAL23
A-11 PAGE 10 : Change U4 from OR gate to AND gate
A-12 PAGE 10 : Add PU resistors R468,R469 2.2Kohm
A-13 PAGE 10 : Stuff R211 and Nonstuff Y4,R210,C282,C283
A-14 PAGE 12 : VCCADAC0/1 connecto to +3V_RUN and VSSA_DAC0/1 connect to GND for Disable UMA setting
A-15 PAGE 12 : VCCALVDS,VCCTX_LVDS[4:1] connect to GND, and VSSA_LVDS to be NC for Disable UMA setting
A-16 PAGE 19,25 : Reserve R565 and D27, and Add control signal LAN_PCIE_PWR_CTRL# for LAN Power Saving Control
A-17 PAGE 20 : Delete H13,H20
A-18 PAGE 24 : Add AR23,AR24,AR25,AC36 for ALC269 VA and VB version control
A-19 PAGE 25,32,43,44 : Add Contorl Signal DGPU_PWR_EN to control +VGA_CORE,+3V_GPU,+1.8V_GPU,+1.5V_GPU,+1.0V_GPU Power On/Off
A-20 PAGE 10,25,33,38 : SMBCLK/SMBDATA for Charger and Battery SMBus signals, and SMBCLK2/SMBDATA2 for VGA Thermal Sensor and PCH SMBus signals.
A-21 PAGE 25 : Delete R353
A-22 PAGE 25 : Add MODEL_ID signal to U21 Pin67, and stuff PU resistor R353 10Kohm for MODEL selection
A-23 PAGE 16,26 : Change Fan Controller U2 P/N, and Change LVDS LDO U14 P/N
A-24 PAGE 32 : Add VGA Power and +1.5V_SUS Discharge Circuit
A-25 PAGE 32,43,44 : Add +VGA_CORE,+3V_GPU,+1.5V_GPU,+1.8V_GPU,+1.0V_GPU circuits for Park LP Power
A-26 PAGE 37~42 : Add Park LP circuits
A-27 PAGE 30 : Change PU8 footprint
A-28 PAGE 20 : Add VGA thermal Nut H29, Fan Hole H74 and Modify H12 footprint
A-29 PAGE 29 : Reserve PC39,PC40,PC41,PC43 1uF for Power On/Off Fail issue(Battery Capacity less than 60%)
A-30 PAGE 27 : Change PR95 from 180K to 200K
A-31 PAGE 27 : Change PR98 from 237K to 280K
A-32 PAGE 28 : Change PR148 from 5.1K to 6.8K
A-33 PAGE 30 : Change PR168 from 40.2K to 31.2K
A-34 PAGE 31 : Change PR96 from 10.2K to 12K
A-35 PAGE 32 : Change PR82 from 560 to 1M
A-36 PAGE 32 : Change PR204 from 560 to 1M
A-37 PAGE 33 : Change PD1 & PD2 from ZD3.6V to UDZS5.6BTE-17
A-38 PAGE 43 : Change PR7077 from 10K to 60K, PR7080 from 2K to 12K and PR7095 from 30K to 180K
A-39 PAGE 44 : Change PU7009 & PU7011 from RT9025 to APL5920
A-40 PAGE 29 : Change PQ4 & PQ45 from AOL1448 to RJK03B9DP
A-41 PAGE 29 : Change PQ3, PQ7, PQ41& PQ44 from AOL1718 to RJK03D3DPA
A-42 PAGE 32 : Change PQ7018 from AOL1718 to RJK03D3DPA
A-43 PAGE 32 : Change PC137 & PC152 from CC71004MZ81 to CC71004MZ04