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



## PCI DEVICES IRQ ROUTING

DEVICE	IDSEL #	REQ/GNT #	PCI_INT
Ricoh 5C832	AD25	0	E,F

## PCB STACK UP


LAYER 1 : TOP  
 LAYER 2 : GND  
 LAYER 3 : IN1  
 LAYER 4 : IN2  
 LAYER 5 : GND  
 LAYER 6 : IN3  
 LAYER 7 : VCC  
 LAYER 8 : BOT

## Power & Ground

Label	ACTIVE	Description	Control Signal
VIN	S0, S3, S4, S5	AC ADAPTER (19V)	
MBAT	S0, S3, S4, S5	MAIN BATTERY + (10~17V)	
VCCRTC	S0, S3, S4, S5	RTC & KBC POWER (3_3V)	
+15V	S0, S3, S4, S5	+15V	
CPU_CORE	S0	CPU CORE POWER (1.25/1.15V)	VRON
+1.05V	S0	FSB POWER (1.05V)	VRON
+3V	S0		MAIND
3VSUS	S0, S3		SUSON
3V_S5	S0, S3, S4, S5		S5_ON
3VPCU	S0, S3, S4, S5	ALWAYS POWER (3V)	
+5V	S0		MAIND
5VSUS	S0, S3		SUSON
5V_S5	S0, S3, S4, S5		S5_ON
5VPCU	S0, S3, S4, S5	ALWAYS POWER (5V)	
+1.5V	S0		MAIND
1.5V_S5	S0, S3, S4, S5		S5_ON
1.8VSUS	S0, S3	DDR CORE POWER	SUSON
+2.5V	S0		MAINON
SMDDR_VTERM	S0	DDR COMMAND & CONTROL PULL UP POWER	MAINON
SMDDR_VREF	S0, S3	DDR REF POWER	SUSON
VDDA	S0	AUDIO ANALOG POWER (5V)	MAINON
 GND	ALL PAGES	DIGITAL GROUND	
 AGND		AUDIO GND	
 T-GND		AUDIO JACK GND	
 6260AGND		CPU ANALOG GROUND	

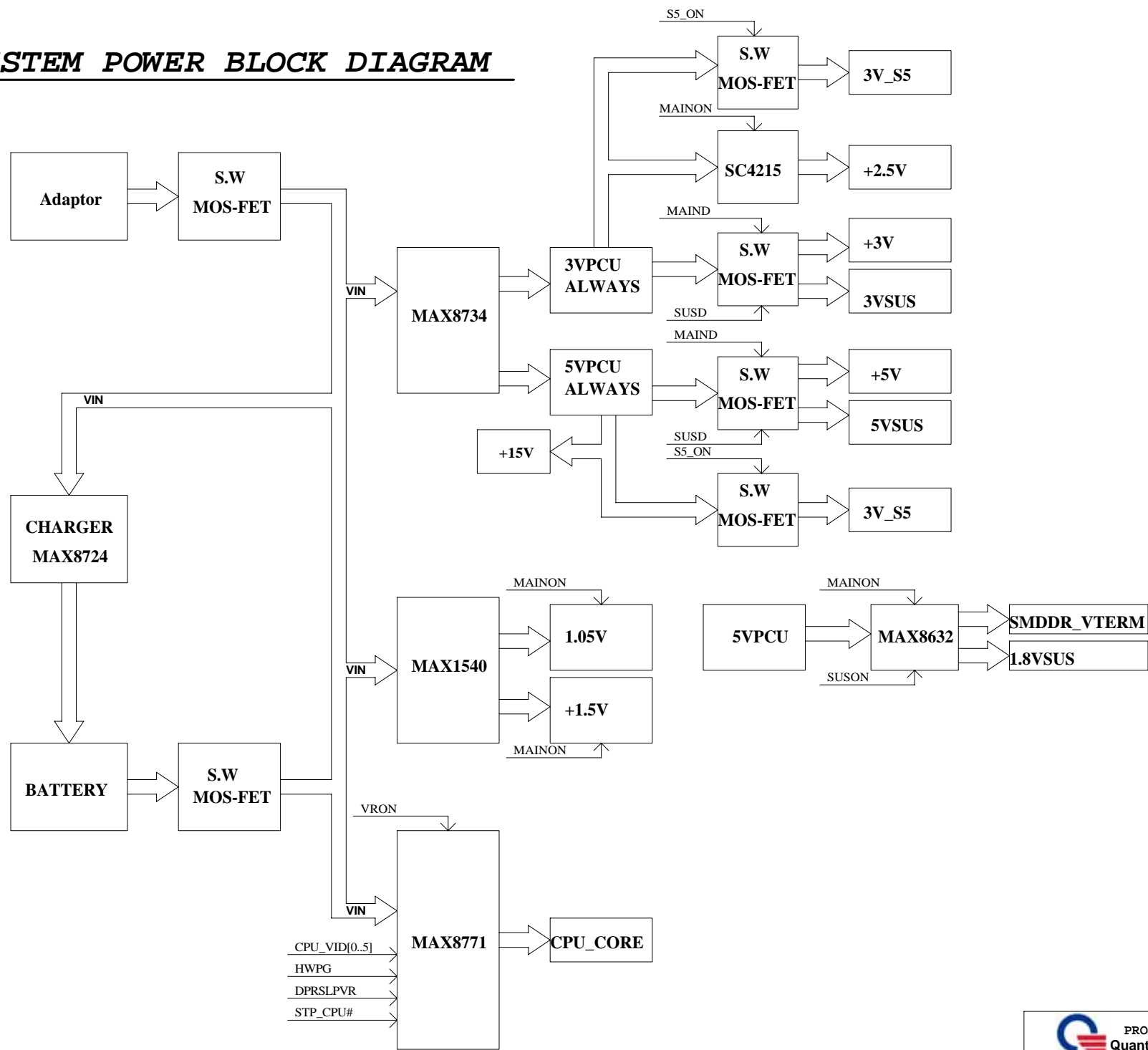
## SM BUS

DEVICE	ADDRESS	BUS
CLOCK GENERATOR	D2H	(ICH6) PCLK_SMB, PCLK_SMB
DDR II	A0H	(ICH6) PCLK_SMB, PCLK_SMB
LCD EDID	TBD	GMCH
CHARGER	16H	(KBC) MBDATA, MBCLK
CPU THERMAL SENSOR	98H	(KBC) MBDATA, MBCLK

 **PROJECT : DW1**  
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Size Custom	Document Number System Information	Rev 1A
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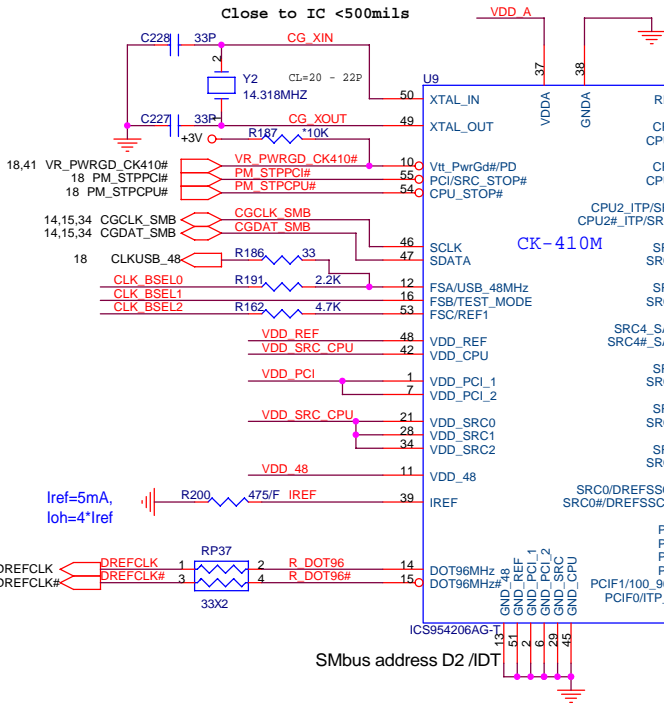
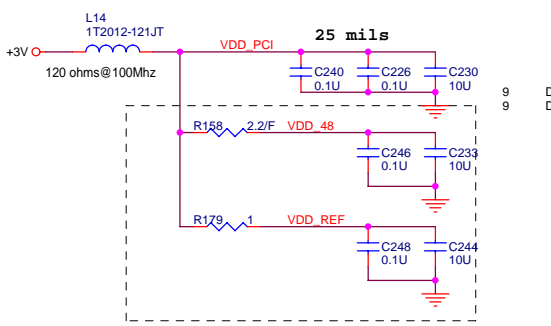
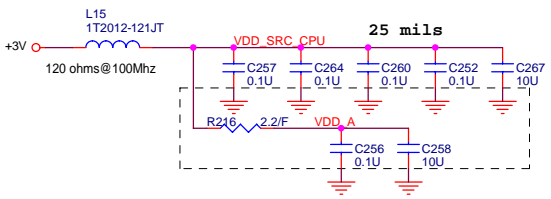
# SYSTEM POWER BLOCK DIAGRAM



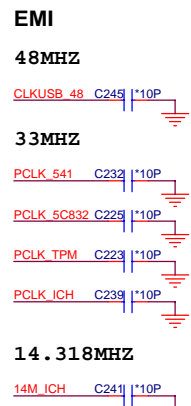
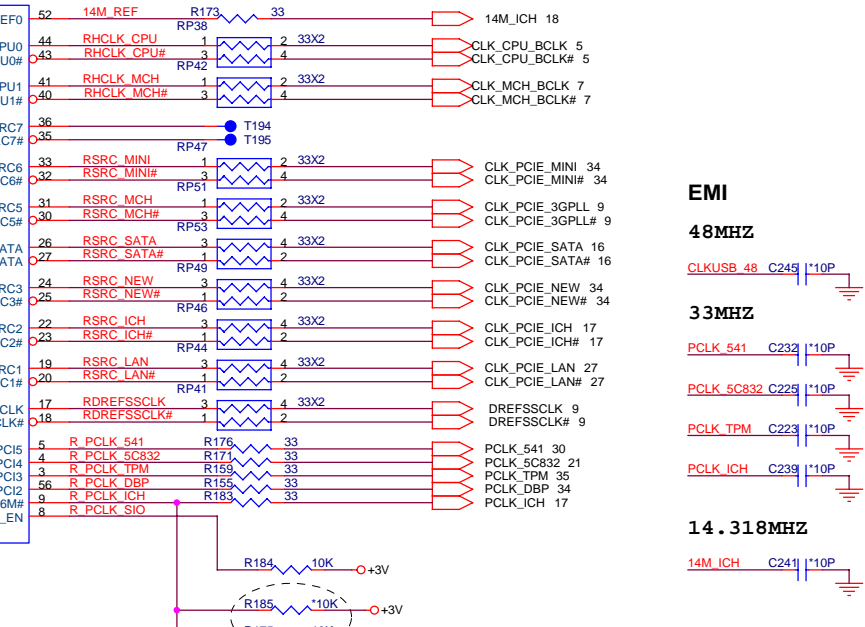
FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	200	100	33

Default

5,9,11,13,14,15,16,17,18,19,20,24,29,30,31,32,33,34,35,36,38 +3V  
 5,6,7,10,11,16,19,36,39 +1.05V



Place these termination to close CK410M.



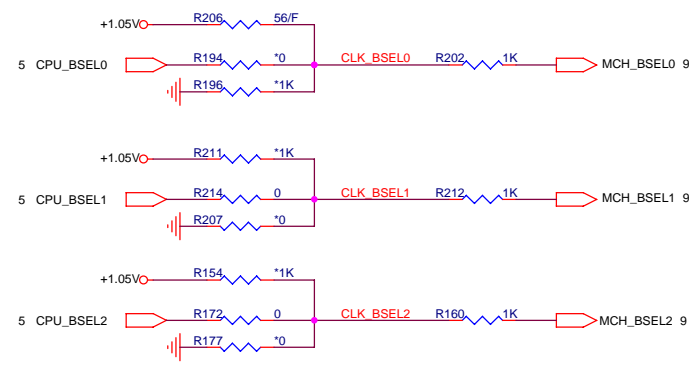
Iref=5mA, loh=4\*Iref

Smbus address D2 /IDT

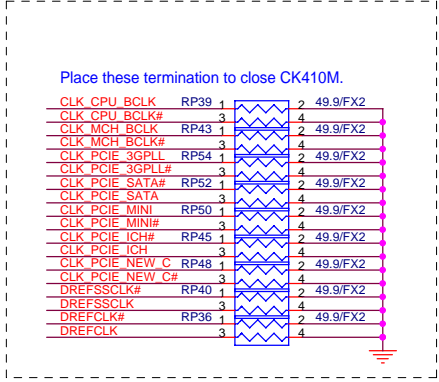
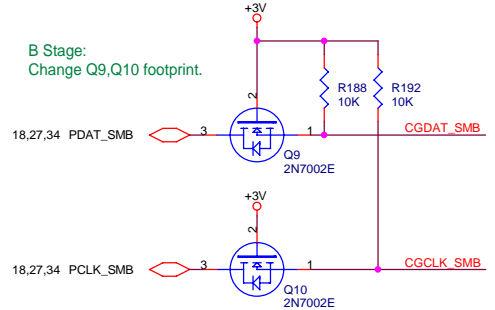
DREFSSCLK Frequency Select.  
 "0" : 96MHz  
 "1" : 100MHz

To check intel reference circuit default setting.  
 100MHZ? or 96MHZ?  
 EMI problem?

FSB frequency will be selected by CPU internal.

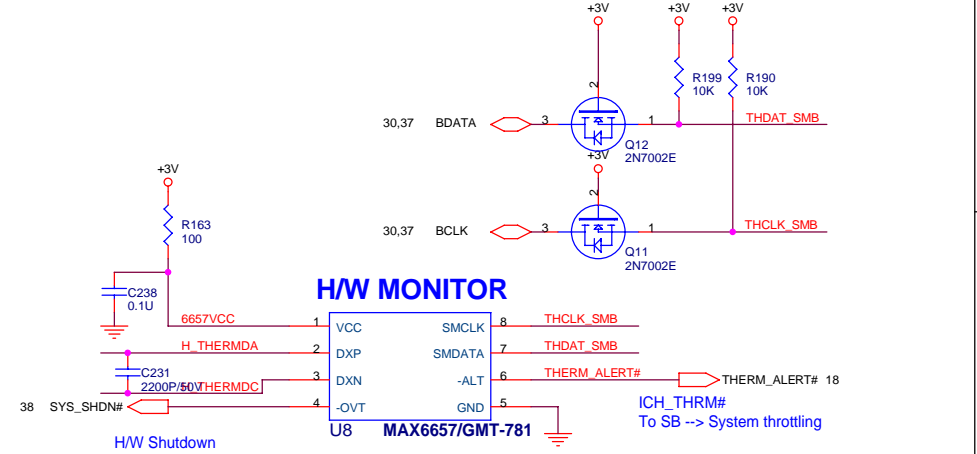
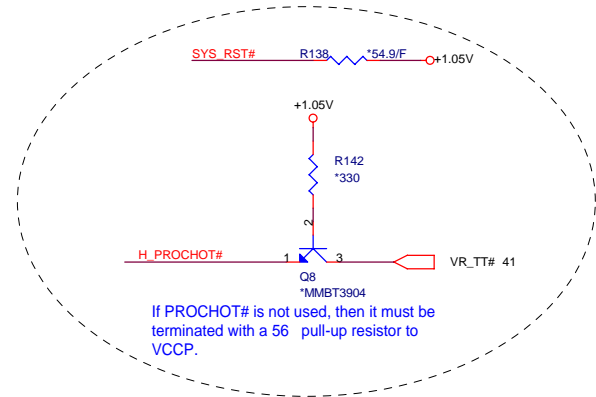
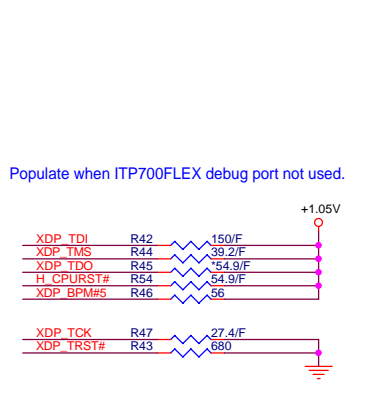
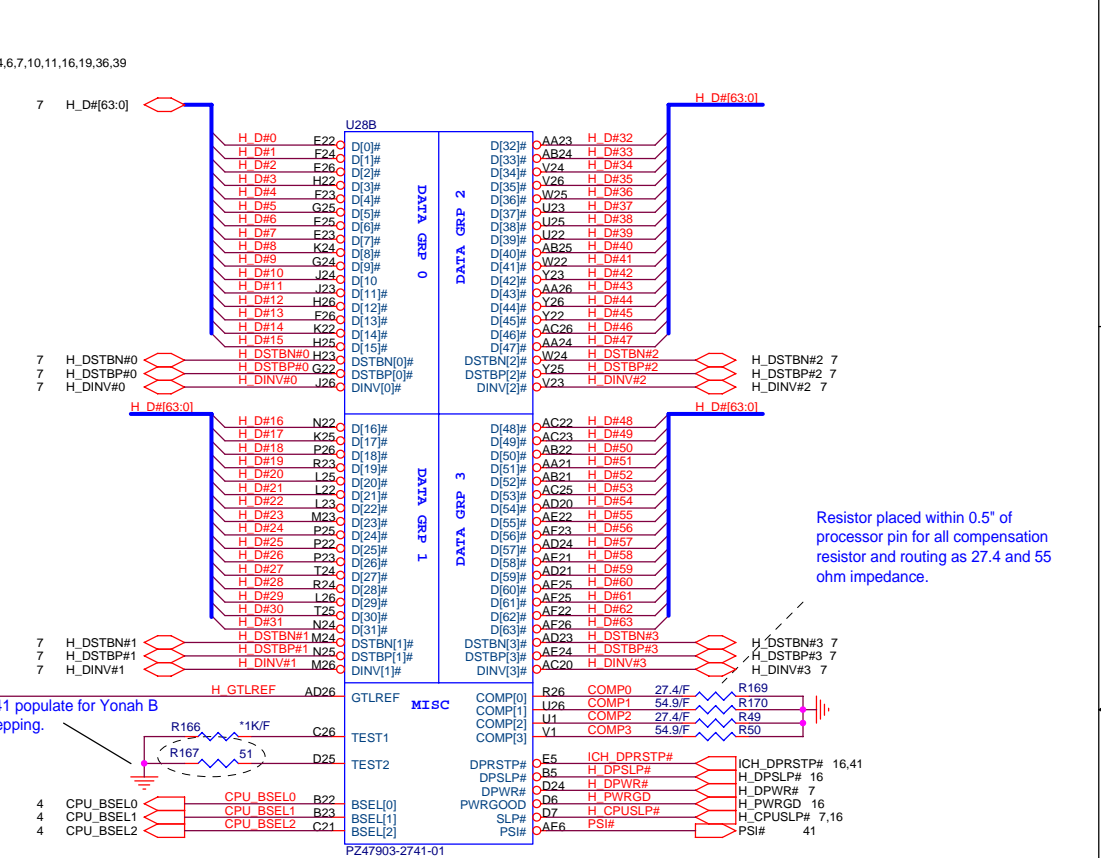
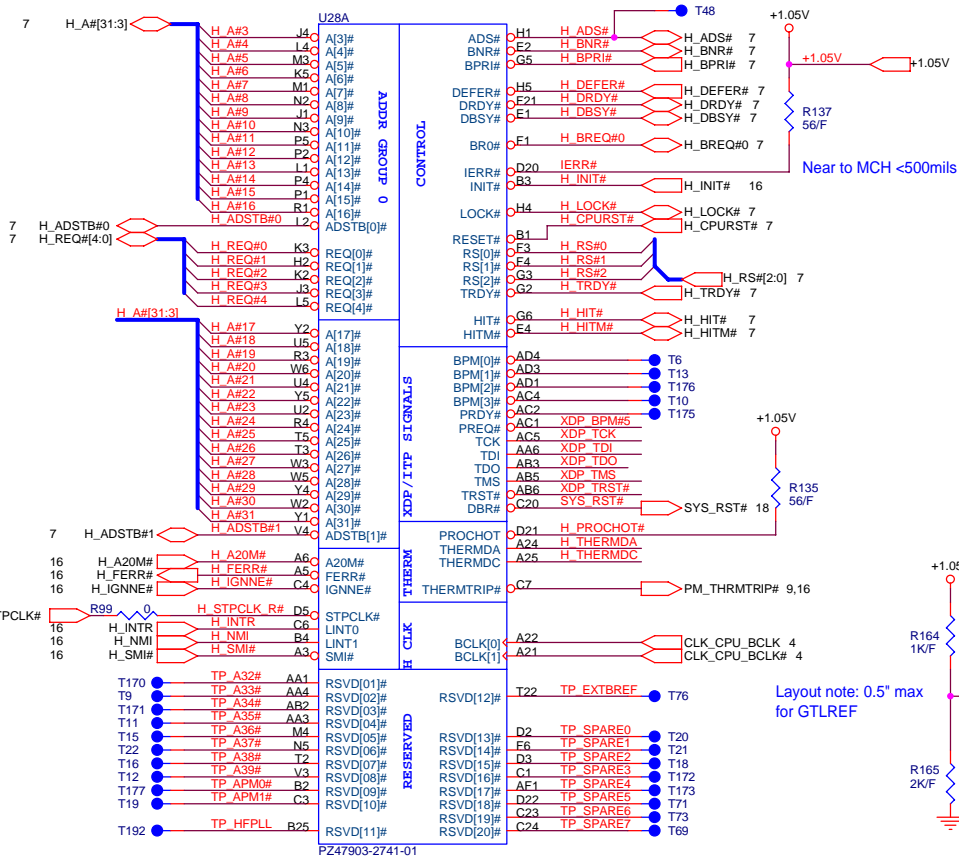


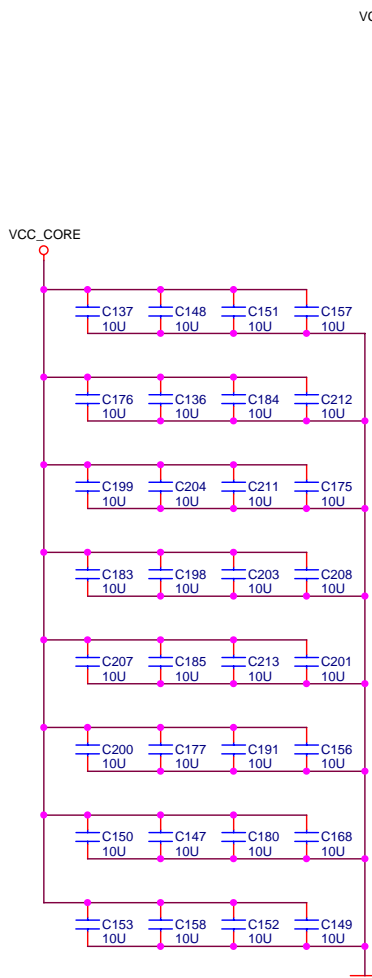
B Stage: Change Q9,Q10 footprint.



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Custom	CLOCK GENERATOR	1A
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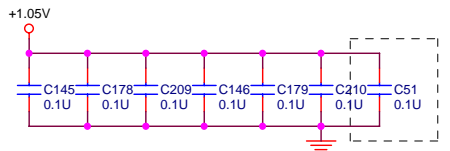
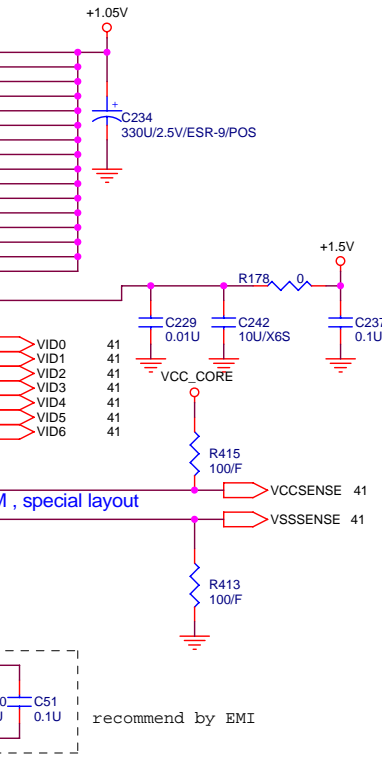


B stage:  
Change to 10UF/X6S material(105C).

U28C		U28D	
A7	VCC[001]	VCC[68]	AB20
A9	VCC[002]	VCC[69]	AC7
A10	VCC[003]	VCC[70]	AC9
A12	VCC[004]	VCC[71]	AC12
A13	VCC[005]	VCC[72]	AC13
A15	VCC[006]	VCC[73]	AC15
A17	VCC[007]	VCC[74]	AC17
A18	VCC[008]	VCC[75]	AC18
A20	VCC[009]	VCC[76]	AD7
B7	VCC[010]	VCC[77]	AD9
B9	VCC[011]	VCC[78]	AD10
B10	VCC[012]	VCC[79]	AD12
B12	VCC[013]	VCC[80]	AD14
B14	VCC[014]	VCC[81]	AD15
B15	VCC[015]	VCC[82]	AD17
B18	VCC[016]	VCC[83]	AD18
B20	VCC[017]	VCC[84]	AE9
C9	VCC[018]	VCC[85]	AE10
C10	VCC[019]	VCC[86]	AE12
C12	VCC[021]	VCC[88]	AE13
C13	VCC[022]	VCC[89]	AE15
C15	VCC[023]	VCC[90]	AE17
C17	VCC[024]	VCC[91]	AE18
C18	VCC[025]	VCC[92]	AE20
D8	VCC[026]	VCC[93]	AE9
D10	VCC[027]	VCC[94]	AE10
D12	VCC[028]	VCC[95]	AE12
D14	VCC[029]	VCC[96]	AE14
D15	VCC[030]	VCC[97]	AE15
D17	VCC[031]	VCC[98]	AE17
D18	VCC[032]	VCC[99]	AE18
E7	VCC[033]	VCC[100]	AE20
E9	VCC[034]		
E10	VCC[035]	VCCP[01]	V6
E12	VCC[036]	VCCP[02]	G21
E13	VCC[037]	VCCP[03]	J6
E15	VCC[038]	VCCP[04]	K6
E17	VCC[039]	VCCP[05]	M6
E20	VCC[040]	VCCP[06]	J21
F7	VCC[041]	VCCP[07]	K21
F9	VCC[042]	VCCP[08]	M21
F10	VCC[043]	VCCP[09]	N21
F12	VCC[044]	VCCP[10]	N6
F14	VCC[045]	VCCP[11]	R21
F15	VCC[046]	VCCP[12]	R6
F17	VCC[047]	VCCP[13]	T21
F18	VCC[048]	VCCP[14]	T6
F20	VCC[049]	VCCP[15]	V21
F20	VCC[050]	VCCP[16]	W21
AA7	VCC[051]		
AA9	VCC[052]	VCCA	B26
AA10	VCC[053]		
AA12	VCC[054]		
AA13	VCC[055]	VID[0]	AD6
AA15	VCC[056]	VID[1]	AE5
AA17	VCC[057]	VID[2]	AE5
AA18	VCC[058]	VID[3]	AE4
AA20	VCC[059]	VID[4]	AE3
AB9	VCC[060]	VID[5]	AE2
AC10	VCC[061]	VID[6]	AE2
AB10	VCC[062]		
AB12	VCC[063]		
AB14	VCC[064]		
AB15	VCC[065]	VCCSENSE	AE7
AB17	VCC[066]		
AB18	VCC[067]	VSSSENSE	AE7

+1.05V  
VCC\_CORE  
+1.5V

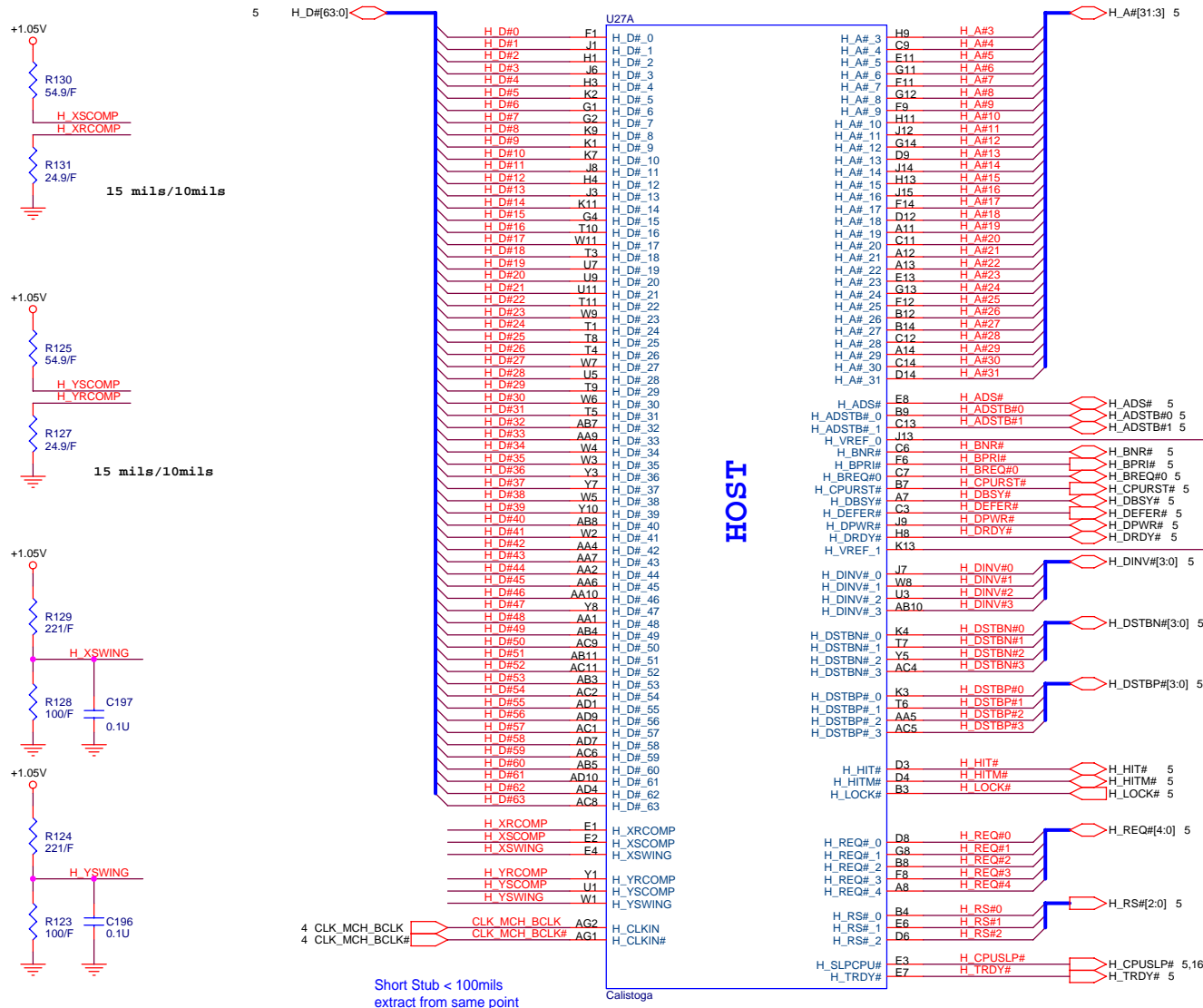
+1.05V 4,5,7,10,11,16,19,36,39  
VCC\_CORE 36,41  
+1.5V 11,17,19,34,36,39



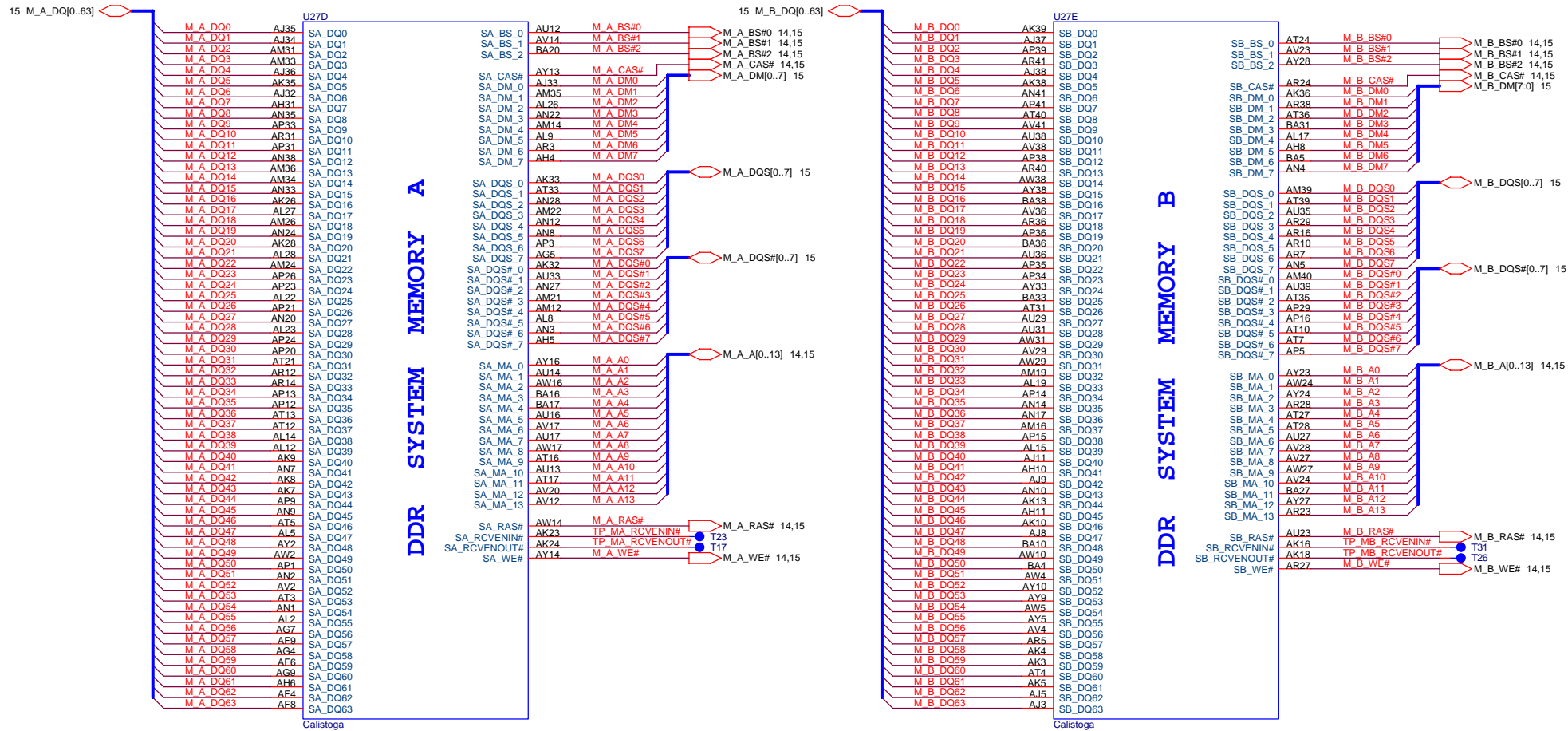
U28D		P6	
A4	VSS[001]	VSS[082]	P21
A8	VSS[002]	VSS[083]	P24
A11	VSS[003]	VSS[084]	R2
A14	VSS[004]	VSS[085]	R5
A16	VSS[005]	VSS[086]	R22
A19	VSS[006]	VSS[087]	R25
A23	VSS[007]	VSS[088]	T1
A26	VSS[008]	VSS[089]	T4
B6	VSS[009]	VSS[090]	T23
B8	VSS[010]	VSS[091]	T26
B11	VSS[011]	VSS[092]	U3
B13	VSS[012]	VSS[093]	U6
B16	VSS[013]	VSS[094]	U21
B19	VSS[014]	VSS[095]	U24
B21	VSS[015]	VSS[096]	V2
B24	VSS[016]	VSS[097]	V5
C5	VSS[017]	VSS[098]	V22
C8	VSS[018]	VSS[099]	V25
C11	VSS[019]	VSS[100]	W1
C14	VSS[020]	VSS[101]	W4
C16	VSS[021]	VSS[102]	W23
C19	VSS[022]	VSS[103]	W26
C2	VSS[023]	VSS[104]	Y3
C22	VSS[024]	VSS[105]	Y6
C25	VSS[025]	VSS[106]	Y21
D1	VSS[026]	VSS[107]	Y24
D4	VSS[027]	VSS[108]	AA2
D8	VSS[028]	VSS[109]	AA5
D11	VSS[029]	VSS[110]	AA8
D13	VSS[030]	VSS[111]	AA11
D19	VSS[031]	VSS[112]	AA14
D23	VSS[032]	VSS[113]	AA16
D26	VSS[033]	VSS[114]	AA19
E3	VSS[034]	VSS[115]	AA22
E6	VSS[036]	VSS[117]	AA25
F8	VSS[037]	VSS[118]	AB1
F11	VSS[038]	VSS[119]	AB4
F14	VSS[039]	VSS[120]	AB8
F16	VSS[040]	VSS[121]	AB11
F19	VSS[041]	VSS[122]	AB13
F21	VSS[042]	VSS[123]	AB16
F24	VSS[043]	VSS[124]	AB19
F5	VSS[044]	VSS[125]	AB23
F8	VSS[045]	VSS[126]	AB26
F11	VSS[046]	VSS[127]	AC3
F13	VSS[047]	VSS[128]	AC6
F16	VSS[048]	VSS[129]	AC8
F19	VSS[049]	VSS[130]	AC11
F2	VSS[050]	VSS[131]	AC14
F22	VSS[051]	VSS[132]	AC16
F25	VSS[052]	VSS[133]	AC19
G4	VSS[053]	VSS[134]	AC21
G1	VSS[054]	VSS[135]	AC24
G23	VSS[055]	VSS[136]	AD2
G26	VSS[056]	VSS[137]	AD5
H3	VSS[057]	VSS[138]	AD8
H6	VSS[058]	VSS[139]	AD11
H21	VSS[059]	VSS[140]	AD13
H24	VSS[060]	VSS[141]	AD16
J2	VSS[061]	VSS[142]	AD19
J5	VSS[062]	VSS[143]	AD22
J22	VSS[063]	VSS[144]	AD25
J25	VSS[064]	VSS[145]	AE1
K1	VSS[065]	VSS[146]	AE4
K4	VSS[066]	VSS[147]	AE8
K23	VSS[067]	VSS[148]	AE11
L3	VSS[068]	VSS[149]	AE14
L6	VSS[069]	VSS[150]	AE16
L21	VSS[070]	VSS[151]	AE19
L24	VSS[071]	VSS[152]	AE23
M2	VSS[072]	VSS[153]	AE26
M5	VSS[073]	VSS[154]	AE3
M22	VSS[074]	VSS[155]	AE6
M25	VSS[075]	VSS[156]	AE8
N1	VSS[076]	VSS[157]	AE11
N4	VSS[077]	VSS[158]	AE13
N23	VSS[078]	VSS[159]	AE16
N26	VSS[079]	VSS[160]	AE19
P3	VSS[080]	VSS[161]	AE21
	VSS[081]	VSS[162]	AE24

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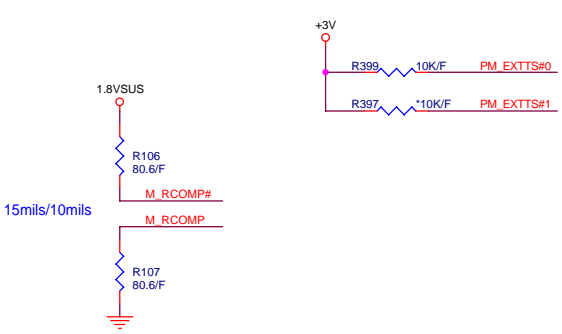
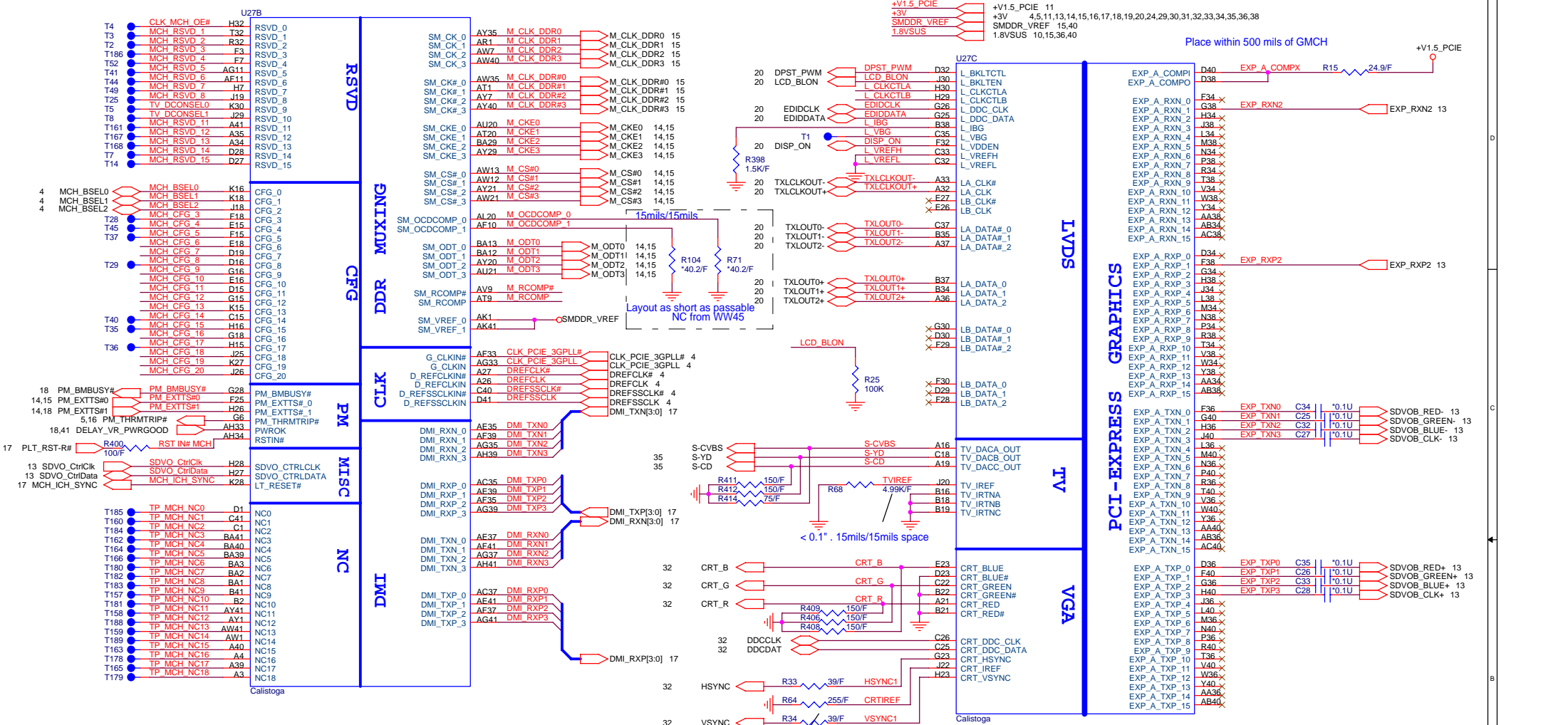
Size B	Document Number	Rev 1A
<b>CPU POWER/GND (2 OF 2)</b>		
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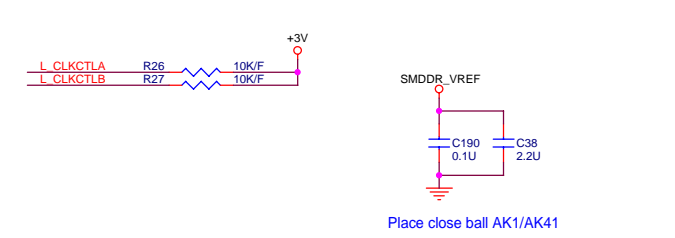






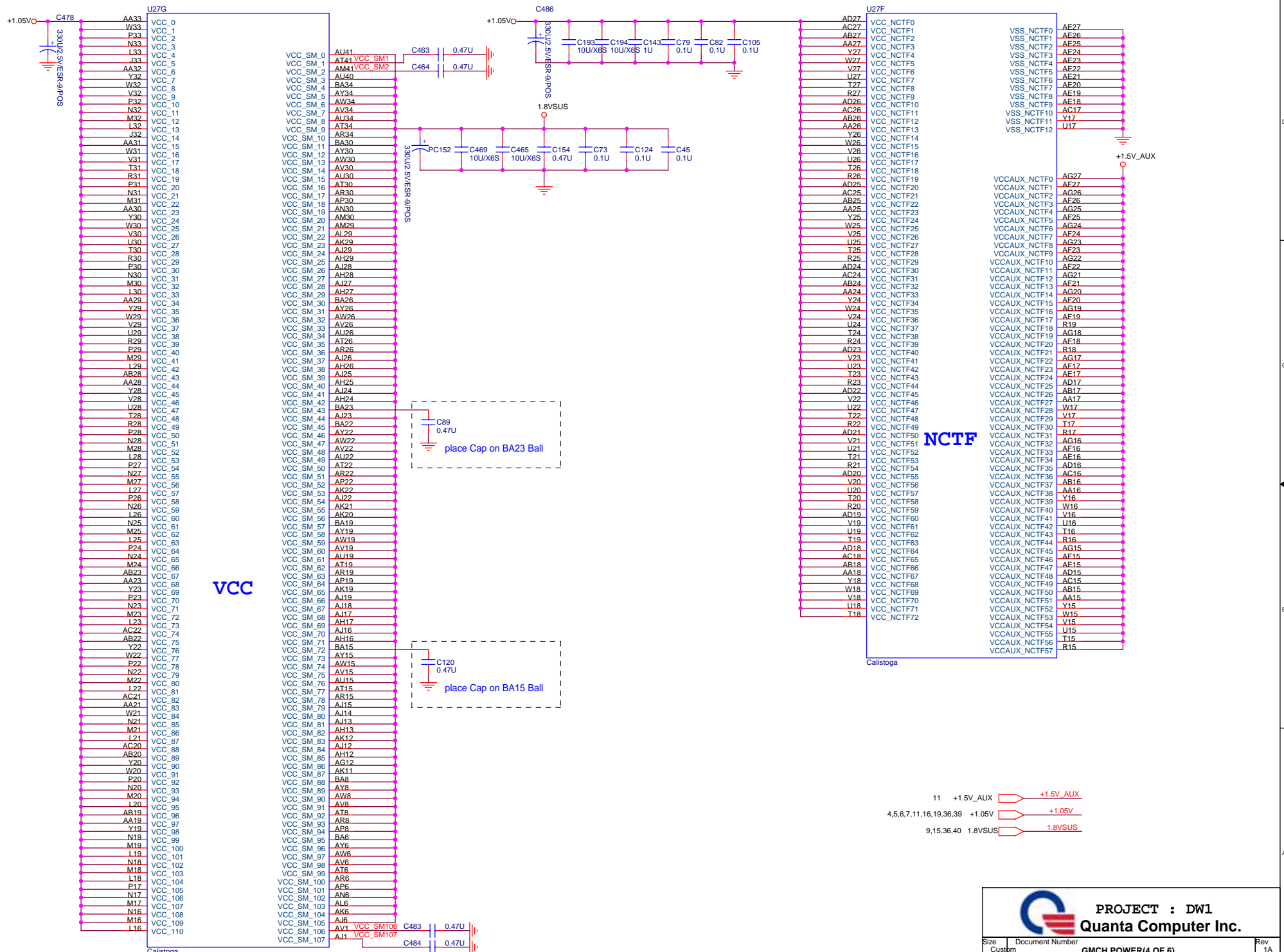
**GMCH Strap pin need to check**

MCH_CFG_5	R82	*2.2K	1.MCH_CFG_5 Low = DMI X2, High=DMIX4
MCH_CFG_6	R103	*2.2K	2.MCH_CFG_6 DDR: Low=Moby Dick, High= Callistoga (Default)
MCH_CFG_7	R17	*2.2K	3.MCH_CFG_7 CPU Strap Low=RSVD, High=Mobile CPU
MCH_CFG_8	R77	*2.2K	4.MCH_CFG_8 PCIE Exp Graphics Lane: Low=Reserved,High=Mobility
MCH_CFG_10	R108	*2.2K	5.MCH_CFG_10 Host PLL VCC Select Low=Reserved, High=Mobility
MCH_CFG_11	R109	*2.2K	6.MCH_CFG_11: Low=Callistoga, High=Reserved
MCH_CFG_12	R105	*2.2K	
MCH_CFG_13	R95	*2.2K	
MCH_CFG_16	R75	*2.2K	7.MCH_CFG_16 FSB Dynamic ODT: Low=Dynamic ODT Disabled, High=Dynamic ODT Enabled
MCH_CFG_19	R396	*1K/F	8.MCH_CFG_19 DMI LANE Reversal:Low=Normal, High=LANES Reverse
MCH_CFG_18	R59	*1K	9.MCH_CFG_18 VCC Select: Low=1.05V, High=1.5V
MCH_CFG_20	R41	*1K/F	10.MCH_CFG_20 PCIE Backward interoperability mode: Low= only SDVO or PCIE x1 is operational (defaults), High=SDVO and PCIE x1 are operation simultaneously via the PEG port.



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Size	Document Number	Rev
Custom	<b>GMCH DMI VEDIO(3 OF 6)</b>	1A
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VCC

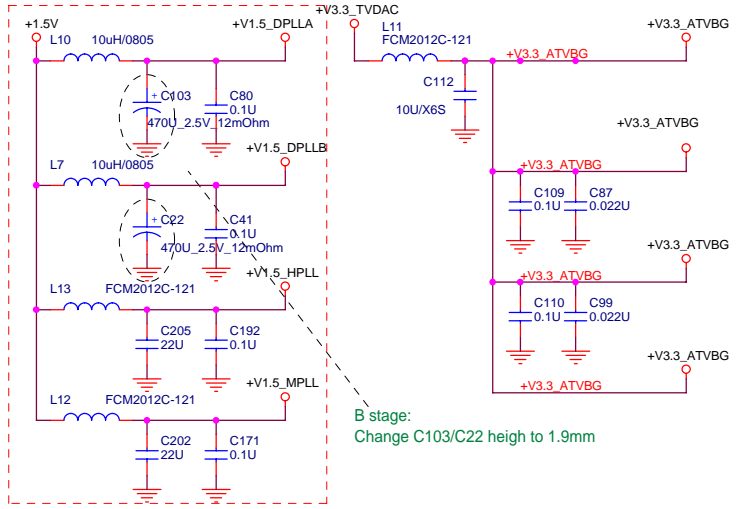
NCTF

Calistoga

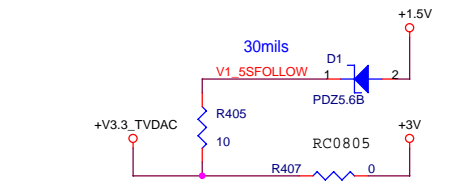
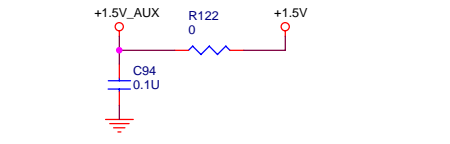
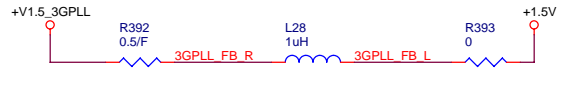
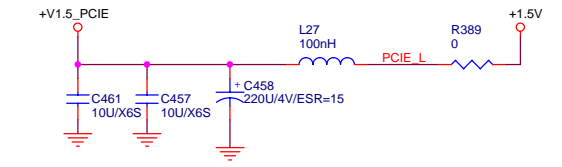
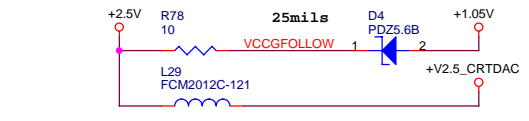
- 11 +1.5V\_AUX
- 4,5,6,7,11,16,19,36,39 +1.05V
- 9,15,36,40 1.8VSUS

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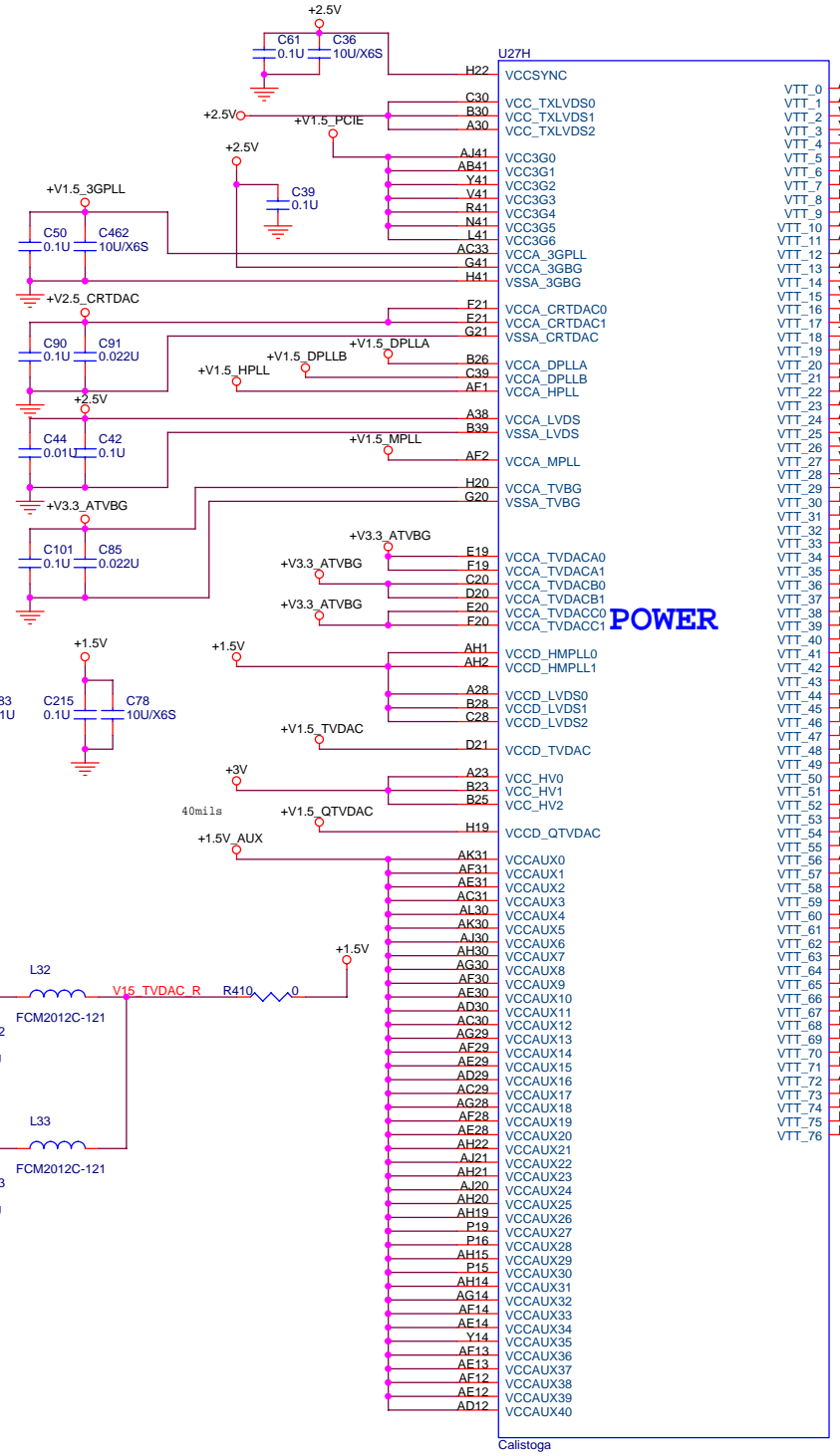
Size	Document Number	Rev
Custpm	GMCH POWER(4 of 6)	1A
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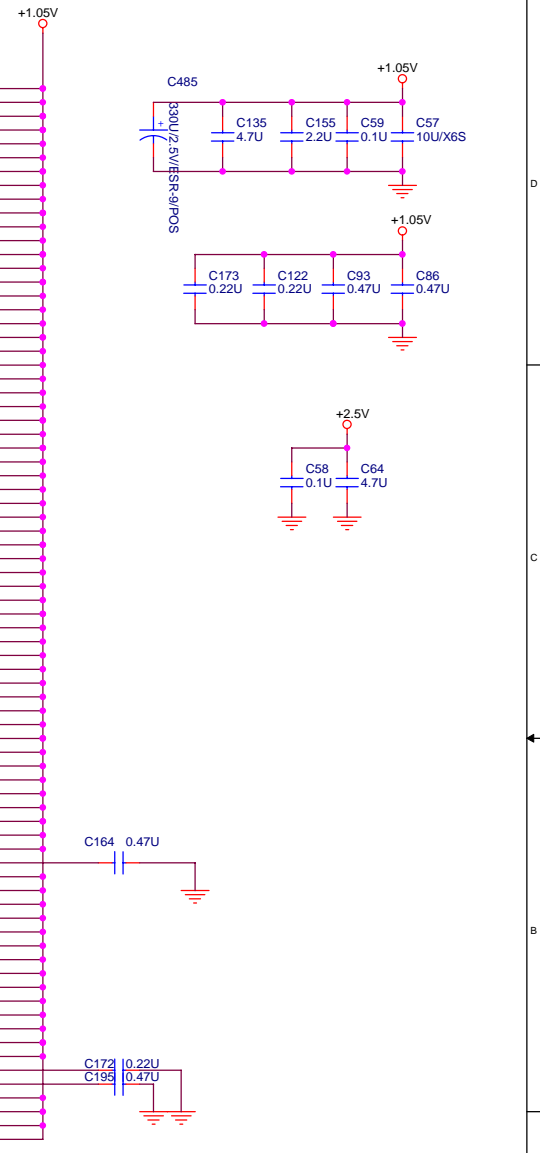
B stage:  
Change C103/C22 height to 1.9mm




+1.05V	+1.05V	4, 5, 6, 7, 10, 16, 19, 36, 39
+1.5V	+1.5V	6, 17, 19, 34, 36, 39
+V1.5_PCIE	+V1.5_PCIE	9
+2.5V	+2.5V	13, 35, 36, 39
+3V	+3V	4, 5, 9, 13, 14, 15, 16, 17, 18, 19, 20, 24, 29, 30, 31, 32, 33, 34, 35, 36, 38



**POWER**



Need to check.  
HF: Two 0402 @ 0.22 uF (one cap placed at the Edge pin location D2, one cap placed at power corridor); Two 0603 @ 0.47 uF (placed at Edge pin locations AB1 and A6)



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Custom	GMCH POWER (5 OF 6)	1A
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U27I		VSS	
AC41	VSS_0	VSS_97	AK34
AA41	VSS_1	VSS_98	AG34
V41	VSS_2	VSS_99	AF34
T41	VSS_3	VSS_100	AE34
P41	VSS_4	VSS_101	AC34
M41	VSS_5	VSS_102	C34
J41	VSS_6	VSS_103	AW33
F41	VSS_7	VSS_104	AV33
AV40	VSS_8	VSS_105	AP33
AF40	VSS_9	VSS_106	AE33
AN40	VSS_10	VSS_107	AB33
AK40	VSS_11	VSS_108	Y33
AL40	VSS_12	VSS_109	V33
AH40	VSS_13	VSS_110	T33
AG40	VSS_14	VSS_111	R33
AF40	VSS_15	VSS_112	M33
AE40	VSS_16	VSS_113	H33
E40	VSS_17	VSS_114	G33
AY39	VSS_18	VSS_115	F33
AW39	VSS_19	VSS_116	D33
AV39	VSS_20	VSS_117	B33
AR39	VSS_21	VSS_118	AH32
AN39	VSS_22	VSS_119	AG32
AJ39	VSS_23	VSS_120	AF32
AC39	VSS_24	VSS_121	AE32
AB39	VSS_25	VSS_122	AC32
AA39	VSS_26	VSS_123	AB32
Y39	VSS_27	VSS_124	G32
W39	VSS_28	VSS_125	B32
V39	VSS_29	VSS_126	AY31
T39	VSS_30	VSS_127	AV31
R39	VSS_31	VSS_128	AN31
P39	VSS_32	VSS_129	AJ31
N39	VSS_33	VSS_130	AG31
M39	VSS_34	VSS_131	AB31
L39	VSS_35	VSS_132	Y31
J39	VSS_36	VSS_133	AB30
H39	VSS_37	VSS_134	E30
G39	VSS_38	VSS_135	AT29
F39	VSS_39	VSS_136	AN29
D39	VSS_40	VSS_137	AB29
AT38	VSS_41	VSS_138	T29
AM38	VSS_42	VSS_139	N29
AH38	VSS_43	VSS_140	K29
AG38	VSS_44	VSS_141	G29
AF38	VSS_45	VSS_142	E29
AE38	VSS_46	VSS_143	C29
C38	VSS_47	VSS_144	B29
AK37	VSS_48	VSS_145	A29
AH37	VSS_49	VSS_146	BA28
AB37	VSS_50	VSS_147	AW28
AA37	VSS_51	VSS_148	AU28
Y37	VSS_52	VSS_149	AP28
W37	VSS_53	VSS_150	AM28
V37	VSS_54	VSS_151	AD28
T37	VSS_55	VSS_152	AC28
R37	VSS_56	VSS_153	W28
P37	VSS_57	VSS_154	J28
N37	VSS_58	VSS_155	E28
M37	VSS_59	VSS_156	AP27
L37	VSS_60	VSS_157	AM27
J37	VSS_61	VSS_158	AK27
H37	VSS_62	VSS_159	J27
G37	VSS_63	VSS_160	G27
F37	VSS_64	VSS_161	F27
D37	VSS_65	VSS_162	C27
AY36	VSS_66	VSS_163	B27
AW36	VSS_67	VSS_164	AN26
AV36	VSS_68	VSS_165	M26
AH36	VSS_69	VSS_166	K26
AG36	VSS_70	VSS_167	F26
AF36	VSS_71	VSS_168	D26
AE36	VSS_72	VSS_169	AK25
AC36	VSS_73	VSS_170	P25
C36	VSS_74	VSS_171	K25
B36	VSS_75	VSS_172	H25
BA35	VSS_76	VSS_173	E25
AV35	VSS_77	VSS_174	D25
AR35	VSS_78	VSS_175	A25
AH35	VSS_79	VSS_176	BA24
AB35	VSS_80	VSS_177	AU24
AA35	VSS_81	VSS_178	AL24
Y35	VSS_82	VSS_179	AW23
W35	VSS_83		
V35	VSS_84		
T35	VSS_85		
R35	VSS_86		
P35	VSS_87		
N35	VSS_88		
M35	VSS_89		
L35	VSS_90		
J35	VSS_91		
H35	VSS_92		
G35	VSS_93		
F35	VSS_94		
D35	VSS_95		
AN34	VSS_96		

Calistoga

U27J		VSS	
AT23	VSS_180	VSS_273	J11
AN23	VSS_181	VSS_274	D11
AM23	VSS_182	VSS_275	B11
AH23	VSS_183	VSS_276	AV10
AC23	VSS_184	VSS_277	AP10
W23	VSS_185	VSS_278	AL10
K23	VSS_186	VSS_279	AJ10
AV33	VSS_187	VSS_280	AG10
F23	VSS_188	VSS_281	AC10
C23	VSS_189	VSS_282	W10
AA22	VSS_190	VSS_283	L10
K22	VSS_191	VSS_284	BA9
G22	VSS_192	VSS_285	AW9
F22	VSS_193	VSS_286	AR9
E22	VSS_194	VSS_287	AH9
D22	VSS_195	VSS_288	AB9
A22	VSS_196	VSS_289	Y9
BA21	VSS_197	VSS_290	R9
AV21	VSS_198	VSS_291	G9
AR21	VSS_199	VSS_292	E9
AN21	VSS_200	VSS_293	A9
AL21	VSS_201	VSS_294	AG8
AB21	VSS_202	VSS_295	AD8
Y21	VSS_203	VSS_296	AA8
P21	VSS_204	VSS_297	U8
K21	VSS_205	VSS_298	K8
AB32	VSS_206	VSS_299	C8
H21	VSS_207	VSS_300	BA7
C21	VSS_208	VSS_301	AV7
AW20	VSS_209	VSS_302	AP7
AR20	VSS_210	VSS_303	AL7
AM20	VSS_211	VSS_304	AJ7
AA20	VSS_212	VSS_305	AH7
K20	VSS_213	VSS_306	AF7
B20	VSS_214	VSS_307	AC7
Y20	VSS_215	VSS_308	R7
AN19	VSS_216	VSS_309	G7
AC19	VSS_217	VSS_310	D7
W19	VSS_218	VSS_311	AG6
K19	VSS_219	VSS_312	AD6
G19	VSS_220	VSS_313	AB6
C19	VSS_221	VSS_314	Y6
AH18	VSS_222	VSS_315	U6
K18	VSS_223	VSS_316	N6
H18	VSS_224	VSS_317	K6
D18	VSS_225	VSS_318	H6
A18	VSS_226	VSS_319	B6
AY17	VSS_227	VSS_320	AV5
AR17	VSS_228	VSS_321	AF5
AP17	VSS_229	VSS_322	AD5
AM17	VSS_230	VSS_323	AY4
AK17	VSS_231	VSS_324	AR4
AV16	VSS_232	VSS_325	AP4
AN16	VSS_233	VSS_326	AL4
AL16	VSS_234	VSS_327	AJ4
J16	VSS_235	VSS_328	Y4
F16	VSS_236	VSS_329	U4
C16	VSS_237	VSS_330	R4
AN15	VSS_238	VSS_331	J4
AM15	VSS_239	VSS_332	F4
AK15	VSS_240	VSS_333	C4
N15	VSS_241	VSS_334	AY3
M15	VSS_242	VSS_335	AW3
L15	VSS_243	VSS_336	AV3
B15	VSS_244	VSS_337	AL3
A15	VSS_245	VSS_338	AH3
BA14	VSS_246	VSS_339	AG3
AT14	VSS_247	VSS_340	AF3
AK14	VSS_248	VSS_341	AD3
K14	VSS_249	VSS_342	AC3
AD14	VSS_250	VSS_343	AA3
U14	VSS_251	VSS_344	G3
K14	VSS_252	VSS_345	AT2
H14	VSS_253	VSS_346	AR2
E14	VSS_254	VSS_347	AP2
AV13	VSS_255	VSS_348	AK2
AR13	VSS_256	VSS_349	AJ2
D25	VSS_257	VSS_350	AD2
AM13	VSS_258	VSS_351	AB2
AL13	VSS_259	VSS_352	Y2
AG13	VSS_260	VSS_353	U2
P13	VSS_261	VSS_354	T2
F13	VSS_262	VSS_355	N2
D13	VSS_263	VSS_356	J2
B13	VSS_264	VSS_357	H2
AY12	VSS_265	VSS_358	F2
AC12	VSS_266	VSS_359	C2
K12	VSS_267	VSS_360	AL1
H12	VSS_268		
E12	VSS_269		
AD11	VSS_270		
AA11	VSS_271		
Y11	VSS_272		

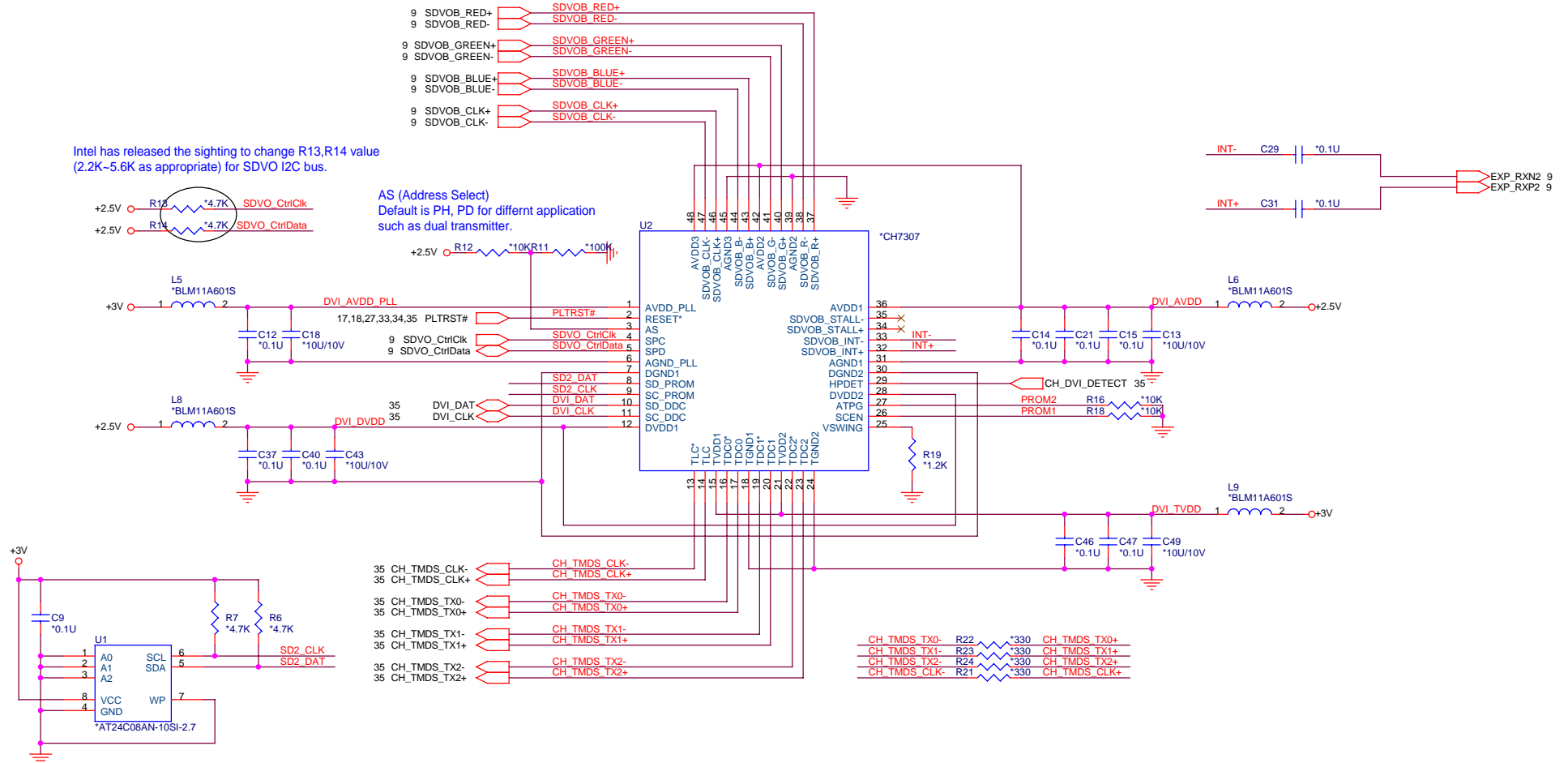
Calistoga



**PROJECT : DW1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	GMCH GND(6 OF 6)	1A
Date:	Tuesday, November 29, 2005	Sheet 12 of 42

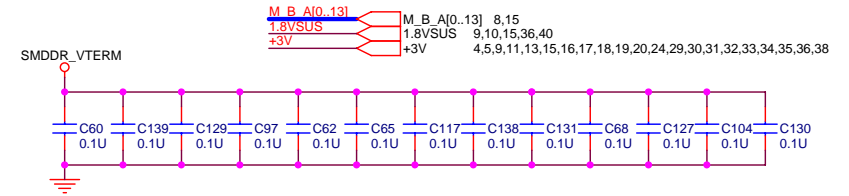
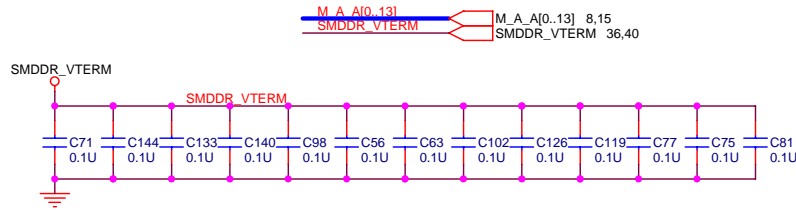
# GMCH SDVO Signal to DVI Signal Bridge



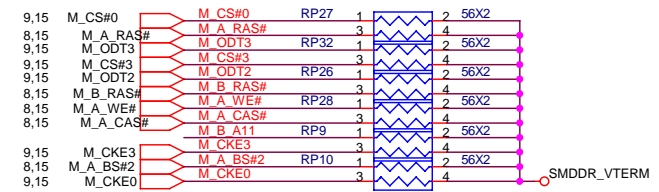
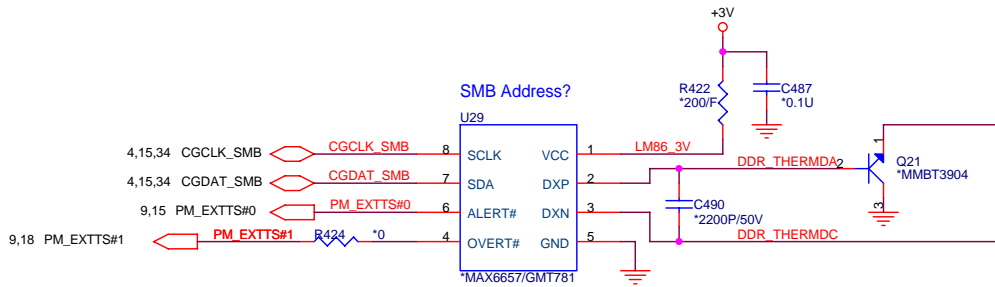
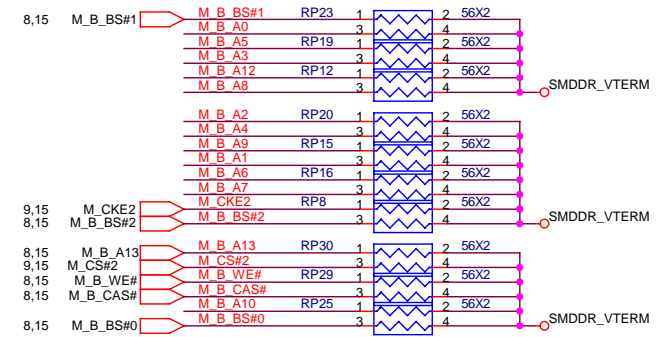
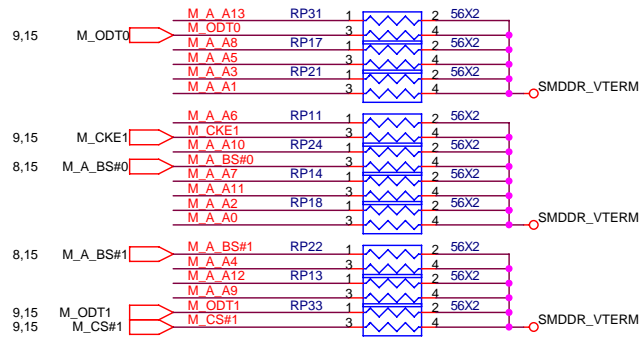
# DDR II DUAL CHANNEL A, B

## DDR II A CHANNEL

## DDR II B CHANNEL



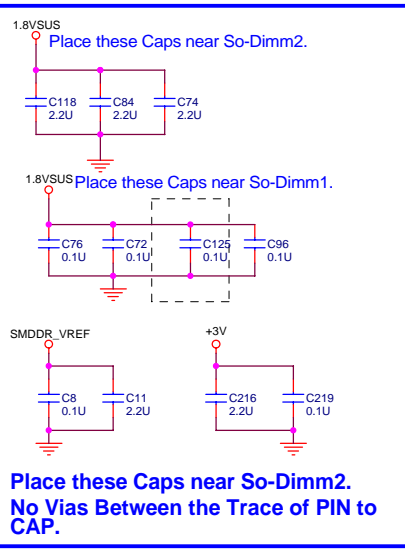
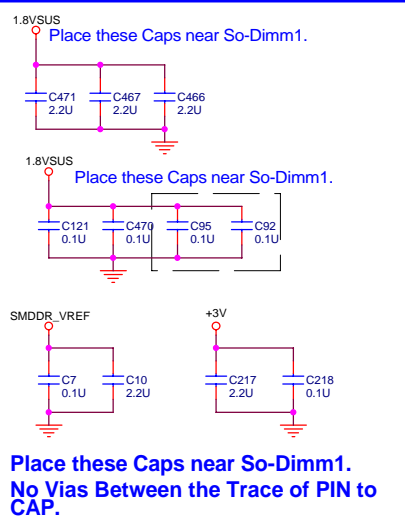
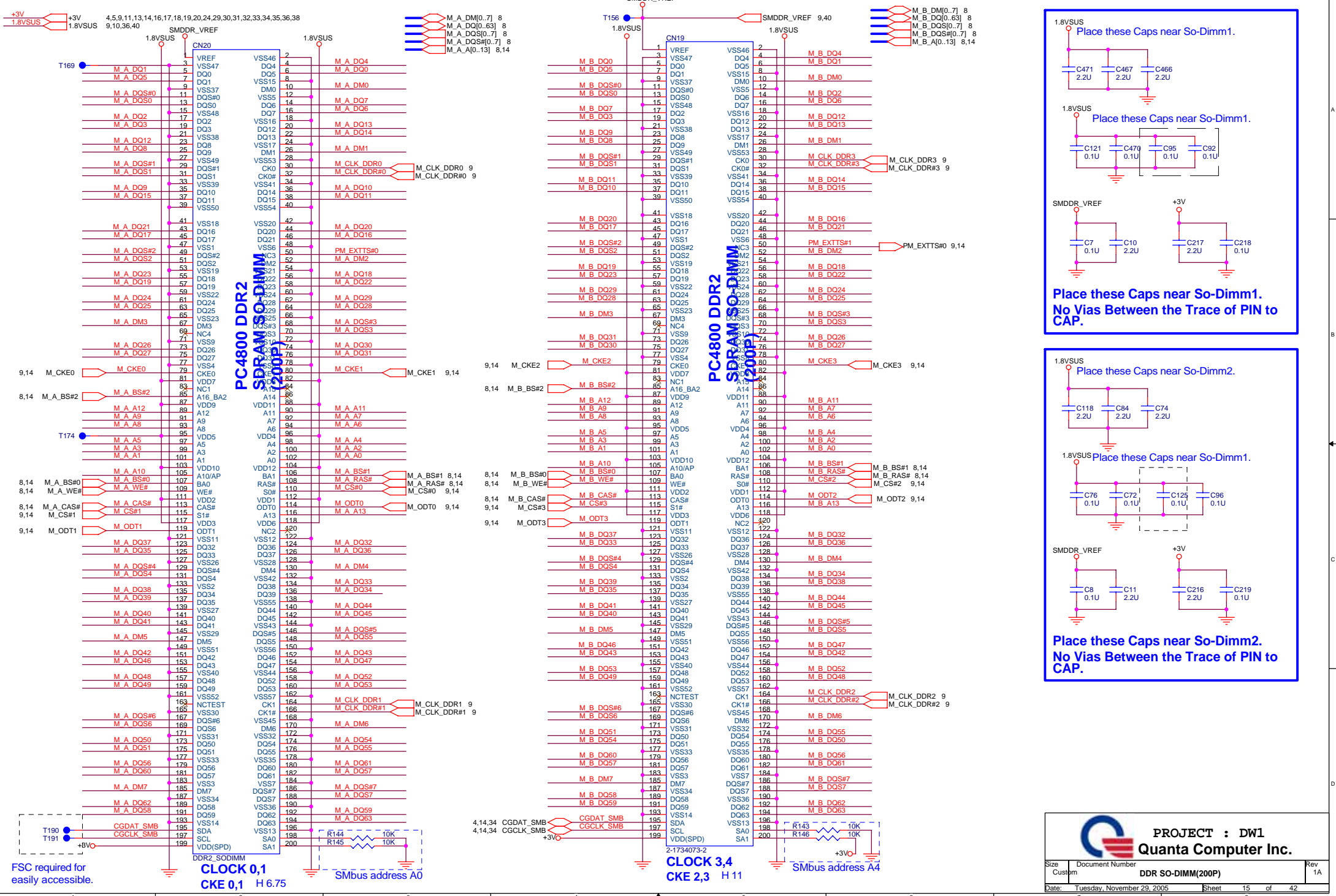
Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR\_VTERM



**PROJECT : CT6**  
**Quanta Computer Inc.**

Size B	Document Number <b>DDR RES. ARRAY</b>	Rev 1A
Date: Tuesday, November 29, 2005		Sheet 14 of 42





**PROJECT : DW1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custpm	DDR SO-DIMM(200P)	1A
Date:	Tuesday, November 29, 2005	Sheet 15 of 42

FSC required for easily accessible.

**CLOCK 0,1**  
**CKE 0,1** H 6.75

SMBus address A0

**CLOCK 3,4**  
**CKE 2,3** H 11

SMBus address A4

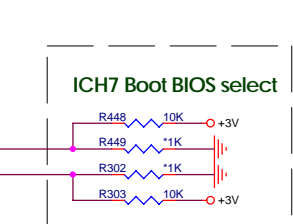
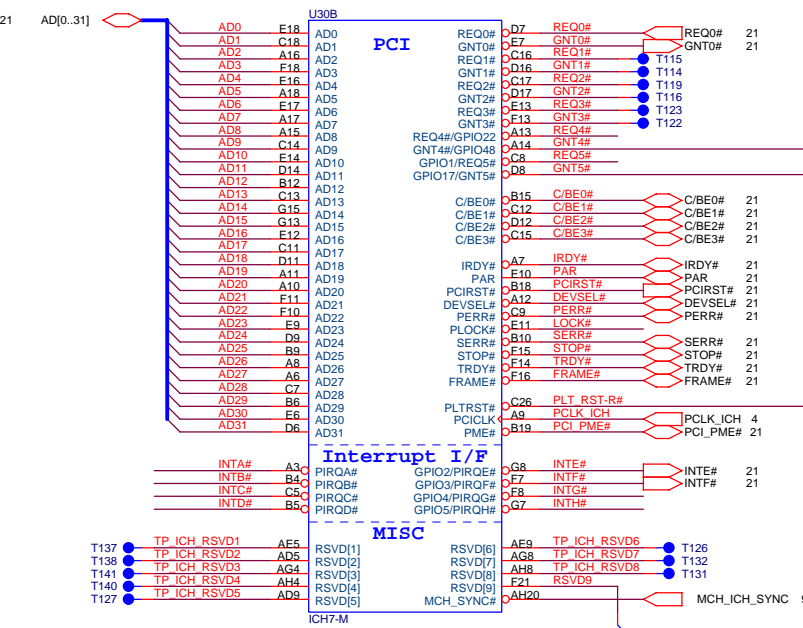
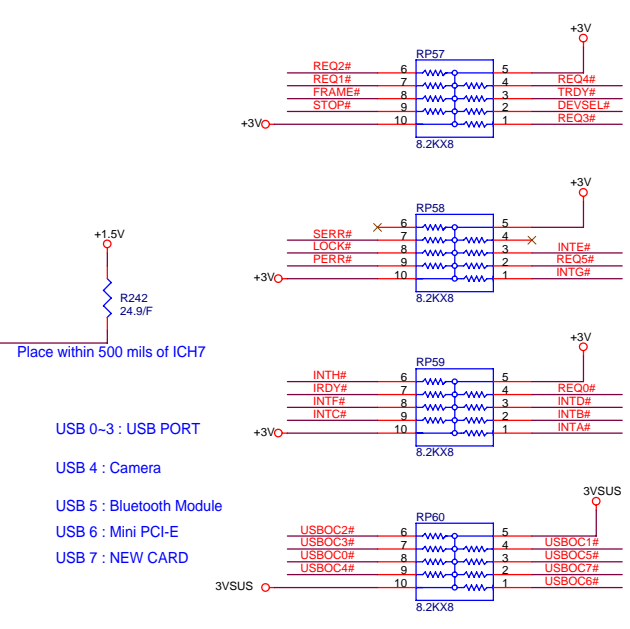
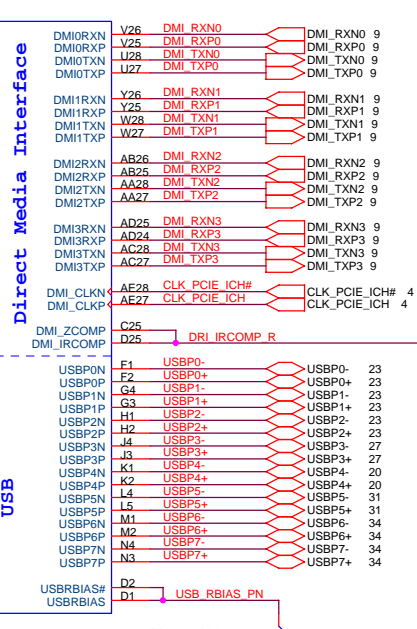
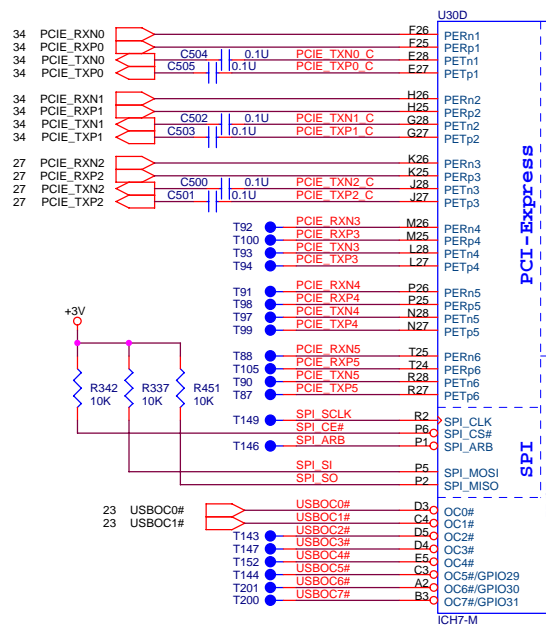




For MINI CARD PCI-E

For EXPRESS CARD (NEW CARD)

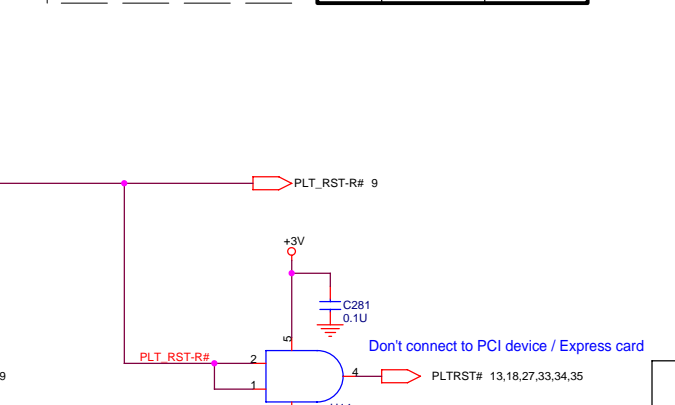
For 82573 GigaLAN



**ICH7 Boot BIOS select**

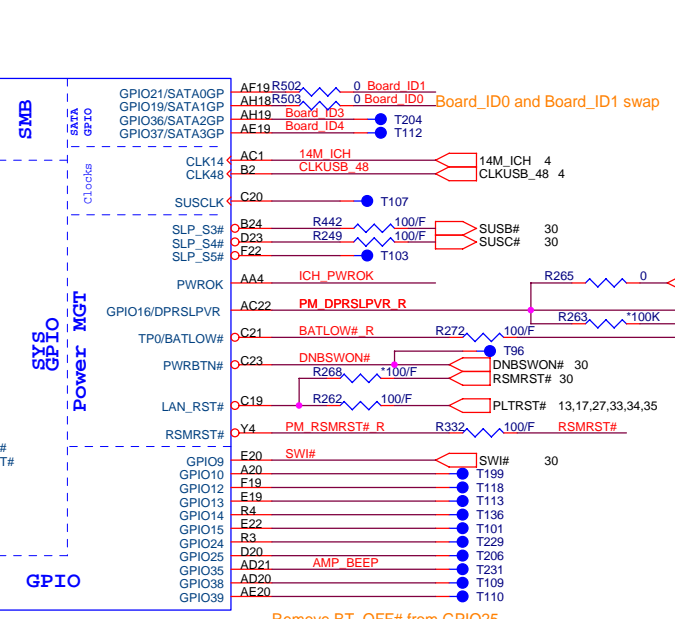
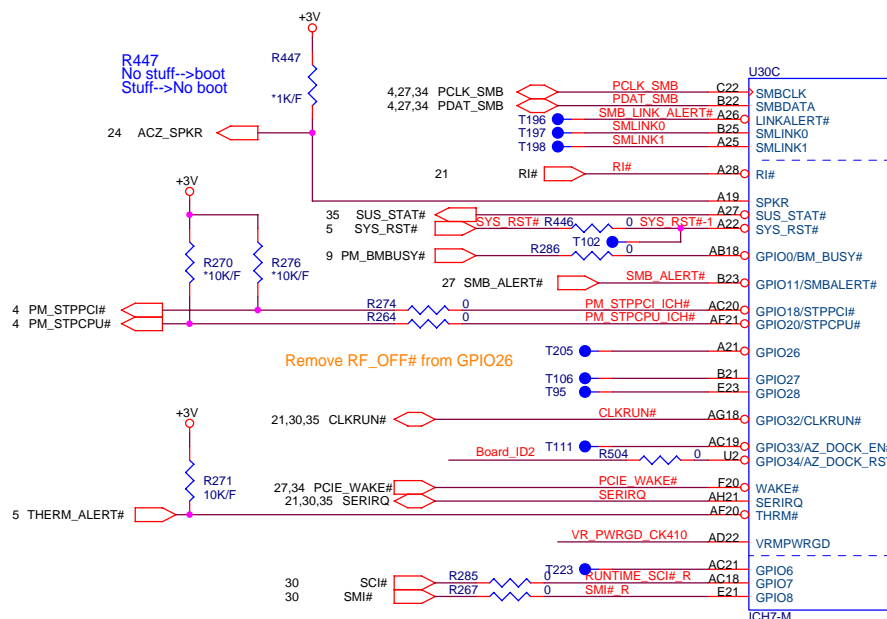
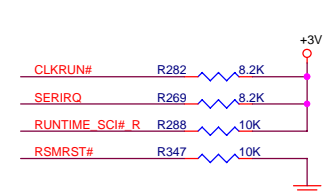
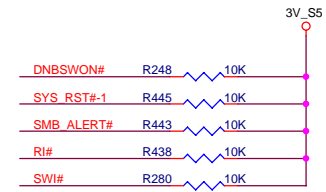
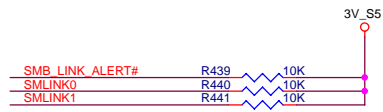
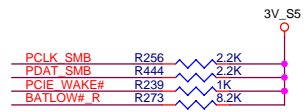
STRAP	GNT4#	GNT5#
LPC	1	1
SPI	0	1

(default)

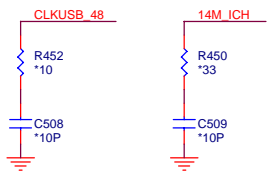


**PROJECT : DW1**  
**Quanta Computer Inc.**

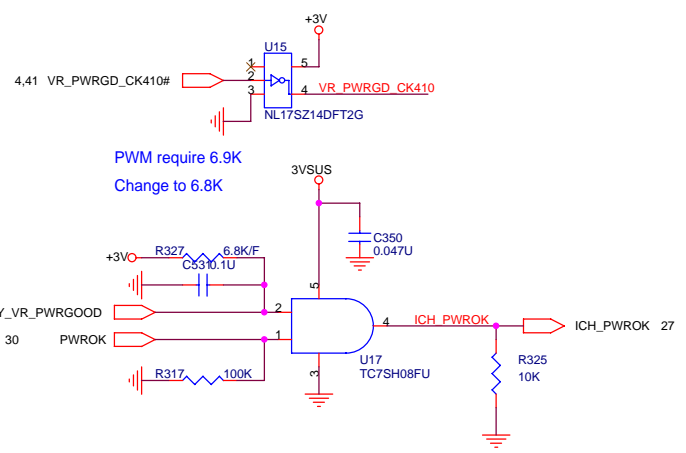
Size	Document Number	Rev
Custom	ICH7-M PCI E (2 OF 4)	1A
Date:	Tuesday, November 29, 2005	Sheet 17 of 42



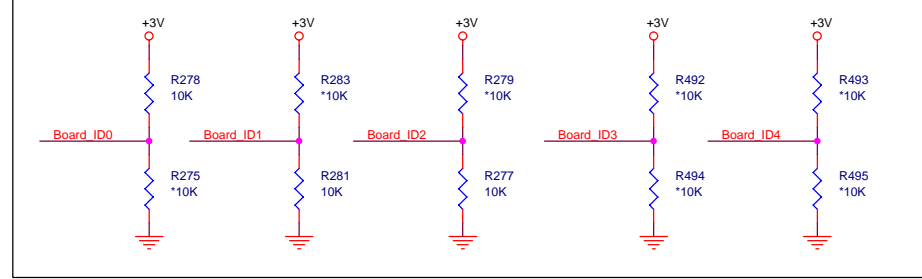
For EMI Perfomance



Lan\_RST#  
 1. If use 82573E (PCI-E), Lan\_RST# tie to RSMRST#.  
 2. If use 82562GX/GZ (LCI), Lan\_RST# tie to PLTRST#.



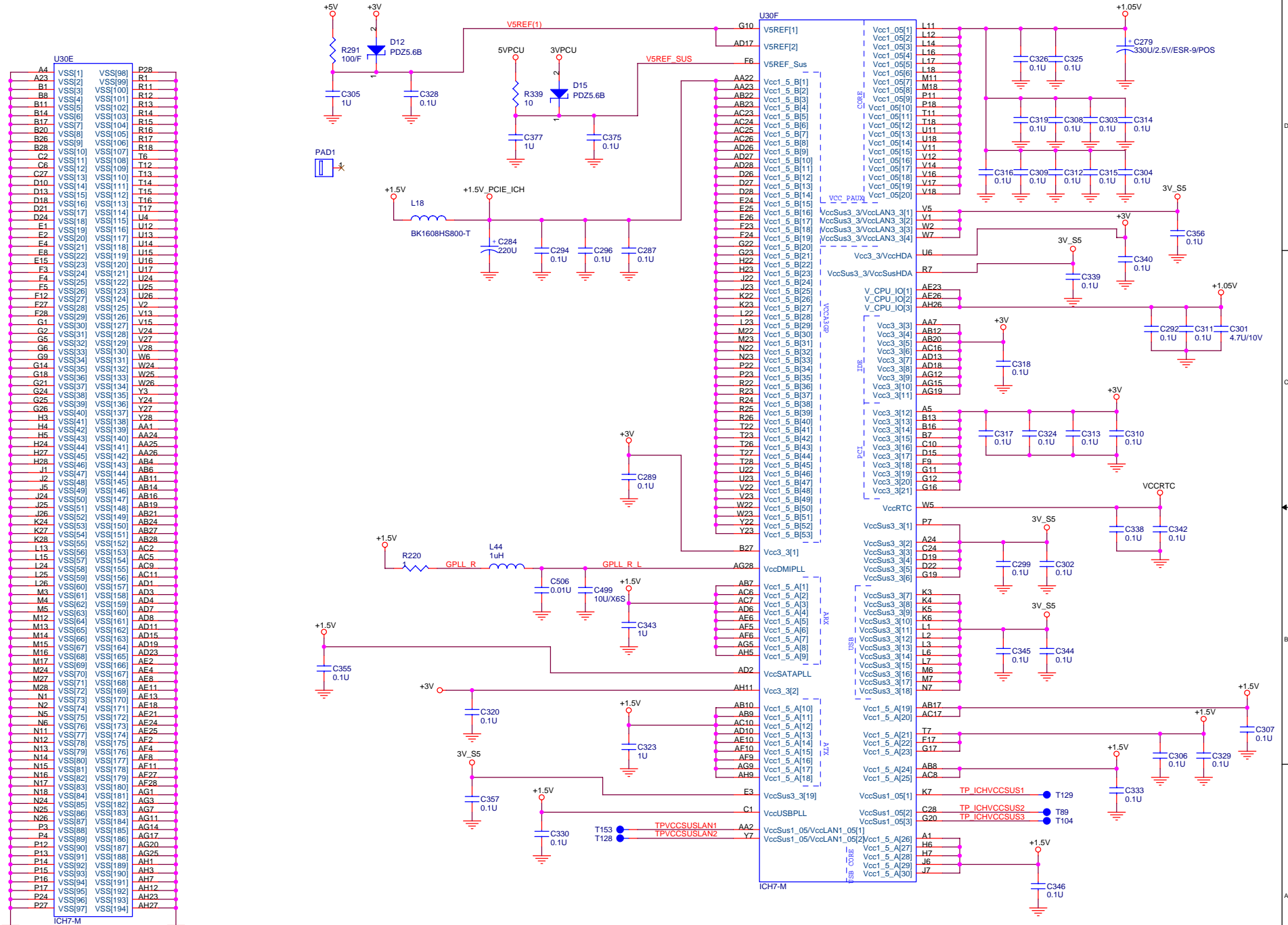
BOARD ID Selection



Board\_ID0 Board\_ID1 Board\_ID2  
 Board\_ID0 30  
 Board\_ID1 30  
 Board\_ID2 30

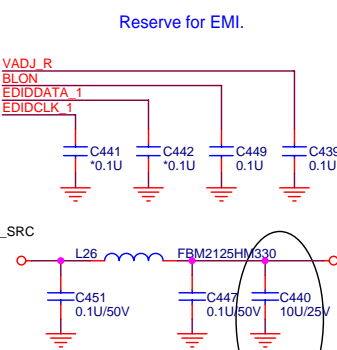
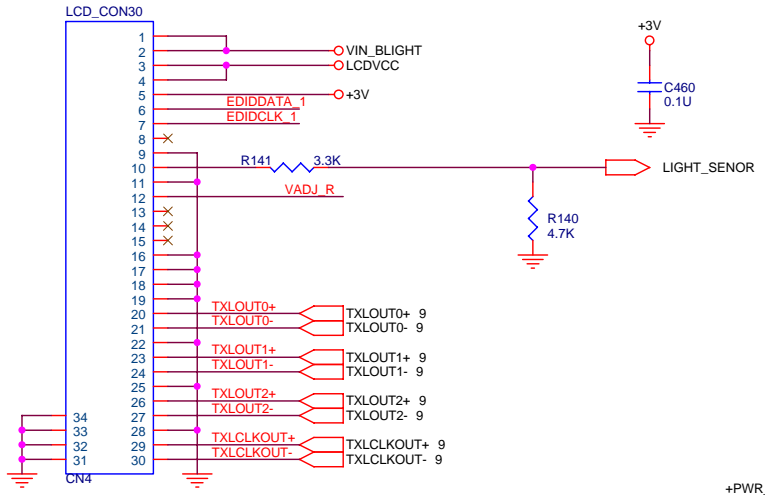
**PROJECT : DW1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custpm	ICH7-M GPIO (3 OF 4)	1A
Date:	Tuesday, November 29, 2005	Sheet 18 of 42

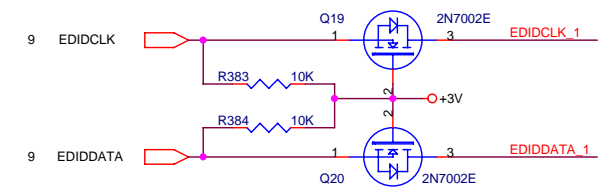
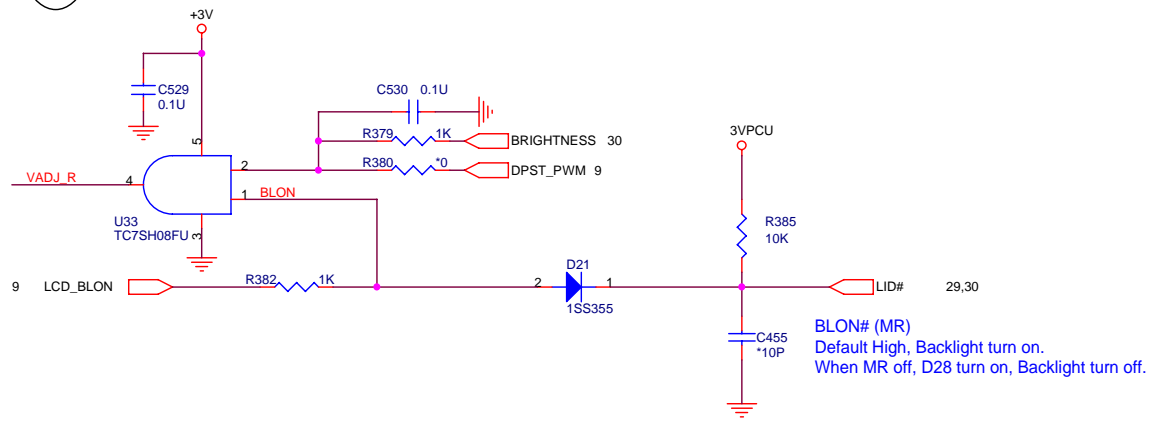
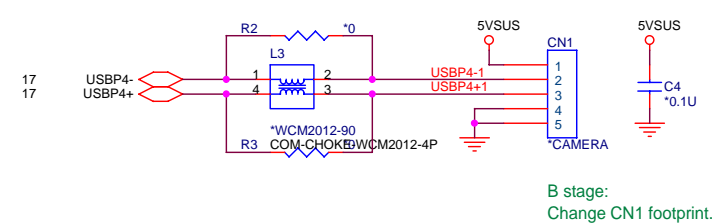
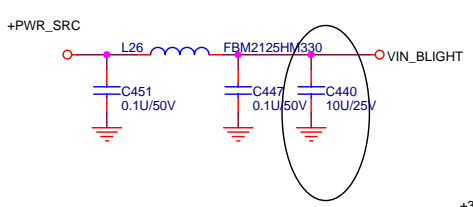
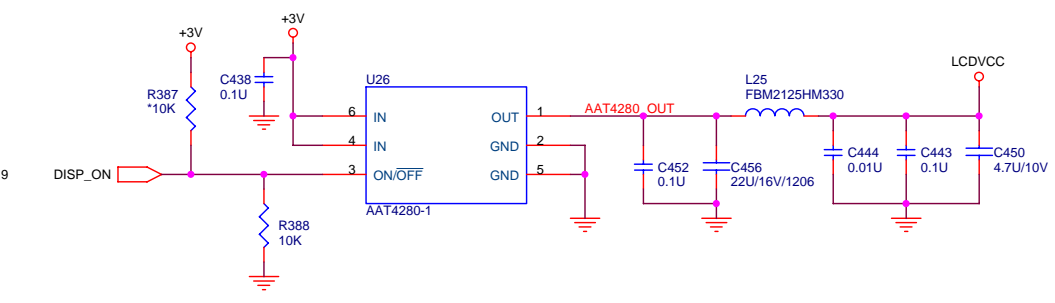


**PROJECT : DW1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	<b>ICH7-M POWER (4 OF 4)</b>	1A
Date:	Tuesday, November 29, 2005	Sheet 19 of 42

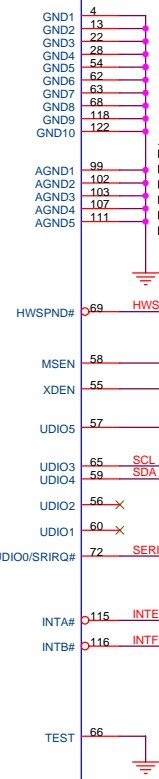
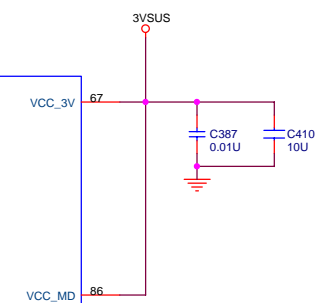
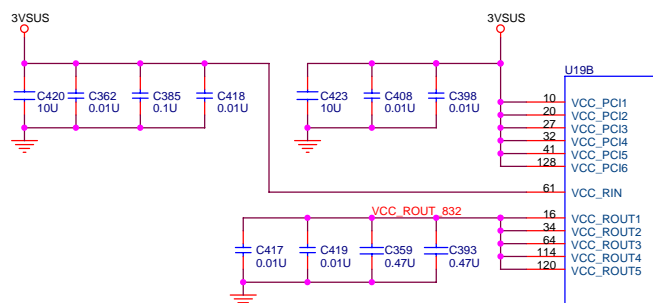


### PANEL VCC CONTROL



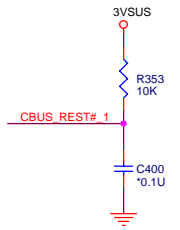
**PROJECT : DW1**  
**Quanta Computer Inc.**

Size B	Document Number	Rev 1A
LCD CONN		
Date: Tuesday, November 29, 2005	Sheet 20 of 42	

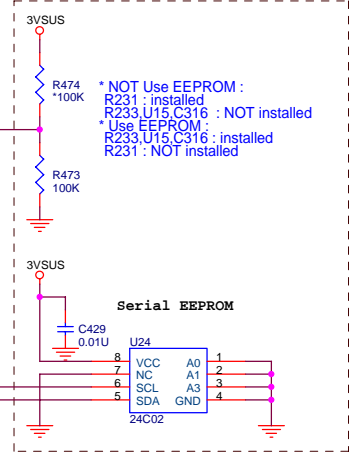
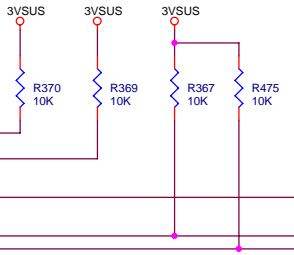


PCI / OTHER

**PowerOnReset for VccCore**  
 When GRESET# is controlled by system, the pull-up resistor(R353) and capacitor(C400) do not need to apply.

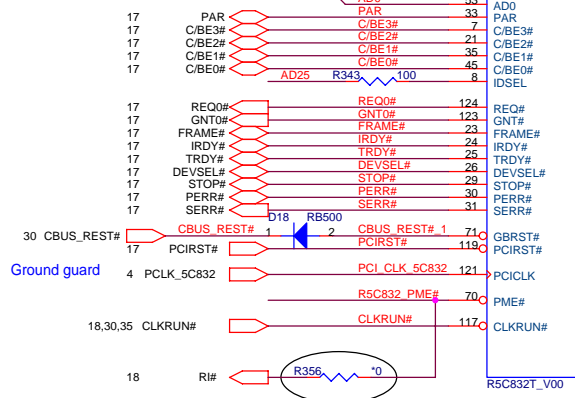


When HWSPND# is controlled by system, the pull-up resistor(R232) dose not need to apply.



\* NOT Use EEPROM :  
 R233 U15 C316 : NOT installed  
 \* Use EEPROM :  
 R233 U15 C316 : installed  
 R231 : NOT installed

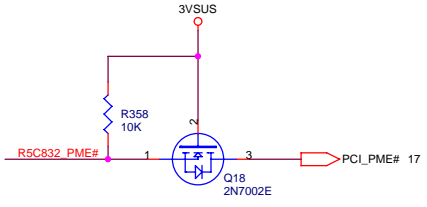
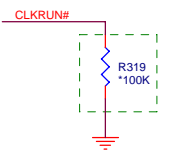
Serial EEPROM

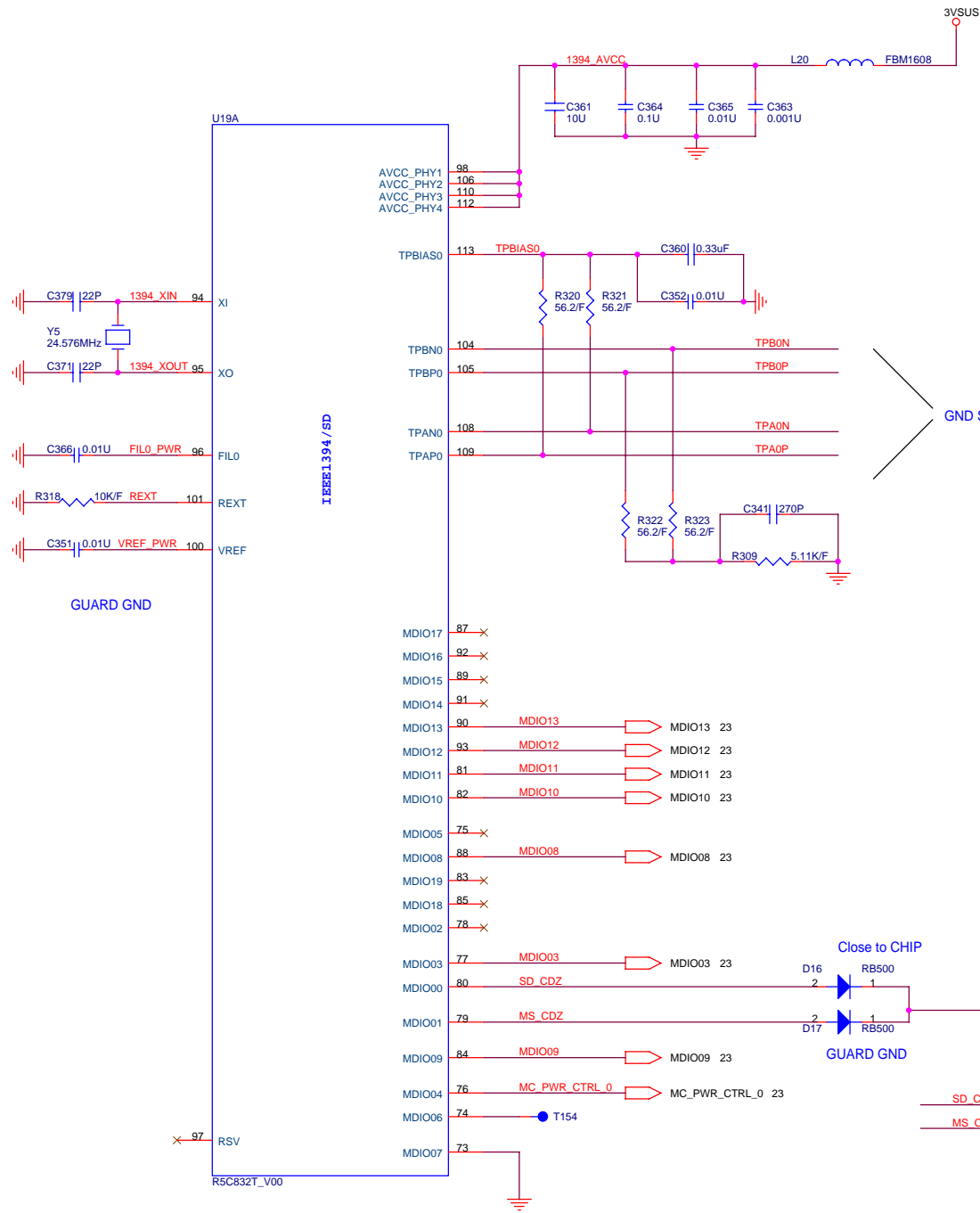


Ground guard

This part needs to populate?

**CoreLogic CLOCKRUN#**  
 When CLKRUN# is controlled by system, the pull-down resistor(R244) dose not need to apply.



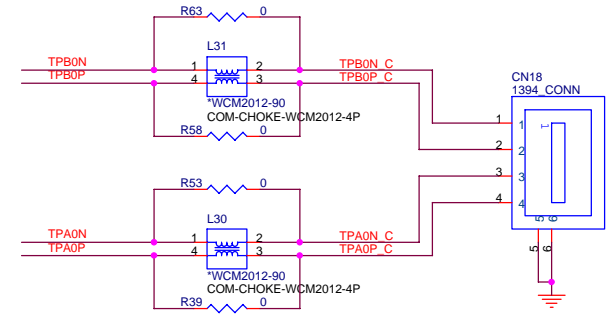


GUARD GND

IEEE1394 / SD

GND Shields

AS CLOSE AS POSSIBLE TO 1394 CONNECTOR.

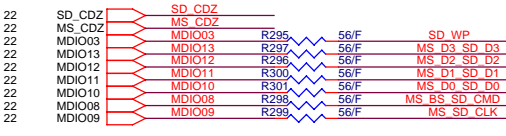


Close to CHIP

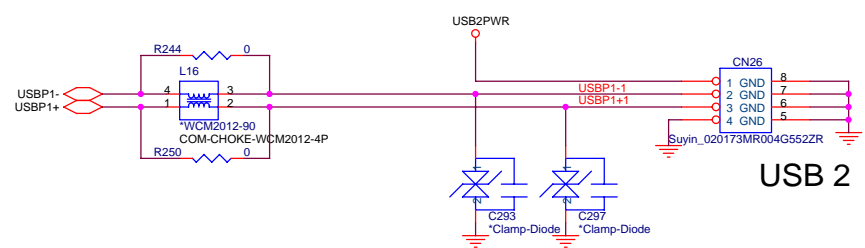
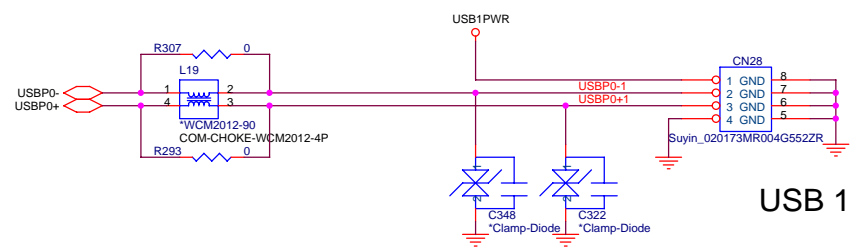
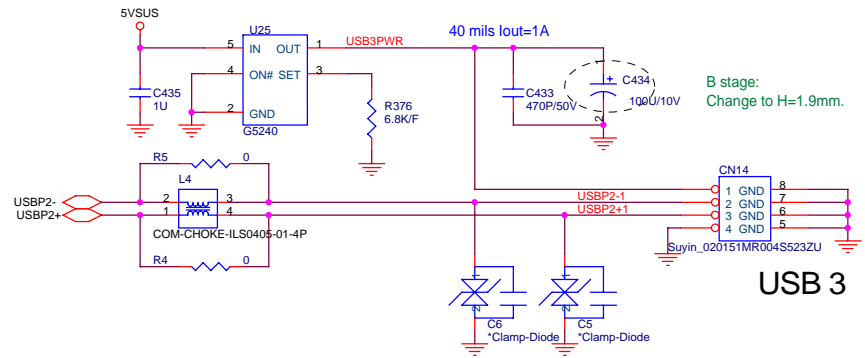
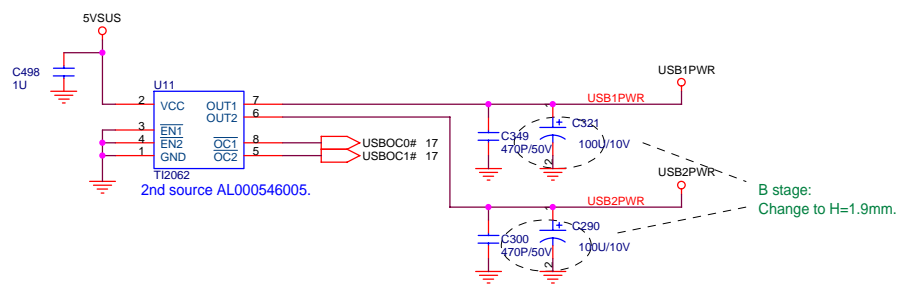
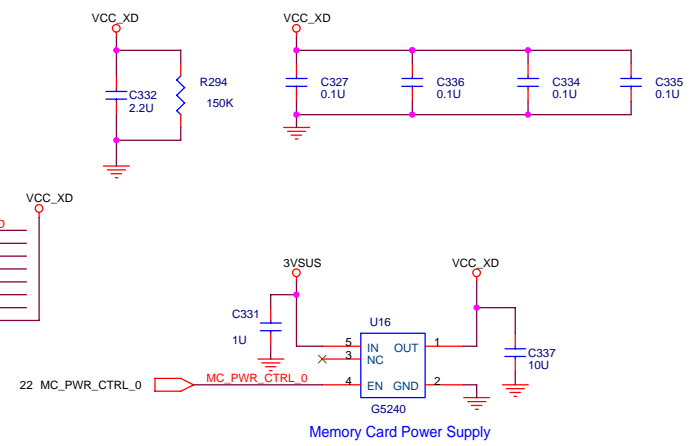
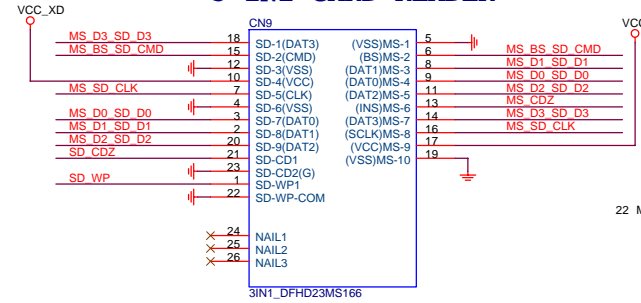
GUARD GND

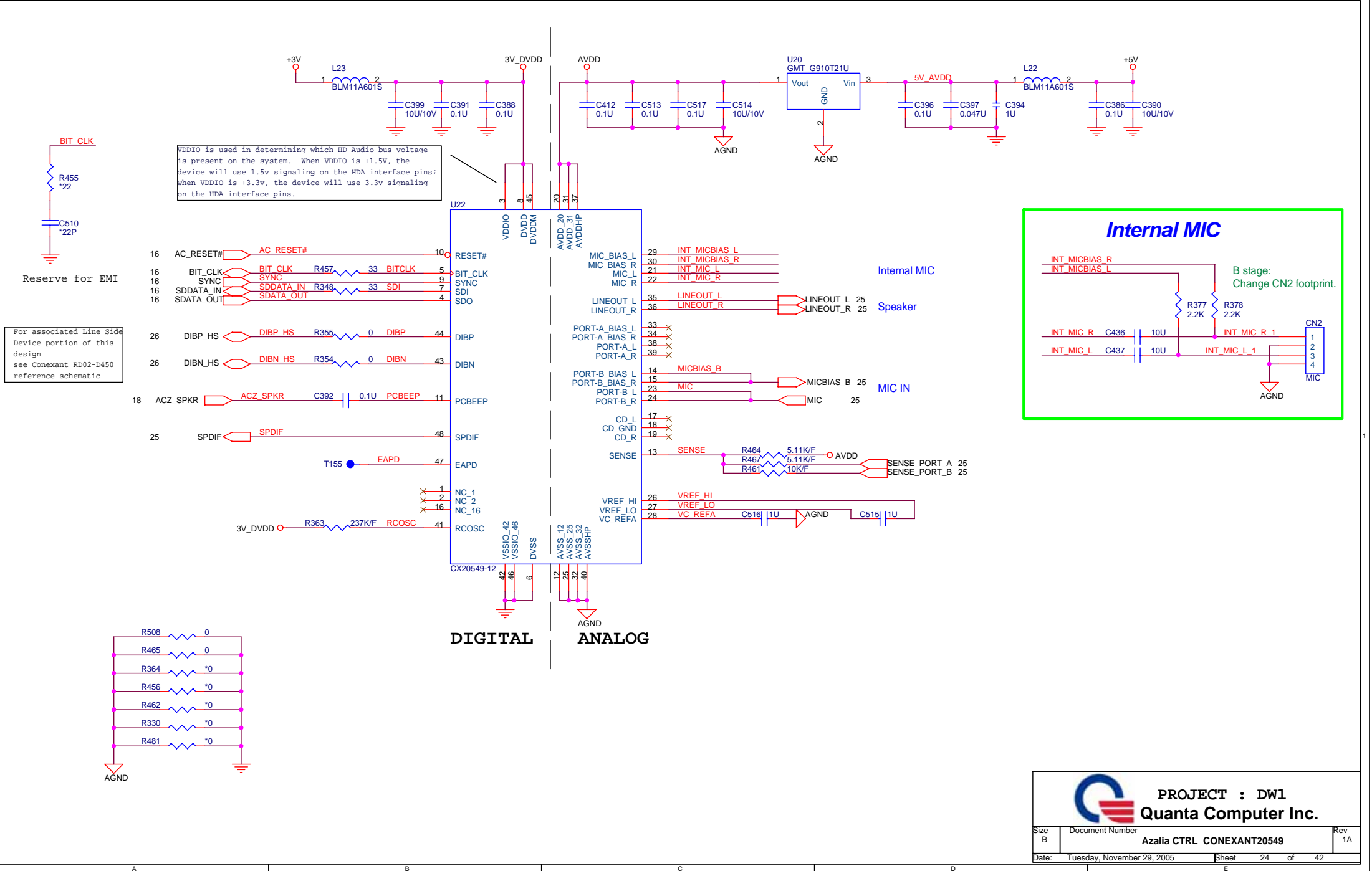
		PROJECT : DW1	
		Quanta Computer Inc.	
Size Custom	Document Number IEEE1394	Rev 1A	
Date: Tuesday, November 29, 2005	Sheet 22	of 42	





### 3 IN1 CARD READER

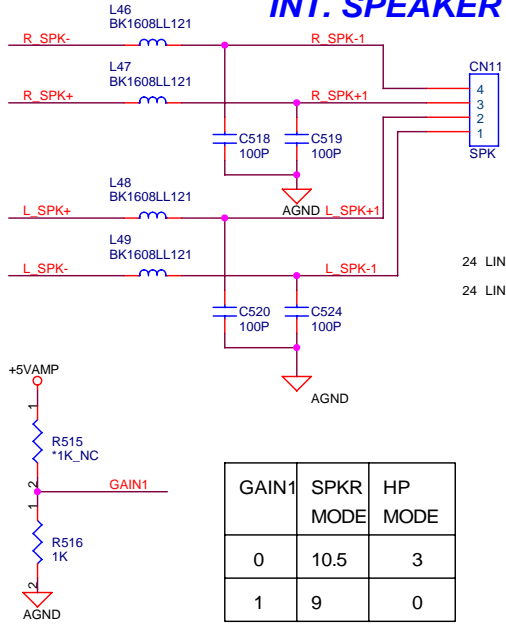




**PROJECT : DW1**  
**Quanta Computer Inc.**

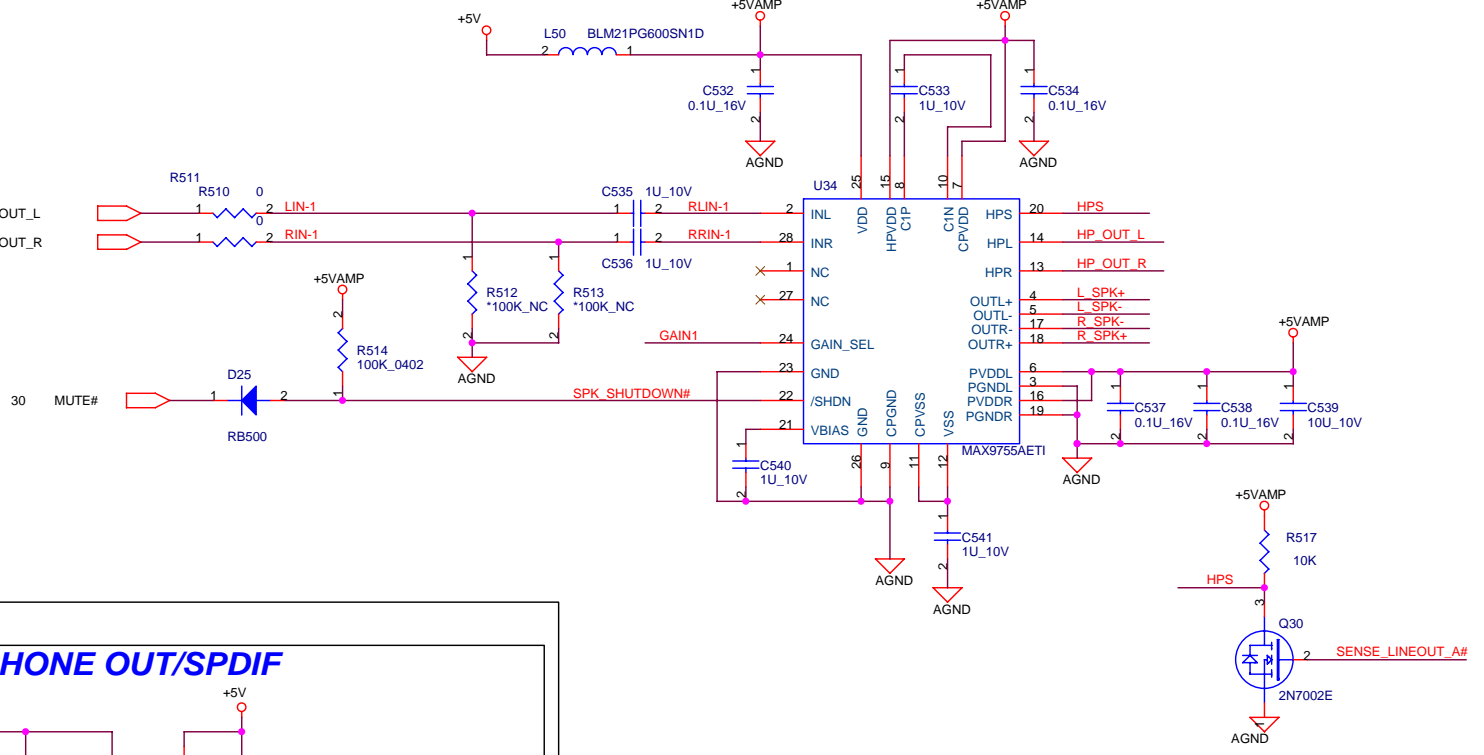
Size B	Document Number <b>Azalia CTRL_CONEXANT20549</b>	Rev 1A
Date: Tuesday, November 29, 2005		Sheet 24 of 42

### INT. SPEAKER

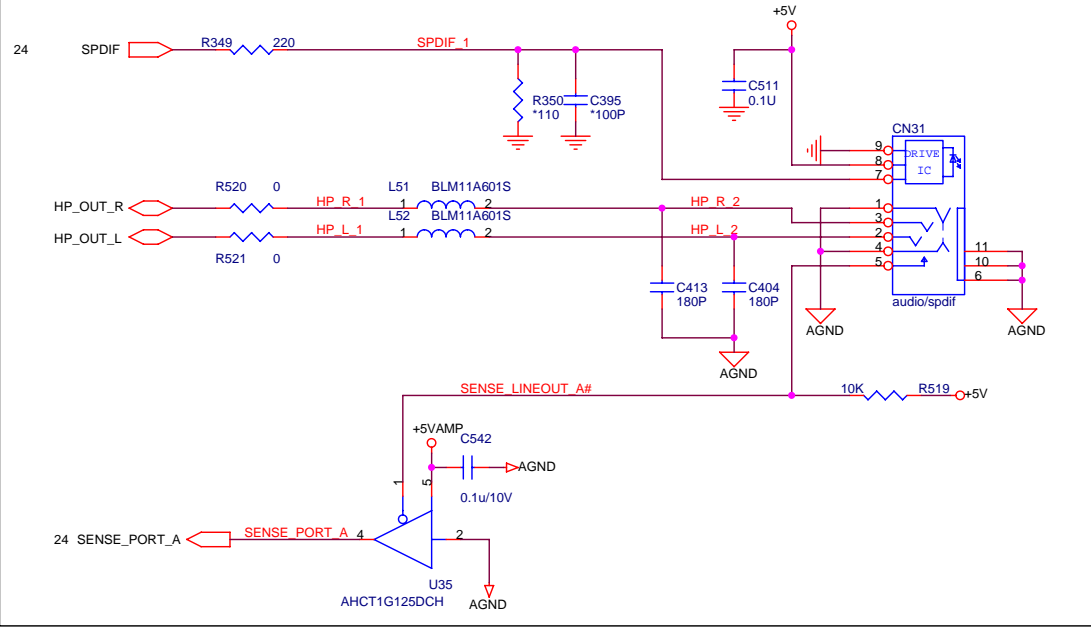


GAIN1	SPKR MODE	HP MODE
0	10.5	3
1	9	0

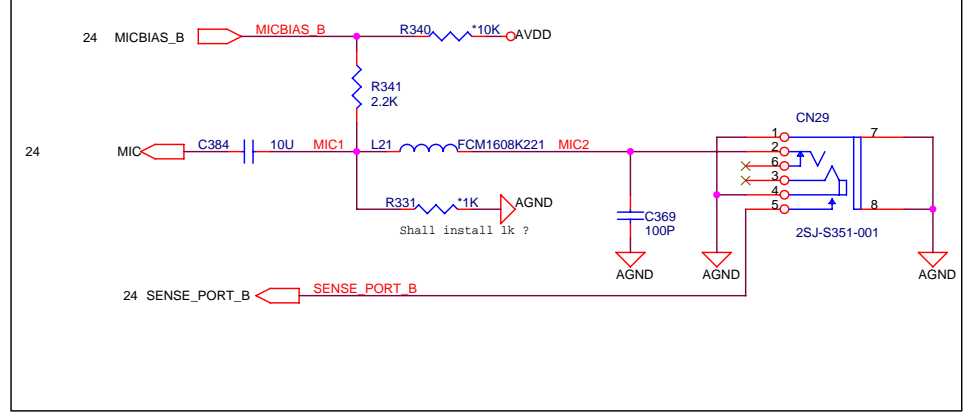
### Audio amplifier



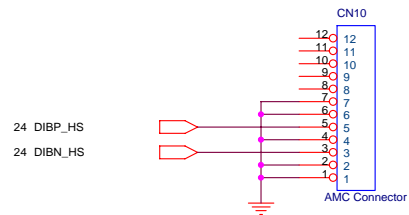
### HEADPHONE OUT/SPDIF



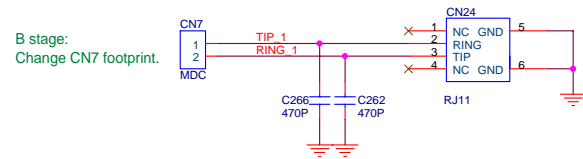
### MIC JACK



**PROJECT : DW1**  
**Quanta Computer Inc.**

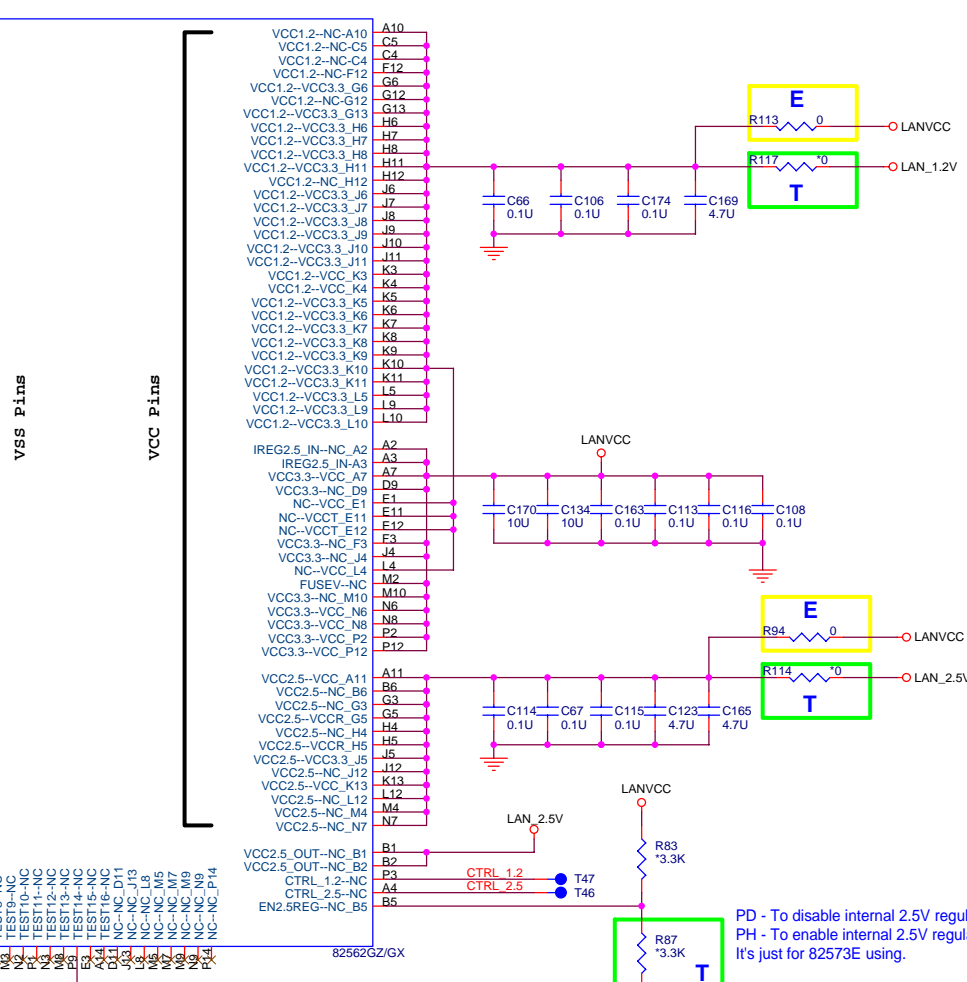
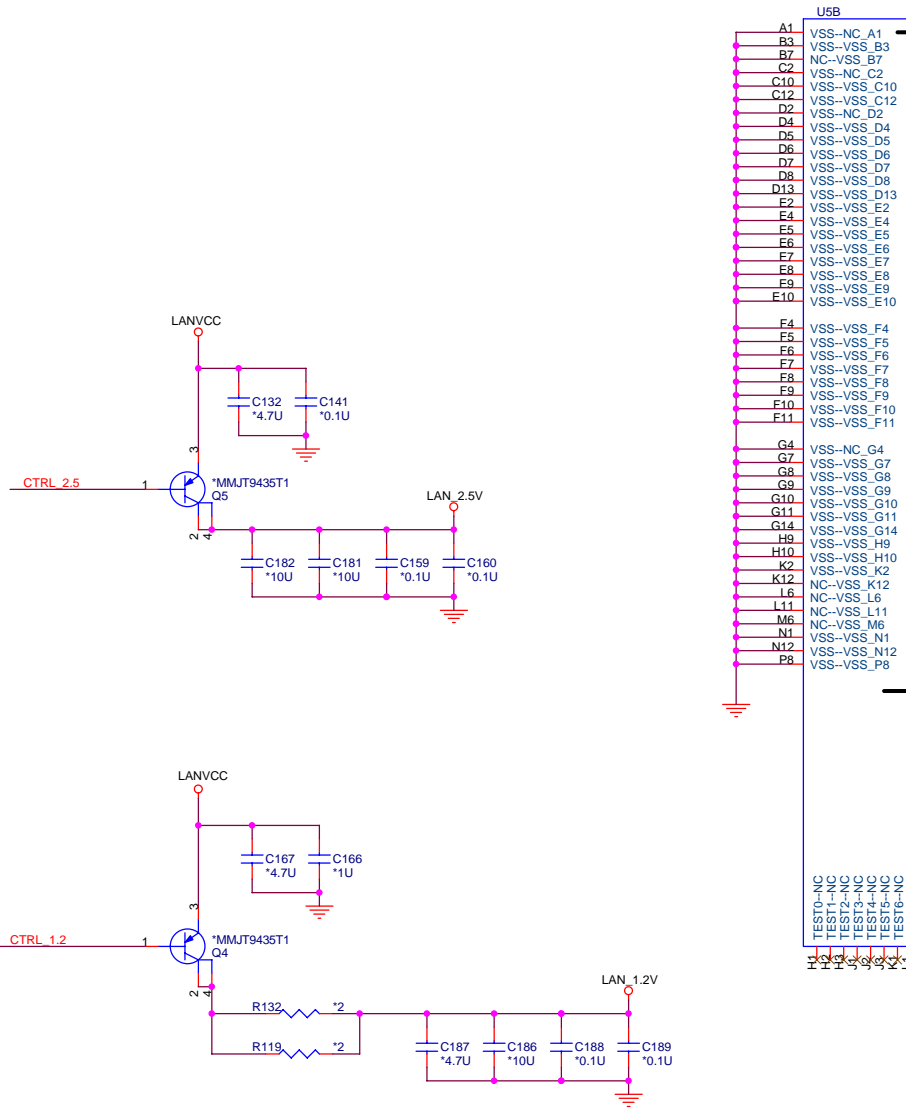


**RJ11 CONNECTOR**



B stage:  
Change CN7 footprint.





- VSS Pins**
- A1 VSS--NC\_A1
  - B3 VSS--VSS\_B3
  - B7 NC--VSS\_B7
  - C2 VSS--NC\_C2
  - C10 VSS--VSS\_C10
  - C12 VSS--VSS\_C12
  - D2 VSS--NC\_D2
  - D4 VSS--VSS\_D4
  - D5 VSS--VSS\_D5
  - D6 VSS--VSS\_D6
  - D7 VSS--VSS\_D7
  - D8 VSS--VSS\_D8
  - D13 VSS--VSS\_D13
  - E2 VSS--VSS\_E2
  - E4 VSS--VSS\_E4
  - E5 VSS--VSS\_E5
  - E6 VSS--VSS\_E6
  - E7 VSS--VSS\_E7
  - E8 VSS--VSS\_E8
  - E9 VSS--VSS\_E9
  - F10 VSS--VSS\_F10
  - F11 VSS--VSS\_F11
  - F4 VSS--VSS\_F4
  - F5 VSS--VSS\_F5
  - F6 VSS--VSS\_F6
  - F7 VSS--VSS\_F7
  - F8 VSS--VSS\_F8
  - F9 VSS--VSS\_F9
  - G4 VSS--NC\_G4
  - G7 VSS--VSS\_G7
  - G8 VSS--VSS\_G8
  - G9 VSS--VSS\_G9
  - G10 VSS--VSS\_G10
  - G11 VSS--VSS\_G11
  - G14 VSS--VSS\_G14
  - H8 VSS--VSS\_H8
  - H9 VSS--VSS\_H9
  - H10 VSS--VSS\_H10
  - K2 NC--VSS\_K2
  - K12 NC--VSS\_K12
  - L6 NC--VSS\_L6
  - L11 NC--VSS\_L11
  - M6 NC--VSS\_M6
  - N1 VSS--VSS\_N1
  - N12 VSS--VSS\_N12
  - P8 VSS--VSS\_P8

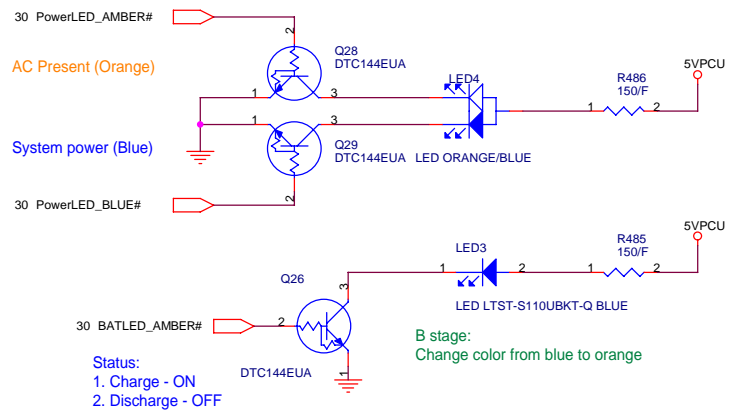
- VCC Pins**
- A10 VCC1.2--NC\_A10
  - C5 VCC1.2--NC\_C5
  - C4 VCC1.2--NC\_C4
  - F12 VCC1.2--NC\_F12
  - G6 VCC1.2--VCC3.3\_G6
  - G12 VCC1.2--NC\_G12
  - G13 VCC1.2--NC\_G13
  - H6 VCC1.2--VCC3.3\_H6
  - H7 VCC1.2--VCC3.3\_H7
  - H8 VCC1.2--VCC3.3\_H8
  - H11 VCC1.2--VCC3.3\_H11
  - H12 VCC1.2--NC\_H12
  - J6 VCC1.2--VCC3.3\_J6
  - J7 VCC1.2--VCC3.3\_J7
  - J8 VCC1.2--VCC3.3\_J8
  - J9 VCC1.2--VCC3.3\_J9
  - J10 VCC1.2--VCC3.3\_J10
  - J11 VCC1.2--VCC3.3\_J11
  - K3 VCC1.2--VCC\_K3
  - K4 VCC1.2--VCC\_K4
  - K5 VCC1.2--VCC3.3\_K5
  - K6 VCC1.2--VCC3.3\_K6
  - K7 VCC1.2--VCC3.3\_K7
  - K8 VCC1.2--VCC3.3\_K8
  - K9 VCC1.2--VCC3.3\_K9
  - K10 VCC1.2--VCC3.3\_K10
  - K11 VCC1.2--VCC3.3\_K11
  - L5 VCC1.2--VCC3.3\_L5
  - L9 VCC1.2--VCC3.3\_L9
  - L10 VCC1.2--VCC3.3\_L10
  - A2 IREG2.5\_IN--NC\_A2
  - A3 IREG2.5\_IN--A3
  - A7 VCC3.3--VCC\_A7
  - D9 VCC3.3--NC\_D9
  - E1 NC--VCC\_E1
  - E11 NC--VCC\_T\_E11
  - E12 NC--VCC\_T\_E12
  - F3 VCC3.3--NC\_F3
  - L4 VCC3.3--NC\_L4
  - L4 NC--VCC\_L4
  - M2 FUSEV--NC\_M10
  - M10 VCC3.3--VCC\_M10
  - N6 VCC3.3--VCC\_N6
  - N8 VCC3.3--VCC\_N8
  - P2 VCC3.3--VCC\_P2
  - P12 VCC3.3--VCC\_P12
  - A11 VCC2.5--VCC\_A11
  - B6 VCC2.5--NC\_B6
  - G3 VCC2.5--NC\_G3
  - G5 VCC2.5--VCCR\_G5
  - H4 VCC2.5--NC\_H4
  - H5 VCC2.5--VCCR\_H5
  - J5 VCC2.5--VCC3.3\_J5
  - J12 VCC2.5--NC\_J12
  - K13 VCC2.5--VCC\_K13
  - L12 VCC2.5--NC\_L12
  - M4 VCC2.5--NC\_M4
  - N7 VCC2.5--NC\_N7
  - B1 VCC2.5\_OUT--NC\_B1
  - B2 VCC2.5\_OUT--NC\_B2
  - P3 CTRL\_1.2--NC\_P3
  - A4 CTRL\_1.2--NC\_A4
  - A5 CTRL\_2.5--NC\_A5
  - B5 EN2.5REG--NC\_B5

To enable clocks for Tekoa-M, stuff R1, Unstuff R2

PD - To disable internal 2.5V regulator.  
PH - To enable internal 2.5V regulator.  
It's just for 82573E using.

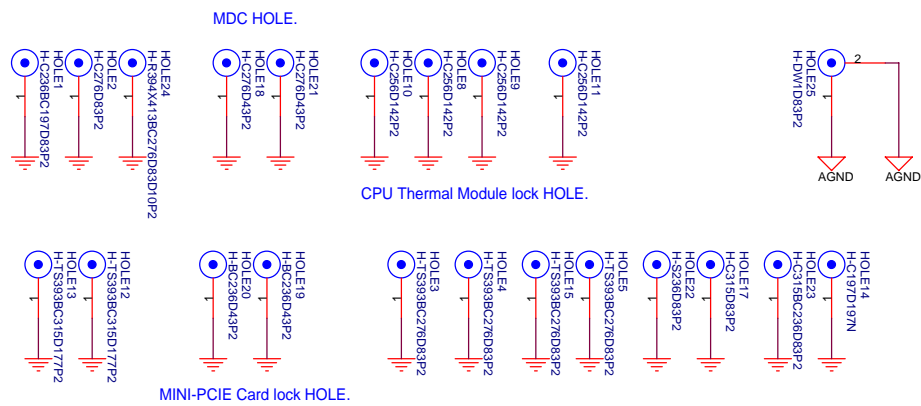
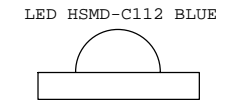
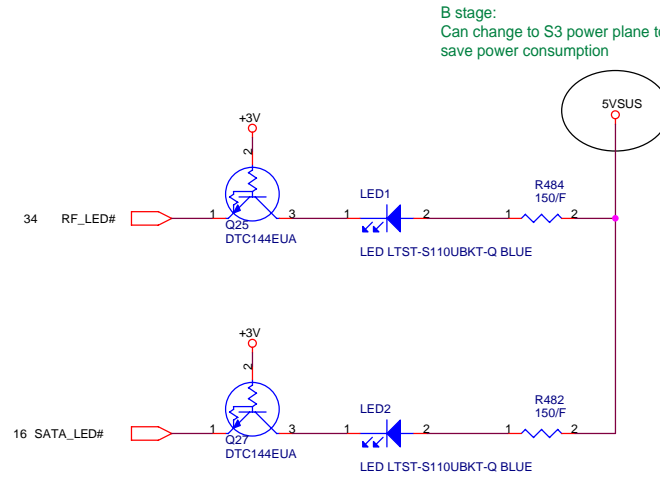
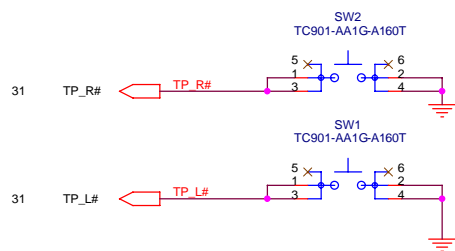
**PROJECT : DW1**  
**Quanta Computer Inc.**

Size Custom	Document Number	LAN Power	Rev 1A
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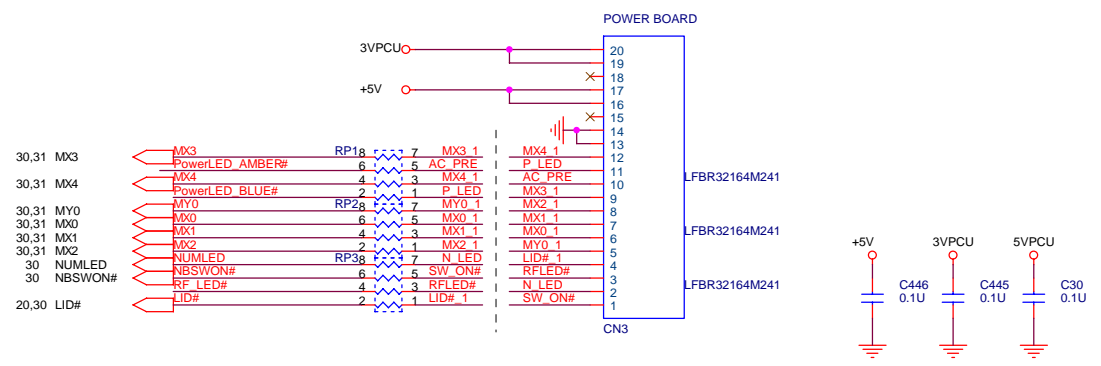


B stage:  
Change color from blue to orange

Status:  
1. Charge - ON  
2. Discharge - OFF



Need to apply Nut part number for Thermal, MDC and Mini-card module.

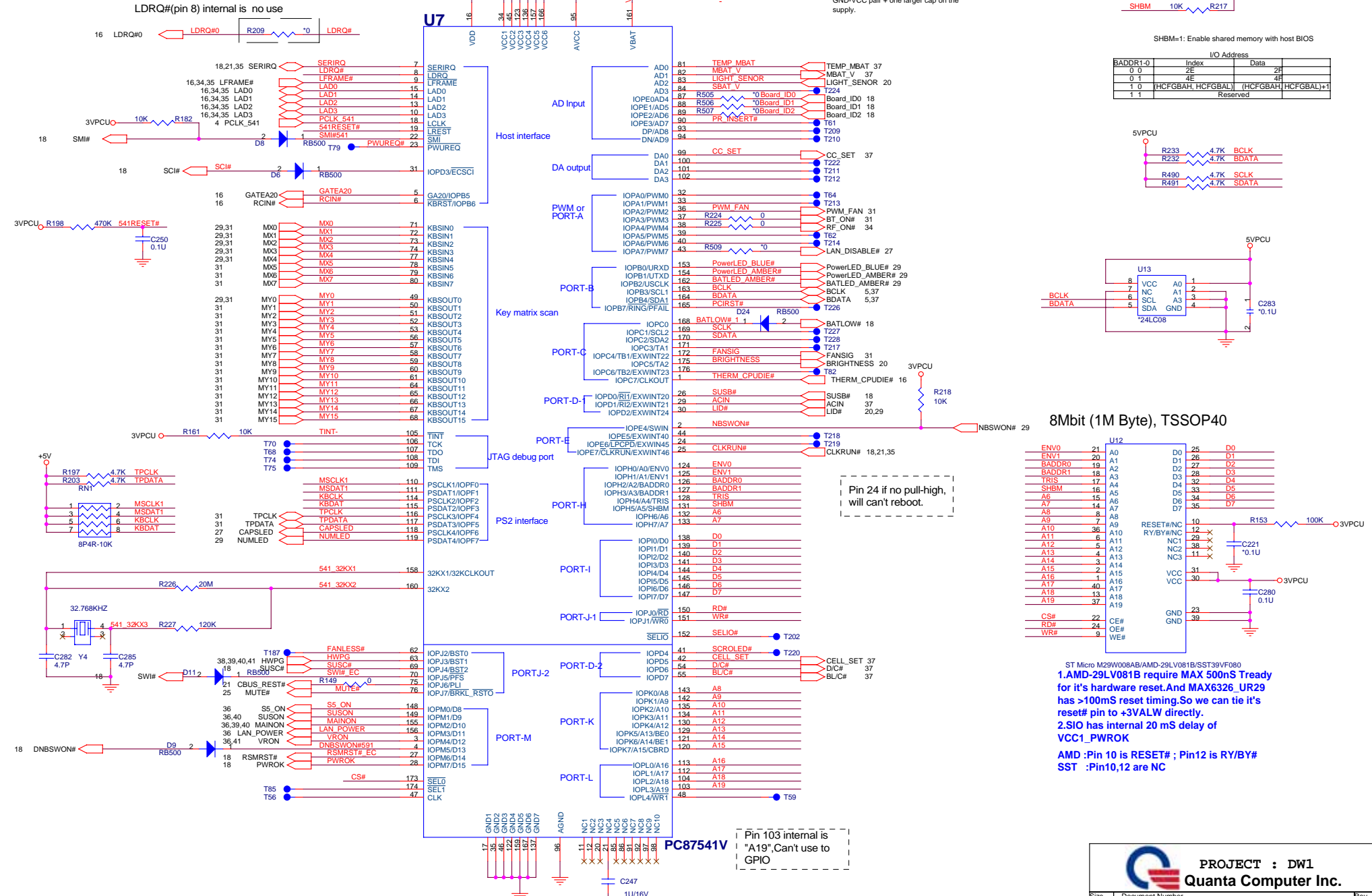


**PROJECT : DW1**  
**Quanta Computer Inc.**

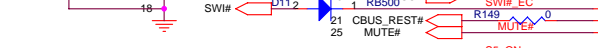
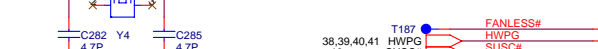
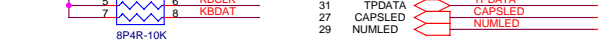
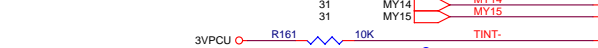
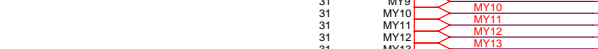
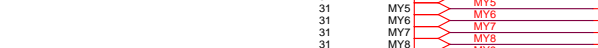
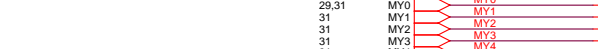
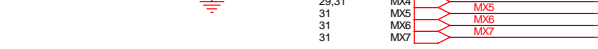
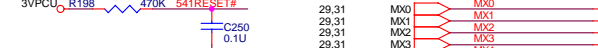
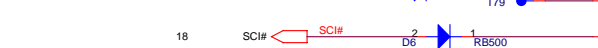
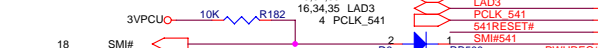
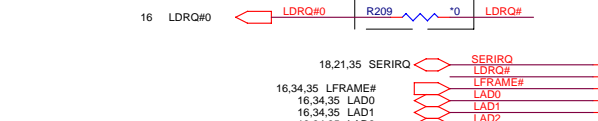
Size	Document Number	Rev
Custom	LED, Hole, TP SW, SW/B	1A
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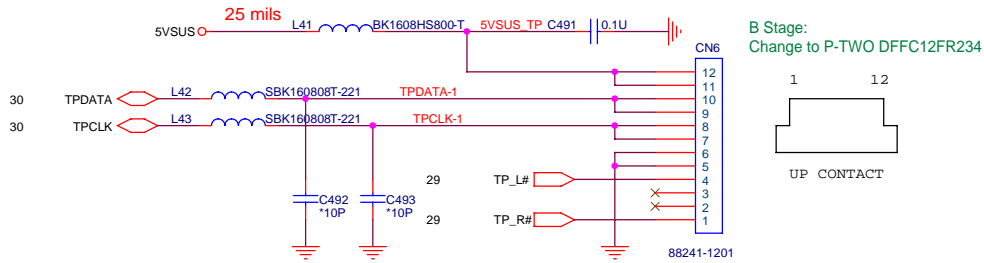
KBC-NS87541L



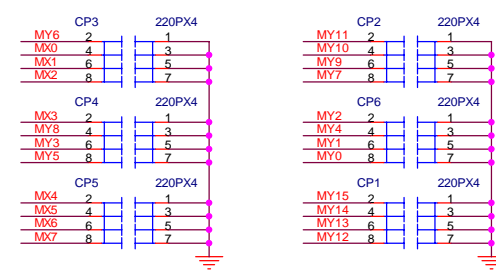
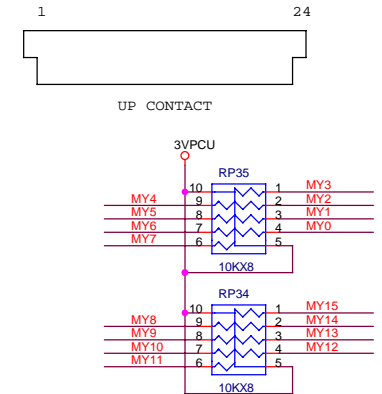
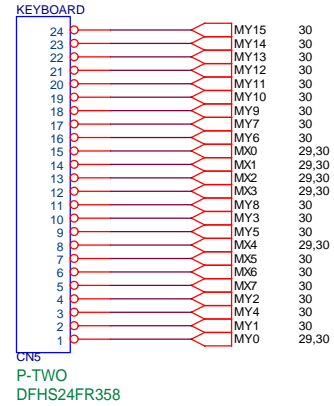
LDRQ#(pin 8) internal is no use



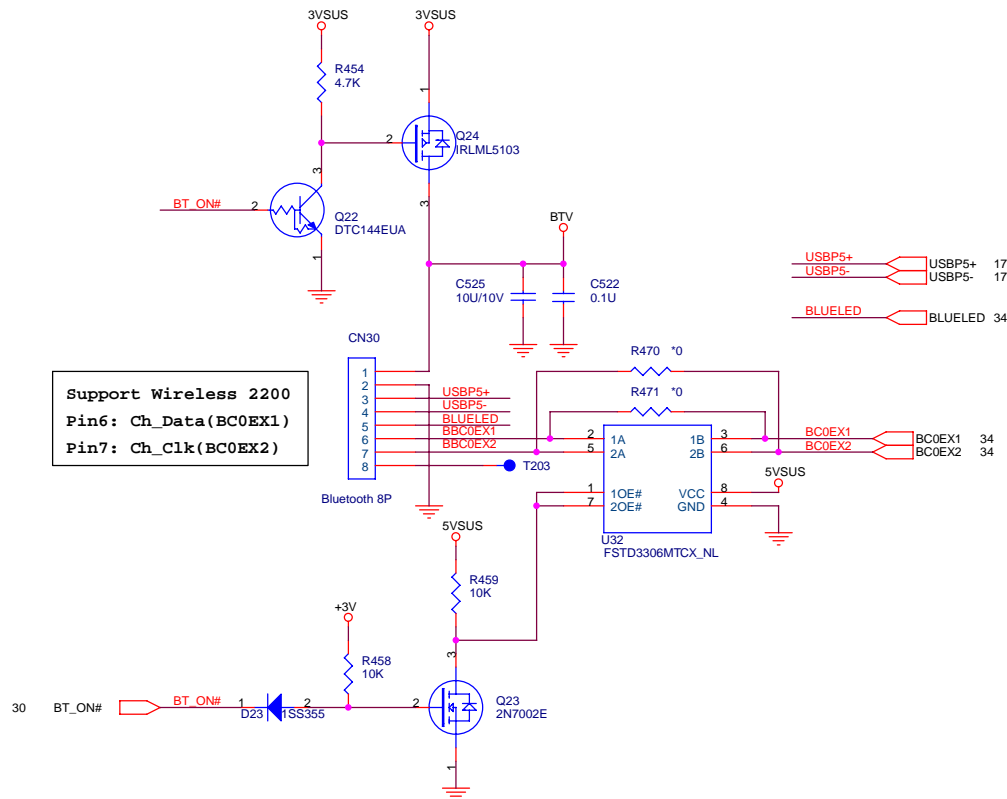
# TOUCH PAD CONNECTOR



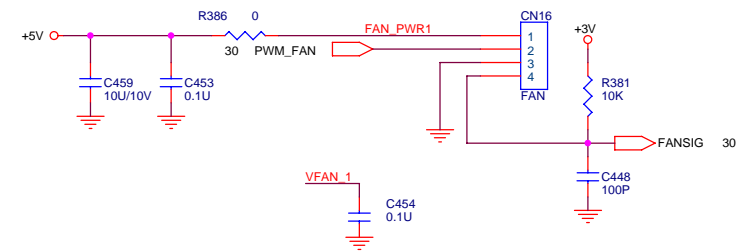
# KEYBOARD CONNECTOR

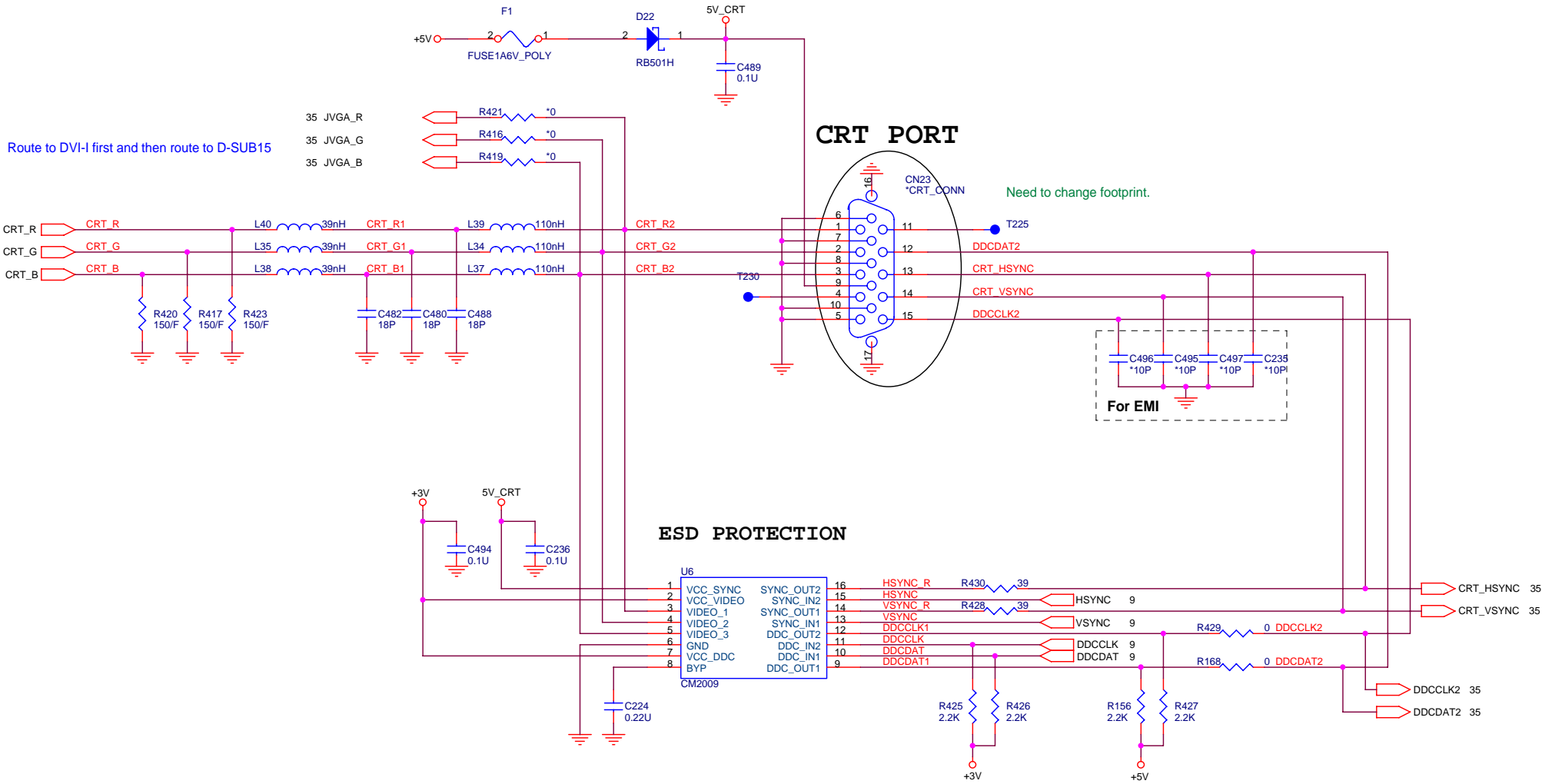



# BLUETOOTH



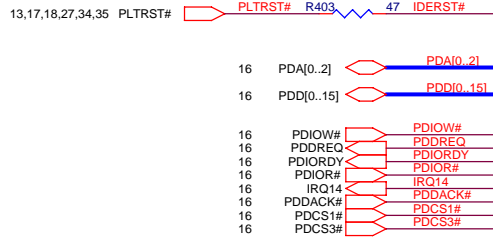
# FAN CONTROL





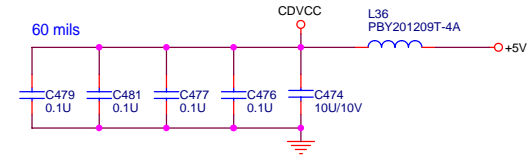
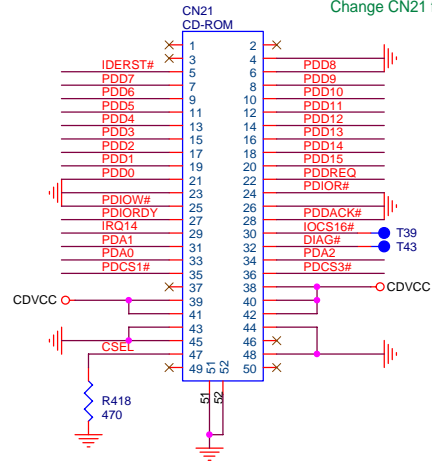

**PROJECT : DW1**  
**Quanta Computer Inc.**

Size B	Document Number <b>CRT, DVI-I</b>	Rev 1A
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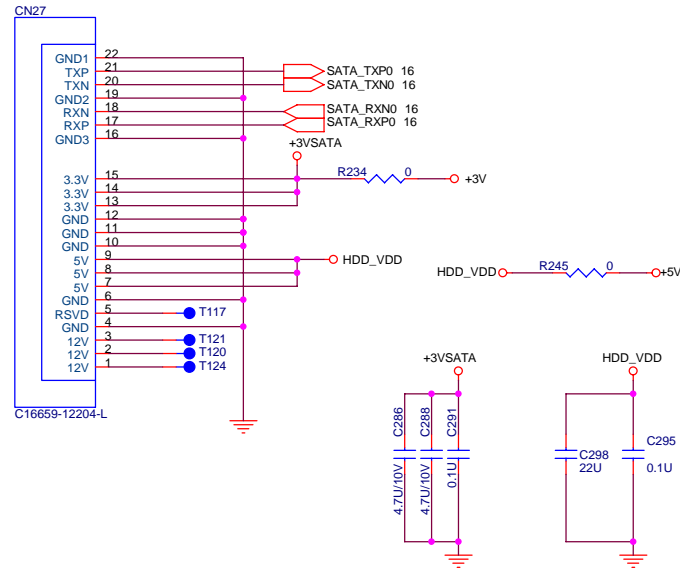
### CD-ROM

B stage:  
Change CN21 footprint.

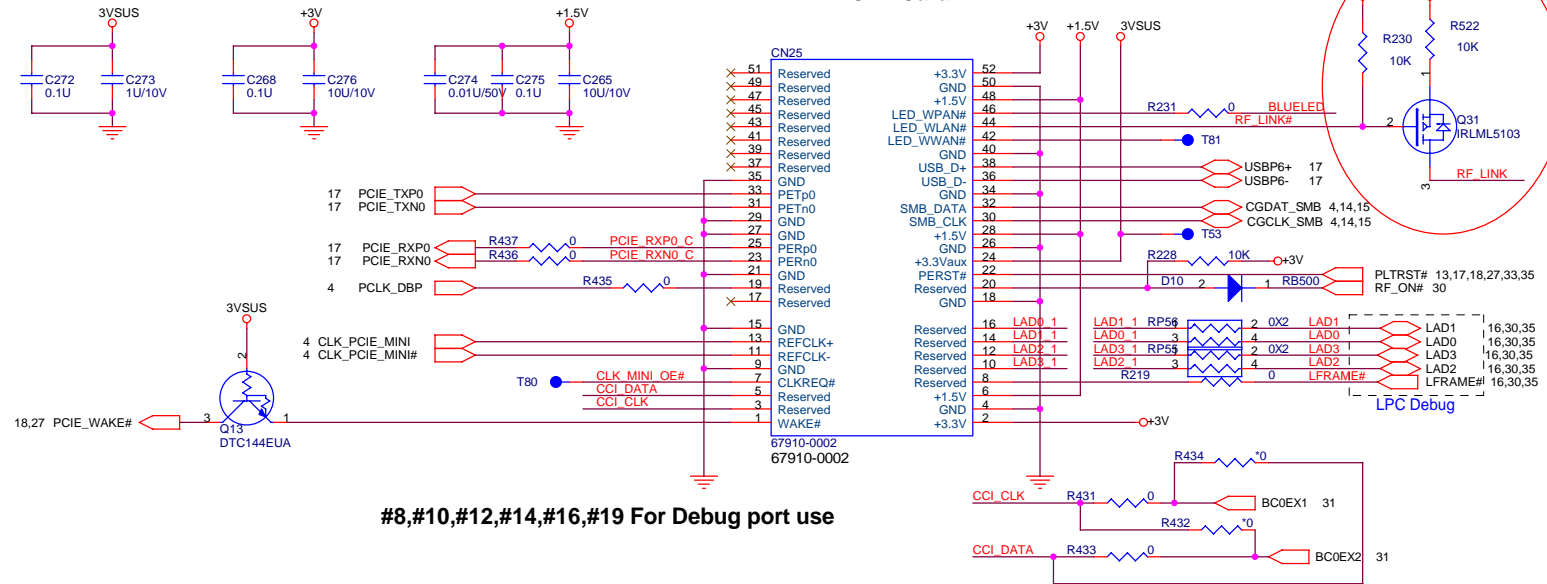
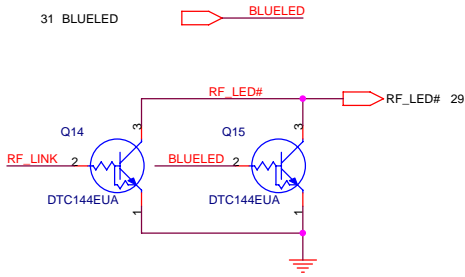


### SATA CONNECTOR

B stage:  
Change CN27 net.

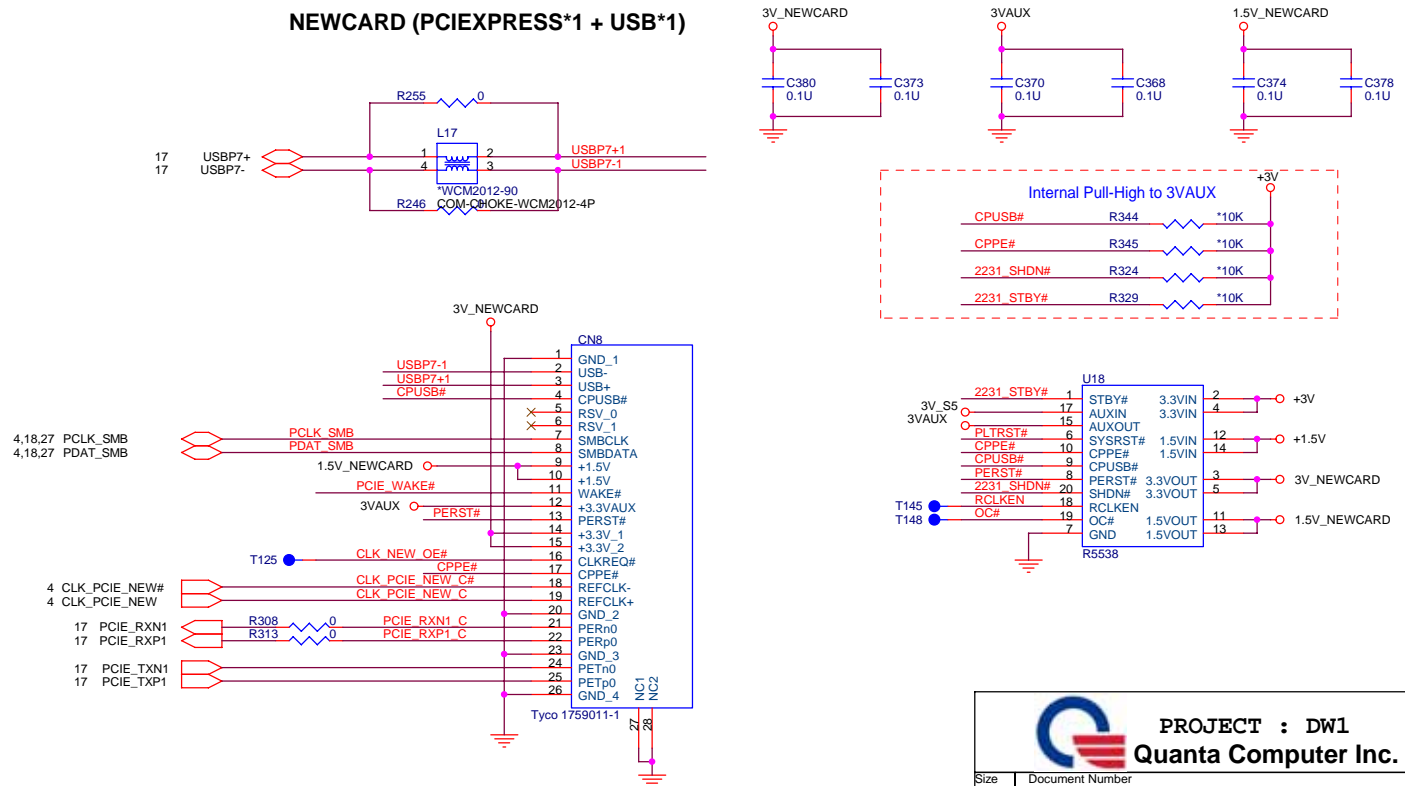


### RF LED control.



#8,#10,#12,#14,#16,#19 For Debug port use

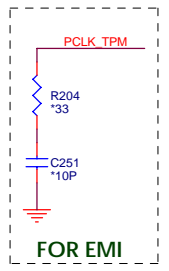
### NEWCARD (PCIEXPRESS\*1 + USB\*1)





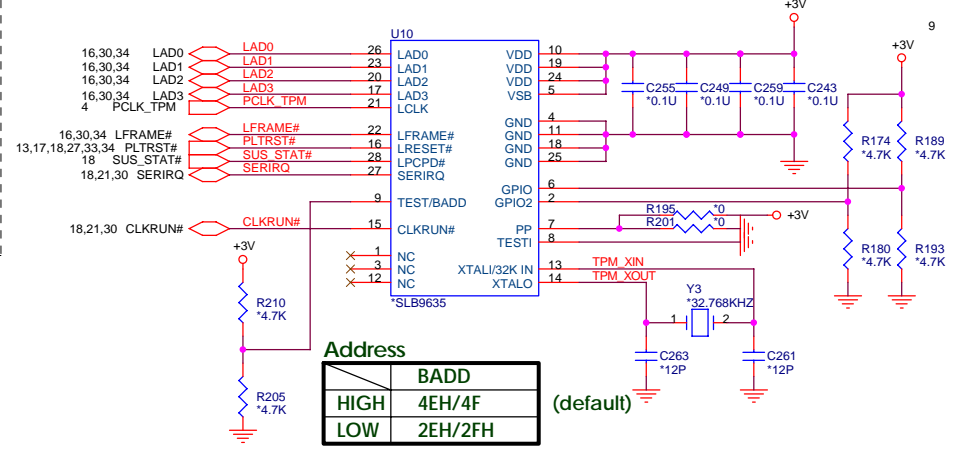
**PROJECT : DW1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	<b>NEW CARD, MINI CARD</b>	1A
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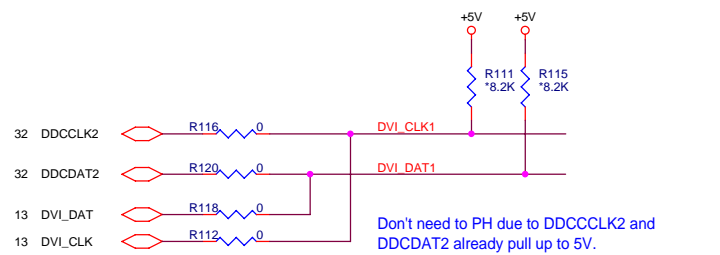
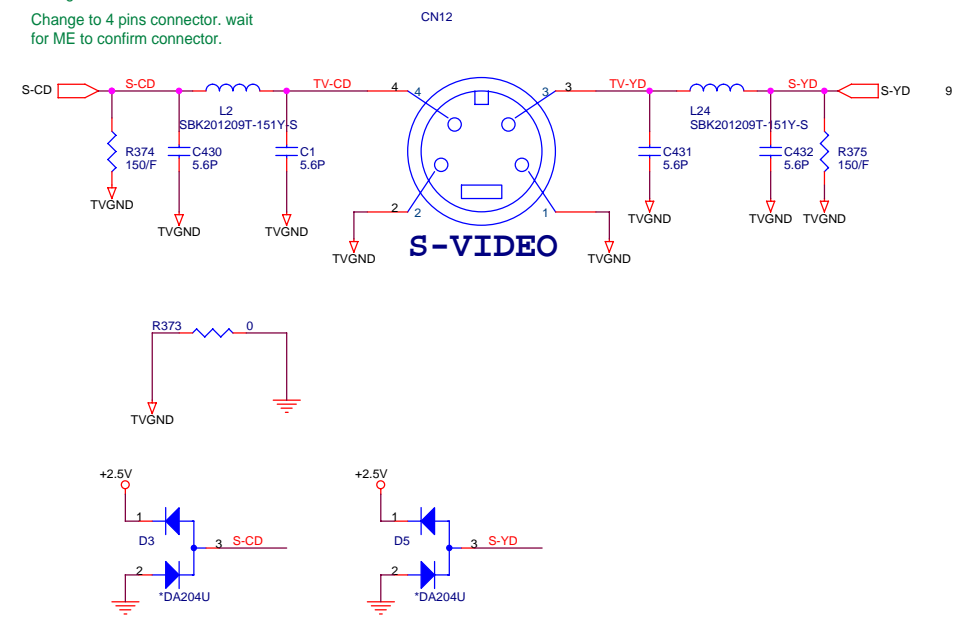
### TPM (1.2)

B stage:  
Change U10 footprint.



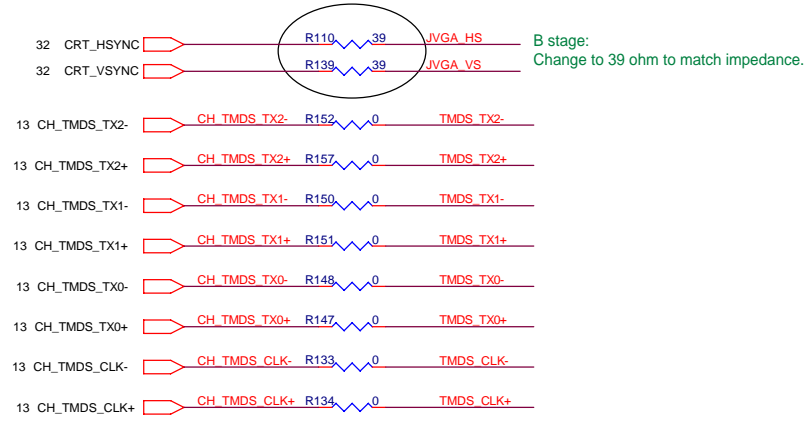
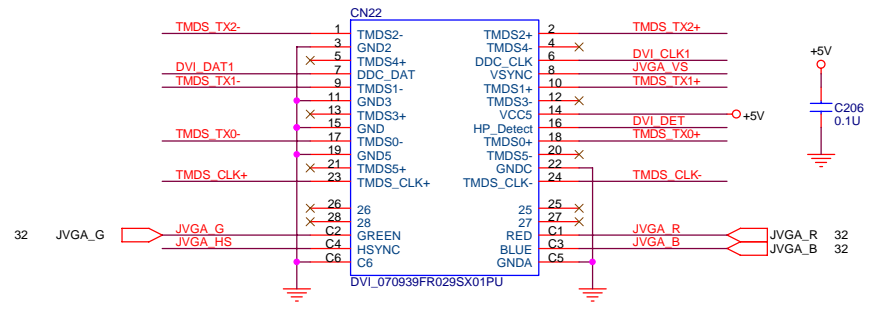
Address		BADD
HIGH	4EH/4F	(default)
LOW	2EH/2FH	

B stage:  
Change to 4 pins connector. wait for ME to confirm connector.



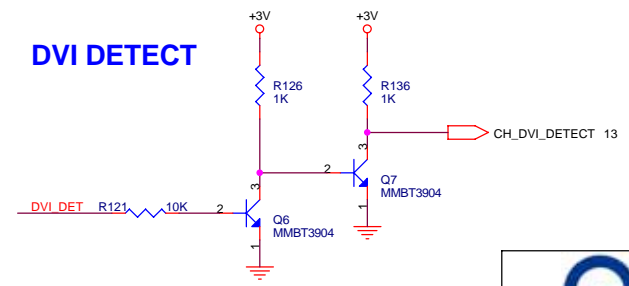
Don't need to PH due to DDCCLK2 and DDCDAT2 already pull up to 5V.

### DVI-I Port



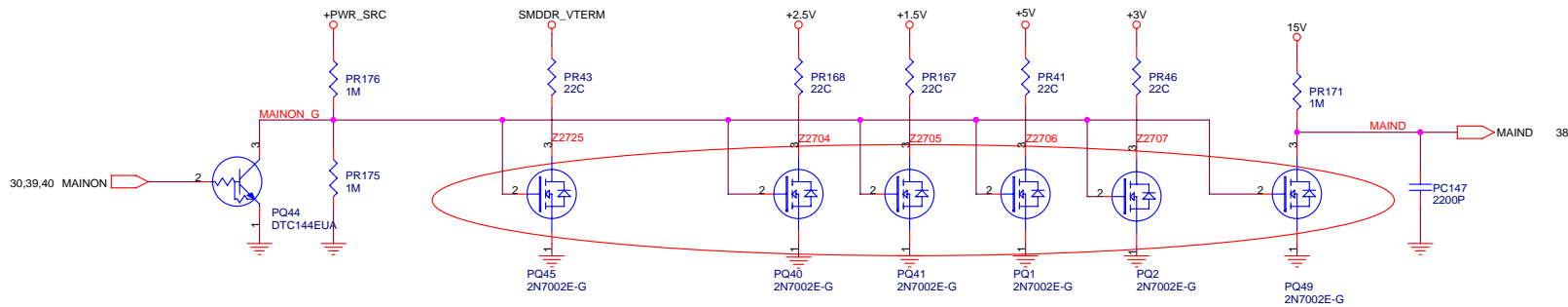
B stage:  
Change to 39 ohm to match impedance.

### DVI DETECT

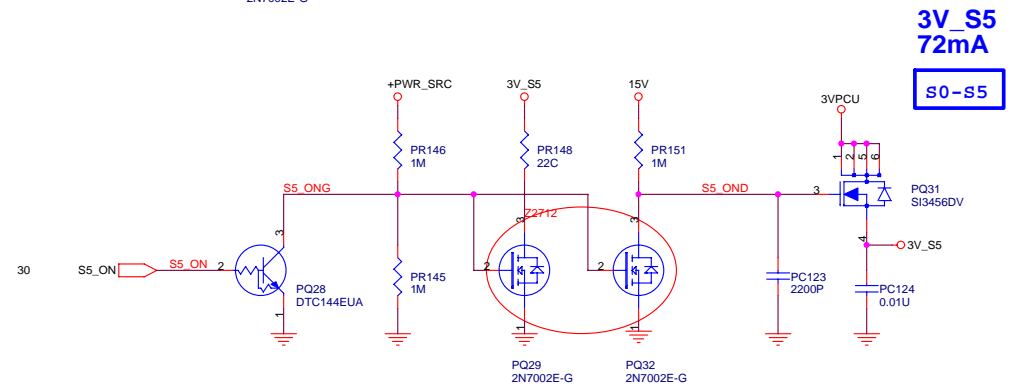


**PROJECT : DW1**  
**Quanta Computer Inc.**

Size	Document Number	TPM	Rev
Custom			1A
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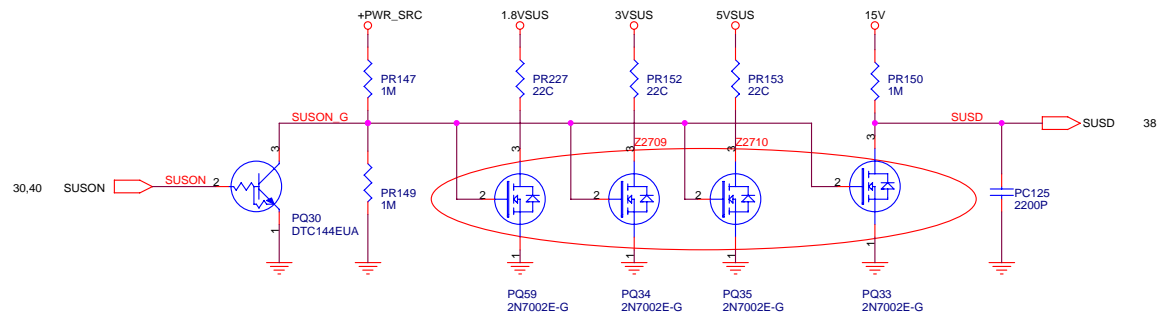
modify from 2N7002E TO 2M7002E-G



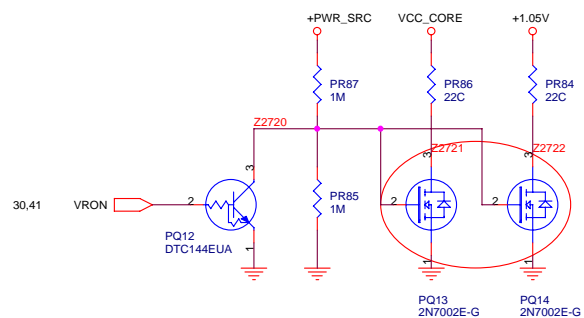
3V\_S5  
72mA

S0-S5

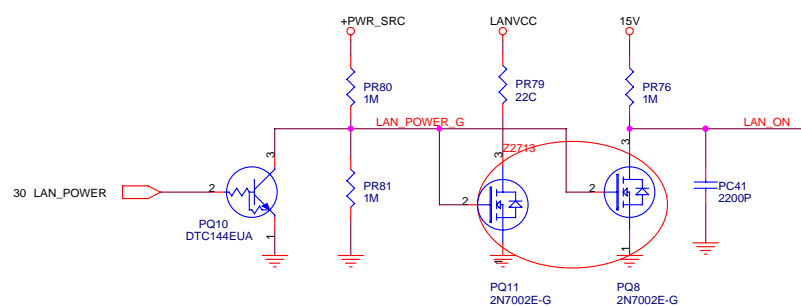
modify from 2N7002E TO 2M7002E-G



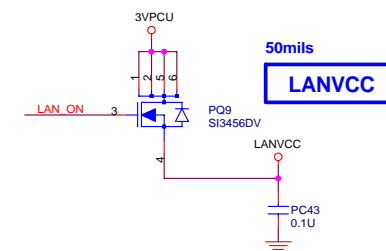
modify from 2N7002E TO 2M7002E-G



modify from 2N7002E TO 2M7002E-G



modify from 2N7002E TO 2M7002E-G



50mils

LANVCC

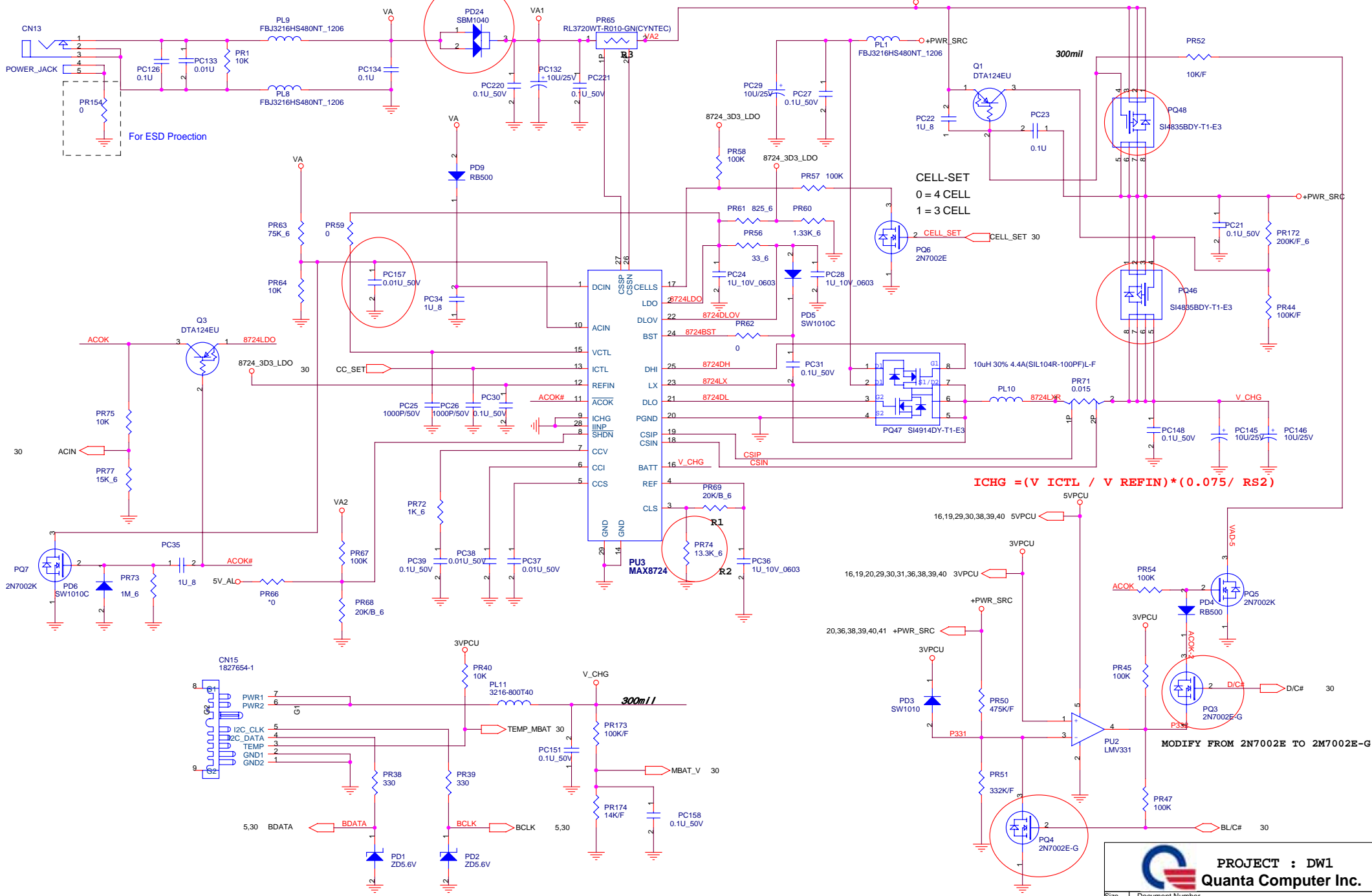
**PROJECT : DW1**  
**Quanta Computer Inc.**

Size Custom	Document Number DISCHARGE	Rev 1A
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A2 TEST TO B TEST PD14 AND PD15 MODIFY FROM SSM24PT TO SBM1040

$$I_{input} = (V_{CLS} / V_{REF}) * (0.075 / R_{S1})$$



$$I_{CHG} = (V_{ICTCL} / V_{REFIN}) * (0.075 / R_{S2})$$

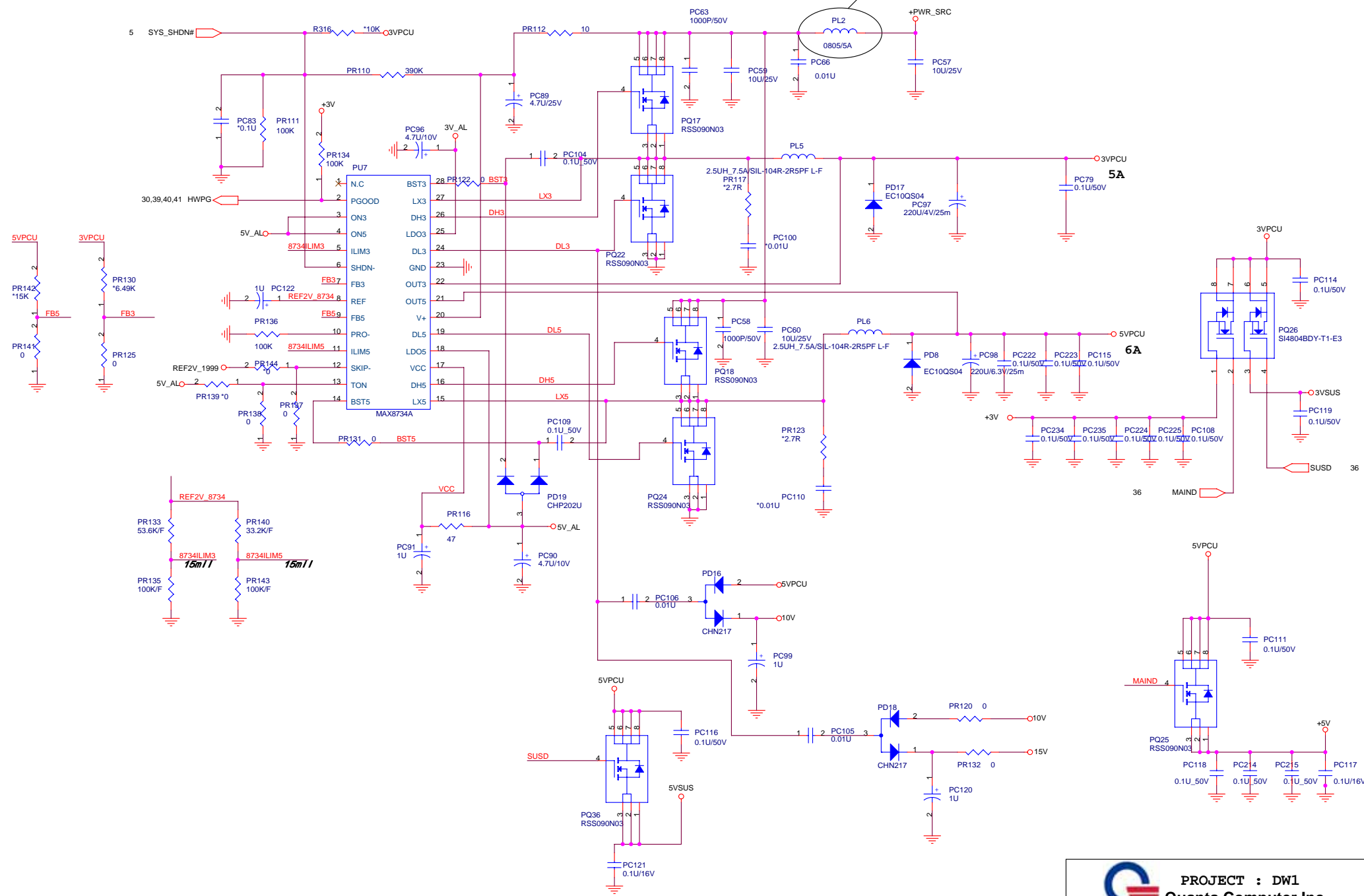
MODIFY FROM 2N7002E TO 2M7002E-G

**PROJECT : DW1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	CHARGE	1A
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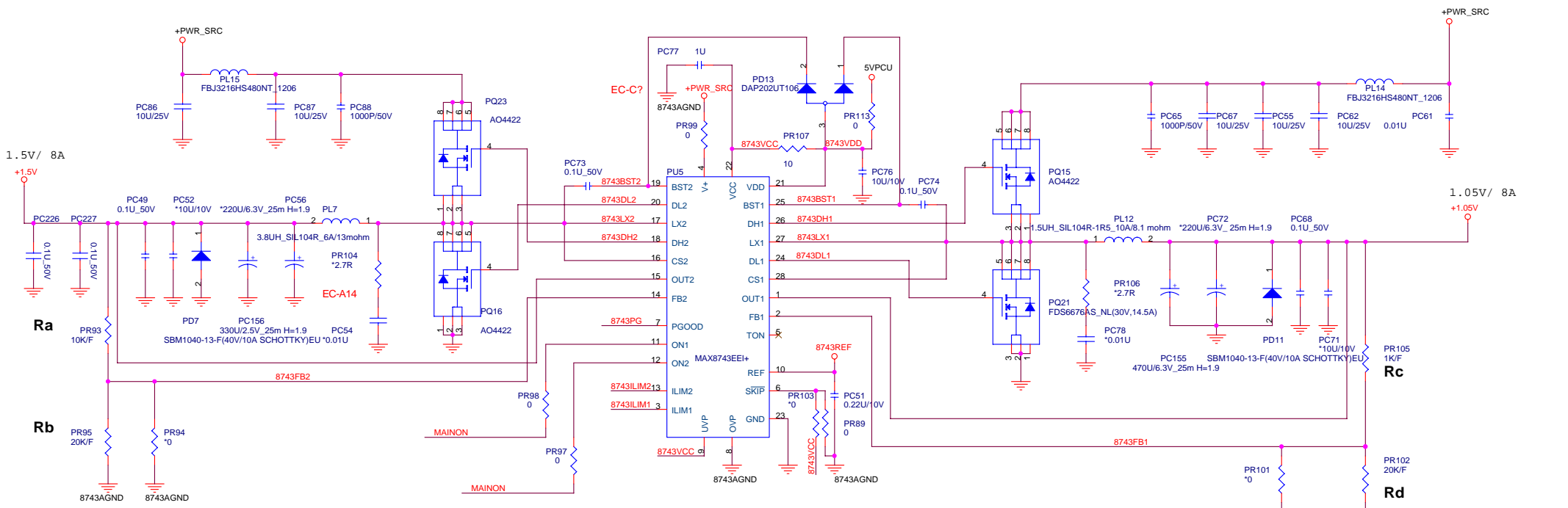
# DC-DC (MAX8734A)

Need create L-F Part number.



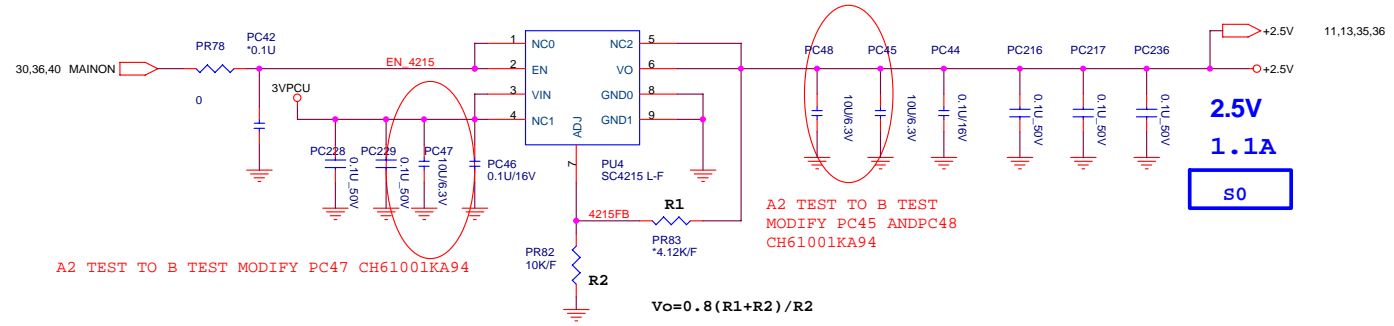
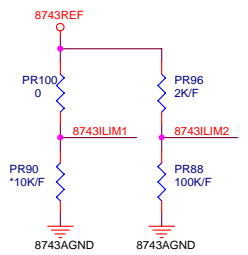
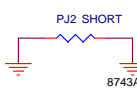
**PROJECT : DW1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	3V/5V	1A
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$V_{out} = (1 + R_a/R_b) * 1$

$V_{out} = (1 + R_c/R_d) * 1$



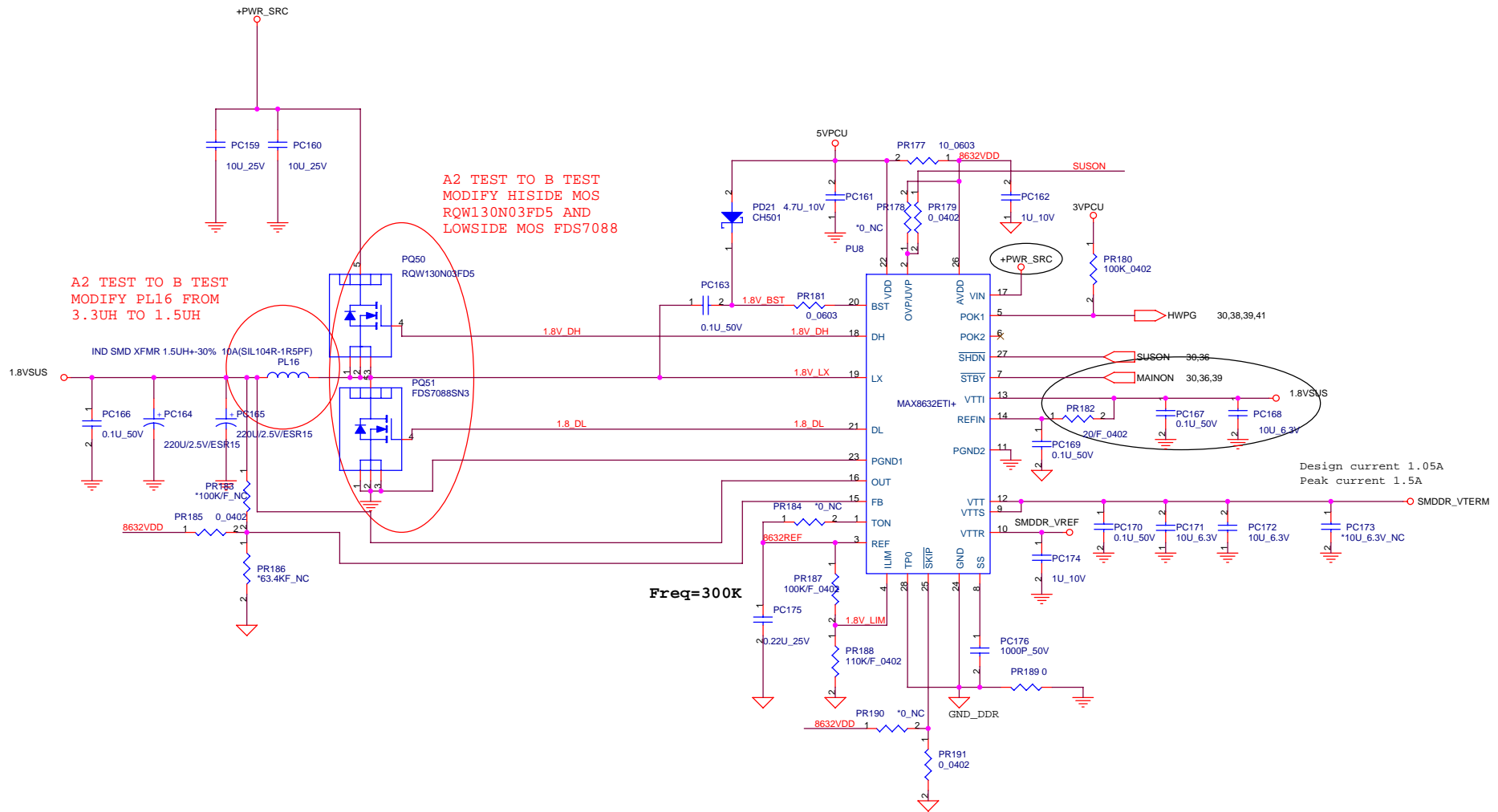
A2 TEST TO B TEST MODIFY PC47 CH61001KA94


A2 TEST TO B TEST MODIFY PC45 AND PC48 CH61001KA94

$V_o = 0.8 (R1 + R2) / R2$

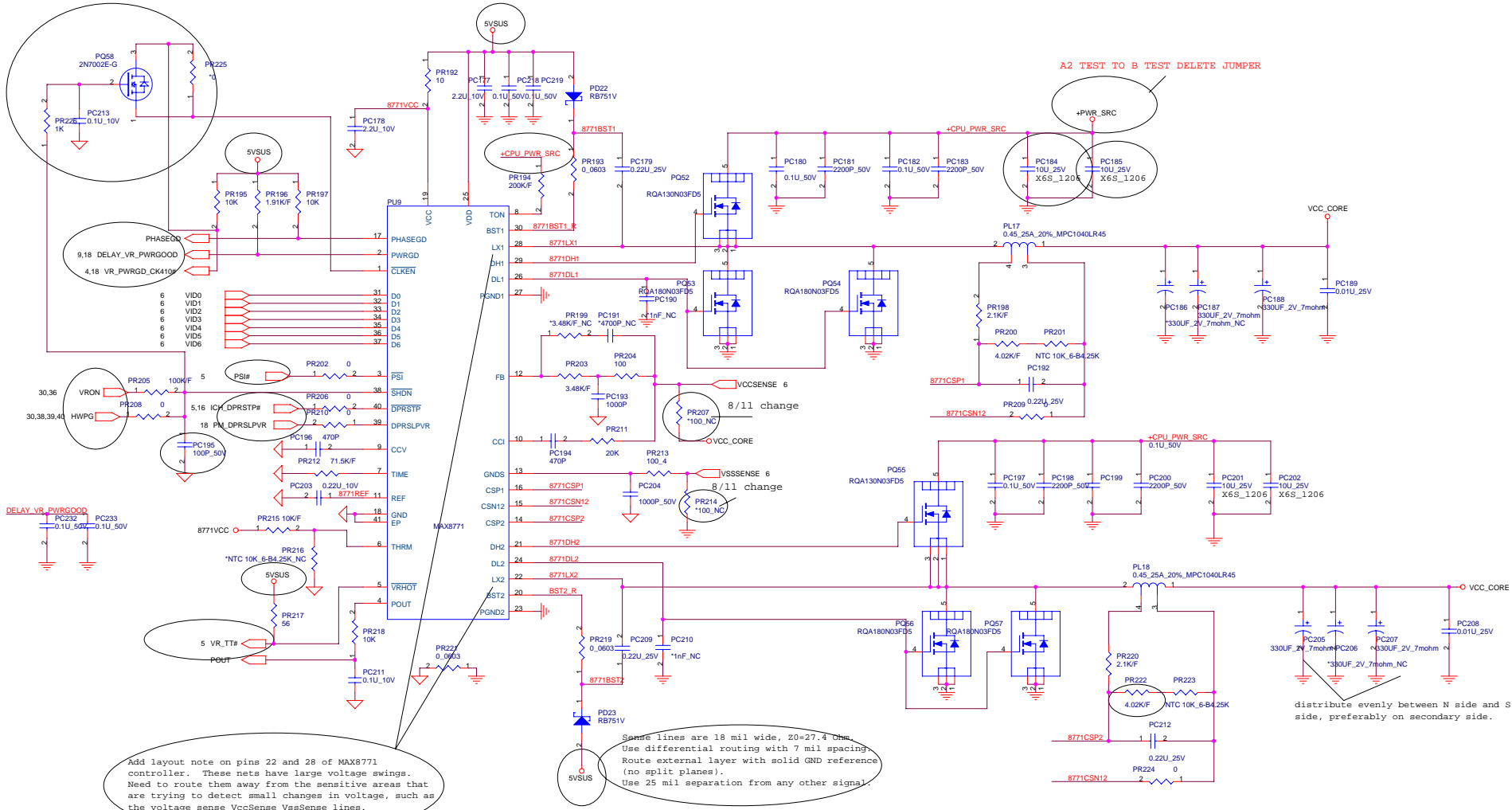
**PROJECT : DW1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	MAX8743 1.5VS_5/+1.05V/2.5V	1A
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**PROJECT : DW1**  
**Quanta Computer Inc.**

Size	Document Number	Rev	
Custom	<b>1.8V/0.9V</b>	1A	
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Add layout note on pins 22 and 28 of MAX8771 controller. These nets have large voltage swings. Need to route them away from the sensitive areas that are trying to detect small changes in voltage, such as the voltage sense VccSense VssSense lines.

Sense lines are 18 mil wide, 20=27.4 Ohm. Use differential routing with 7 mil spacing. Route external layer with solid GND reference (no split planes). Use 25 mil separation from any other signal.

distribute evenly between N side and S side, preferably on secondary side.

IMVP Spec. Rev. 0.8

(Nom.)	Yonah-2M	Meron
HFM	1.2875 V	1.1500 V
LFM	0.8375 V	0.8375 V
Deeper	0.7625 V	0.7625 V
VBOOT	1.2000 V	1.2000 V
SLOPE	-2.1 mV/A	-2.1 mV/A

(Max.)	Yonah-2M	Meron
HFM	36 A	44 A
LFM	9.5 A	12.5 A
Deeper	3.5 A	5.5 A
Dynamic	27 A	34.5 A
TDC	26 A	32 A

V <sub>o</sub>	VID6	VID5	VID4	VID3	VID2	VID1	VID0
1.5000	0	0	0	0	0	0	0
1.4375	0	0	0	0	1	0	1
1.4000	0	0	0	1	0	0	0
1.3000	0	0	1	0	0	0	0
1.2875	0	0	1	0	0	0	1
1.2000	0	0	1	1	0	0	0
1.1500	0	0	1	1	1	0	0
1.1000	0	1	0	0	0	0	0
1.0000	0	1	0	1	0	0	0
0.9625	0	1	0	1	0	1	1
0.9000	0	1	1	0	0	0	0
0.8375	0	1	1	0	1	0	1
0.8000	0	1	1	1	0	0	0
0.7625	0	1	1	1	0	1	1
0.7500	0	1	1	1	1	0	0
0.7000	1	0	0	0	0	0	0
0.6000	1	0	0	1	0	0	0
0.5000	1	0	1	0	0	0	0
0.3000	1	1	0	0	0	0	0

CCM : Continuous Conduction Mode  
DCM : Dis-Continuous Mode

