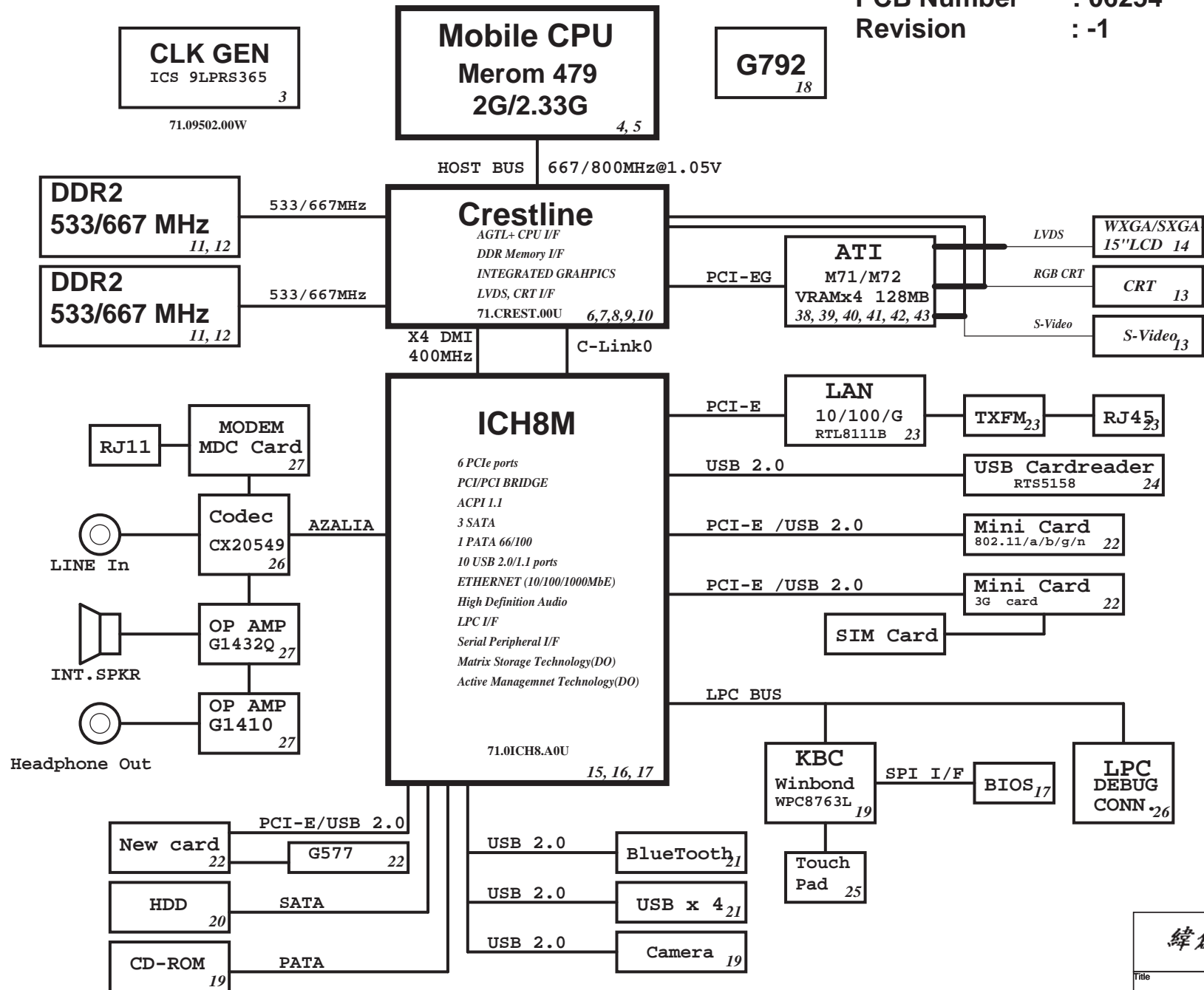


C45/C46 Block Diagram

C45 Project code: 91.4U501.001
 C46 Project code: 91.4V001.001
 PCB Number : 06254
 Revision : -1



SYSTEM DC/DC TPS51120	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 (6A) 3D3V_S5 (7A)
SYSTEM DC/DC SC411	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 (9.5A) 1D8V_S3 (8.5A)
SC411 TPS51110	
DCBATOUT	OUTPUTS
	DDR_VREF_S0 (1.5A) DDR_VREF_S3
APL5913	
1D8V_S3	1D5V_S0 (2A)
APL5915	
3D3V_S0	2D5V_S0 (300mA)
APL5915	
3D3V_S5	1D25V_S0

MAXIM CHARGER MAX8725	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 4.0A UP+5V 5V 100mA

CPU DC/DC ISL6262	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 47A

PCB STACKUP	
L1:	Signal 1
L2:	POWER
L3:	Signal 2
L4:	Signal 3
L5:	GND
L6:	Signal 4

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Title: **BLOCK DIAGRAM**

Size: Custom Document Number: **C45/C46** Rev: **-1**

Date: Tuesday, April 24, 2007 Sheet 1 of 45

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers: offset 224h)
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE config2 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#/SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM's when sampled high
LAN100_SLP	Integrated VccLAN1_05 and VccCL1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccLAN1_05 and VccCL1_05 VRM's when sampled high
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	This signal has a weak internal pull-up. Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be used in manufacturing environments.

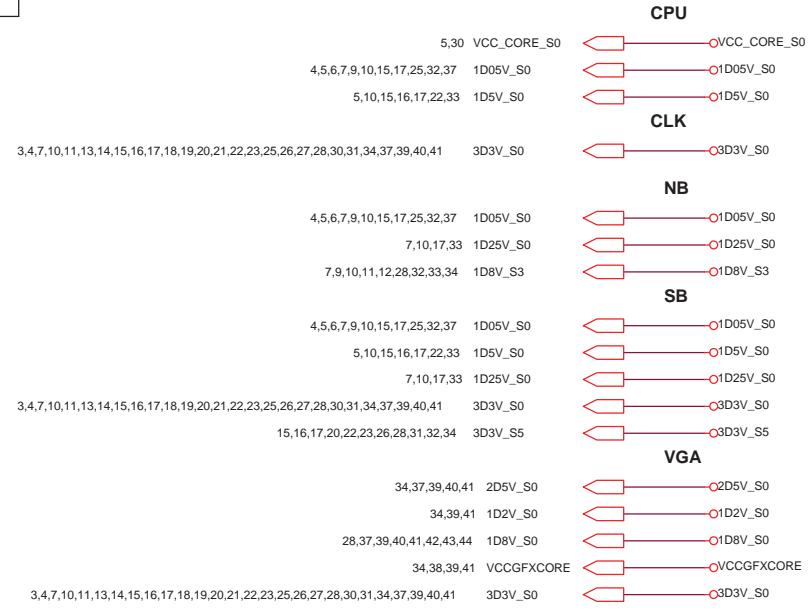
SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	PULL-UP TBD

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB800 011 = FSB667 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG[7:6]	Reserved	
CFG8	Low Power PCI Express	0 = Normal mode 1 = Low Power mode (Default)
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. 1 = Normal operation(Default):Lane Numbered in order
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal operation (Default):lane Numbered in order 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	0 = Only SDVO or PCIE x1 is operational (Default) 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCTRL_DATA	SDVO Present	0 = No SDVO Card present (Default) 1 = SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Calistoga GMCH PWROK in signal.

ICH8M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------



PCI Routing page 17

	IDSEL	INT	REQ	GNT

USB Table

Pair	Device
0	USB1(ON BOARD)
1	USB2(EXT. USB)
2	USB3(EXT. USB)
3	USB4(EXT. USB)
4	MINICARD
5	USB Cardreader
6	MINICARD
7	NEW CARD
8	BLUETOOTH
9	MINICARD

PCIE Routing

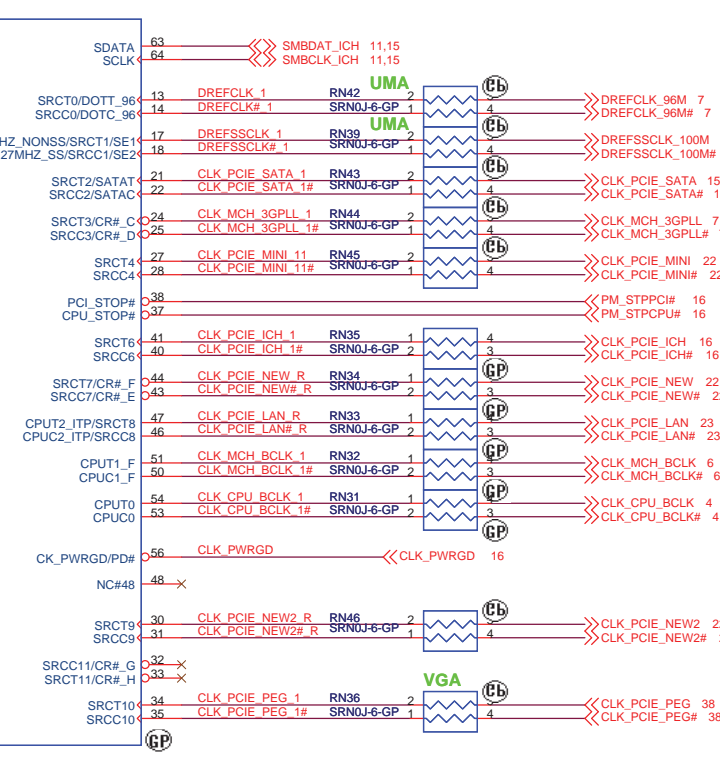
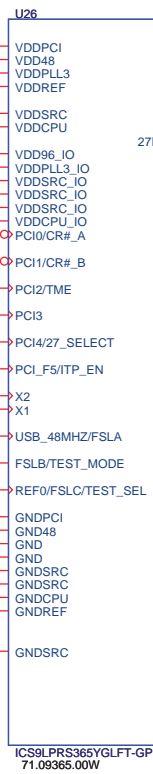
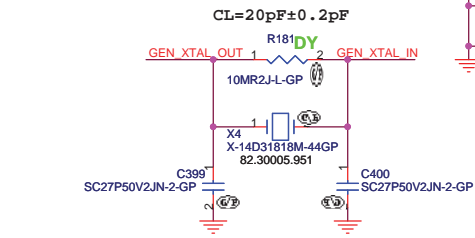
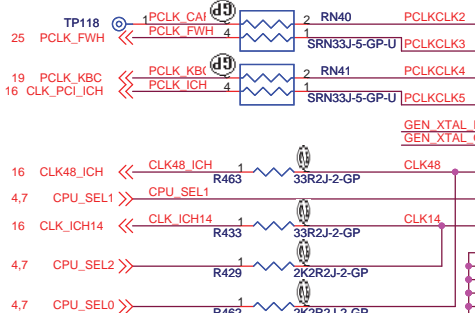
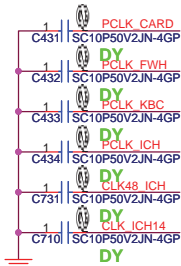
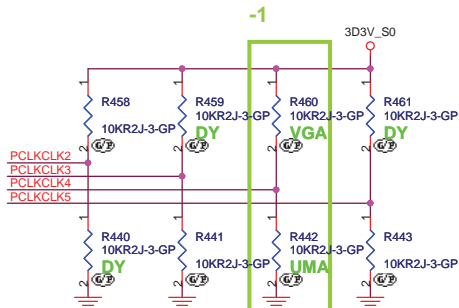
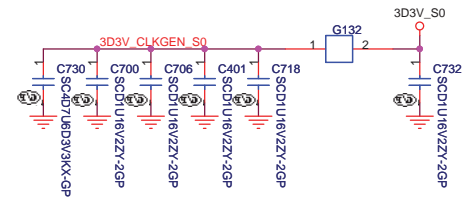
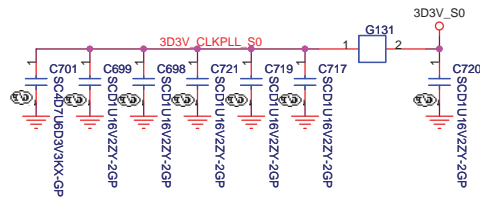
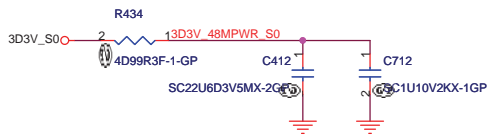
LANE1	LAN

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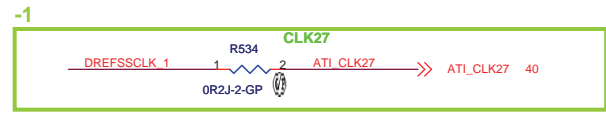
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Size Custom: Document Number **C45/C46** Rev **SA**

Date: Wednesday, April 25, 2007 Sheet 2 of 45



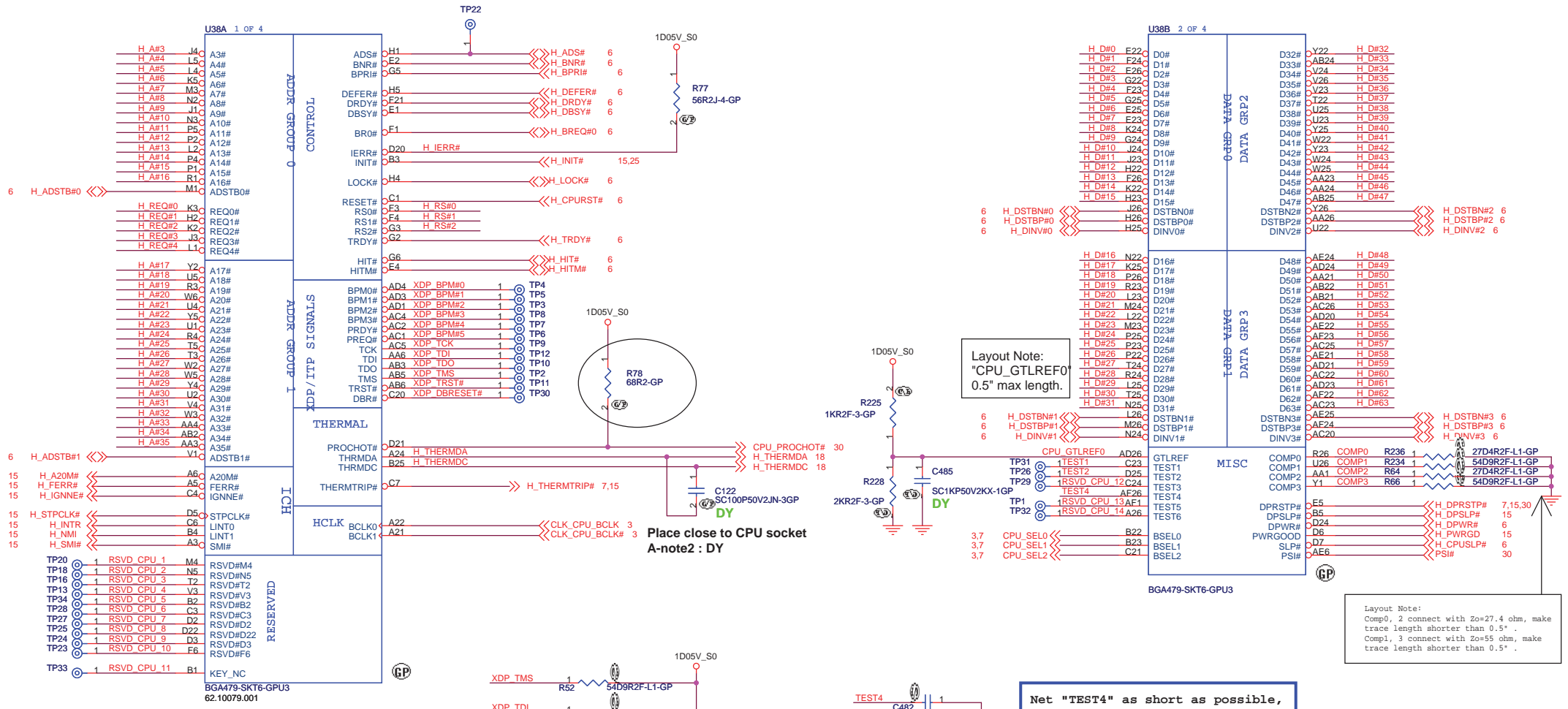
Ext. VGA:71.09365.00W (64pin)



SEL2	SEL1	SELO	CPU	FSB
FSC	FSB	FSA		X
1	0	1	100M	X
0	0	1	133M	667M
0	1	1	166M	800M
0	1	0	200M	

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1 = CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1 = CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1 = CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1 = CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3/RC-5_EN	0 = Pin37 as CPU_STOP#, pin 38 as PCI_STOP#. 1 = Pins37,38 as SRC-5 differential pair.
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96#, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/I TP_EN	0 = SRC8/SRC8# 1 = ITP/I TP#

- H_RS#[0..2] 6
- H_REQ#[0..4] 6
- H_D#[0..63] 6
- H_A#[3..35] 6

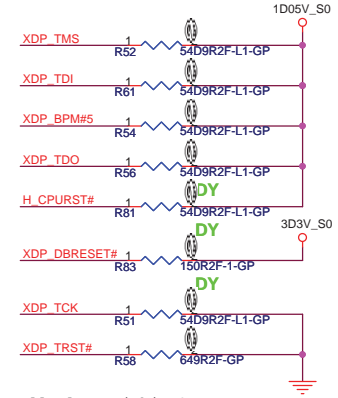


Layout Note:
"CPU_GTLREF0"
0.5" max length.

Layout Note:
Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5".
Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5".

Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals

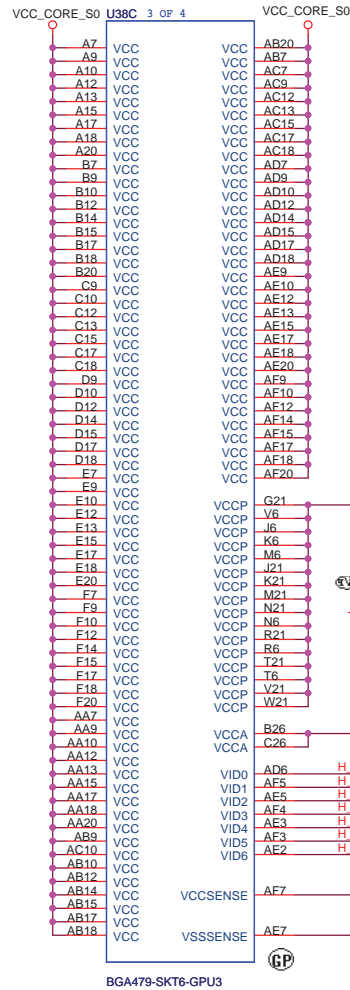
1st source : 62.10053.401
2nd source : 62.10079.001



All place within 2" to CPU

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

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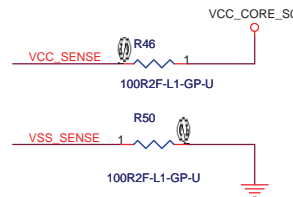


lvccp boot= 4.5A
lvccp stable= 2.5A

Place close to CPU socket
A-note2

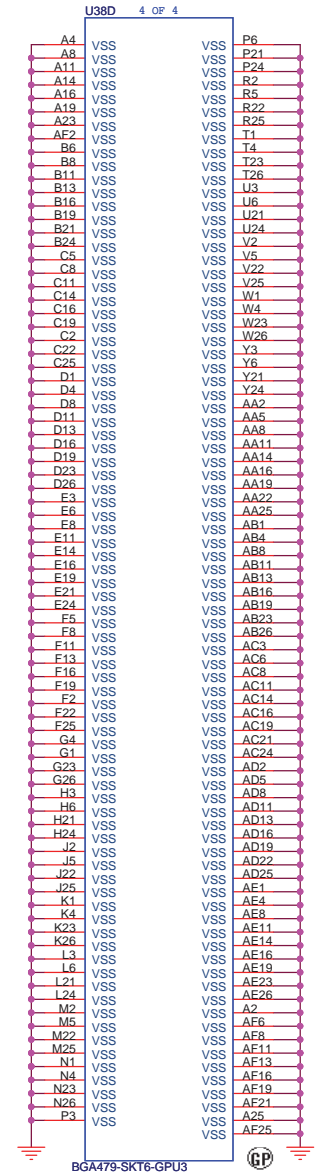
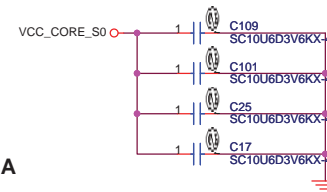
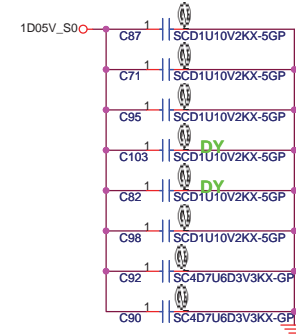
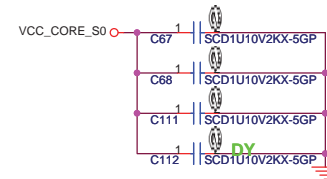
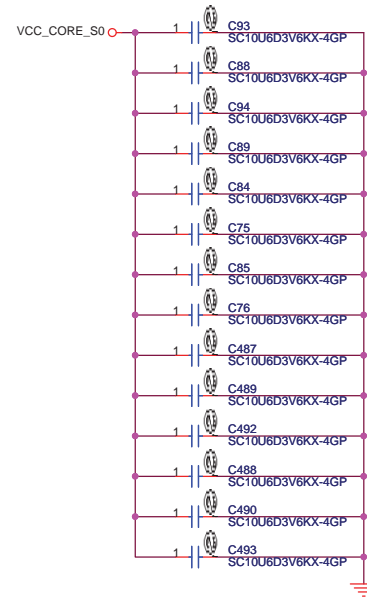
IVCCA = 130mA

layout note: "1D5V_VCCA_S0"
as short as possible



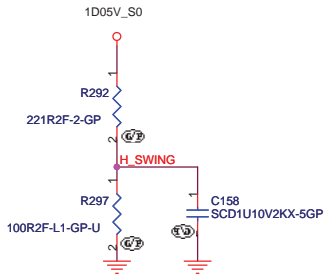
Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.

Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.



H_SWING routing Trace width and Spacing use 10 / 20 mil

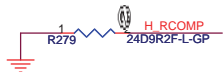
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_SCOMP and H_SCOMP# Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")

U46A 1 OF 10

H_D#0	E2C	H_D#0	H_A#3	J13	H_A#3
H_D#1	G2C	H_D#1	H_A#4	B11	H_A#4
H_D#2	G7C	H_D#2	H_A#5	C11	H_A#5
H_D#3	M6C	H_D#3	H_A#6	M11	H_A#6
H_D#4	H7C	H_D#4	H_A#7	C15	H_A#7
H_D#5	G4C	H_D#5	H_A#8	E16	H_A#8
H_D#6	F3C	H_D#6	H_A#9	L13	H_A#9
H_D#7	N8C	H_D#7	H_A#10	G17	H_A#10
H_D#8	H2C	H_D#8	H_A#11	C14	H_A#11
H_D#9	M10C	H_D#9	H_A#12	K16	H_A#12
H_D#10	N12C	H_D#10	H_A#13	B13	H_A#13
H_D#11	N9C	H_D#11	H_A#14	L16	H_A#14
H_D#12	H5C	H_D#12	H_A#15	J17	H_A#15
H_D#13	P13C	H_D#13	H_A#16	B14	H_A#16
H_D#14	K9C	H_D#14	H_A#17	K19	H_A#17
H_D#15	W10C	H_D#15	H_A#18	P15	H_A#18
H_D#16	M2C	H_D#16	H_A#19	R17	H_A#19
H_D#17	Y8C	H_D#17	H_A#20	B16	H_A#20
H_D#18	V4C	H_D#18	H_A#21	H20	H_A#21
H_D#19	M3C	H_D#19	H_A#22	L19	H_A#22
H_D#20	J1C	H_D#20	H_A#23	D17	H_A#23
H_D#21	N5C	H_D#21	H_A#24	M17	H_A#24
H_D#22	N3C	H_D#22	H_A#25	N16	H_A#25
H_D#23	W8C	H_D#23	H_A#26	J19	H_A#26
H_D#24	Y7C	H_D#24	H_A#27	B18	H_A#27
H_D#25	N2C	H_D#25	H_A#28	E19	H_A#28
H_D#26	P4C	H_D#26	H_A#29	B17	H_A#29
H_D#27	W3C	H_D#27	H_A#30	B15	H_A#30
H_D#28	Y9C	H_D#28	H_A#31	E17	H_A#31
H_D#29	AD12C	H_D#29	H_A#32	C18	H_A#32
H_D#30	AE3C	H_D#30	H_A#33	A19	H_A#33
H_D#31	AD9C	H_D#31	H_A#34	B19	H_A#34
H_D#32	AC9C	H_D#32	H_A#35	N19	H_A#35
H_D#33	AC7C	H_D#33			
H_D#34	AD11C	H_D#34			
H_D#35	AC11C	H_D#35			
H_D#36	AB2C	H_D#36			
H_D#37	AD7C	H_D#37			
H_D#38	AB1C	H_D#38			
H_D#39	Y3C	H_D#39			
H_D#40	AC6C	H_D#40			
H_D#41	AE2C	H_D#41			
H_D#42	AC5C	H_D#42			
H_D#43	AG3C	H_D#43			
H_D#44	AJ9C	H_D#44			
H_D#45	AH8C	H_D#45			
H_D#46	AJ14C	H_D#46			
H_D#47	AE9C	H_D#47			
H_D#48	AE11C	H_D#48			
H_D#49	AH12C	H_D#49			
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H_D#51	AH5C	H_D#51			
H_D#52	AJ6C	H_D#52			
H_D#53	AE7C	H_D#53			
H_D#54	AJ7C	H_D#54			
H_D#55	AJ2C	H_D#55			
H_D#56	AE5C	H_D#56			
H_D#57	AJ3C	H_D#57			
H_D#58	AH2C	H_D#58			
H_D#59	AH13C	H_D#59			

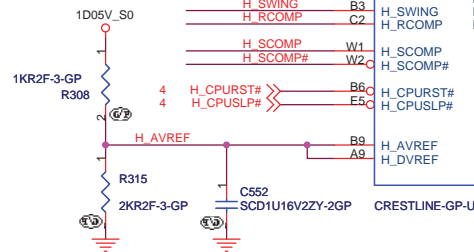


HOST

H_ADS#	G12	H_ADS#	4
H_ADSTB#0	H17	H_ADSTB#0	4
H_ADSTB#1	G20	H_ADSTB#1	4
H_BNR#	C8	H_BNR#	4
H_BPR#	E8	H_BPR#	4
H_BREQ#	F12	H_BREQ#	4
H_DEFER#	D6	H_DEFER#	4
H_DBSY#	C10	H_DBSY#	4
HPLL_CLK#	AM5	CLK_MCH_BCLK	3
HPLL_CLK#	AM7	CLK_MCH_BCLK#	3
H_DPWR#	H8	H_DPWR#	4
H_DRDY#	K7	H_DRDY#	4
H_HIT#	E4	H_HIT#	4
H_HITM#	C6	H_HITM#	4
H_LOCK#	G10	H_LOCK#	4
H_TRDY#	B7	H_TRDY#	4

H_DIN#0	K5	H_DIN#0	4
H_DIN#1	L2	H_DIN#1	4
H_DIN#2	AD13	H_DIN#2	4
H_DIN#3	AE13	H_DIN#3	4
H_DSTBN#0	M7	H_DSTBN#0	4
H_DSTBN#1	K3	H_DSTBN#1	4
H_DSTBN#2	AD2	H_DSTBN#2	4
H_DSTBN#3	AH11	H_DSTBN#3	4
H_DSTBP#0	L7	H_DSTBP#0	4
H_DSTBP#1	K2	H_DSTBP#1	4
H_DSTBP#2	AC2	H_DSTBP#2	4
H_DSTBP#3	AJ10	H_DSTBP#3	4

H_REQ#0	M14	H_REQ#0	
H_REQ#1	E13	H_REQ#1	
H_REQ#2	A11	H_REQ#2	
H_REQ#3	H13	H_REQ#3	
H_REQ#4	B12	H_REQ#4	
H_RS#0	E12	H_RS#0	
H_RS#1	D7	H_RS#1	
H_RS#2	D8	H_RS#2	

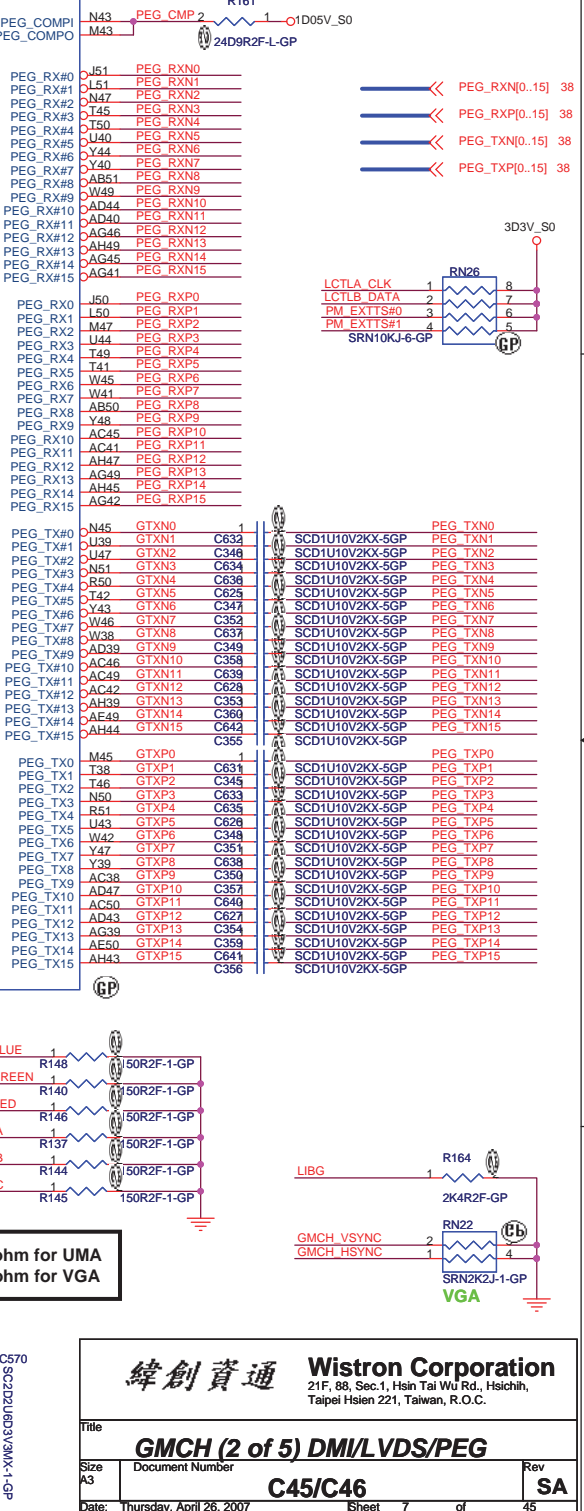
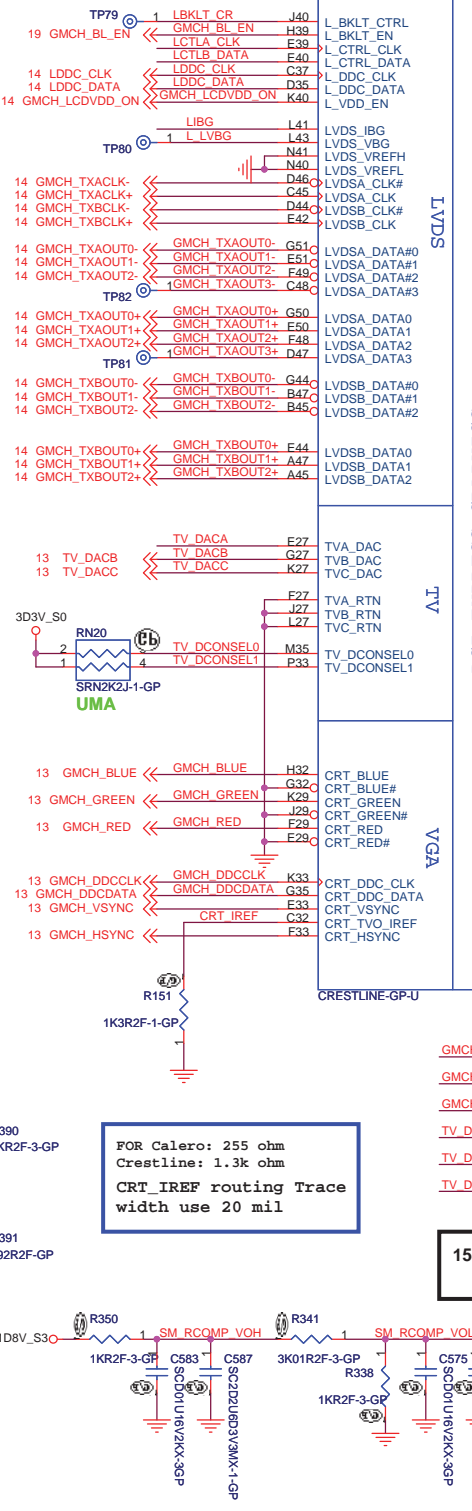
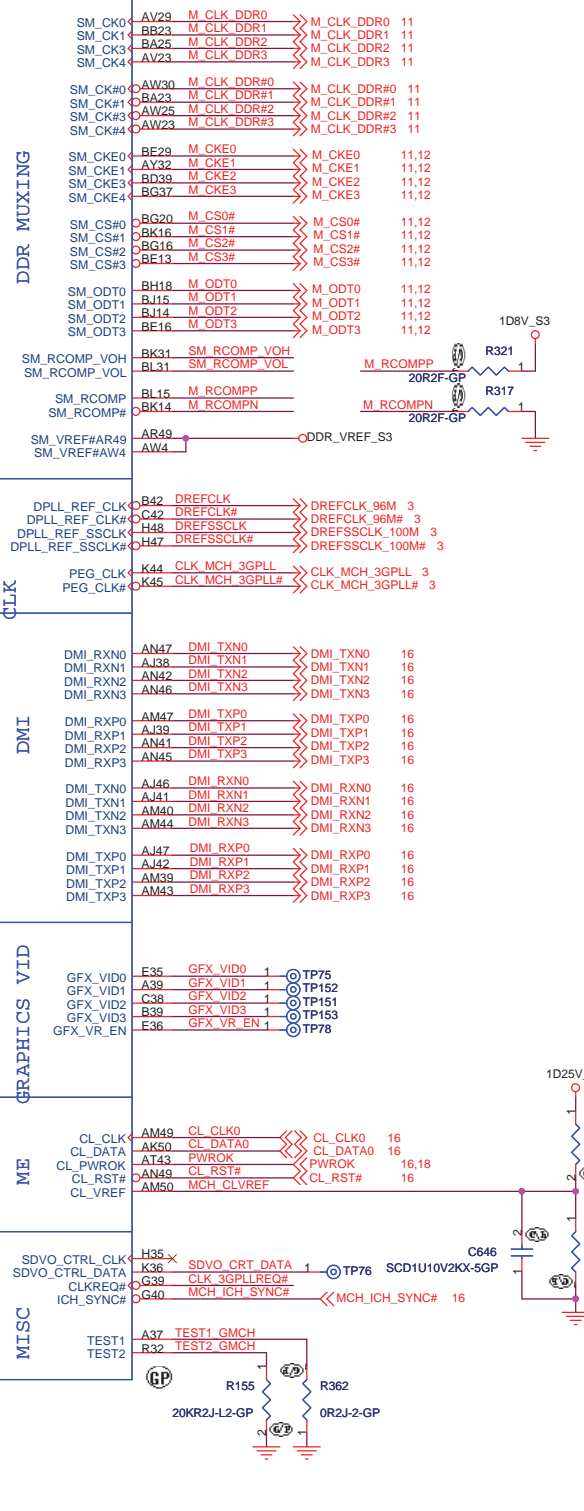
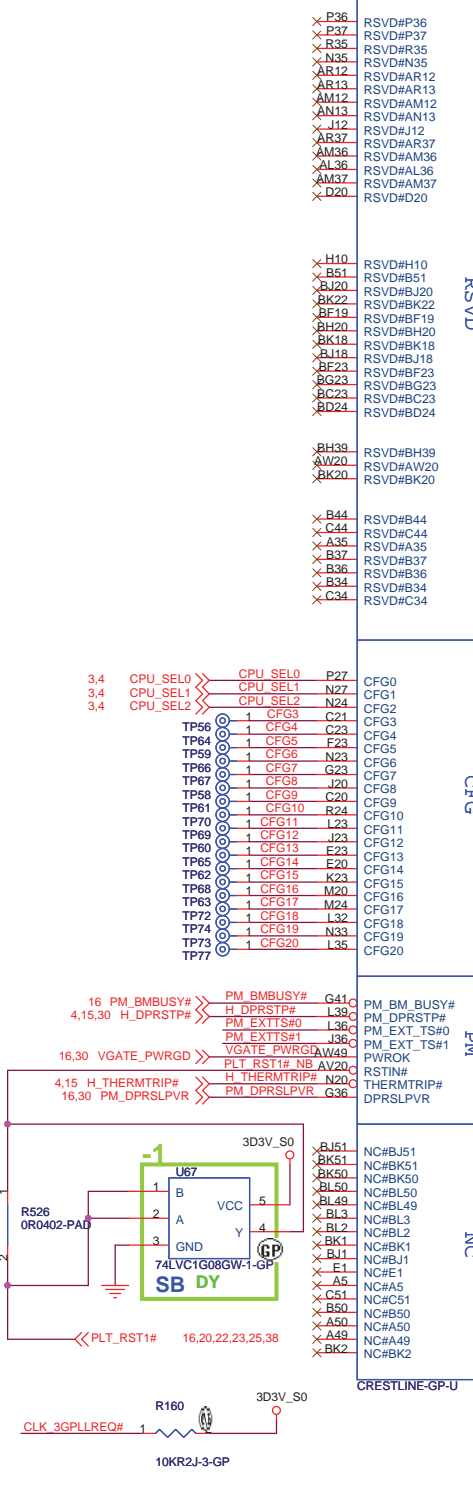


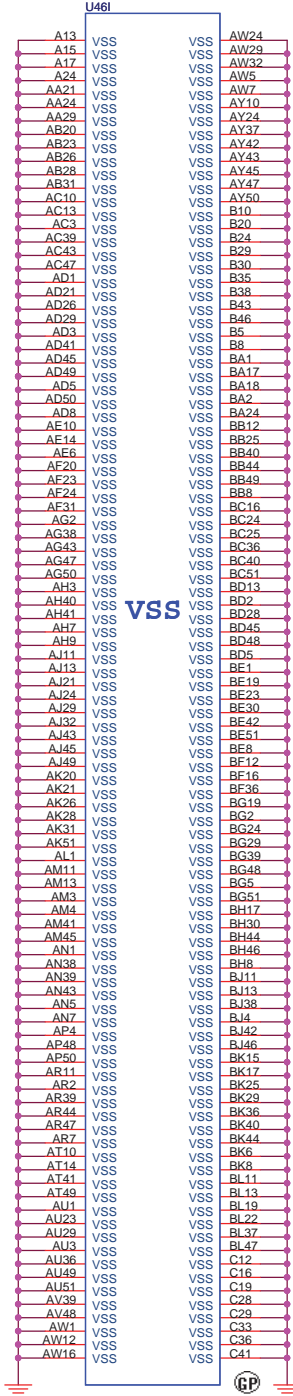
H_REF Decoupling Crestline close Crestline 100 mil

965GM (71.GM965.00U)
965PM (71.PM965.00U)

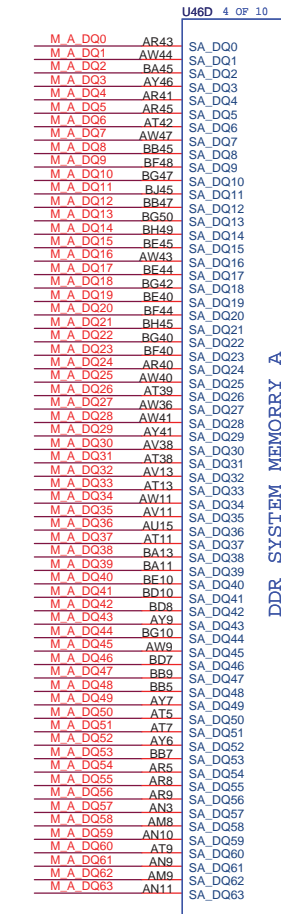
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Title		
GMCH (1 of 5) AGTL		
Size	Document Number	Rev
Custom	C45/C46	SA
Date:	Wednesday, April 25, 2007	Sheet 6 of 45





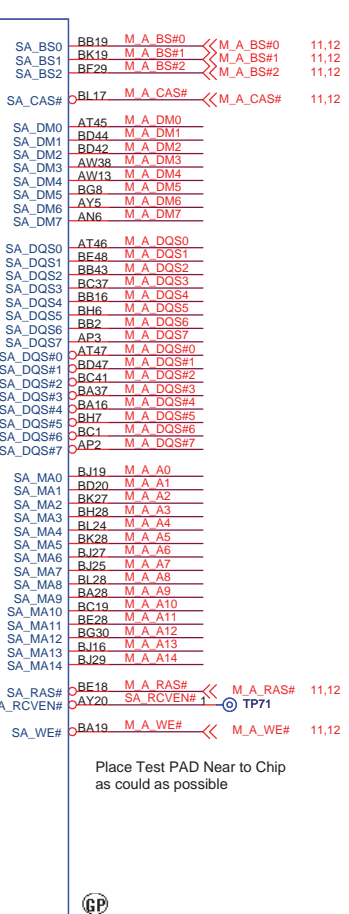
CRESTLINE-GP-U



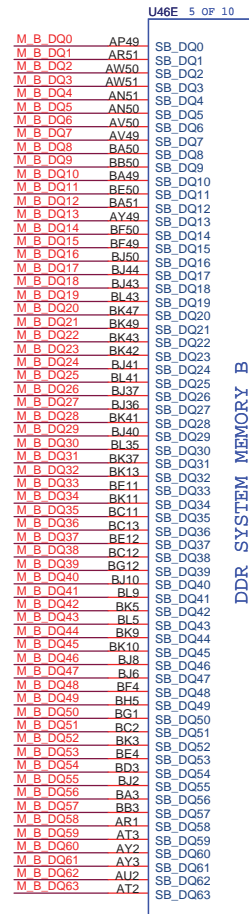
CRESTLINE-GP-U



DDR SYSTEM MEMORY A

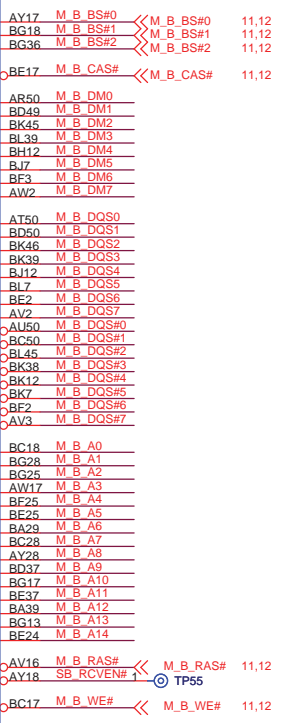


Place Test PAD Near to Chip as could as possible



CRESTLINE-GP-U

DDR SYSTEM MEMORY B



Place Test PAD Near to Chip as could as possible



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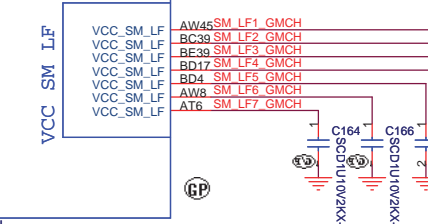
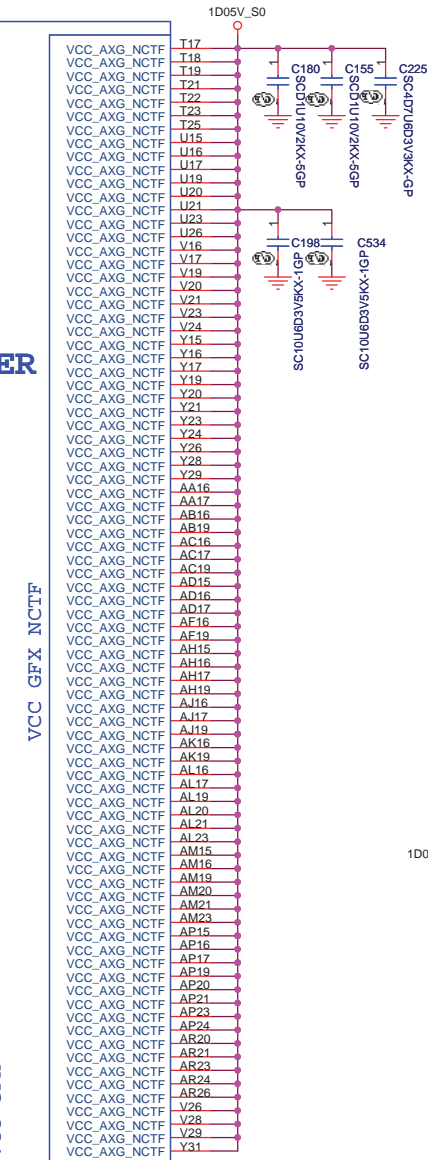
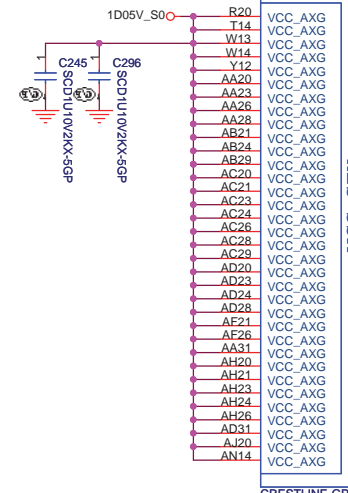
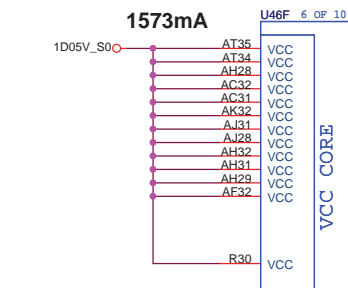
Title: **GMCH (3 of 5) MEMORY**

Size: Custom Document Number: **C45/C46** Rev: SA

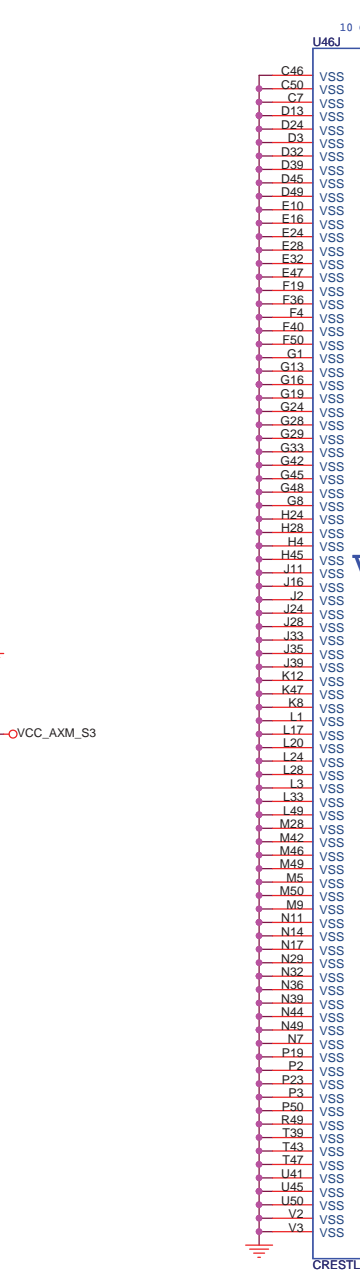
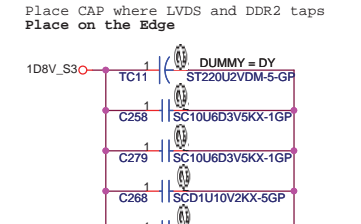
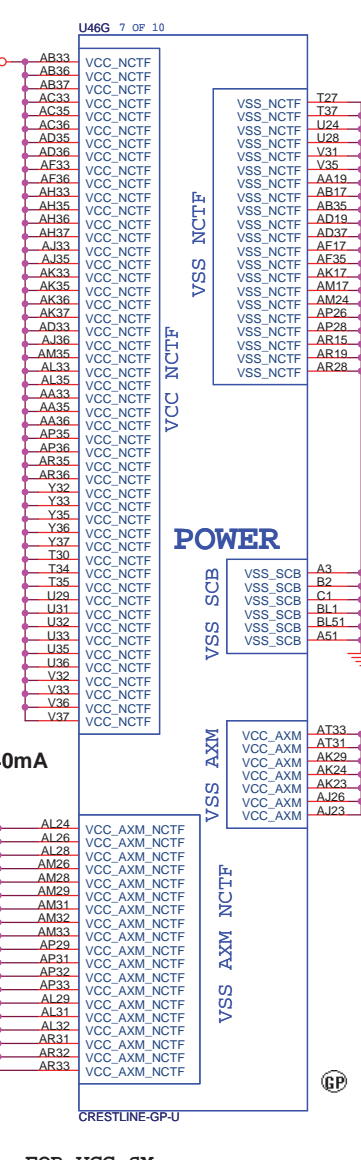
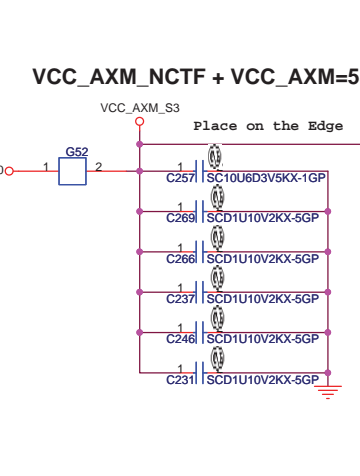
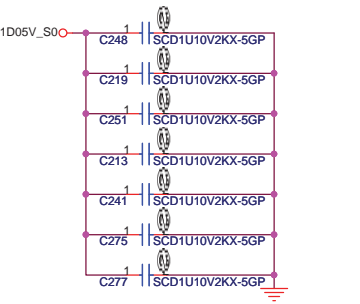
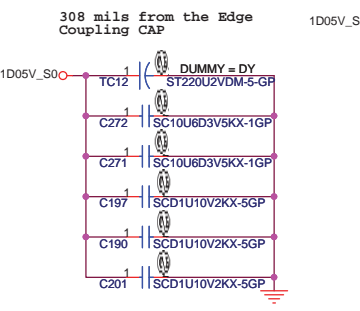
Date: Wednesday, April 25, 2007 Sheet 8 of 45

VCC_NCTF + VCC=1573mA

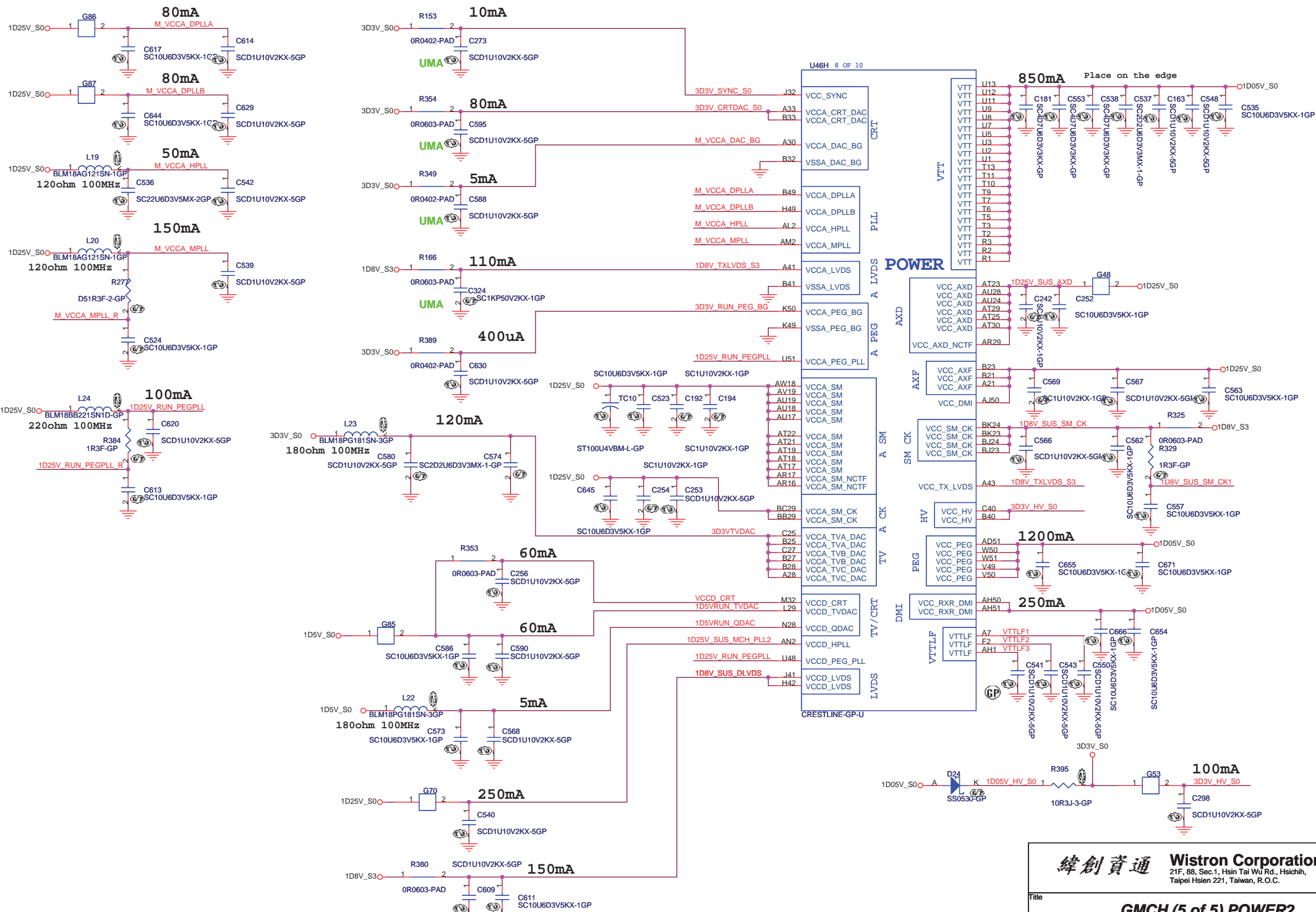
VCC_AXG_NCTF + VCC_AXG=7700mA



FOR VCC CORE AND VCC NCTF

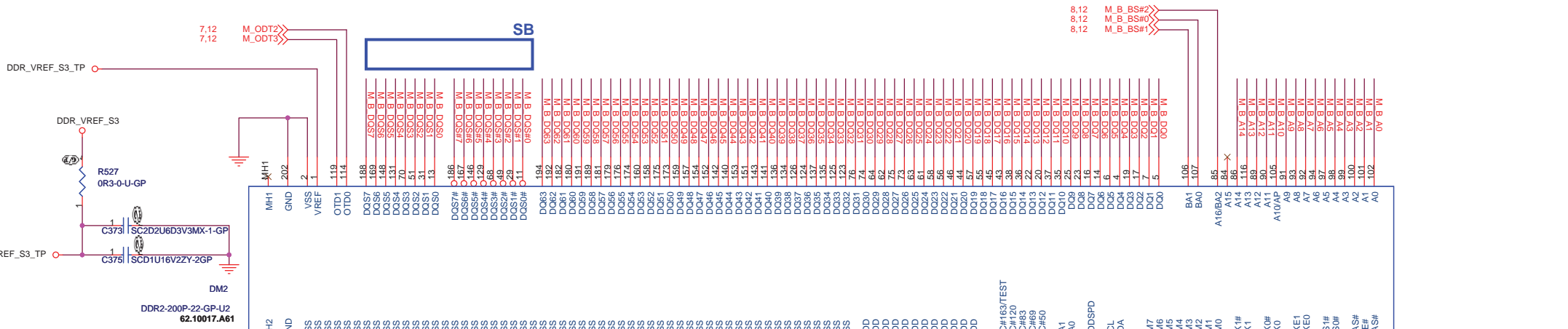


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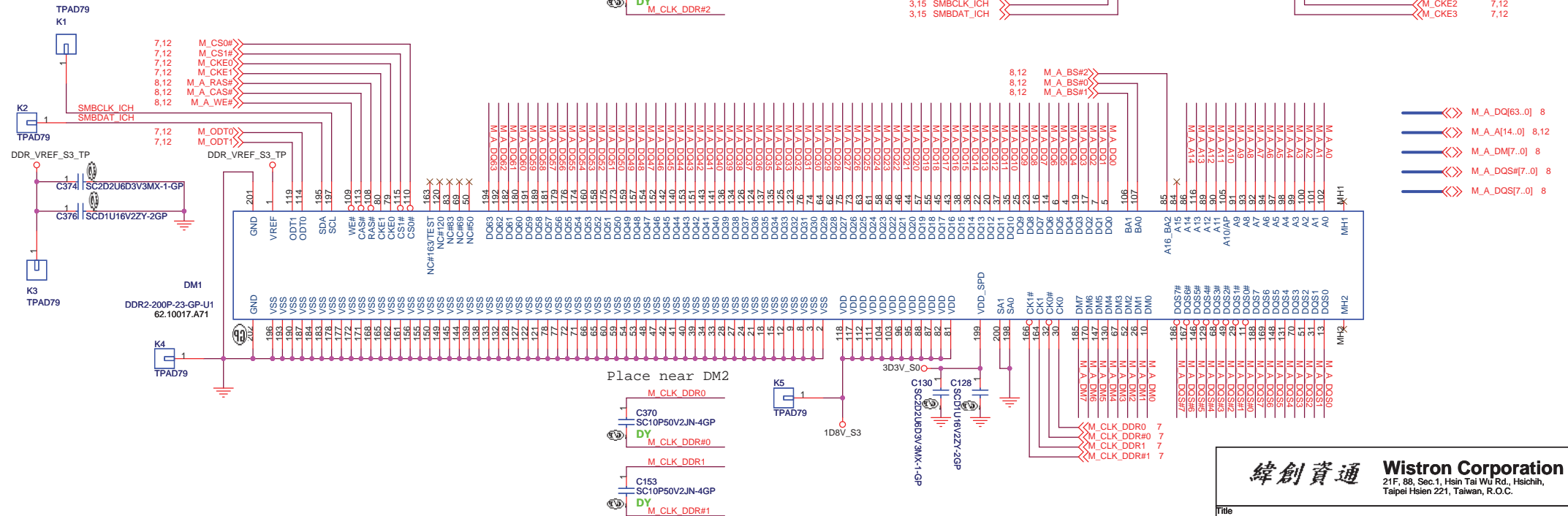


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Title			
GMCH (5 of 5) POWER2			
Size A3	Document Number	Rev SA	
C45/C46		Date: Tuesday, April 24, 2007	Sheet 10 of 45



SB ADD TEST PAD for Customer request



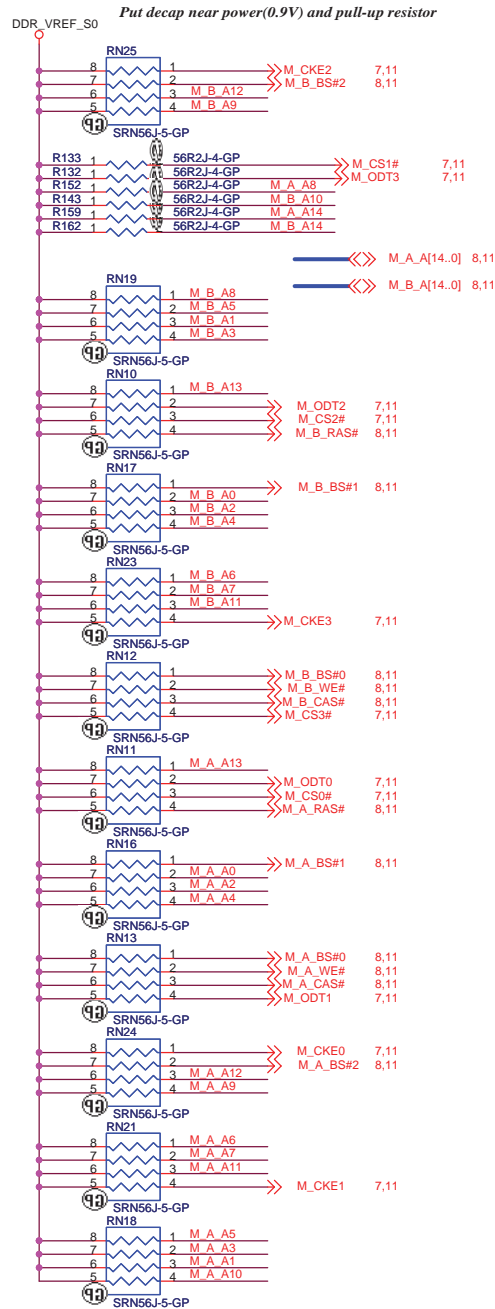
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR2-SOCKET**

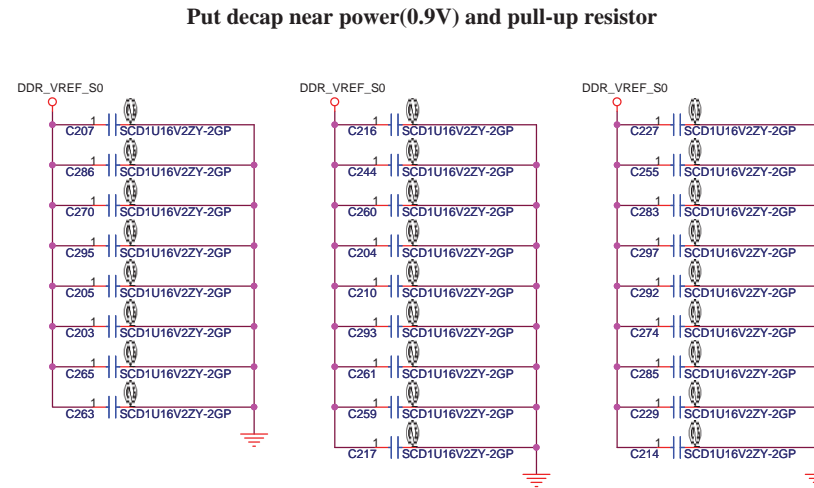
Size: Custom Document Number: **C45/C46** Rev: **SA**

Date: Wednesday, April 25, 2007 Sheet 11 of 45

PARALLEL TERMINATION



Decoupling Capacitor



Place these Caps near DM1



Place these Caps near DM2



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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR2-RESISTOR&CAPACITOR**

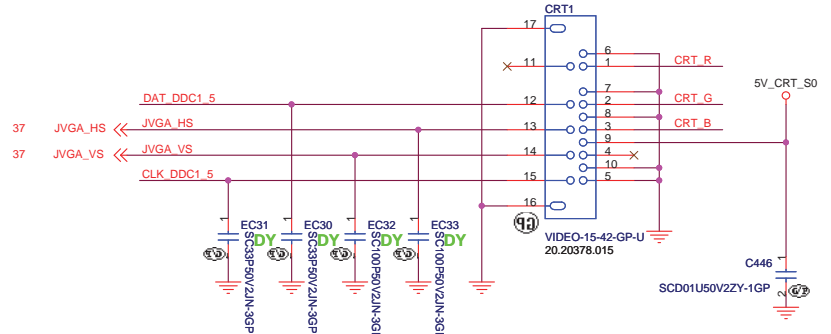
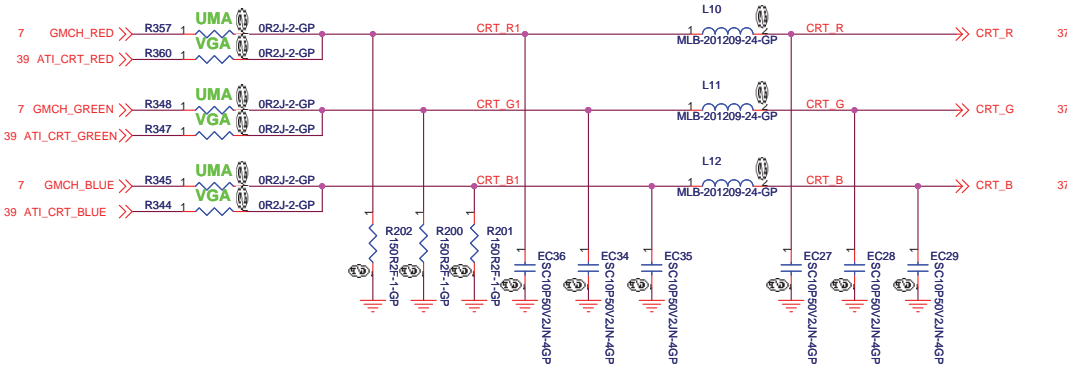
Size: Custom Document Number: **C45/C46** Rev: **SA**

Date: Wednesday, April 25, 2007 Sheet 12 of 45

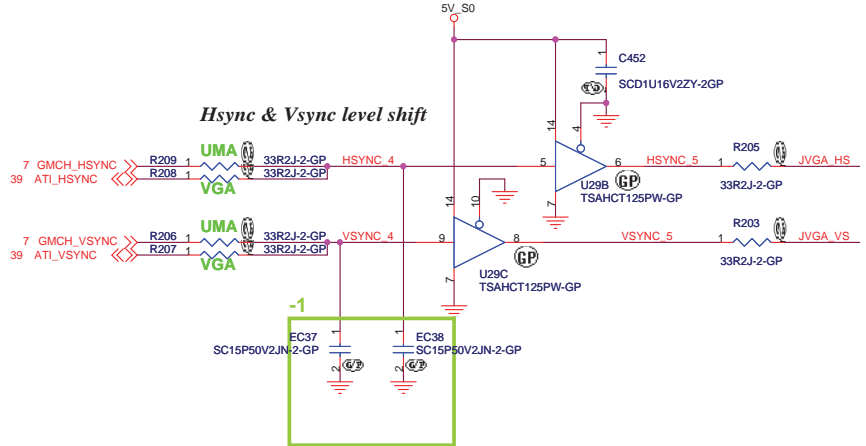
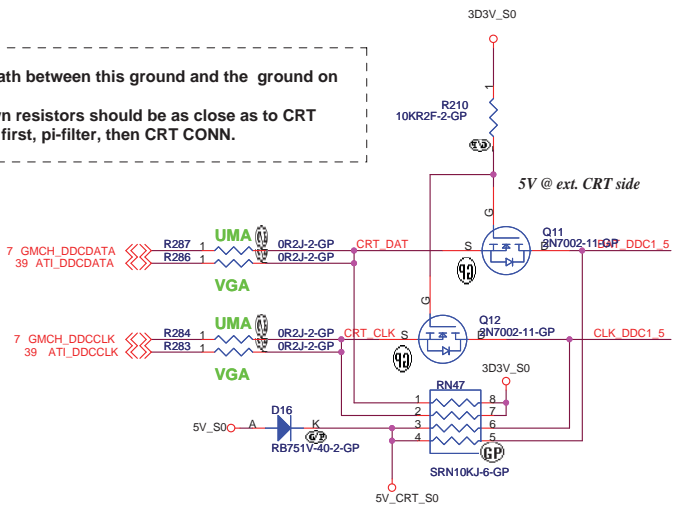
CRT CONNECTOR

Layout Note:
Place these resistors close to the CRT-out connector

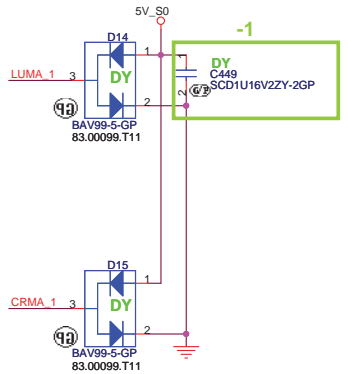
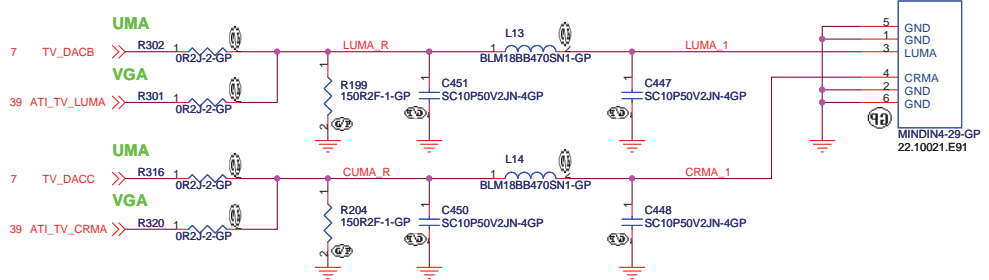
SB
Change L10, L11, L12 the same as X40



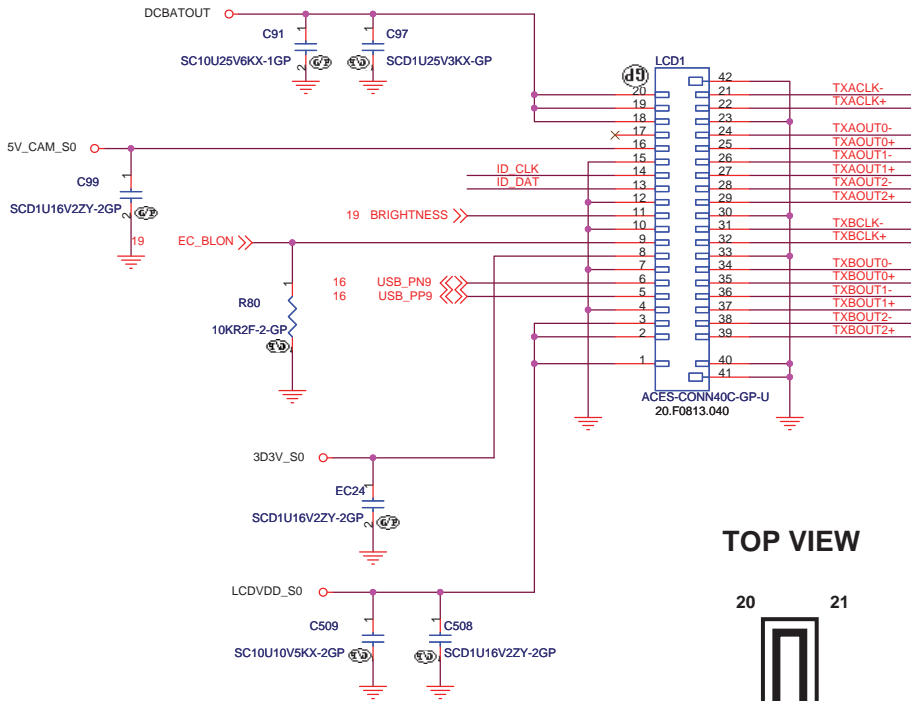
Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



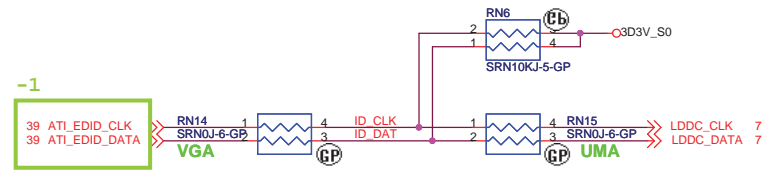
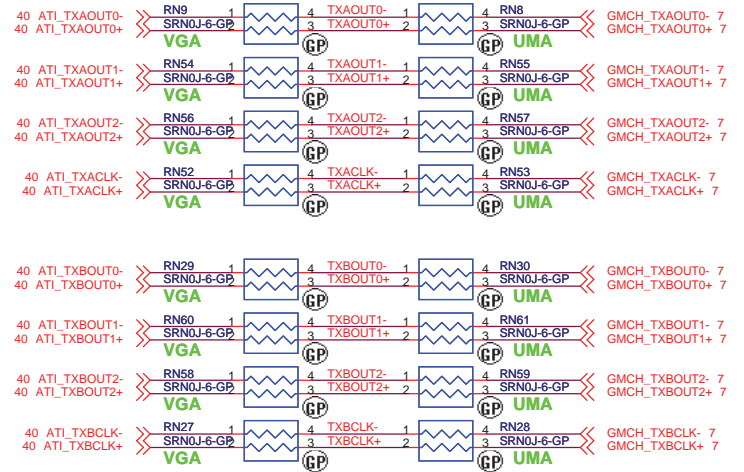
S-VIDEO CONNECTOR



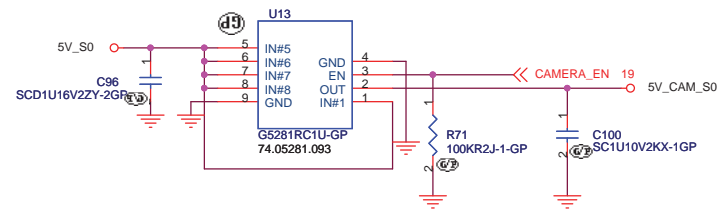
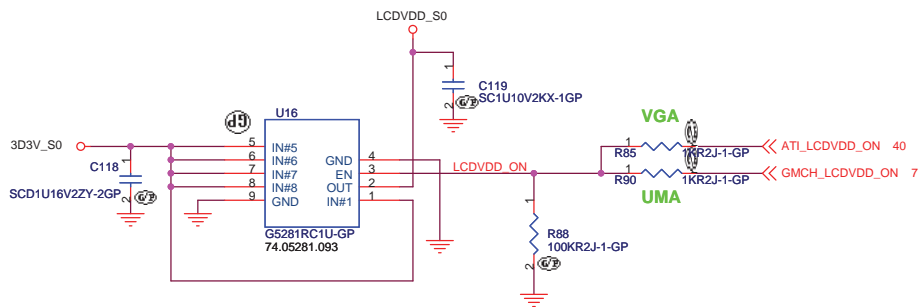
LCD CONNECTOR



TOP VIEW

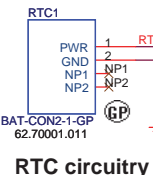
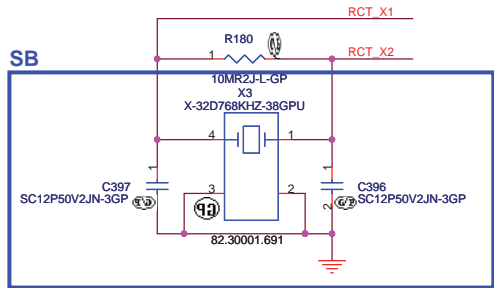


CAMERA POWER

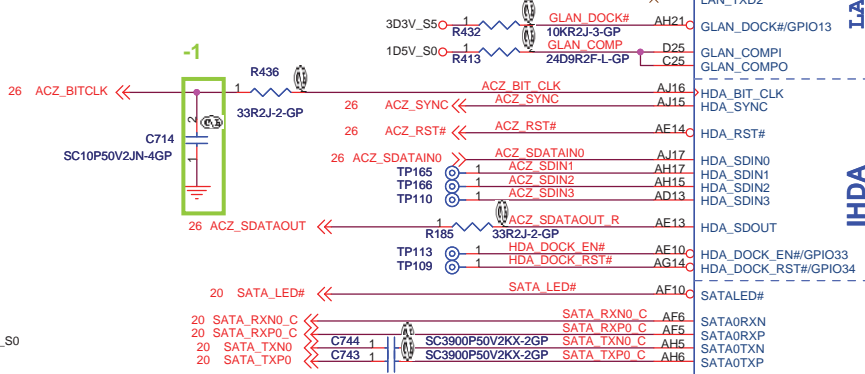


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Taipei Hsien 221, Taiwan, R.O.C.

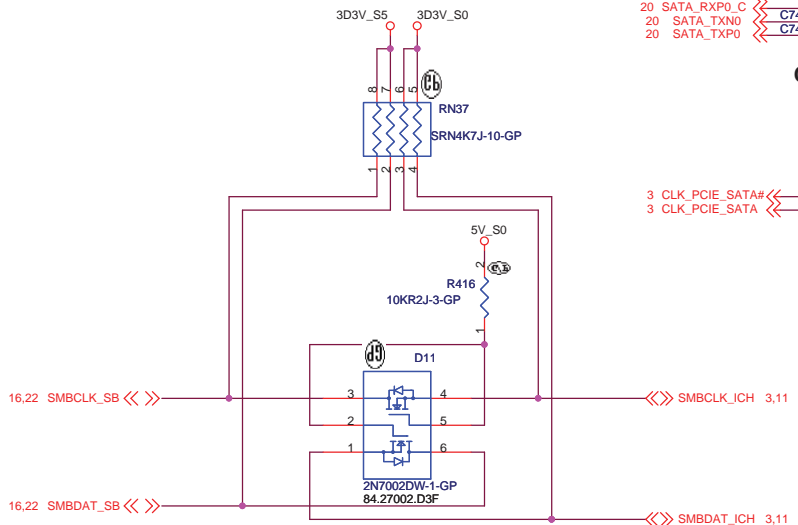
Title			LCD/DVI CONN		
Size	Document Number	C45/C46		Rev	SA
A3					
Date:	Thursday, April 26, 2007	Sheet	14	of	45



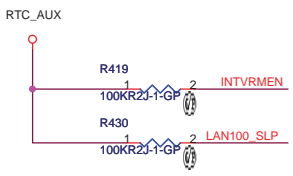
GLAN_COMP place within 500 mil of ICH8M



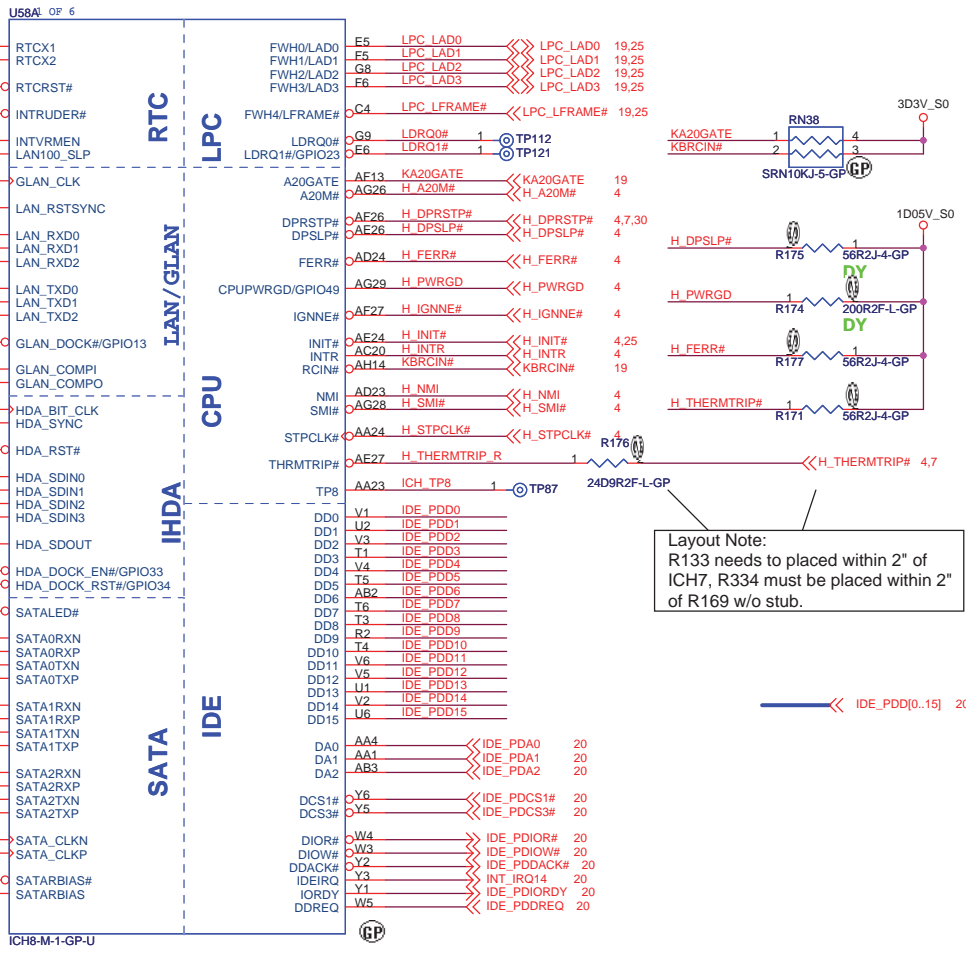
Close to SB



Place within 500 mils of ICH8 ball
Change to 24.9 1% ohm when use SATA HD



Integrated VccSus1_05,VccSus1_5,VccCl1_5		
INTVRMEN	High=Enable	Low=Disable
Integrated VccLan1_05VccCl1_05		
LAN100_SLP	High=Enable	Low=Disable



Layout Note:
R133 needs to be placed within 2" of ICH7, R334 must be placed within 2" of R169 w/o stub.

◀ IDE_PDD0[.15] 20

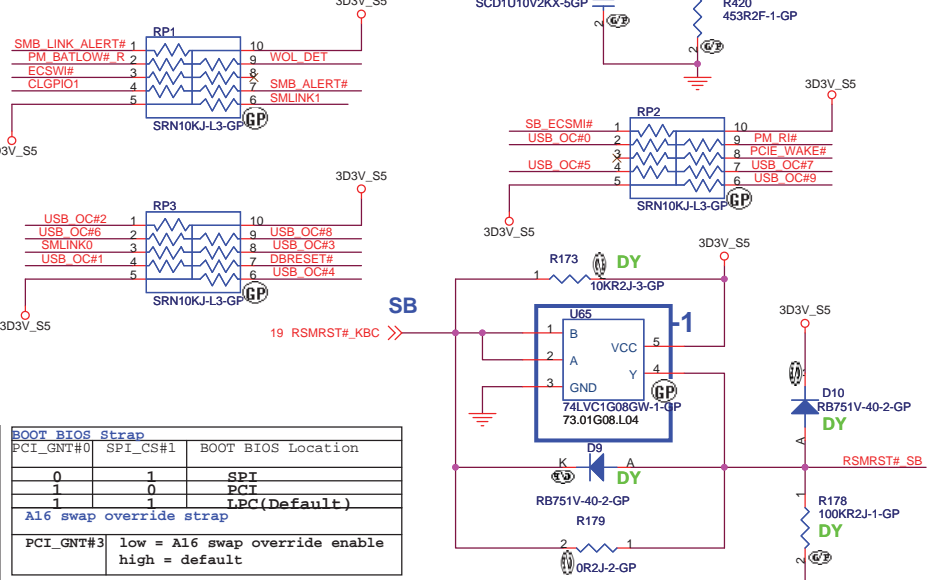
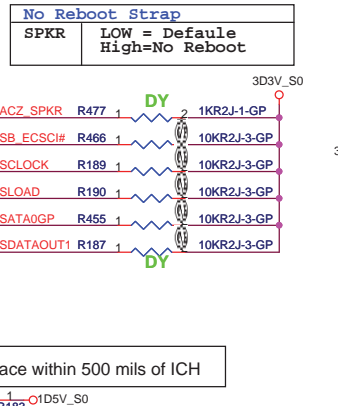
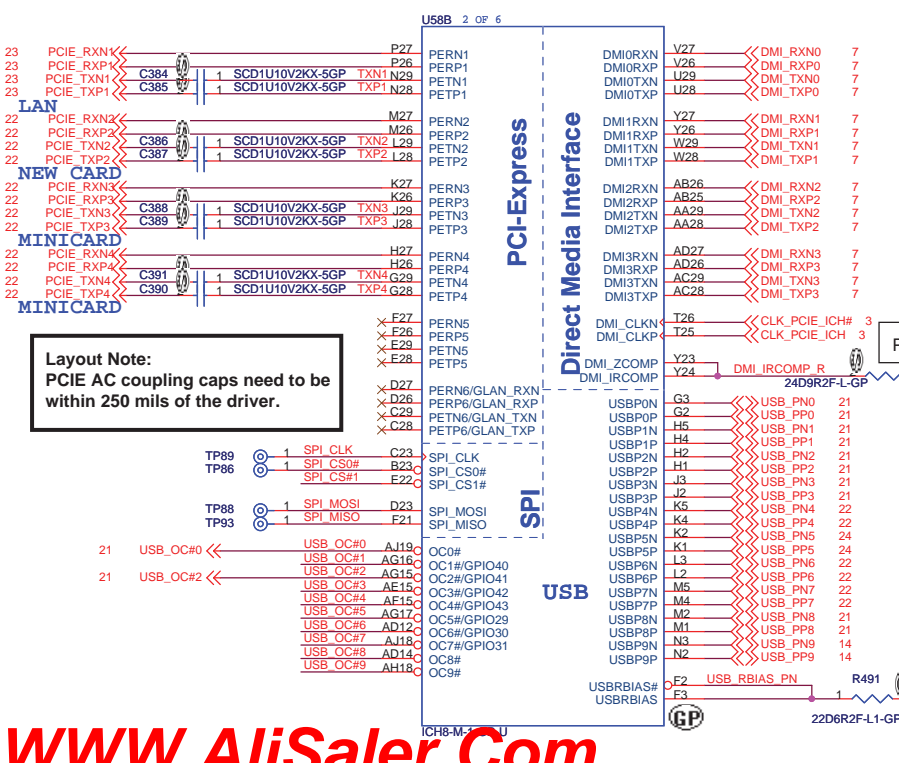
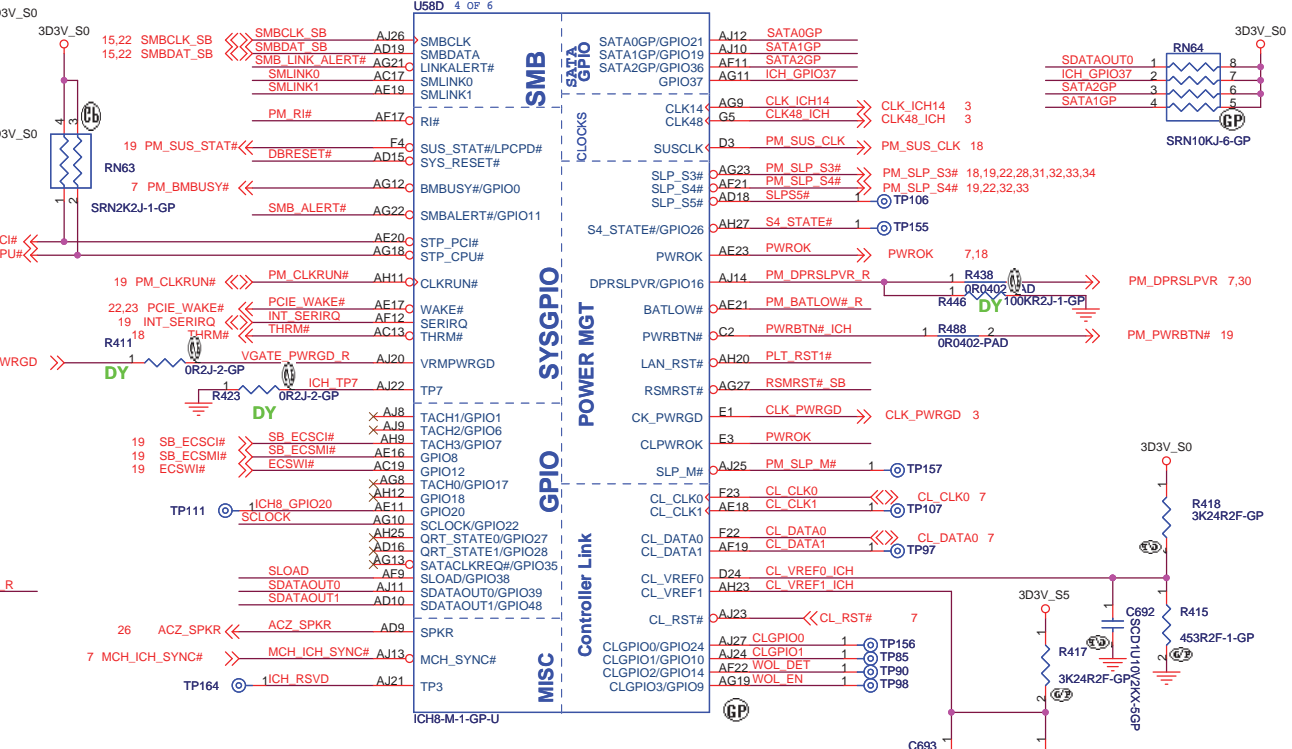
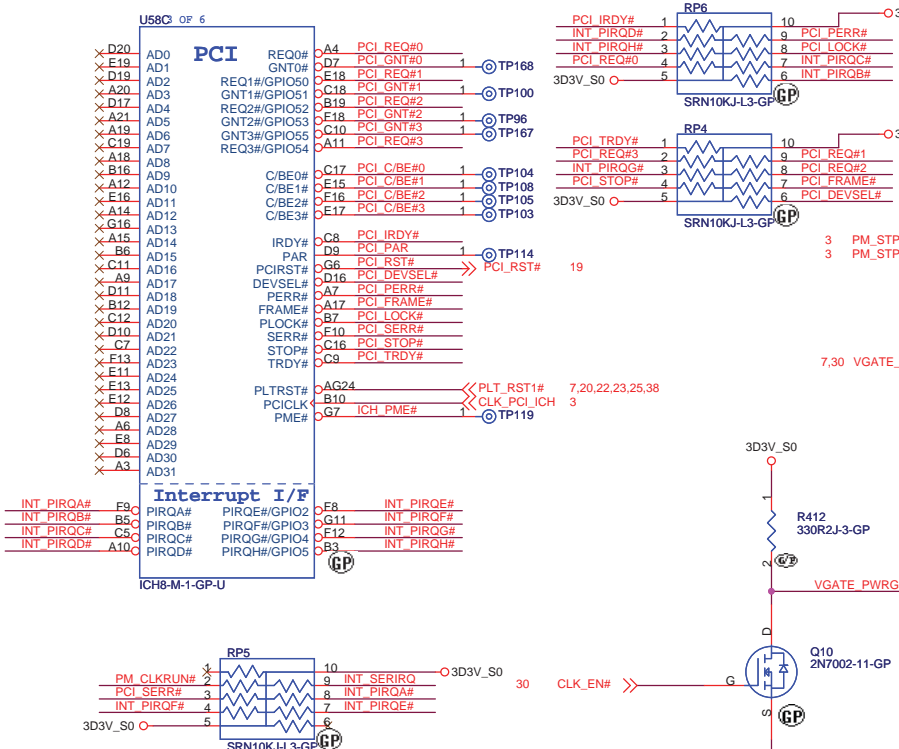
D55 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

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Title: **ICH8 (1 of 3) SATA/IDE/RTC**

Size Custom	Document Number	Rev
	C45/C46	SA

Date: Friday, April 27, 2007 Sheet 15 of 45



Layout Note:
 PCIe AC coupling caps need to be within 250 mils of the driver.

Pair	Device
0	USB1(ON BOARD)
1	USB2(EXT. USB)
2	USB3(EXT. USB)
3	USB4(EXT. USB)
4	MINICARD
5	USB Cardreader
6	MINICARD
7	NEW CARD
8	BLUETOOTH
9	WEBCAM

PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPT
1	0	PCT
1	1	LPC(Default)

A16 swap override strap

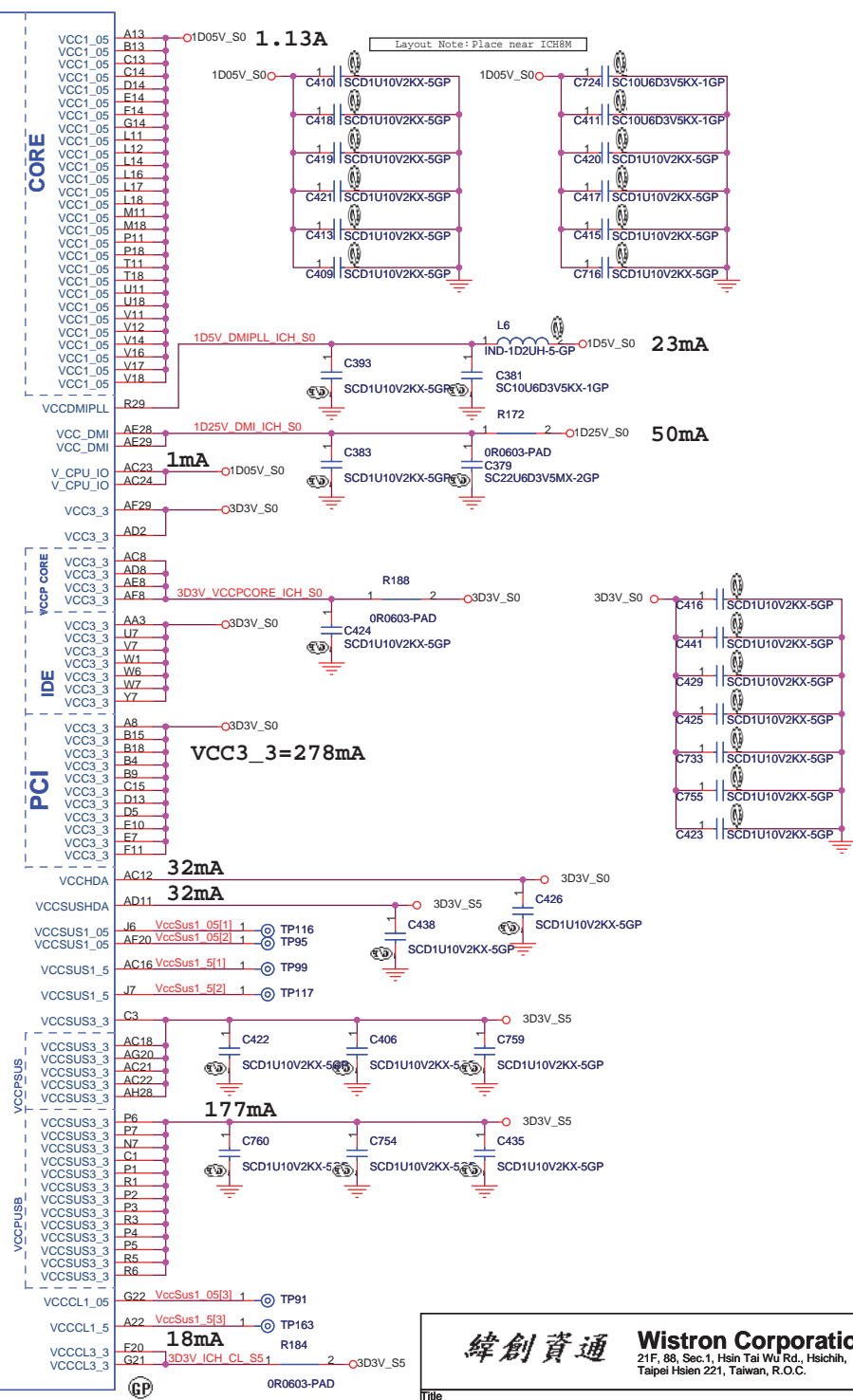
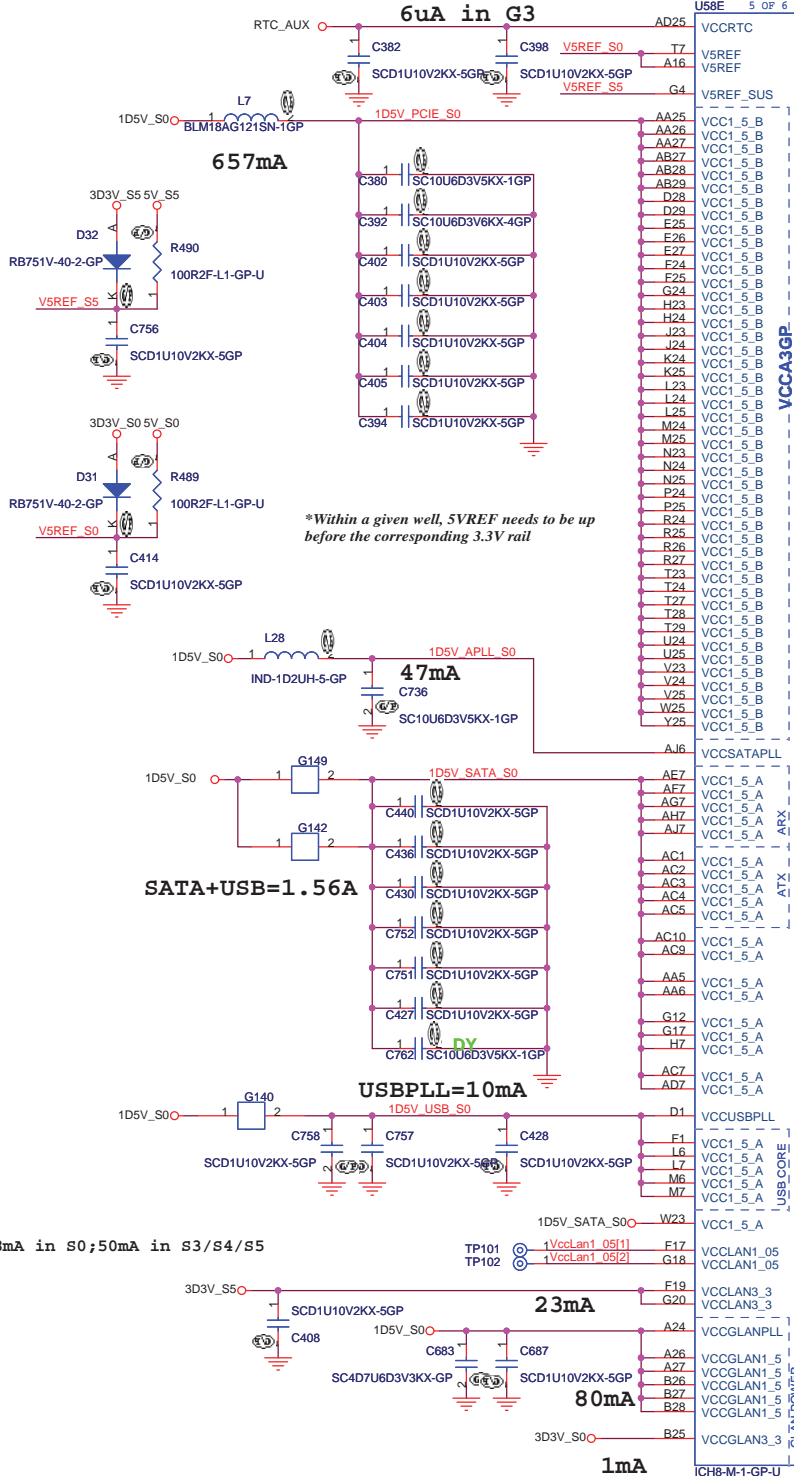
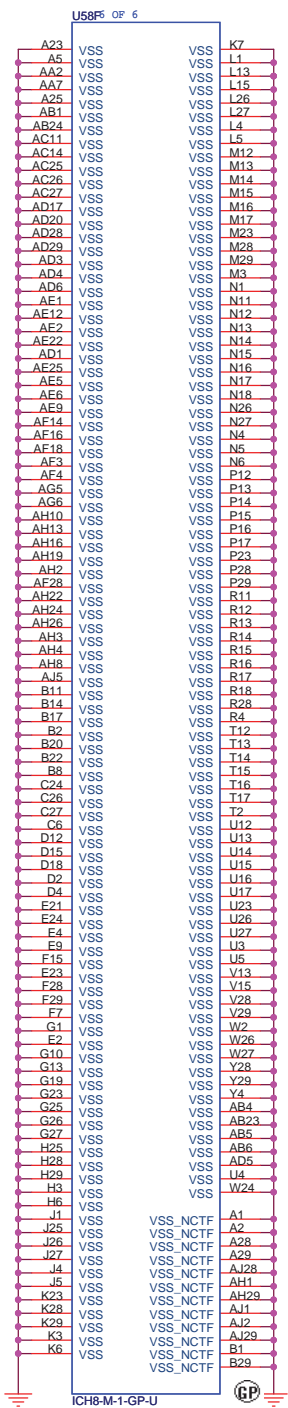
PCI_GNT#3 low = A16 swap override enable
 high = default

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Title: **ICH8 (2 of 3) DMI/PCIE/USB**

Size: Custom Document Number: **C45/C46** Rev: SA

Date: Wednesday, April 25, 2007 Sheet 16 of 45

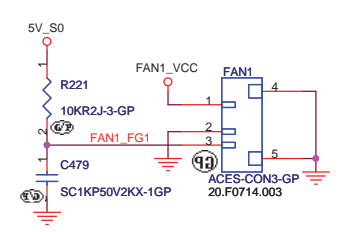
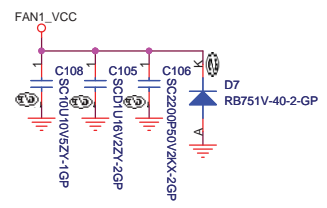
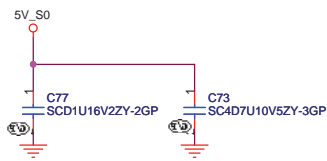


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Title: **ICH8 (3 of 3) POWER**

Size: Custom Document Number: **C45/C46** Rev: **SA**

Date: Tuesday, April 24, 2007 Sheet: 17 of 45

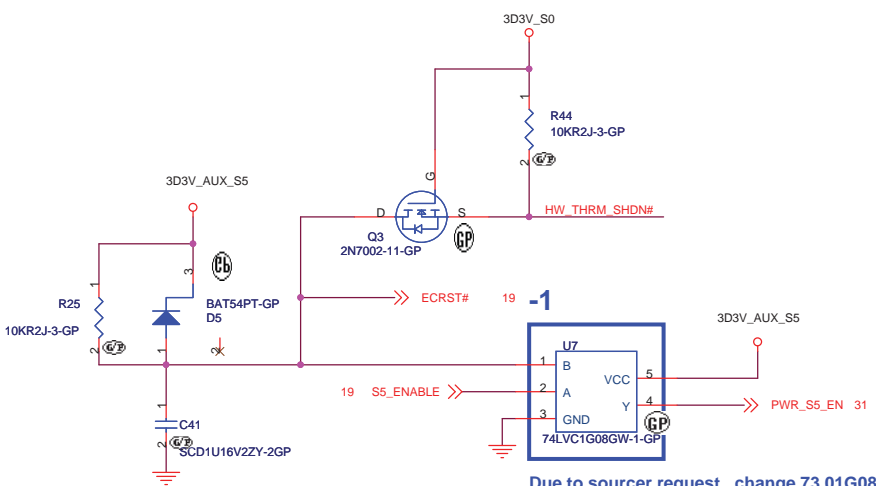
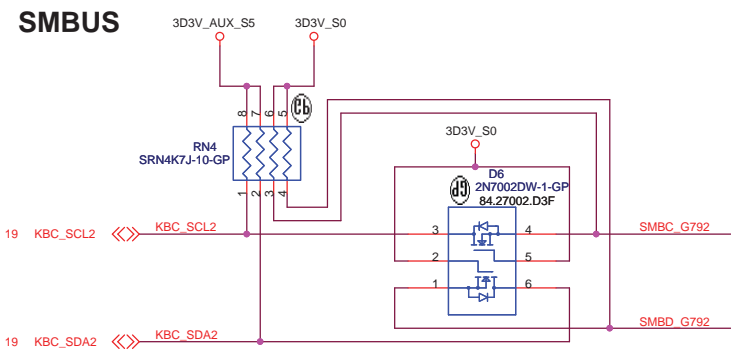
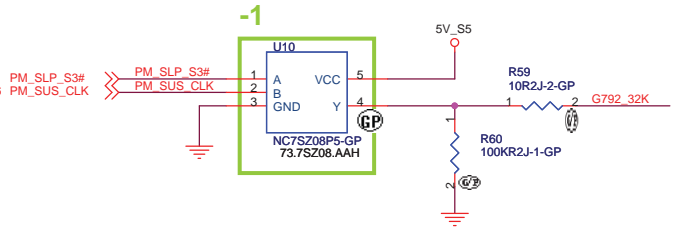
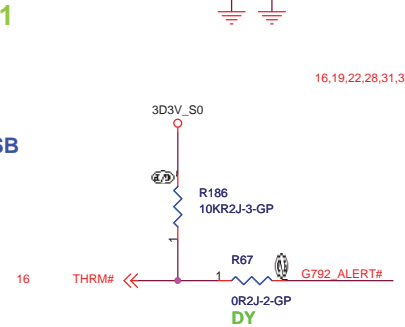
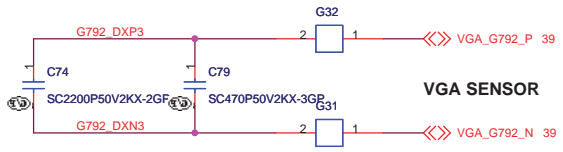
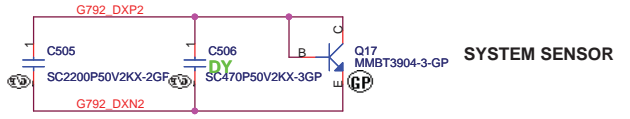
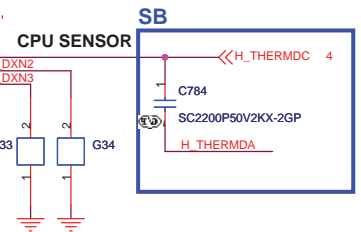
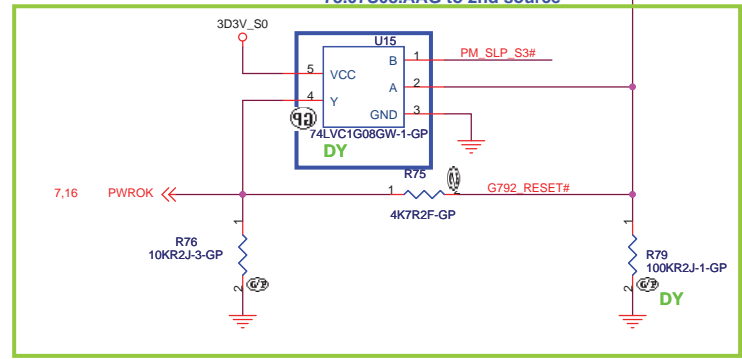


Setting T8 as 100 Degree

$$V_DEGREE = (((Degree - 72) * 0.02) + 0.34) * VCC$$

DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree

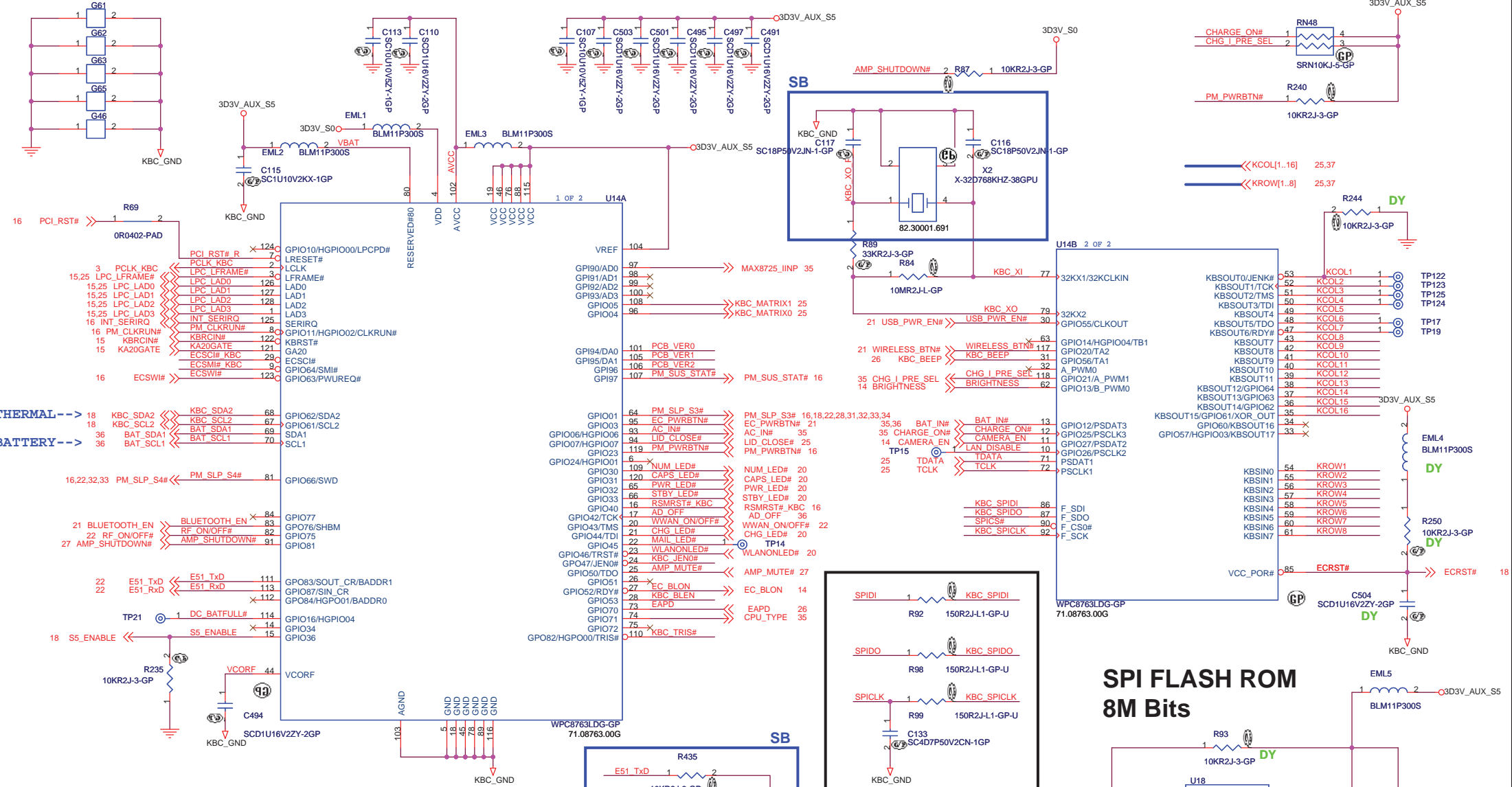
Due to sourcer request, change 73.01G08.L04 to main source, 73.07S08.AAG to 2nd source



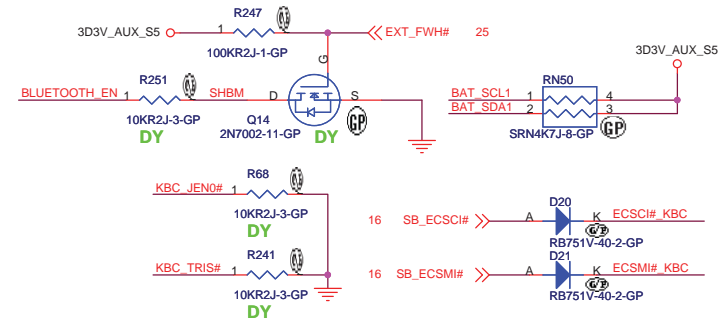
Due to sourcer request, change 73.01G08.L04 to main source, 73.07S08.AAG to 2nd source

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Title		
THERMAL G792		
Size	Document Number	Rev
A3	C45/C46	SA
Date:	Thursday, April 26, 2007	Sheet 18 of 45

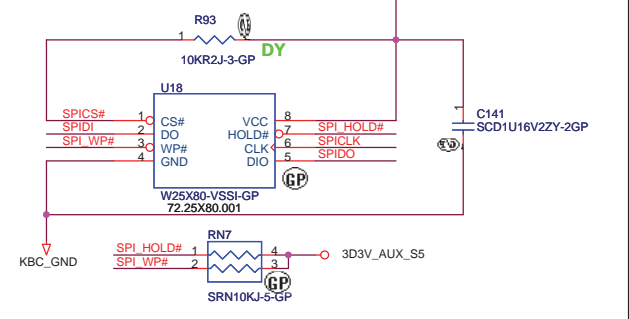


FOR KBC STRAPPING



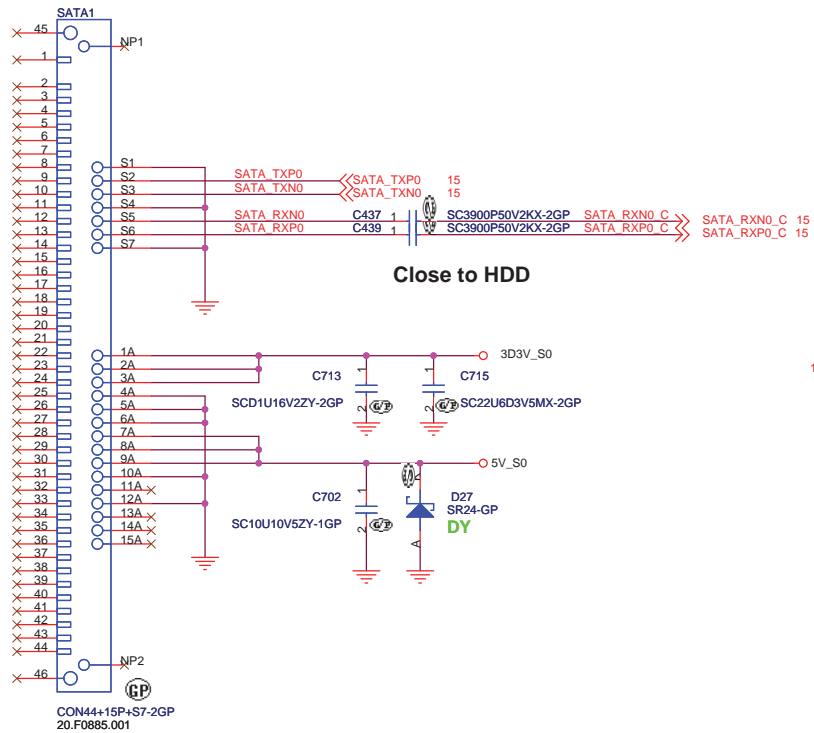
PlanarID (2,1,0)(Model, Stage)
C45 C46
 SA: 0,0 SA: 1,0
 SB: 0,0,1 SB: 1,0,1
 -1: 0,1,0 -1: 1,1,0

SPI FLASH ROM 8M Bits

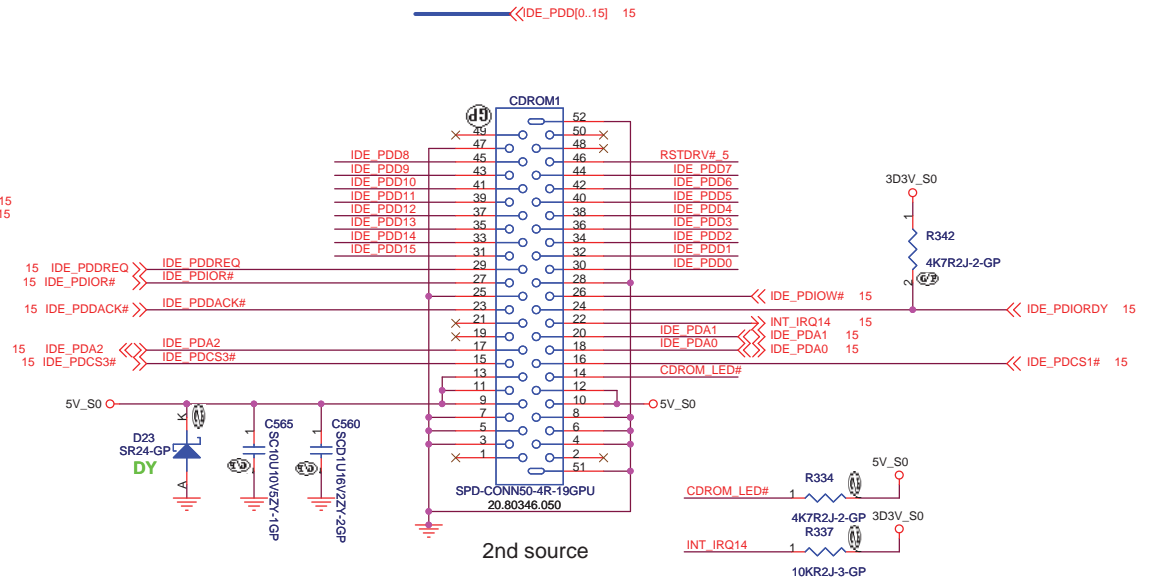


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Title KBC_WPC8763L	
Size A3	Document Number C45/C46
Date: Wednesday, April 25, 2007	Sheet 19 of 45

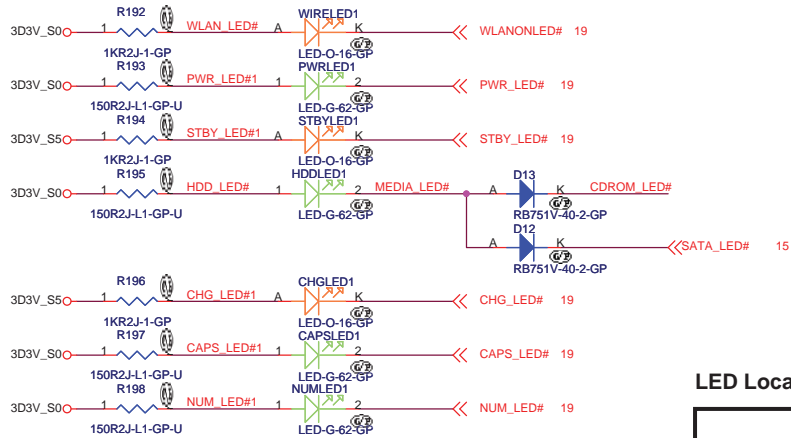
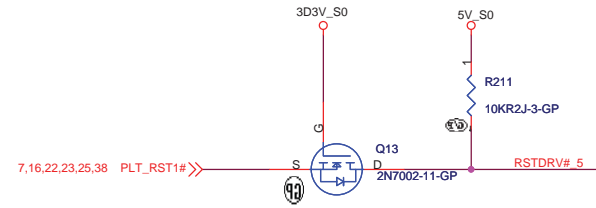
SATA HDD Connector



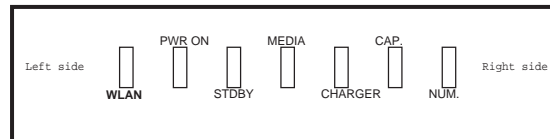
CD-ROM CONNECTOR



PCIRST# 3V to 5V level shift for HDD & CDROM



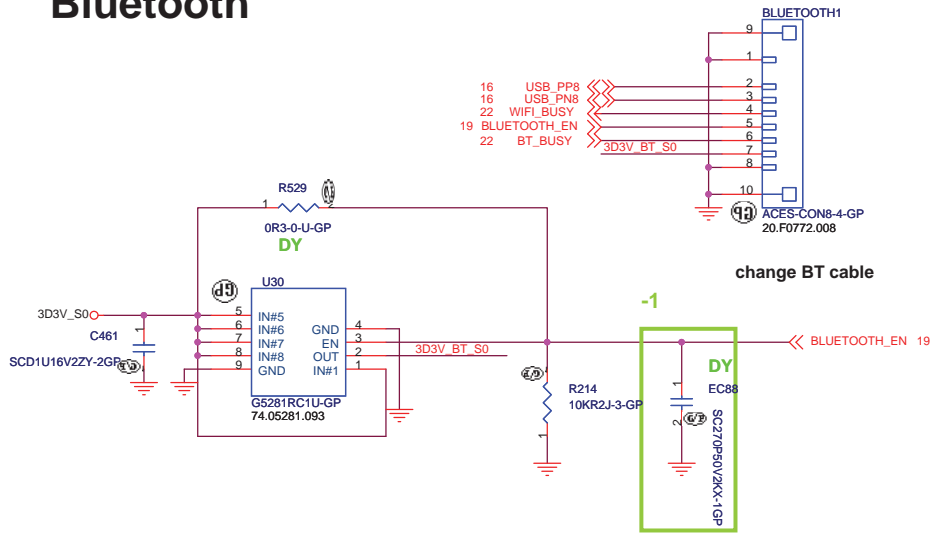
LED Location and Sequence (The edge of PCB,Top view)



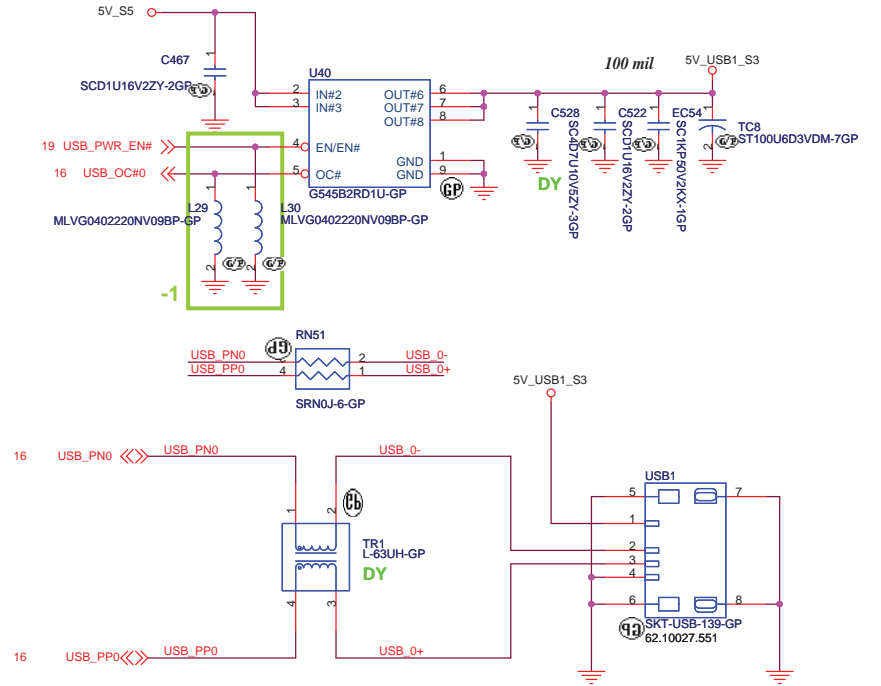
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
HDD/CDROM/LED		
Size	Document Number	Rev
Custom	C45/C46	SA
Date:	Wednesday, April 25, 2007	Sheet 20 of 45

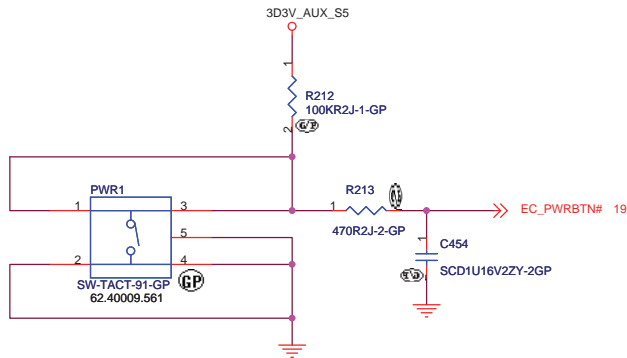
Bluetooth



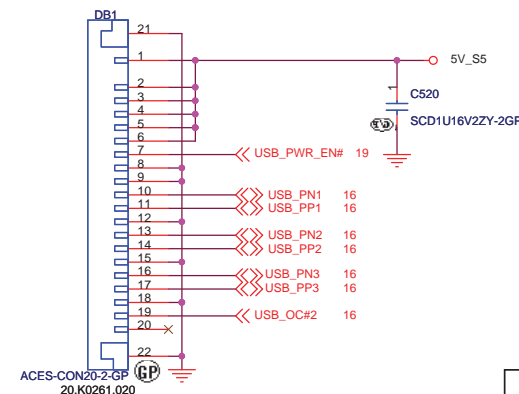
USB PORT



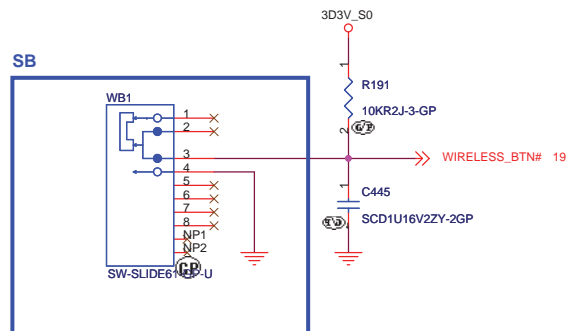
LAUNCH BOTTON



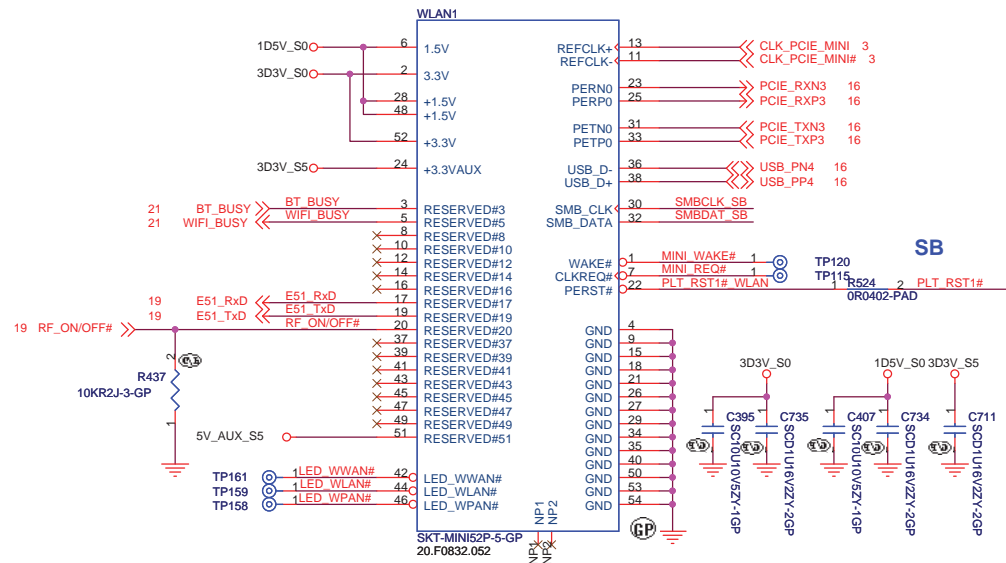
USB BOARD CONN



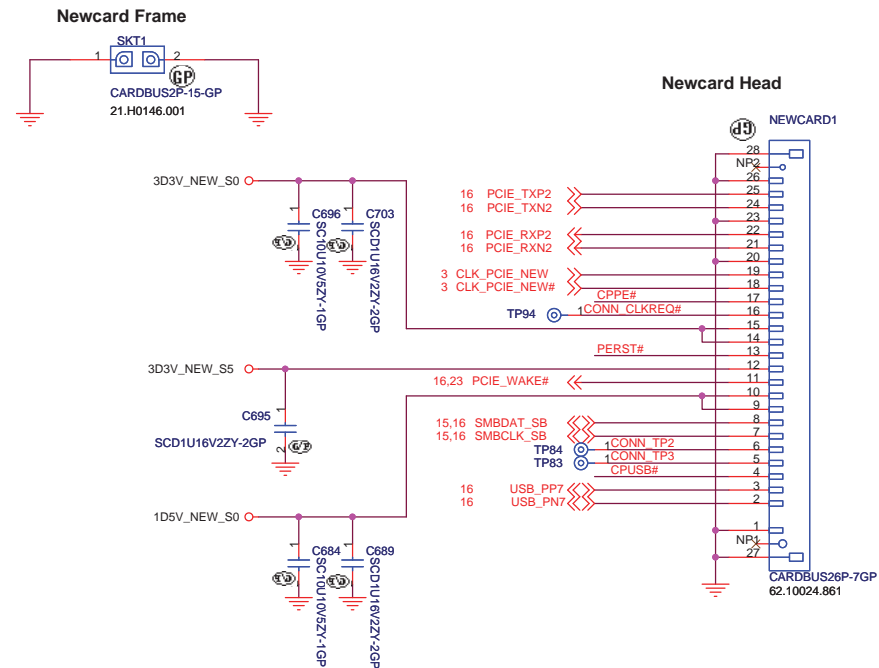
WIRELESS BOTTON



Mini Card Connector

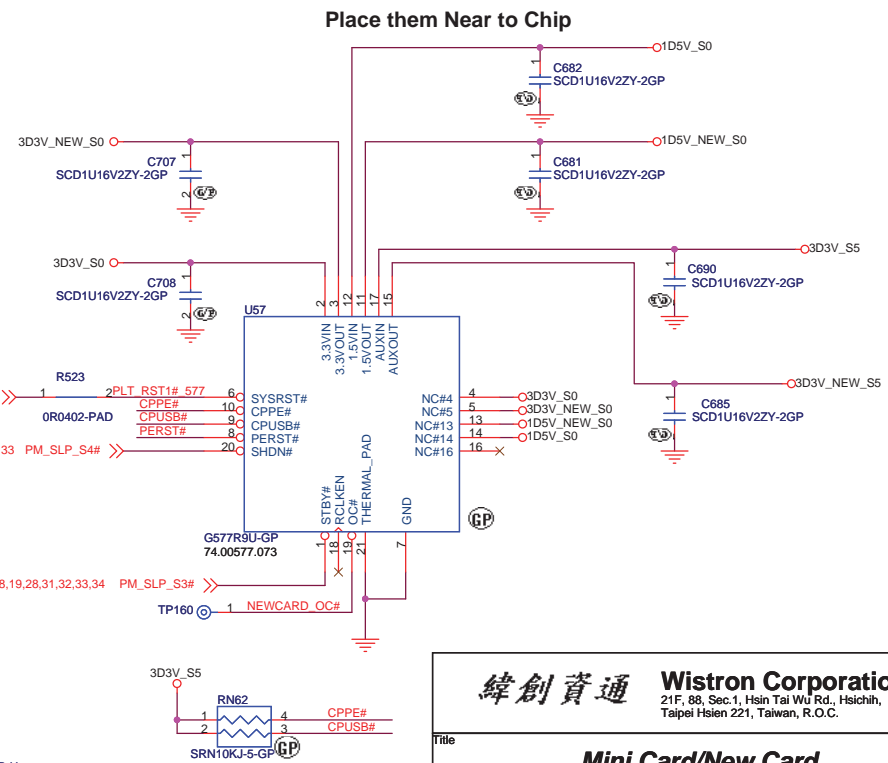
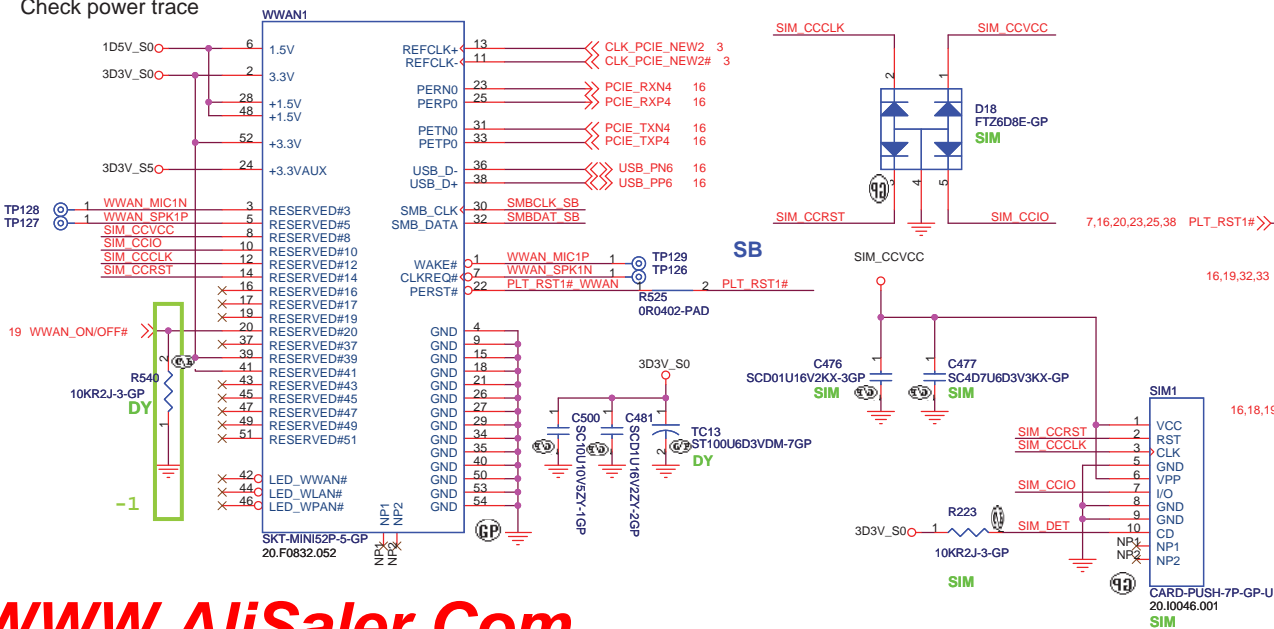


NEWCARD Connector



WWAN Connector

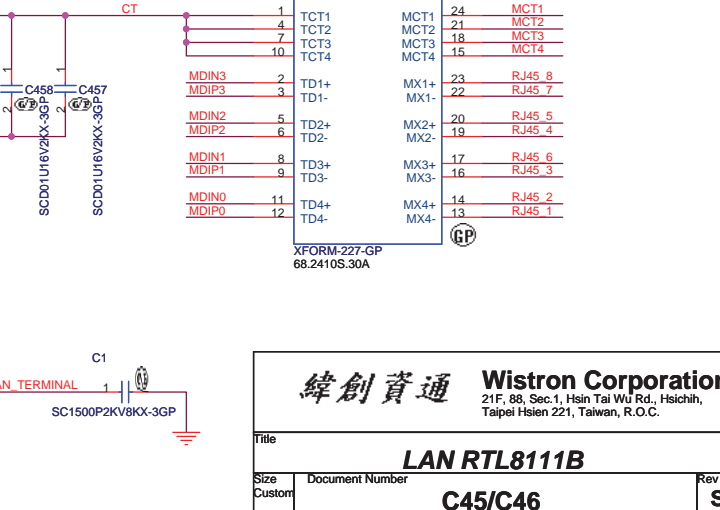
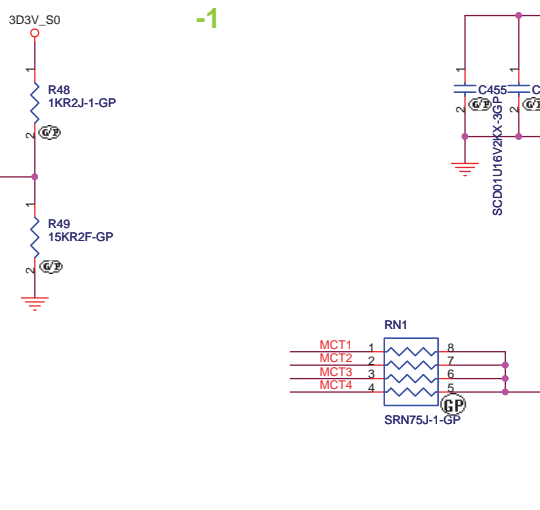
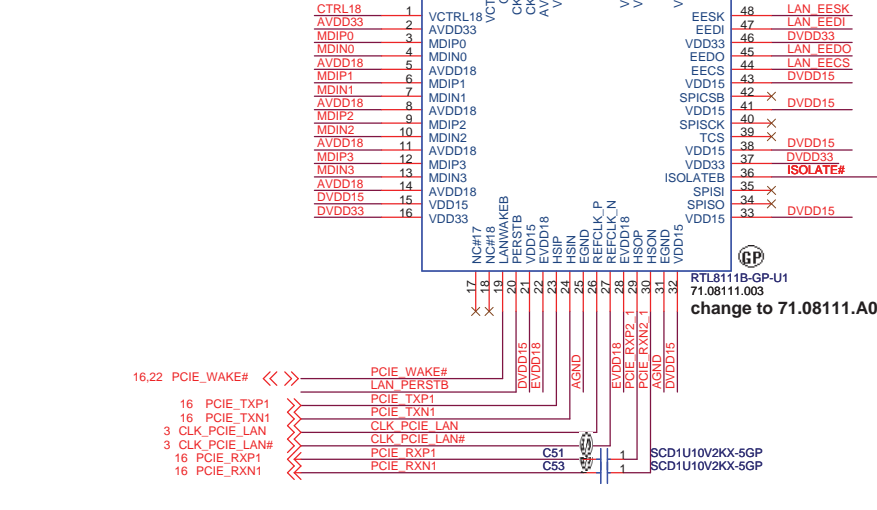
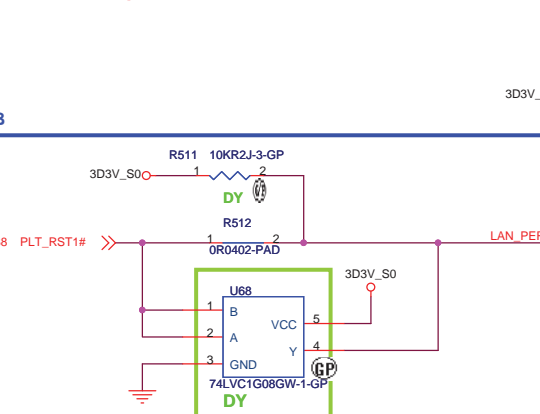
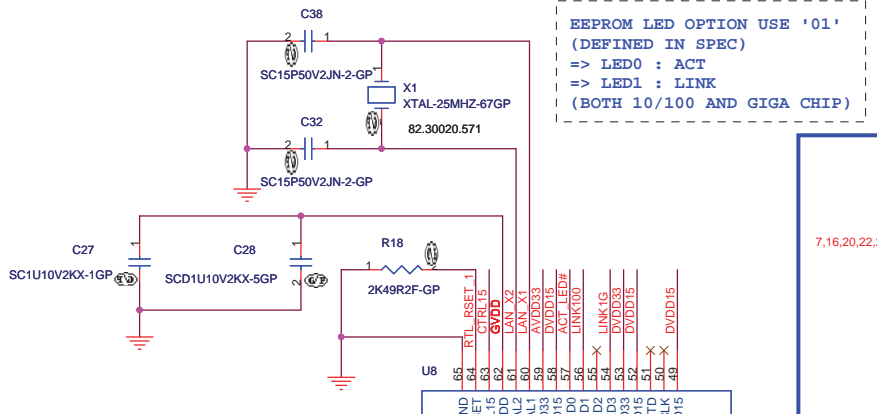
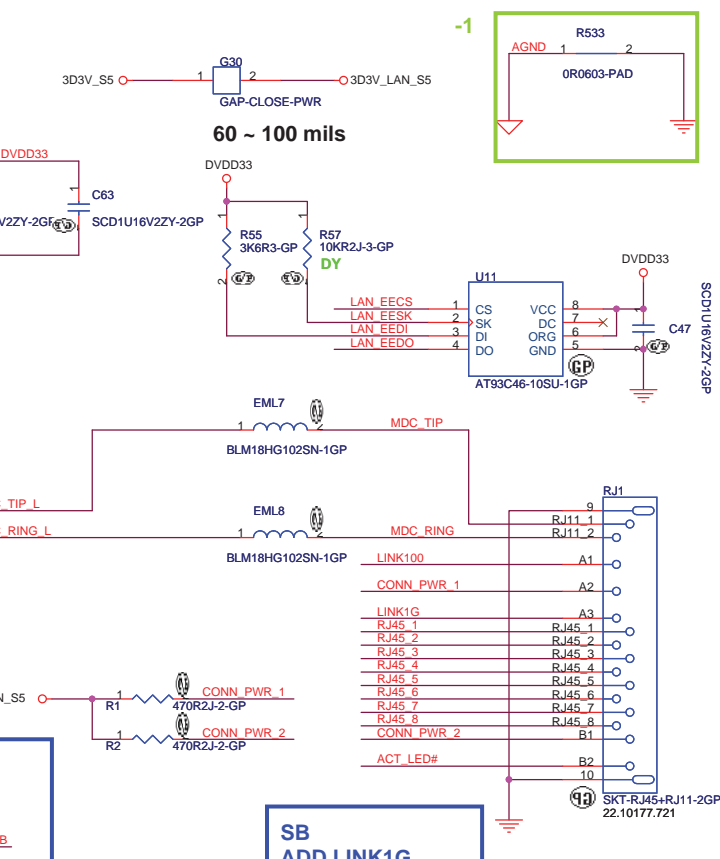
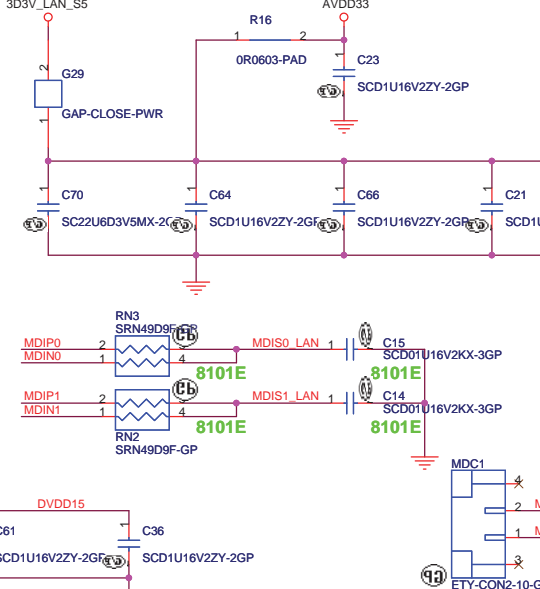
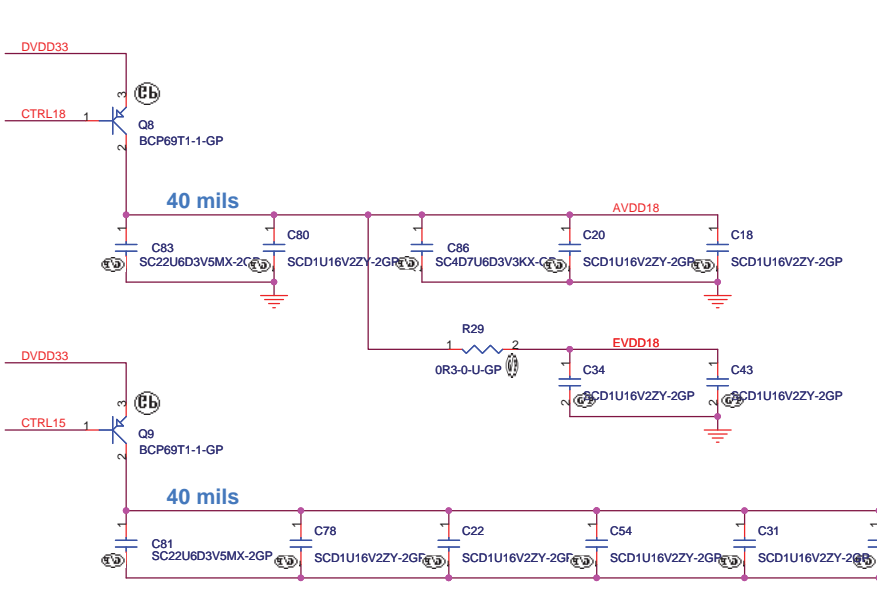
Check power trace



Place them Near to Chip

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Title		
Mini Card/New Card		
Size	Document Number	Rev
Custom	C45/C46	SA
Date:	Thursday, April 26, 2007	Sheet 22 of 45



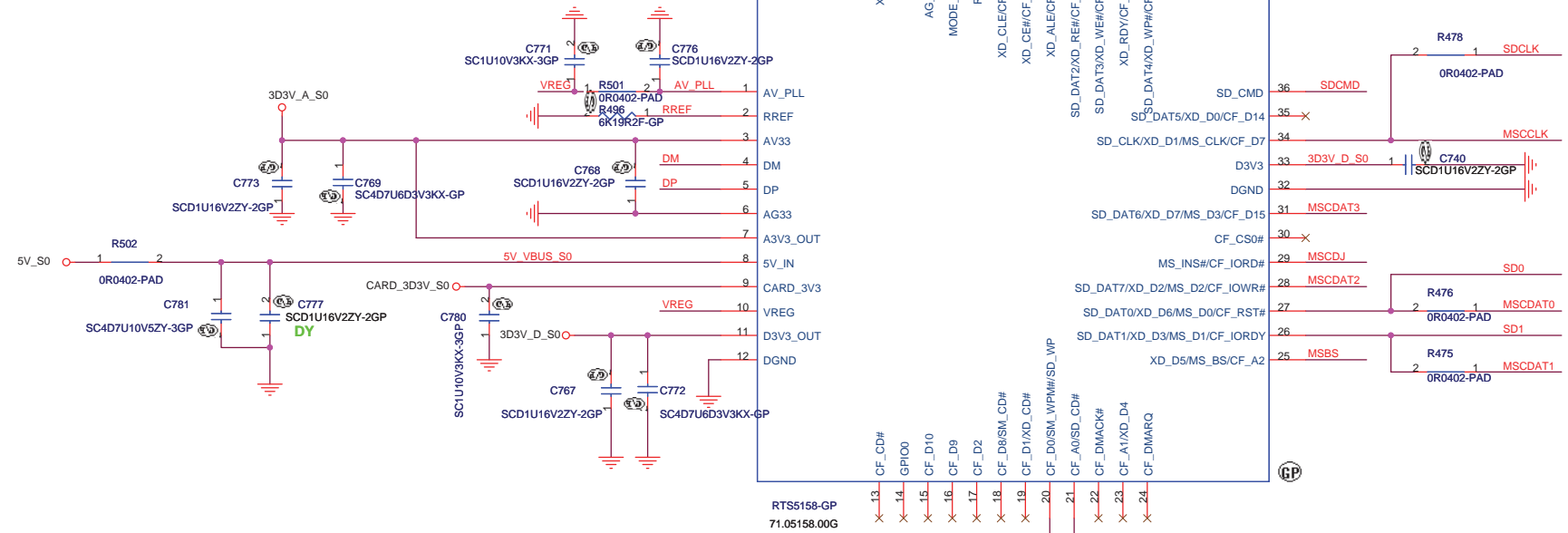
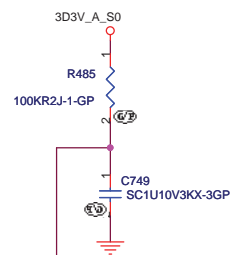
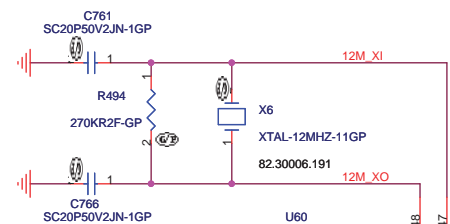
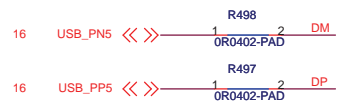
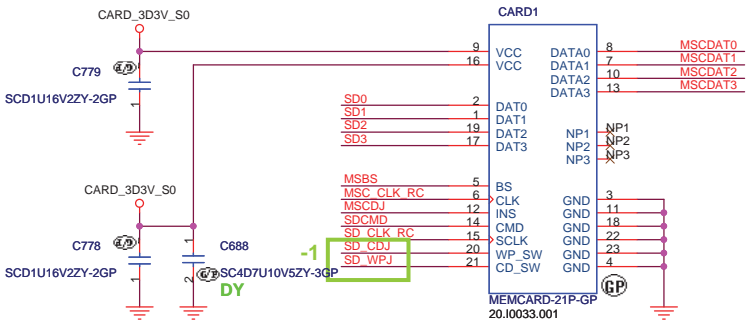
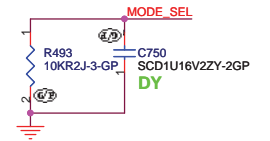
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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN RTL8111B**

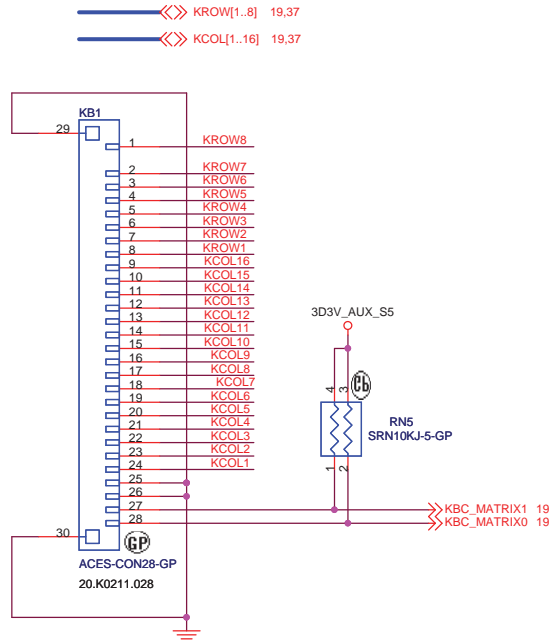
Size: Custom, Document Number: **C45/C46**, Rev: **SA**

Date: Thursday, April 26, 2007, Sheet 23 of 45

MS / MS PRO
SD / MMC



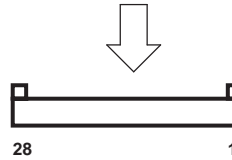
Internal Keyboard Connector



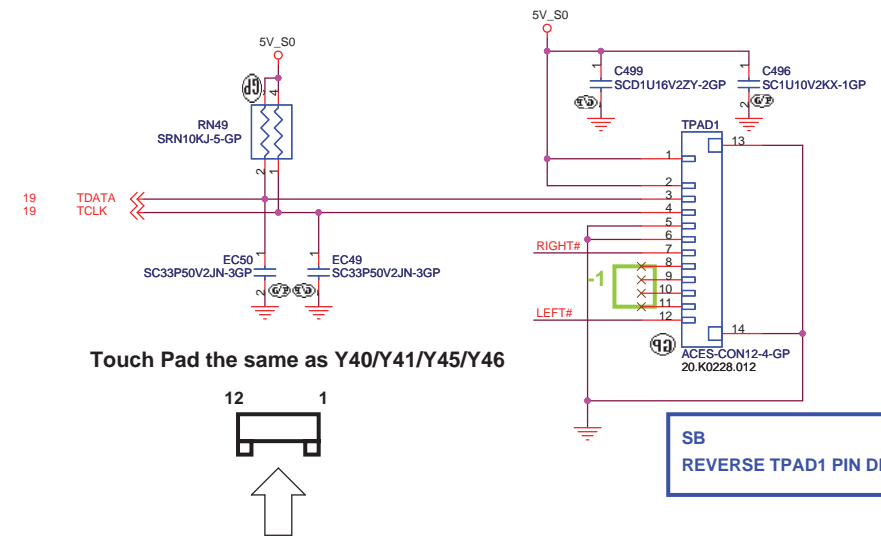
KEYBOARD MARTIX the same as Y40/Y41/Y45/Y46

Keyboard matrix (from vendor)

	US	Eur	Jap	Ohter
MATRIXID0#	1	0	1	0
MATRIXID1#	1	1	0	0



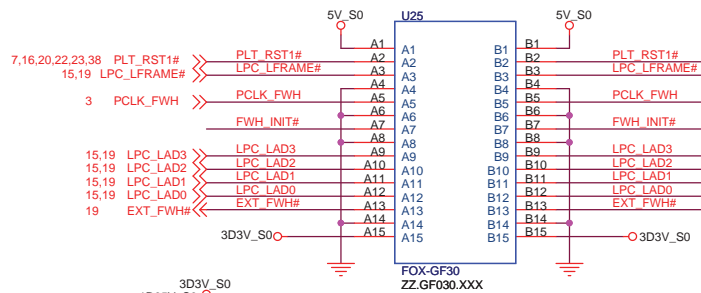
TouchPad Connector



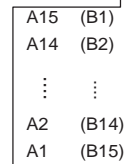
Touch Pad the same as Y40/Y41/Y45/Y46



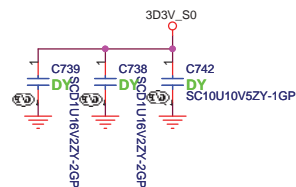
GOLDEN FINGER FOR DEBUG BOARD



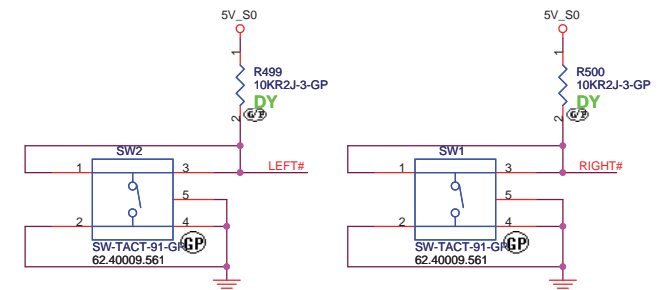
TOP VIEW



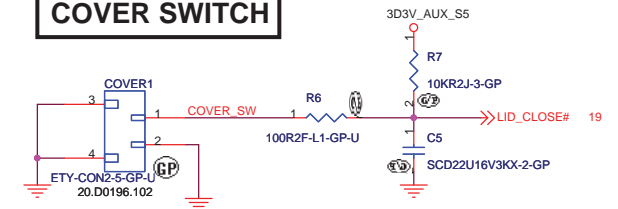
(BOTTOM VIEW)



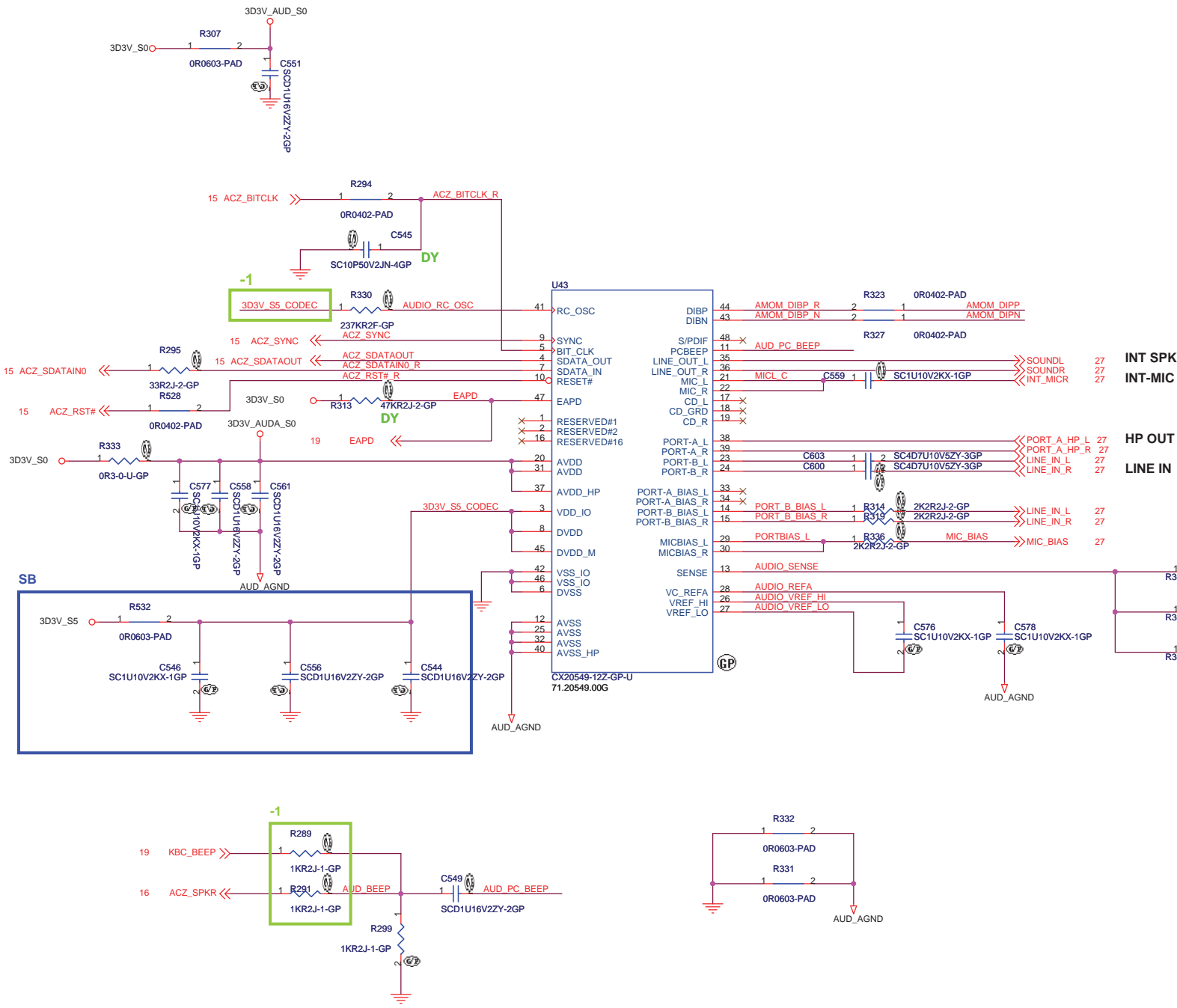
15" TOUCHPAD BUTTON SWITCH



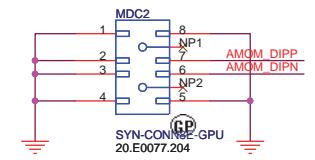
COVER SWITCH



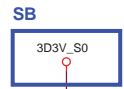
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MDC CONN



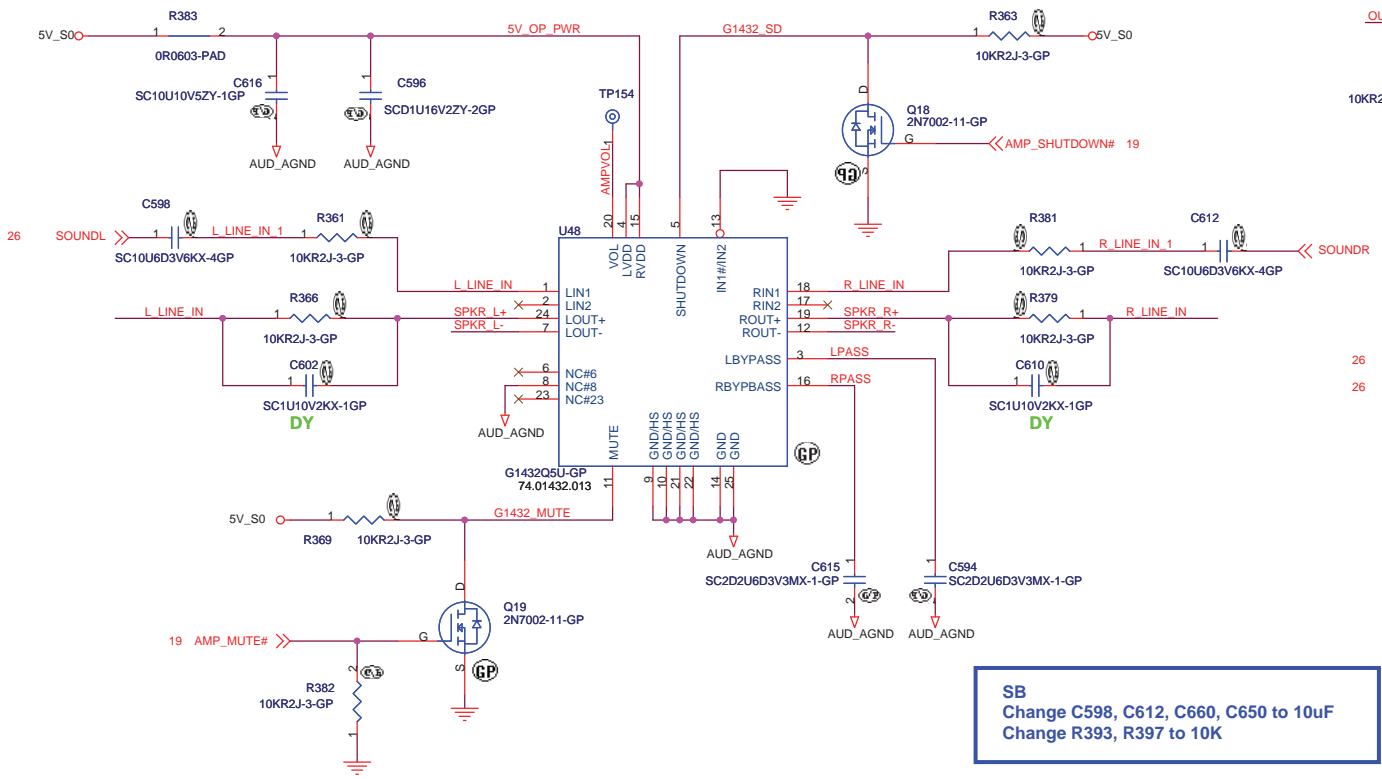
check pin define



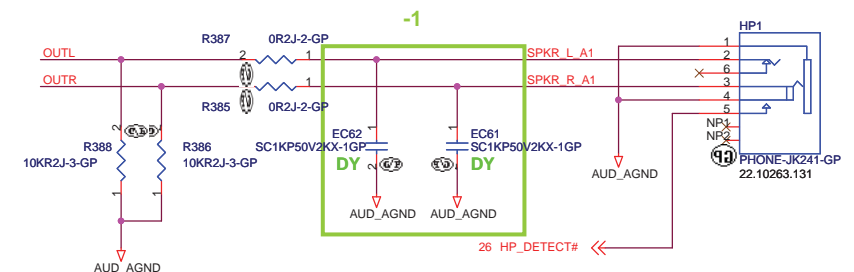
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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO CODEC CX20549-12Z/MDC**
 Size: Document Number
 Custom: C45/C46
 Date: Thursday, April 26, 2007
 Sheet: 26 of 45
 Rev: SA

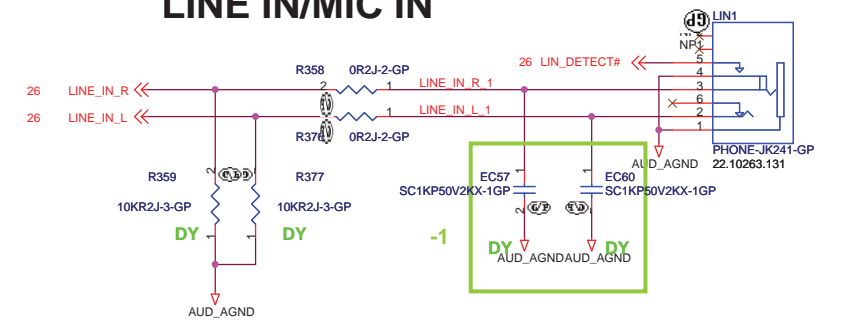
AUDIO AMPLIFIER



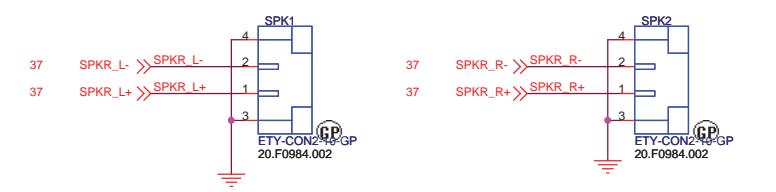
Headphone OUT



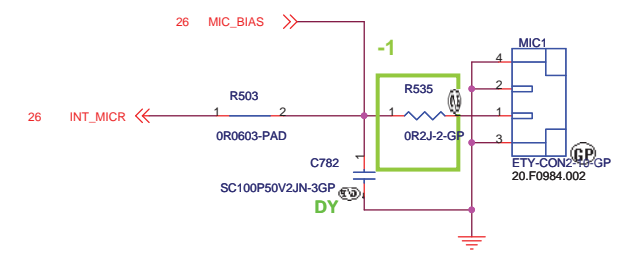
LINE IN/MIC IN



Internal Speaker



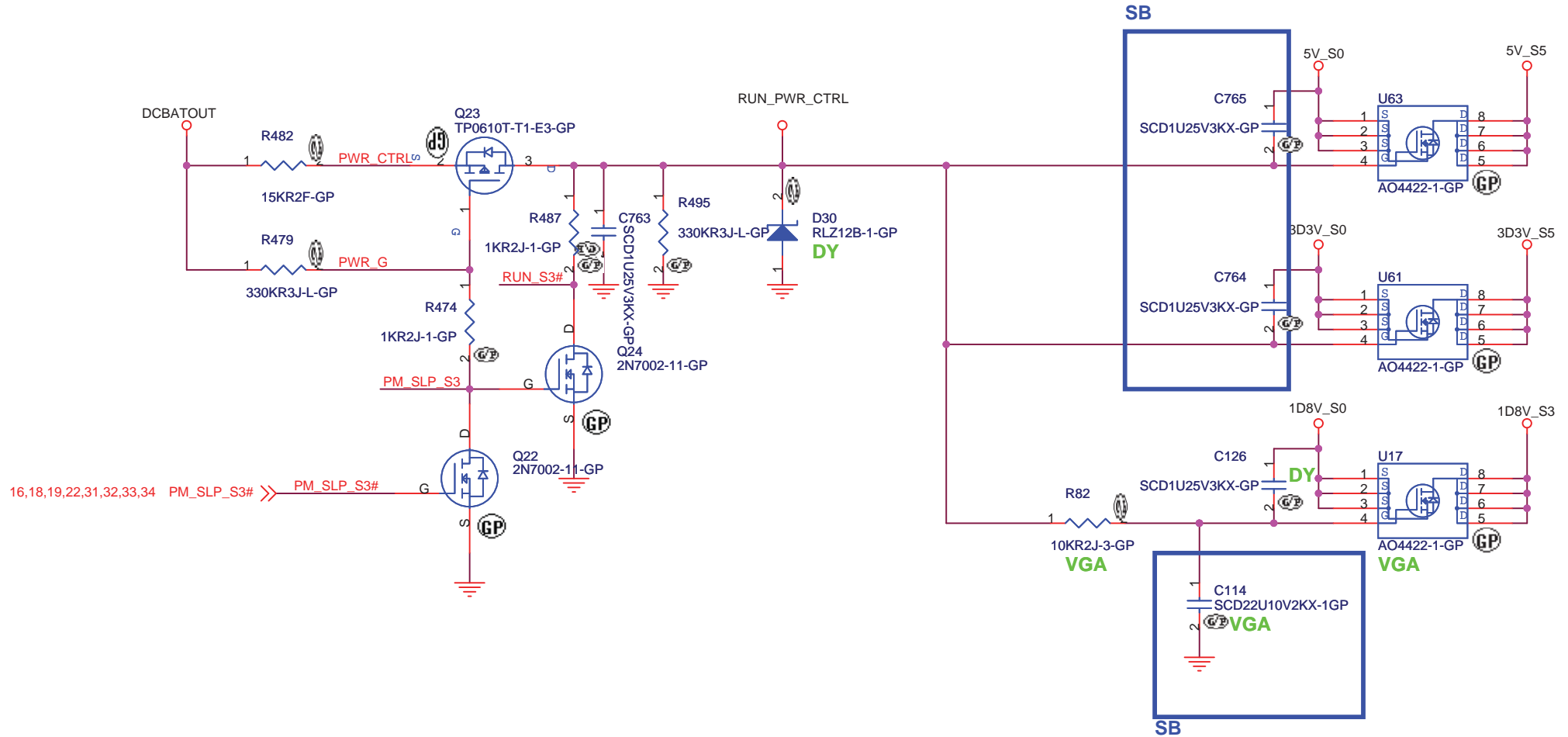
Internal MIC



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Title: **Audio AMP(G1432)& JACK**
 Size A3 Document Number: **C45/C46** Rev SA
 Date: Thursday, April 26, 2007 Sheet 27 of 45

Run Power



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Title **RUN POWER / CTRL LOGIC**

Size A4 Document Number

C45/C46

Rev **SA**

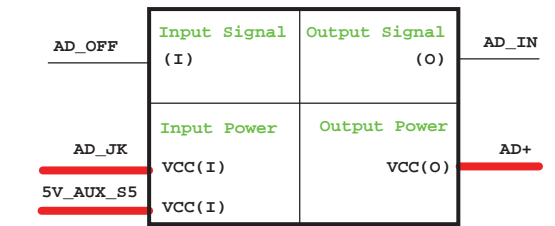
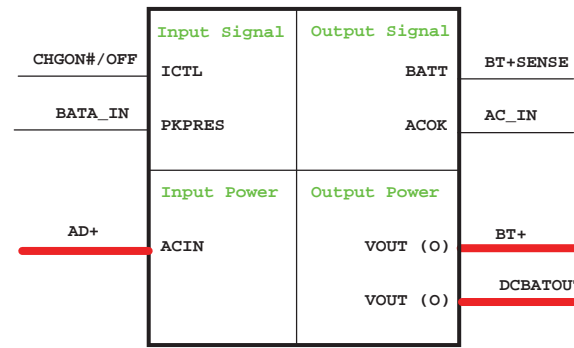
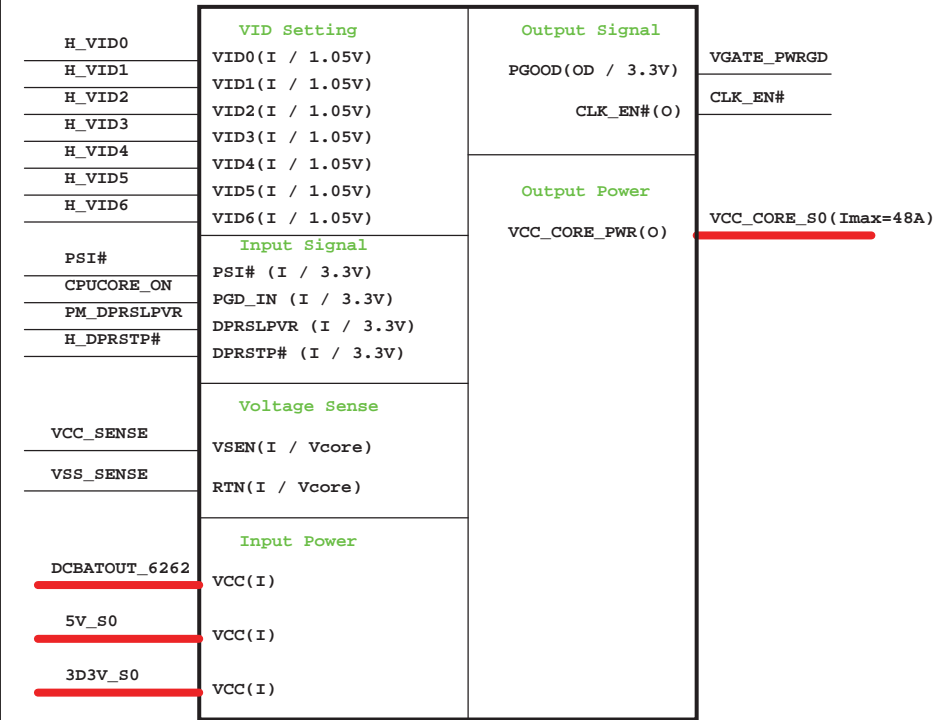
Date: Wednesday, April 25, 2007

Sheet 28 of 45

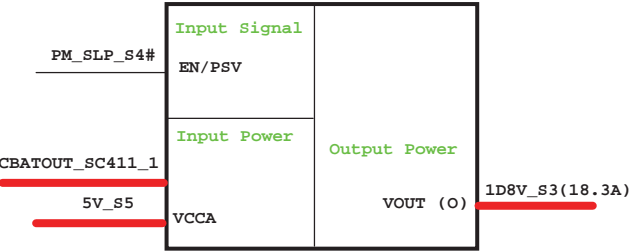
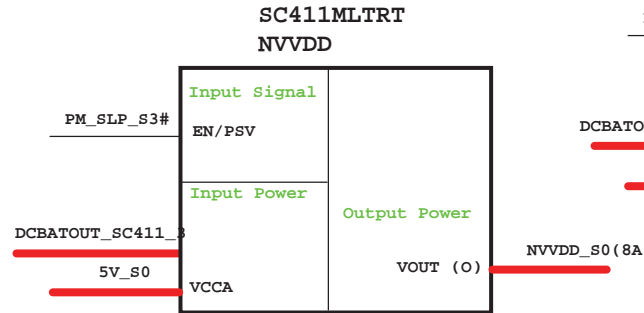
CPU_CORE
Intersil ISL6262A

Charger Max8725

Adapter

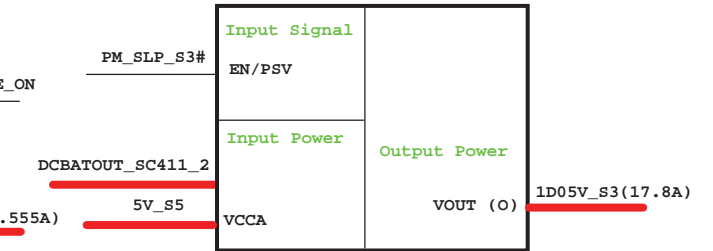
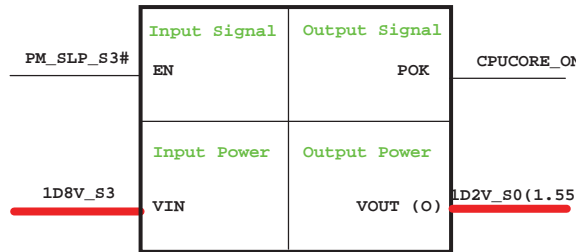


SC411MLTRT
1D8V_S3

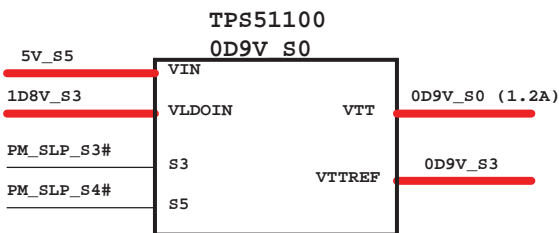
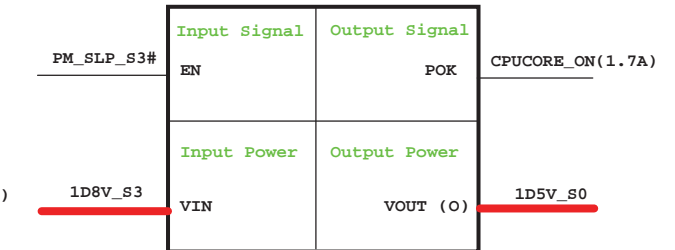
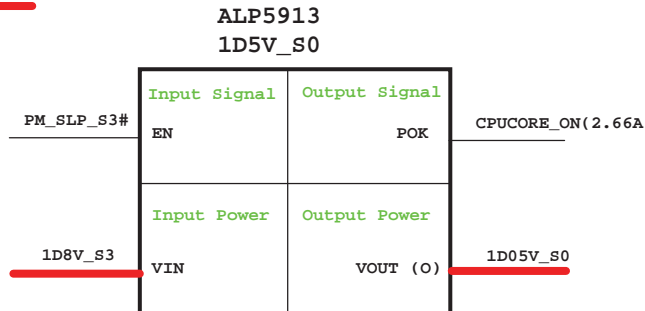
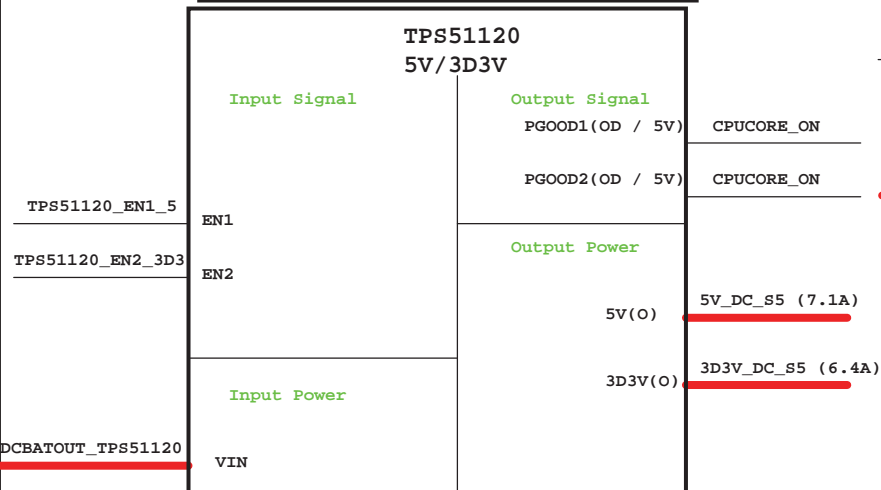


ALP5915
1D2V_S0

SC411MLTRT
1D05V_S3



ALP5915
1D25V_S0

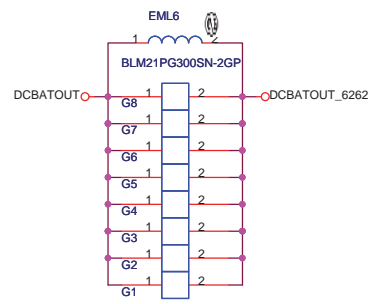
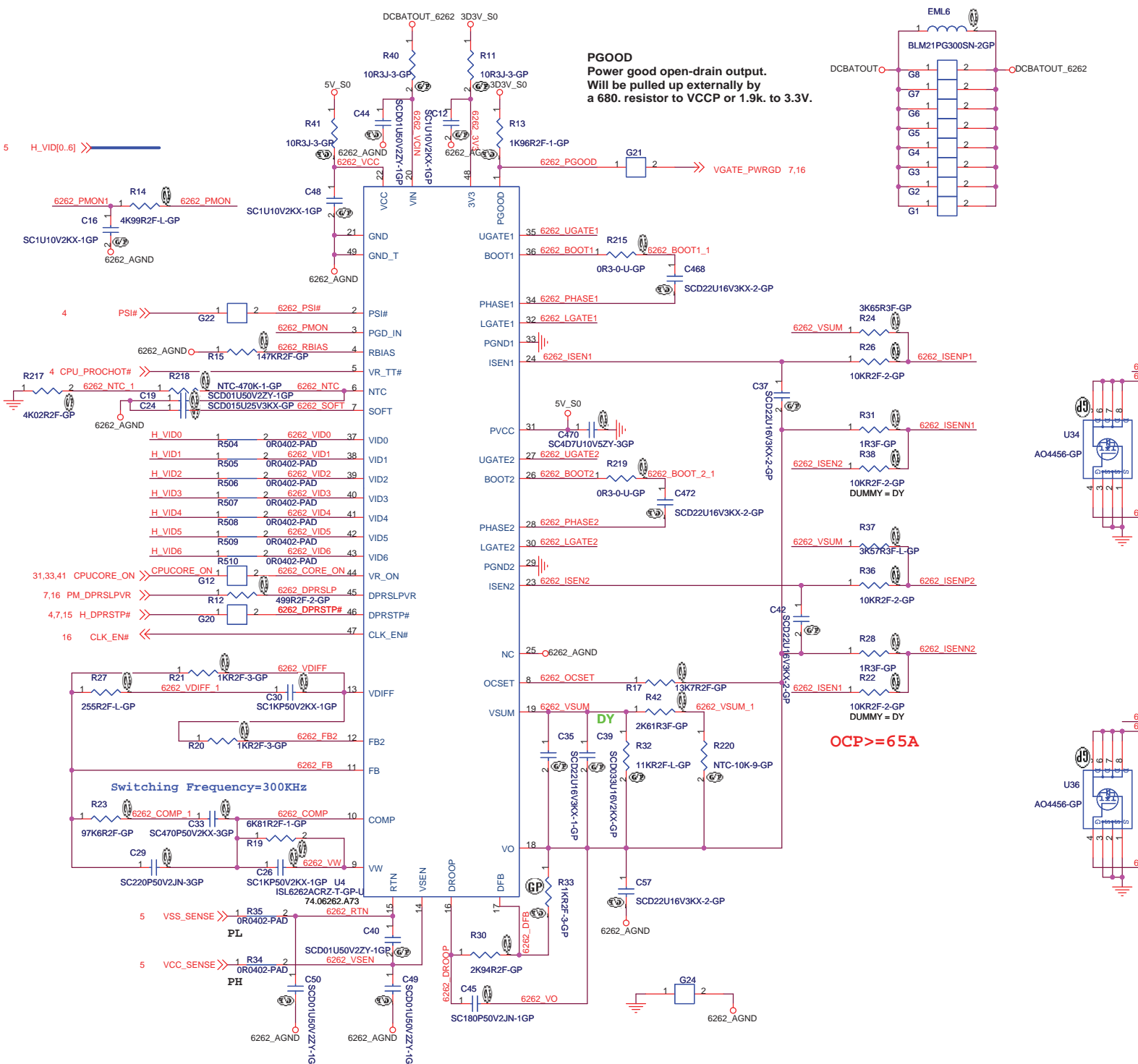


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Title: **Power Block Diagram**

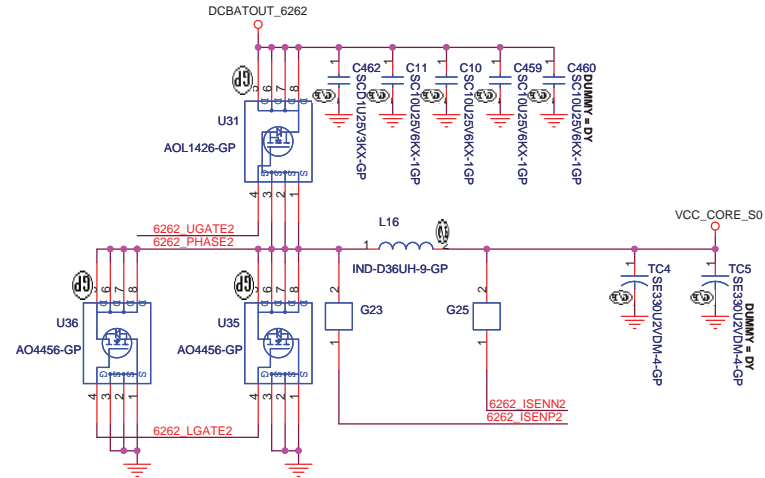
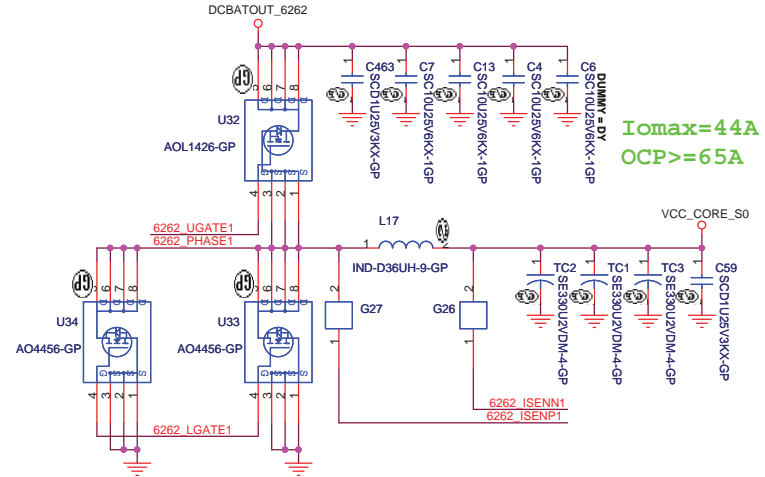
Size: Custom Document Number: **C45/C46** Rev: **SA**

Date: Wednesday, March 07, 2007 Sheet 29 of 45

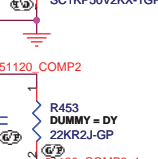
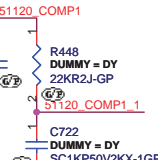
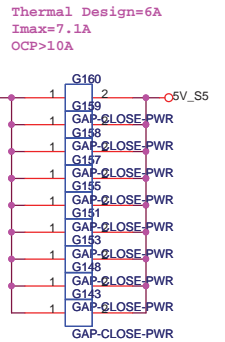
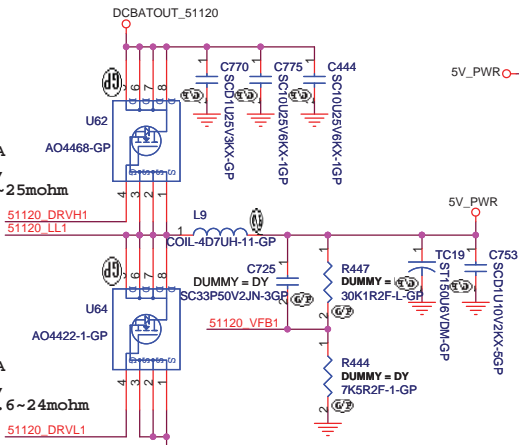
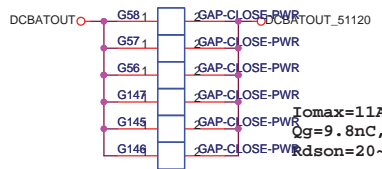
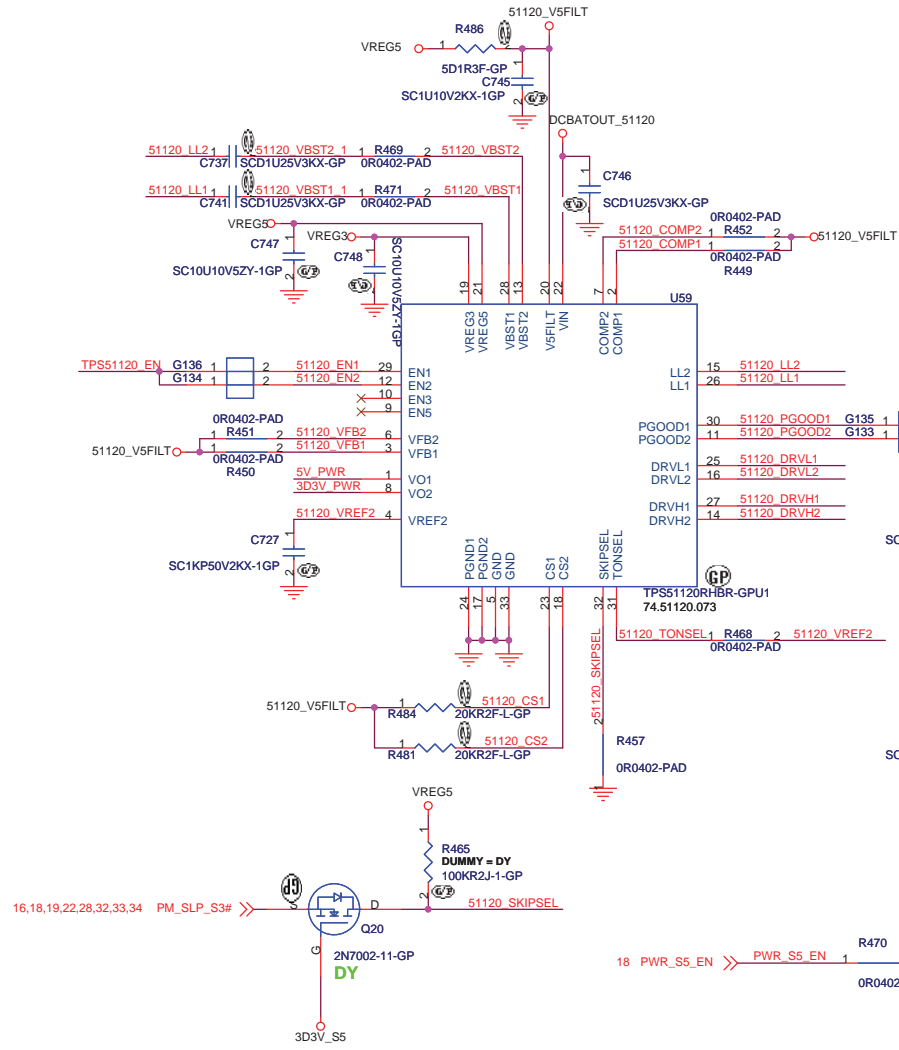


Panasonic ETQP4LR36WFC
10*11.5*4mm
0.34uH / 24A
DCR=1.1mohm

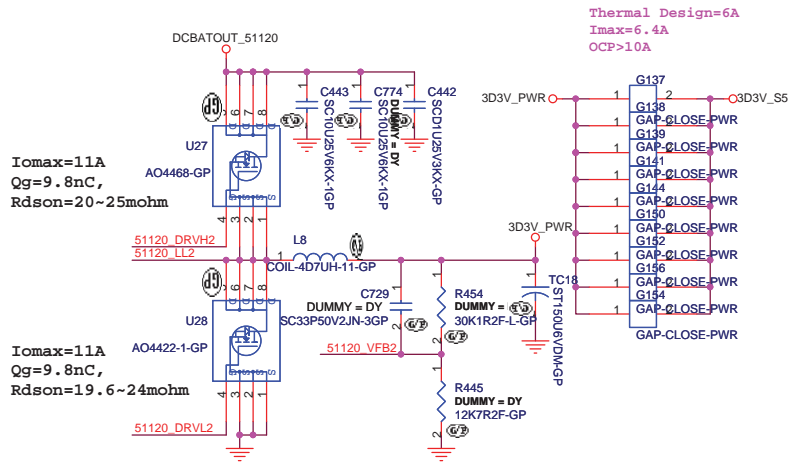
KEMET
330uF / 3V / V size
ESR=9mohm / Iripple=3.7A



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Title		
CPU CORE		
Size	Document Number	Rev
Custom	C45/C46	SA
Date:	Wednesday, April 25, 2007	Sheet 30 of 45



GS 10*10*4 4D7uH
DCR=25mohm, Isat=6A
NEC 220uF, V size
ESR=25mohm
Tripple=2.2A



Thermal Design=6A
Imax=6.4A
OCP>10A

	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP / FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	220k/CH1 330k/CH2	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1, EN2	Switcher OFF	not use	Switchchr ON	Switcher ON
EN3, EN5	LDO OFF	not use	LDO ON	VREG3 on

$$V_{out}=1V \cdot (R1+R2) / R2$$

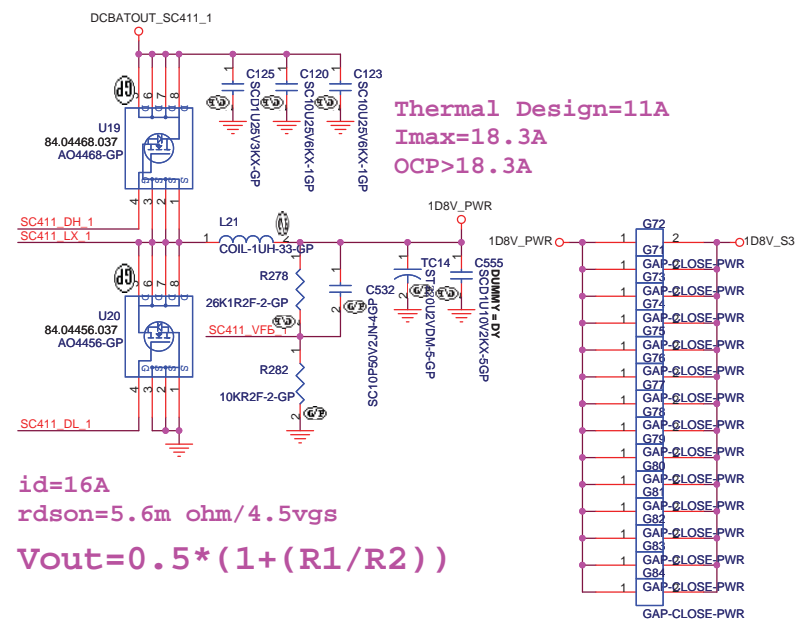
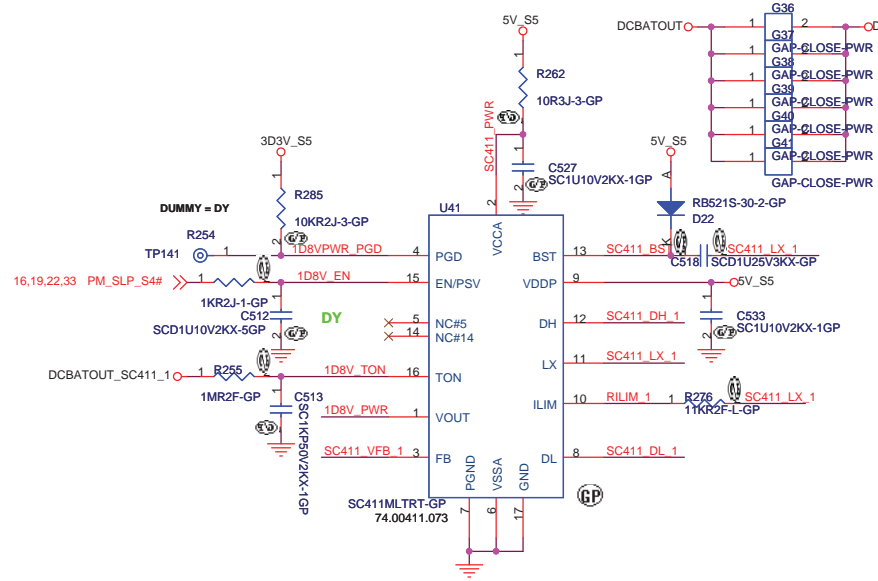
- For TPS51120, Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
 2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
 3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.
- Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
 2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
 3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

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Title: **TPS51120 3D3V 5V**

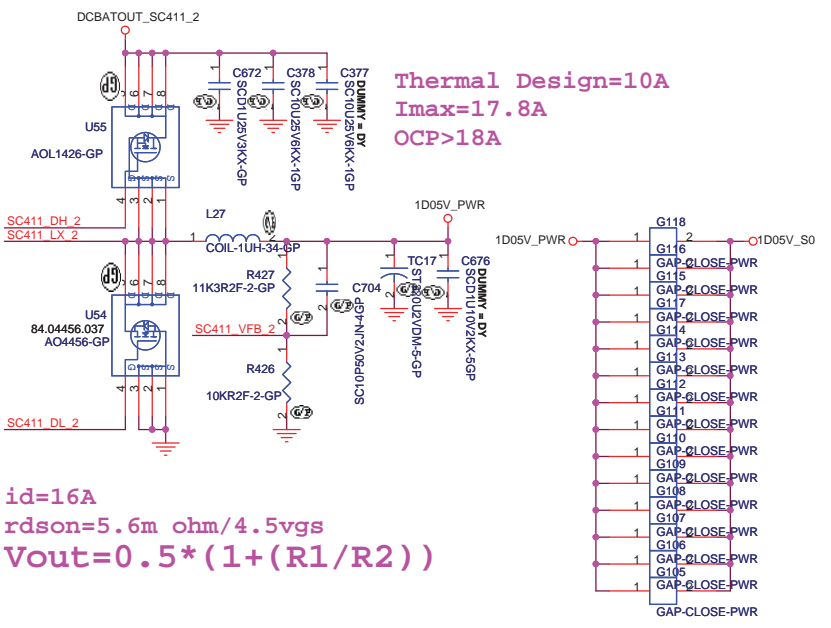
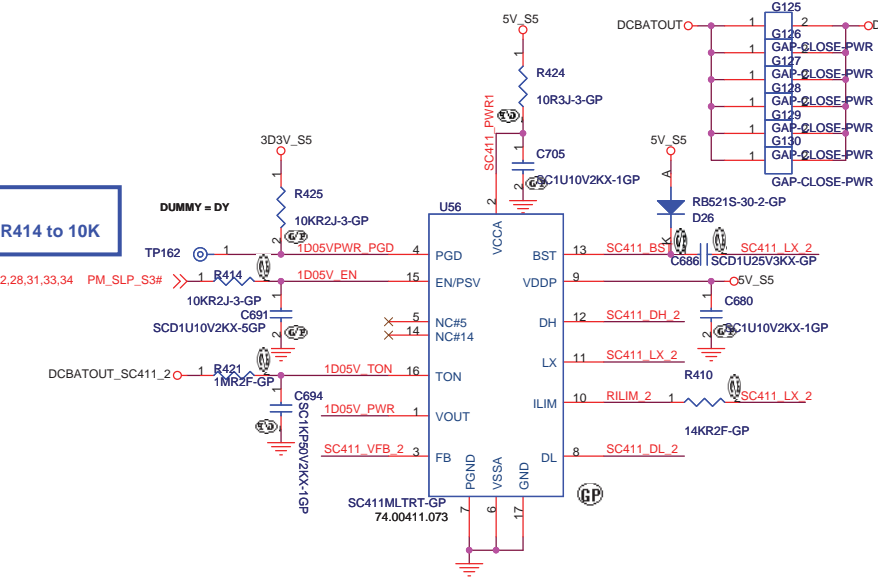
Size: Custom Document Number: **C45/C46** Rev: **SA**

Date: Wednesday, April 25, 2007 Sheet 31 of 45



Thermal Design=11A
 I_{max}=18.3A
 OCP>18.3A

$i_d=16A$
 $r_{dson}=5.6m\ ohm/4.5vgs$
 $V_{out}=0.5*(1+(R1/R2))$

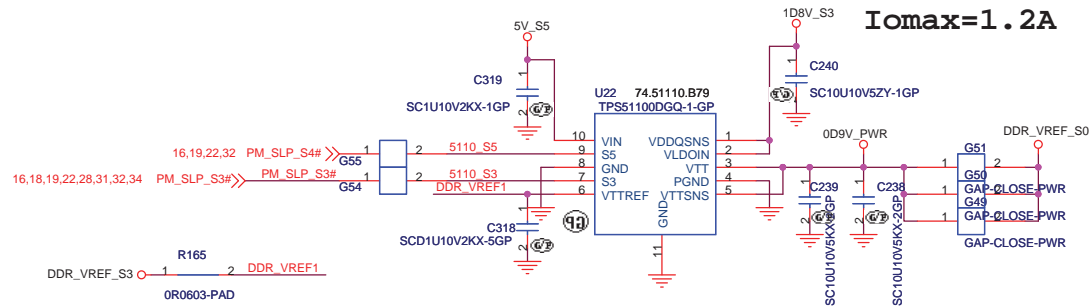


Thermal Design=10A
 I_{max}=17.8A
 OCP>18A

$i_d=16A$
 $r_{dson}=5.6m\ ohm/4.5vgs$
 $V_{out}=0.5*(1+(R1/R2))$

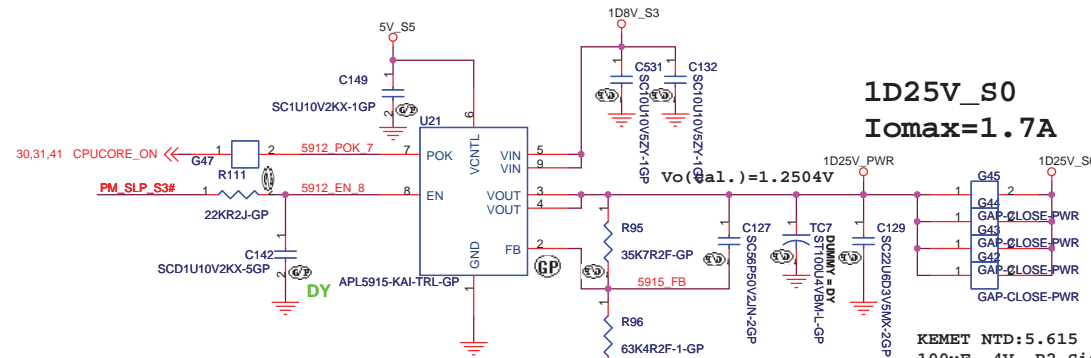
SB
 Change R414 to 10K

0D9V
Iomax=1.2A



Place near the Test point DDRVREF

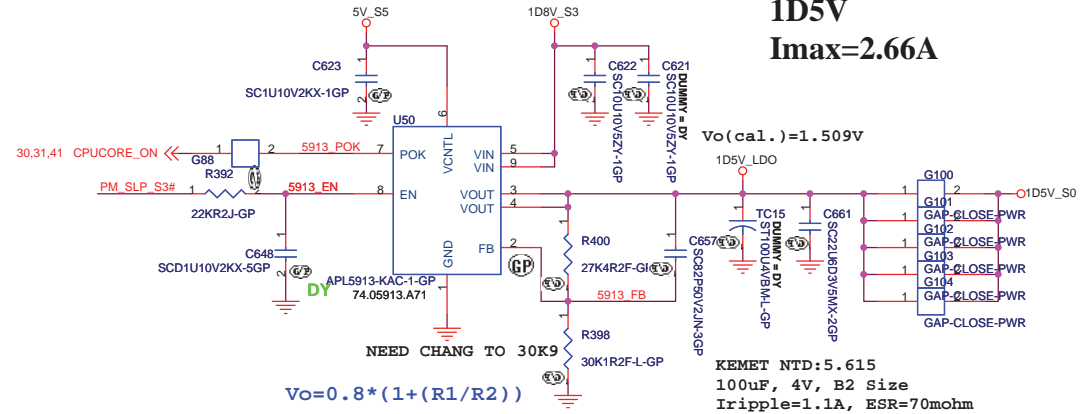
1D25V_S0
Iomax=1.7A



KEMET NTD:5.615
100uF, 4V, B2 Size
Iripple=1.1A, ESR=70mohm

SB
1D5V_S0 : Dummy C648, R392 change to 22K
1D25V_S0 : Dummy C142, R111 change to 22K

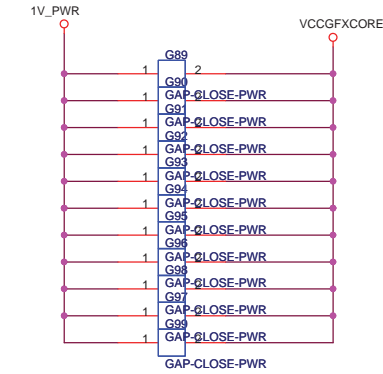
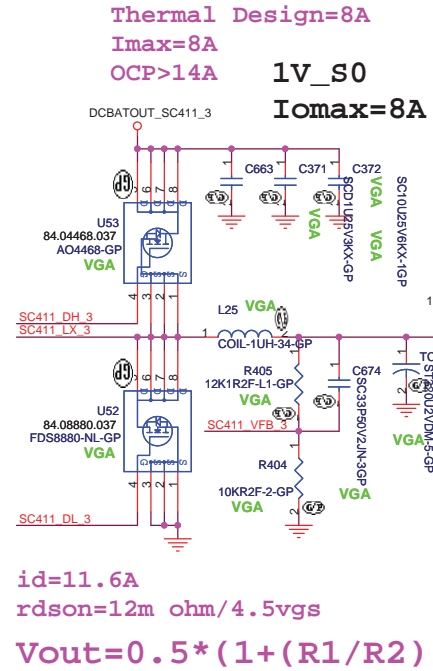
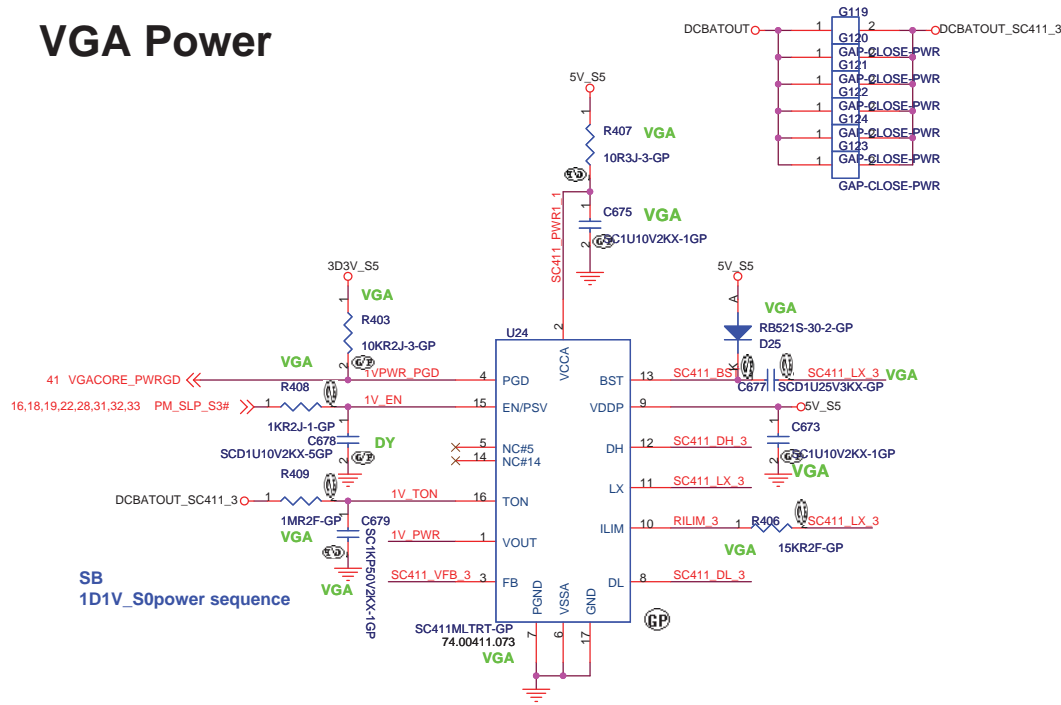
1D5V
Iomax=2.66A



KEMET NTD:5.615
100uF, 4V, B2 Size
Iripple=1.1A, ESR=70mohm

$V_o = 0.8 * (1 + (R1/R2))$

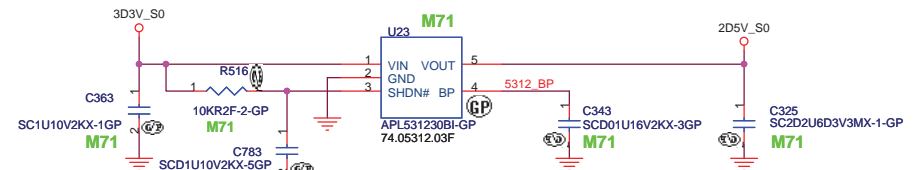
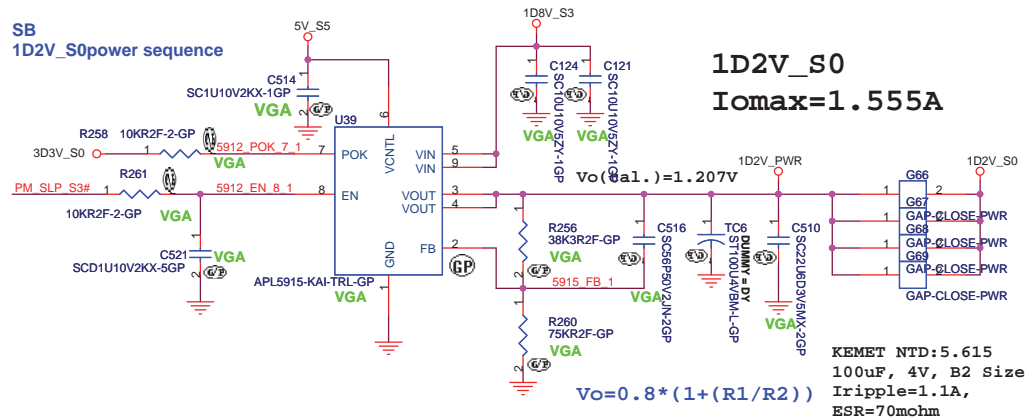
VGA Power



R405
FOR M71 ----> 1.2V 14K (64.14025.6DL)
FOR M72 ----> 1.1V 12.1K (64.12125.6DL)

id=11.6A
rdson=12m ohm/4.5vgs
Vout=0.5*(1+(R1/R2))

2D5V Iomax=300mA

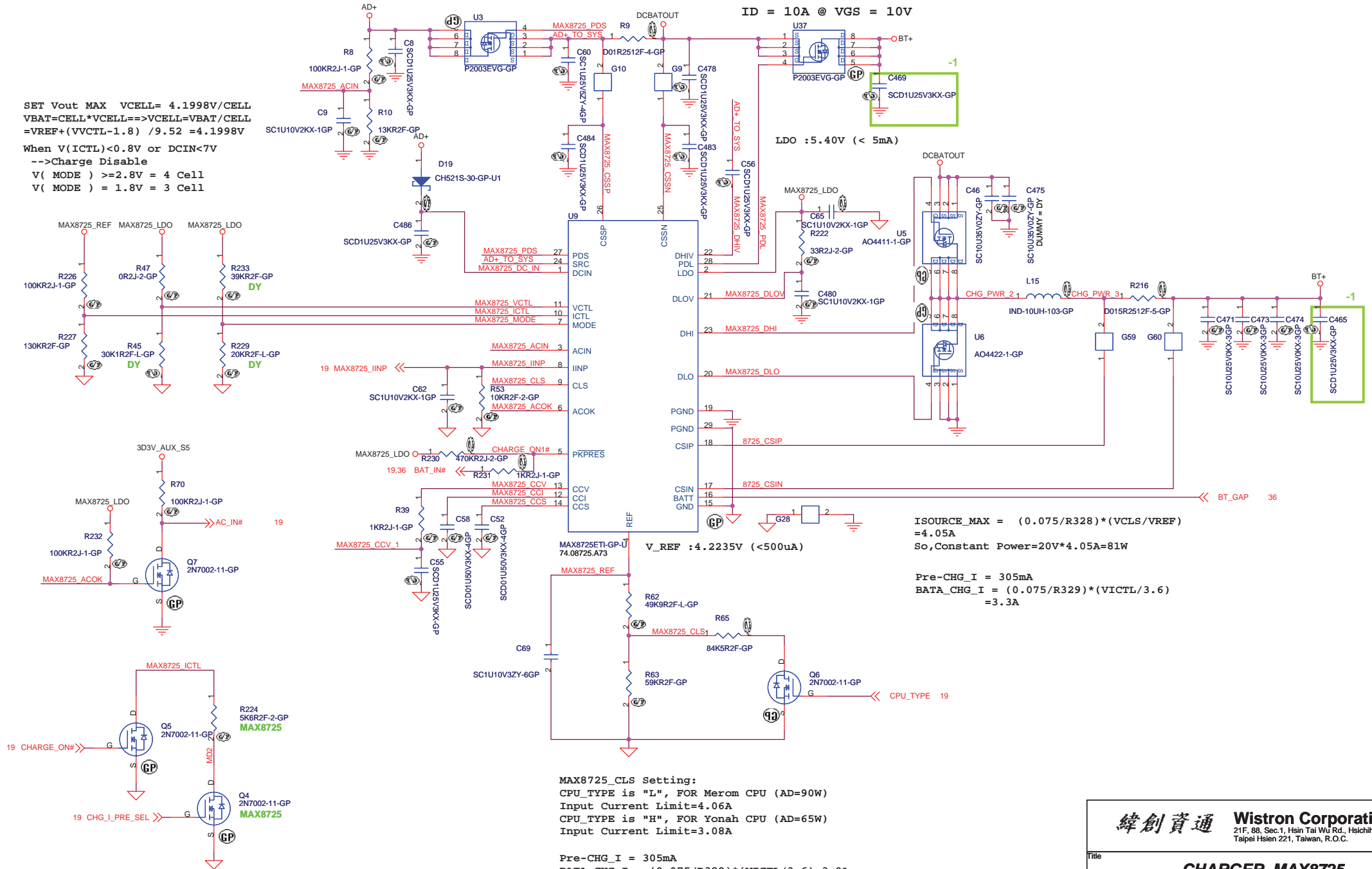


KEMET NTD:5.615
100uF, 4V, B2 Size
Iripple=1.1A,
ESR=70mohm

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VGA POWER	
Title Size A3 Date: Wednesday, April 25, 2007	Document Number C45/C46 Sheet 34 of 45
Rev SA	

SET Vout MAX VCELL = 4.1998V/CELL
 VBAT=CELL*VCELL==>VCELL=VBAT/CELL
 =VREF+(VCTRL-1.8) /9.52 =4.1998V

When V(ICTL)<0.8V or DCIN<7V
 -->Charge Disable
 V(MODE) >=2.8V = 4 Cell
 V(MODE) = 1.8V = 3 Cell



ID = 10A @ VGS = 10V

LDO : 5.40V (< 5mA)

V_REF : 4.2235V (<500uA)

ISOURCE_MAX = (0.075/R328)*(VCLS/VREF)
 =4.05A
 So, Constant Power=20V*4.05A=81W

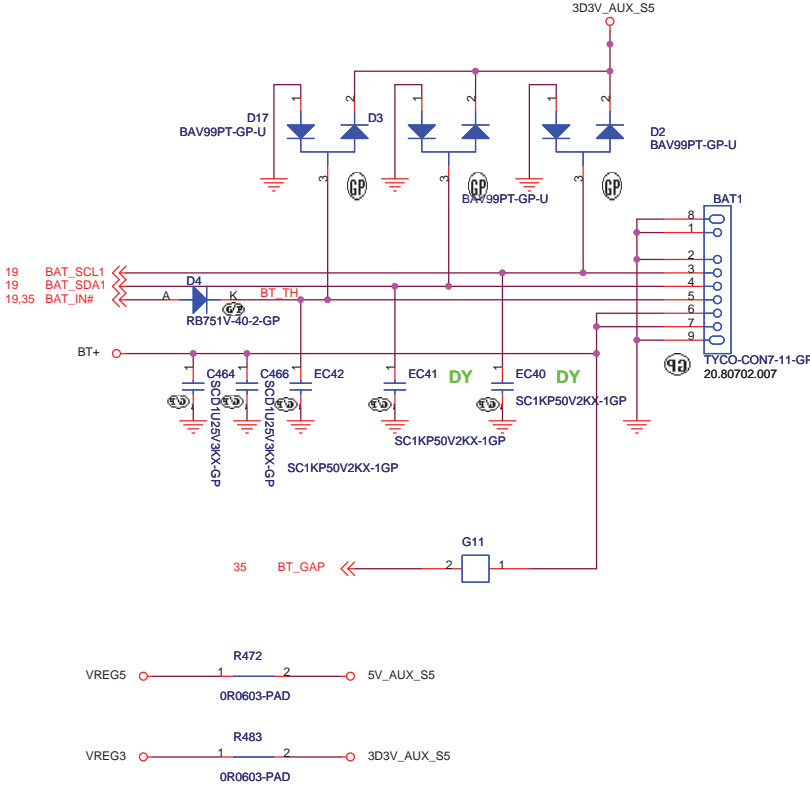
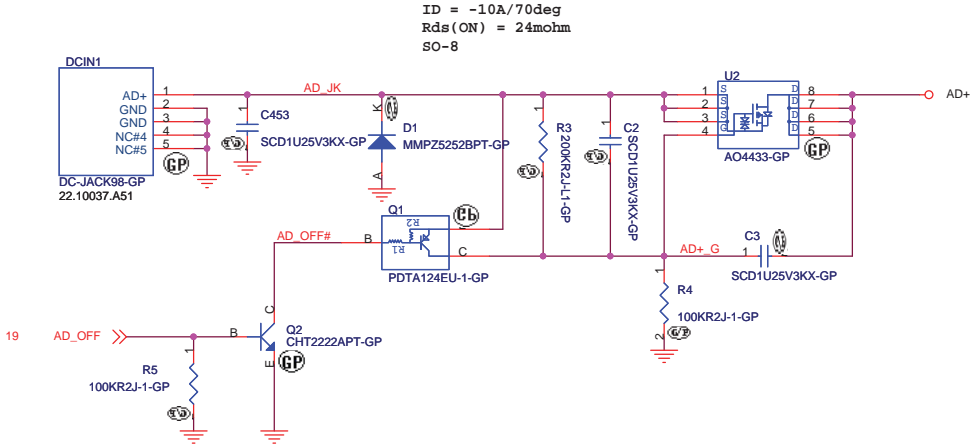
Pre-CHG_I = 305mA
 BATA_CHG_I = (0.075/R329)*(VICTL/3.6)
 =3.3A

MAX8725_CLS Setting:
 CPU_TYPE is "L", FOR Merom CPU (AD=90W)
 Input Current Limit=4.06A
 CPU_TYPE is "H", FOR Yonah CPU (AD=65W)
 Input Current Limit=3.08A

Pre-CHG_I = 305mA
 BATA_CHG_I = (0.075/R329)*(VICTL/3.6)=3.0A

BATTERY CONNECTOR

Adaptor in to generate DCBATOUT



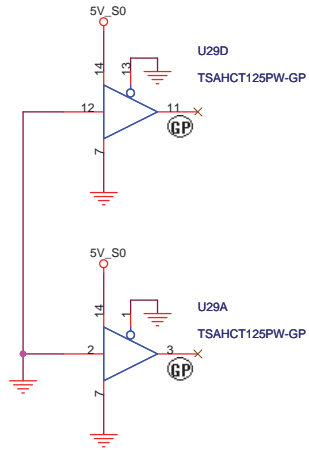
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **AD IN/BAT Conn**

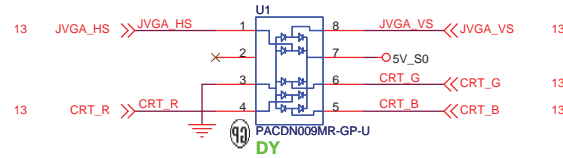
Size: Custom Document Number: **C45/C46** Rev: **SA**

Date: Friday, April 27, 2007 Sheet 36 of 45

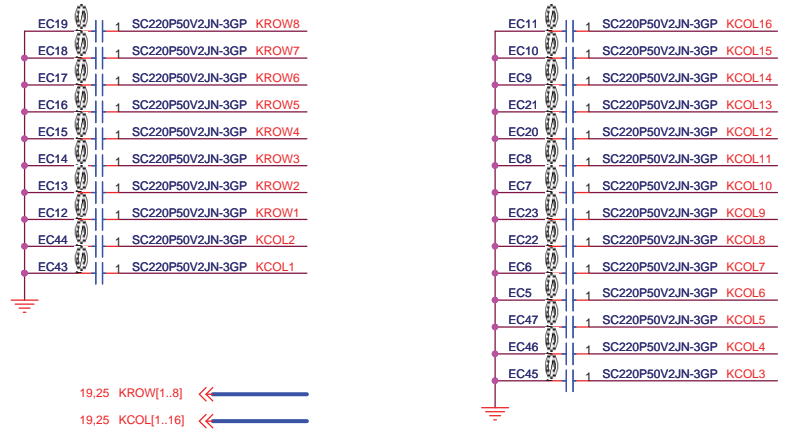
UNUSE Parts



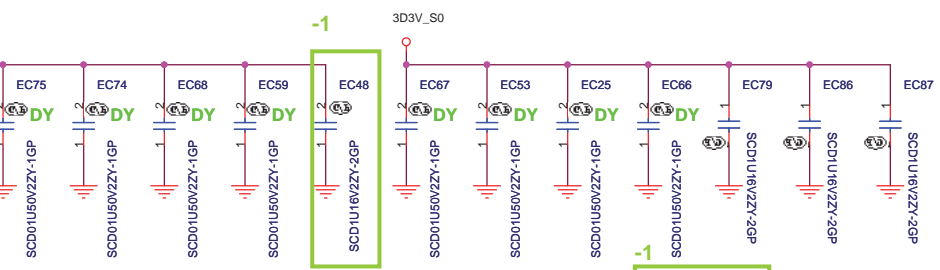
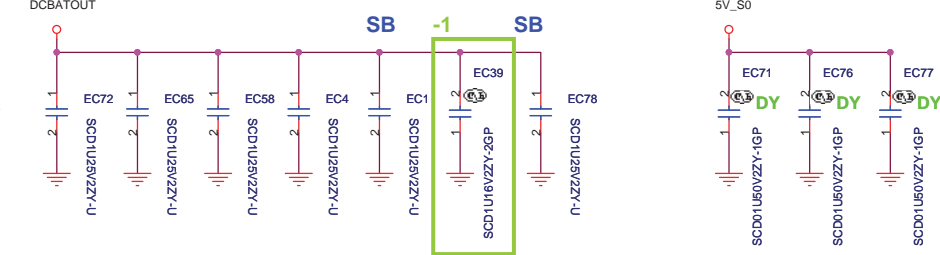
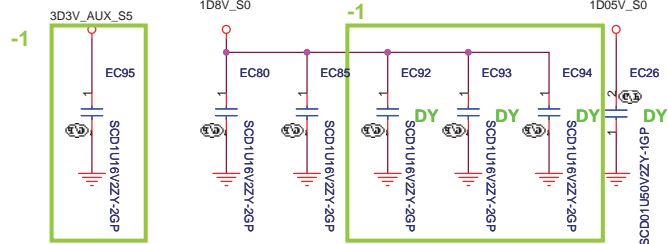
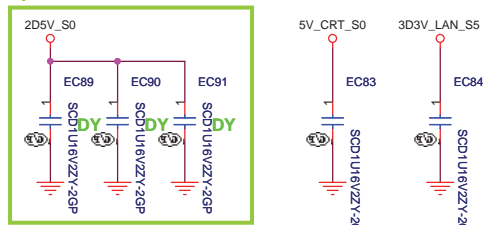
ESD Parts



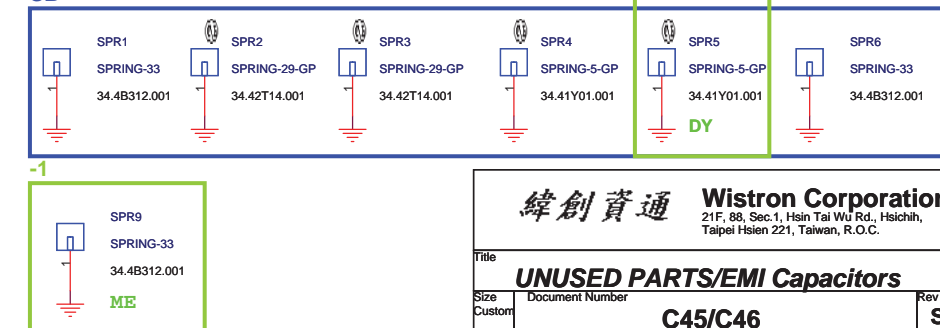
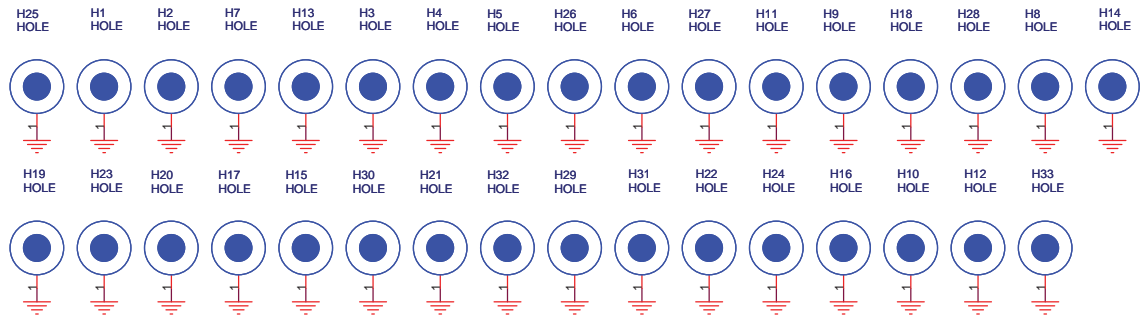
Keyboard EMI Caps

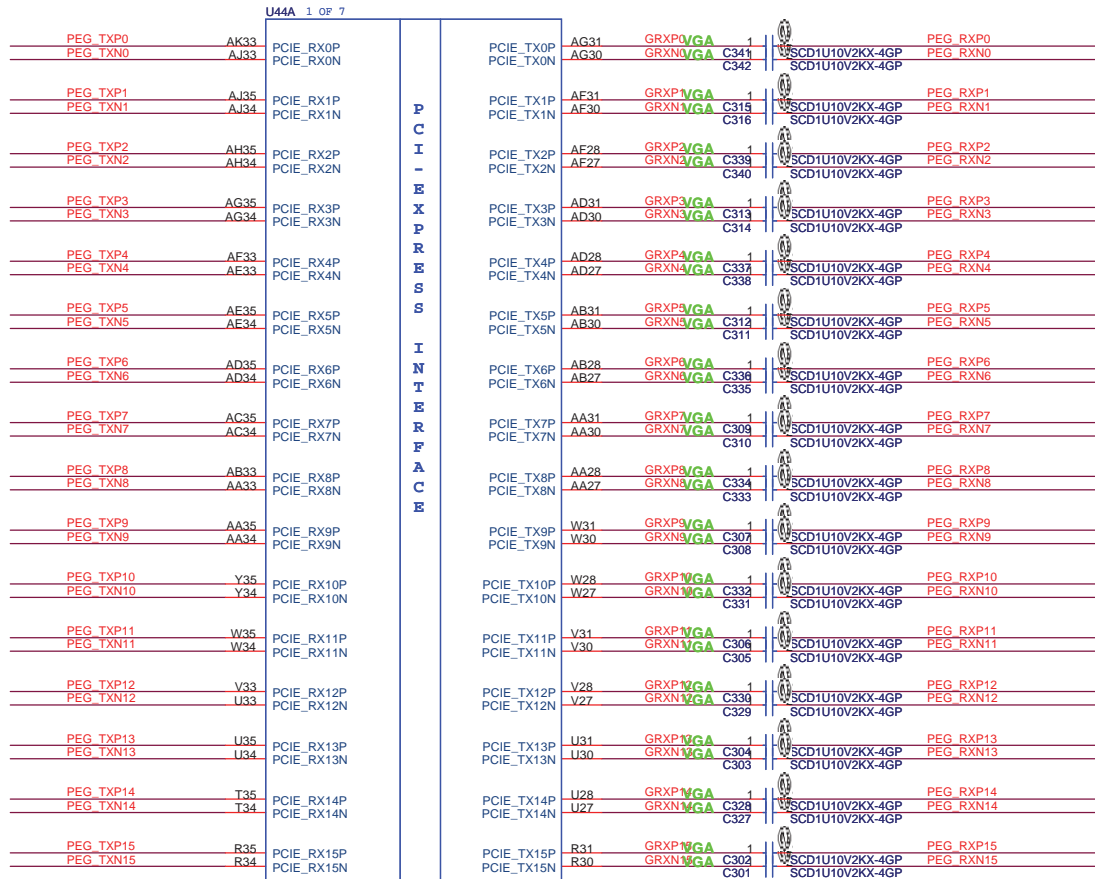


EMI Caps

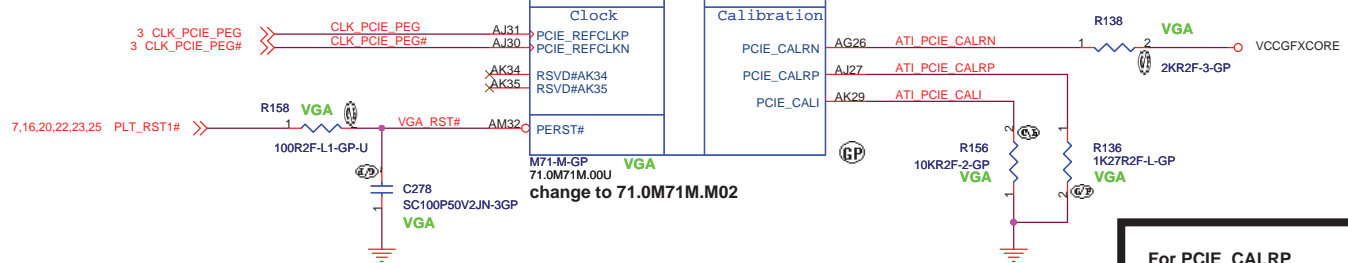


Holes





PEG_RXN[0..15] 7
 PEG_RXP[0..15] 7
 PEG_TXN[0..15] 7
 PEG_TXP[0..15] 7



For PCIE_CALRP
1.27K to PCIE_VSS for M72M,M76M
562R to PCIE_VSS for M66M,M71M

For PCIE_CALI
10K to PCIE_VSS for M72M,M76M
1.47K to PCIE_VSS for M66M,M71M

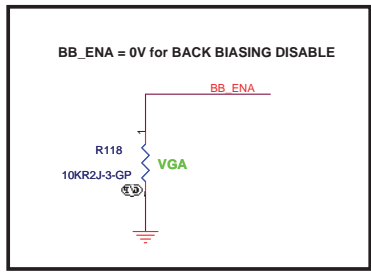
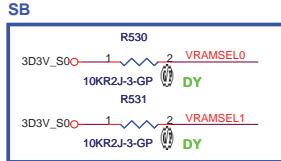
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Title
VGA-M71/M72-M(1/5) PCIE

Size A3 Document Number
C45/C46

Date: Wednesday, April 25, 2007 Sheet 38 of 45

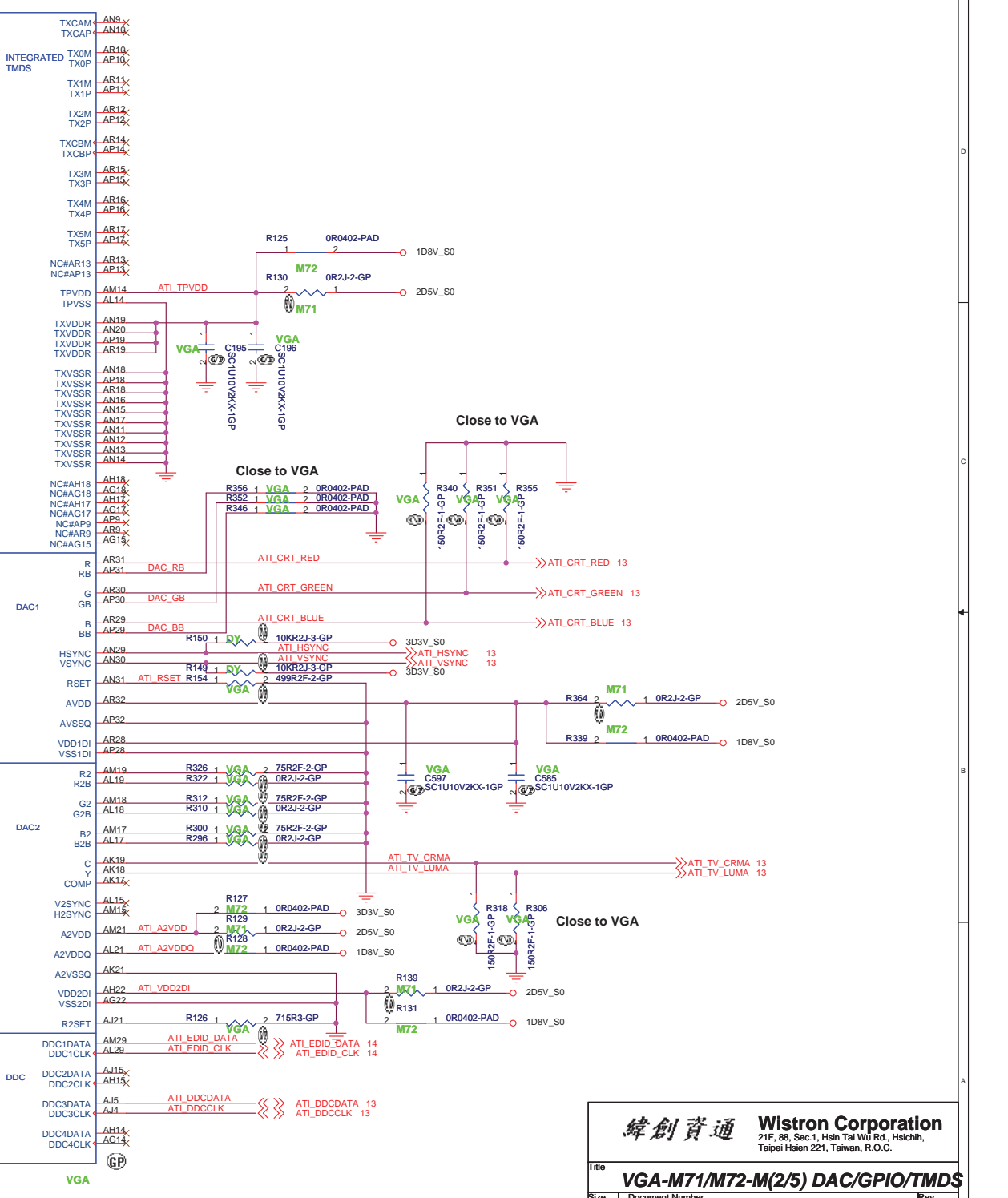
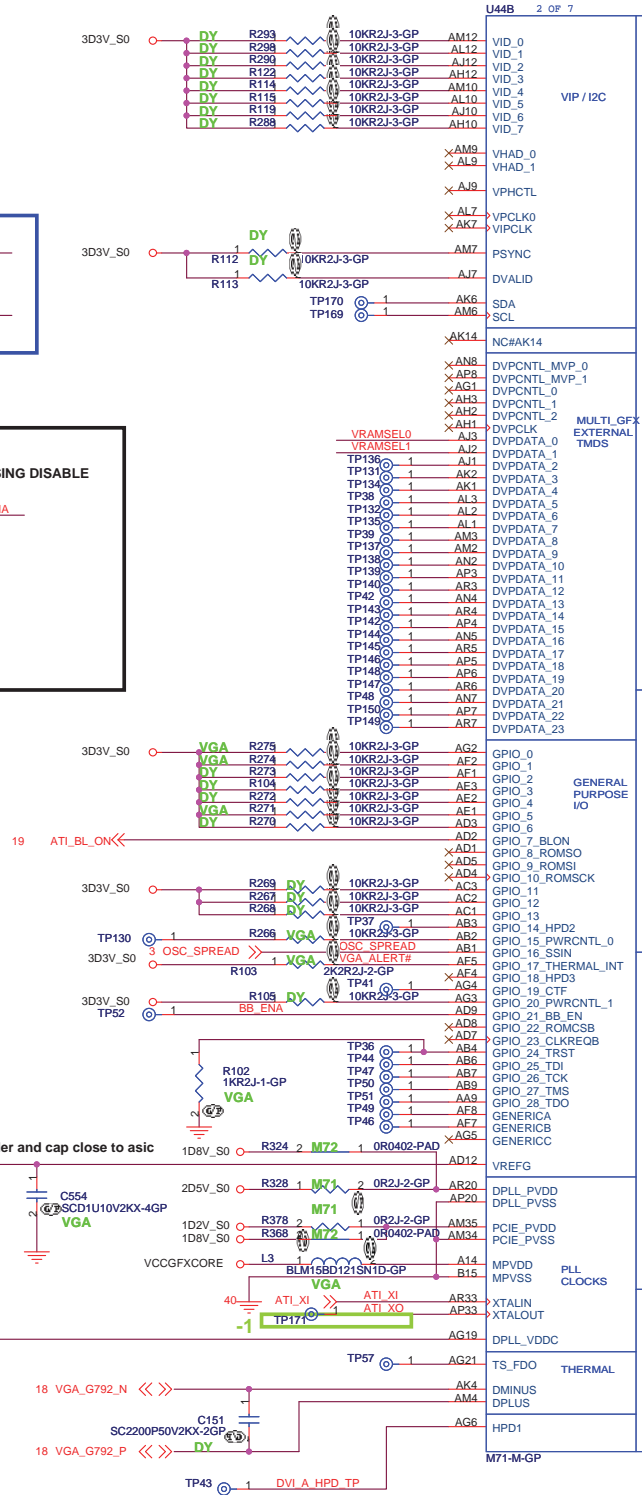
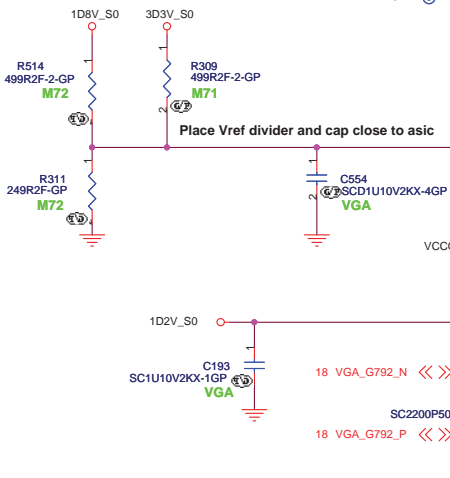
Rev SA



SB

For M72M,M76M
Vrefrg voltage divider is
(vrefrg=1.8v/3=0.6v) 249ohm

For M66M,M71M
Vrefrg voltage divider is
(vrefrg=3.3v/2=1.65v) 499ohm



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Title
VGA-M71/M72-M(2/5) DAC/GPIO/TMDS

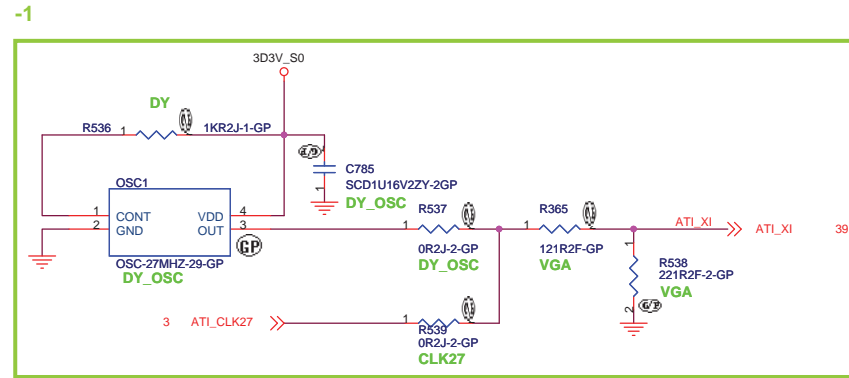
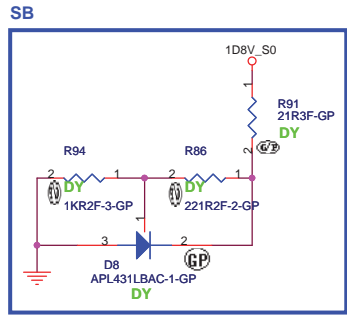
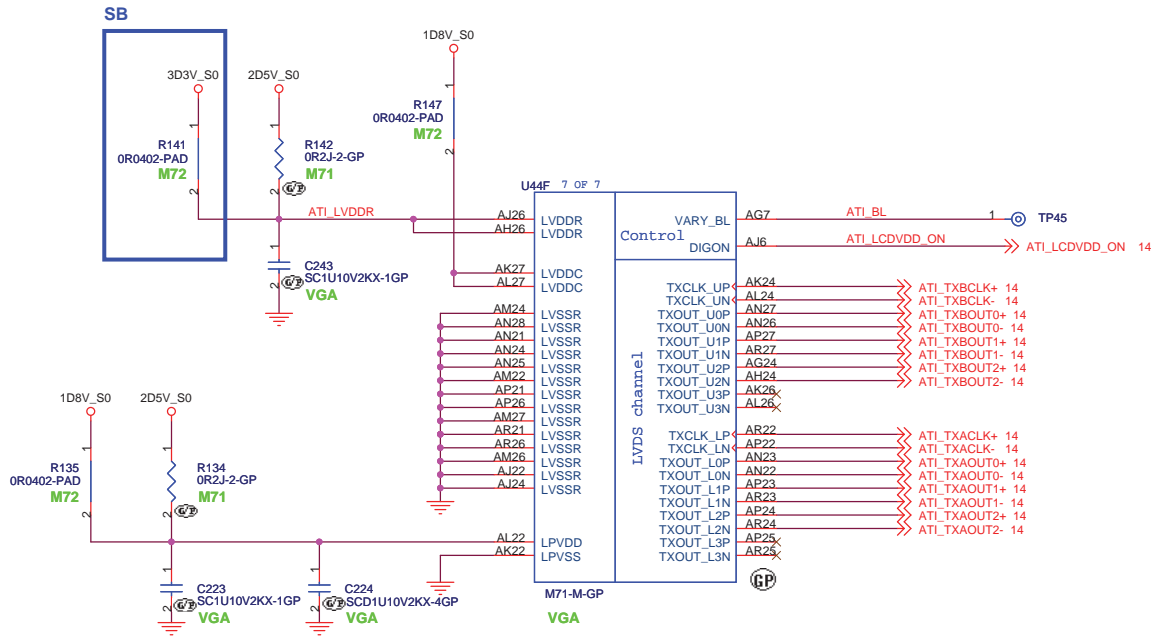
Size
Custom

Document Number
C45/C46

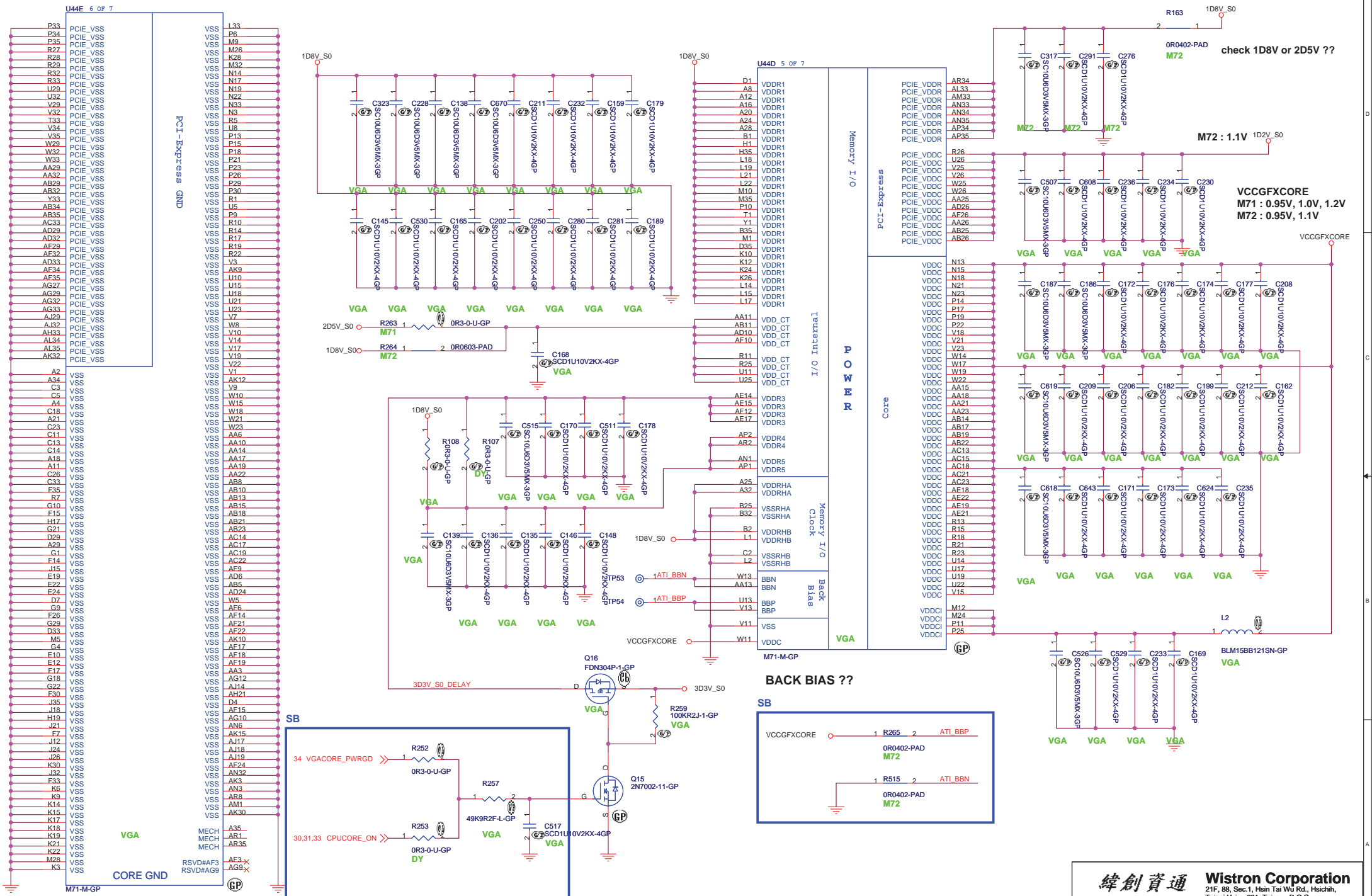
Date
Thursday, April 26, 2007

Rev
SA

Sheet 39 of 45



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Title VGA-M71/M72-M(3/5)LVDS	
Size A3	Document Number C45/C46
Date: Thursday, April 26, 2007	Rev SA
Sheet 40 of 45	



check 1D8V or 2D5V ??

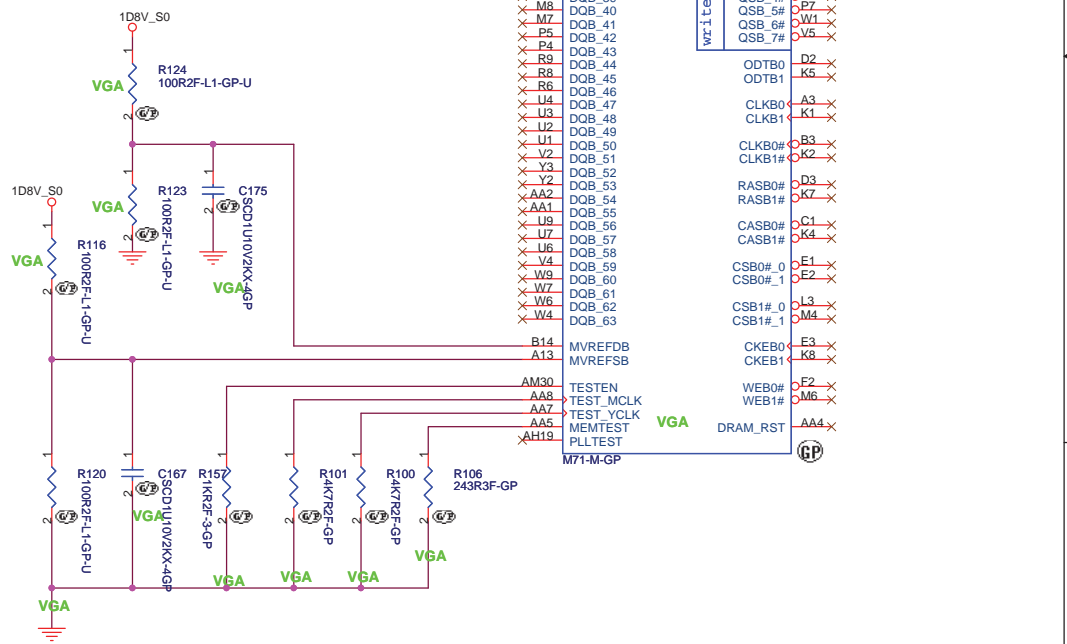
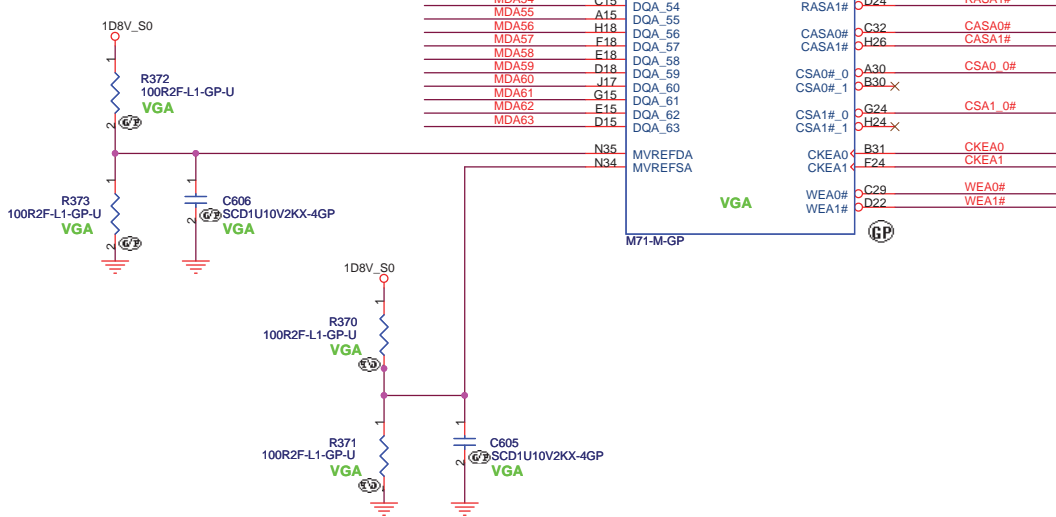
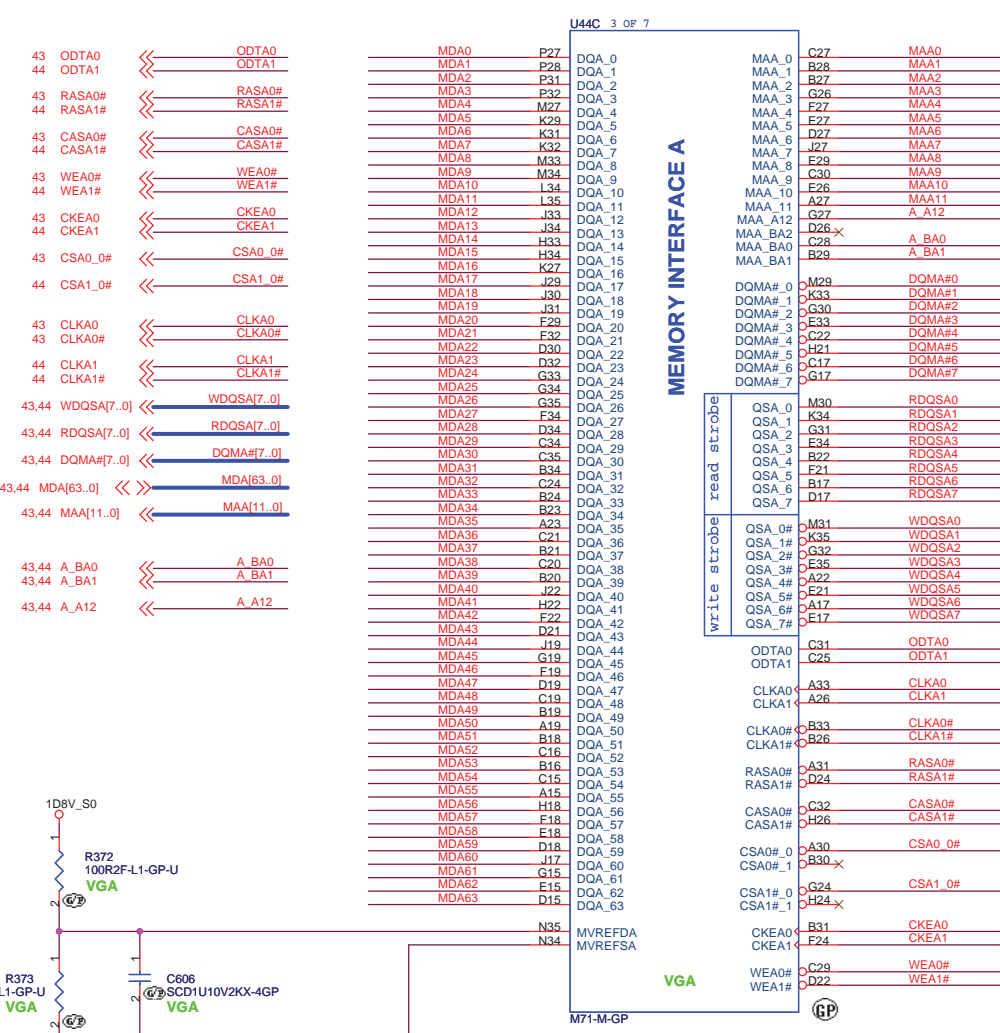
M72 : 1.1V

VCCGFXCORE
M71 : 0.95V, 1.0V, 1.2V
M72 : 0.95V, 1.1V

BACK BIAS ??

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 Taipei Hsien 221, Taiwan, R.O.C.

Title			VGA-M71/M72-M(4/5) POWER		
Size	Document Number				Rev
Custom	C45/C46				SA
Date:	Wednesday, April 25, 2007		Sheet	41	of 45



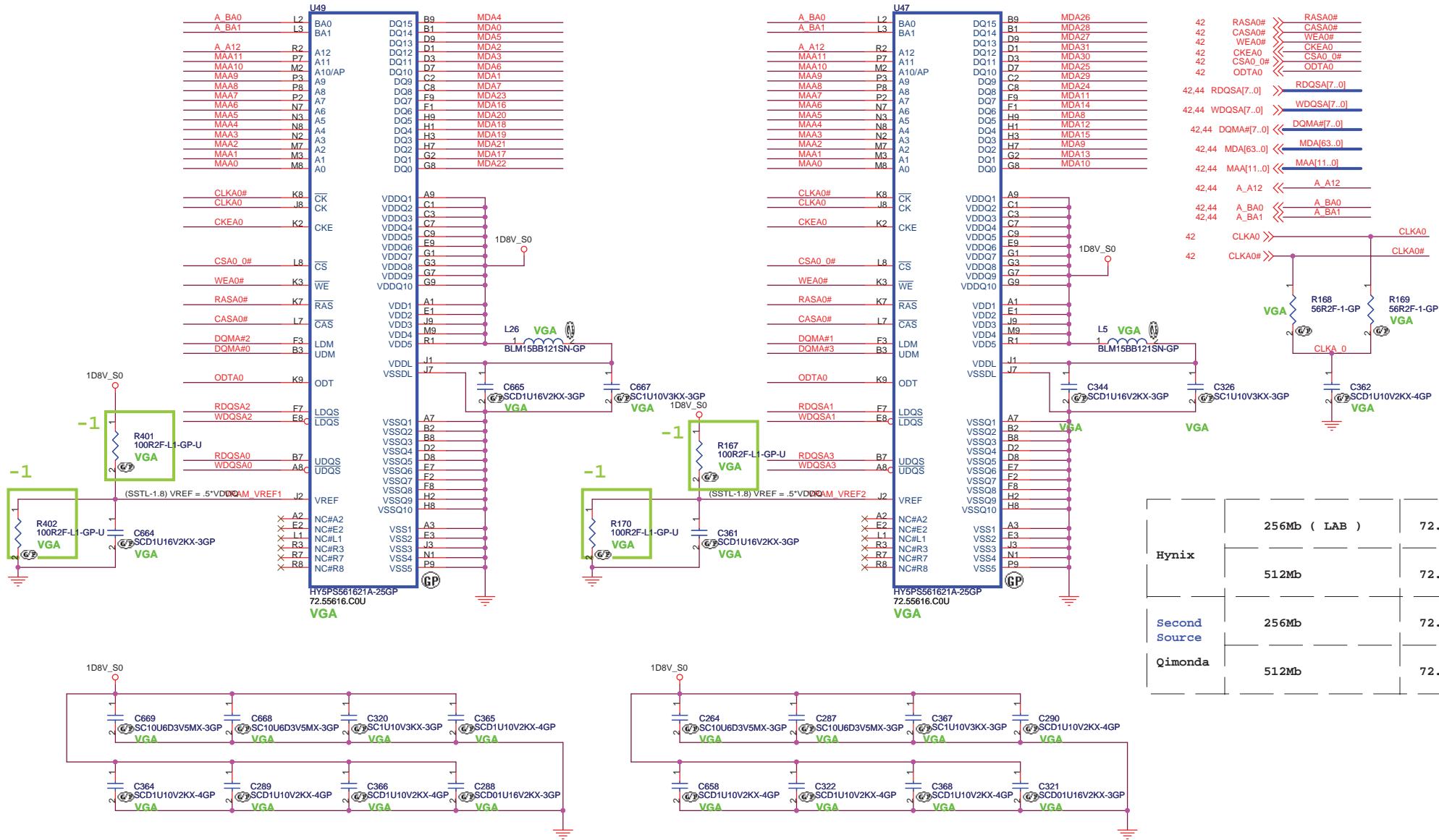
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsein 221, Taiwan, R.O.C.

Title: **VGA-M71/M72-M(5/5) MEMORY I/O**

Size A3 Document Number **C45/C46** Rev SA

Date: Wednesday, April 25, 2007 Sheet 42 of 45

DDR2 BGA MEMORY (16M x 16)



Hynix	256Mb (LAB)	72.55616.C0U
	512Mb	72.51216.D0U
Second Source	256Mb	72.18256.B0U
Qimonda	512Mb	72.18512.A0U

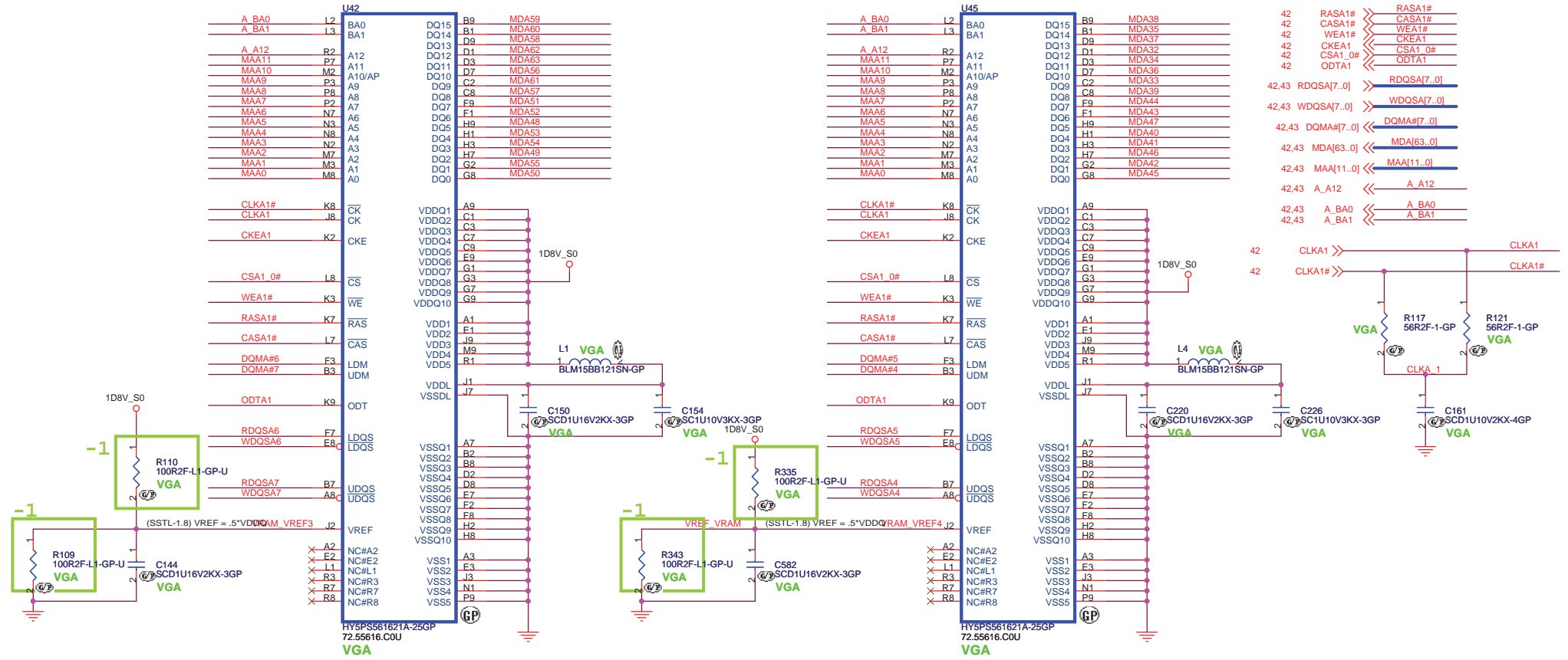
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **VGA-VRAM(1/2)**

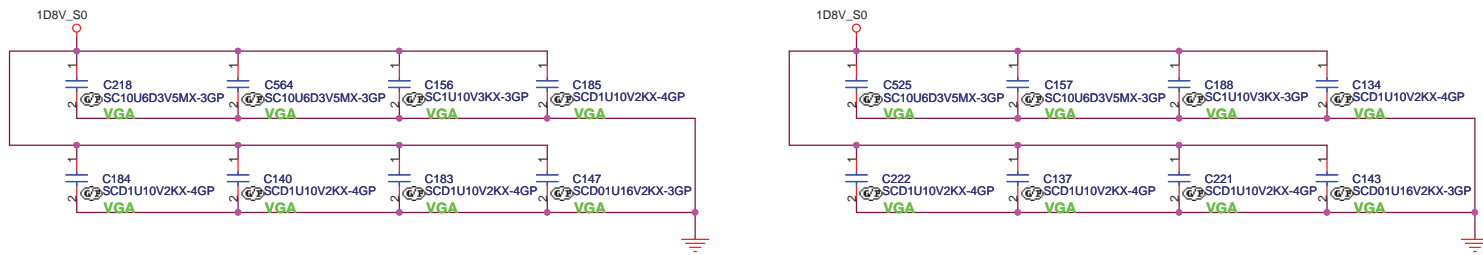
Size A3 Document Number **C45/C46** Rev **SA**

Date: Thursday, April 26, 2007 Sheet 43 of 45

DDR2 BGA MEMORY (16M x 16)



Second Source: Qimonda 72.18256.B0U



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Title: **VGA-VRAM(2/2)**

Size A3 Document Number **C45/C46** Rev SA

Date: Thursday, April 26, 2007 Sheet 44 of 45

History

2006/11/17

1. Schematic drawing start..

2006/12/12

1. Change to project name to C45/C46

2007/01/08

1. LAB gerber out

BOM Change (LAB)

2006/12/29

1. VGA Change to M72, VRAM 128MB, but verify M71 (71.0M71M.M02) and M72(71.0M72M.M01) in LAB

2. 965GM (71.GM965.00U)

3. 965PM (71.PM965.00U)

4. RTS5158 (71.08111.A03)

5. ME stand off 34.4G901.001 (H23, H25, H9, H11) for MINI Card

6. ME stand off 34.4B601.001 (H26, H27) for MODEM

7. ME stand off 87.00055.120 (H4) for LVDS

8. ICH8-M (71.ICH8M.A0U)

LAB Chipset Part Number

C45:

NB: 71.CREST.M03

SB: 71.0ICH8.M08

C46:

NB: 71.CREST.A0U

SB: 71.0ICH8.M08

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Title

HISTORY

Size

A3

Document Number

C45/C46

Rev

SA

Date: Wednesday, March 07, 2007

Sheet 45 of 45