Intel Calpella BlOCK DIAGRAM

Intel Calpella Arrandale UMA

POWER

SYSTEM RESET CIRCUIT

BATT CHARGER

AC/BATT CONNECTOR

RUN POWER SW

+3V_S5/+5V_S5

+3V_SUS/+5V_SUS

+5V_RUN/+3V_RUN/+1.8V_RUN

FAN & THERMAL

CLOCK
SLG8SP585VTR
(QFN-32)

POWER

REGULATOR
+1.5V_SUS/+0.75V_DDR_VTT

+1.05V_PCH

+1.05V_VTT

CPU VR

DC/DC
+3VPCU/+5VPCU/

CPU
Arrandale 35W
37.5mm X 37.5mm
(rPGA 989)

DDR3-SODIMM1 CHA

DDR3-SODIMM2 CHB

Dual Channel DDR3
1066 1.5V

FDI

DMI X 4

PCH
82801IBM
(HM55)
27mm X 25mm

SATA-ODD

SATA-HDD

SATA

SATA

IHDA

AUDIO/AMP
ALC269

Audio SPK conn

Audio Jacks

LPC

EC
ITE8502

18X8

Keyboard

SPI

PS/2

FLASH 2Mbyts

Touchpad

SPI

FLASH 2Mbyts

HDMI

LVDS

VGA

USB2.0 x 3

PCIEx1

PCIEx1

PCIEx1

PCIEx1

PS8101

HDMI

Panel Connector

CRT CONN.

USB conn x 3

Card Reader SD MS CARD
RTS5159

GLAN 10/100/1000 LAN
Realtek RTL8111E-GR

MINI-CARD
WLAN

NEW CARD

W83L351YG

MINI-CARD
3G

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	BLOCK DIAGRAM	1A

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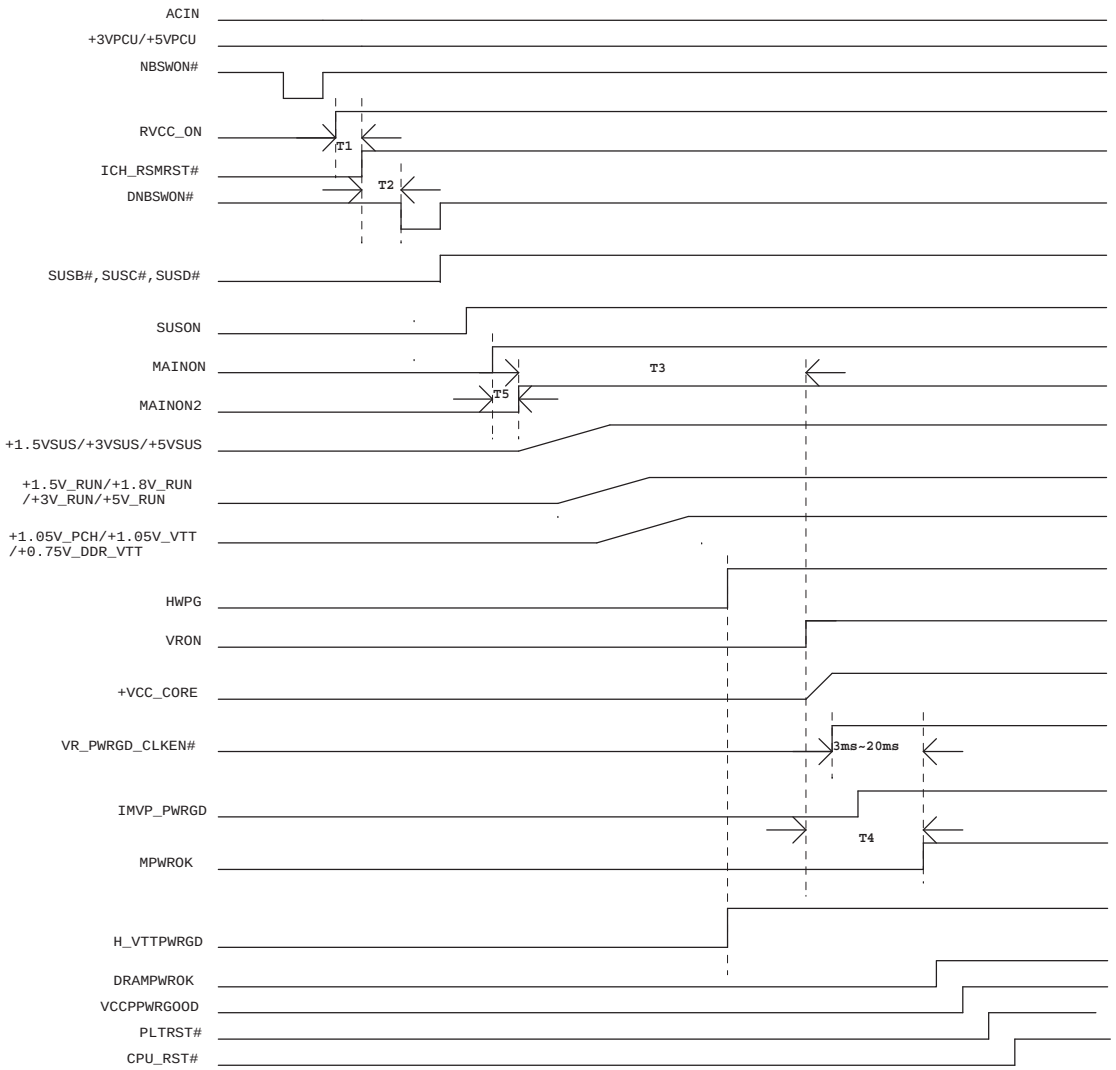
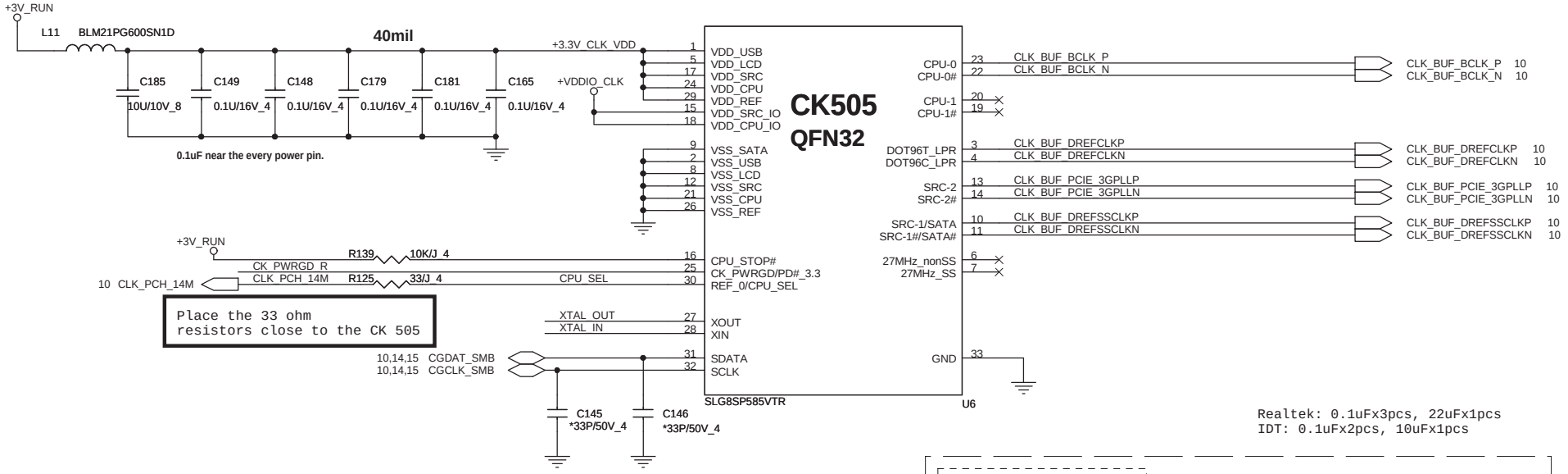
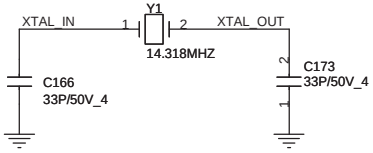
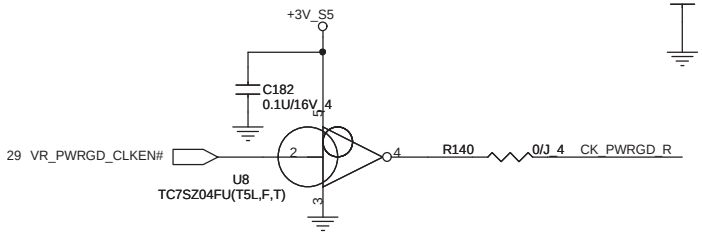
Power Sequence

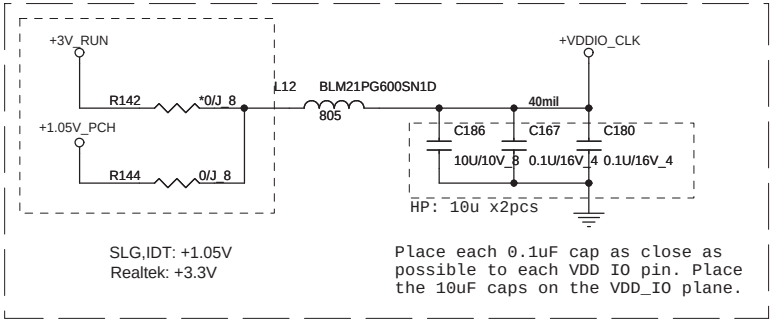


T1: RVCCON TO RSMRST# = 30ms (spec:mini 10ms)
T2: RSMRST# TO-DNBSWON = 110ms (spec:mini 100ms)
T3: MAINON2 TO VRON = 110ms (spec:mini 99ms)
T4: VRON TO MPWROK = 10ms (HWPG NEED TO BE HIGH at that time)
Note: IMVP_CLK_EN# (inverted) assertion to SYS_PWROK/PCH_PWROK assertion.
SPEC:3ms~20ms
T5: MAINON to MAINON2 =500us



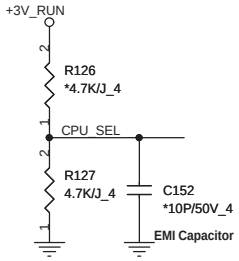






Realtek: 0.1uFx3pcs, 22uFx1pcs
IDT: 0.1uFx2pcs, 10uFx1pcs

+VDDIO_CLK:
SLG date sheet (V0.2) P15: Min 1.05V,Max3.465V.
Realtek date sheet(V1.2) P11: Min 1.05V,Max 3.3V.
IDT date sheet(V0.7) P10: Min 0.9975V,Max 3.465V.



PIN 30	CPU_0	CPU_1
0(default)	133MHz	133MHz
1(0.7V-1.5V)	100MHz	100MHz

CPU_SEL:
SLG date sheet (V0.2) P15:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
Realtek date sheet(V1.2) P11:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
IDT date sheet(V0.7) P10:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.

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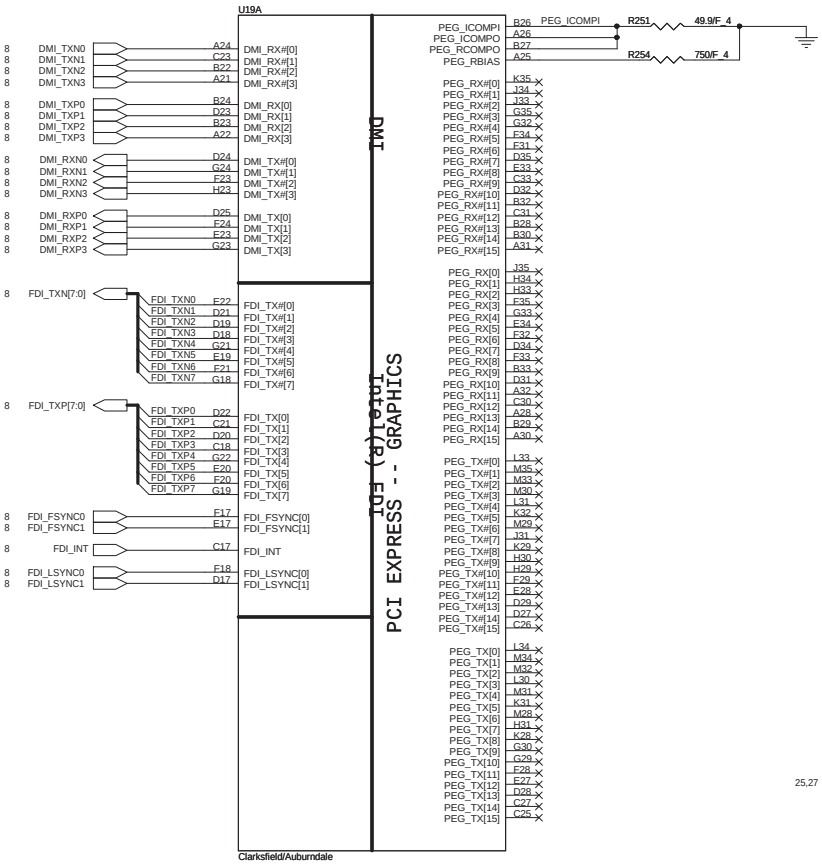

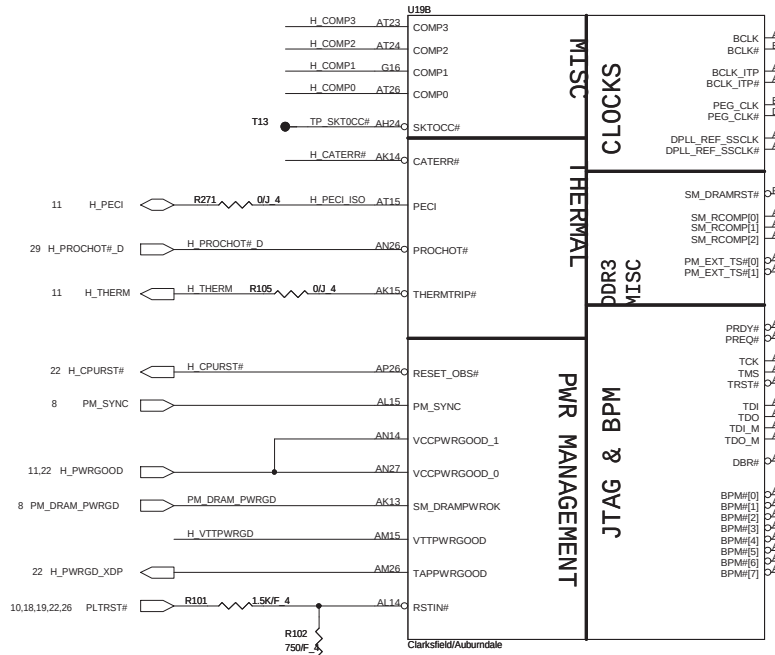

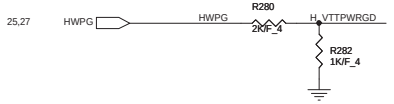

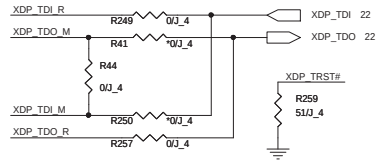

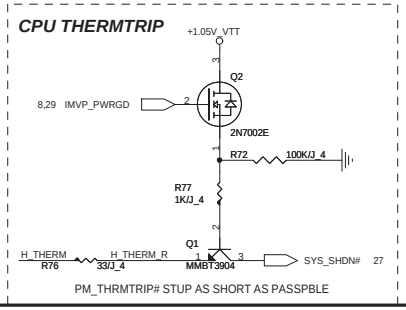

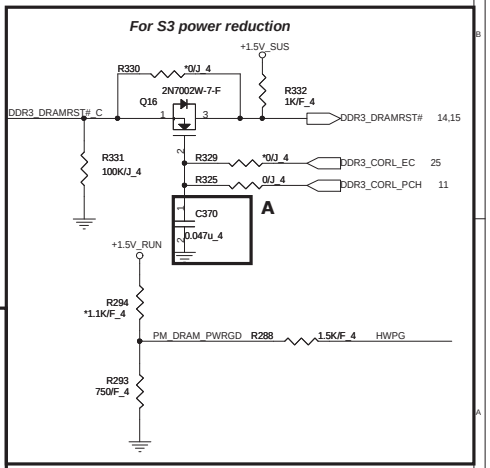

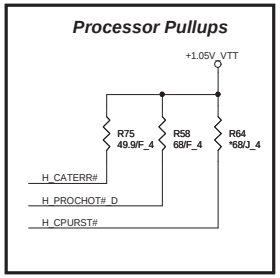

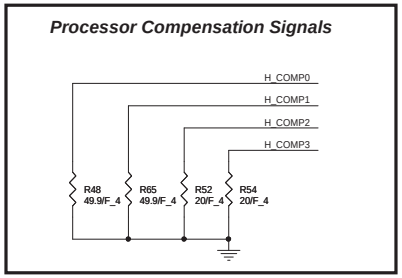

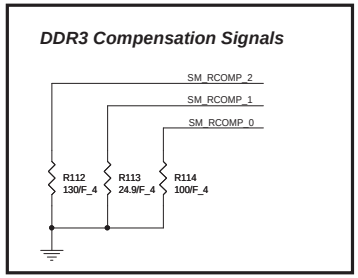

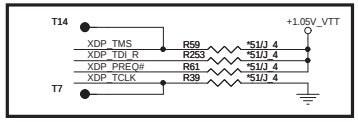

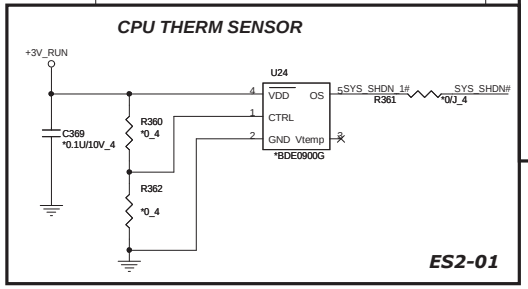

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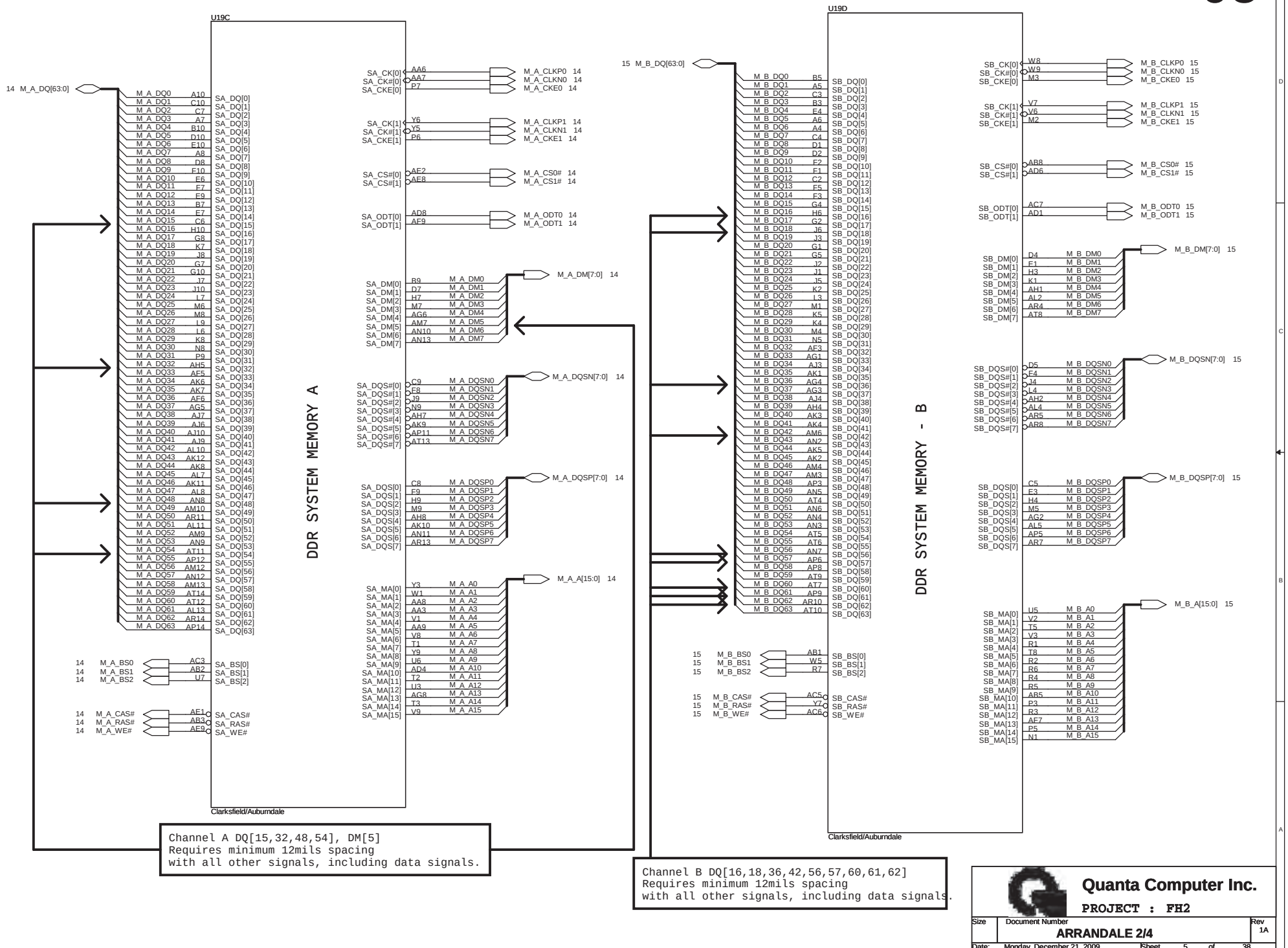
ARRANDALE PROCESSOR (DDR3)

05



Channel A DQ[15,32,48,54], DM[5]
Requires minimum 12mils spacing
with all other signals, including data signals.

Channel B DQ[16,18,36,42,56,57,60,61,62]
Requires minimum 12mils spacing
with all other signals, including data signals.

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ARRANDALE PROCESSOR (GRAPHICS POWER)

CPU Core Power

+VCC_CORE=4.8 max

U19F

1.1V RAIL POWER

CPU CORE SUPPLY

POWER

CPU VIDS

SENSE LINES

+1.05V_VTT=1.8 max

VTT0_43,VTT0_44:(Intel feedback)
They are connected to hidden page for intel validation purpose.

U19G

GRAPHICS POWER

SENSE LINES

GRAPHICS VIDs

DDR3 - 1.5V RAILS

1.1V

1.8V

PCI & DMI

Clarksfield/Auburndale

For S3 power reduction

Check to ensure that 4 stitching caps per SODIMM connector between SODIMM 1.5V and GND are placed as close as possible to the connectors – caps should be evenly distributed between the connectors

VSS_SENSE_VTT:
SC(V1.0)P20
Connect VSS_SENSE_VTT to GND or can be left floating.
Note: CRB has the VSS_SENSE_VTT floating.

PROC_DPRSLPVR:
SC(V1.0)P19:
It is important to have the resistor stuffing options in the design for the Turbo functionality. The stuffing and no-stuffing of the resistors will depend on the POC configuration of AUB and CFD
CRB(V1.0)P67:
uses 1K pull-up and pull-down resistors
CRB default setting is "1"

VCC_SENSE & VSS_SENSE:
SC(V1.0)P19
100- ±1% pull-down to GND near processor

Note:
For Validating IMVP VR R814 should be STUFF and R827 NO_STUFF

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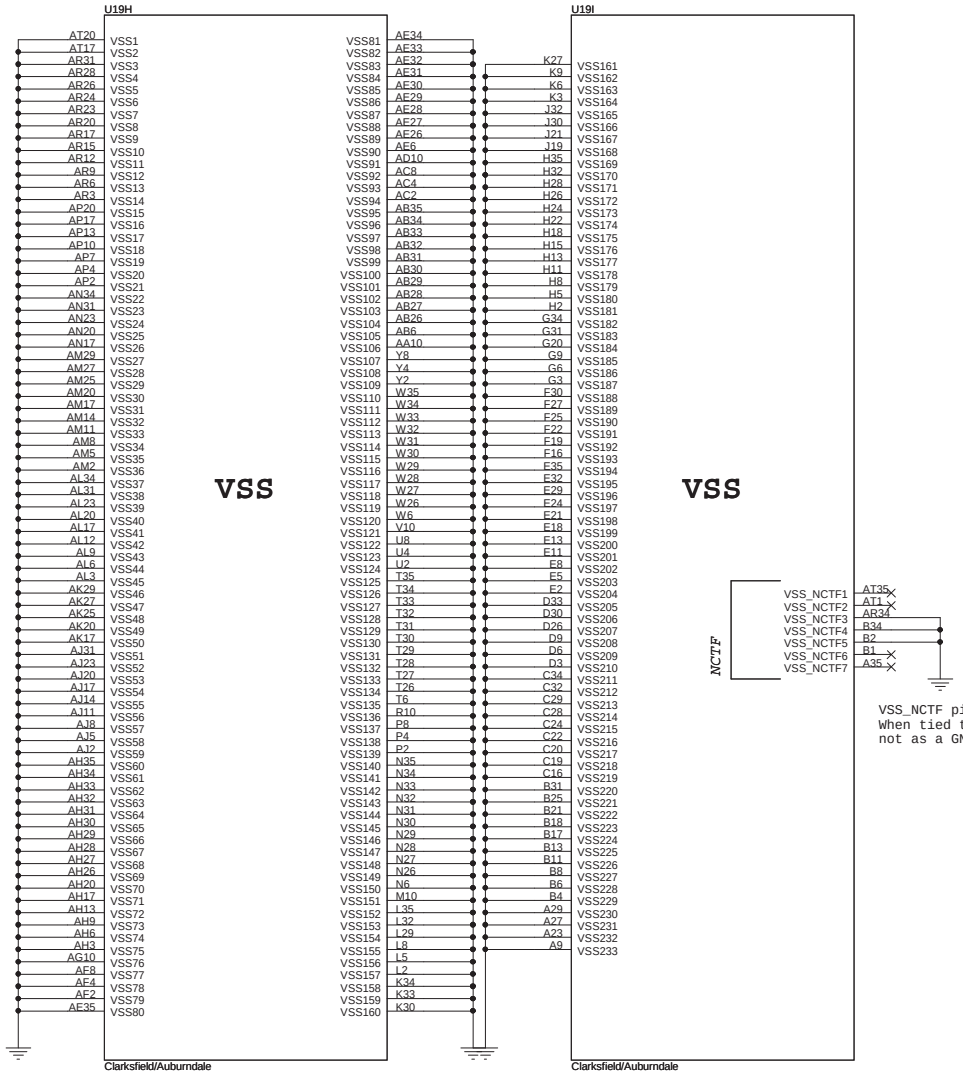
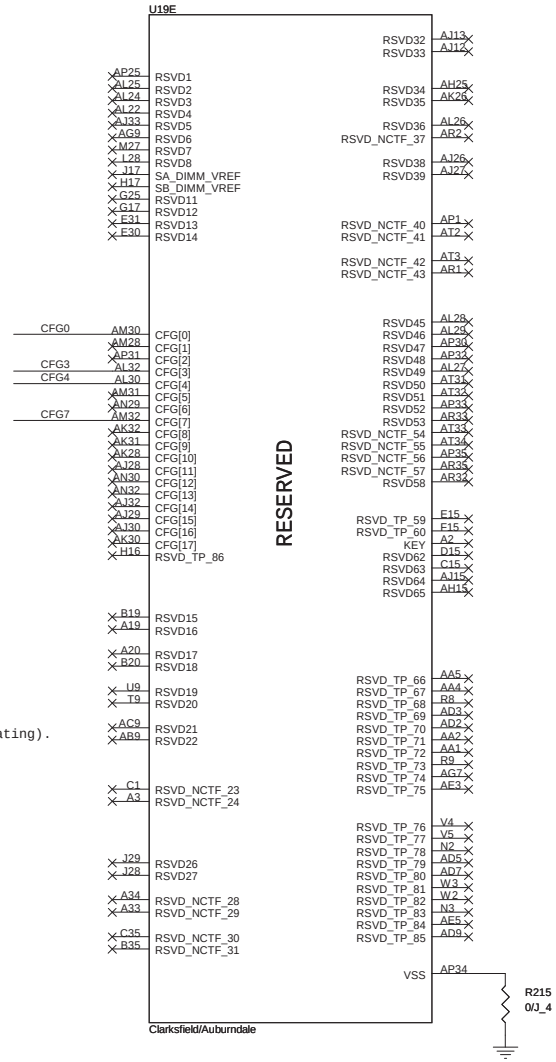
AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

ARRANDALE PROCESSOR (GND)



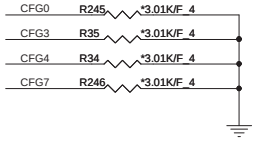
VSS_NCTF pins can be connected to GND or left as NC (floating). When tied to GND they should be routed as trace and not as a GND plane.

ARRANDALE PROCESSOR(RESERVED, CFG)



Can be left NC is Intel CRM implementation; ESD/DG recommendation to GND

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.



	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

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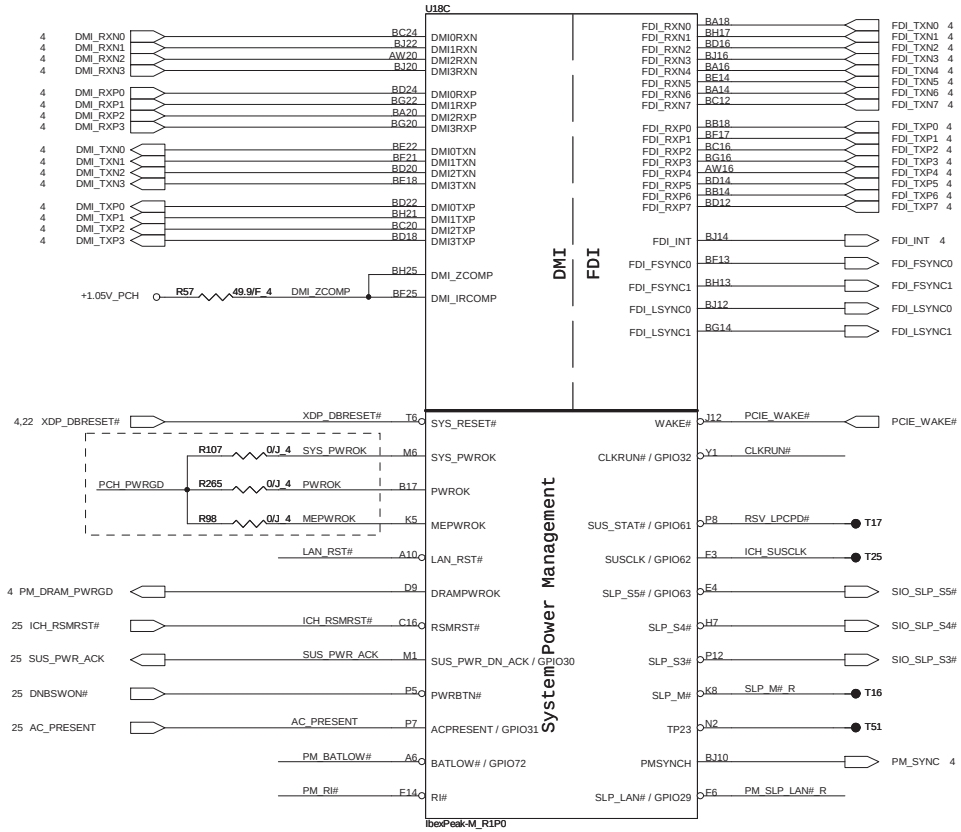
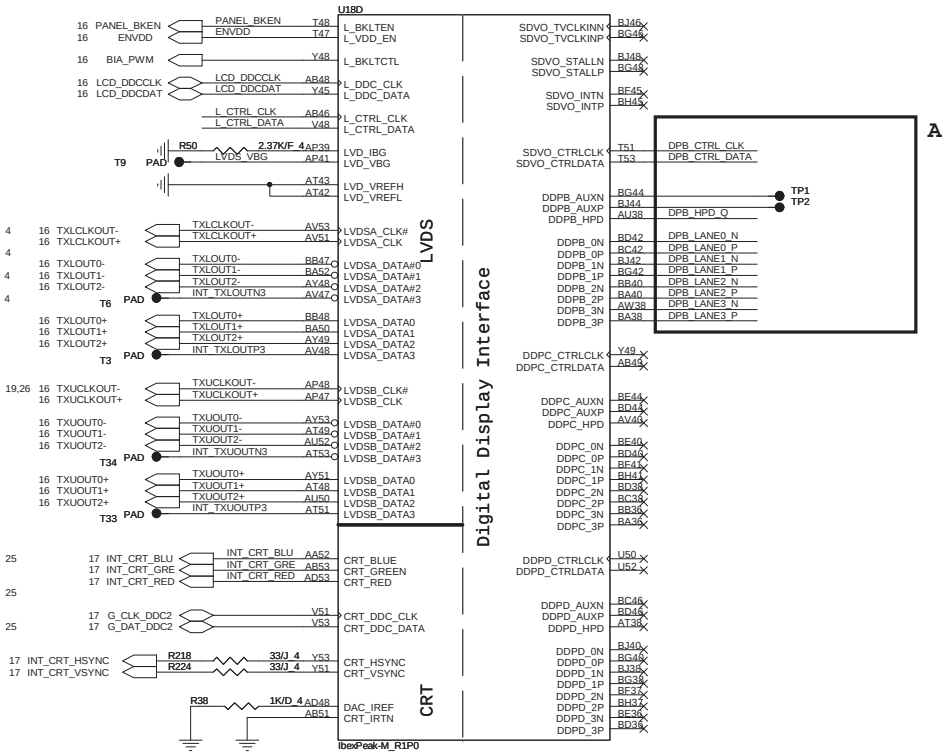
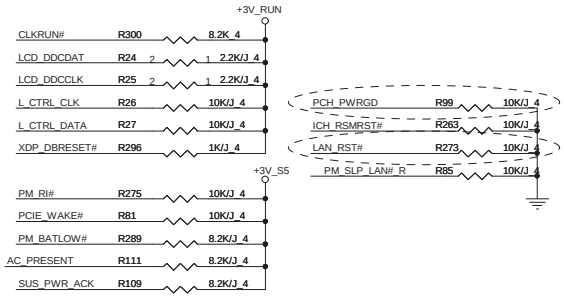
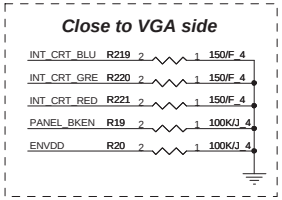
IBEX PEAK-M (DMI,FDI,GPIO)

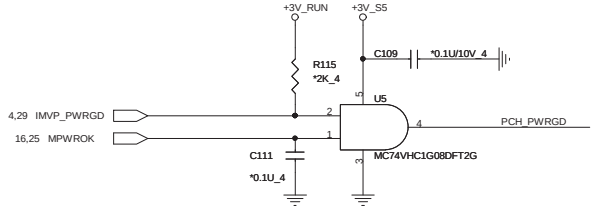


IBEX PEAK-M (LVDS,DDI)

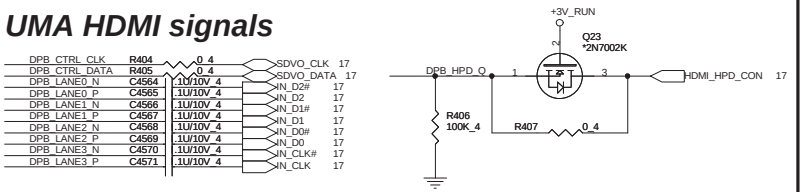








UMA HDMI signals



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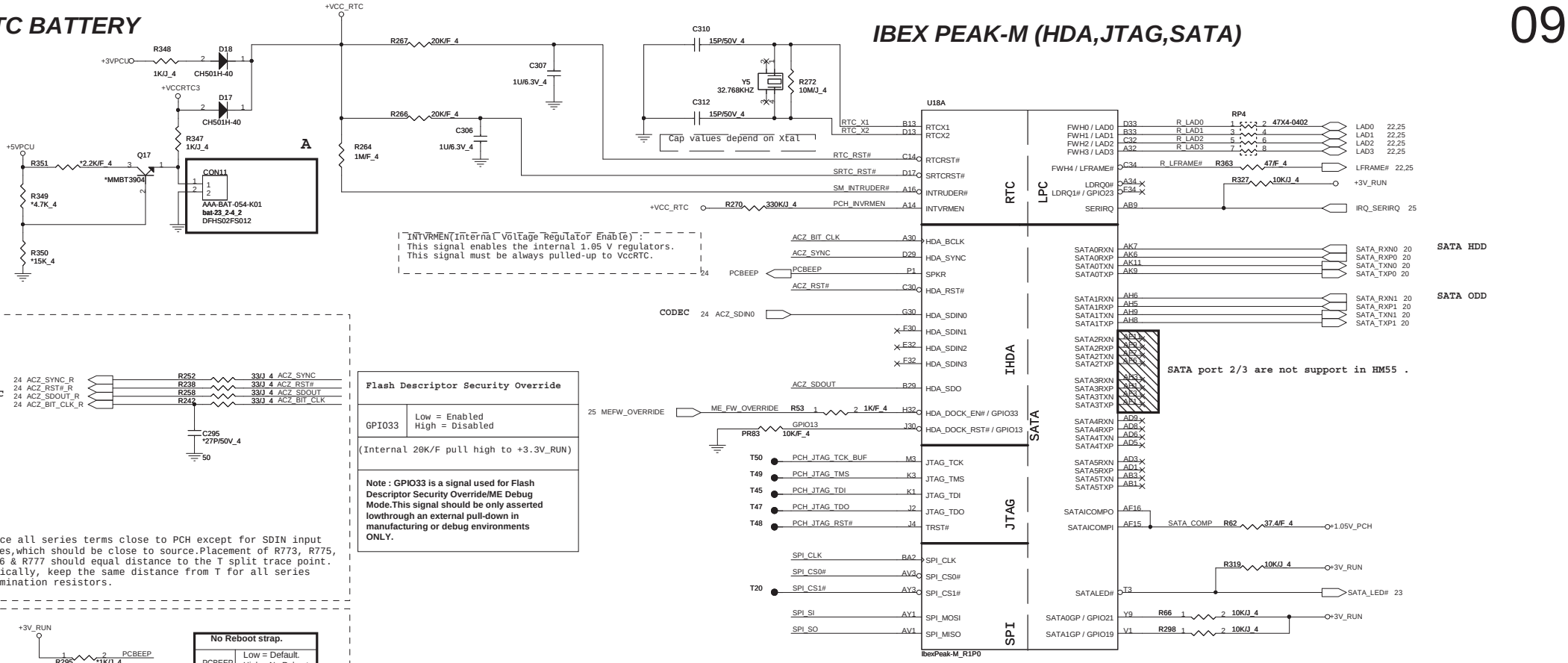
RTC BATTERY

IBEX PEAK-M (HDA,JTAG,SATA)

09



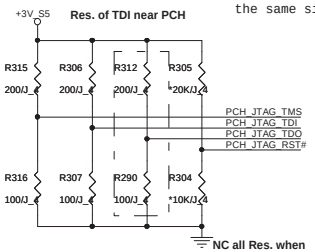
Place all series terms close to PCH except for SDIN input lines,which should be close to source.Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

Flash Descriptor Security Override	
GPIO33	Low = Enabled High = Disabled
(Internal 20K/F pull high to +3.3V_RUN)	

Note : GPIO33 is a signal used for Flash Descriptor Security Override/ME Debug Mode.This signal should be only asserted lowthrough an external pull-down in manufacturing or debug environments ONLY.

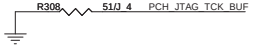
No Reboot strap.	
PCBEEP	Low = Default. High = No Reboot.

JTAG
Test Pads are need to put on the same side of mother board.



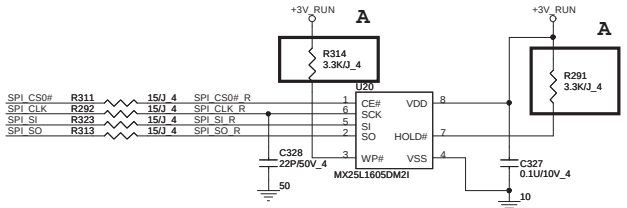
NC all Res. when PCH is production stage.

Res. of TDO
PCH ES1 stage : NC
PCH ES2 stage : pop

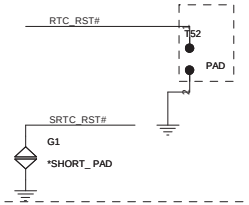


Note : Only pop when PCH is production stage & need "JTAG boundary Scan". Remember to depop XDP side Res.

For PCH 32Mbit (4M Byte)



RESET JUMP (Near ROOM DOOR)



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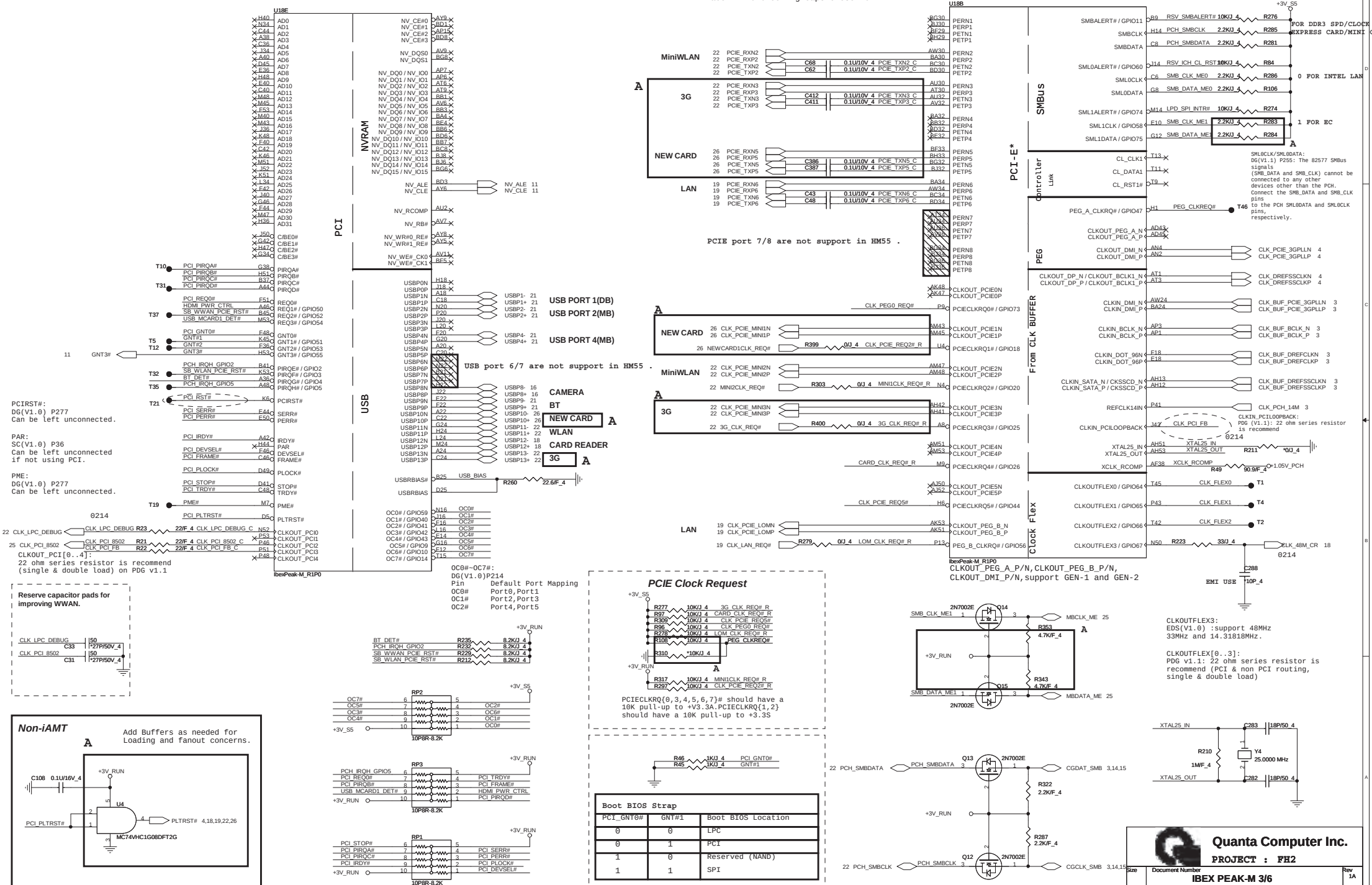
IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (PCI-E,SMBUS,CLK)

Place TX DC blocking caps close PCH.



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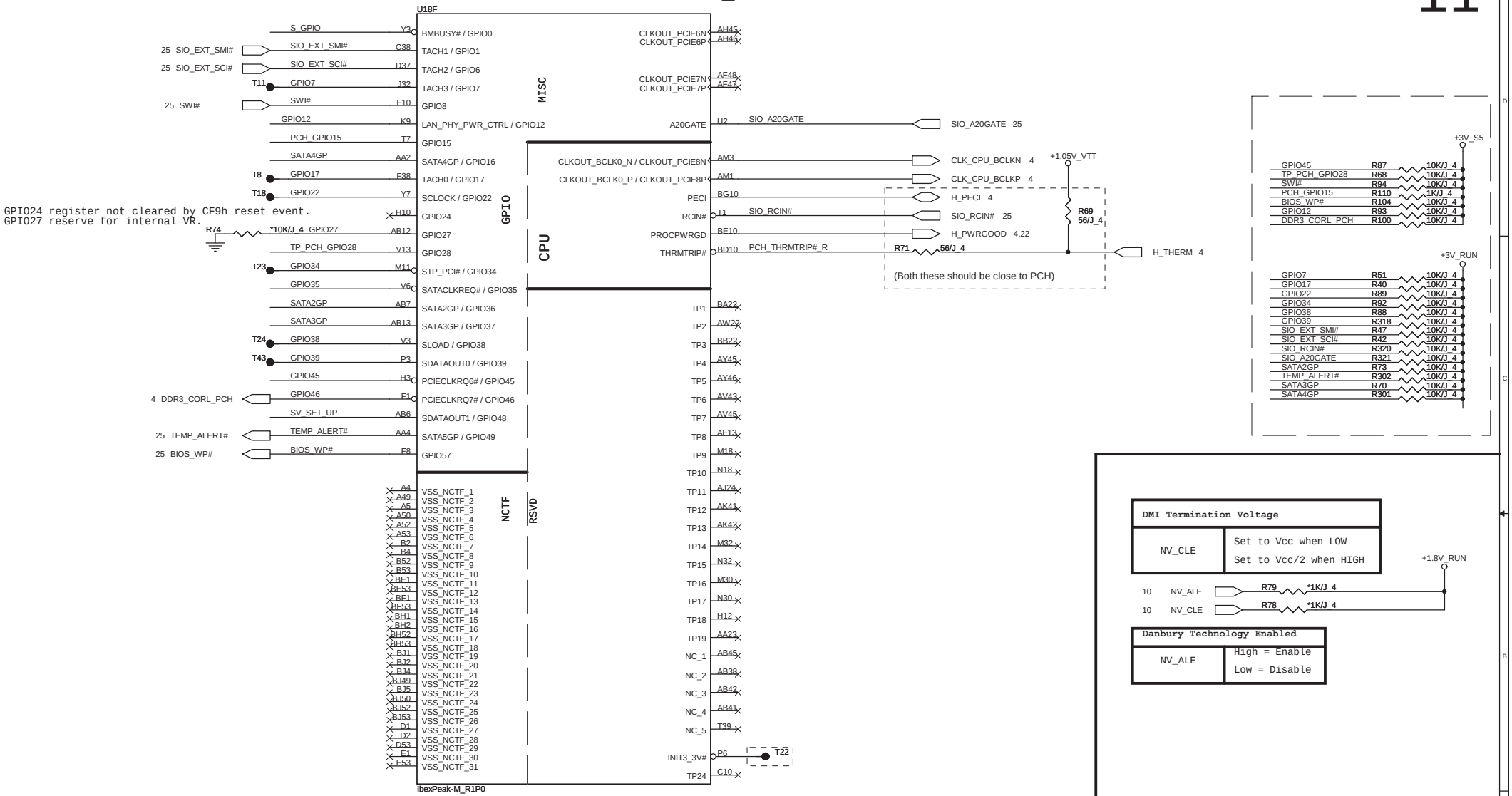
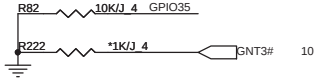
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



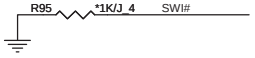
GPIO24 register not cleared by CF9h reset event.
GPIO27 reserve for internal VR.

DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable



A16 swap override Strap/Top-Block Swap Override jumper	
GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default



Integrated Clock Chip Enable (Reserve to validate for future platforms)	
RSV_WOL_EN (GPIO8)	Enable when sampled low Disable when sampled high

SV_SET_UP	1-X High = Strong (Default)

BMBUSY#:
If not used, require a weak pull-up (8.2- KΩ to 10 kΩ) to Vcc3_3.
CRB(V1.0)P28: it has 1K PU and 100 ohm on this net for validation purpose.

BMBUSY#:(Intel feedback)
Follow CRB checklist, 1K is
for intel BIOS validation purpose.

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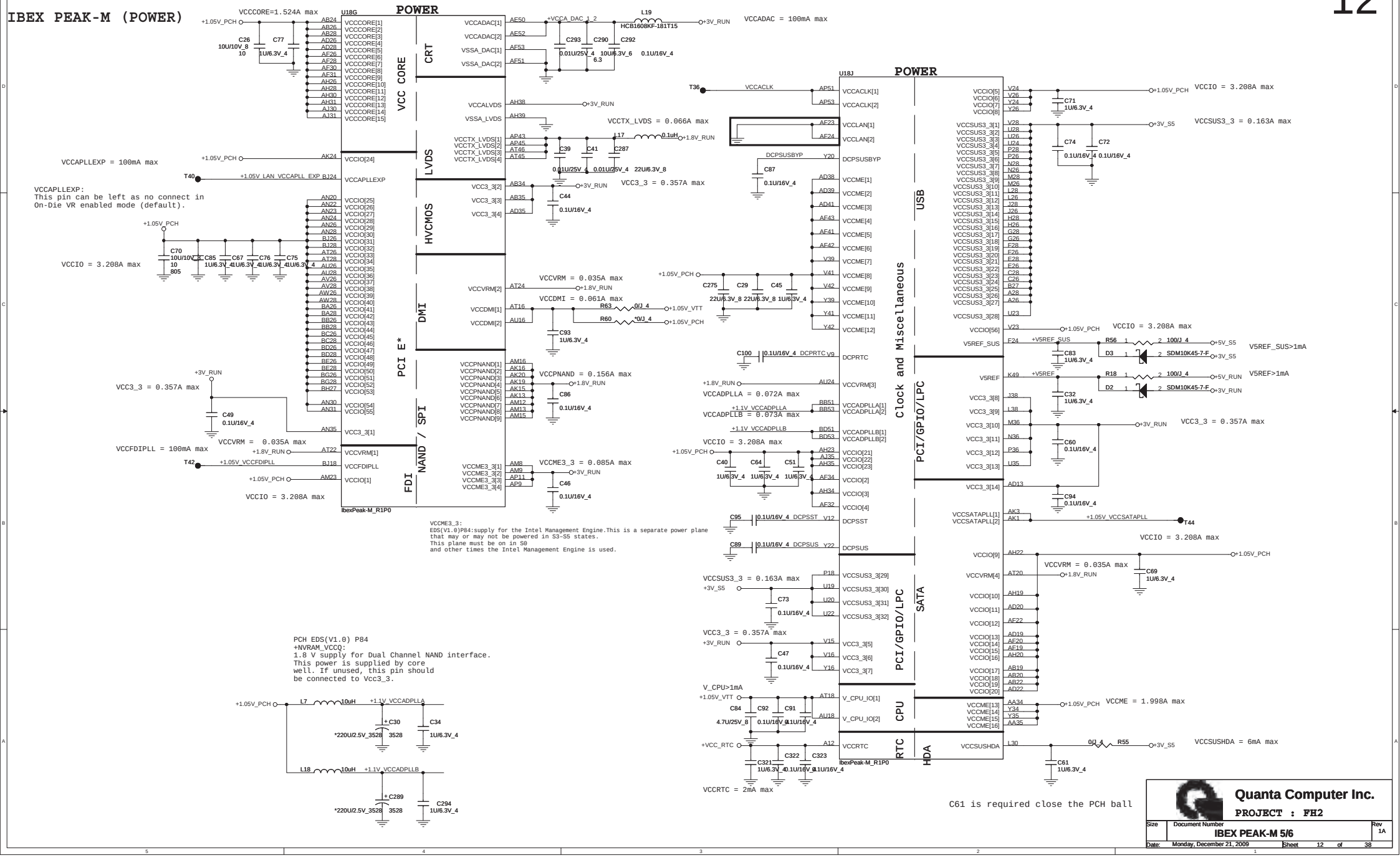
IBEX PEAK-M (POWER)



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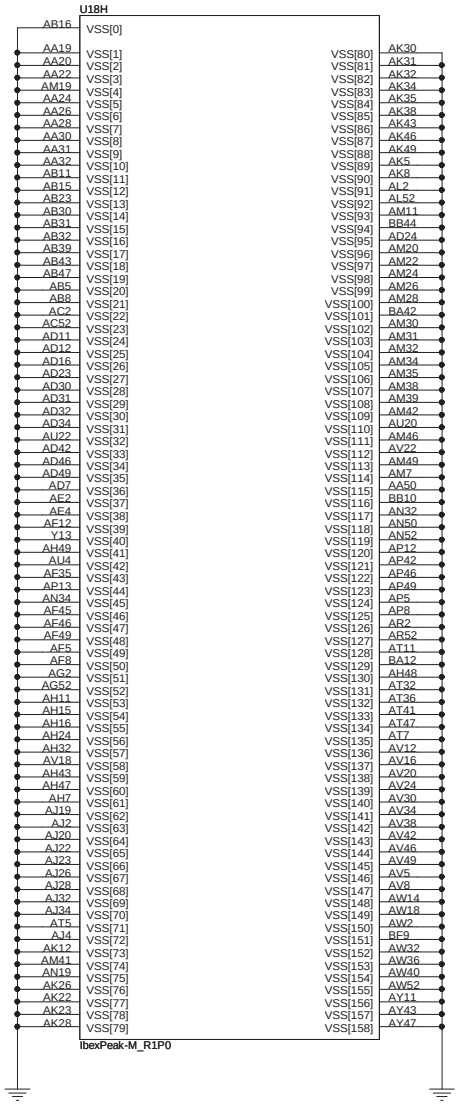
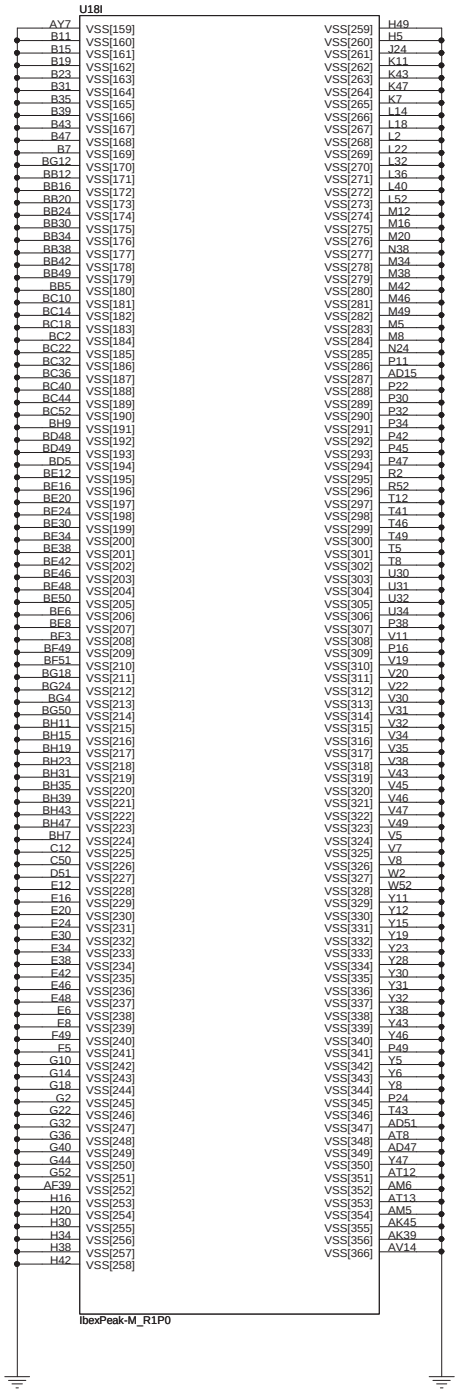
IBEX PEAK-M (GND)





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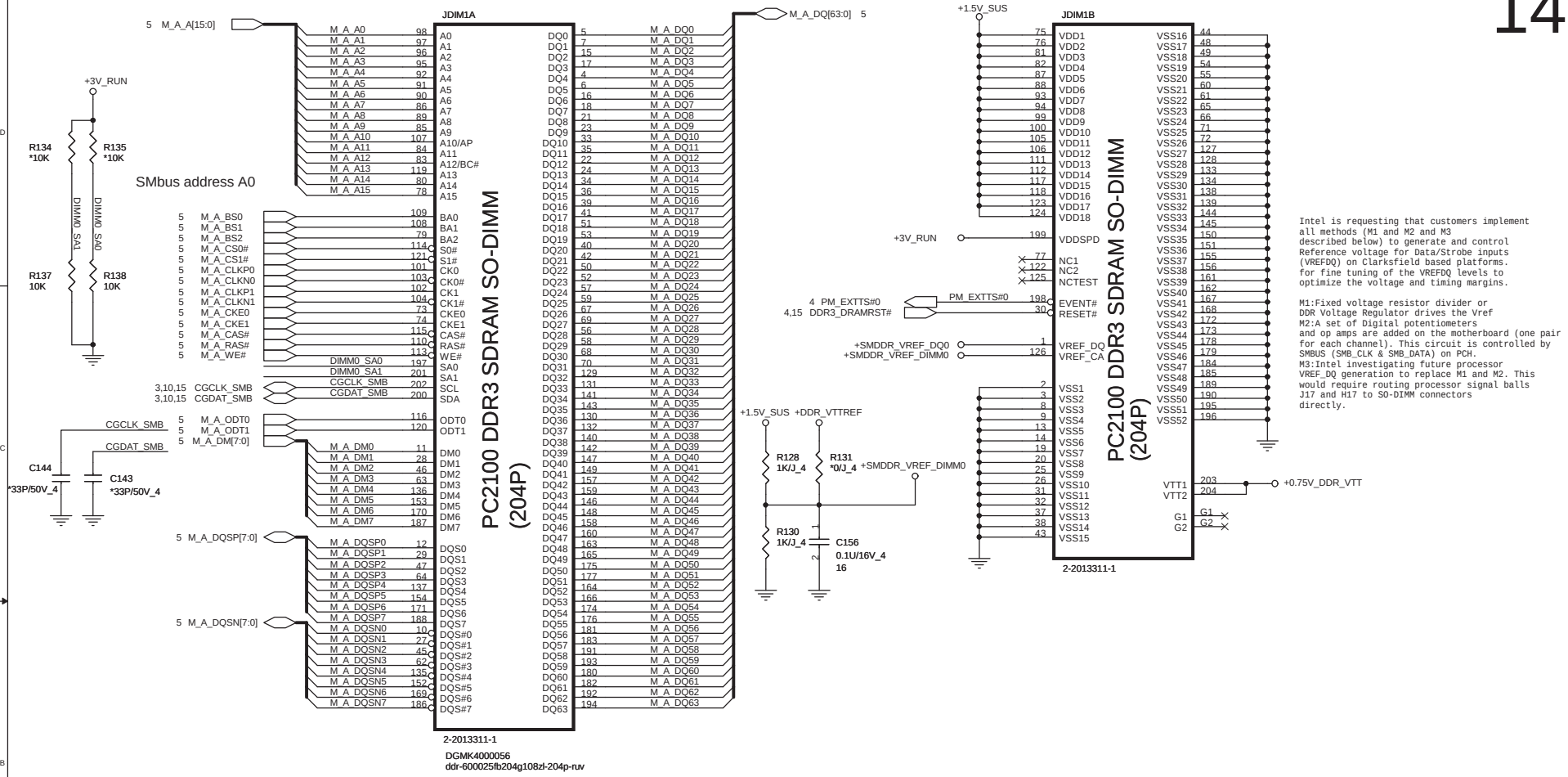
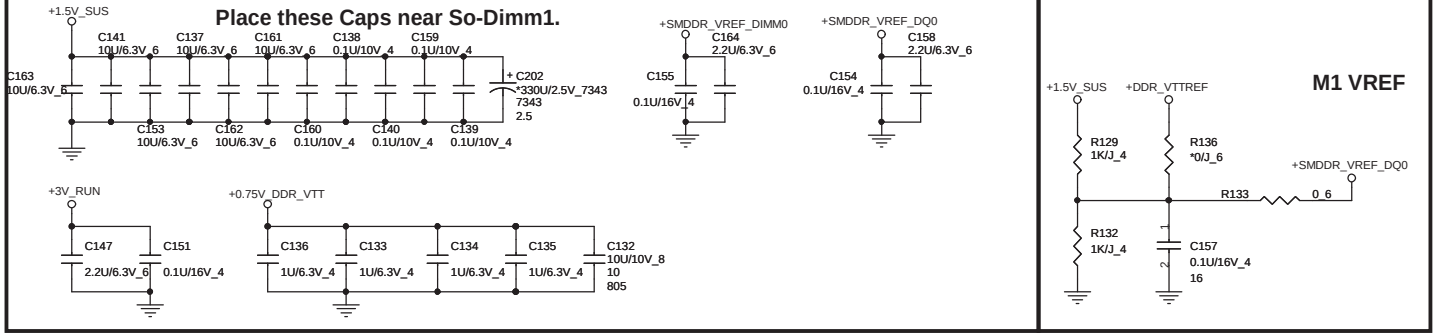


Intel is requesting that customers implement all methods (M1 and M2 and M3 described below) to generate and control Reference voltage for Data/Strobe inputs (VREFDQ) on Clarksfield based platforms. for fine tuning of the VREFDQ levels to optimize the voltage and timing margins.

M1:Fixed voltage resistor divider or DDR Voltage Regulator drives the Vref
M2:A set of Digital potentiometers and op amps are added on the motherboard (one pair for each channel). This circuit is controlled by SMBUS (SMB_CLK & SMB_DATA) on PCH.
M3:Intel investigating future processor VREF_DQ generation to replace M1 and M2. This would require routing processor signal balls J17 and H17 to SO-DIMM connectors directly.



Quanta Computer Inc.

PROJECT : FH2

Size	Document Number	Rev
	DDR3 DIMM-1	1A
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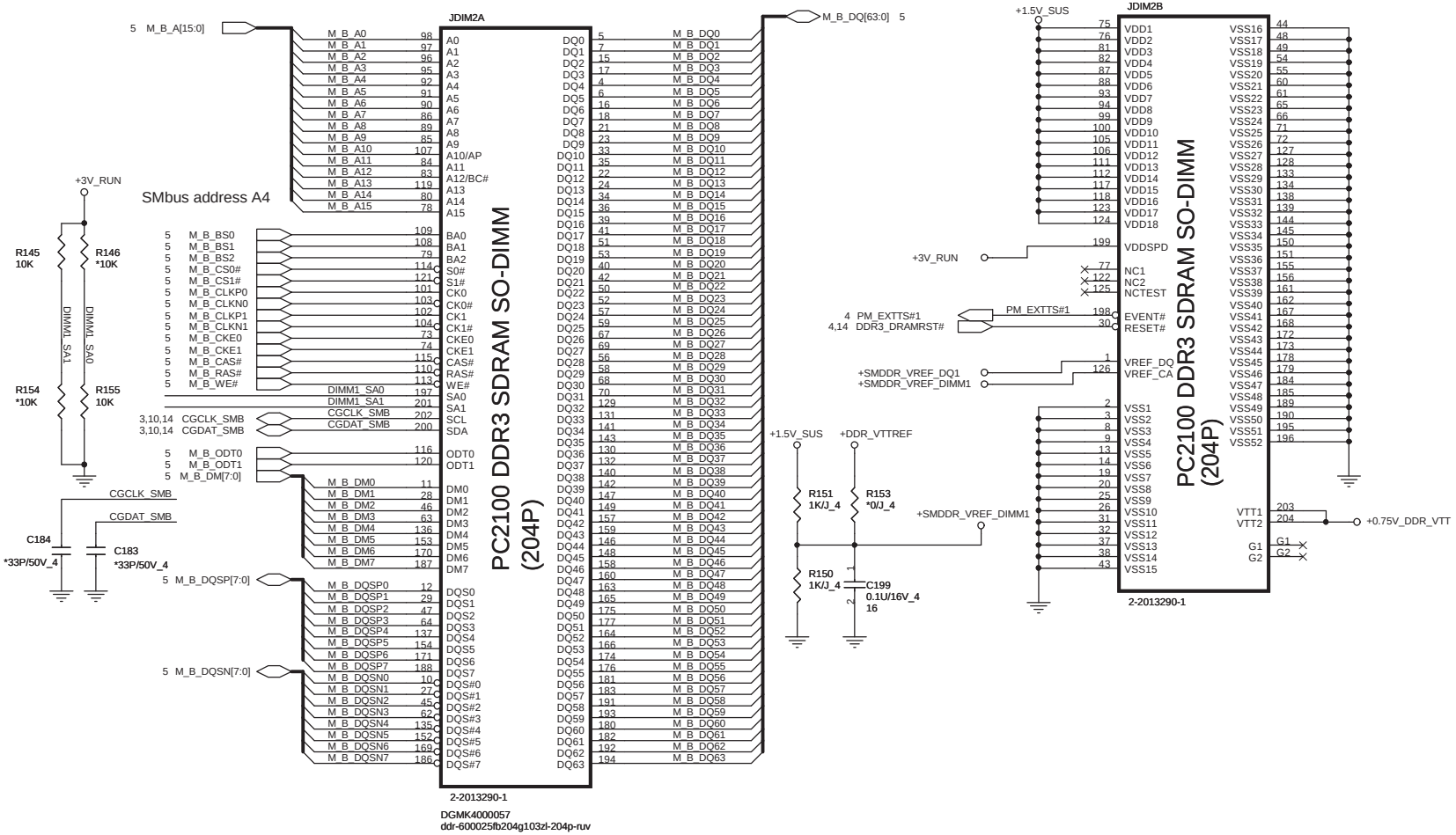
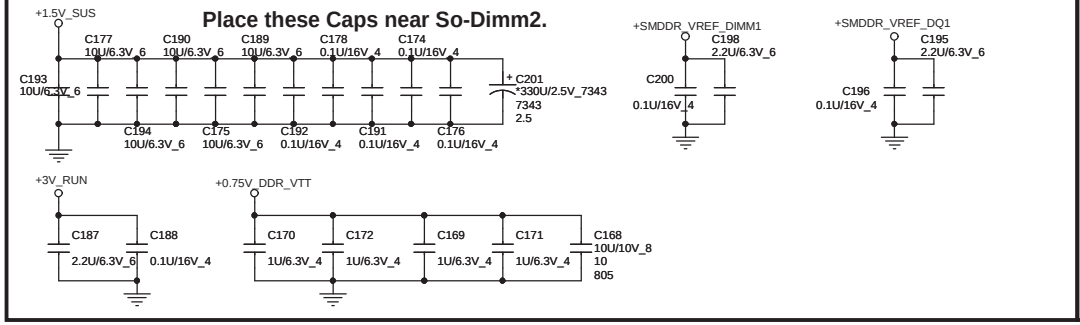
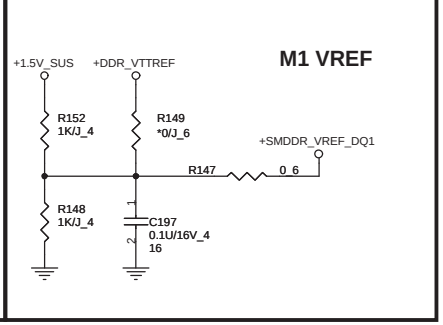


Place these Caps near So-Dimm2.



M1 VREF



Quanta Computer Inc.

PROJECT : FH2

Size	Document Number	Rev
	DDR3 DIMM-2	1A
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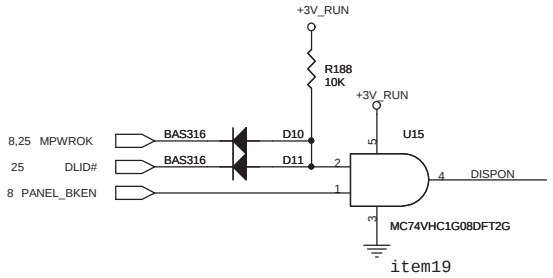
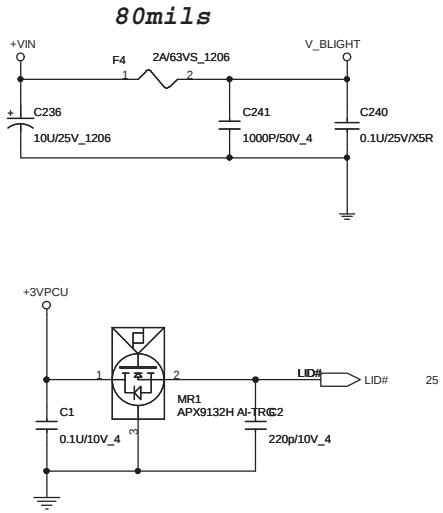
Backlight Control(LDS)

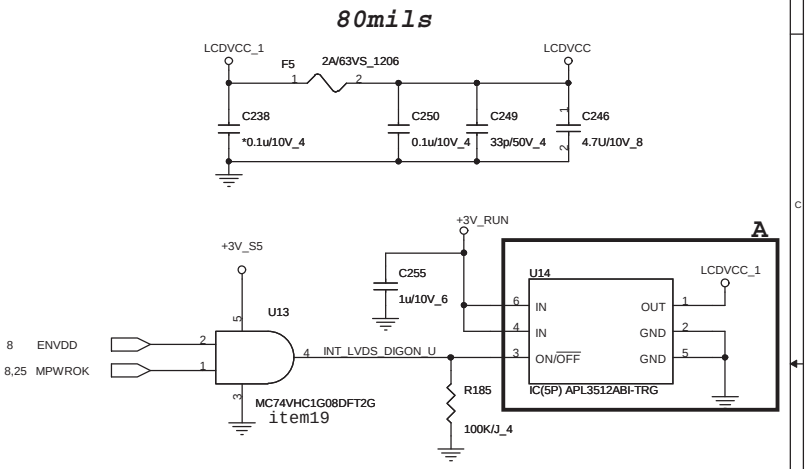


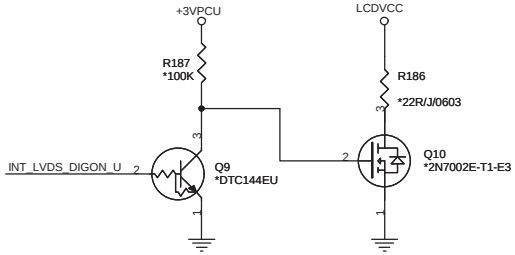
BACKLIGHT POWER



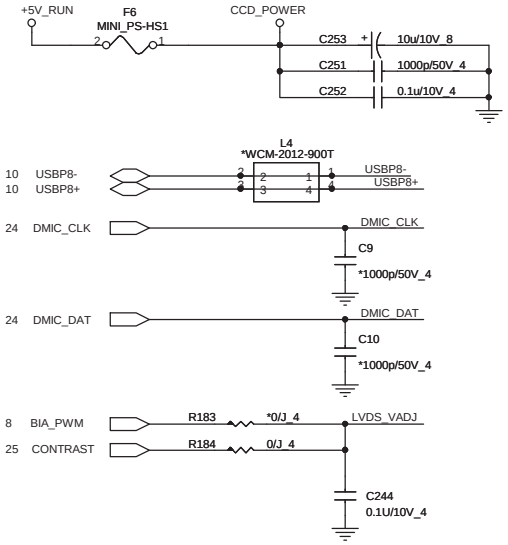
LED Panel POWER SWITCH(LVDS)

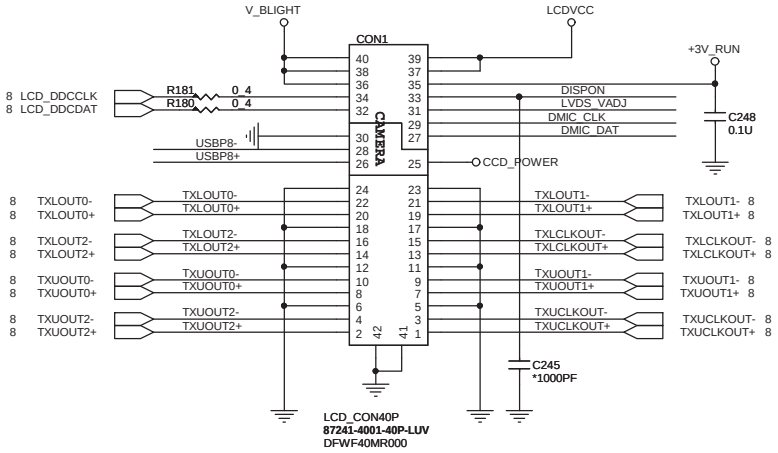
16





LVDS/CCD





Quanta Computer Inc.

PROJECT : FH2

Size	Document Number	Rev
	LCD/LED Panel/CCD	1A
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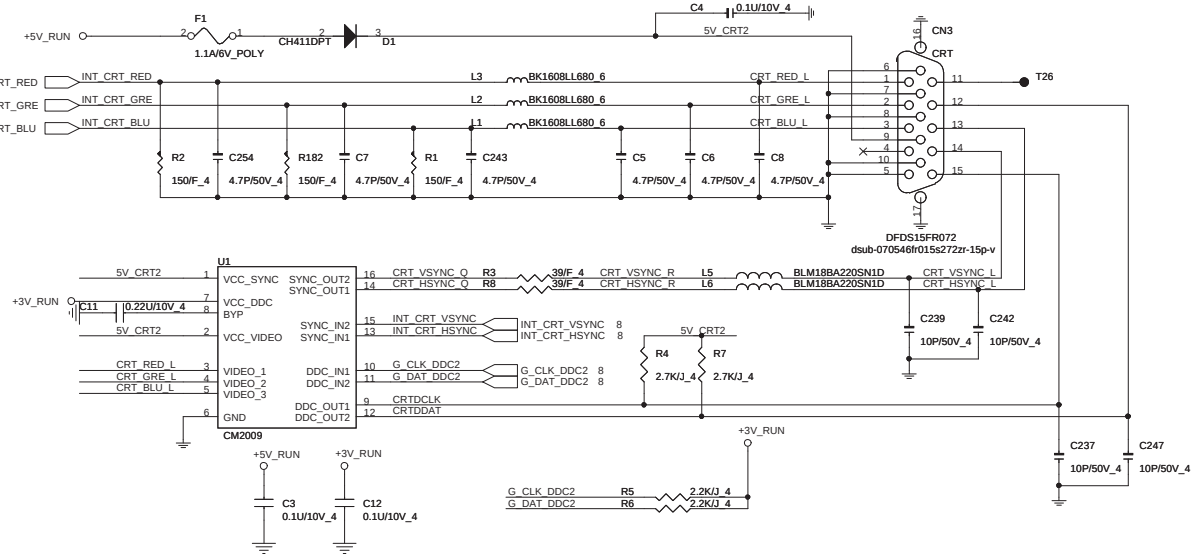
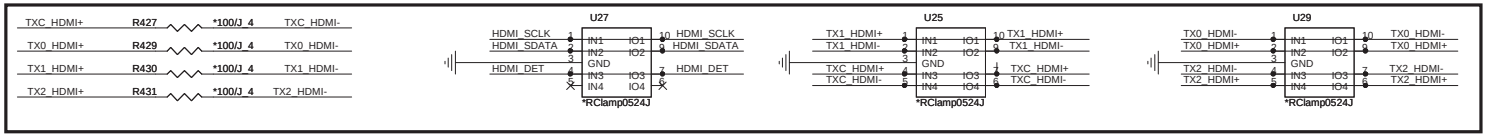
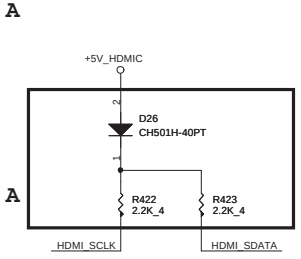
CRT CONN/DDC LEVEL SHIFT

40mils

TBD CN5500 FOOTPRINT



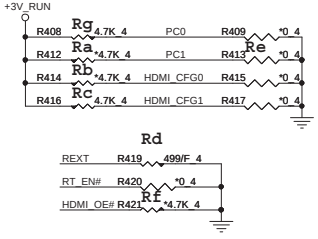


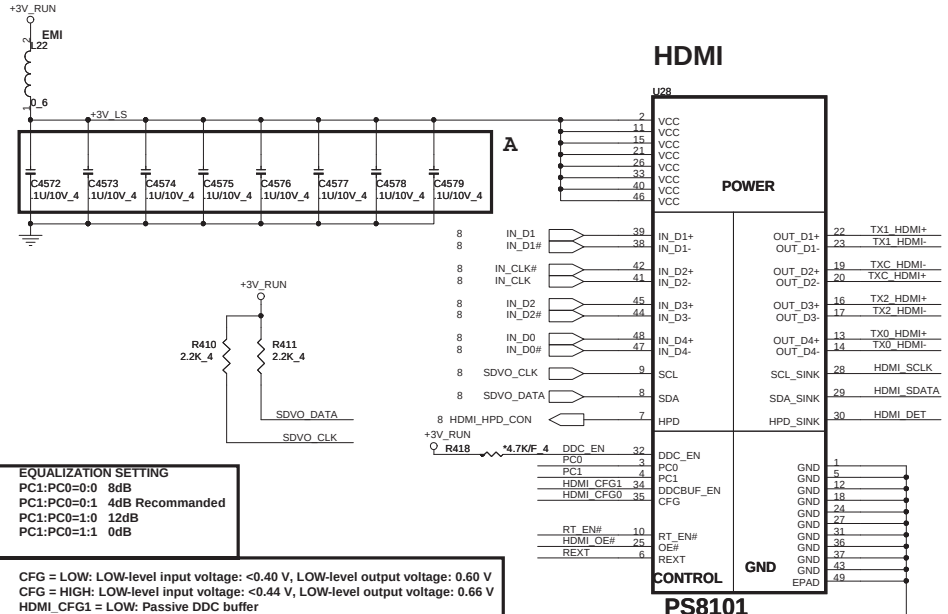


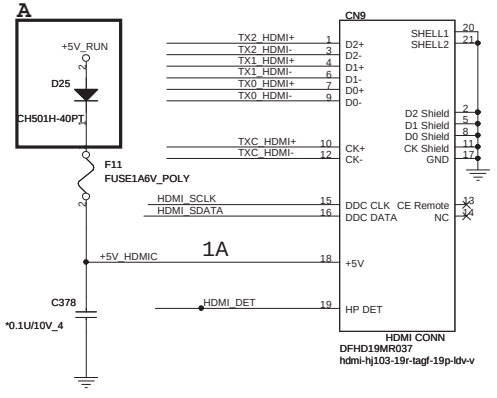
reserve for EMI

Signals		PDT	CHR	PIM
PC1	Ra	NC	4.7K	NC
HDMI_CFG0	Rb	NC	NC	NC
HDMI_CFG1	Rc	4.7K	NC	NC
REXT	Rd	499	1.2K	4.7K
PC1	Re	NC	NC	4.7K
HDMI_OE#	Rf	NC	4.7K	NC
PC0	Rg	4.7K	4.7K	4.7K

Vendor:PDT P/N:AL008101000
Vendor:CHR P/N:AL007318001
Vendor:PIM P/N:ALP411LS004







EQUALIZATION SETTING
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommanded
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB

CFG = LOW: LOW-level input voltage: <0.40 V, LOW-level output voltage: 0.60 V
CFG = HIGH: LOW-level input voltage: <0.44 V, LOW-level output voltage: 0.66 V
HDMI_CFG1 = LOW: Passive DDC buffer
HDMI_CFG1 = HIGH: Active DDC buffer

Quanta Computer Inc.
PROJECT : FH2

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	CRT CONN/HDMI	1A
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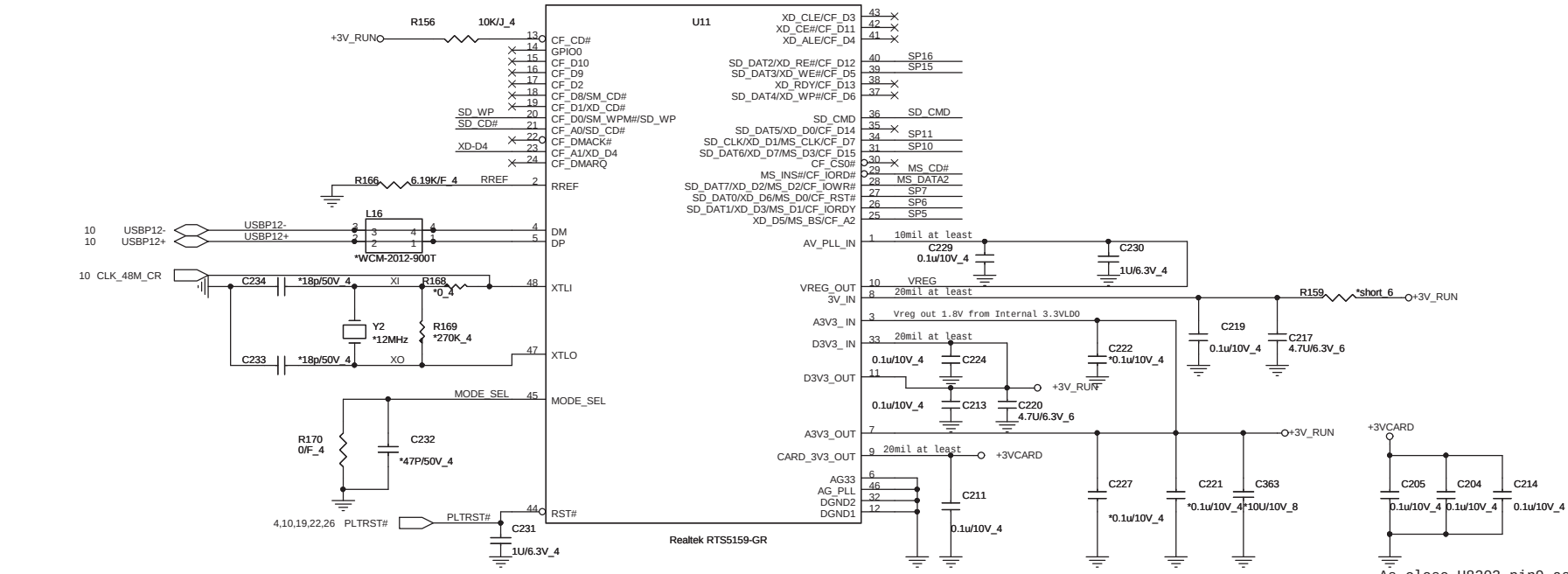
Card Reader



As close U8203 pin9 as possible

XD-D4 R158 short_4 SD_DAT1

For 5158E

SP7 R162 short_4 MS_DATA0_SD_DAT0

SP6 R161 short_4 MS_DATA1

SP16 R171 short_4 SD_DAT2

SP5 R160 short_4 MS_BS

SP15 R167 short_4 SD_DAT3

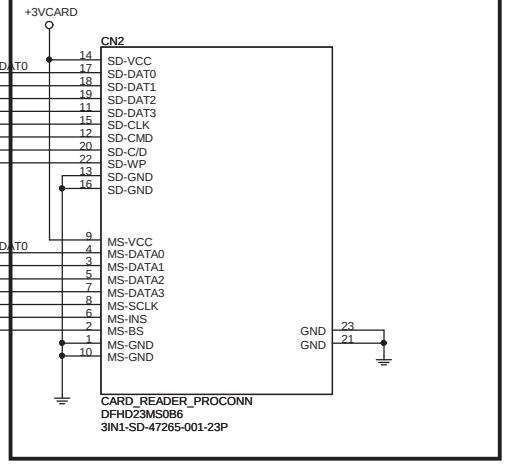
R164 short_4 SD_CLK

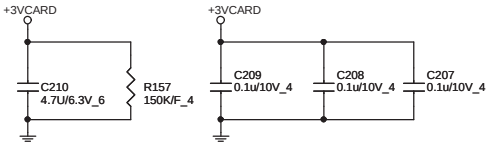
SP11 R165 short_4 MS_CLK

C226 *22P

SP10 R163 short_4 MS_DATA3

A





Quanta Computer Inc.

PROJECT : FH2

Size	Document Number	Rev
	Card Reader RTS5159	1A
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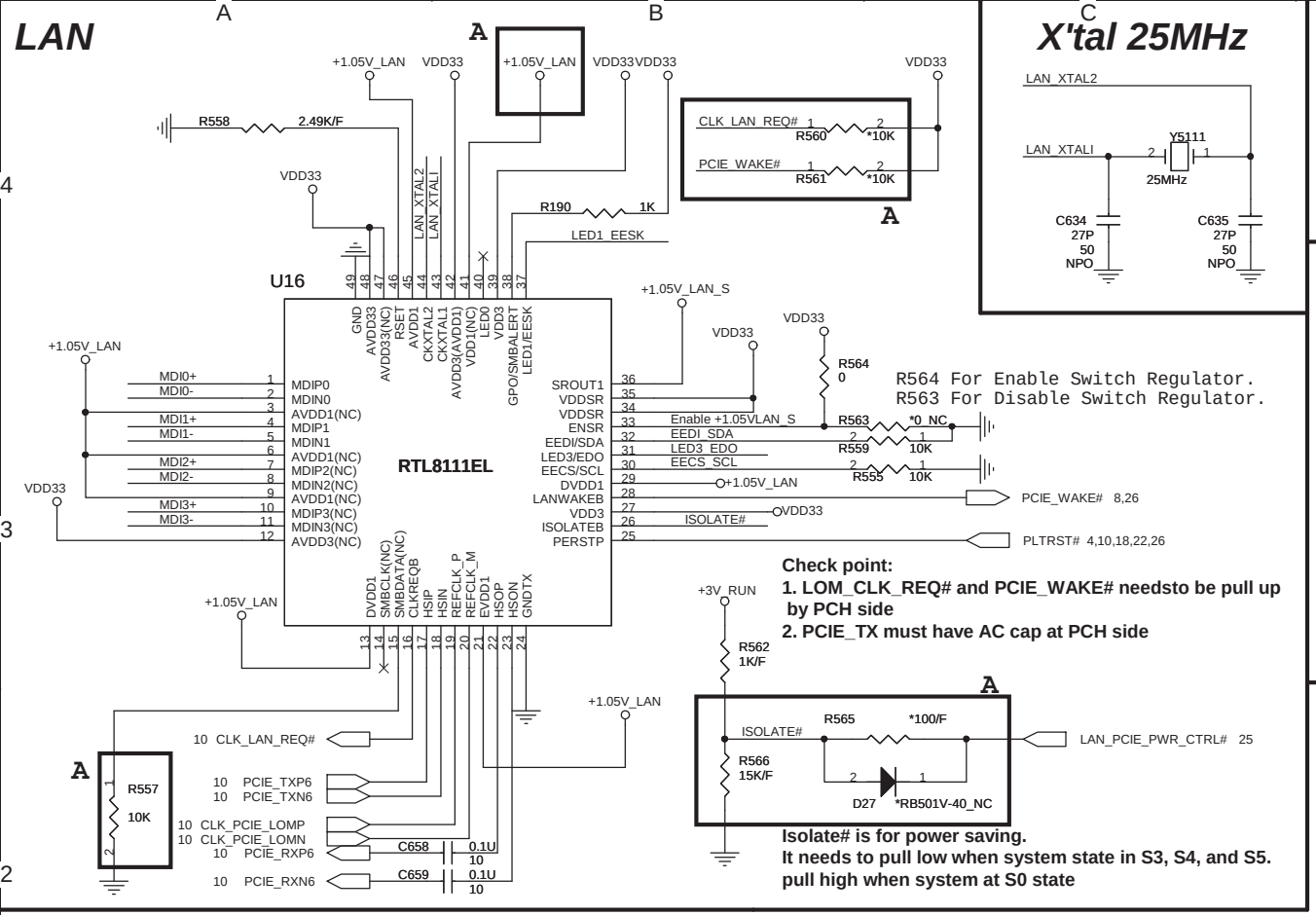
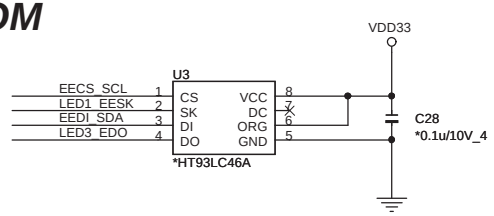
LAN

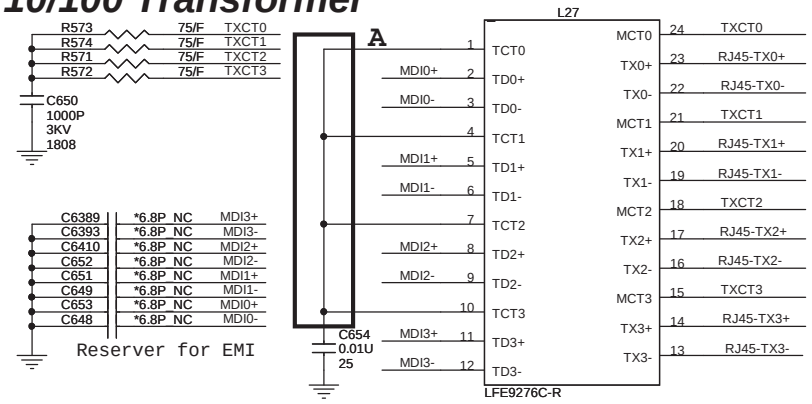


X'tal 25MHz

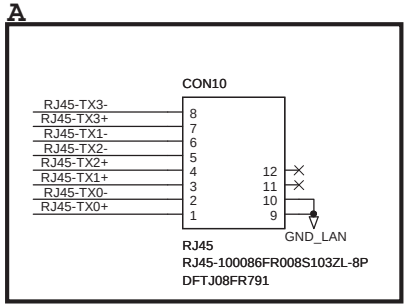
LAN EEPROM

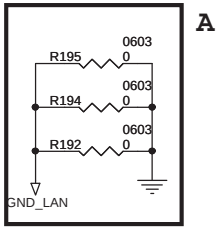


10/100 Transformer

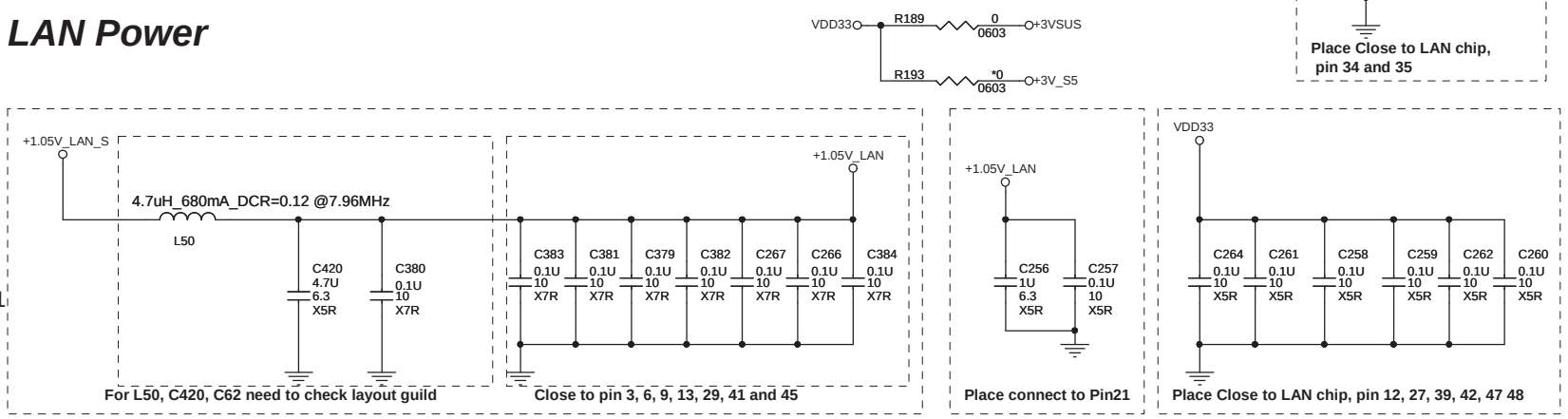


RJ45





LAN Power



REQ by layout

Quanta Computer Inc.		
PROJECT : FH2		
Size	Document Number: LAN_RTL8111E-GR/RJ45	Rev 1A
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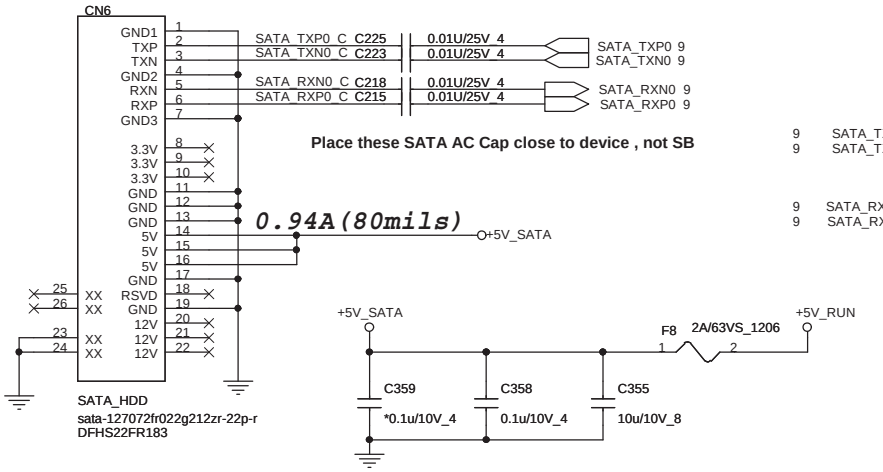
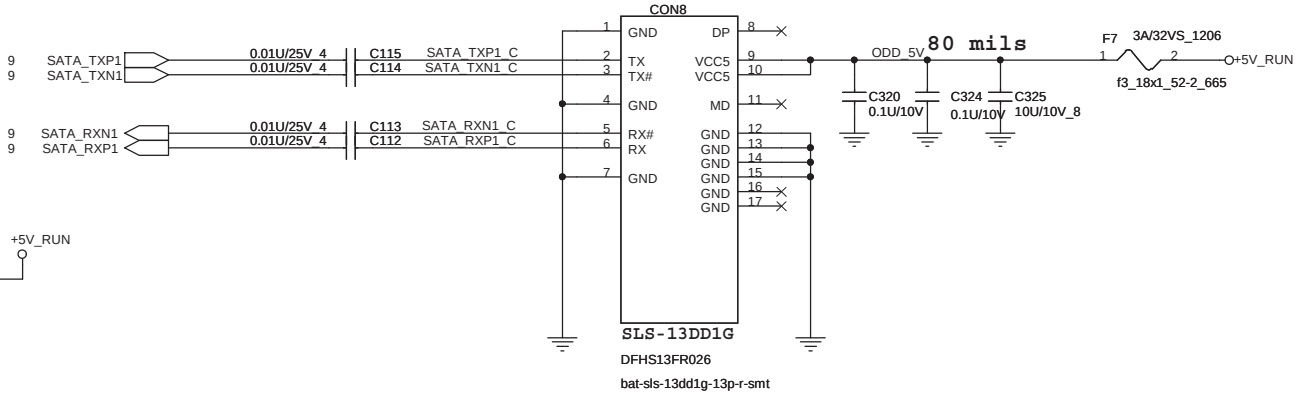
2.5" SATA HDD

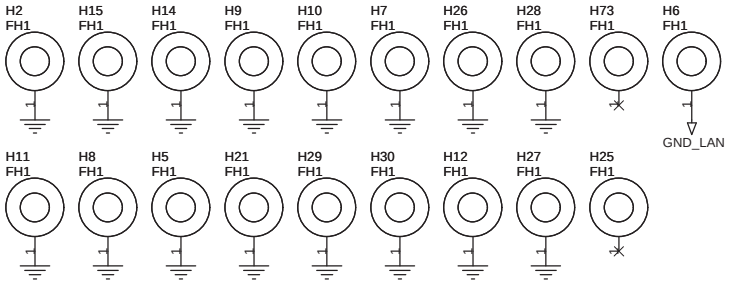


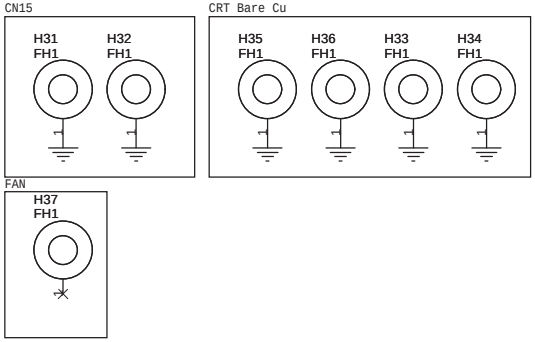
SATA ODD

ODD CONN

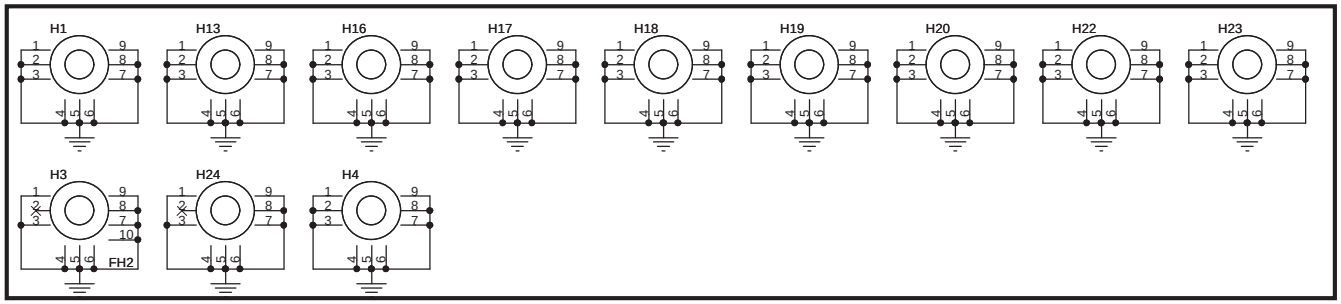


Hole

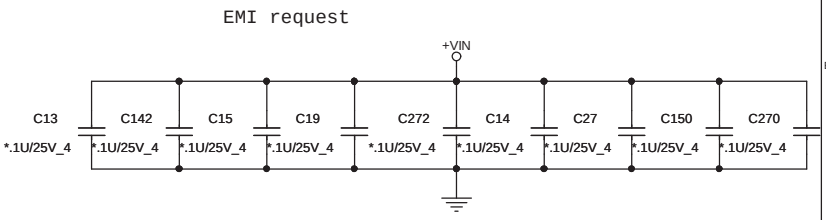




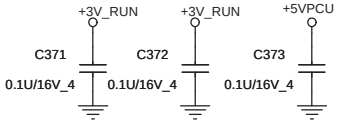
ESD



Decoupling Cap



EMI(Decoupling Cap)



Quanta Computer Inc.

PROJECT : FH2

Size	Document Number	Rev
	HDD/ ODD/HOLE	1A

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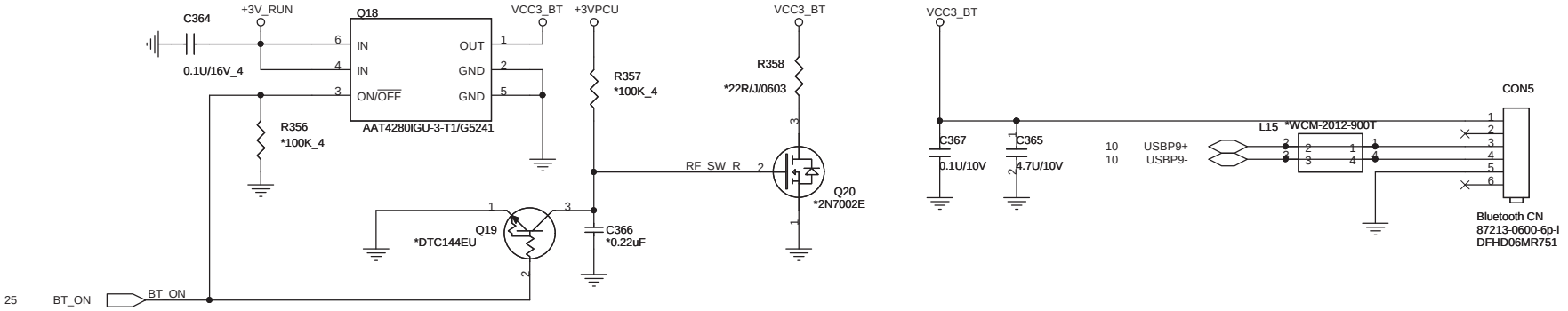
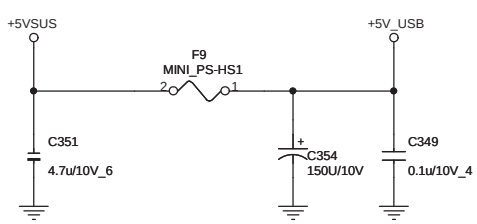
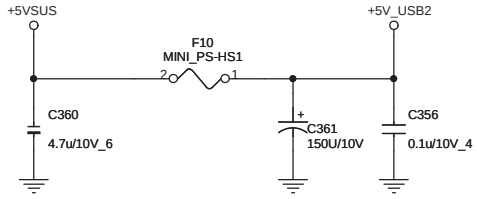
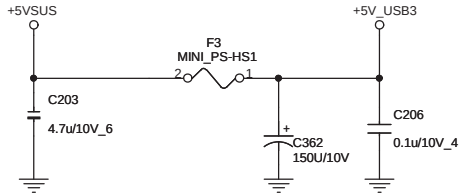
BuleTooth (BTM)

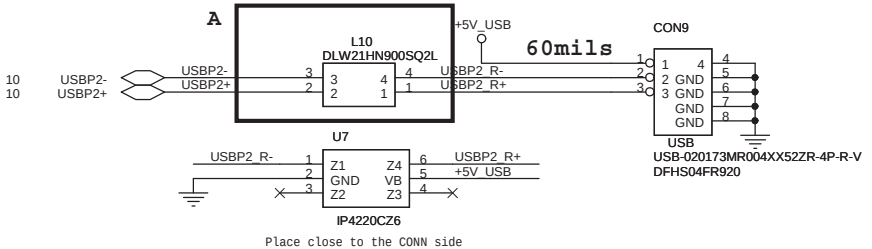


USB Connector

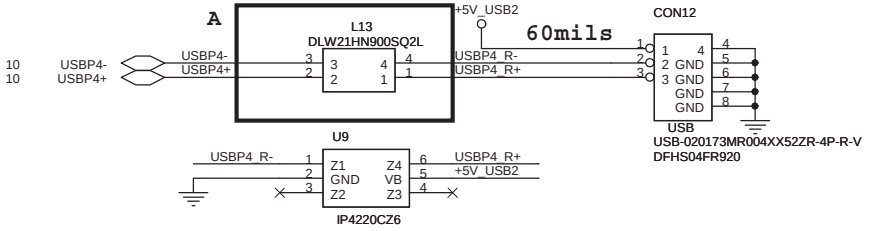


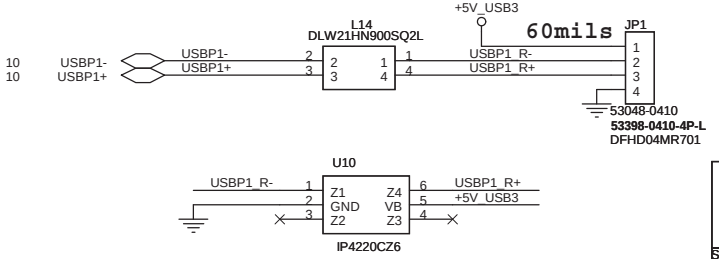






Place close to the CONN side





Quanta Computer Inc.

PROJECT : FH2

Size	Document Number	Rev
	USB/BLUE TOOTH	1A
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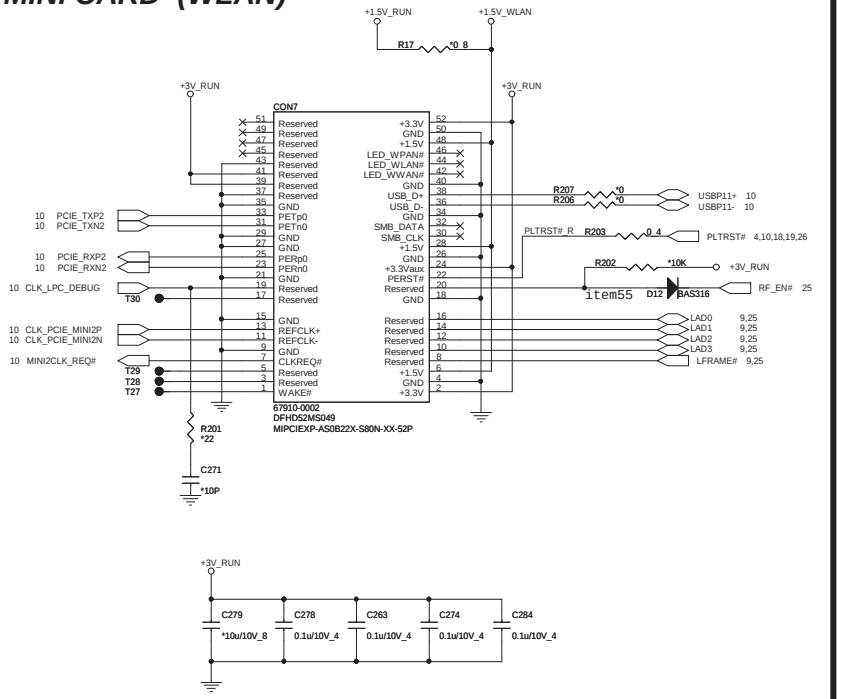
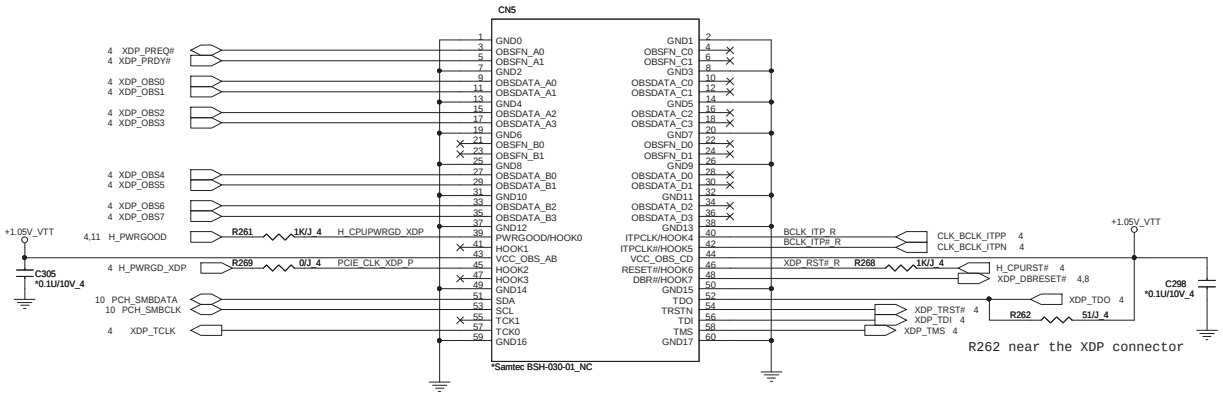
MINI CARD (WLAN)



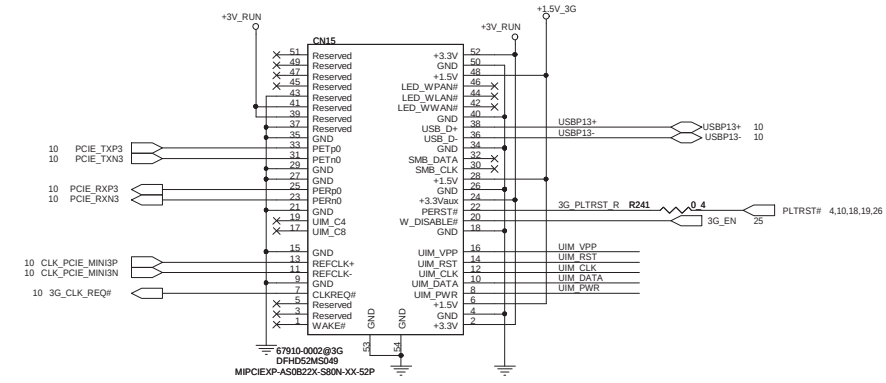
XDP

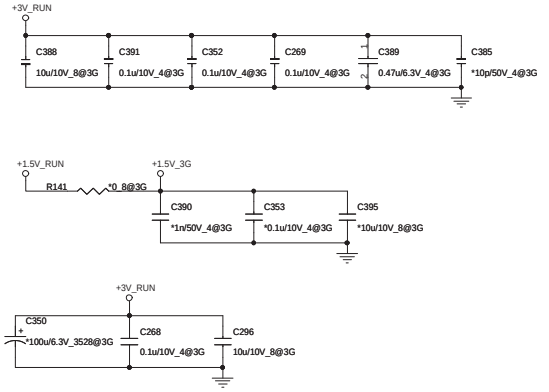


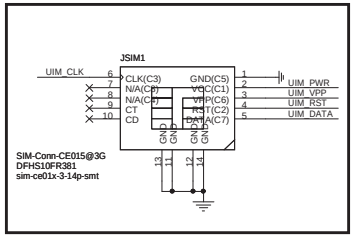
R262 near the XDP connector

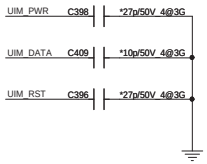
It is for debug. requesst vendeer provide 200 pcs sample.

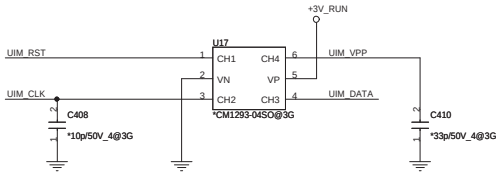
Mini Card2-3G(MNC)

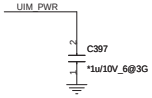












Quanta Computer Inc.		
PROJECT : FH2		
Size	Document Number: MINI CARD(WLAN/3G)/XDP	Rev: 1A
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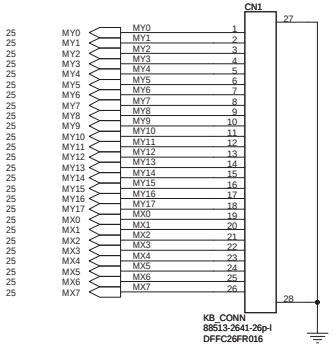
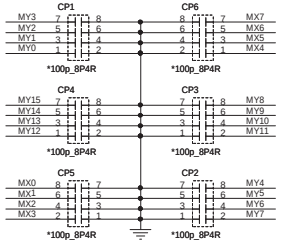
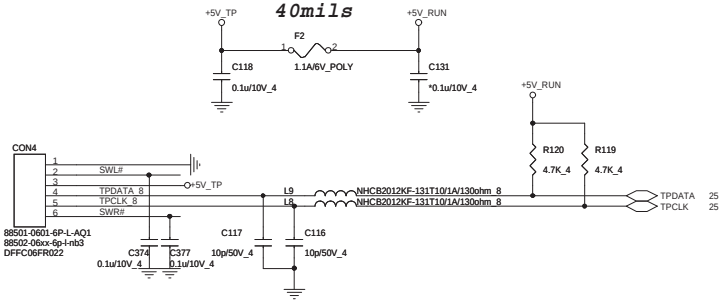
Keyboard(KBC)

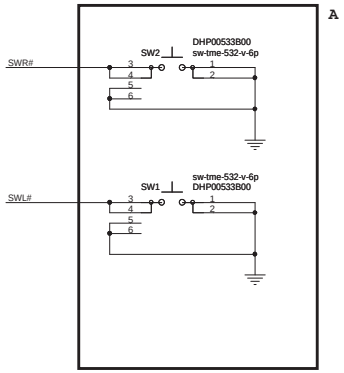


For EMI Reserve Caps for debug

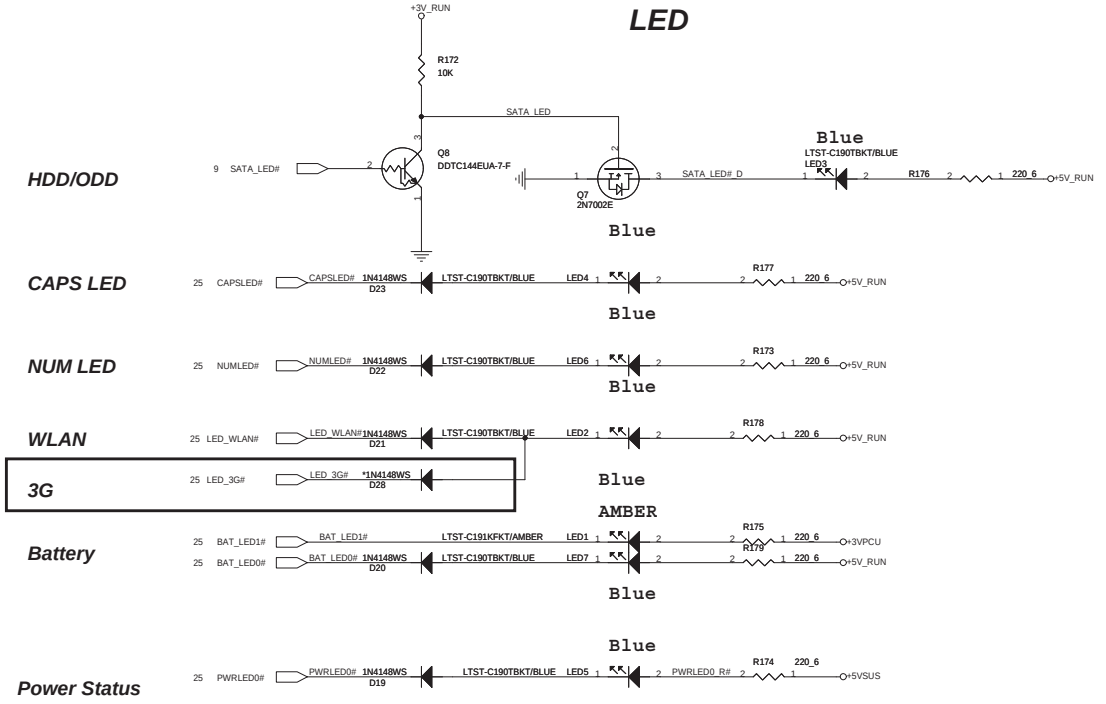


Touch Pad





LED



Quanta Computer Inc.	
PROJECT : FH2	
Size	Document Number: KB/TOUCH PAD/LED — Rev: 1A
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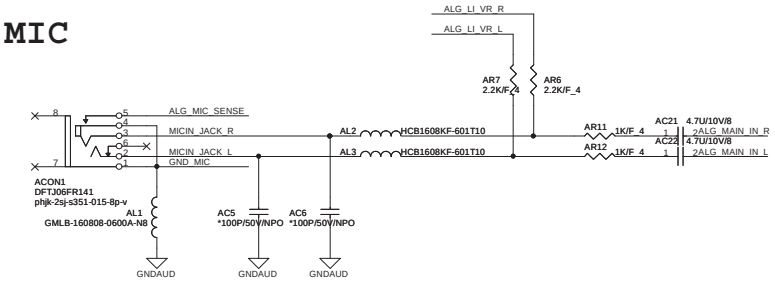
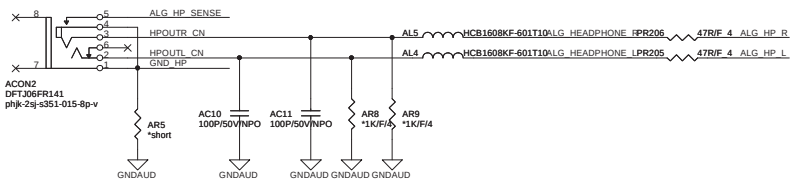
Codec ALC269

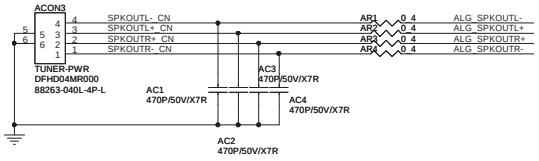
MIC



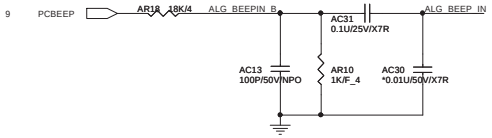
HP



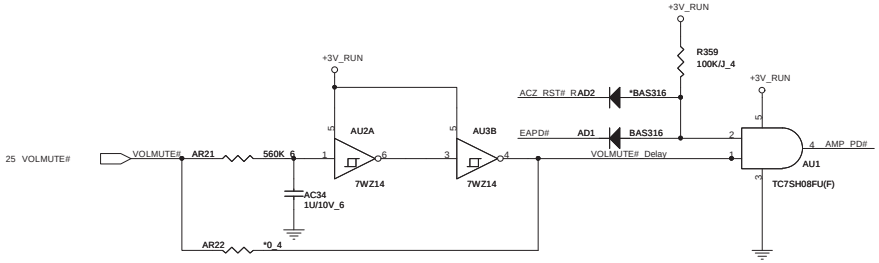
SPKR



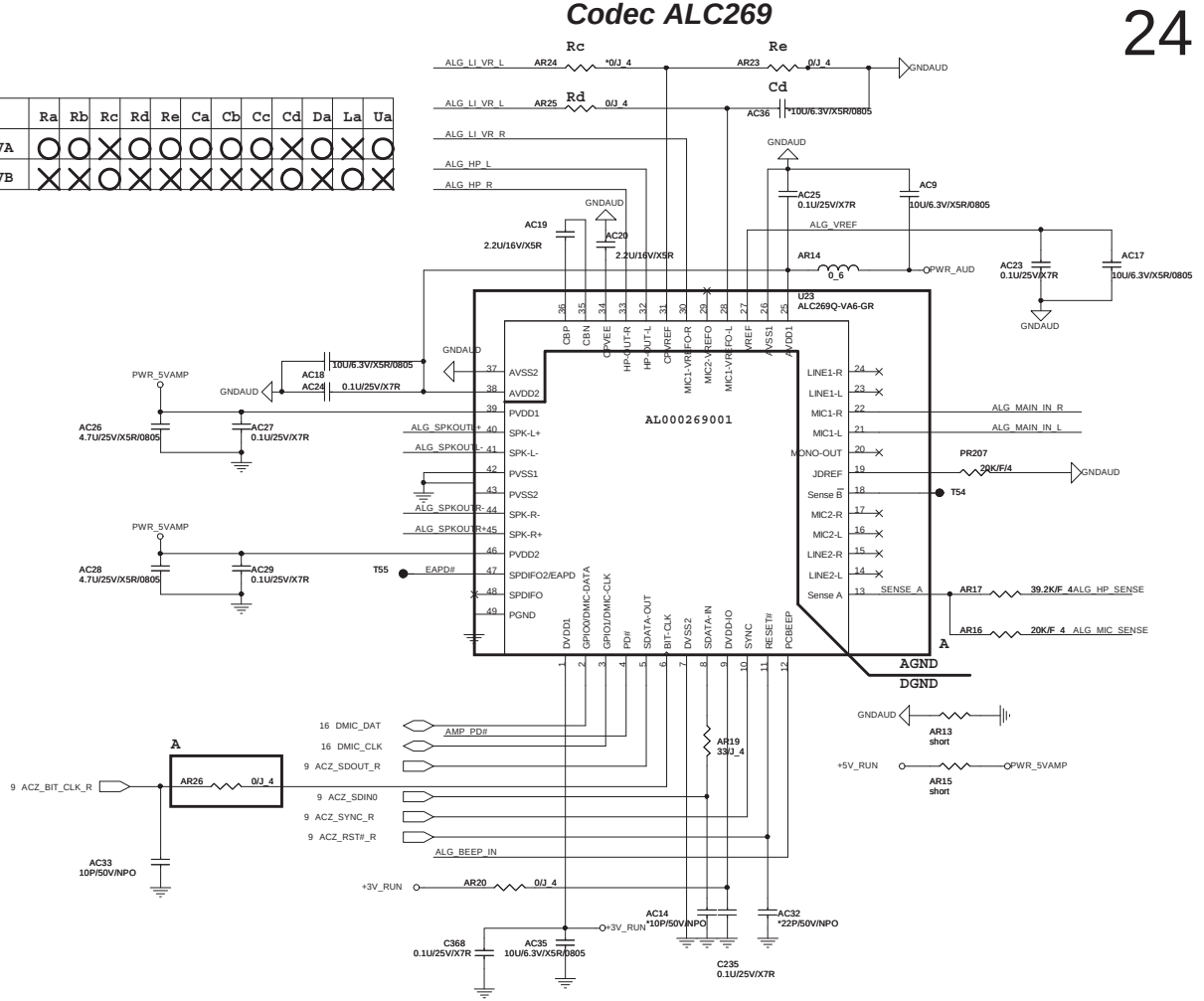
BEEP

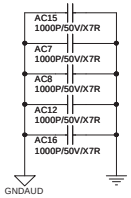


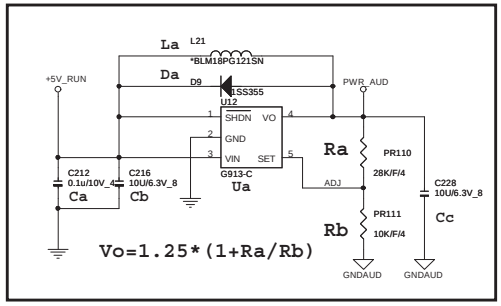
VOLMUTE



U23	Ra	Rb	Rc	Rd	Re	Ca	Cb	Cc	Cd	Da	La	Ua
ALC269Q-VA	O	O	X	O	O	O	O	O	X	O	X	O
ALC269Q-VB	X	X	O	X	X	X	X	X	O	X	O	X







Quanta Computer Inc.

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	CODEC (ALC269)	1A

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EC(KBC)

IT8502

Layout Note:
Place all capacitors close to IT8502.

Layout Note:
net "3VPCU" and "RTC_VCC" minimum trace width 12mils.

Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.

Layout Note:
32.768kHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.

PCB REV	MODEL_ID0	MODEL_ID1
C	LOW	LOW
D	HIGH	LOW
E	LOW	HIGH
F	HIGH	HIGH

BIOS Write Protect

2MB

Near ROOM DOOR

Quanta Computer Inc.
PROJECT : FH2

Size	Document Number	Rev
	EC_ITE8502	1A

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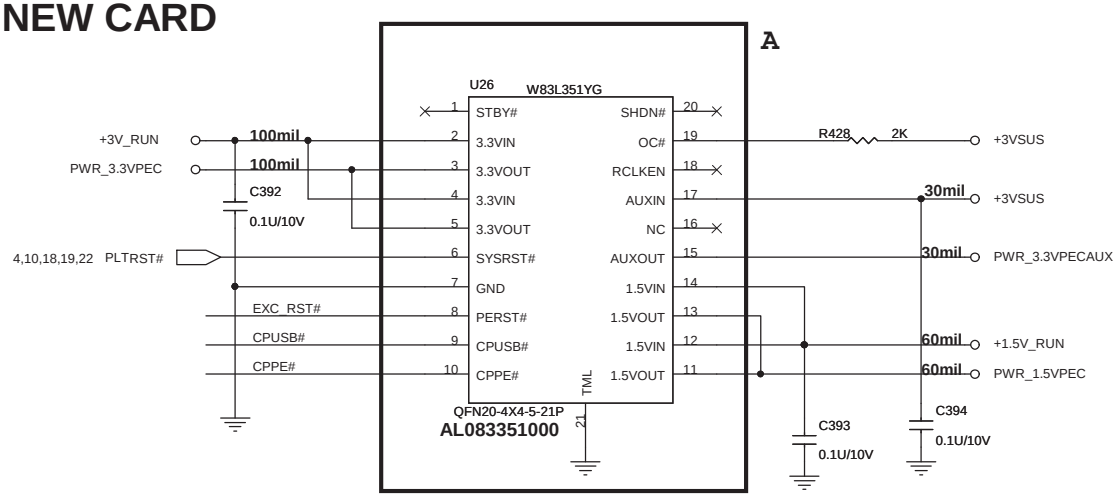
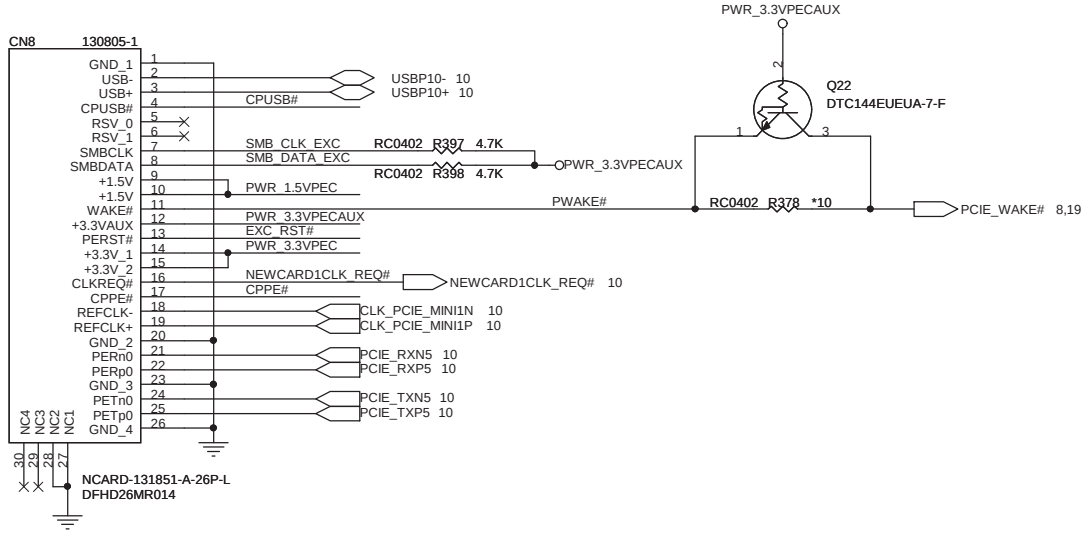
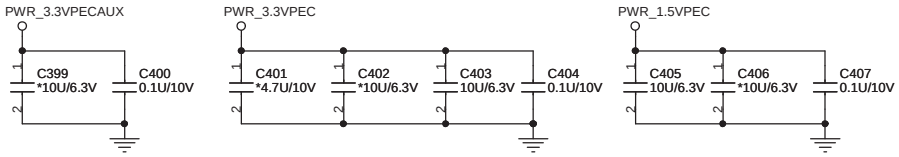
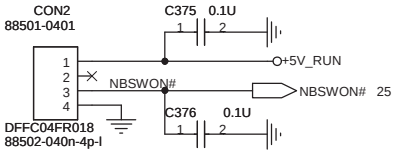
NEW CARD



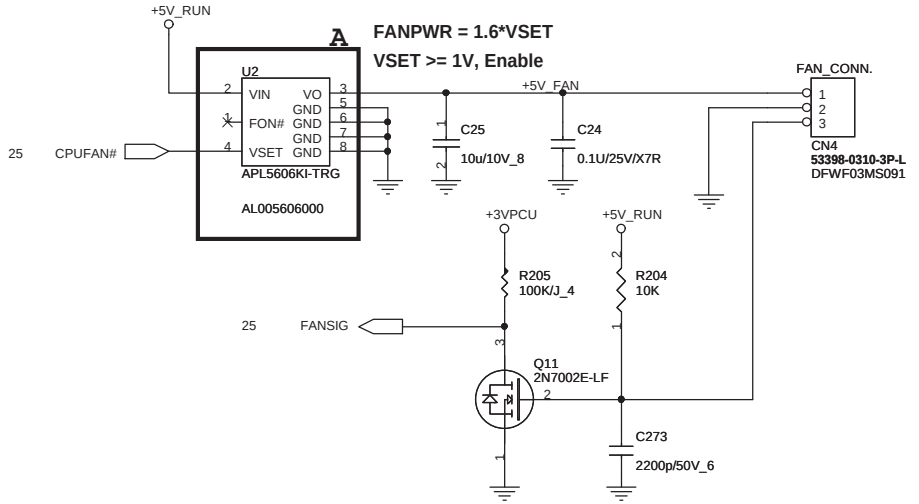




SW BOARD CON



CPU FAN CTRL



Quanta Computer Inc.

PROJECT : FH2

Size	Document Number	Rev
	FAN/SW/NEWCARD	1A

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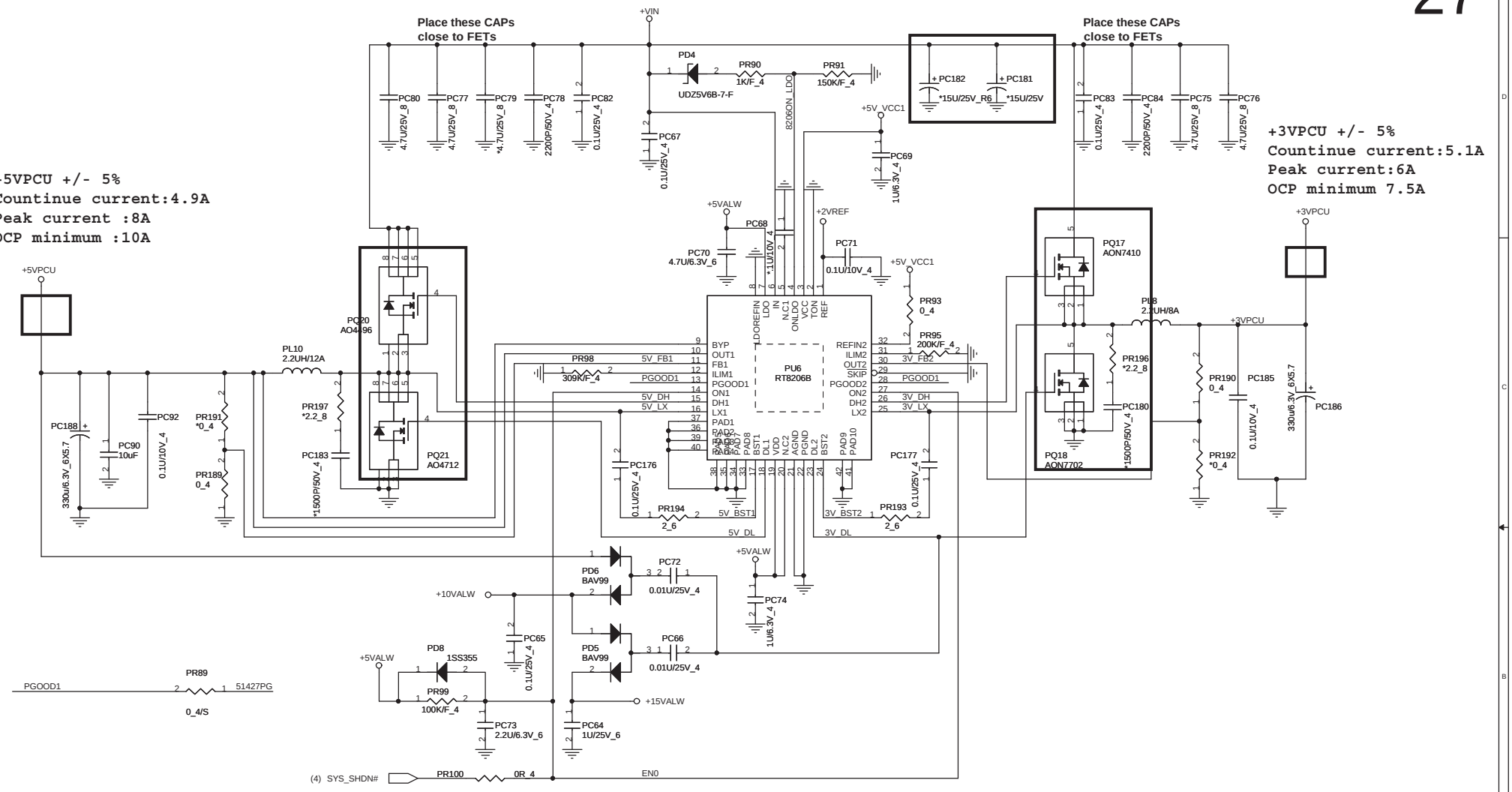
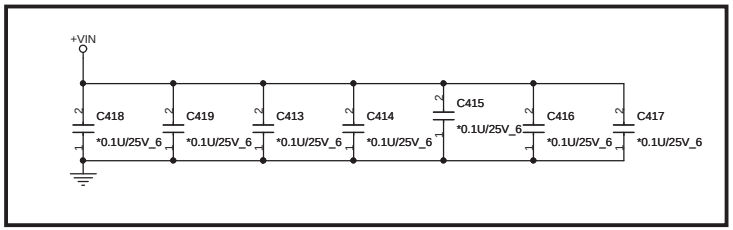
DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

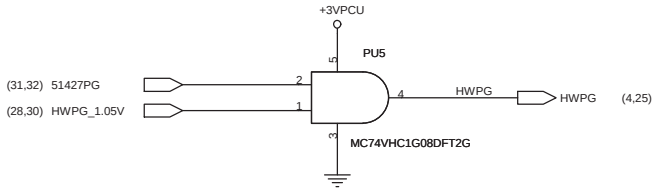
+5VPCU +/- 5%
Countinue current:4.9A
Peak current :8A
OCP minimum :10A

+3VPCU +/- 5%
Countinue current:5.1A
Peak current:6A
OCP minimum 7.5A



EMI





Quanta Computer Inc.
PROJECT : FH1

Size	Document Number	Rev
	+5V/+3V (RT8206B)	1A
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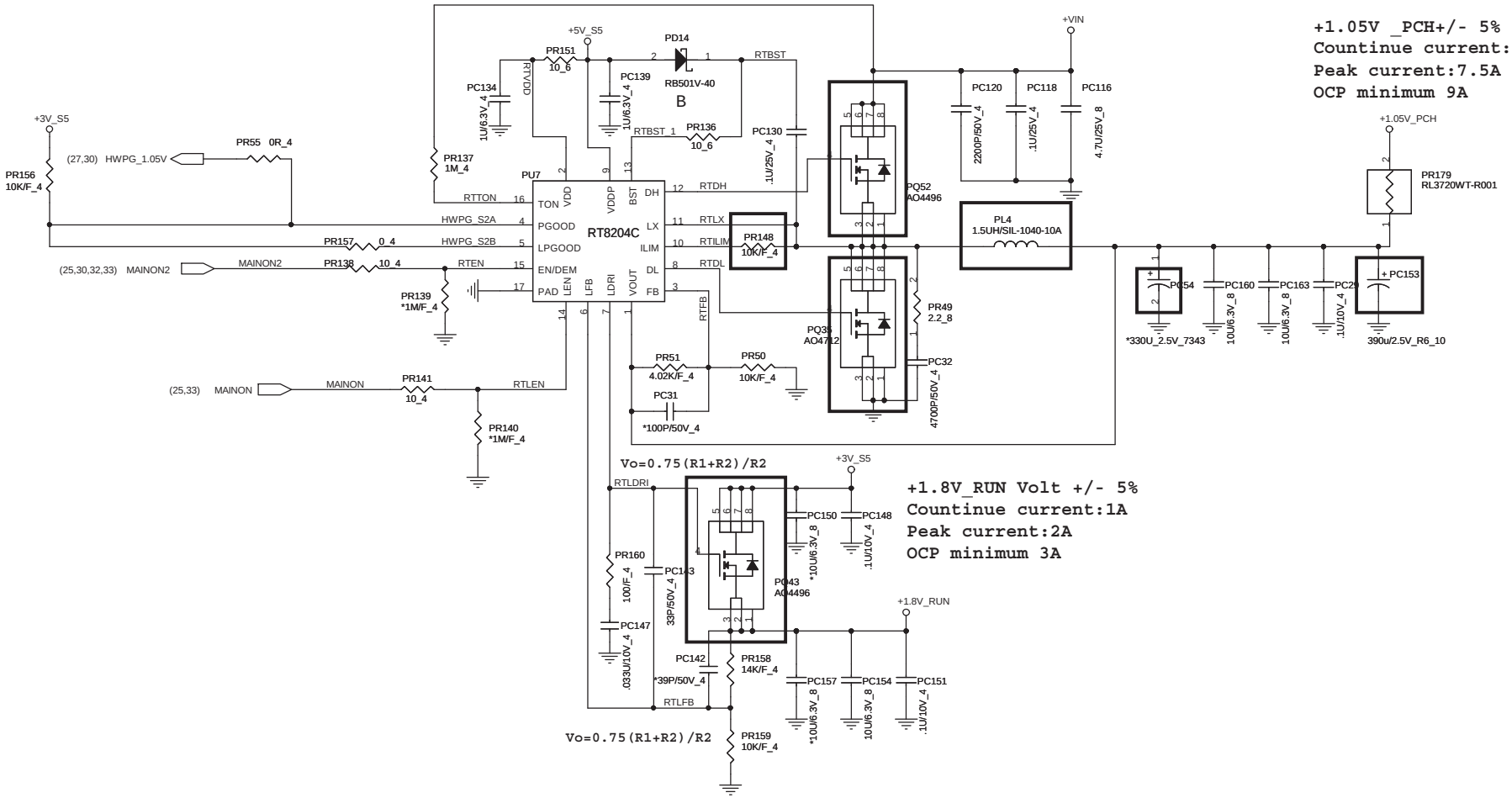
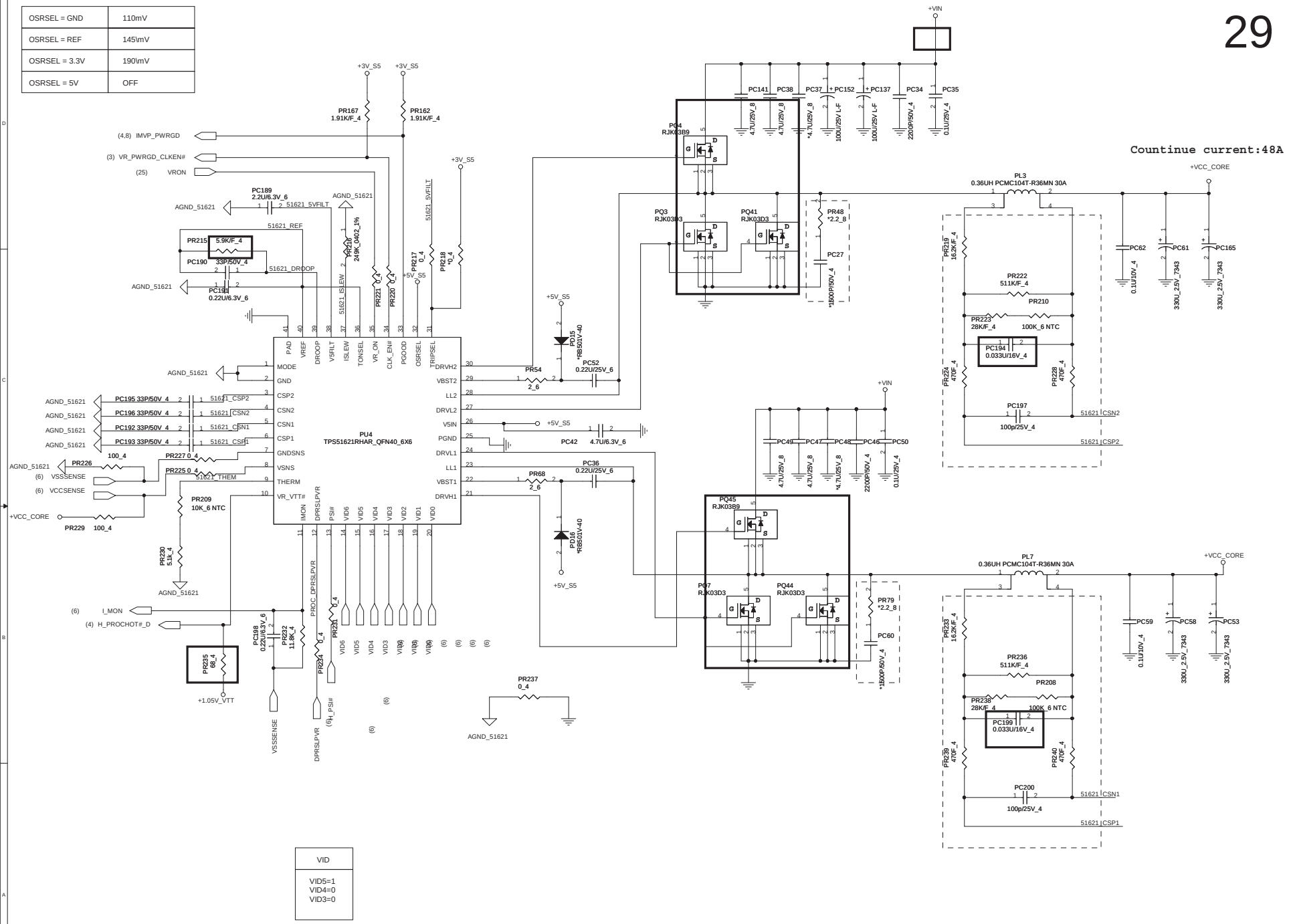


Quanta Computer Inc.		
PROJECT : FH1		
Size	Document Number: +1.05V/+1.8V (RT8204C)	Rev: 1A
Date: Monday, December 21, 2009	Sheet 28 of 39	

OSRSEL = GND	110mV
OSRSEL = REF	145\mV
OSRSEL = 3.3V	190\mV
OSRSEL = 5V	OFF

Countinue current:48A



Quanta Computer Inc.			
PROJECT : FH1			
Size	Document Number		Rev
	CPU Core (TPS51621)		1A
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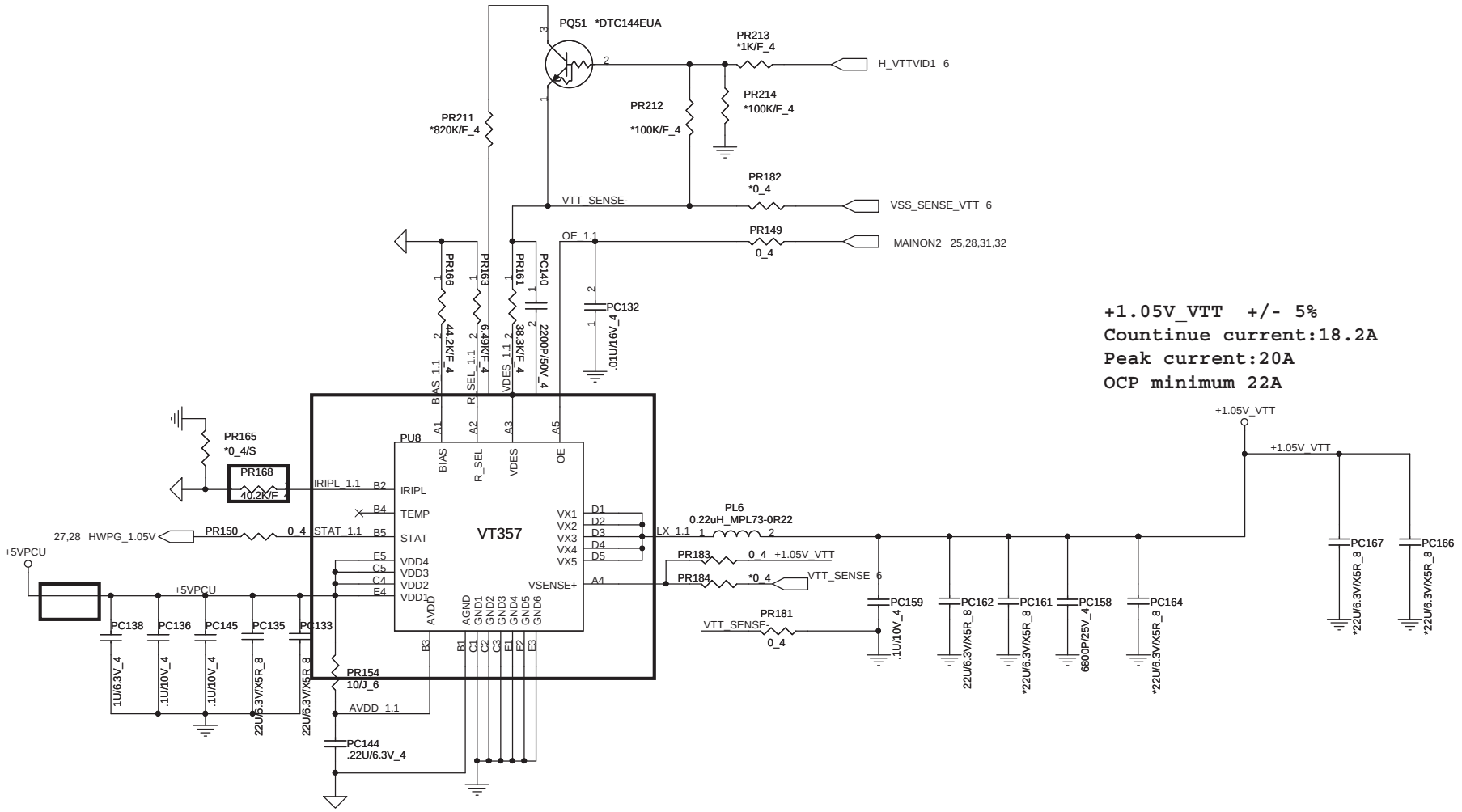
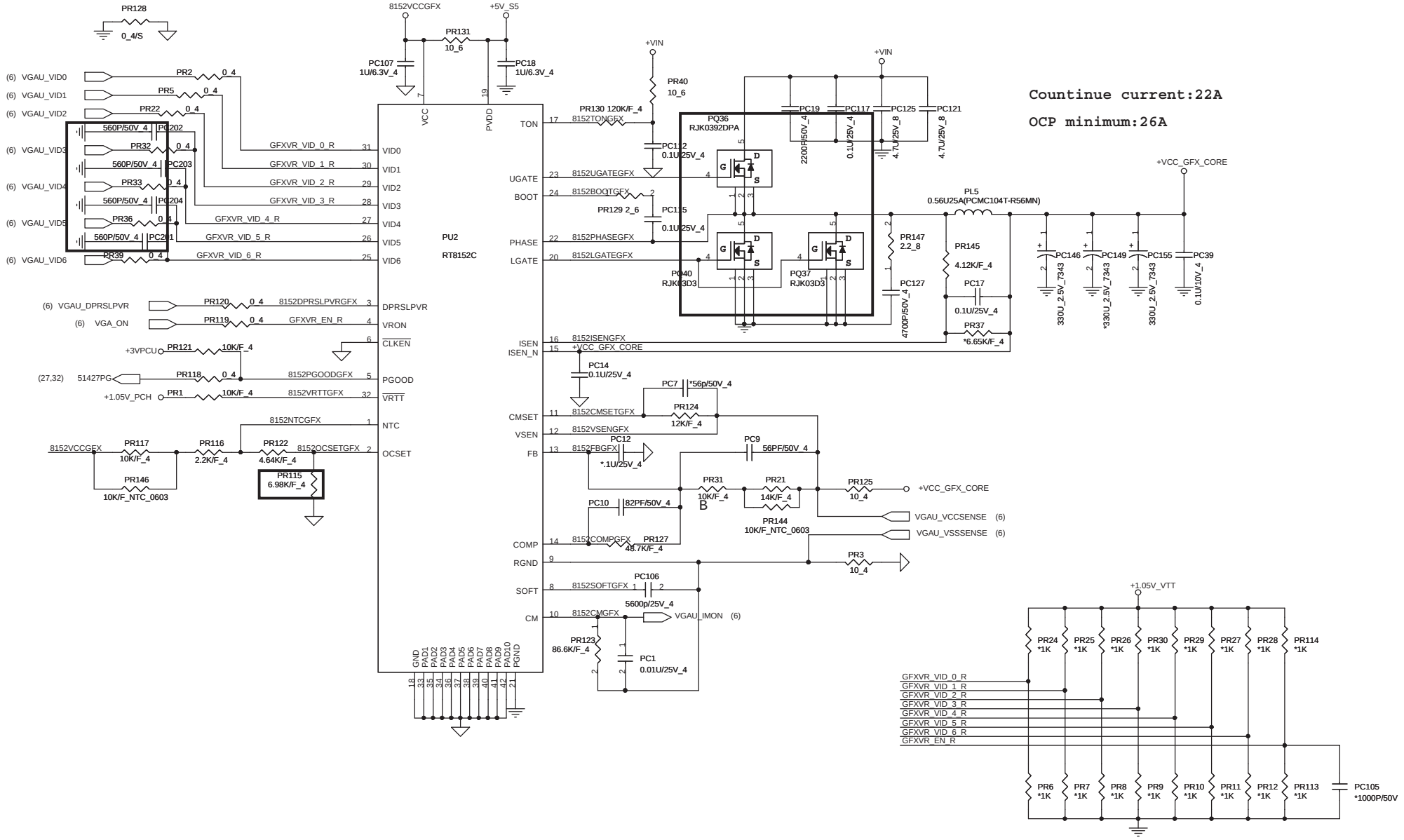


+1.05V_VTT +/- 5%
Countinue current:18.2A
Peak current:20A
OCP minimum 22A

Quanta Computer Inc.		
PROJECT : FH1A		
Size	Document Number	Rev
	+1.05V_VTT (VT358)	1A
Date: Monday, December 21, 2009	Sheet 30 of 45	



Quanta Computer Inc.			
PROJECT : FH1			
Size	Document Number		Rev
	UMA GPU CORE (RT8152C)		1A
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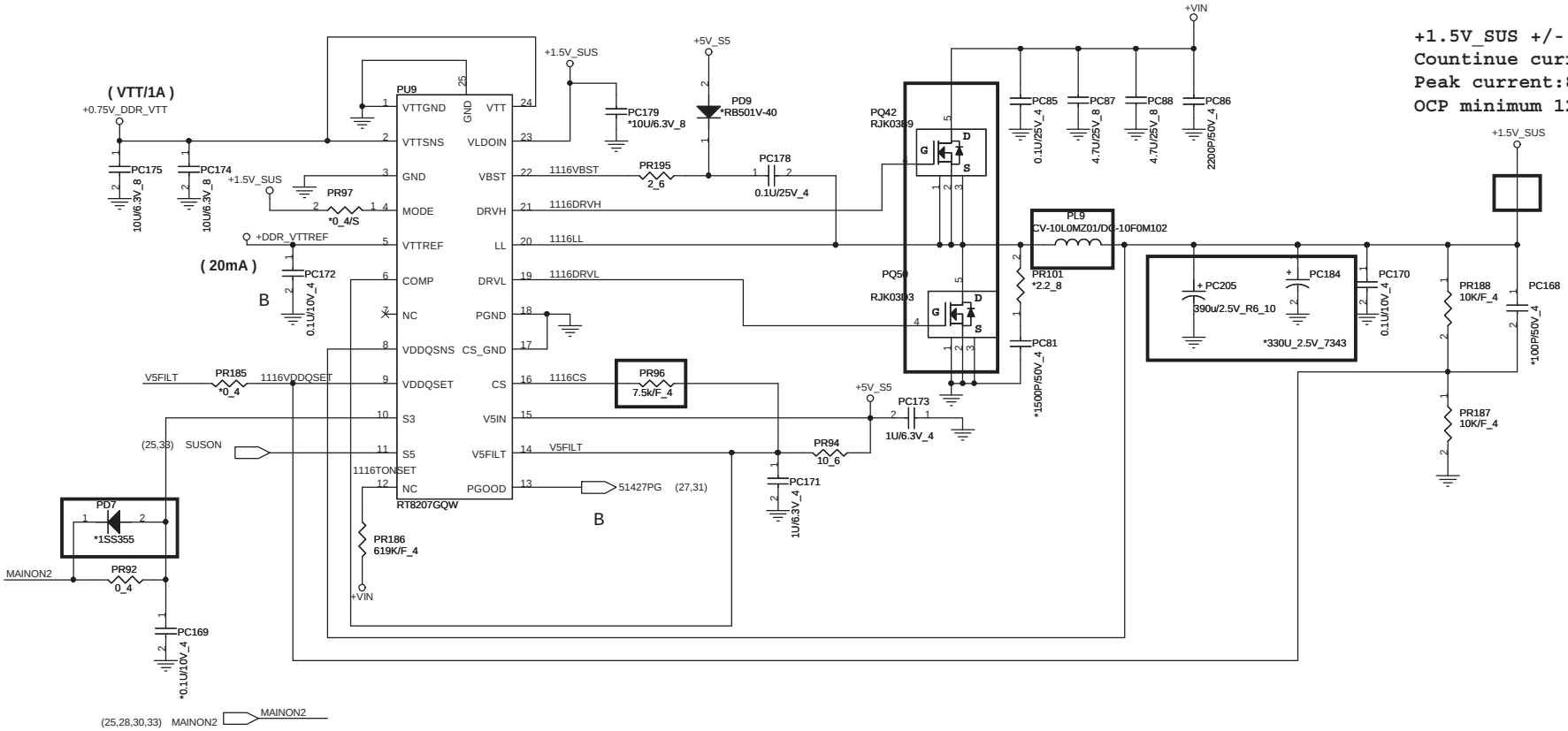
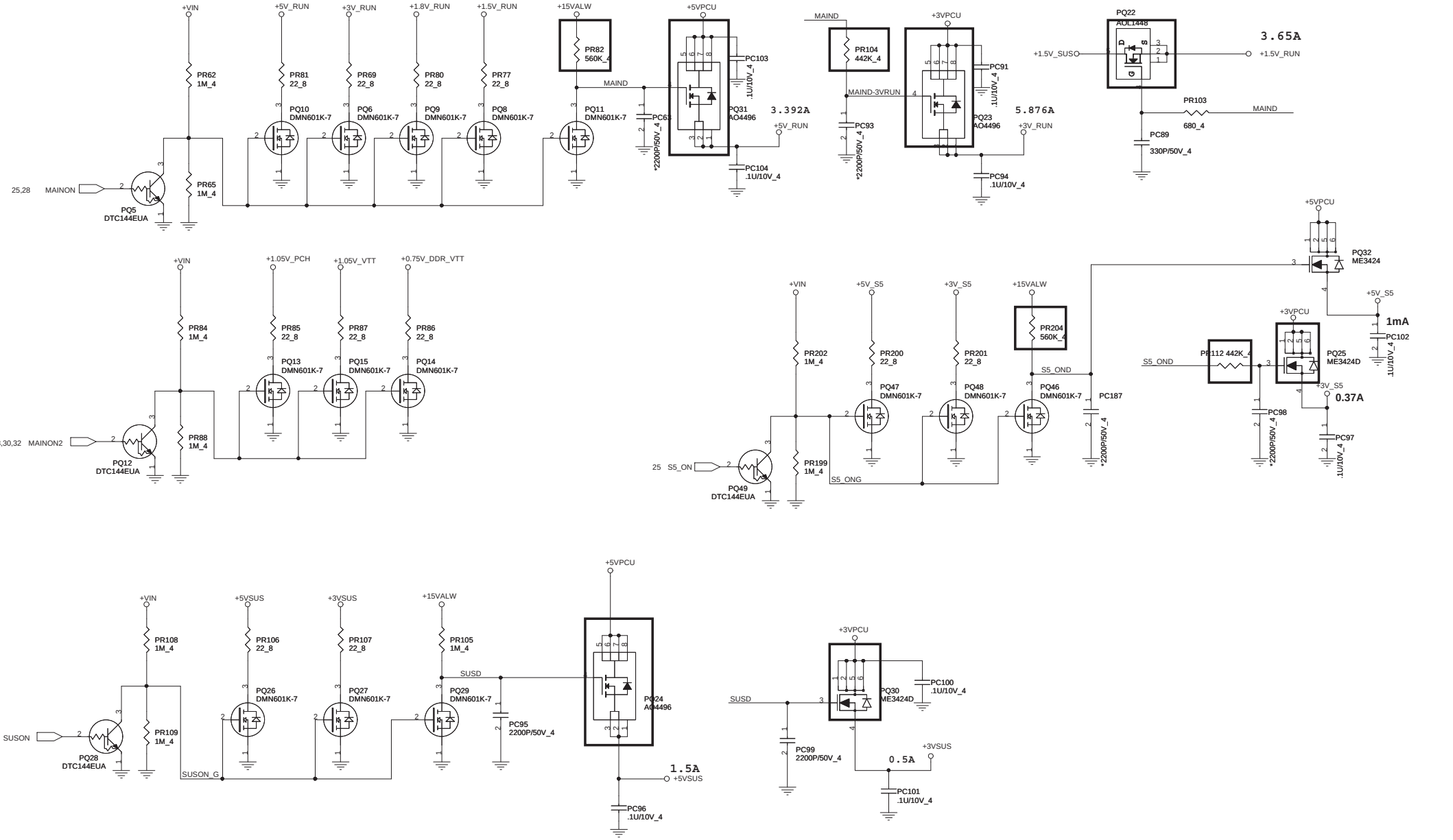


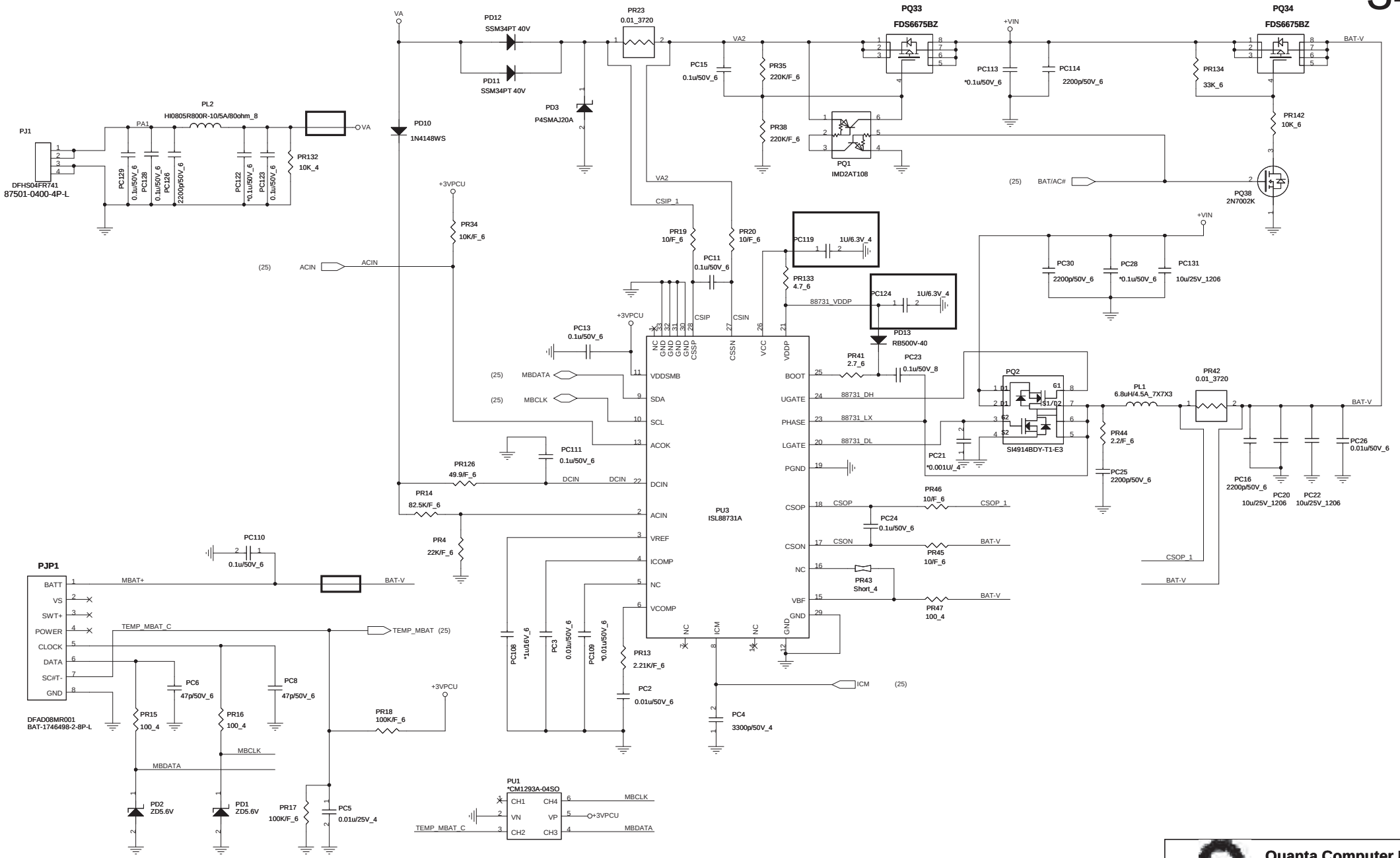
Quanta Computer Inc.		
PROJECT : FH1		
Size	Document Number: DDR3 (RT8207)	Rev: 1A
Date: Monday, December 21, 2009	Sheet 32 of 39	



Quanta Computer Inc.

PROJECT : FH2

Size	Document Number	Rev
	DISCHARGE/3VS5/5VS5/LAN	1A
Date: Monday, December 21, 2009	Sheet 33 of 38	



Quanta Computer Inc.

PROJECT : FH1

Size	Document Number	Rev
	CHARGER (ISL88731)	1A
Date: Monday, December 21, 2009	Sheet 34 of 39	