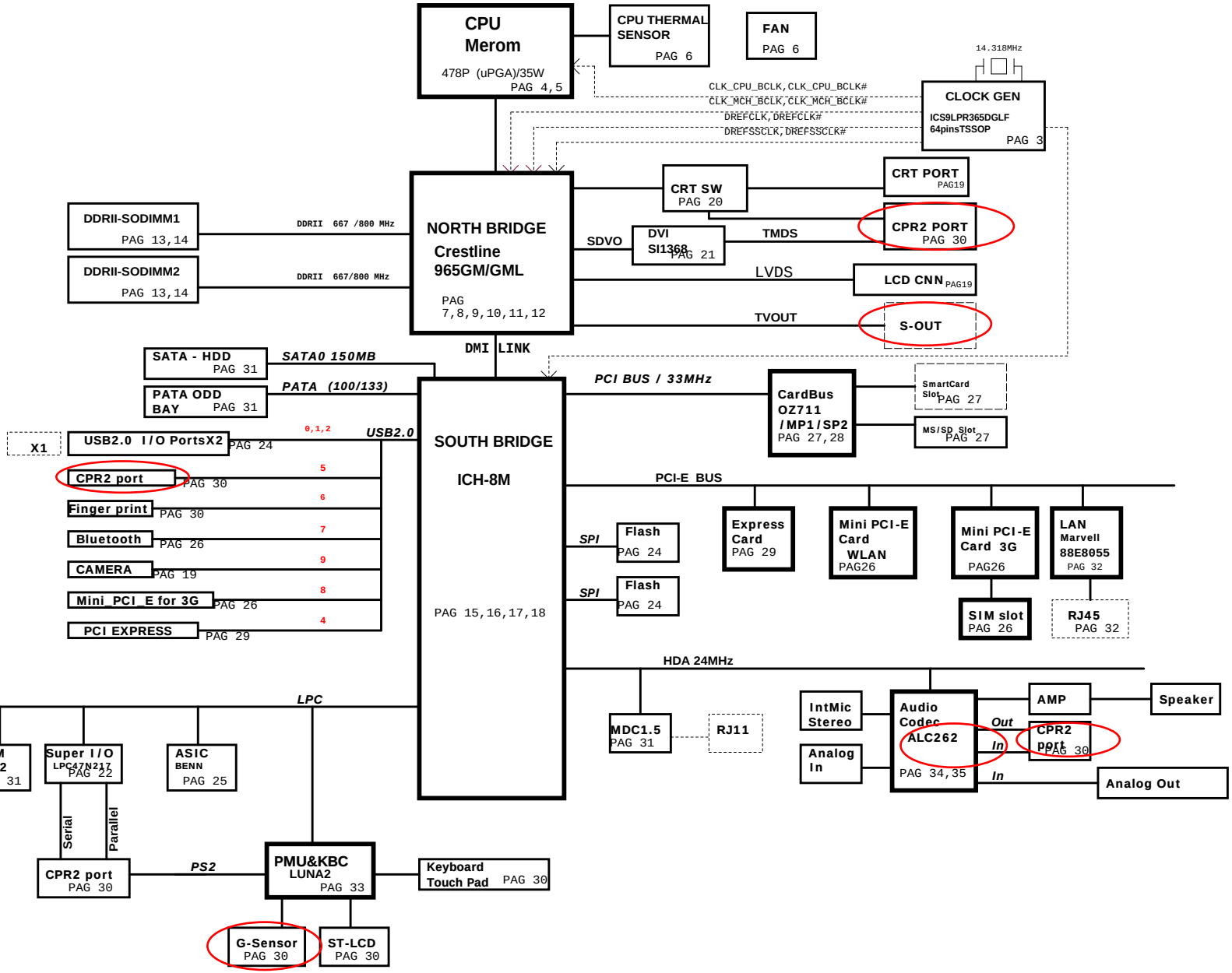
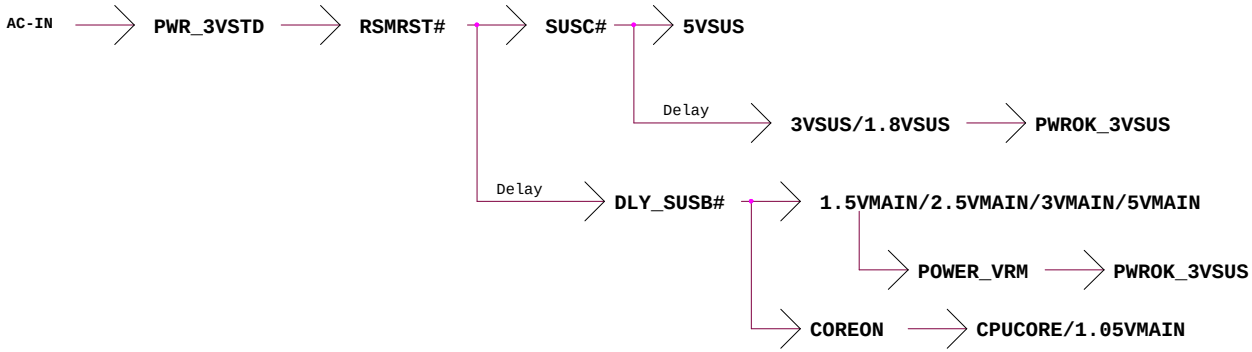
FJ1 BLOCK DIAGRAM



Title	FJ1 BLOCK DIAGRAM	
Size: Custom	Document Number: FJ1 MAIN BOARD	Rev: 1A
Date: Friday, June 22, 2007	Sheet 1 of 44	

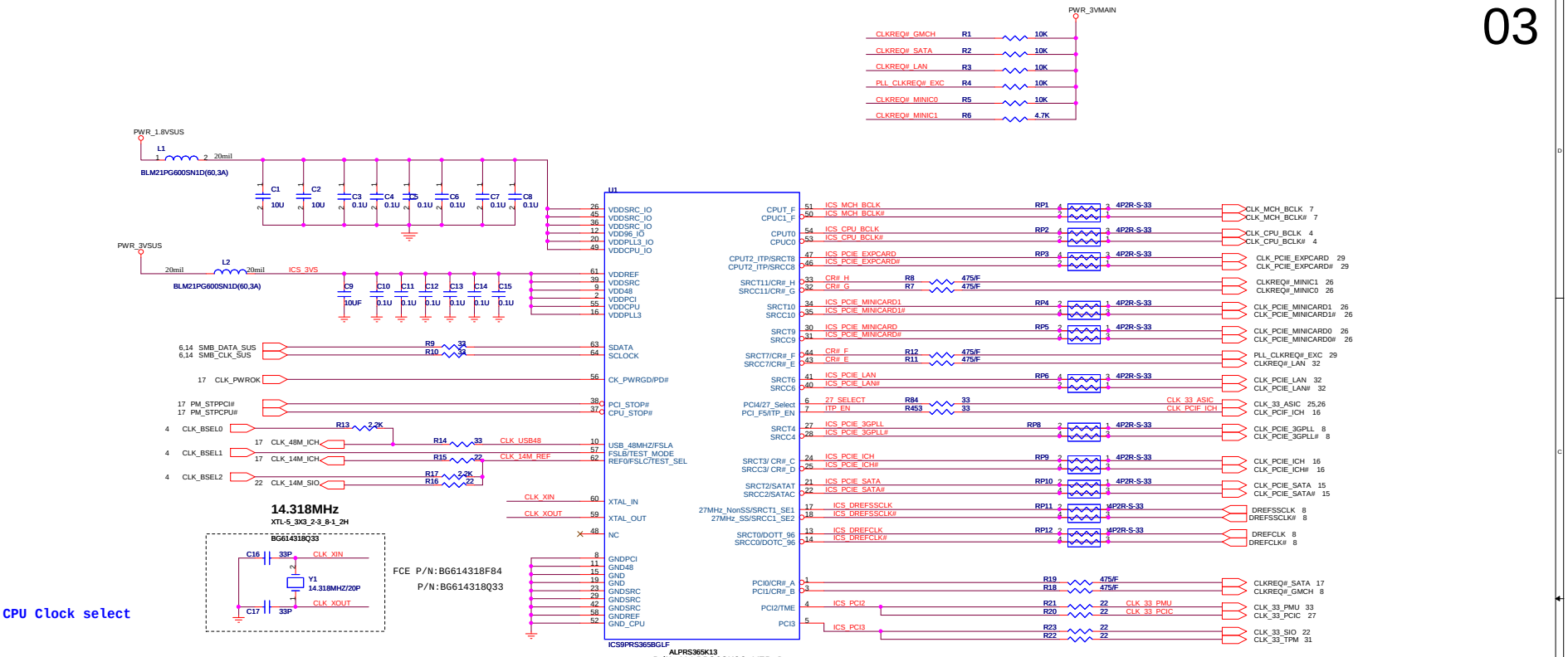
PAGE LIST

POWER_Control_Tree



QUANTA COMPUTER

Title: SCHEMATIC PAGE LIST		
Size: Custom	Document Number: FJ1 MAIN BOARD	Rev: 1A
Date: Monday, June 25, 2007	Sheet 2 of 44	



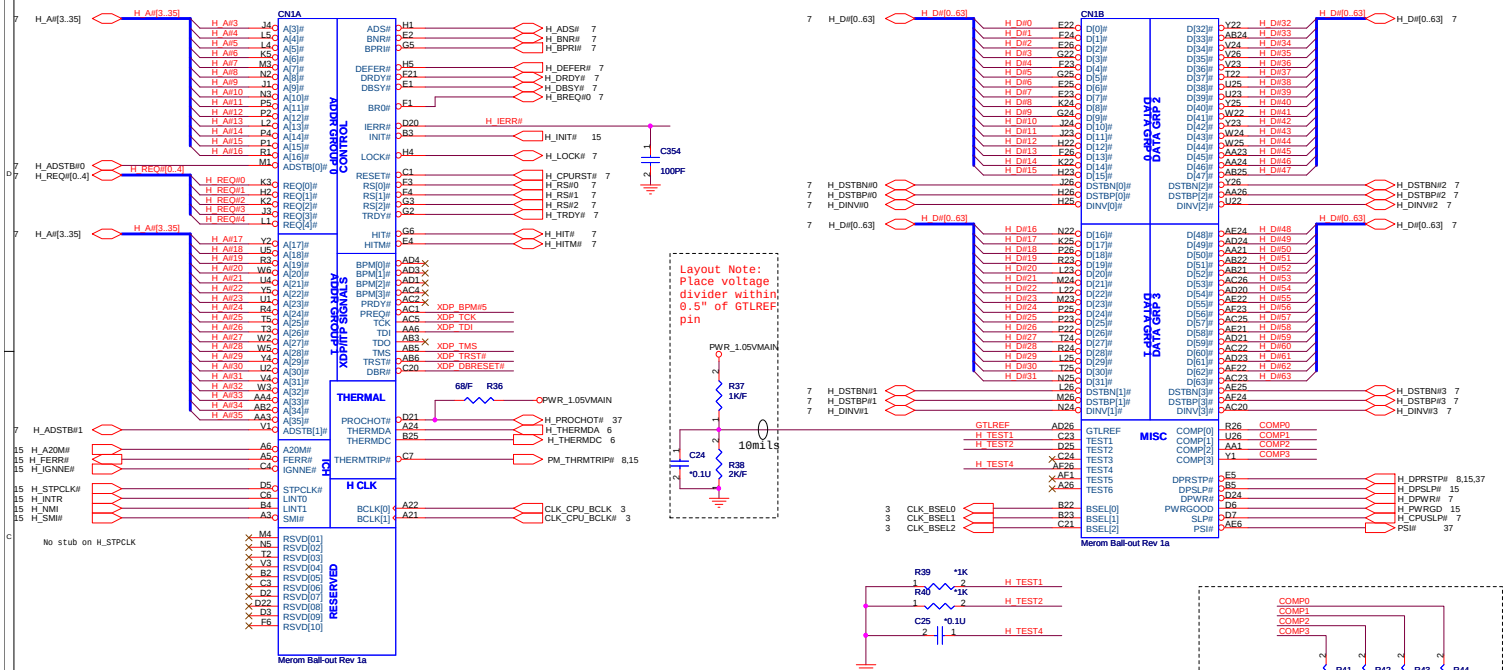
FSC BSEL2	FSB BSEL1	FSA BSEL0	CPU	SRC	PCI	REF	USB	DOT	Spread %
0	0	0	266.66	100	33.33	14.318	48	96	0.5 Down
0	0	1	133.33	100	33.33	14.318	48	96	0.5 Down
* 0	1	0	200.00	100	33.33	14.318	48	96	0.5 Down
0	1	1	**166.66**	100	33.33	14.318	48	96	0.5 Down
1	0	0	333.33	100	33.33	14.318	48	96	0.5 Down
1	0	1	100.00	100	33.33	14.318	48	96	0.5 Down
1	1	0	400.00	100	33.33	14.318	48	96	0.5 Down
1	1	1	200.00	100	33.33	14.318	48	96	0.5 Down

QUANTA COMPUTER

Title: CLOCK G_ICS365

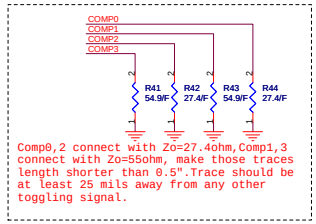
Size: Custom | Document Number: FJ1 MAIN BOARD | Rev: 1A

Date: Monday, June 25, 2007 | Sheet 3 of 44



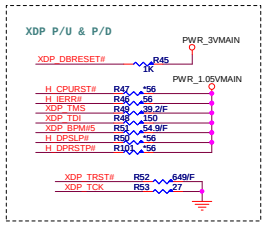
Layout Note: Place voltage divider within 0.5" of GTLREF pin

Place C close to the CPU_TEST4 pin. Make sure CPU_TEST4 routing is reference to GND and away from other noisy signal.



Comp0,2 connect with Zo=27.4ohm,Comp1,3 connect with Zo=55ohm, make those traces length shorter than 0.5".Trace should be at least 25 mils away from any other toggling signal.

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0



ITP disable guidelines

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the ITP
TMS	39 ohm +/- 1%	VTT	Within 2.0" of the ITP
TRST#	500-680ohm +/- 5%	GND	Within 2.0" of the ITP
TCK	27 ohm +/- 1%	GND	Within 2.0" of the ITP
TDO	150 ohm +/- 5%	VTT	Within 2.0" of the ITP

Note: Populate R5, R8, C372 & R430 when ITP connector is populated.

QUANTA COMPUTER

Title: Merom Processor (HOST BUS)

Size: Custom | Document Number: FJ1 MAIN BOARD | Rev: 1A

Date: Monday, June 25, 2007 | Sheet 4 of 44

PWR_CPUCORE

C26 10U C41 10U C34 10U C27 10U C28 10U

C29 10U C42 10U C30 10U C31 10U C32 10U

8 inside cavity, north side, secondary layer.

C43 10U C45 10U

DEL C33,C35,C37,C39,C40,C44,C46,C48,C49,C58

C38 10U

8 inside cavity, south side, secondary layer.

C47 10U C50 10U C51 10U C52 10U

C55 10U C56 10U C57 10U C59 10U C60 10U

8 inside cavity, north side, primary layer. 8 inside cavity, south side, primary layer.

PWR_1.05VMAIN

C61 0.1U C62 0.1U C63 0.1U C64 0.1U C65 0.1U C66 0.1U

Layout out:
Place these inside socket cavity on North side secondary.

PWR_CPUCORE 6,37
PWR_1.5VMAIN 11,15,18,26,29,38,41
PWR_1.05VMAIN 4,7,10,11,15,18,41,44

CN1C

A7	VCC[001]	VCC[068]	AB20		
A9	VCC[002]	VCC[069]	AB7		
A10	VCC[003]	VCC[070]	AC7		
A12	VCC[004]	VCC[071]	AC9		
A13	VCC[005]	VCC[072]	AC12		
A15	VCC[006]	VCC[073]	AC13		
A17	VCC[007]	VCC[074]	AC15		
A18	VCC[008]	VCC[075]	AC17		
A20	VCC[009]	VCC[076]	AC18		
B7	VCC[010]	VCC[077]	AD7		
B9	VCC[011]	VCC[078]	AD9		
B10	VCC[012]	VCC[079]	AD10		
B12	VCC[013]	VCC[080]	AD12		
B14	VCC[014]	VCC[081]	AD14		
B15	VCC[015]	VCC[082]	AD15		
B17	VCC[016]	VCC[083]	AD17		
B18	VCC[017]	VCC[084]	AD18		
B20	VCC[018]	VCC[085]	AE9		
C9	VCC[019]	VCC[086]	AE10		
C10	VCC[020]	VCC[087]	AE12		
C12	VCC[021]	VCC[088]	AE13		
C13	VCC[022]	VCC[089]	AE15		
C15	VCC[023]	VCC[090]	AE17		
C17	VCC[024]	VCC[091]	AE18		
C18	VCC[025]	VCC[092]	AE20		
D9	VCC[026]	VCC[093]	AF9		
D10	VCC[027]	VCC[094]	AF10		
D12	VCC[028]	VCC[095]	AF12		
D14	VCC[029]	VCC[096]	AF14		
D15	VCC[030]	VCC[097]	AF15		
D17	VCC[031]	VCC[098]	AF17		
D18	VCC[032]	VCC[099]	AF18		
E7	VCC[033]	VCC[100]	AF20		
E9	VCC[034]				
E10	VCC[035]	VCCP[01]	G21		
E12	VCC[036]	VCCP[02]	V6		
E13	VCC[037]	VCCP[03]	J6		
E15	VCC[038]	VCCP[04]	K6		
E17	VCC[039]	VCCP[05]	M6		
E18	VCC[040]	VCCP[06]	J21		
E20	VCC[041]	VCCP[07]	K21		
F7	VCC[042]	VCCP[08]	M21		
F9	VCC[043]	VCCP[09]	N21		
F10	VCC[044]	VCCP[10]	N6		
F12	VCC[045]	VCCP[11]	R21		
F14	VCC[046]	VCCP[12]	R6		
F15	VCC[047]	VCCP[13]	T21		
F17	VCC[048]	VCCP[14]	T6		
F18	VCC[049]	VCCP[15]	V21		
F20	VCC[050]	VCCP[16]	W21		
AA7	VCC[051]				
AA9	VCC[052]	VCCA[01]	B26		
AA10	VCC[053]	VCCA[02]	C26		
AA12	VCC[054]				
AA13	VCC[055]	VID[0]	AD6	CPU_VID0	37
AA15	VCC[056]	VID[1]	AF5	CPU_VID1	37
AA17	VCC[057]	VID[2]	AE5	CPU_VID2	37
AA18	VCC[058]	VID[3]	AF4	CPU_VID3	37
AA20	VCC[059]	VID[4]	AE3	CPU_VID4	37
AB9	VCC[060]	VID[5]	AF3	CPU_VID5	37
AC10	VCC[061]	VID[6]	AE2	CPU_VID6	37
AB10	VCC[062]				
AB12	VCC[063]				
AB14	VCC[064]	VCCSENSE	AF7	CPU_VCC_SENSE	37
AB15	VCC[065]				
AB17	VCC[066]				
AB18	VCC[067]	VSSSENSE	AE7	CPU_VSS_SENSE	37

Merom Ball-out Rev 1a

PWR_CPUCORE

ICCODE:
for Merom processors
recommended design
target is 44A

EC8

PWR_1.05VMAIN

Via:2.5A >100mils

C58 10U C135 10U C36 220U/2.5V

ICCP:
1before vccore stable
peak current is 4.5A
2.after vccore stable
continue current is
2.5A

ICCA 130mA

PWR_1.5VMAIN

C53 0.01U C54 10U

Layout Note:
Place C105 near PIN
B26.

PWR_CPUCORE

R54 100/F

CPU_VCC_SENSE
CPU_VSS_SENSE

R55 100/F

Route VCCSENSE and VSSSENSE
traces at 27.4ohms and
length matched to within 25
mil. Place PU and PD within
2 inch of CPU.

CN1D

A4	VSS[001]	VSS[082]	P6		
A8	VSS[002]	VSS[083]	P21		
A11	VSS[003]	VSS[084]	P24		
A14	VSS[004]	VSS[085]	R2		
A16	VSS[005]	VSS[086]	R5		
A19	VSS[006]	VSS[087]	R22		
A23	VSS[007]	VSS[088]	R25		
AF2	VSS[008]	VSS[089]	T1		
B6	VSS[009]	VSS[090]	T4		
B8	VSS[010]	VSS[091]	T23		
B11	VSS[011]	VSS[092]	T26		
B13	VSS[012]	VSS[093]	U3		
B16	VSS[013]	VSS[094]	U6		
B19	VSS[014]	VSS[095]	U21		
B21	VSS[015]	VSS[096]	U24		
B24	VSS[016]	VSS[097]	V2		
C5	VSS[017]	VSS[098]	V5		
C8	VSS[018]	VSS[099]	V22		
C11	VSS[019]	VSS[100]	V25		
C14	VSS[020]	VSS[101]	W1		
C16	VSS[021]	VSS[102]	W4		
C19	VSS[022]	VSS[103]	W23		
C2	VSS[023]	VSS[104]	W26		
C22	VSS[024]	VSS[105]	Y3		
C25	VSS[025]	VSS[106]	Y6		
D1	VSS[026]	VSS[107]	Y21		
D4	VSS[027]	VSS[108]	Y24		
D8	VSS[028]	VSS[109]	AA2		
D11	VSS[029]	VSS[110]	AA5		
D13	VSS[030]	VSS[111]	AA8		
D16	VSS[031]	VSS[112]	AA11		
D19	VSS[032]	VSS[113]	AA14		
D23	VSS[033]	VSS[114]	AA16		
D26	VSS[034]	VSS[115]	AA19		
E3	VSS[035]	VSS[116]	AA22		
E6	VSS[036]	VSS[117]	AA25		
E8	VSS[037]	VSS[118]	AB1		
E11	VSS[038]	VSS[119]	AB4		
E14	VSS[039]	VSS[120]	AB8		
E16	VSS[040]	VSS[121]	AB11		
E19	VSS[041]	VSS[122]	AB13		
E21	VSS[042]	VSS[123]	AB16		
E24	VSS[043]	VSS[124]	AB19		
F5	VSS[044]	VSS[125]	AB23		
F8	VSS[045]	VSS[126]	AB26		
F11	VSS[046]	VSS[127]	AC3		
F13	VSS[047]	VSS[128]	AC6		
F16	VSS[048]	VSS[129]	AC8		
F19	VSS[049]	VSS[130]	AC11		
F2	VSS[050]	VSS[131]	AC14		
F22	VSS[051]	VSS[132]	AC16		
F25	VSS[052]	VSS[133]	AC19		
G4	VSS[053]	VSS[134]	AC21		
G1	VSS[054]	VSS[135]	AC24		
G23	VSS[055]	VSS[136]	AD2		
G26	VSS[056]	VSS[137]	AD5		
H3	VSS[057]	VSS[138]	AD8		
H6	VSS[058]	VSS[139]	AD11		
H21	VSS[059]	VSS[140]	AD13		
H24	VSS[060]	VSS[141]	AD16		
J2	VSS[061]	VSS[142]	AD19		
J5	VSS[062]	VSS[143]	AD22		
J22	VSS[063]	VSS[144]	AD25		
J25	VSS[064]	VSS[145]	AE1		
K1	VSS[065]	VSS[146]	AE4		
K4	VSS[066]	VSS[147]	AE8		
K23	VSS[067]	VSS[148]	AE11		
K26	VSS[068]	VSS[149]	AE14		
L3	VSS[069]	VSS[150]	AE16		
L6	VSS[070]	VSS[151]	AE19		
L21	VSS[071]	VSS[152]	AE23		
L24	VSS[072]	VSS[153]	AE26		
M2	VSS[073]	VSS[154]	A2		
M5	VSS[074]	VSS[155]	AF6		
M22	VSS[075]	VSS[156]	AF8		
M25	VSS[076]	VSS[157]	AF11		
N1	VSS[077]	VSS[158]	AF13		
N4	VSS[078]	VSS[159]	AF16		
N23	VSS[079]	VSS[160]	AF19		
N26	VSS[080]	VSS[161]	AF21		
P3	VSS[081]	VSS[162]	A25		
		VSS[163]	AF25		

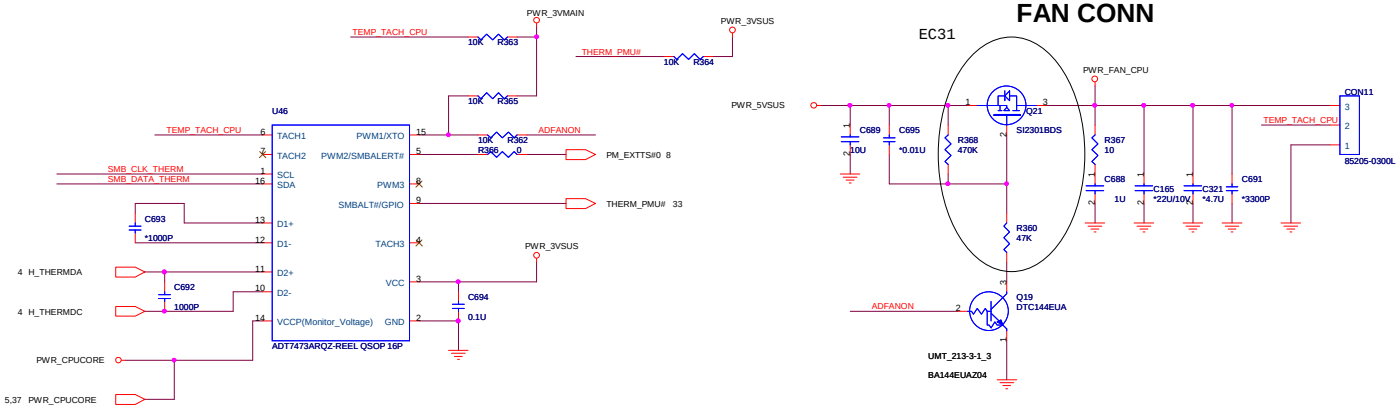
Merom Ball-out Rev 1a

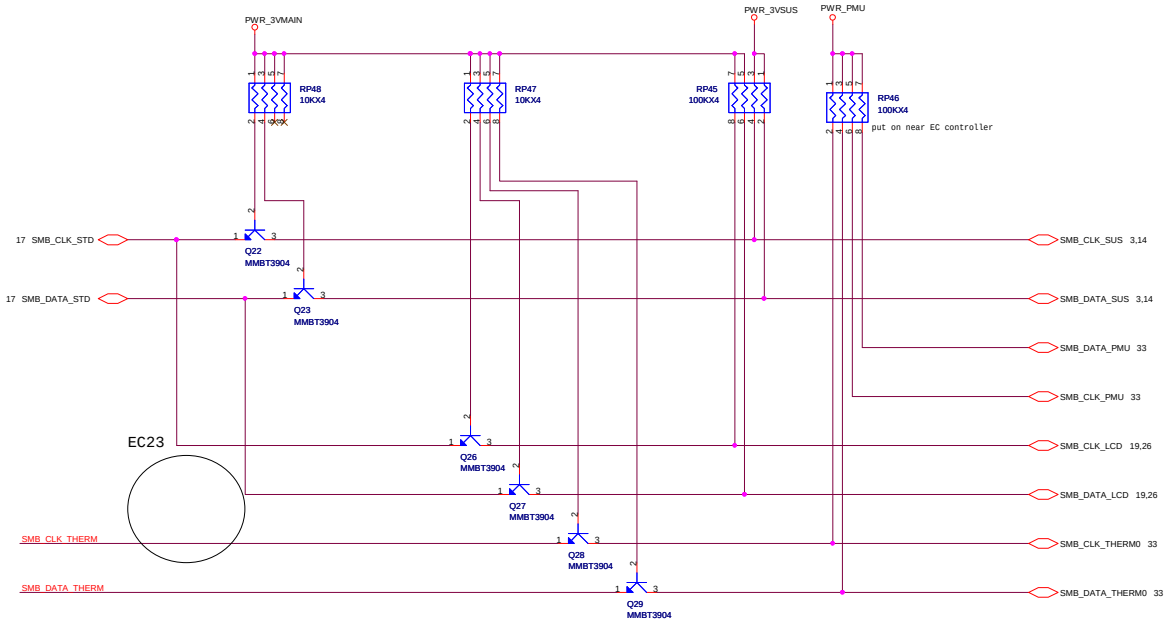
QUANTA COMPUTER

Title	Merom Processor (Power/NC)	
Size: Custom	Document Number: FJ1 MAIN BOARD	Rev: 1A
Date: Monday, June 25, 2007	Sheet 5 of 44	

Thermal Senser

06



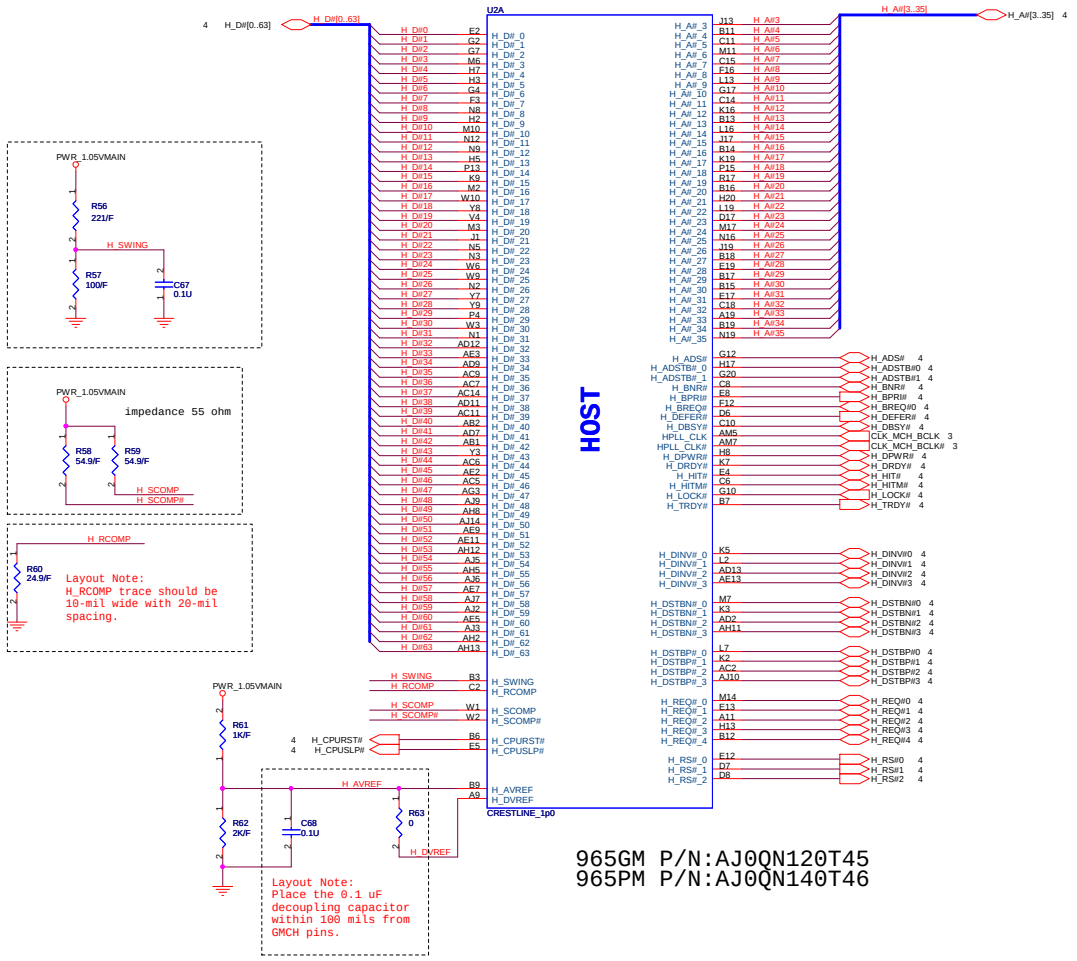


QUANTA COMPUTER

Title: Thermal Sensor and Fan

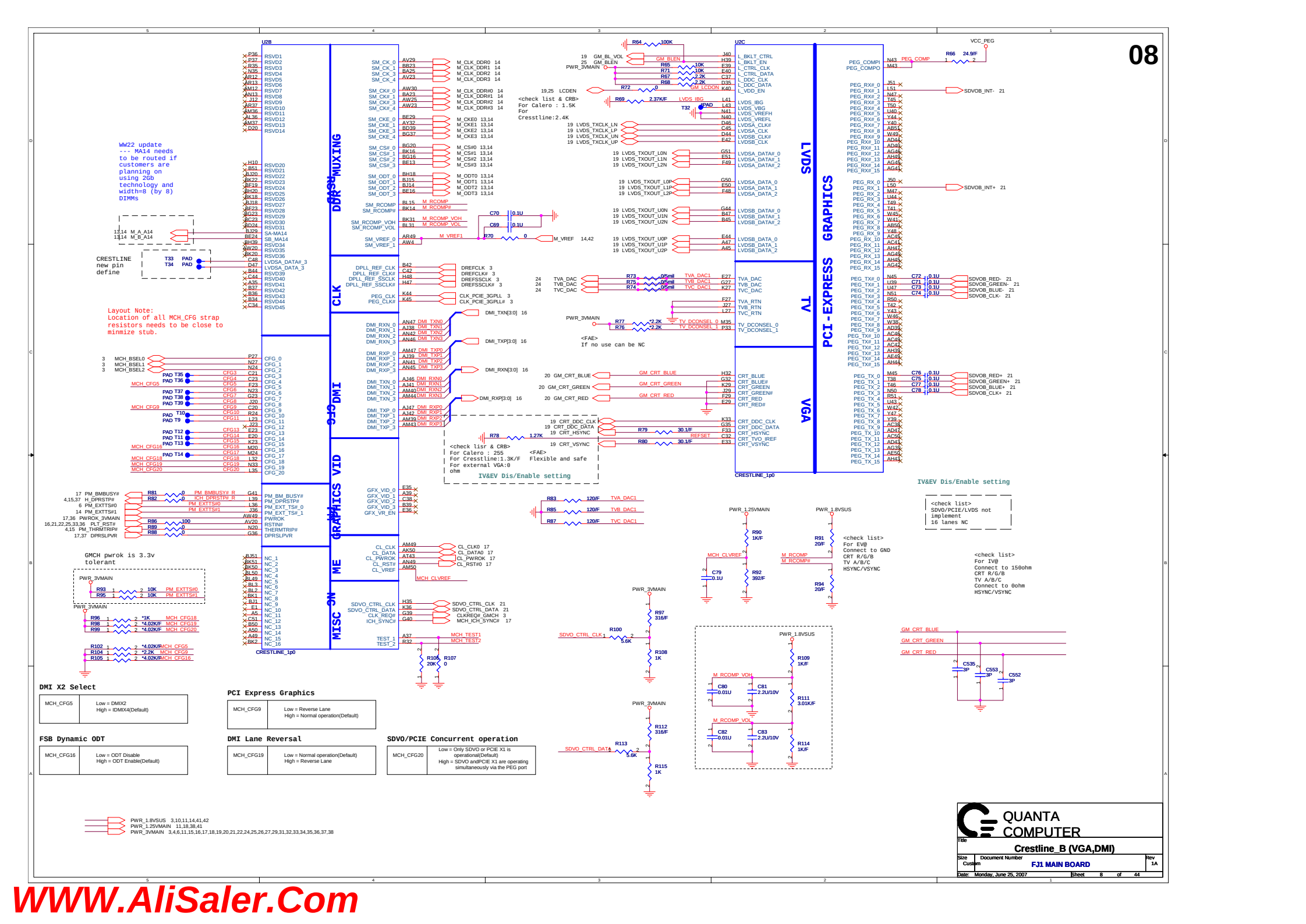
Size	Document Number	Rev
Custom	FJ1 MAIN BOARD	1A

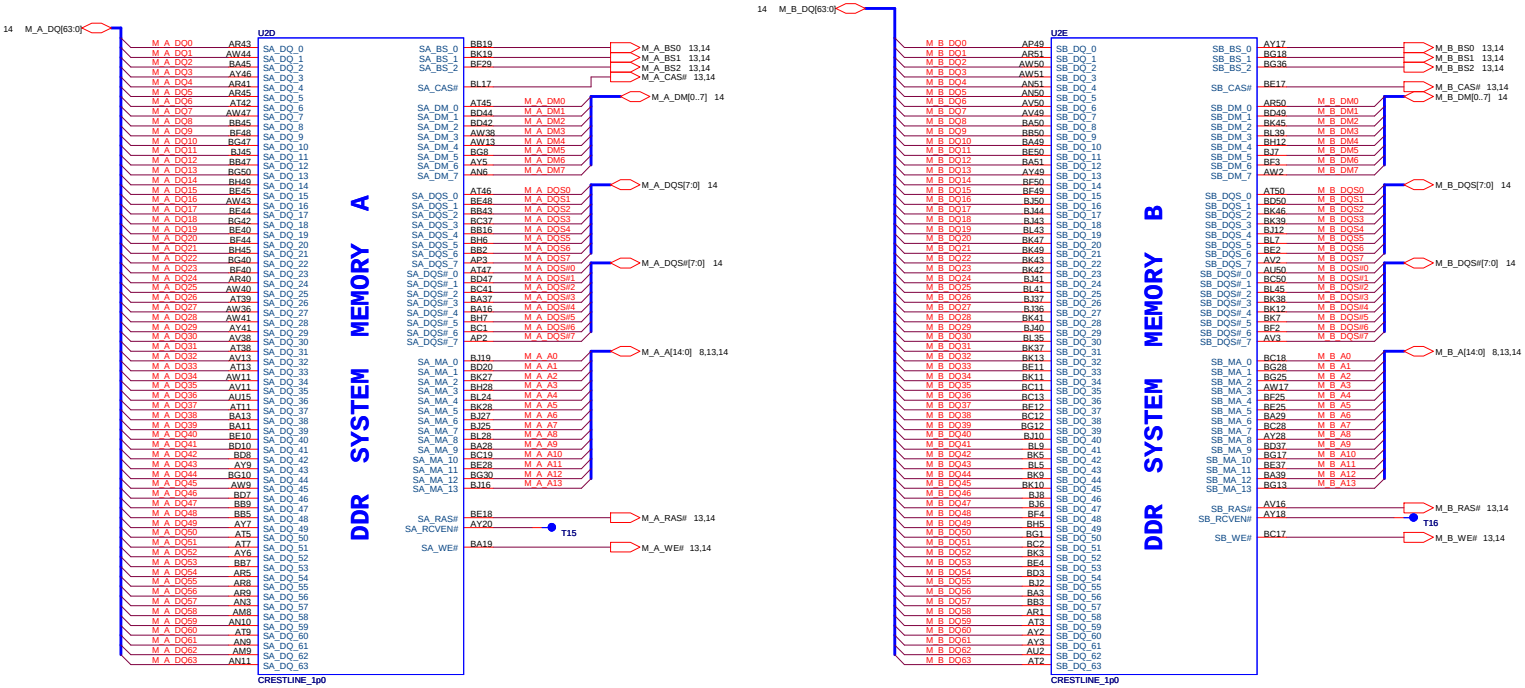
Date: Monday, June 25, 2007 Sheet 6 of 44



965GM P/N:AJ0QN120T45
965PM P/N:AJ0QN140T46

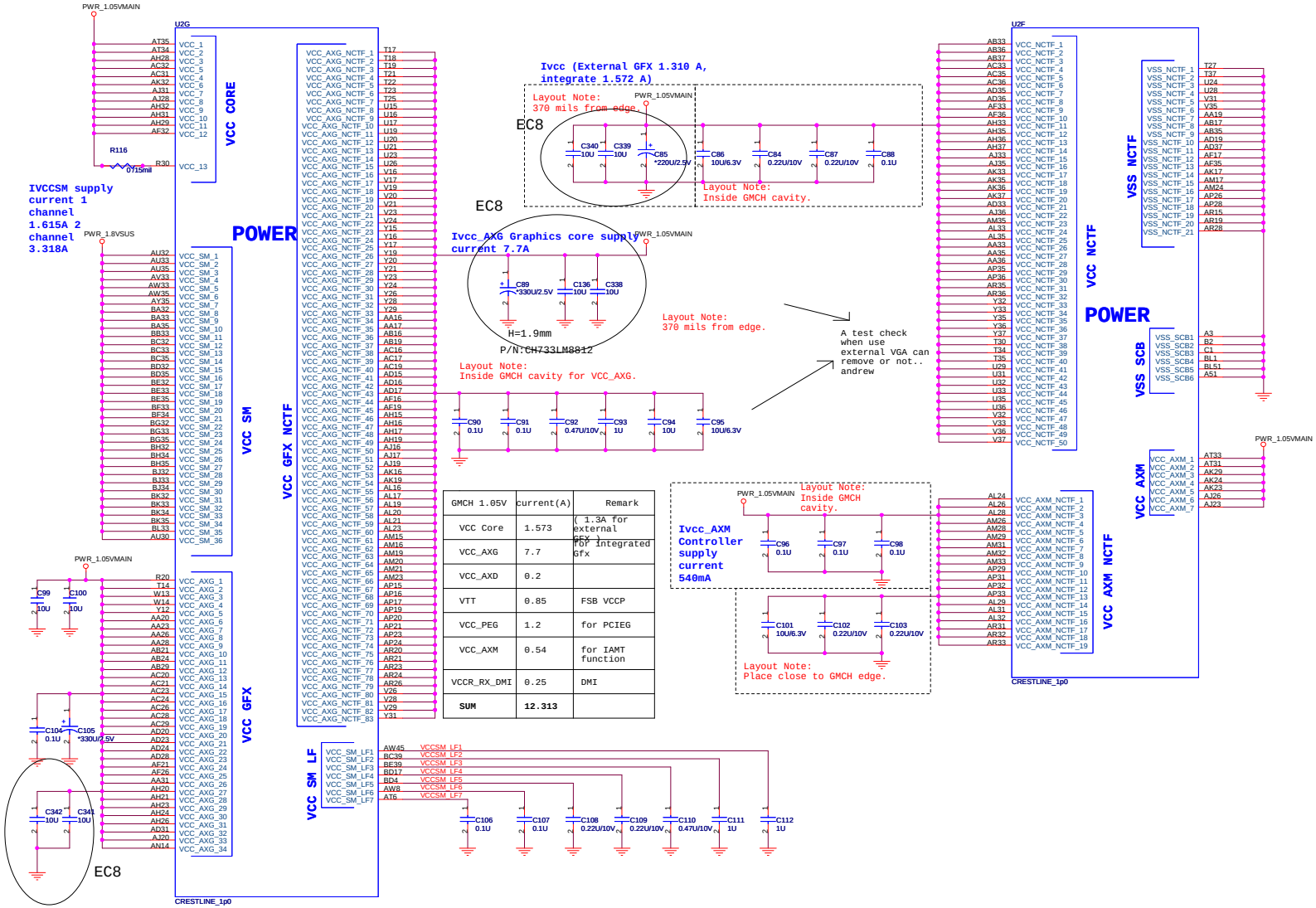
QUANTA COMPUTER		
Title: Crestline_A (HOST)		
Size: Custom	Document Number: FJ1 MAIN BOARD	Rev: 1A
Date: Monday, June 25, 2007	Sheet 7 of 44	



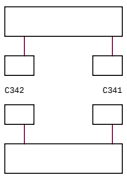


QUANTA COMPUTER

Title	Crestline_C (DDR2)	
Size: Custom	Document Number: FJ1 MAIN BOARD	Rev: 1A
Date: Monday, June 25, 2007	Sheet 9 of 44	



GMCH 1.05V	current(A)	Remark
VCC Core	1.573	(1.3A for external GFX)
VCC_AXG	7.7	for integrated Gfx
VCC_AXD	0.2	
VTT	0.85	FSB VCCP
VCC_PEG	1.2	for PCIEG
VCC_AXM	0.54	for IAMT function
VCCR_RX_DMI	0.25	DMI
SUM	**12.313**	



QUANTA COMPUTER

Title: Crestline_D (VCC,NCTF)

Size: Custom | Document Number: FJ1 MAIN BOARD | Rev: 1A

Date: Monday, June 25, 2007 | Sheet 10 of 44

LVDS Disable/Enable guideline

External VGA with EV@part,Internal VGA with IV@ part

Signal	Ef SDVO Disable LVDS Disable	Ef LVDS Enable
VCCD_LVDS	GND	1.8V
VCCA_LVDS	GND	1.8V
VCC_TX_LVDS	GND	1.8V

CRT/TV Disable/Enable guideline

External VGA with EV@part,Internal VGA with IV@ part

Ball	Enable	Disable	Ball	Enable	Disable
VCCA_CRT_DAC	3.3V	GND	VCCA_TVC_DAC	3.3V	GND
VCCD_CRT	1.5V	GND	VCCD_TVDAC	1.5V	1.5V
VCCD_QDAC	1.5V	GND	VCCA_DAC_BG	3.3V	GND
VCCA_TVA_DAC	3.3V	GND	VSS_DAC_BG	GND	GND
VCCA_TVB_DAC	3.3V	GND	VCCSYNC	3.3V	GND

IV&EV Dis/Enable setting

FB_180ohm+-25%_100mHz_1500mA_0.09ohm DC

FB_180ohm+-25%_100mHz_1500mA_0.09ohm DC

FB_120ohm+-25%_100mHz _200mA_0.2ohm DC

FB_220ohm+-25%_100MHz _2A_0.1ohm DC

0.1Caps should be placed 200 mils with in its pins.

Ivcc_VTT FSB supply current 0.85A

Place on the edge.

Place on the edge.

Ivcca_PEG_BG supply current 100mA

Ivcc_DMI supply current 100mA

Place caps close to VCC_AXD.

Ivcc_PEG supply current 1.2A

Ivcc_RX_DMI supply current 250mA

Place caps close to VCC_AXF

EC8

EC12

C127

+3V_VCC_HV

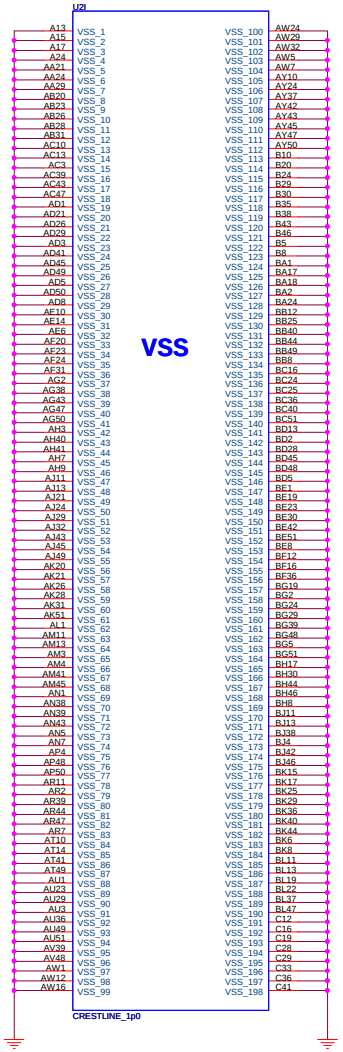
40 mil wide

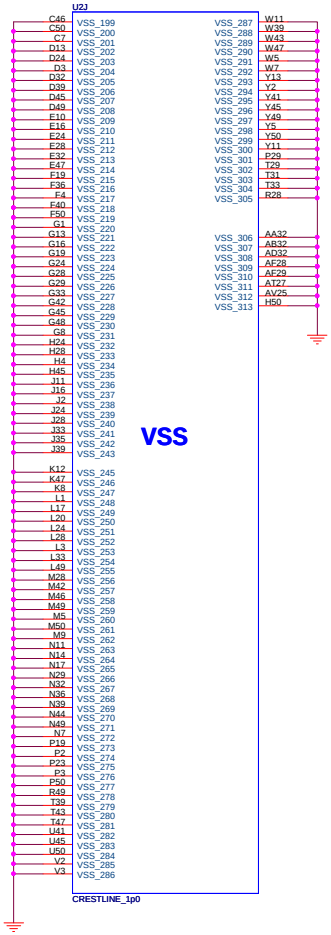
QUANTA COMPUTER

Title: Crestline_E (Power)

Size: Custom | Document Number: FJ1 MAIN BOARD | Rev: 1A

Date: Monday, June 25, 2007 | Sheet 11 of 44



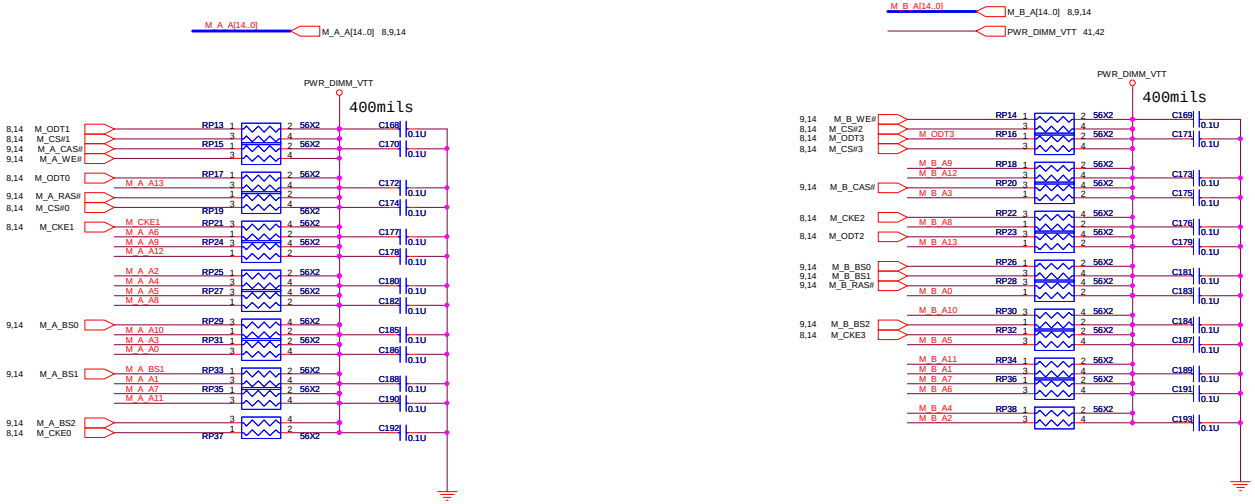


Title	Crestline_F (VSS)
Size: Custom	Document Number: FJ1 MAIN BOARD
Rev: 1A	
Date: Monday, June 25, 2007	Sheet 12 of 44

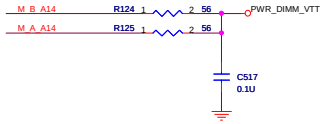
QUANTA COMPUTER

DDRII DUAL CHANNEL A,B.

DDRII A CHANNEL

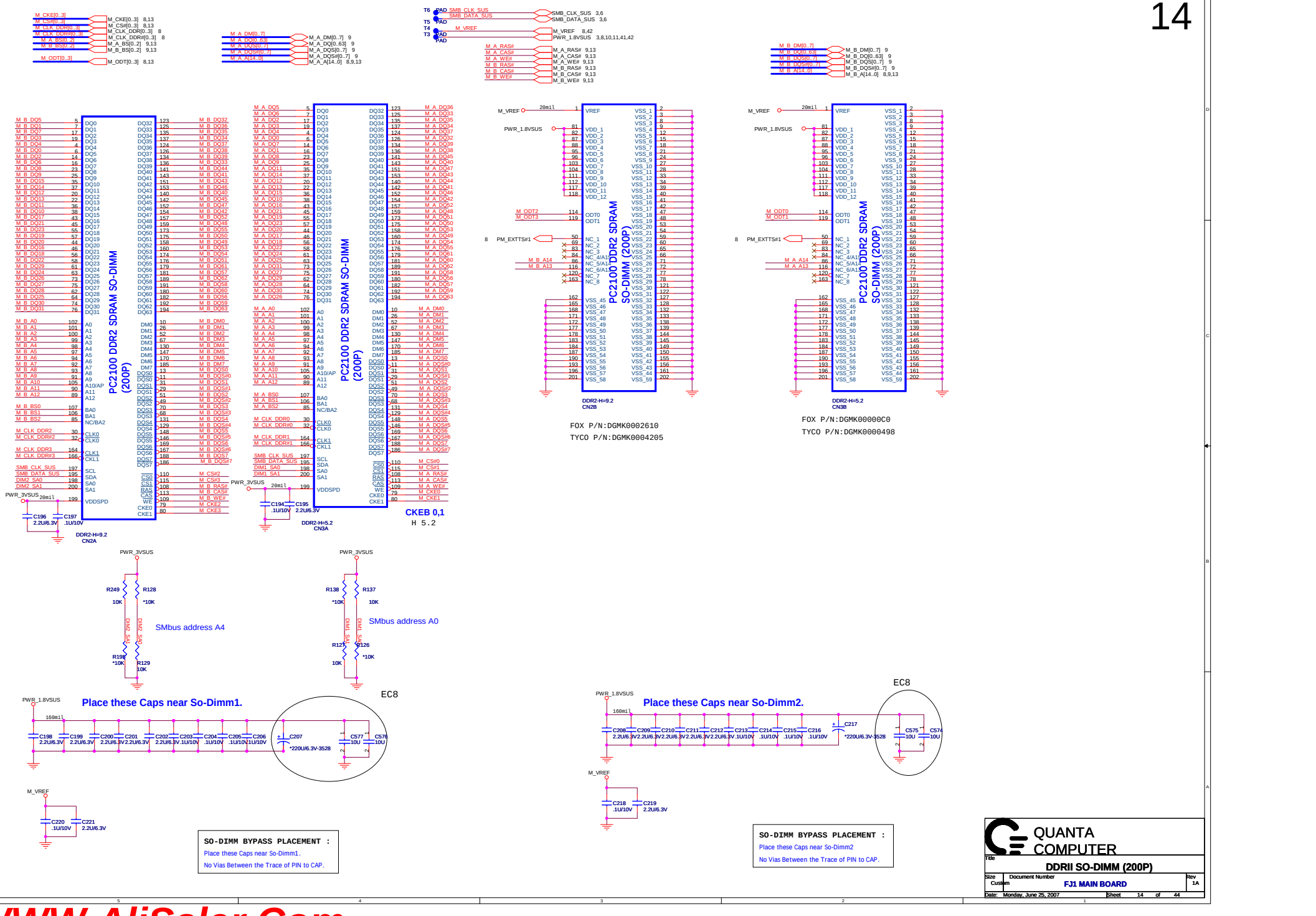


DDRII B CHANNEL



QUANTA COMPUTER

Title	DDRII RES.ARRAY	
Size: Custom	Document Number: FJ1 MAIN BOARD	Rev: 1A
Date: Monday, June 25, 2007	Sheet 13 of 44	

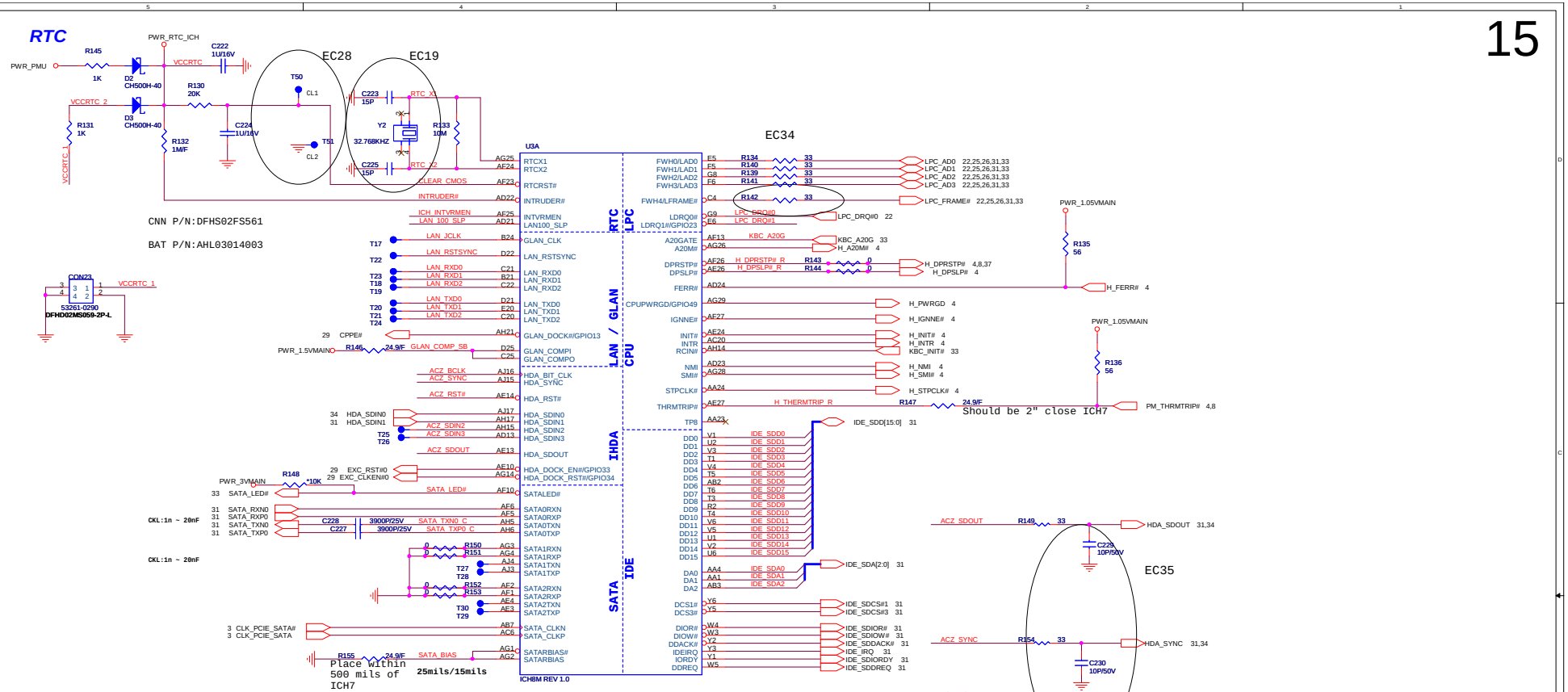


QUANTA COMPUTER

Title: DDRII SO-DIMM (200P)

Size: Custom | Document Number: FJ1 MAIN BOARD | Rev: 1A

Date: Monday, June 25, 2007 | Sheet 14 of 44



SB Strap

ICH8-M Internal VR Enable strap (Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)

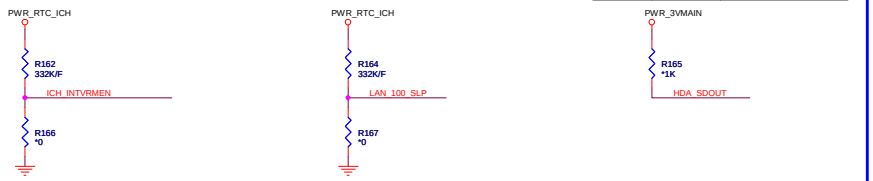
INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)

ICH8-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1.05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)

XOR Chain Entrance Strap

ICH_RSV0	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1



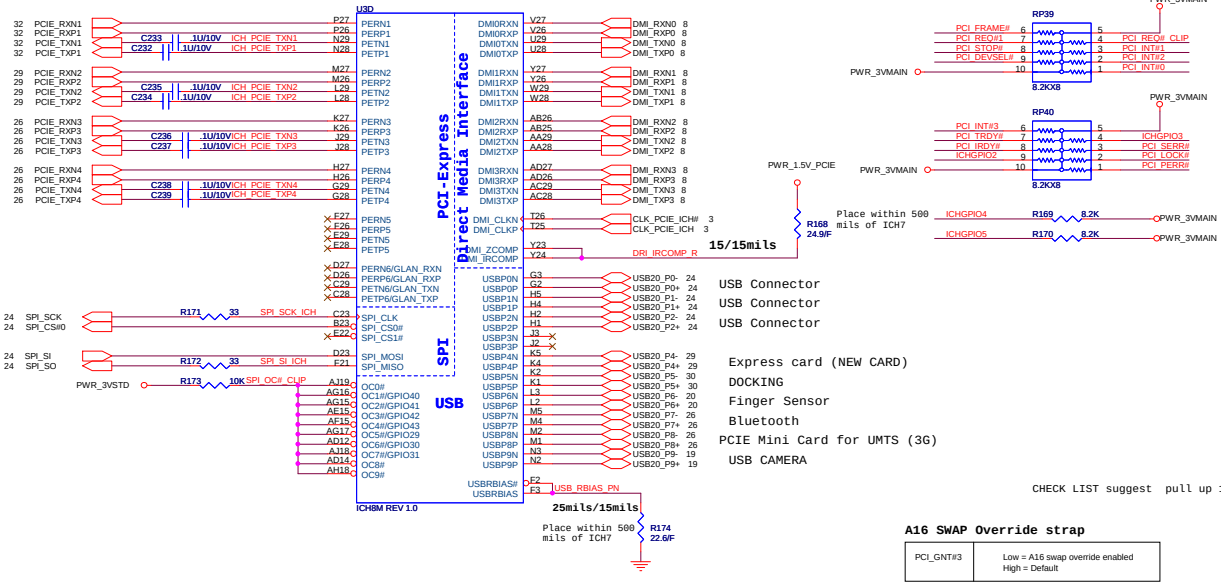
QUANTA COMPUTER			
Title: ICH8-M HOST (1 of 4)			
Size: Custom	Document Number: FJ1 MAIN BOARD		Rev: 1A
Date: Monday, June 25, 2007	Sheet 15 of 44		

PCIE-LAN

EXPRESS CARD(NEW CARD)

MINI CARD PCI-E 3G

MINI CARD PCI-E



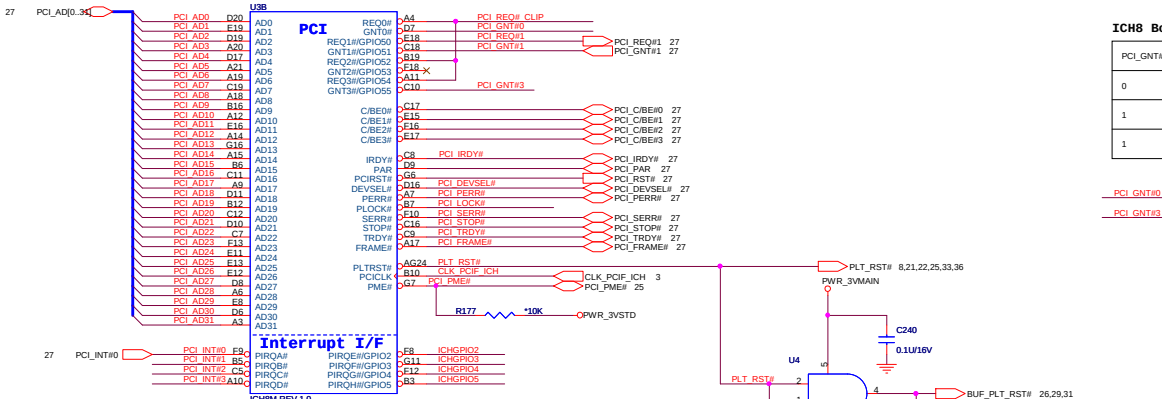
USB Connector
USB Connector
USB Connector

Express card (NEW CARD)
DOCKING
Finger Sensor
Bluetooth
PCIE Mini Card for UMTS (3G)
USB CAMERA

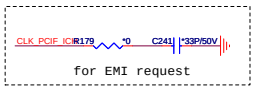
CHECK LIST suggest pull up 10k

A16 SWAP Override strap

PCI_GNT#3	Low = A16 swap override enabled High = Default

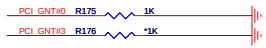


Don't connect to PCI device / Express card



ICH8 Boot BIOS select

PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC



QUANTA COMPUTER

Title: ICH8-M PCIE (2 of 4)

Size: Custom | Document Number: FJ1 MAIN BOARD | Rev: 1A

Date: Monday, June 25, 2007 | Sheet 16 of 44

PWR_3VMAIN 3,4,6,8,11,15,16,18,19,20,21,22,24,25,26,27,29,31,32,33,34,35,36,37,38

PWR_3VSTD 16,18,19,25,26,29,31,32,36,38,41

PWR_3VSTD

SMB_CLK_STD R180 10K
SMB_DATA_STD R182 10K
PCIE_WAKE# R183 1K
SERB_RI# R188 10K
SYS_RST# R187 1K

PWR_3VSTD

CL_RST#1 R181 10K
SMLINK0 R185 10K
SMLINK1 R184 10K
PLLB# R186 10K
EXTSMI# R190 10K
SMB_ALERT# R189 10K

U3C

6 SMB_CLK_STD
6 SMB_DATA_STD
SMB_CLK_STD AJ26 SMBCLK
SMB_DATA_STD AD19 SMBDATA
CL_RST#1 AG21 LINKALERT#
SMLINK0 AC17 SMLINK0
SMLINK1 AE19 SMLINK1

SMB

36 SERB_RI#
SERB_RI# AF17 RI#

22,23,31 SUSTAT#
SUSTAT# F4
SYS_RST# AD15 SUS_STAT#/LPCPD#
T1
SYS_RESET#

8 PM_BMBUSY#
PM_BMBUSY# AG12 BMBUSY#/GPIO0

33 SMB_ALERT#
SMB_ALERT# AG22 SMBALERT#/GPIO11

SYS GPIO

3 PM_STPPCI#
3 PM_STPCPU#
R193 0
R192 0
STP_PCI#/GPIO15 AE20
STP_CPU#/GPIO25 AG18

22,27,31,33 PCI_CLKRUN#
PCI_CLKRUN# AH11 CLKRUN#/GPIO32

close to ICH

25,29 PCIE_WAKE#
22,26,27,31,33 SERIRQ
PCIE_WAKE# AE17 WAKE#
SERIRQ AF12 SERIRQ
PM_THRM# AC13 THRM#

Power MGT

25 PWROK_VRM_ICH
VRMPWRGD AJ20

ICH_TP7
TP7 AJ22

PWR_3VSTD

R197 100K

30,33 LCDCL#_SW
D4 LSS355
KBC_SCI 33
LCDCL# AE16
25 EXTSMI#
EXTSMI# AC19
MEM_ID0 AG8
MEM_ID1 AH12
AE11
AG10
AH25
AD16
AG13

3 CLKREQ#_SATA

SMB_CNT1 AF9
SMB_CNT2 AJ11
ICH_GPIO48 AD10

25 SPKSYS
SPKSYS AD9 SPKR

8 MCH_ICH_SYNC#
MCH_SYNC# AJ13

TP3 AJ21

ICH8M REV 1.0

R203 *1K

Stuff for XOR chain testing

TACH1/GPIO1 AJ8
TACH2/GPIO6 AJ9
TACH3/GPIO7 AH9
GPIO8 AE16
GPIO12 AC19
TACH0/GPIO17 AG8
GPIO18
GPIO20
SCLOCK/GPIO22
QRT_STATE0/GPIO27
QRT_STATE1/GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48

GPIO Controller Link

SATA0GP/GPIO21 AJ12
SATA1GP/GPIO19 A10
SATA2GP/GPIO36 AF11
SATA3GP/GPIO37 AG11

R191 10K
SPI_CS# ICHGPIO36
SPI_CS#_GPIO 24
SMB_CNT0

Clocks

CLK14 AG9
CLK48 G5
CLK_14M_ICH
CLK_48M_ICH

CLK_14M_ICH 3
CLK_48M_ICH 3

SUSCLK D3
CLK_32K_STD
CLK_32K_STD 31

SLP_S3# AG23
SLP_S4# AF21
SLP_S5# AD18
SUSB# 25
SUSC# 25,33,41

EC30

C242 5PF
C243 5PF

S4_STATE#/GPIO26 AH27

T2

PWROK AE23
PWROK_3VMAIN
PWROK_3VMAIN 8,36

DPRSLPVR/GPIO16 AJ14
R194 100 DPRSLPVR
DPRSLPVR 8,37

BATLOW# AE21
PLLB#
PLLB# 36

PWRBTN# C2
BSRBTN# 25

LAN_RST# AH20
PLTRST_LAN# R196 10K

RSMRST# AG27
RSMRST#
RSMRST# 25,26

CK_PWRGD E1
CLK_PWROK 3

CLPWROK E3
R198 0
PWROK_3VMAIN 8,36
CL_PWROK 8

SLP_M# AJ25

LAN_RST# pin : 1.if used pci LAN please tie to PLTRST#
2.if used PHY LAN please tie to RSMRST#

CL_CLK0 F23
CL_CLK1 AE18
CL_CLK0 8

CL_DATA0 F22
CL_DATA1 AF19
CL_DATA0 8

CL_VREF0 D24
CL_VREF1 AH23
CL_VREF0_ICH
CL_VREF1_ICH

CL_RST# AJ23
CL_RST#0 8

MEM_LED/GPIO24 AJ27
ME_EC_ALERT/GPIO10 AJ24
EC_ME_ALERT/GPIO14 AF22
WOL_EN/GPIO9 AG19
ICH_GPIO10
ICH_GPIO14
ICH_GPIO9

PWR_3VMAIN

R199 *3.24K/F
R201 *453/F

Controller Link 1
VREF for IAMT
support only

PWR_3VMAIN

R200 3.24K/F
R202 453/F

Controller Link 0
VREF for IAMT
support only

RSMRST#
R312 *10K
C532 100P

No Reboot strap

ACZ_SPKR	Low = Default High = No Reboot

PWR_3VMAIN

SPKSYS R206 *1K

PWR_3VMAIN

PM_THRM# R205 8.2K
PCI_CLKRUN# R204 8.2K
ICHGPIO1 R207 10K
PM_STPPCI# R208 *10K
PM_STPCPU# R209 *10K
SERIRQ R211 10K
SPWG_EXIST R210 10K
MEM_ID0 R213 10K
MEM_ID1 R212 10K

ICH_GPIO48 R215 10K
ICH_TP7 R214 *1K
ICHGPIO36 R217 10K

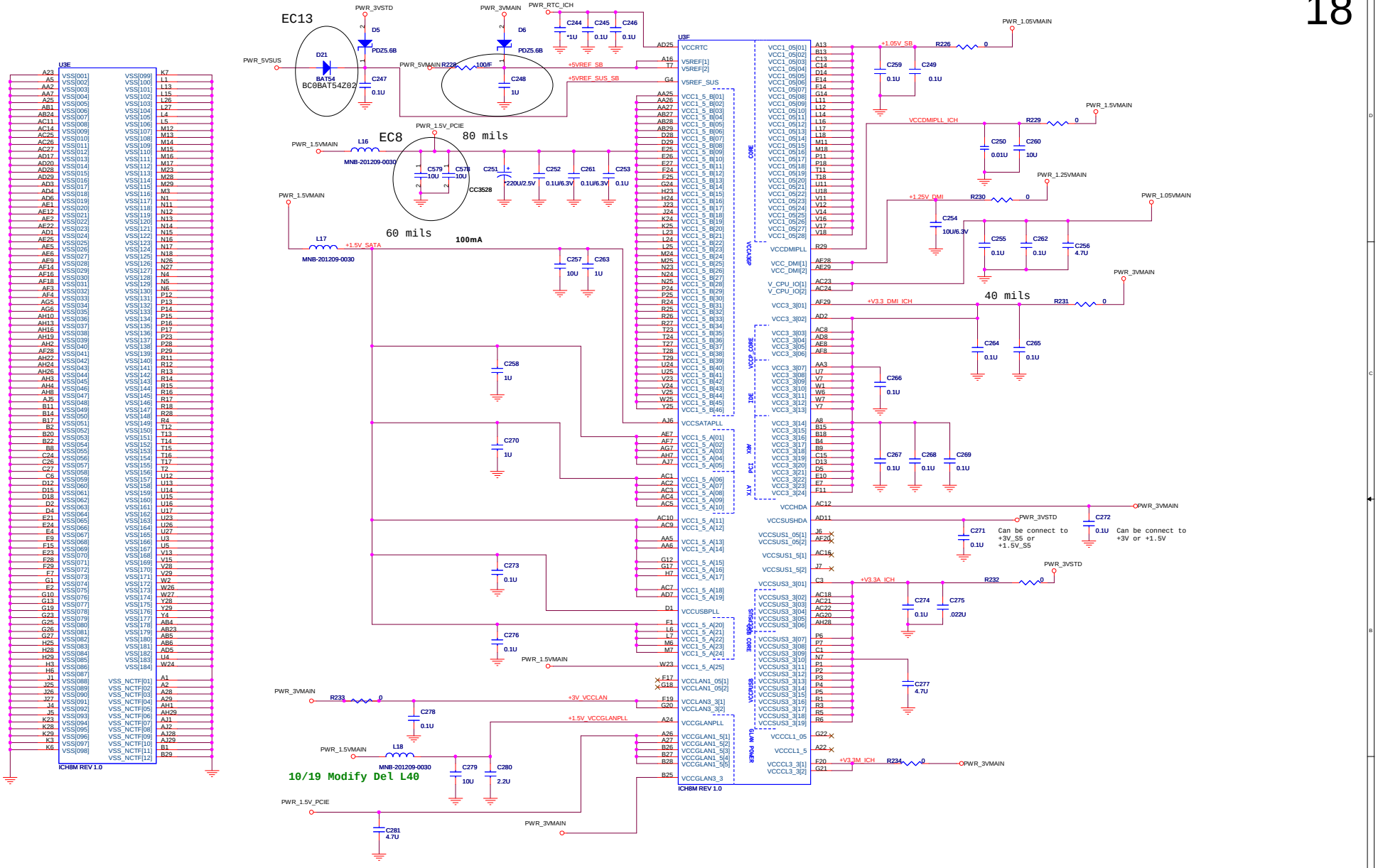
ICH_GPIO10 R219 10K
ICH_GPIO14 R218 10K
ICH_GPIO9 R221 10K
PWROK_3VMAIN R220 10K
PWROK_VRM_ICH R222 10K
SMB_CNT0 R224 10K
SMB_CNT1 R223 10K
SMB_CNT2 R225 10K

QUANTA COMPUTER

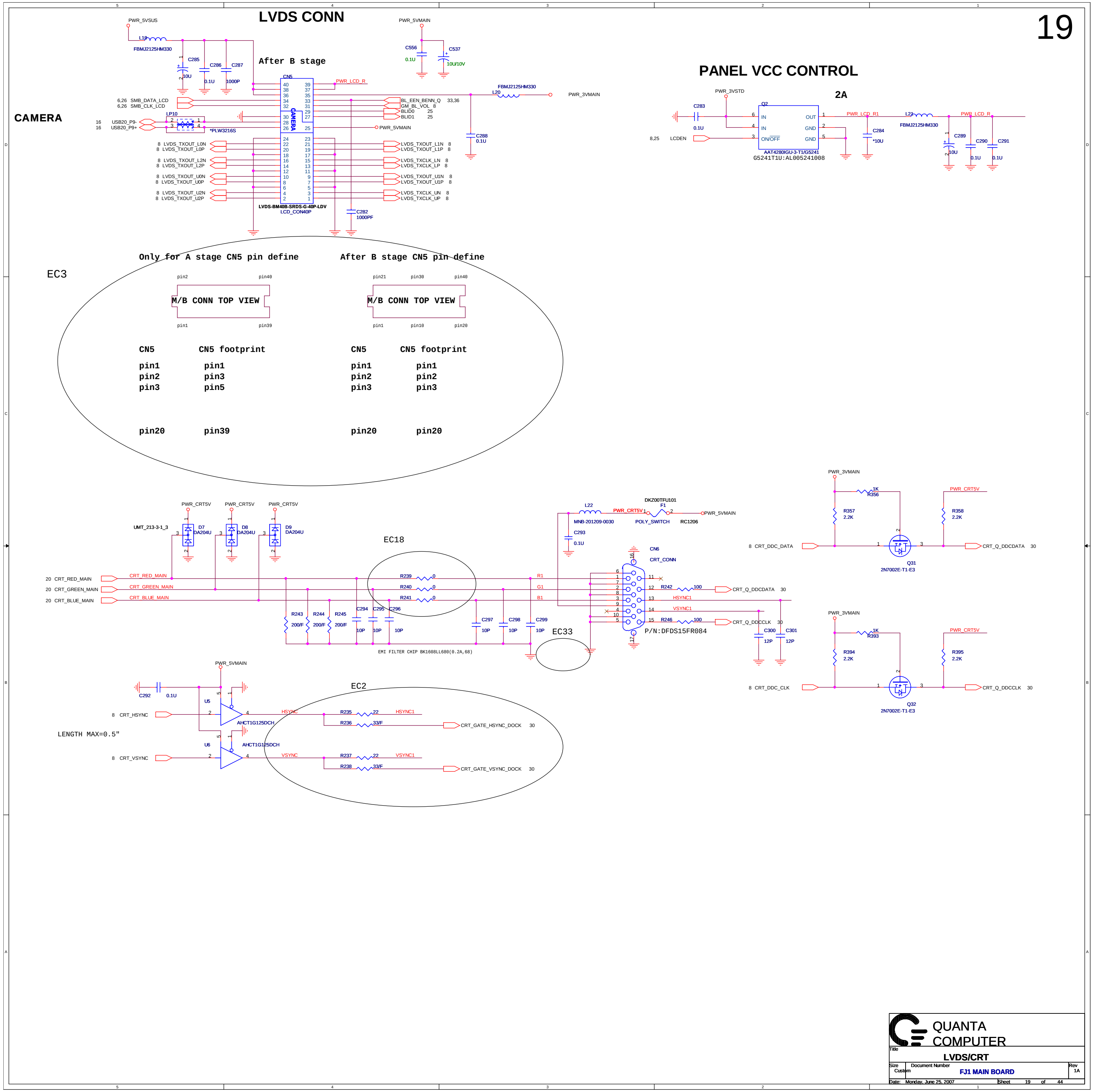
Title: ICH8-M GPIO (3 of 4)

Size: Custom | Document Number: FJ1 MAIN BOARD | Rev: 1A

Date: Monday, June 25, 2007 | Sheet 17 of 44

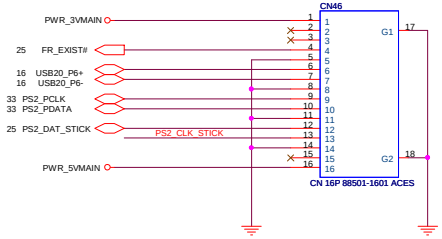


QUANTA COMPUTER	
Title	ICH8-M Power (4 of 4)
Size: Custom	Document Number: FJ1 MAIN BOARD
Rev: 1A	
Date: Monday, June 25, 2007	Sheet 18 of 44

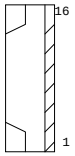


19
LVDS CONN
After B stage
CAMERA
PANEL VCC CONTROL
2A
PWR_5VSUS
PWR_5VMAIN
PWR_3VMAIN
PWR_3VSTD
FBMJ2125HM330
CN5
LVDS-BM40B-SRDS-G-40P-LDV
LCD_CON40P
6,26 SMB_DATA_LCD
6,26 SMB_CLK_LCD
16 USB20_P9-
16 USB20_P9+
LP10
*PLW3216S
BL_EEN_BENN_Q 33,36
GM_BL_VOL 8
BLID0 25
BLID1 25
8 LVDS_TXOUT_L0N
8 LVDS_TXOUT_L0P
8 LVDS_TXOUT_L2N
8 LVDS_TXOUT_L2P
8 LVDS_TXOUT_U0N
8 LVDS_TXOUT_U0P
8 LVDS_TXOUT_U2N
8 LVDS_TXOUT_U2P
LVDS_TXOUT_L1N 8
LVDS_TXOUT_L1P 8
LVDS_TXCLK_LN 8
LVDS_TXCLK_LP 8
LVDS_TXOUT_U1N 8
LVDS_TXOUT_U1P 8
LVDS_TXCLK_UN 8
LVDS_TXCLK_UP 8
PWR_LCD_R
Q2
AAT4280IGU-3-T1/G5241
G5241T1U:AL005241008
8,25 LCDEN
PWR_LCD_R1
EC3
Only for A stage CN5 pin define
After B stage CN5 pin define
M/B CONN TOP VIEW
M/B CONN TOP VIEW
CN5 CN5 footprint
pin1 pin1
pin2 pin3
pin3 pin5
pin20 pin39
CN5 CN5 footprint
pin1 pin1
pin2 pin2
pin3 pin3
pin20 pin20
PWR_CRT5V
UMT_213-3-1_3
D7 DA204U
D8 DA204U
D9 DA204U
20 CRT_RED_MAIN
20 CRT_GREEN_MAIN
20 CRT_BLUE_MAIN
EC18
EC33
EMI FILTER CHIP BK1608LL680(0.2A,68)
L22
MNB-201209-0030
DKZ00TFU101
F1
POLY_SWITCH
RC1206
CN6
CRT_CONN
P/N:DFDS15FR084
CRT_Q_DDCDATA 30
CRT_Q_DDCCLK 30
HSYNC1
VSYNC1
8 CRT_DDC_DATA
8 CRT_DDC_CLK
Q31 2N7002E-T1-E3
Q32 2N7002E-T1-E3
EC2
LENGTH MAX=0.5"
8 CRT_HSYNC
8 CRT_VSYNC
U5 AHCT1G125DCH
U6 AHCT1G125DCH
CRT_GATE_HSYNC_DOCK 30
CRT_GATE_VSYNC_DOCK 30
QUANTA COMPUTER
Title
LVDS/CRT
Size Custom
Document Number
FJ1 MAIN BOARD
Rev 1A
Date: Monday, June 25, 2007
Sheet 19 of 44

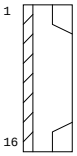
GLIDE PAD CONN



M/B
TOP VIEW

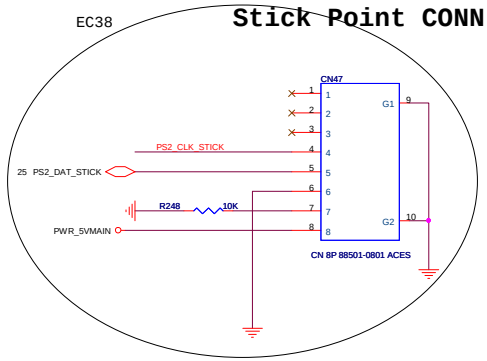


GLIDE PAD/B
TOP VIEW

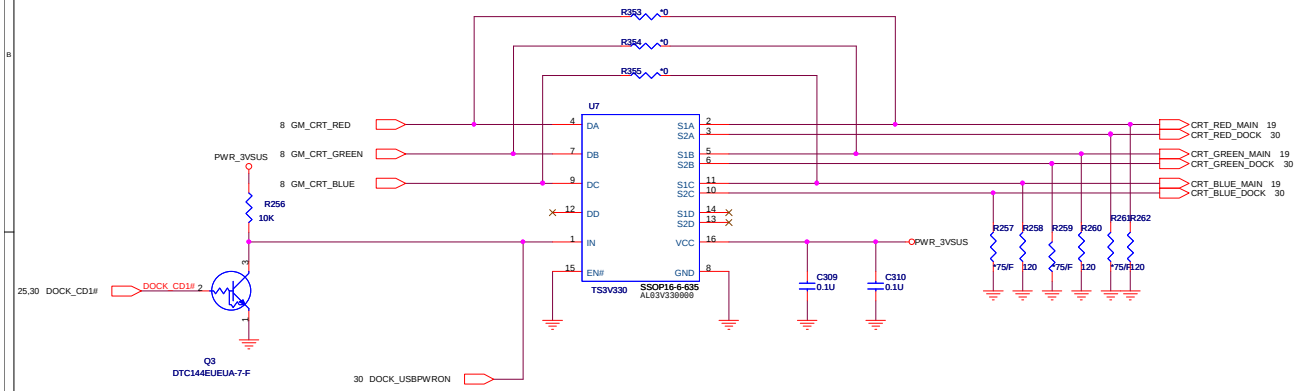


EC38

Stick Point CONN



CRT SW CIRCUIT

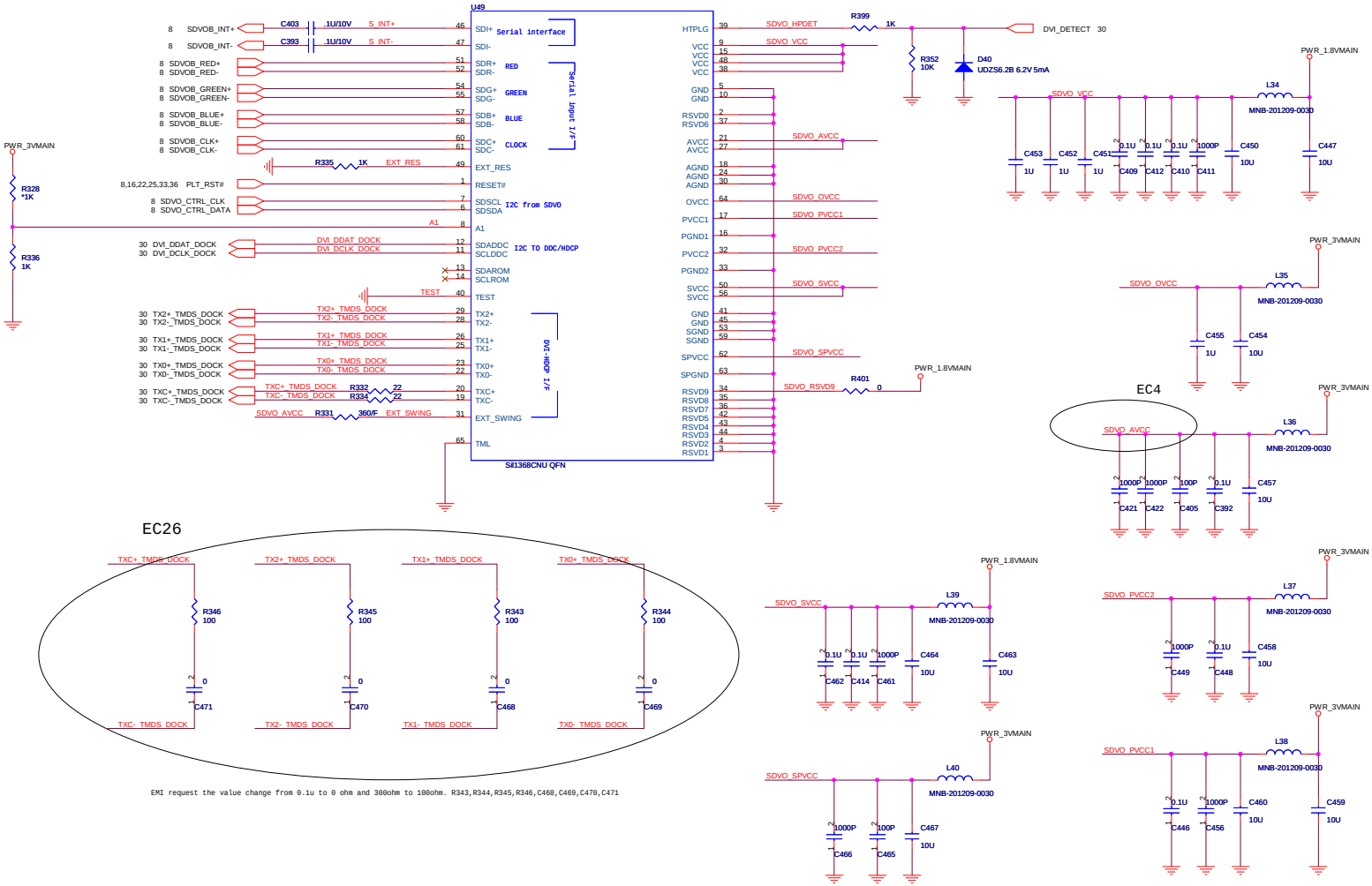


QUANTA COMPUTER

Title: CRT SW/GLIDE PAD/StickPoint

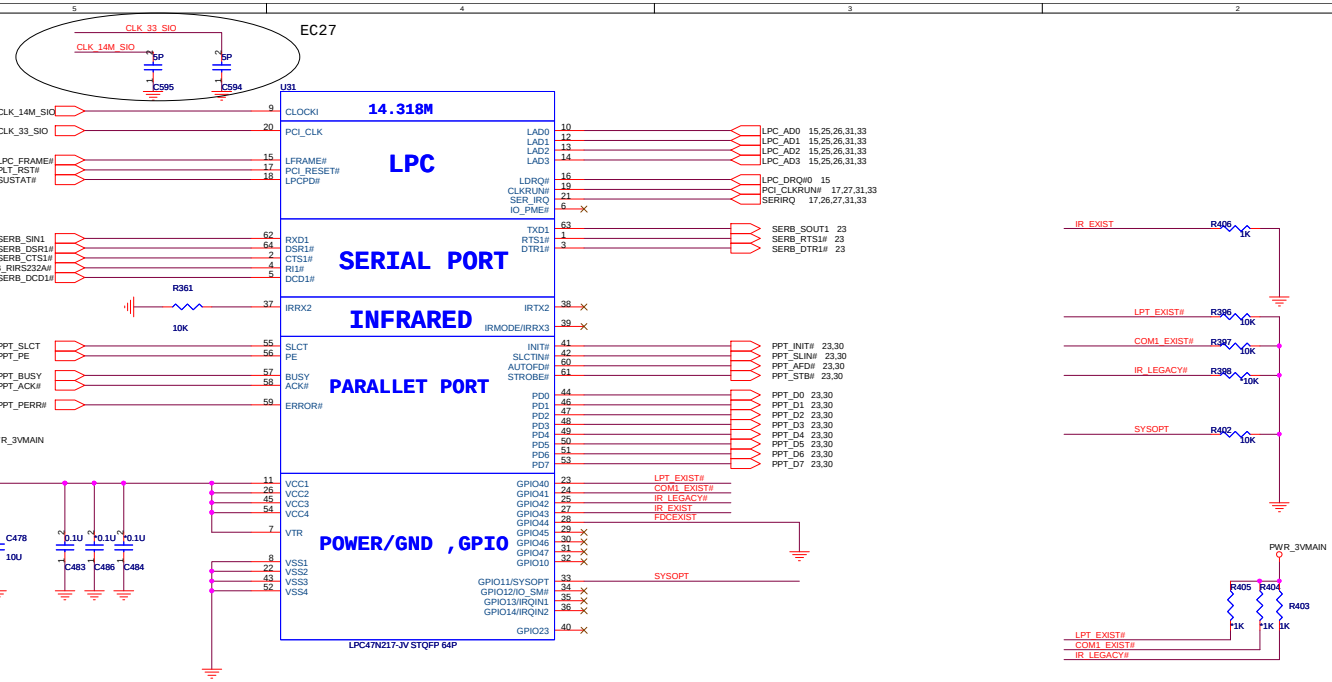
Size	Document Number	Rev
Custom	FJ1 MAIN BOARD	1A

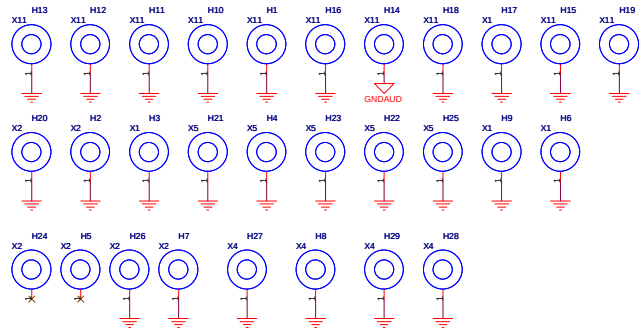
Date: Monday, June 25, 2007 Sheet 20 of 44

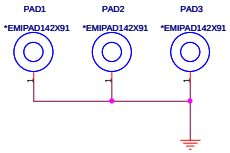


Title	DVI Transfer SI 1368
Size	Custom
Document Number	FJ1 MAIN BOARD
Rev	1A
Date	Monday, June 25, 2007
Sheet	21 of 44

QUANTA COMPUTER





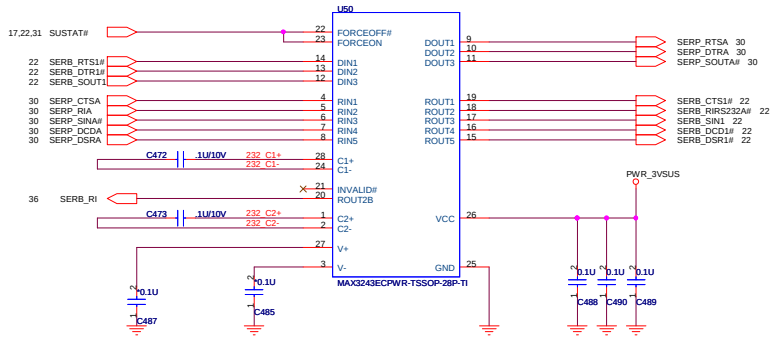


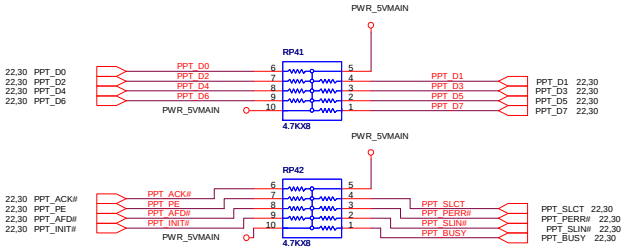
QUANTA COMPUTER

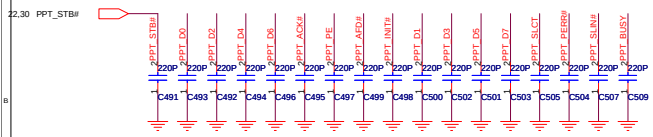
Title: SUPER I/O

Size: Custom | Document Number: FJ1 MAIN BOARD | Rev: 1A

Date: Monday, June 25, 2007 | Sheet 22 of 44



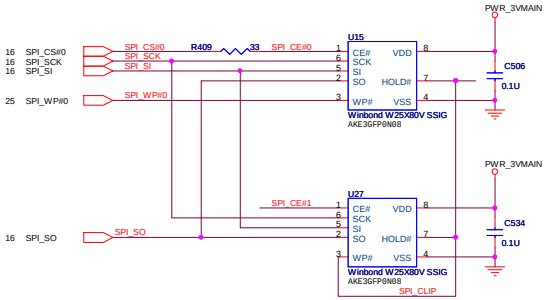


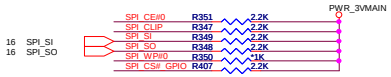


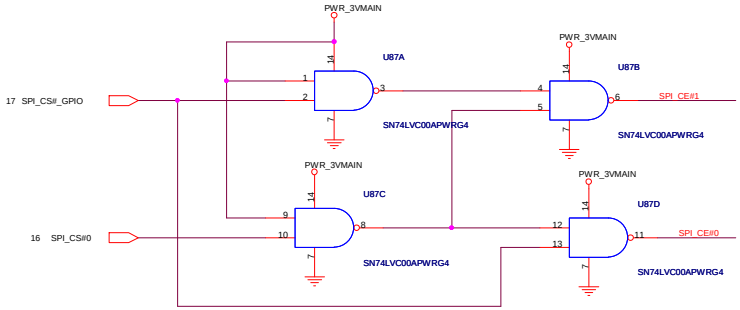
QUANTA COMPUTER

Title	COM /PARALLEL PORT	
Size: Custom	Document Number: FJ1 MAIN BOARD	Rev: 1A
Date: Monday, June 25, 2007	Sheet 23 of 44	

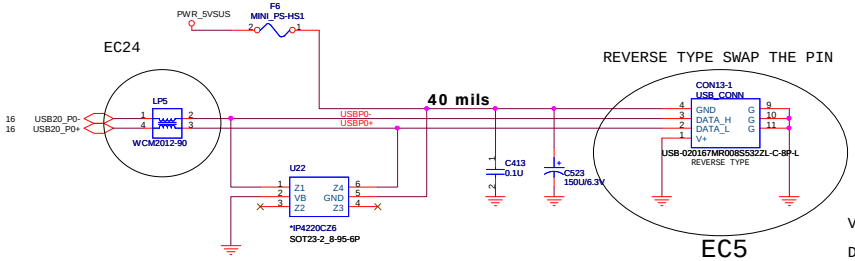
16Mbit (1M Byte), SPI







USB Interface

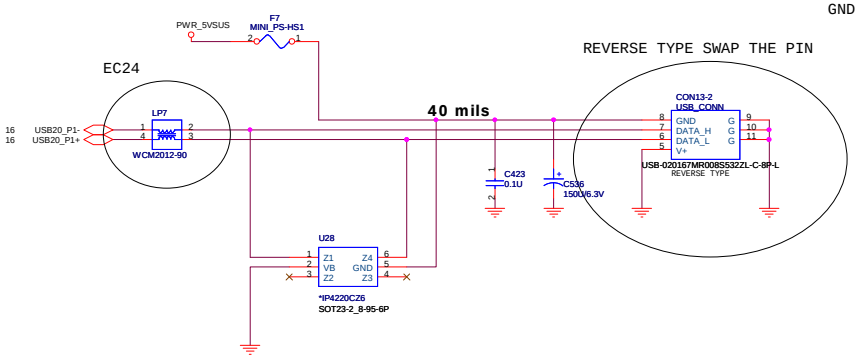


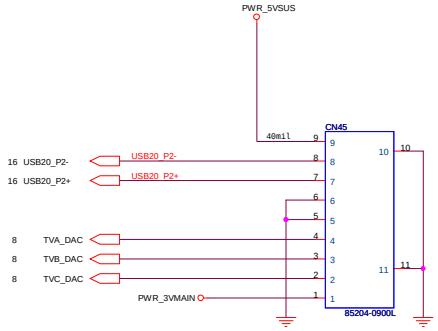
V+ ==>GND

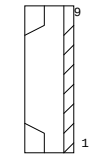
DATA_H ==>DATA_L

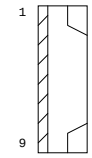
DATA_L ==>DATA_H

GND ==> V+



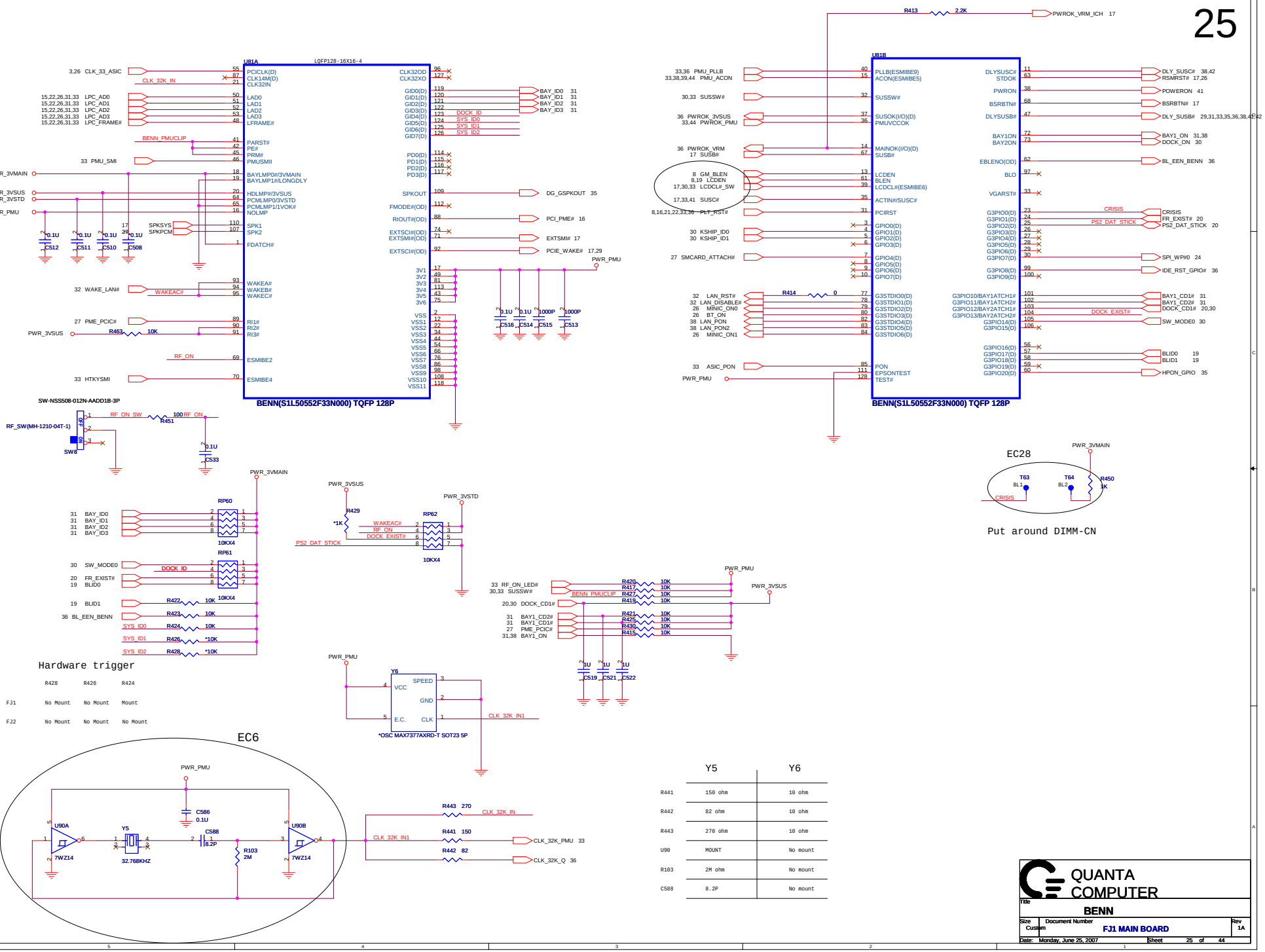




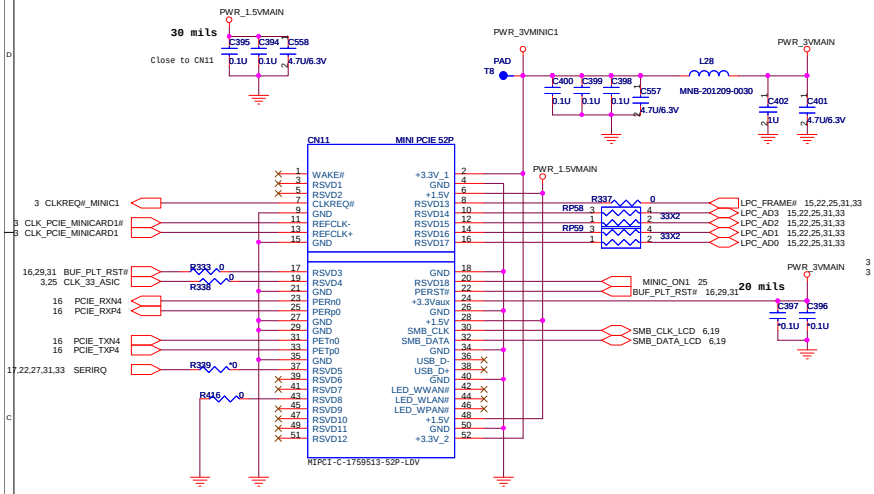


QUANTA COMPUTER

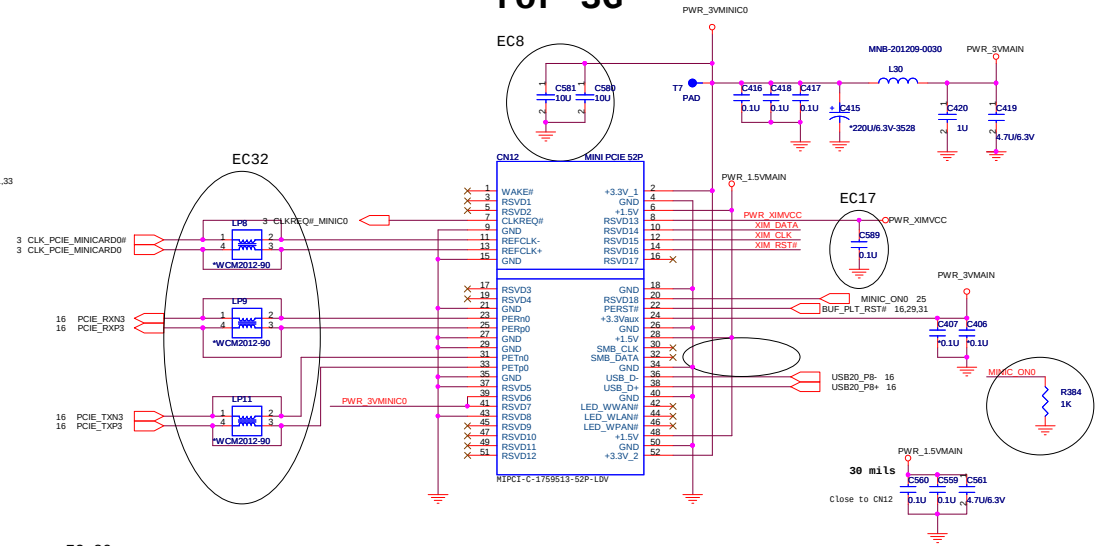
Title	SPI BIOS/USB port/TV CONN	
Size: Custom	Document Number: FJ1 MAIN BOARD	Rev: 1A
Date: Monday, June 25, 2007	Sheet 24 of 44	


U81A
LQFP128-16X16-4
BENN(S1L50552F33N000) TQFP 128P
U81B
BENN(S1L50552F33N000) TQFP 128P
SW-NSS508-012N-AADD1B-3P
RF_SW(MH-1210-04T-1)
SW8
Hardware trigger
R428 R426 R424
FJ1 No Mount No Mount Mount
FJ2 No Mount No Mount No Mount
EC6
EC28
Put around DIMM-CN
*OSC MAX7377AXRD-T SOT23 5P
Y5 Y6
R441 150 ohm 10 ohm
R442 82 ohm 10 ohm
R443 270 ohm 10 ohm
U90 MOUNT No mount
R103 2M ohm No mount
C588 8.2P No mount
QUANTA COMPUTER
Title BENN
Size Custom
Document Number FJ1 MAIN BOARD
Rev 1A
Date: Monday, June 25, 2007
Sheet 25 of 44

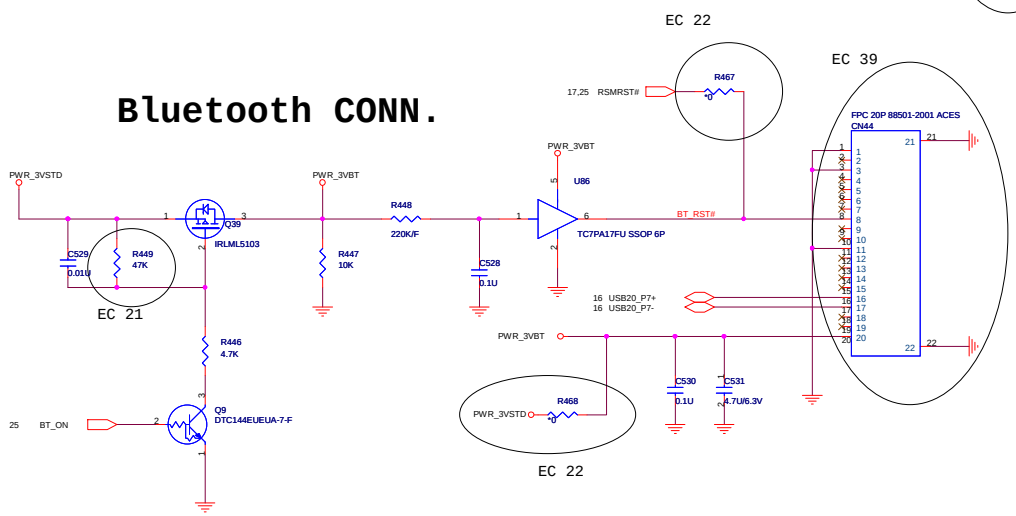
MINI CARD PCI-E



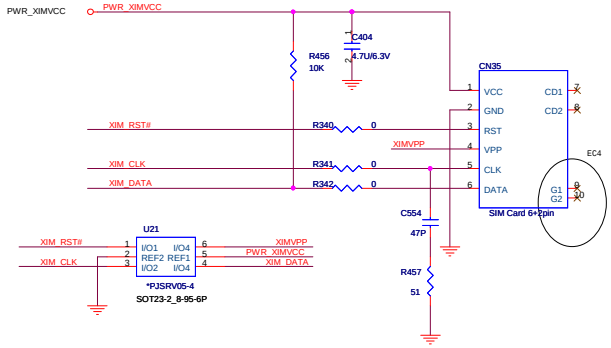
PCIE Mini Card for 3G



Bluetooth CONN.



SIM CARD

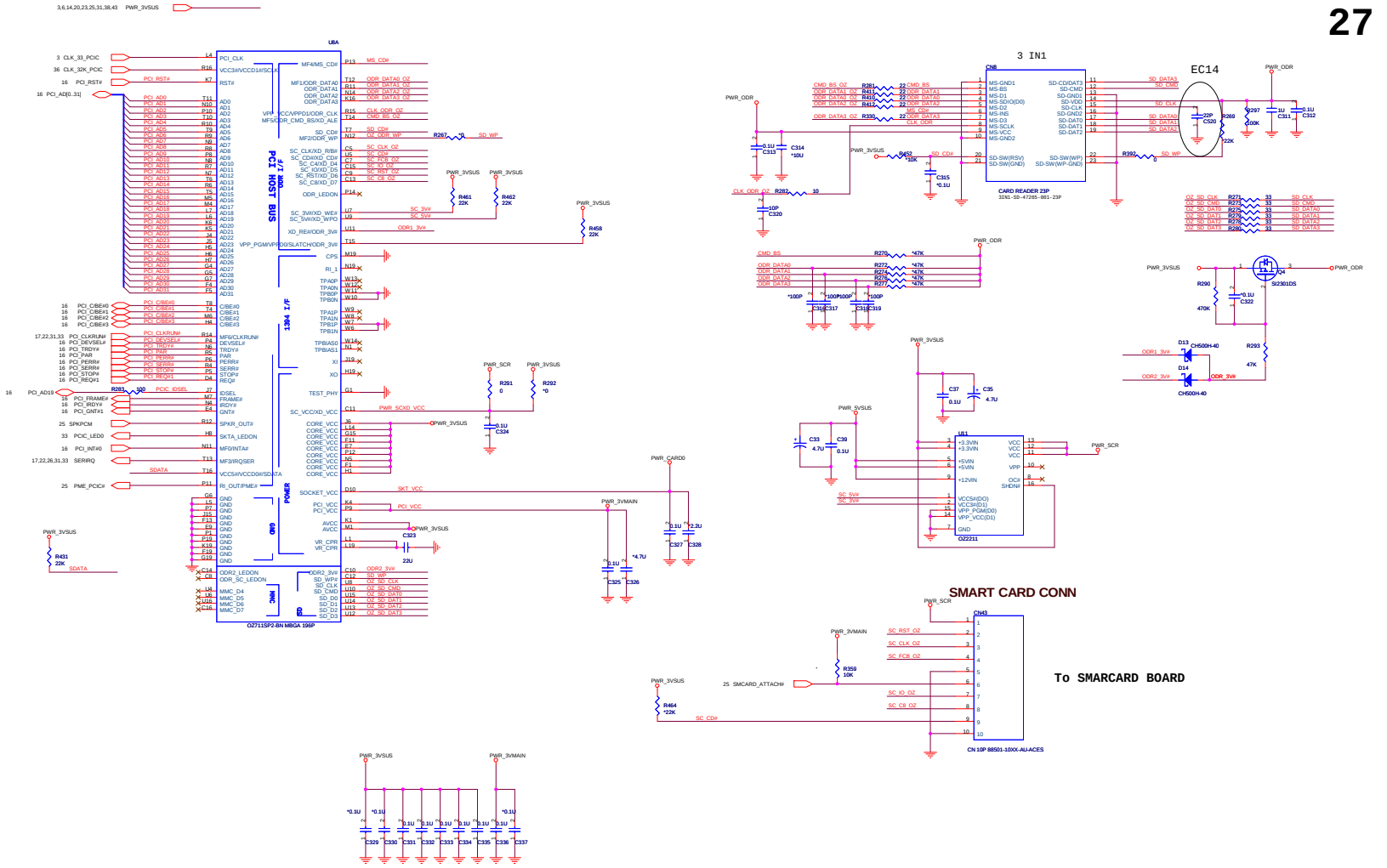


QUANTA COMPUTER

Title: MINI PCIE /SIM/BTOOTH

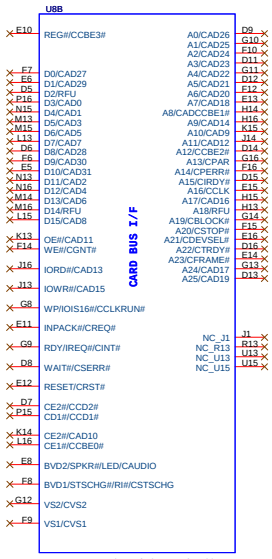
Size: Custom | Document Number: FJ1 MAIN BOARD | Rev: 1A

Date: Monday, June 25, 2007 | Sheet 26 of 44



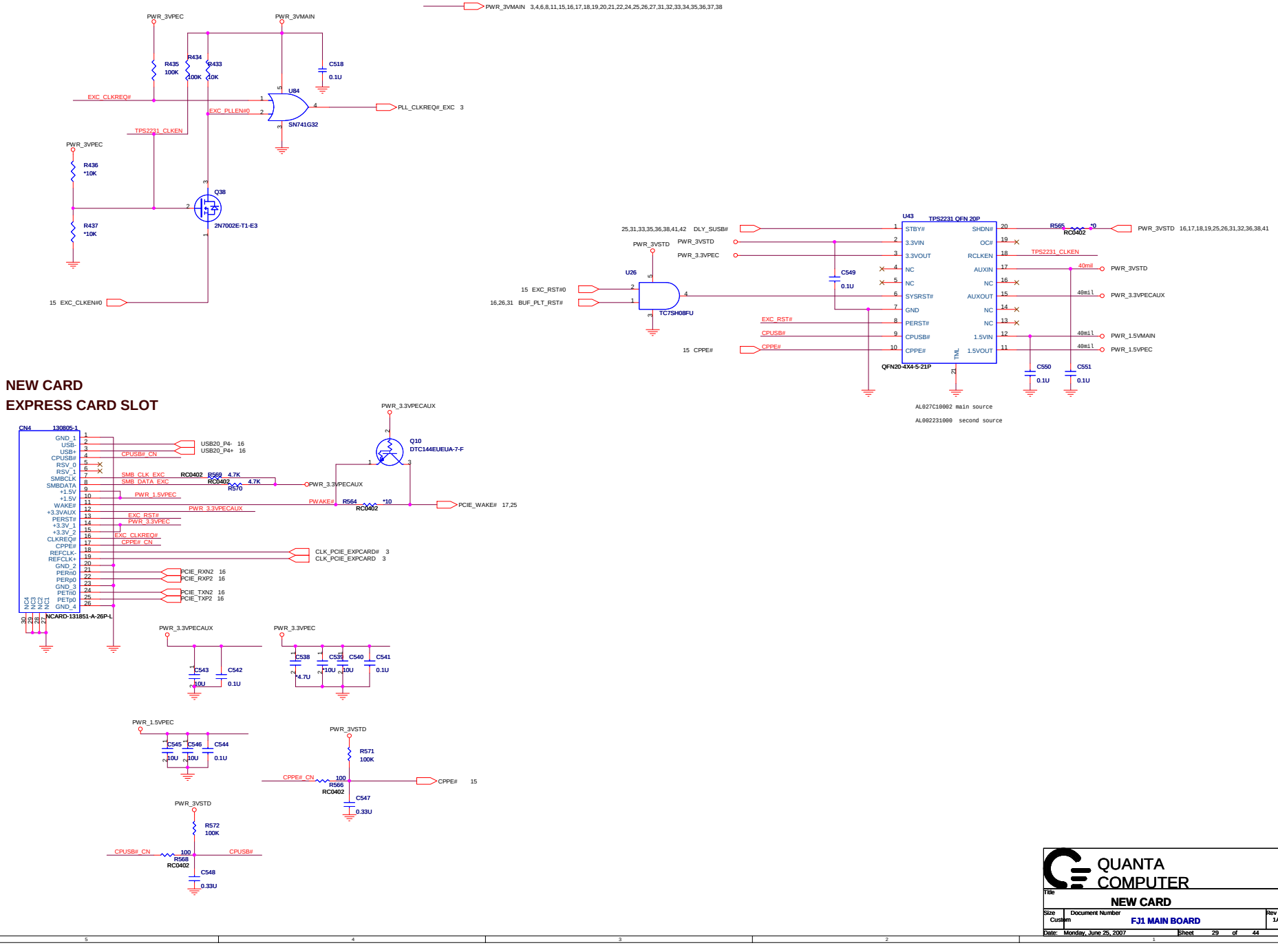
QUANTA COMPUTER

Title	27--OZ711 (1/2)/3 IN1 / SMART CARD CONN		
Size	Document Number		Rev
Custom	FJ1 MAIN BOARD		1A
Date: Monday, June 25, 2007	Sheet 27 of 44		

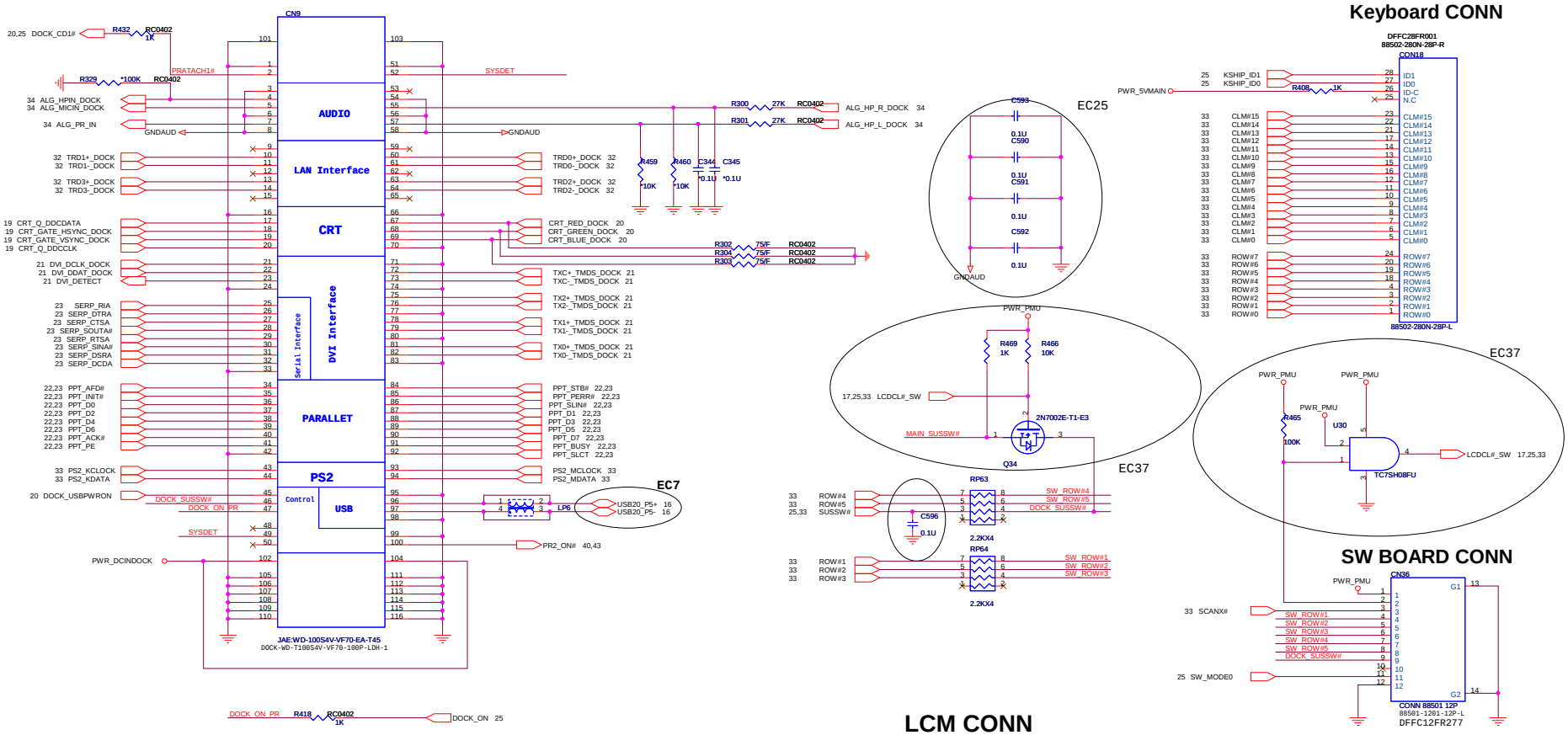


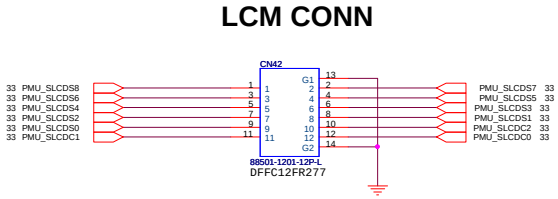
QUANTA COMPUTER

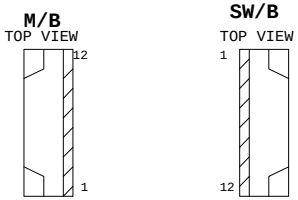
Title: OZ711 (NC)			
Size: Custom	Document Number: FJ1 MAIN BOARD		Rev: 1A
Date: Monday, June 25, 2007	Sheet 28 of 44		



QUANTA COMPUTER			
Title: NEW CARD			
Size: Custom	Document Number: FJ1 MAIN BOARD		Rev: 1A
Date: Monday, June 25, 2007	Sheet 29 of 44		







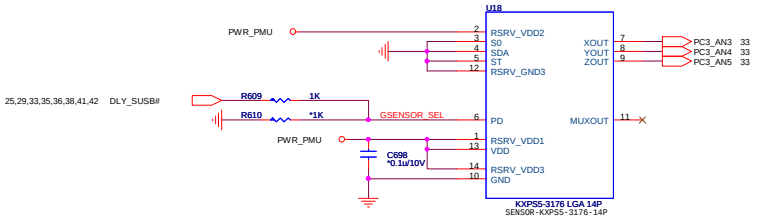
QUANTA COMPUTER

Title: DOCKING CN/ KB /LCM/SW

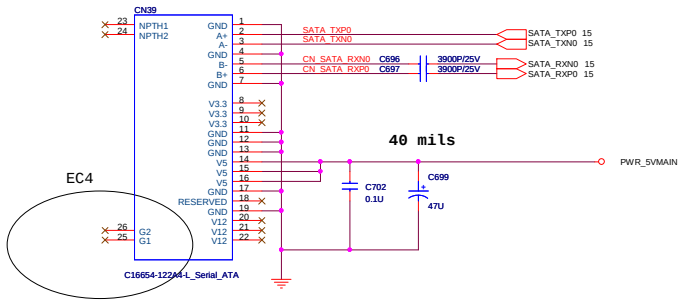
Size: Custom | Document Number: FJ1 MAIN BOARD | Rev: 1A

Date: Monday, June 25, 2007 | Sheet 30 of 44

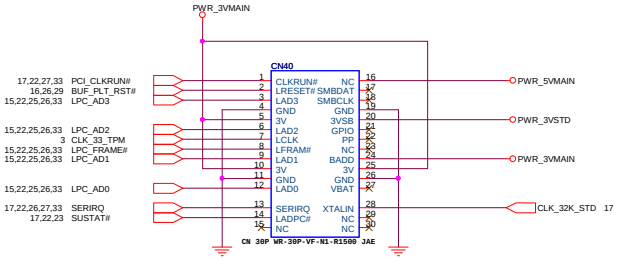
G-SENSOR



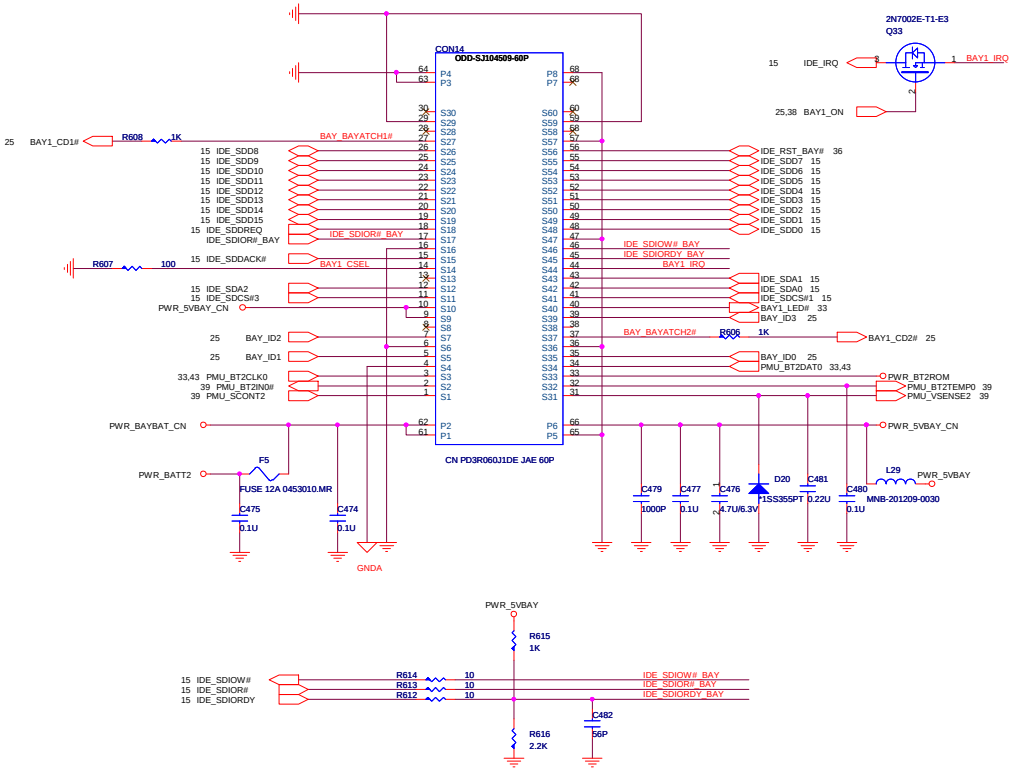
SATA CONN.



TPM CONN.



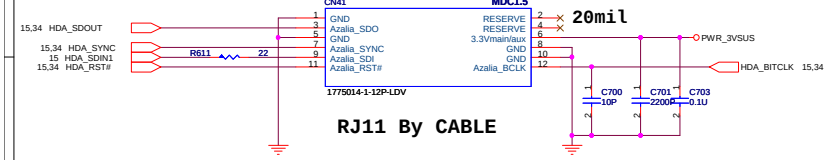
BAY CONN/ODD CONN



PWR_BATT2 39,43

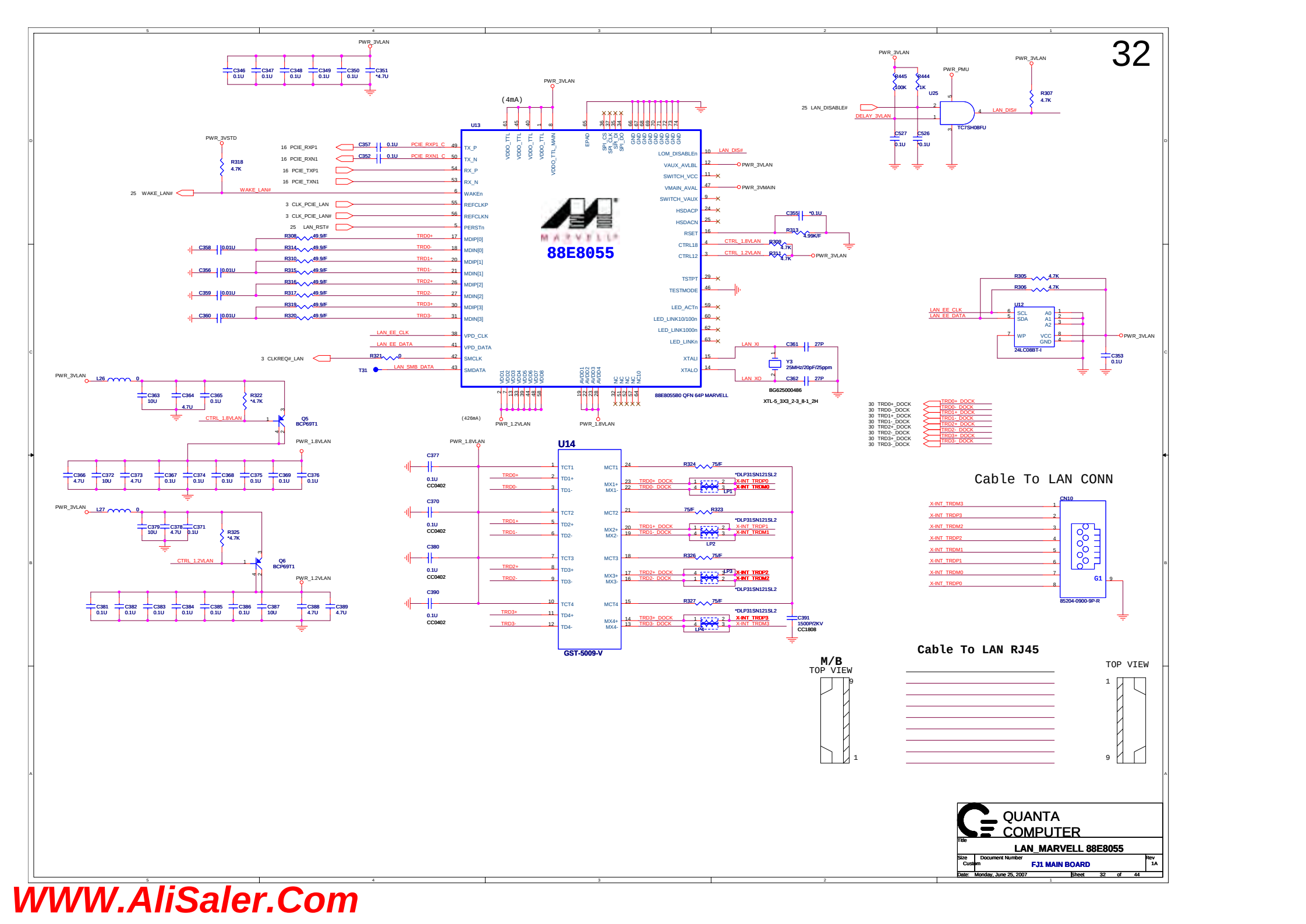
PWR_5VBAY 38

MDC CONN

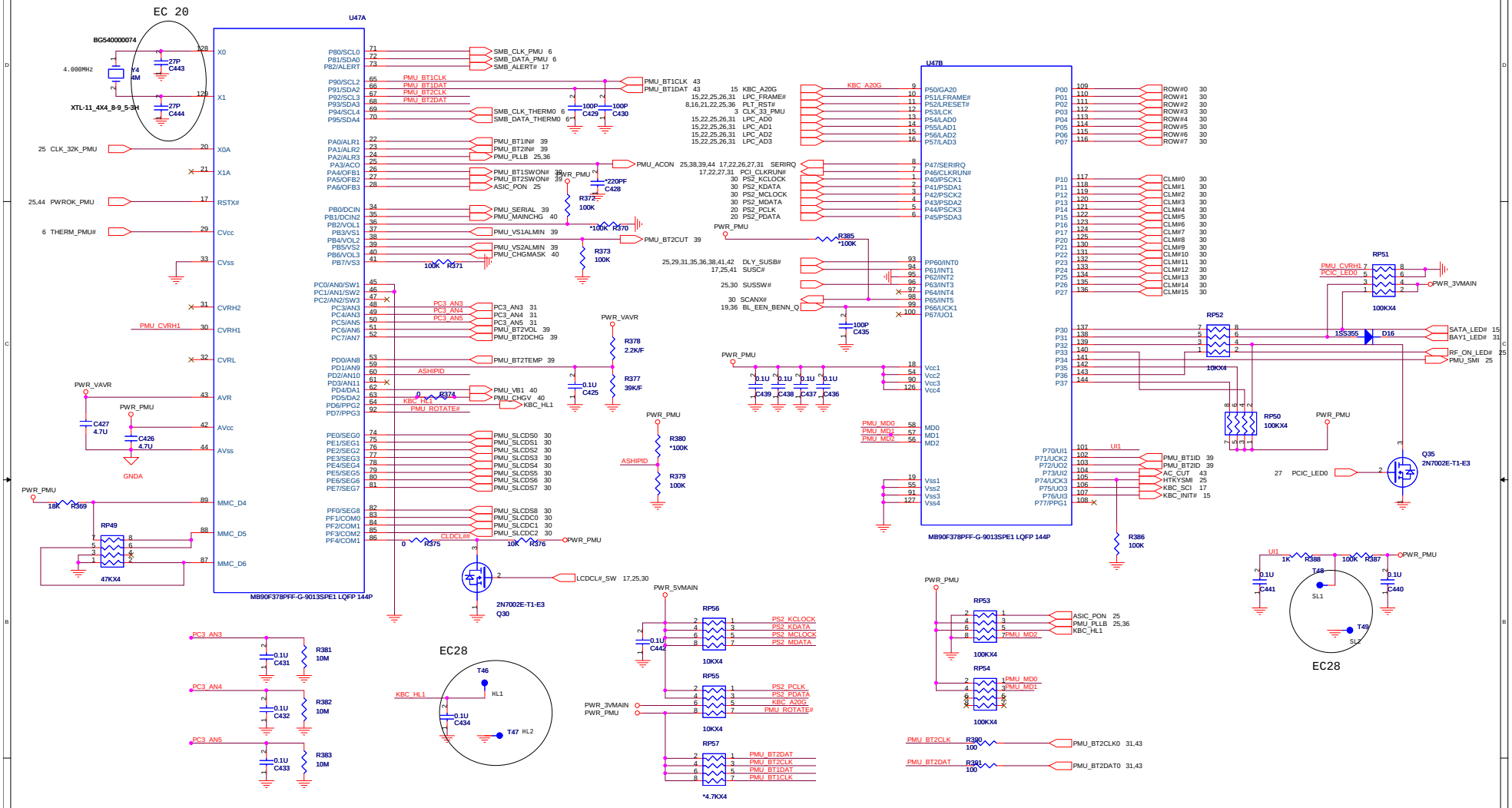


RJ11 By CABLE

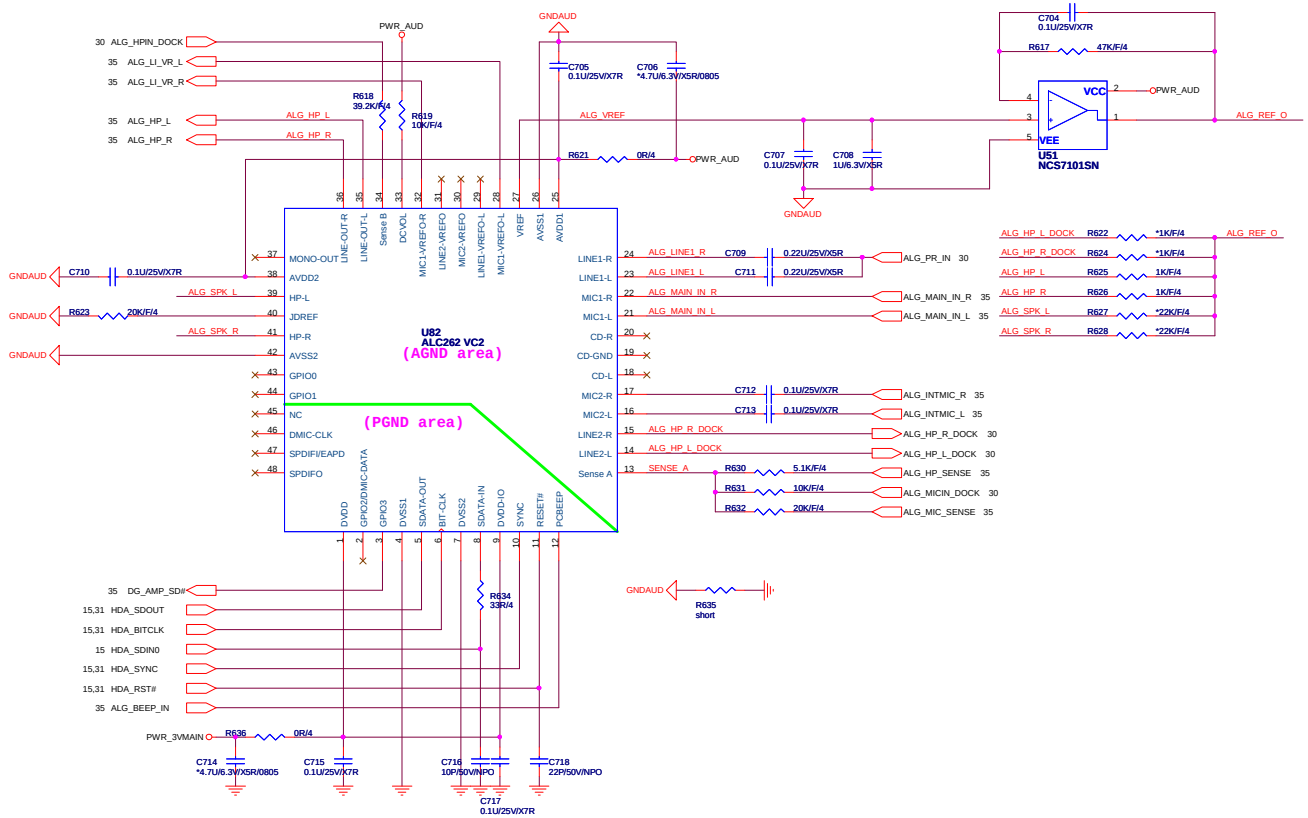
QUANTA COMPUTER		
Title: SATA/MDC/TPM/GSENSOR		
Size: Custom	Document Number: FJ1 MAIN BOARD	Rev: 1A
Date: Monday, June 25, 2007	Sheet 31 of 44	



Title	LAN_MARVELL 88E8055
Size	Custom
Document Number	FJ1 MAIN BOARD
Rev	1A
Date:	Monday, June 25, 2007
Sheet	32 of 44



QUANTA COMPUTER			
Title	EC COntroller		
Size: Custom	Document Number: FJ1 MAIN BOARD		Rev: 1A
Date: Monday, June 25, 2007	Sheet 33 of 44		



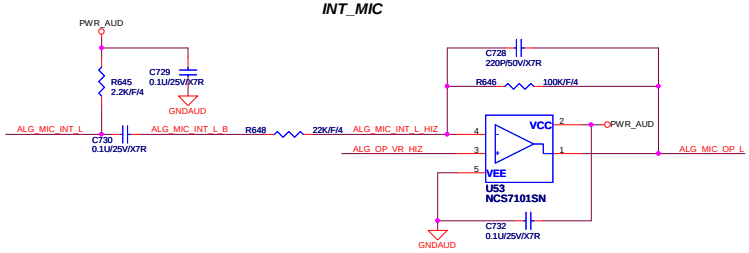
QUANTA COMPUTER

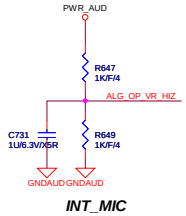
Title: AUDIO AL262 1/2

Size: Custom | Document Number: FJ1 MAIN BOARD | Rev: 1A

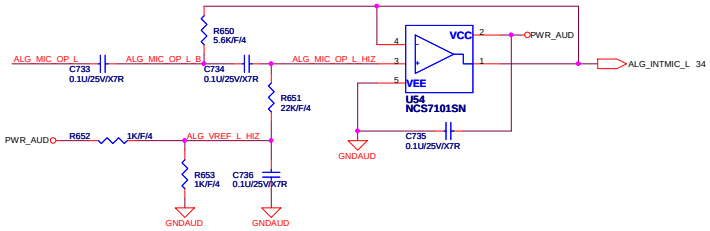
Date: Monday, June 25, 2007 | Sheet 34 of 44

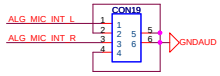
INT_MIC



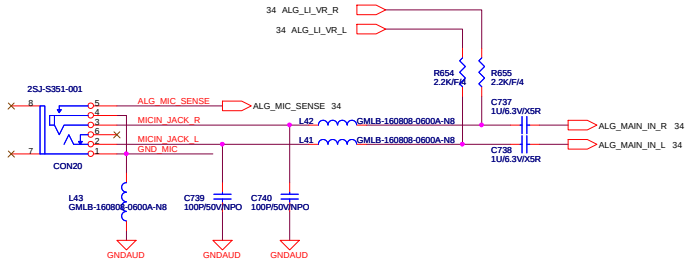


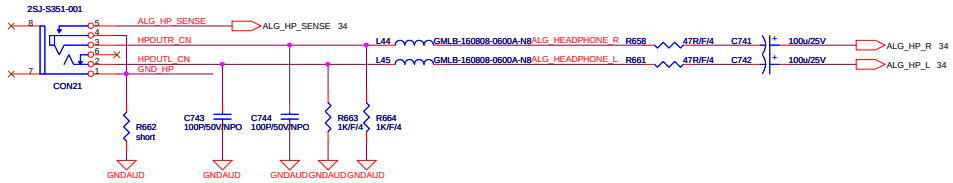
INT_MIC

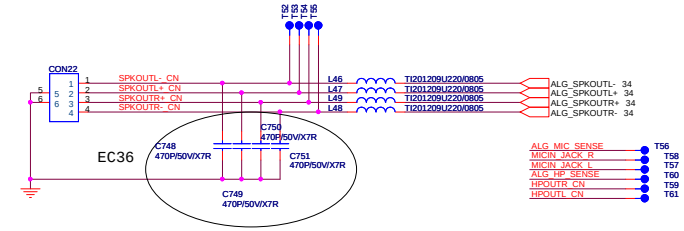




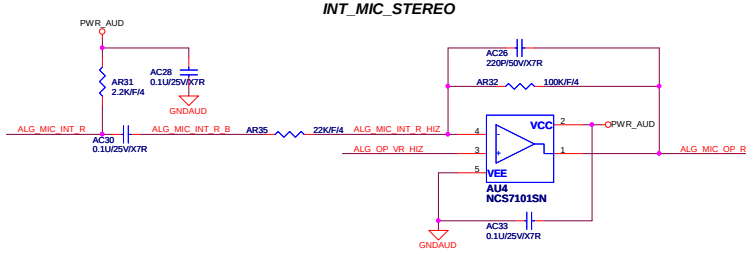
INT_MIC_CN

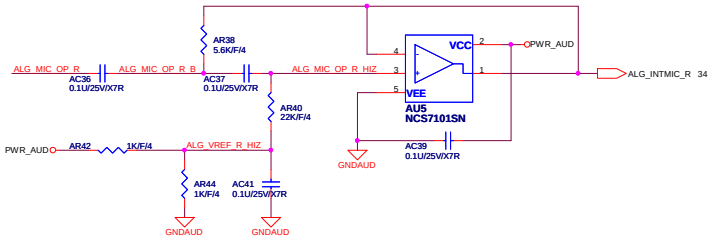


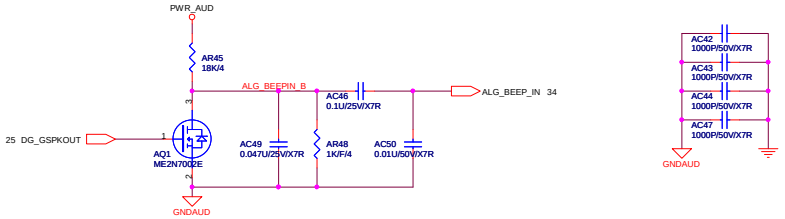


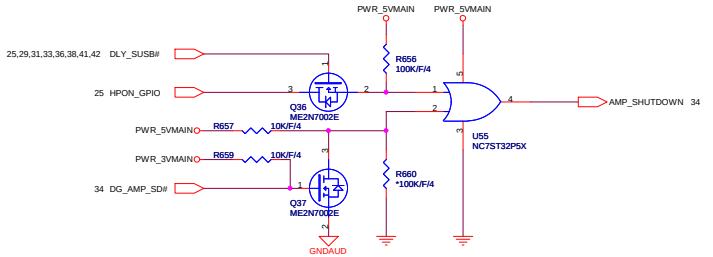


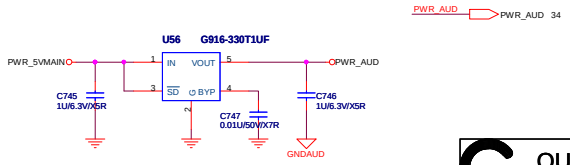
INT_MIC_STEREO







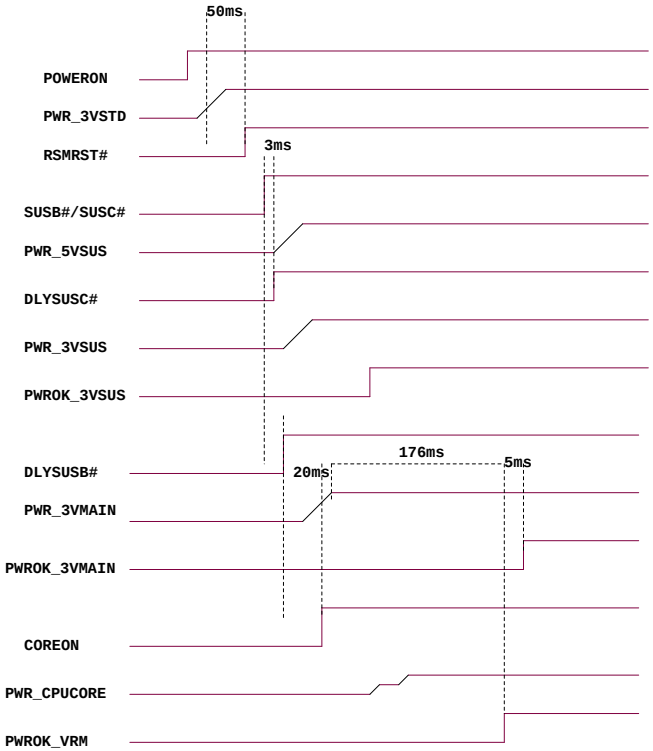


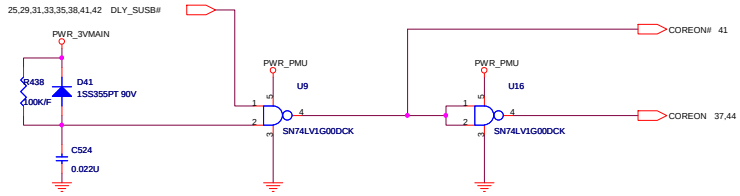


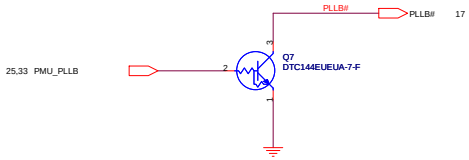
QUANTA COMPUTER

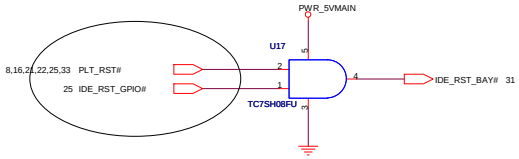
Title	AUDIO AL262 2/2	
Size: Custom	Document Number: FJ1 MAIN BOARD	Rev: 1A
Date: Monday, June 25, 2007	Sheet 35 of 44	

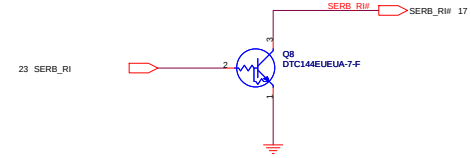
POWER SEQUENCE

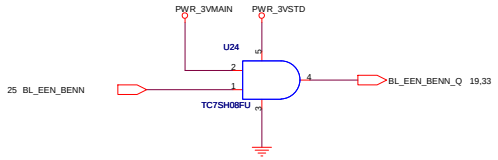


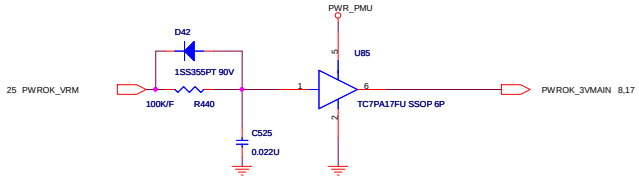


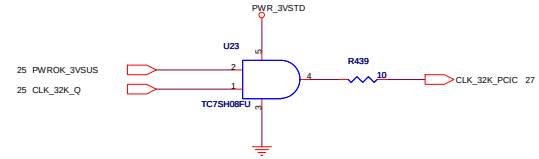




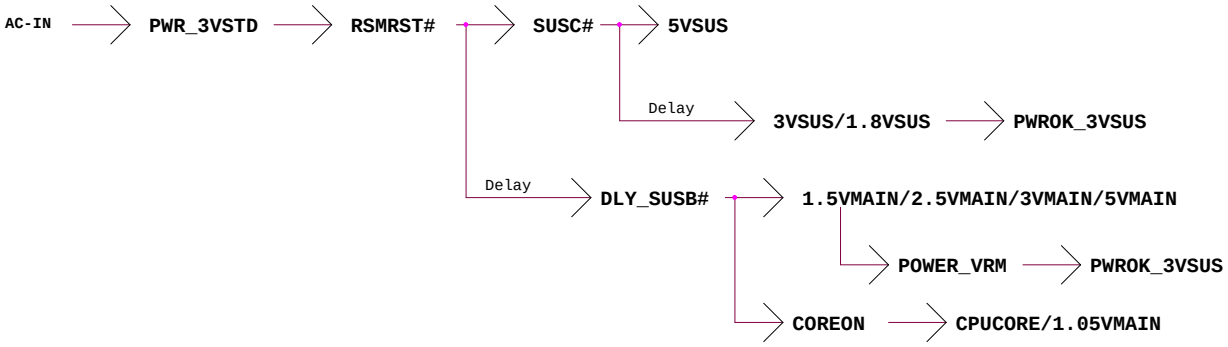








POWER_Control_Tree



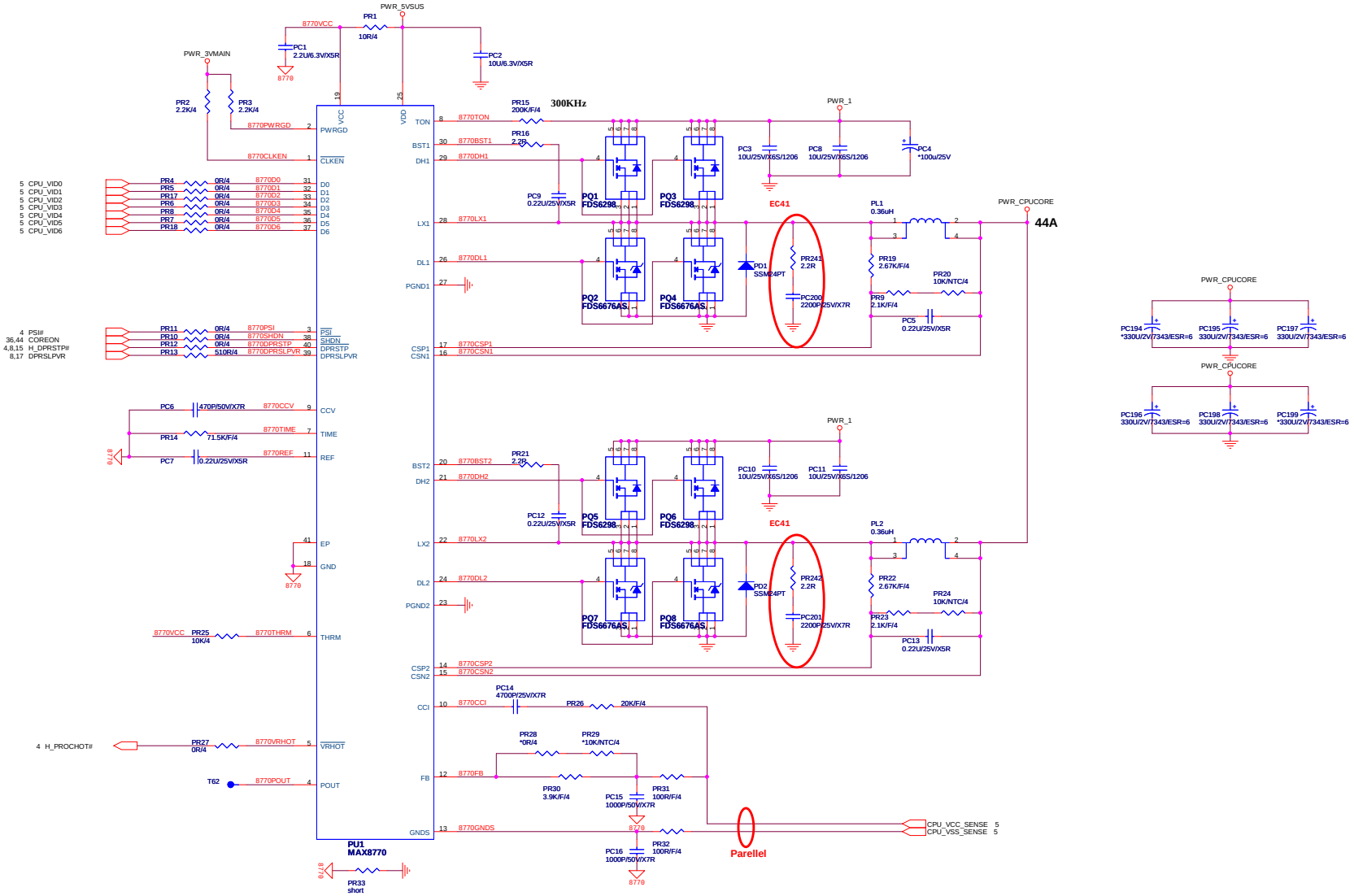
QUANTA COMPUTER

Title: RESET

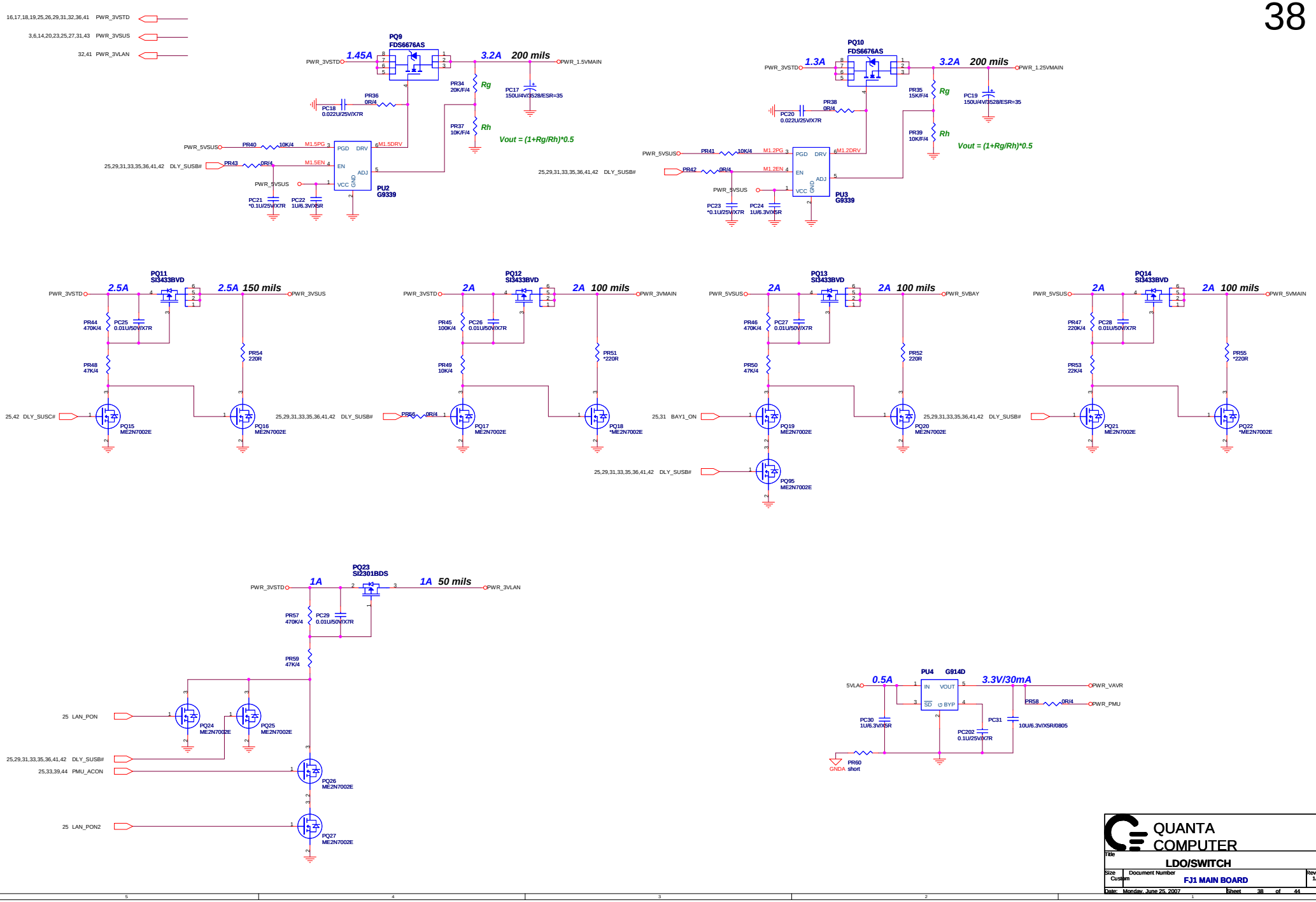
Size: Custom | Document Number: FJ1 MAIN BOARD | Rev: 1A

Date: Monday, June 25, 2007 | Sheet 36 of 44

CPU CORE



QUANTA COMPUTER		
Title: CPU CORE POWER		
Size: Custom	Document Number: FJ1 MAIN BOARD	Rev: 1A
Date: Monday, June 25, 2007	Sheet 37 of 44	

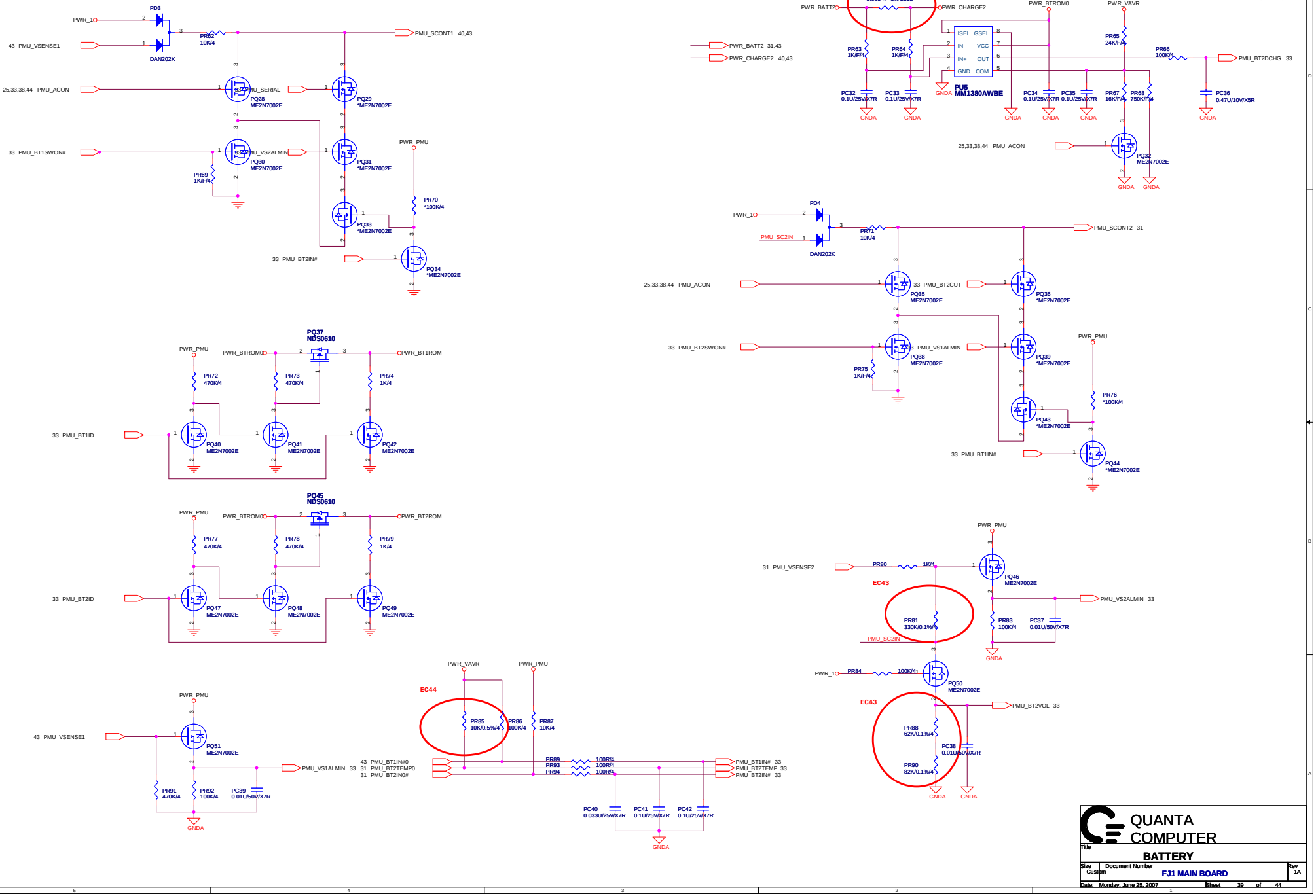


QUANTA COMPUTER

Title: LDO/SWITCH

Size: Custom | Document Number: FJ1 MAIN BOARD | Rev: 1A

Date: Monday, June 25, 2007 | Sheet 38 of 44

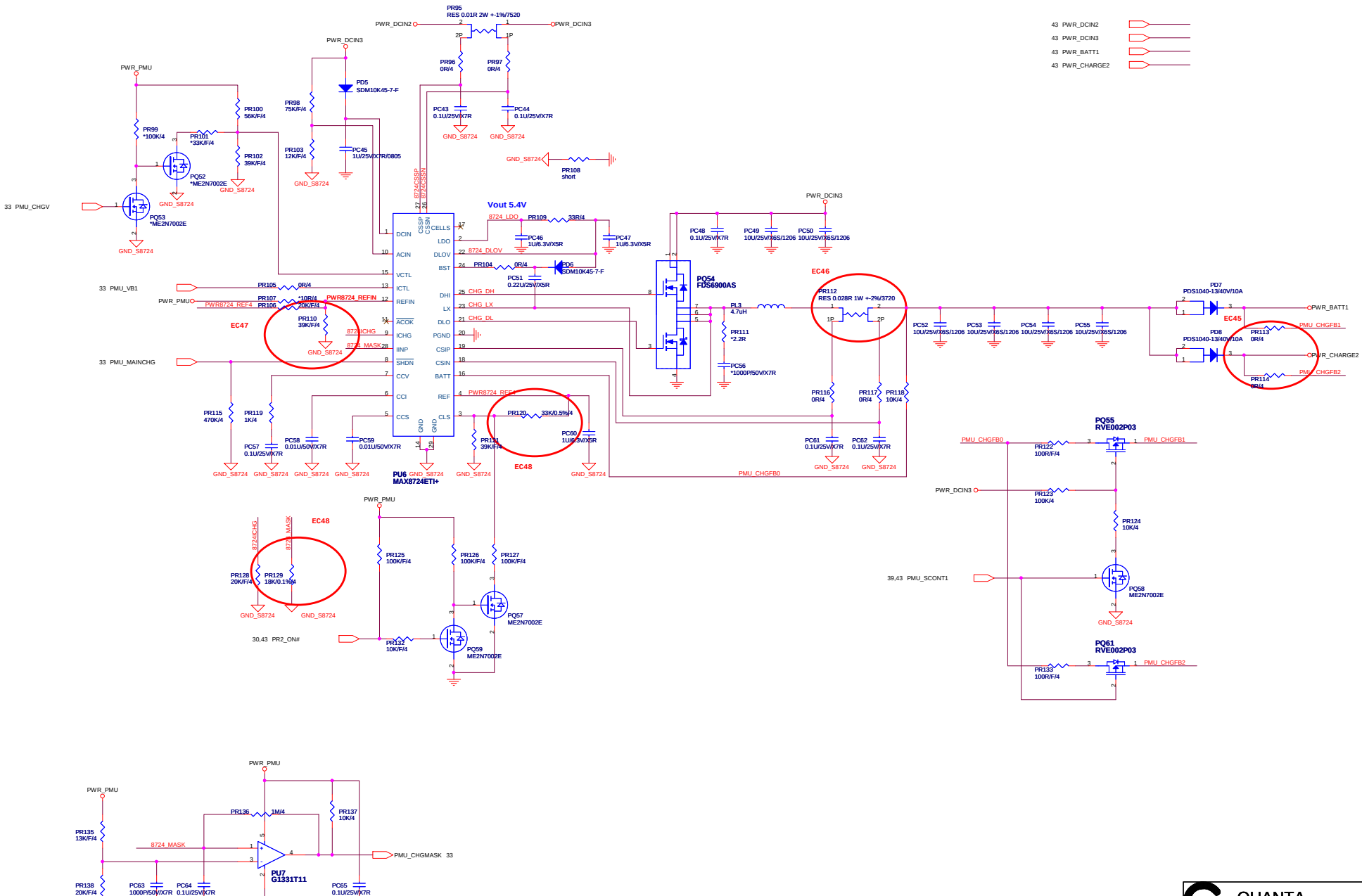


QUANTA COMPUTER

Title: BATTERY

Size: Custom | Document Number: FJ1 MAIN BOARD | Rev: 1A

Date: Monday, June 25, 2007 | Sheet 39 of 44

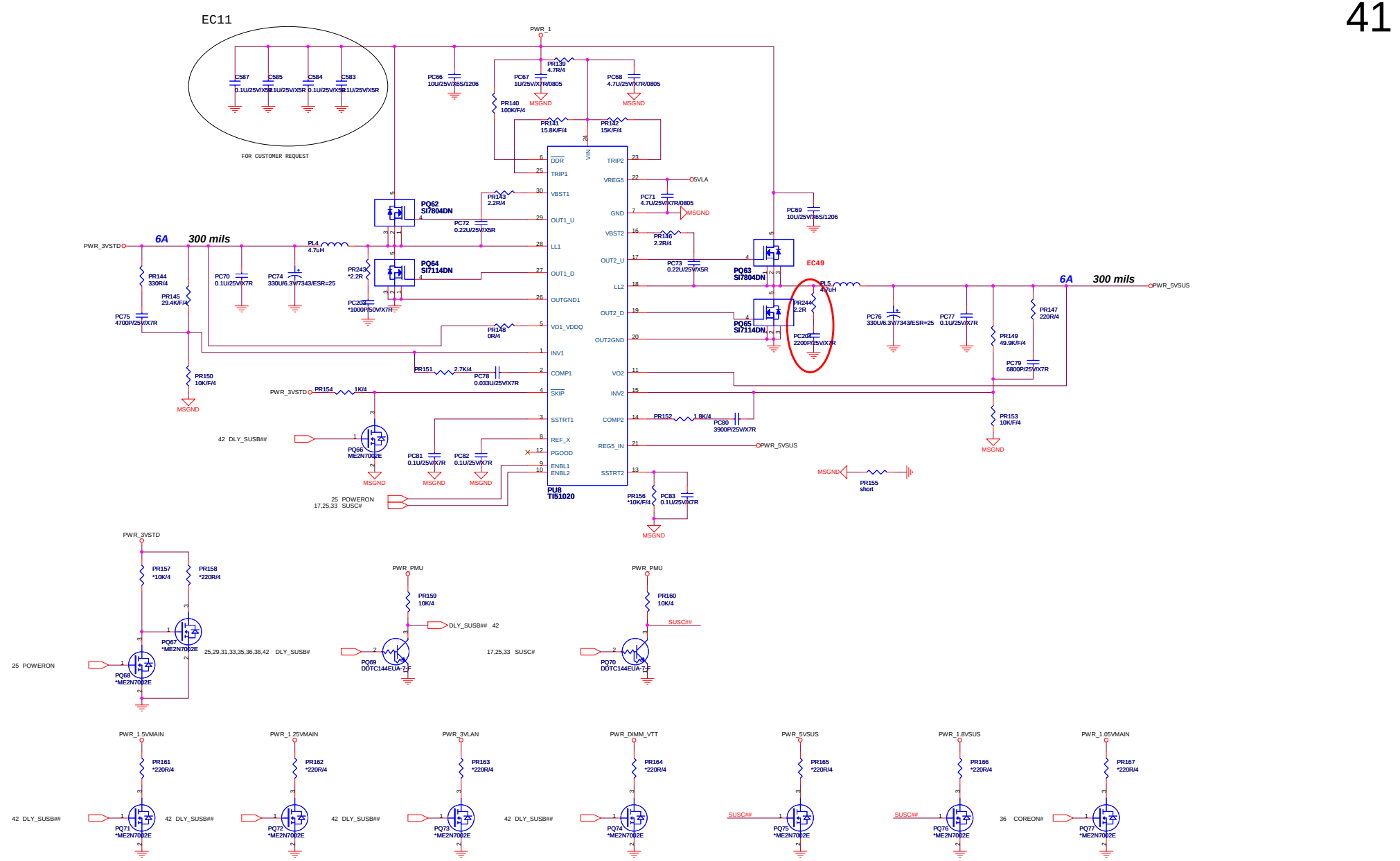


QUANTA COMPUTER

Title: CHARGER

Size: Custom | Document Number: FJ1 MAIN BOARD | Rev: 1A

Date: Monday, June 25, 2007 | Sheet 40 of 44

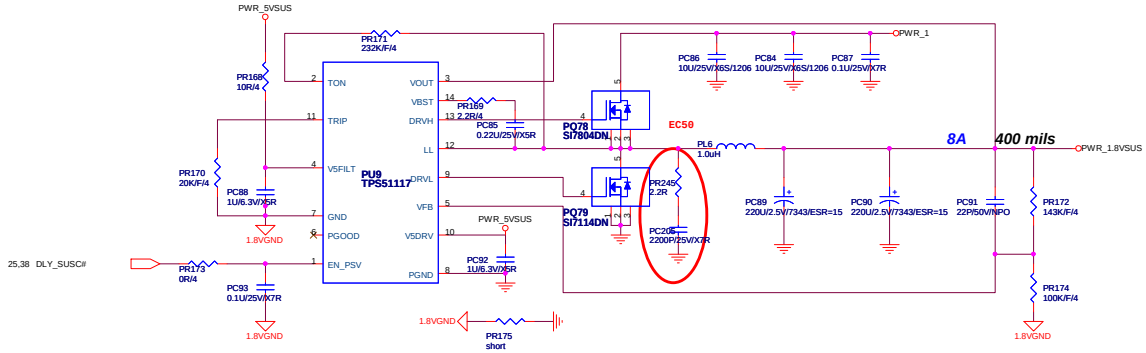


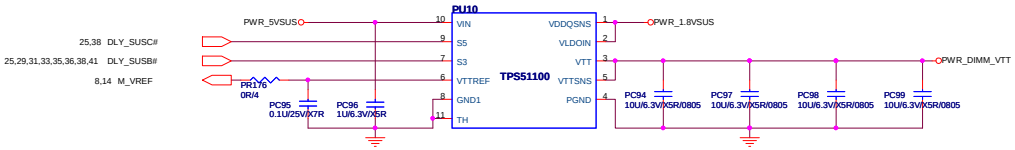
QUANTA COMPUTER

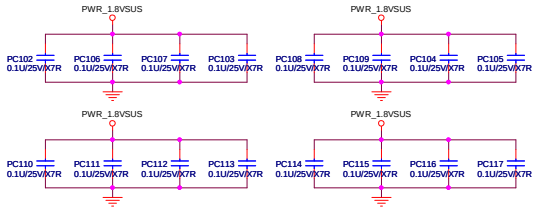
Title: 5VPMU/5VSTD/3VPMU/3VSTD

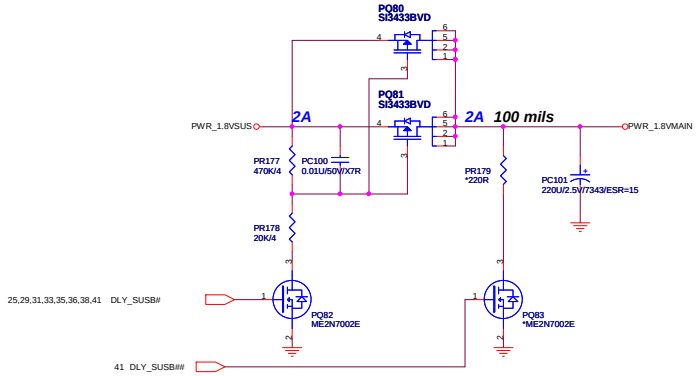
Size: Custom | Document Number: FJ1 MAIN BOARD | Rev: 1A

Date: Monday, June 25, 2007 | Sheet 41 of 44







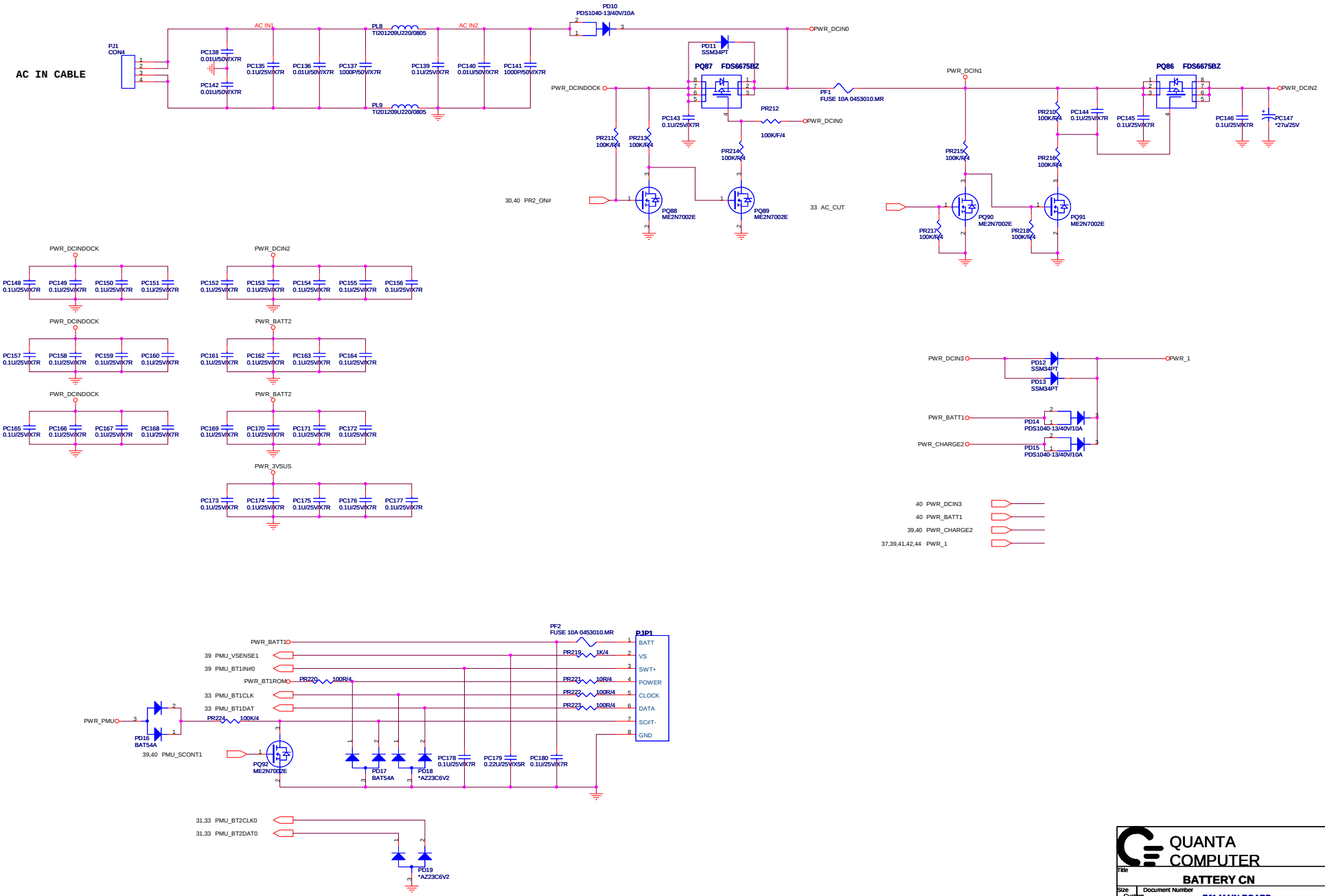


QUANTA COMPUTER

Title: 1.8V_DIMM

Size: Custom | Document Number: FJ1 MAIN BOARD | Rev: 1A

Date: Monday, June 25, 2007 | Sheet 42 of 44

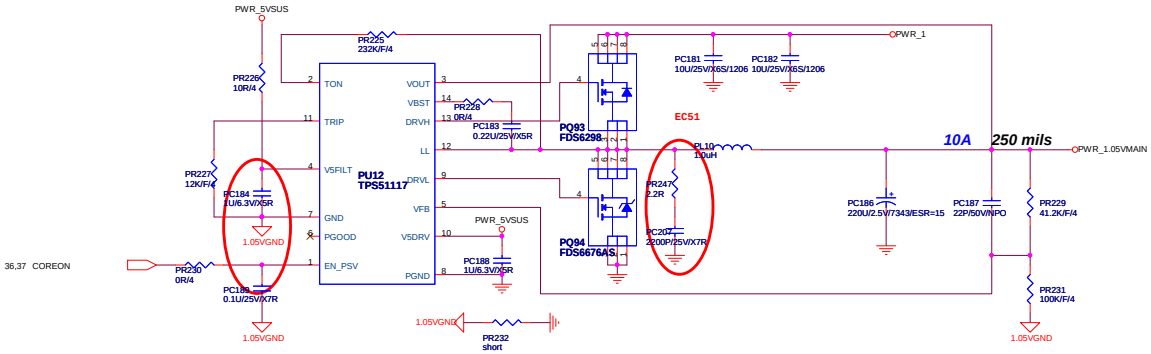


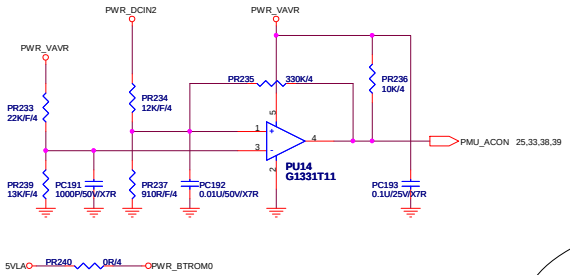
QUANTA COMPUTER

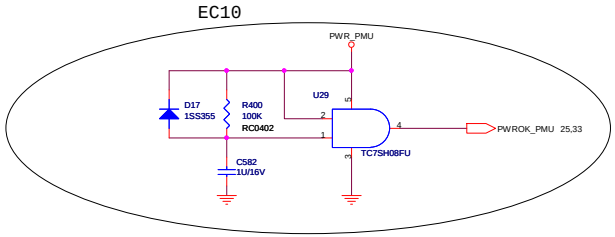
Title: BATTERY CN

Size: Custom | Document Number: FJ1 MAIN BOARD | Rev: 1A

Date: Monday, June 25, 2007 | Sheet 43 of 44







QUANTA COMPUTER

Title: 1.05V/ETC0		
Size: Custom	Document Number: FJ1 MAIN BOARD	Rev: 1A
Date: Monday, June 25, 2007	Sheet 44 of 44	

EC1-Page 03--Delete the R24,R25,R31 ,R32 ,for layout space.

EC2-Page 19--change HSYNC1 VSYNC1 NET Name for correct net.

EC3-Page 19--change CN5 LVDS pin define for macth footprint.

EC4-Page 21--change NET Name to SDVO_AVCC for correct link.

EC5-Page 24--change CON13 NET for reverse type

EC6-Page 25--change 32.768K circuit for material shortage and cost issue.

EC7-Page 30--SWAP USB20_P5+ USB20_P5- ,CN9 #96,97 net for correct layout.

EC8-Page 11--Add two 0805 Capacitor on 220uf/330uf co-layout for layout issue and cost issue.
C36,C85,C89,C105,C116,C126,C127,C133,C151,C155,C144,C207,C217,C251,C415

EC10-Page 41--change PWROK_PMU reset signal circuit for material shortage and cost issue.

EC11-Page 41--ADD C583,C584,C585,C587 on PWR_1 to GND for customer layout request.

EC12-Page 11--ADD R216 for reserve the layout pad.

EC13-Page 18--Change from R226 to D21 to avoid the leakage issue.

EC14-Page 27--Add C520 for EMI request.

EC15-Page 31--Delete the CN39 GND for layout issue.

EC17-Page 26--Add C589 0.1uf for Antana team request.

EC18-Page 19--Change R239,R240,R241 to 68ohm bead for EMI request.

EC19-Page 15--Change C223,C225 from 18pf to 15pf to match the frequency stability.

EC20-Page 33--Change C443,C444 to 27pf to match the frequency stability.

EC21-Page 26--Change R449 from 10K to 47Kohm to solve the bluetooth issue.

EC22-Page 26--Add the R467,R468 PAD for debug.

EC23-Page 6--Remove the R454,R455 for Thermal sensor issue.

EC24-Page 24--Add LP5,LP7 commond chock for EMI request.

EC25-Page 30--Add C590,C591,C592,C593 for EMI request.

EC26-Page 21--Change 300ohm to 100ohm and 0.1uf to 0 ohm for EMI request.

EC27-Page 22--Add C594,C595 5pf for EMI request.

EC28-Page 15,25,33--Delete R466,G2,R384,R389 reserve pad.

EC29-Page 30--Add LP6 commond chock for EMI request.

EC30-Page 17--C242,C243 5PF change to populate for EMI solution.

EC31-Page6 --Change Q21,R360 ,R368 to SI2301BDS,470K,47K to increase current.

EC32-Page26 --Reserve the LP8,LP9,LP11 PAD for Antenna team request.

EC33-Page19 --Delete R247 for EMI request.

EC34-Page15 --Change the R142 to 33ohm to solve signal quarlity issue.

EC35-Page15 --Add C229,C230,C231 10pf in BOM for EMI solution.

EC36-Page35 --Add C748,C749,C750,C751 470pf in BOM for EMI solution.

EC37-Page30 --Change LCD cover close curcuit (Add R469,R466,R465,C596,Q34,U30)

EC38-Page20 --Change CN47 net for machenical design issue.

EC39-Page26 --Change CN44 net for machenical design issue.

EC40-Page34 --Change C723 from 4.7uF to 2.2uF for mute issue.

EC41-Page37 --Add PR242, PC201, PR241, PC200 for EMI issue.

EC42-Page39 --Change PR61 from 10mohm to 5mohm for 2nd battrey current sense.

EC43-Page39 --Change PR81 from 330Kohm 5% to 330Kohm 0.1% and PR88 62Kohm 1% to 62Kohm 0.1% and PR90 82K 1% to 82Kohm 0.1% for precisely battery voltage sense.

EC44-Page39 --Change PR85 from 470Kohm 1% to 10Kohm 0.5% for 2nd battrey detect issue.

EC45-Page40 --Change PR113 and PR114 from 10Kohm 5% to 0ohm 5% for battrey charging voltage sense.

EC46-Page40 --Change PR112 from 25mohm to 28mohm due to Quanta side don't have such material (27mohm).

EC47-Page40 --Change PR110 from 49.9Kohm to 39Kohm due to current sense resistor change.

EC48-Page40 --Change PR120 from 33Kohm 1% to 33Kohm 0.5% and PR129 from 18K 1% to 18K 0.5%.

EC49-Page41 --Add PR244 and PC204 for EMI issue.

EC50-Page42 --Add PR245 and PC205 for EMI issue.

EC51-Page44 --Add PR247 and PC207 for EMI issue.

Title: <Title>		
Size: C	Document Number: <Doc>	Rev: 1A
Date: Friday, June 22, 2007	Sheet 45 of 45	