Compal Confidential

Diner Braswell M/B LA-D704P Schematics Document

Intel Braswell + ATI R16M-M1-30/70

2015/12/12

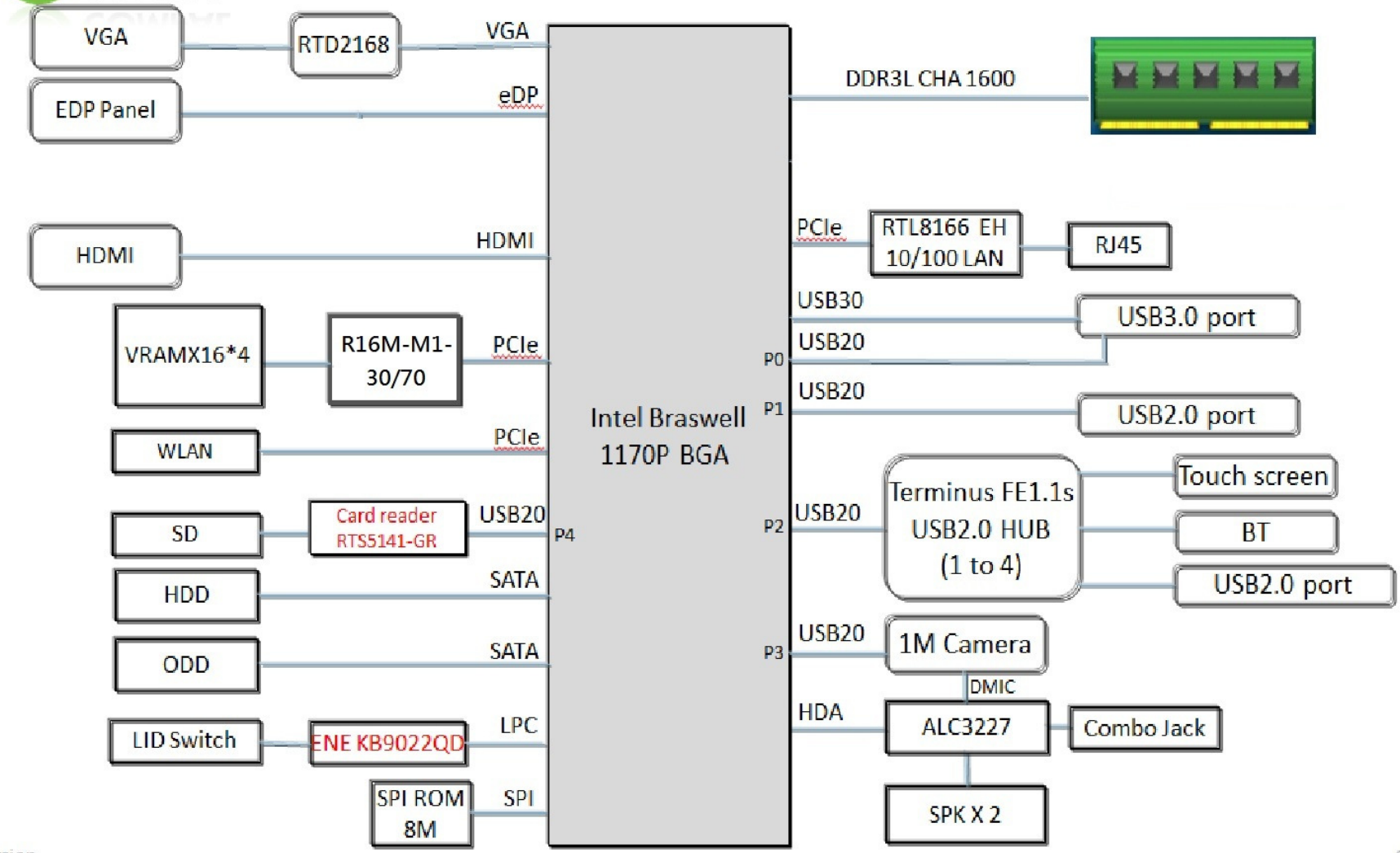
Project Code : BDL50

Rev. 0.3 PV

Security Classification	Compal Secret Data		
Issued Date	2015/10/05	Deciphered Date	2015/10/05

Compal Electronics, Inc.			
Title: *Cover Page*			
Size: B	Document Number		Rev: 1.0
Date: Thursday, January 07, 2016	Sheet 1 of 50		

Intel Braswell 15" Hardware Block Diagram



Sub-borad

page34
CR+USB/B

page34
PWR BTN/B

page36
TP BTN/B

page24
HDD or SSD/B

page24
ODD/B

Security Classification	Compal Secret Data		
Issued Date	2014/07/07	Deciphered Date	2015/07/07

Compal Electronics, Inc.			
Title	Block Diagrams		
Size	Document Number		Rev
Custom			1.0
Date:	Thursday, January 07, 2016	Sheet	2 of 50

Voltage Rails

Power Plane	Description	S0	S3	S4/S5
VIN	19V Adapter power supply	ON	ON	ON
BATT+	12V Battery power supply	ON	ON	ON
B+	AC or battery power rail for power circuit. (19V/12V)	ON	ON	ON
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.0VALW	+1.0v Always power rail	ON	ON	ON
+1.2VALW	+1.2v Always power rail	ON	ON	ON
+1.8VALW	+1.8v Always power rail	ON	ON	ON
+3VALW	+3.3v Always power rail	ON	ON	ON
+5VALW	+5.0v Always power rail	ON	ON	ON
+1.35V	+1.35V power rail for DDR3L	ON	ON	OFF
+SOC_VCC	Core voltage for SOC	ON	OFF	OFF
+SOC_VNN	GFX voltage for SOC	ON	OFF	OFF
+0.675VS	+0.675V power rail for DDR3L Terminator	ON	OFF	OFF
+1.0VS	+1.0v system power rail	ON	OFF	OFF
+1.05VS	+1.05v system power rail	ON	OFF	OFF
+1.35VS	+1.35v system power rail	ON	OFF	OFF
+1.5VS	+1.5v system power rail	ON	OFF	OFF
+1.8VS	+1.8v system power rail	ON	OFF	OFF
+3VS	+3.3v system power rail	ON	OFF	OFF
+5VS	+5.0v system power rail	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

<PCI-E,SATA,USB3.0>

Lane#	USB3.0	DESTINATION	
		UMA	DIS
0		USB3.0	USB3.0
1			

Lane#	SATA	DESTINATION	
		UMA	DIS
0		HDD	HDD
1		ODD	ODD

Lane#	PCIE	DESTINATION	
		UMA	DIS
0			GPU
1			GPU
2		WLAN	WLAN
3		LAN	LAN

<USB2.0 port>

USB2.0 port	UMA	Dis
0	USB 3.0 (MB)	USB 3.0 (MB)
1	USB 2.0 (MB)	USB 2.0 (MB)
2	Camera	Camera
3	Card Reader	Card Reader
4	USB 2.0 Hub	USB 2.0 Hub

<USB2.0 Hub>

USB2.0 port	UMA	Dis
0	Touch Screen	Touch Screen
1	USB 2.0 (SB)	USB 2.0 (SB)
2	BT	BT
3		
4		

EC SM Bus1 address

Device	Address
Charger	
Battery	

EC SM Bus2 address

CPU Thermal Sensor	4C	UC3
ATI GPU EXO Pro		U666

EC SM Bus3 address

GPU Thermal Sensor	4C	UV1

SOC SM Bus address

Device	Address	
ChannelA	A0	DDR DIMM1
ChannelB	A2	DDR DIMM2
Touch Pad		

BOM Structure Table

BOM Config	Description
@	Unpop
CONN@	Connector Part Control by ME
EMI@	EMI pop component
@EMI@	EMI unpop component
ESD@	ESD pop component
@ESD@	ESD unpop component
PX@	For Discrete Sku
8166@	10/100 LAN
8151@	Giga LAN
UMA@	For UMA Sku
NAT@	EC Non Auto Load Code
AUTO@	EC Auto Load Code
TPM@	CPU to EC LPC use 3.3V level
NTPM@	CPU to EC LPC use 1.8V level
GCLK@	Pop Green Clock
GCUMA@	Pop Green Clock UMA
GCDIS@	Pop Green Clock DIS
XTAL@	For XTAL
TS@	Pop Touch Screen component
R30@	For R16M-M1-30 GPU
R70@	For R16M-M1-70 GPU
6U@	For 6U@ (Add CRT Component)
IND@	Pop for India Sku

DAX

PCB
Part Number = DA6001JC000
PCB LA-C811P REV0 M/B 4

ZZZ1

HDMI
Part Number = RO0000003HM
PCB 102 LA-B151P REV0 M/B 3
45@

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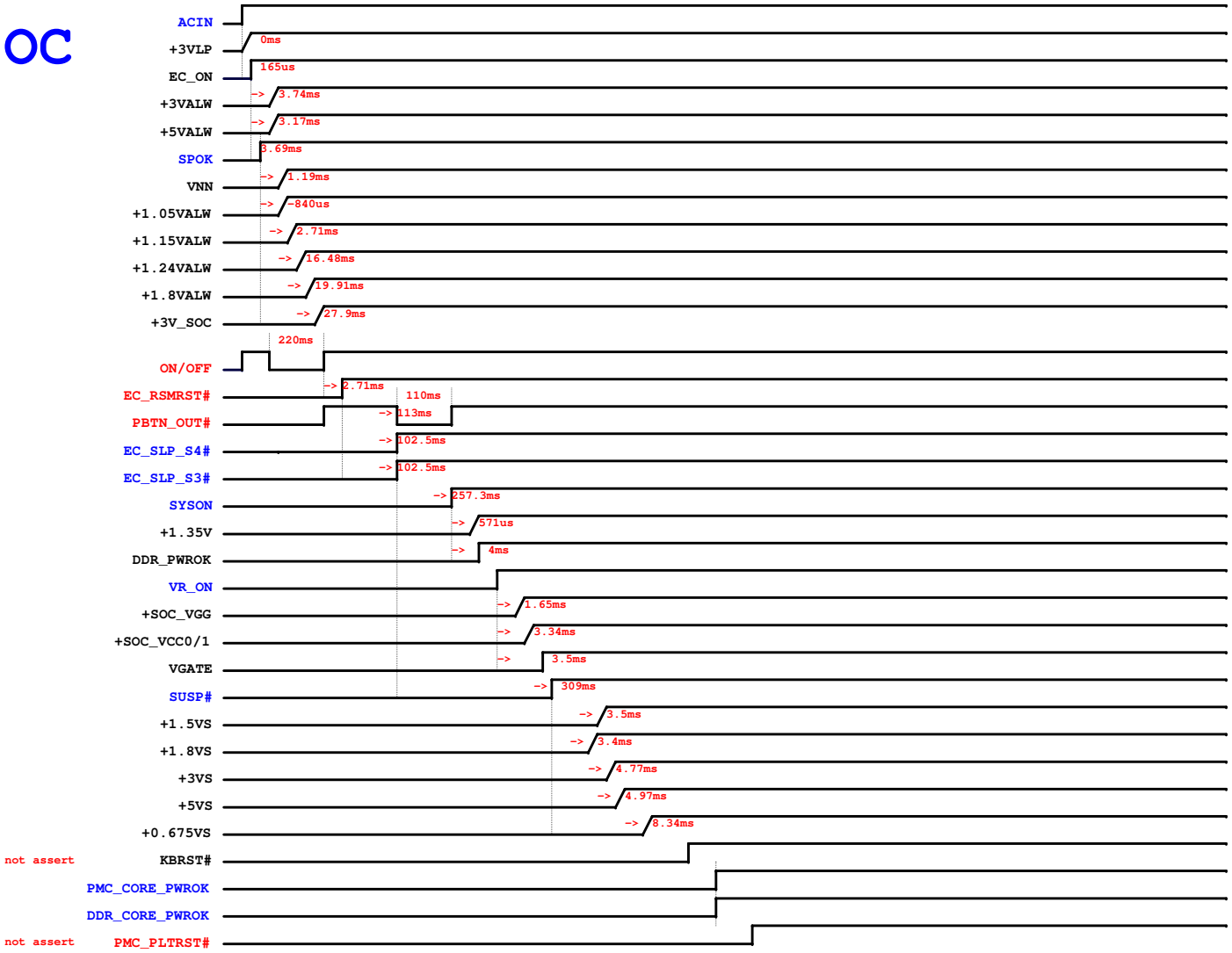
Title: Notes List

Size: Custom | Document Number | Rev: 1.0

Date: Thursday, January 07, 2016 | Sheet 3 of 50

G3->S0

SOC



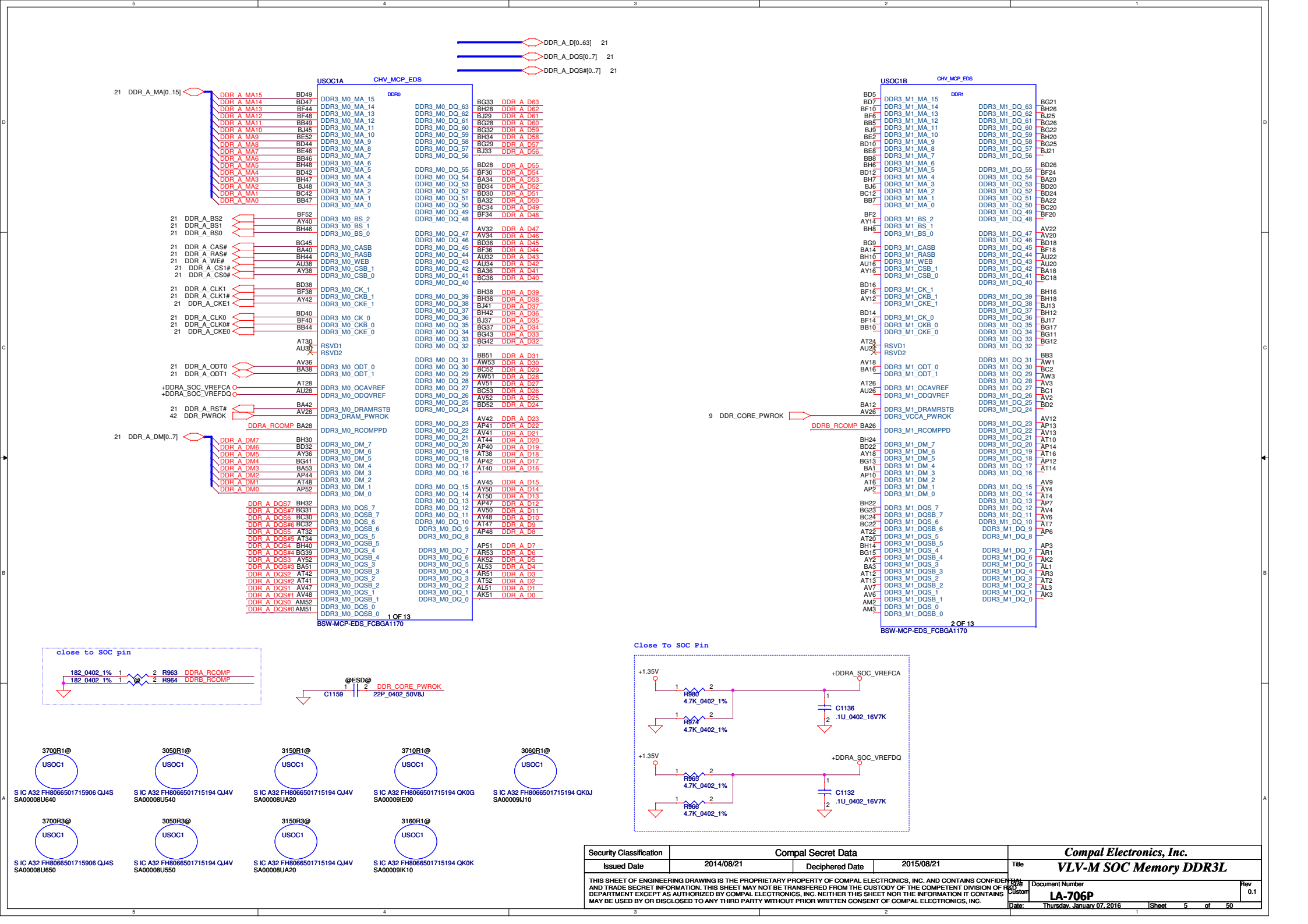
Security Classification	Compal Secret Data		
Issued Date	2014/08/21	Deciphered Date	2015/08/21

Compal Electronics, Inc.

Title: Power Sequence

Size	Document Number	Rev
C	LA-706P	0.1

Date: Thursday, January 07, 2016 | Sheet 4 of 50

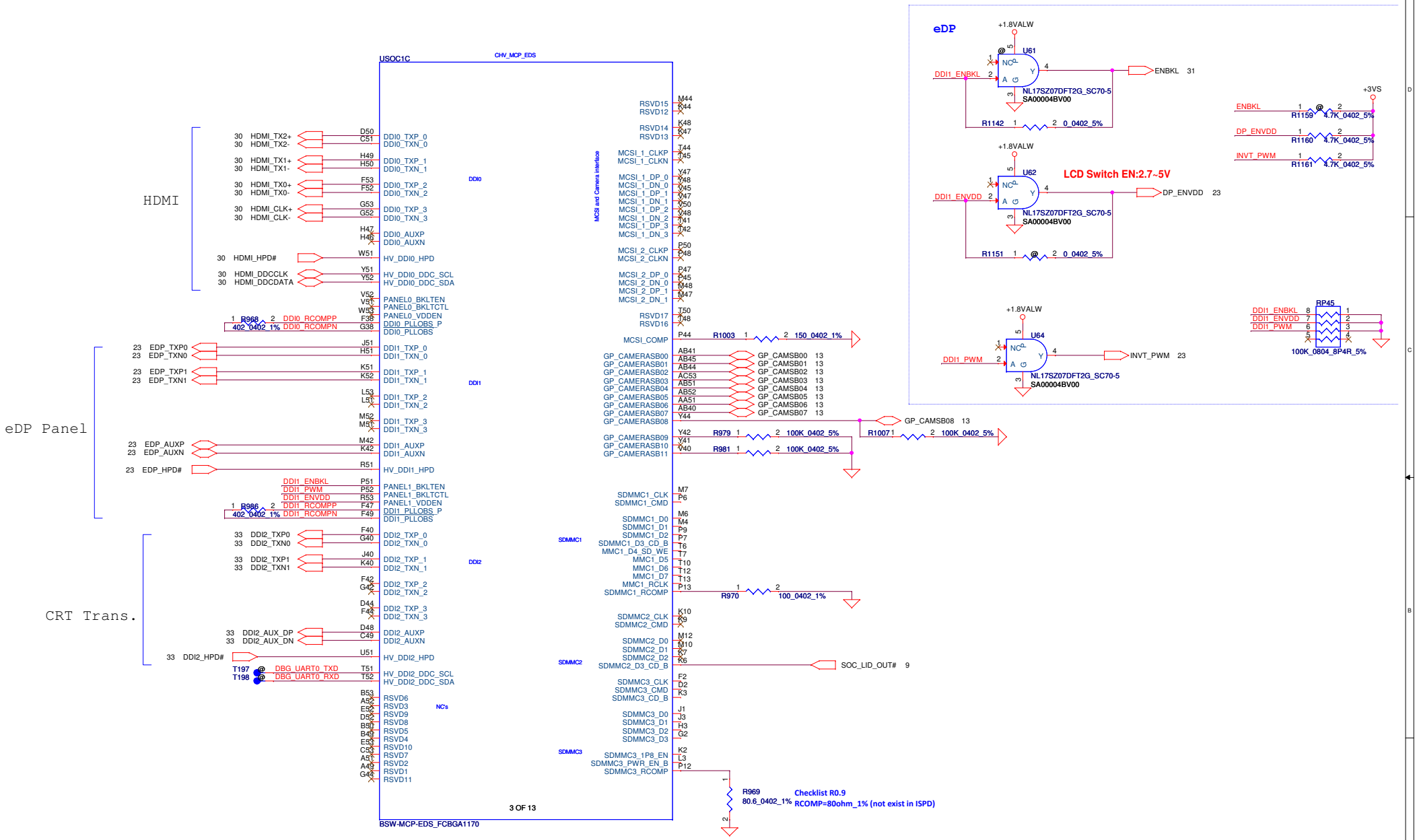


Security Classification	Compal Secret Data		
Issued Date	2014/08/21	Deciphered Date	2015/08/21

Compal Electronics, Inc.

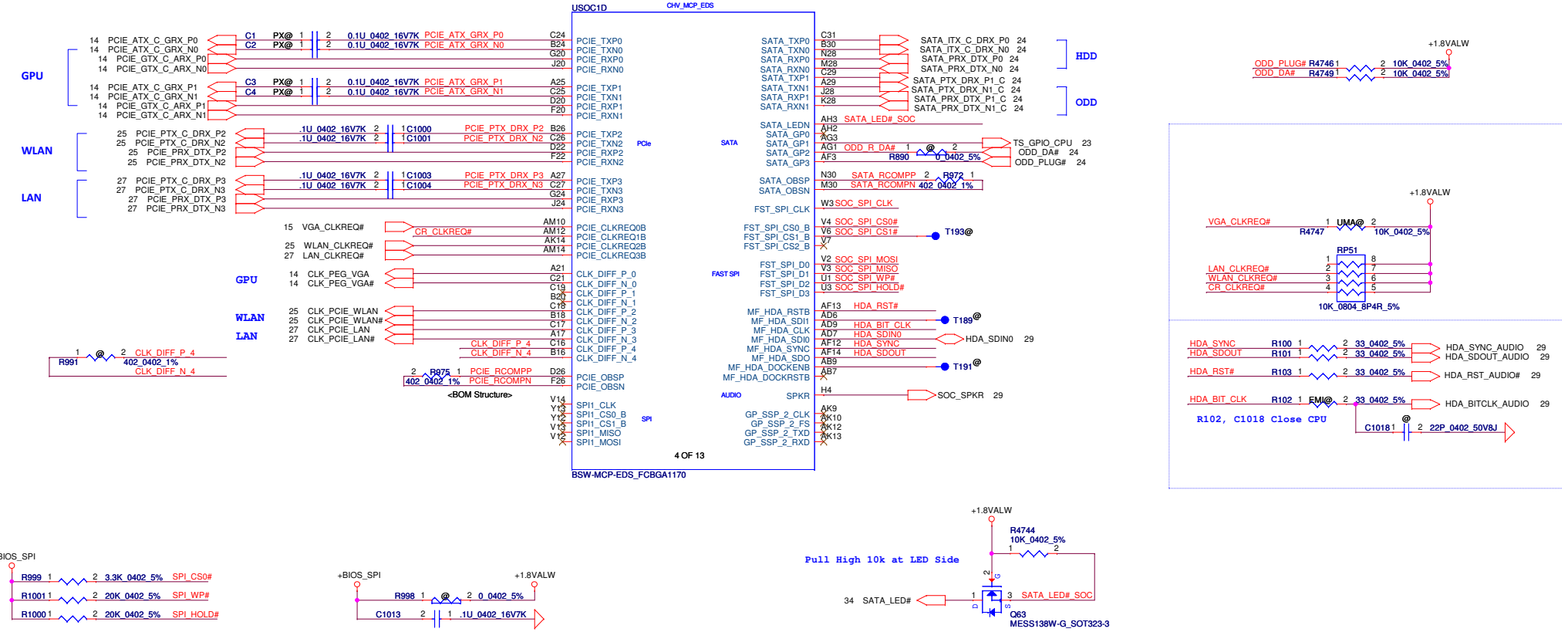
Title: VLV-M SOC Memory DDR3L

Size: Custom	Document Number: LA-706P		Rev: 0.1
Date: Thursday, January 07, 2016	Sheet 5 of 50		



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/08/21	Deciphered Date 2015/08/21	Title VLV-M SOC Display

Size	Document Number	Rev
Custom	LA-706P	0.1
Date: Thursday, January 07, 2016	Sheet 6 of 50	



EC(For Auto Load)

SPI ROM (8MByte) 1.8V

U56 change to SA00006ZV10 for Quad-I/O

R2582/R2588~90 Close U56

RP48 Close U56

CPU ROM CPU SPI ROM EC

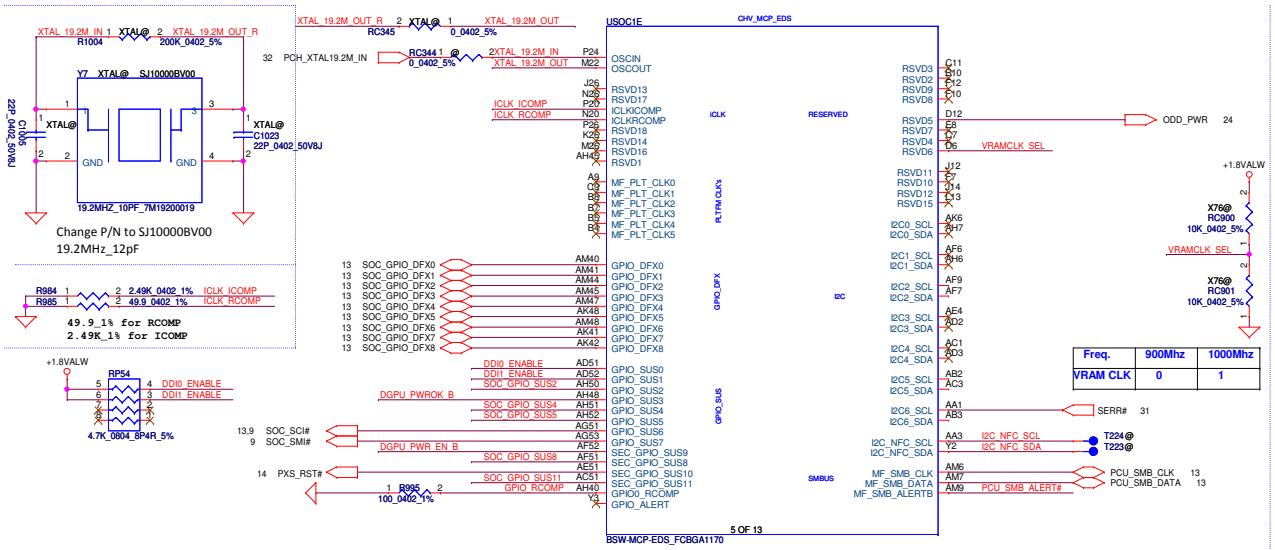
Security Classification	Compal Secret Data		
Issued Date	2014/08/21	Deciphered Date	2015/08/21

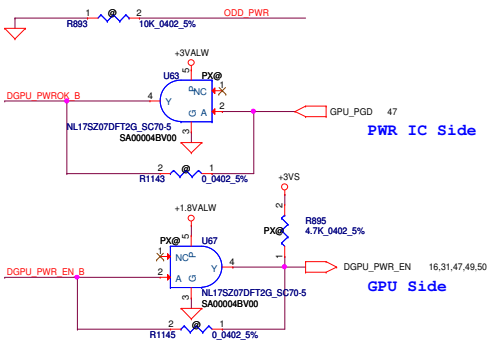
Compal Electronics, Inc.

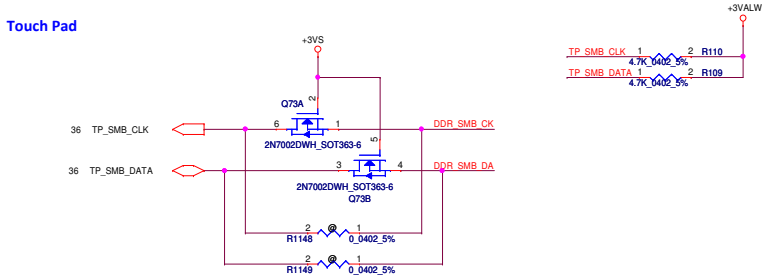
Title: VLV-M SOC SATA/PCI-E/HDA

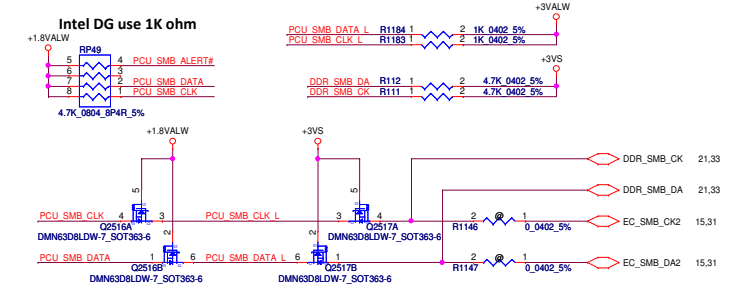
Size: Custom | Document Number: LA-706P | Rev: 0.1

Date: Thursday, January 07, 2016 | Sheet 7 of 50



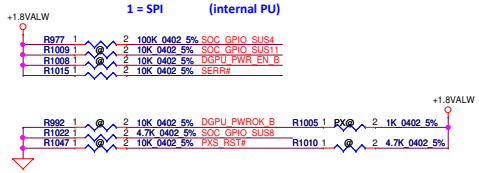


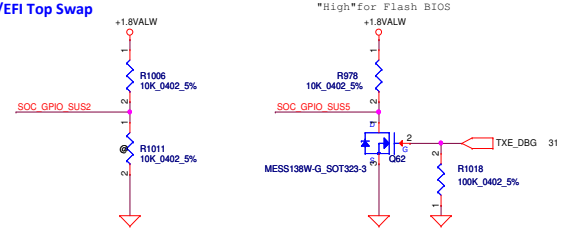


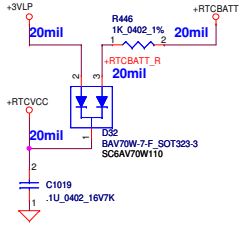


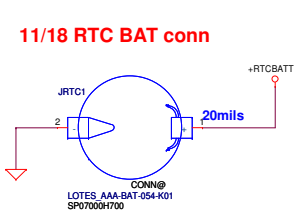
Q2516 change to SB000016K00
Vgs = 0.8V~1.1V

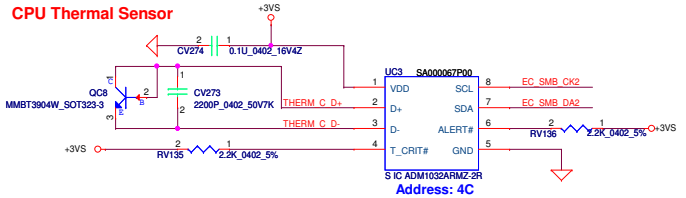
Hardware Strap				
Pin Name	**Purpose**	**PU/PD**	**Description**	**Default State**
GPIO_SUS0	DDI0 Detect	PU	1: DDI0 detected 0: DDI0 not detected	High
GPIO_SUS1	DDI1 Detect	PU	1: DDI1 detected 0: DDI1 not detected	High
GPIO_SUS2	A16 swap overdrive	PU	1: Normal operation 0: Change Boot Loader address	High
GPIO_SUS3	DSI Display Detect	NC	1: DSI detected 0: DSI not detected	Low
GPIO_SUS4	Boot BIOS Strap BBS	PU	1: Boot from SPI 0: Boot from LPC	High
GPIO_SUS5	Flash Descriptor Security Override	PU	1: Security enabled 0: Security disabled	High
GPIO_SUS6	DFX Boot Halt Strap, VISA Early POSM Debug Enable	PU	1: Normal operation 0: Halt boot enable	High
GPIO_SUS7	DFX Sus Debug Strap	PU	1: Normal operation 0: Sus Debug enabled	High
SEC_GPIO_SUS8	ICLK, USB2, DDI SFR Supply Select	PD	1: 1.35V supply 0: 1.25V supply	Low
SEC_GPIO_SUS9	ICLK, USB2, DDI SFR Bypass	NC	1: Bypass with 1.05V 0: No bypass	Low
SEC_GPIO_SUS10	POSM Select	NC	1: PMC 0: Fuse controller	Don't care, if GPIO_SUS6 is pulled high
GP_CAMERASB08	ICLK Xtal OSC Bypass	PD	1: Bypass 0: No bypass	Low
GP_CAMERASB09	CCU SUS RO Bypass	PD	1: Bypass 0: No bypass	Low
GP_CAMERASB11	RTC OSC Bypass	PD	1: Bypass 0: No bypass	Low











Security Classification	Compal Secret Data		
Issued Date	2014/08/21	Deciphered Date	2015/08/21

Compal Electronics, Inc.			
Title	VLV-M SOC CLK/PMU/SPI		
Size C	Document Number LA-706P		Rev 0.1
Date: Thursday, January 07, 2016	Sheet 8 of 50		

USB3 Port 0

USOC1F CHV_MCP_EDS

USB3.0 Port
USB2.0 Port
Camera
CR
USB Hub

DG need 112.5_1% not exist in ISPD

Change 45.3_1% for Intel request

6 OF 13

BSW-MCP-EDS_FCBGA1170

For XDP use

USOC1G CHV_MCP_EDS

7 OF 13

BSW-MCP-EDS_FCBGA1170

PLT_RST# Buffer

Sch. chelist PU 1k

RTC Well Reset

Clear CMOS

Clear CMOS
Close to RAM door

PDG v0.9 page291 : RTC_RST# –
When asserted, this signal resets register bits in the RTC well.

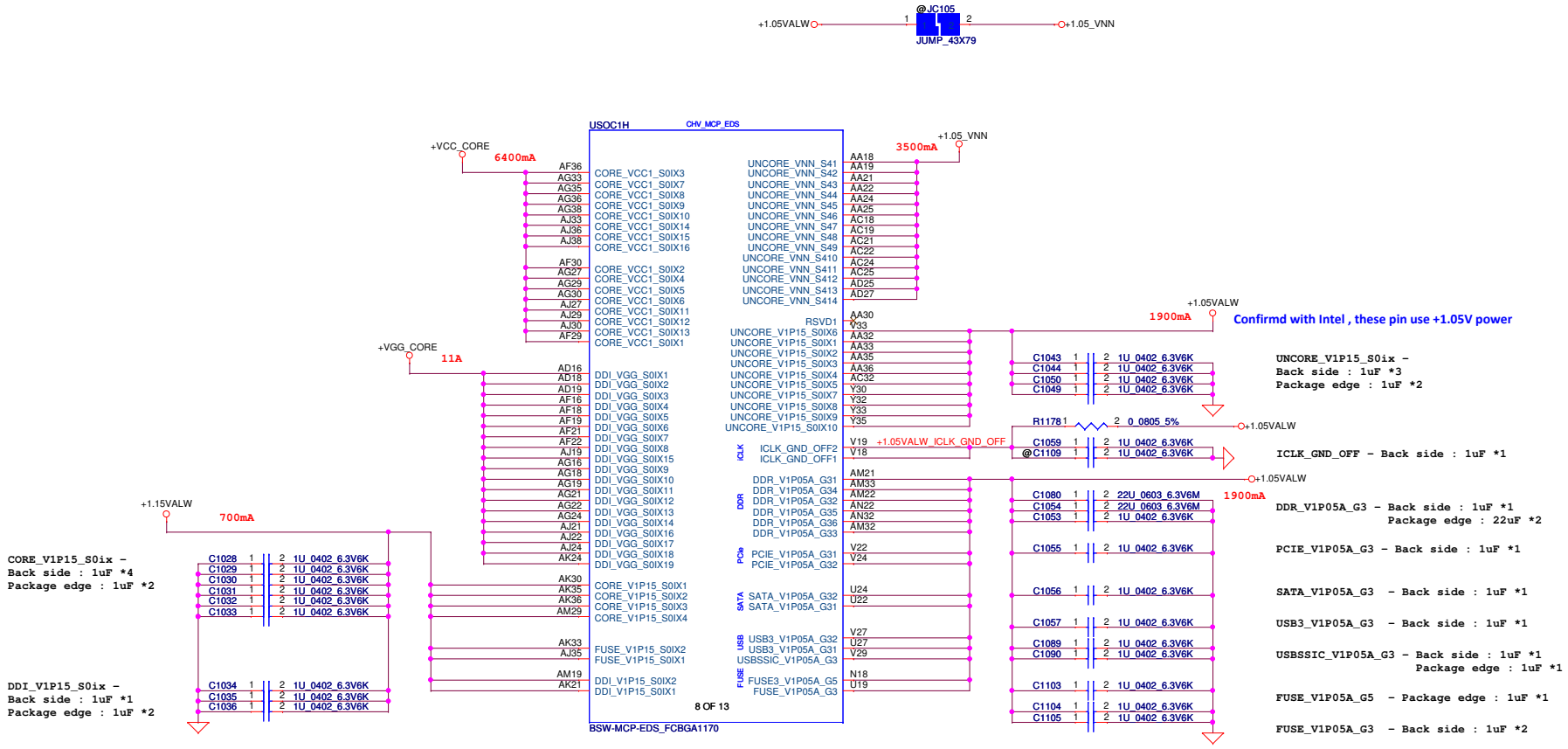
Security Classification	Compal Secret Data		
Issued Date	2014/08/21	Deciphered Date	2015/08/21

Compal Electronics, Inc.

Title: VLV-M SOC USB/LPC/SMBus

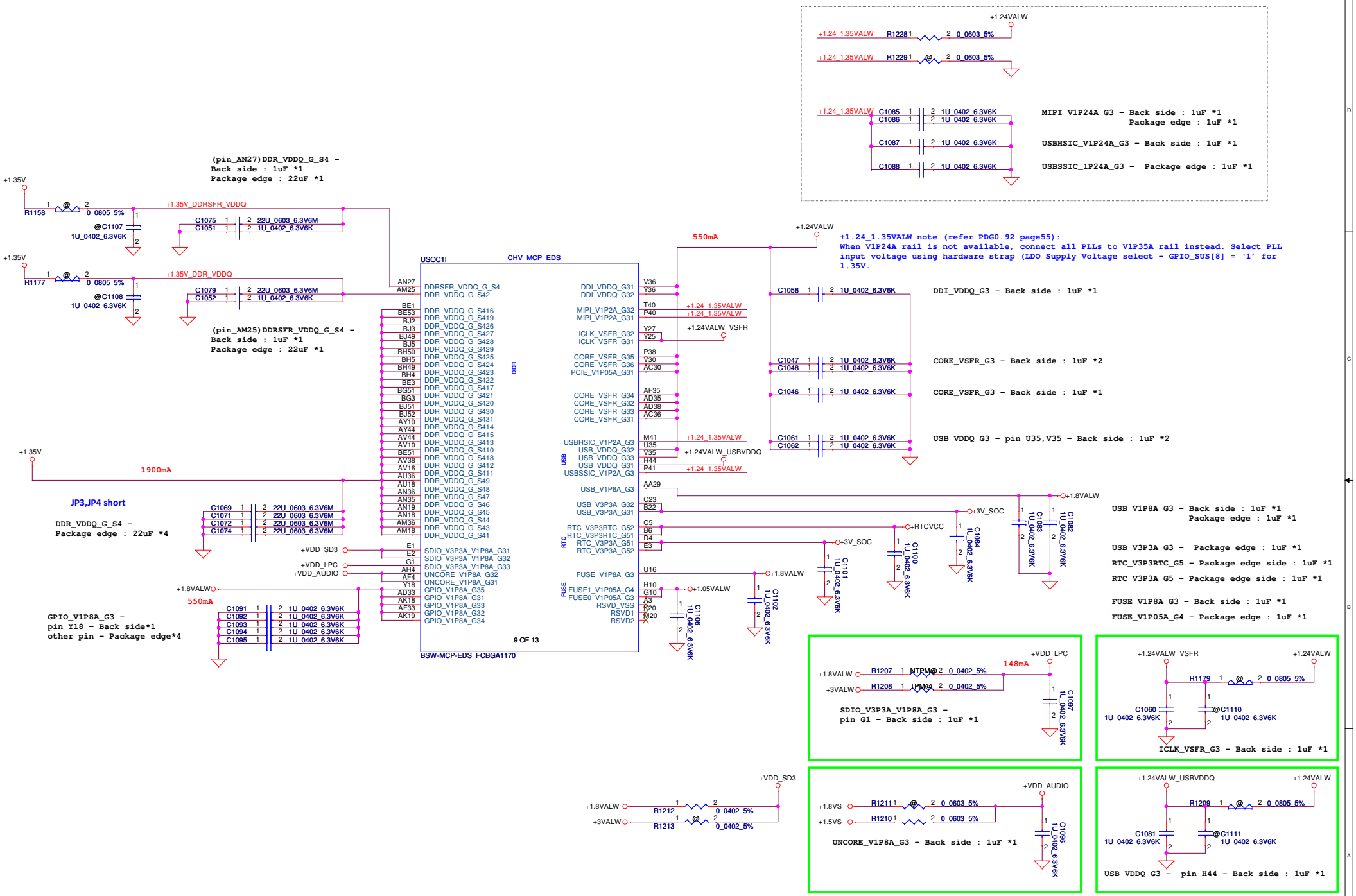
Size: Custom | Document Number: LA-706P | Rev: 0.1

Date: Thursday, January 07, 2016 | Sheet 9 of 50



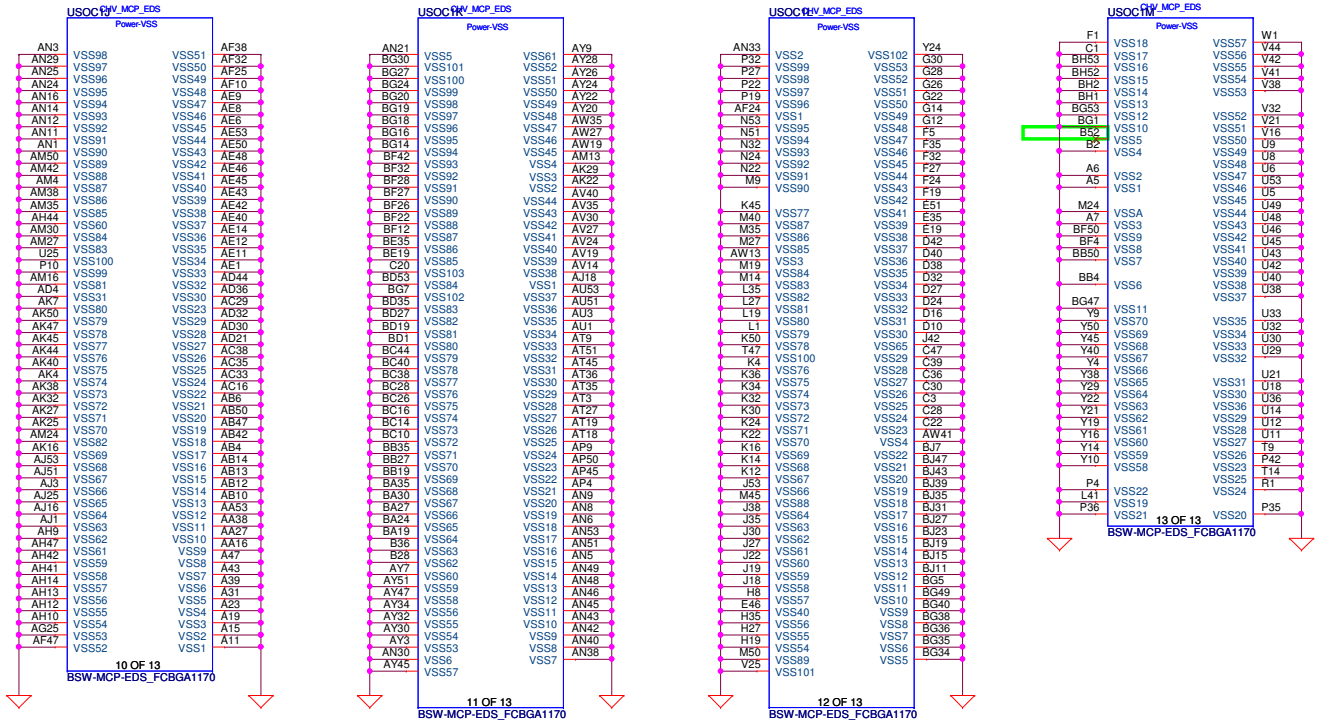
Security Classification	Compal Secret Data		
Issued Date	2014/08/21	Deciphered Date	2015/08/21

Compal Electronics, Inc.			
Title	VLV-M SOC Power		
Size	Custom	Document Number	LA-706P
Rev	0.1		
Date:	Thursday, January 07, 2016	Sheet	10 of 50



Security Classification	Compal Secret Data		
Issued Date	2014/08/21	Deciphered Date	2015/08/21

Compal Electronics, Inc.			
Title: VLV-M SOC Power			
Size: Custom	Document Number: LA-706P		Rev: 0.1
Date: Thursday, January 07, 2016	Sheet 11 of 50		



Security Classification	Compal Secret Data		
Issued Date	2014/08/21	Deciphered Date	2015/08/21

Compal Electronics, Inc.

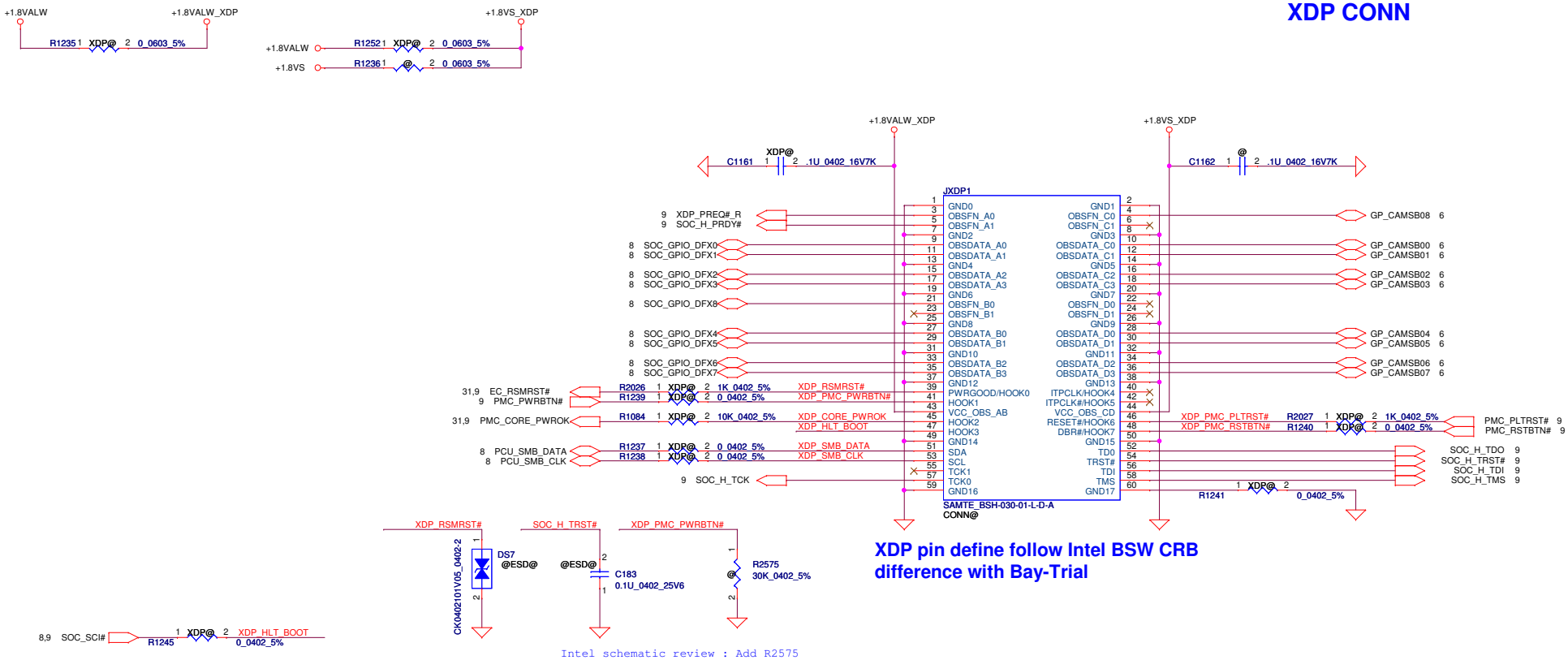
Title: VLV-M SOC GND

Size: Custom | Document Number: LA-706P | Rev: 0.1

Date: Thursday, January 07, 2016 | Sheet 12 of 50

APS CONN

XDP CONN



XDP pin define follow Intel BSW CRB difference with Bay-Trial

Intel schematic review : Add R2575

Security Classification	Compal Secret Data		
Issued Date	2014/08/21	Deciphered Date	2015/08/21

Compal Electronics, Inc.

Title: **BDW MCP(1/11) DDI,MSIC,XDP**

Size	Document Number	Rev
Custom	LA-706P	0.3

Date: Thursday, January 07, 2016 Sheet 13 of 50

R70@
U666
R16M-M1-70
SA00009I800

U666A R30@ SA000087T90

AC Coupling Capacitor
PCIe Gen3: Recommended value is 220 nF
PCIe Gen1 and Gen2 only: Recommended value is 100 nF

7 PCIE_ATX_C_GRX_P0 → AF30 PCIE_RX0P
7 PCIE_ATX_C_GRX_N0 → AE31 PCIE_RX0N
PCIE_TX0P AH30 → PCIE_GTX_ARX_P0 0.1U_0402_16V7K 2 1 PX@ C5187 → PCIE_GTX_C_ARX_P0 7
PCIE_TX0N AG31 → PCIE_GTX_ARX_N0 0.1U_0402_16V7K 2 1 PX@ C5188 → PCIE_GTX_C_ARX_N0 7

7 PCIE_ATX_C_GRX_P1 → AE29 PCIE_RX1P
7 PCIE_ATX_C_GRX_N1 → AD28 PCIE_RX1N
PCIE_TX1P AG29 → PCIE_GTX_ARX_P1 0.1U_0402_16V7K 2 1 PX@ C5189 → PCIE_GTX_C_ARX_P1 7
PCIE_TX1N AF28 → PCIE_GTX_ARX_N1 0.1U_0402_16V7K 2 1 PX@ C5190 → PCIE_GTX_C_ARX_N1 7

AD30 AC31 PCIE_RX2P PCIE_RX2N
PCIE_TX2P PCIE_TX2N AF27 AF26

AC29 AB28 PCIE_RX3P PCIE_RX3N
PCIE_TX3P PCIE_TX3N AD27 AD26

AB30 AA31 PCIE_RX4P PCIE_RX4N
PCIE_TX4P PCIE_TX4N AC25 AB25

AA29 Y28 PCIE_RX5P PCIE_RX5N
PCIE_TX5P PCIE_TX5N Y23 Y24

Y30 W31 PCIE_RX6P PCIE_RX6N
PCIE_TX6P PCIE_TX6N AB27 AB26

W29 V28 PCIE_RX7P PCIE_RX7N
PCIE_TX7P PCIE_TX7N Y27 Y26

V30 U31 NC#V30 NC#U31
NC#W24 NC#W23 W24 W23

U29 T28 NC#U29 NC#T28
NC#V27 NC#U26 V27 U26

T30 R31 NC#T30 NC#R31
NC#U24 NC#U23 U24 U23

R29 P28 NC#R29 NC#P28
NC#T26 NC#T27 T26 T27

P30 N31 NC#P30 NC#N31
NC#T24 NC#T23 T24 T23

N29 M28 NC#N29 NC#M28
NC#P27 NC#P26 P27 P26

M30 L31 NC#M30 NC#L31
NC#P24 NC#P23 P24 P23

L29 K30 NC#L29 NC#K30
NC#M27 NC#N26 M27 N26

CLOCK
7 CLK_PEG_VGA → CLK_PEG_VGA AK30 PCIE_REFCLKP
7 CLK_PEG_VGA# → CLK_PEG_VGA# AK32 PCIE_REFCLKN

CALIBRATION
+1.05VS_VGA
PCIE_CALR_TX Y22 R5159 1 PX@ 2 1.69K_0402_1%
PCIE_CALR_RX AA22 R717 1 PX@ 2 1K_0402_1%

R1400 1 PX@ 2 1K_0402_5% N10 TEST_PG

GPU_RST# AL27 PERSTB

PCI EXPRESS INTERFACE

216-0841018 A0 SUN PRO S3

No Use GPU Display Port outpud

U666F R30@

+VGA_CORE
VARY_BL AB11 R1676 1 R70@ 2 0_0402_5%
DIGON AB12 R1675 1 R70@ 2 0_0402_5%

TXCAP_DPA3P AL15
TXCAM_DPA3N AK14
TX0P_DPA2P AH16
TX0M_DPA2N AJ15
TX1P_DPA1P AL17
TX1M_DPA1N AK16
TX2P_DPA0P AH18
TX2M_DPA0N AJ17
NC_TXOUT_L3P AL19
NC_TXOUT_L3N AK18

TMDP

TXCBP_DPB3P AH20
TXCBM_DPB3N AJ19
TX3P_DPB2P AL21
TX3M_DPB2N AK20
TX4P_DPB1P AH22
TX4M_DPB1N AJ21
TX5P_DPB0P AL23
TX5M_DPB0N AK22
NC_TXOUT_U3P AK24
NC_TXOUT_U3N AJ23

216-0841018 A0 SUNPRO S3

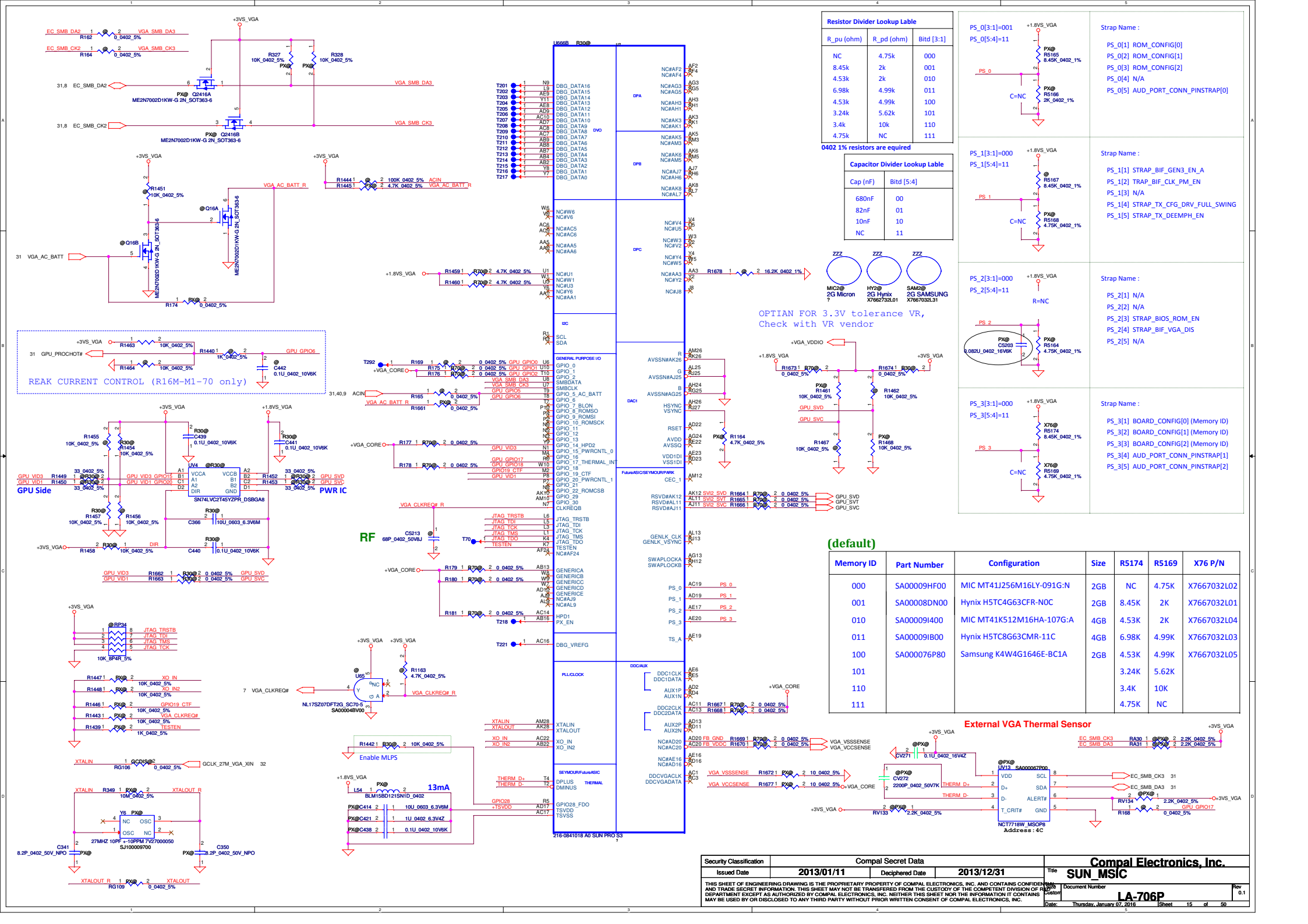
CPU Side 1.8V

+3VS_VGA
+1.8VALW
PX@ U66 NC A Y
R892 10K_0402_5%
8 PXS_RST# → PXS_RST#_B → 25,27,31,9 PLT_RST_BUF#
NL17SZ07DFT2G_SC70-5
SA00004BV00
R1144 1 @ 2 0_0402_5%

+3VS_VGA +3VS
R1681 0_0402_5% @ R1691 0_0402_5%
PX@ U7 B A Y
PXS_RST#_B → GPU_RST#
MC74VHC1G08DFT2G_SC70-5
PX@ R1631 100K_0402_5%
GPU_RST# → DC5 R70@ CH751H-40PT_SOD323-2 → R487 R30@ 0_0402_5% → VGA_PWRGD 47

Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

Compal Electronics, Inc.
Title: SUN_PCIE/DP
Size: Custom | Document Number: LA-706P | Rev: 0.1
Date: Thursday, January 07, 2016 | Sheet 14 of 50


Resistor Divider Lookup Lable
R_pu (ohm) | R_pd (ohm) | Bitd [3:1]
NC | 4.75k | 000
8.45k | 2k | 001
4.53k | 2k | 010
6.98k | 4.99k | 011
4.53k | 4.99k | 100
3.24k | 5.62k | 101
3.4k | 10k | 110
4.75k | NC | 111
0402 1% resistors are equired
Capacitor Divider Lookup Lable
Cap (nF) | Bitd [5:4]
680nF | 00
82nF | 01
10nF | 10
NC | 11
PS_0[3:1]=001
PS_0[5:4]=11
Strap Name :
PS_0[1] ROM_CONFIG[0]
PS_0[2] ROM_CONFIG[1]
PS_0[3] ROM_CONFIG[2]
PS_0[4] N/A
PS_0[5] AUD_PORT_CONN_PINSTRAP[0]
PS_1[3:1]=000
PS_1[5:4]=11
Strap Name :
PS_1[1] STRAP_BIF_GEN3_EN_A
PS_1[2] TRAP_BIF_CLK_PM_EN
PS_1[3] N/A
PS_1[4] STRAP_TX_CFG_DRV_FULL_SWING
PS_1[5] STRAP_TX_DEEMPH_EN
PS_2[3:1]=000
PS_2[5:4]=11
R=NC
Strap Name :
PS_2[1] N/A
PS_2[2] N/A
PS_2[3] STRAP_BIOS_ROM_EN
PS_2[4] STRAP_BIF_VGA_DIS
PS_2[5] N/A
PS_3[3:1]=000
PS_3[5:4]=11
Strap Name :
PS_3[1] BOARD_CONFIG[0] (Memory ID)
PS_3[2] BOARD_CONFIG[1] (Memory ID)
PS_3[3] BOARD_CONFIG[2] (Memory ID)
PS_3[4] AUD_PORT_CONN_PINSTRAP[1]
PS_3[5] AUD_PORT_CONN_PINSTRAP[2]
OPTIAN FOR 3.3V tolerance VR,
Check with VR vendor
REAK CURRENT CONTROL (R16M-M1-70 only)
GPU Side
PWR IC
RF
(default)
Memory ID | Part Number | Configuration | Size | R5174 | R5169 | X76 P/N
000 | SA00009HF00 | MIC MT41J256M16LY-091G:N | 2GB | NC | 4.75K | X7667032L02
001 | SA00008DN00 | Hynix H5TC4G63CFR-N0C | 2GB | 8.45K | 2K | X7667032L01
010 | SA00009I400 | MIC MT41K512M16HA-107G:A | 4GB | 4.53K | 2K | X7667032L04
011 | SA00009IB00 | Hynix H5TC8G63CMR-11C | 4GB | 6.98K | 4.99K | X7667032L03
100 | SA000076P80 | Samsung K4W4G1646E-BC1A | 2GB | 4.53K | 4.99K | X7667032L05
101 | | | | 3.24K | 5.62K |
110 | | | | 3.4K | 10K |
111 | | | | 4.75K | NC |
External VGA Thermal Sensor
13mA
Enable MLPS
216-0841018 A0 SUN PRO S3
Security Classification
Compal Secret Data
Issued Date
2013/01/11
Deciphered Date
2013/12/31
Compal Electronics, Inc.
Title
SUN_MSIC
Size
Custom
Document Number
LA-706P
Rev
0.1
Date:
Thursday, January 07, 2016
Sheet
15
of
50
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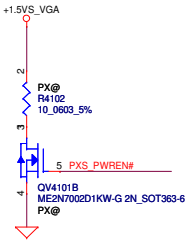
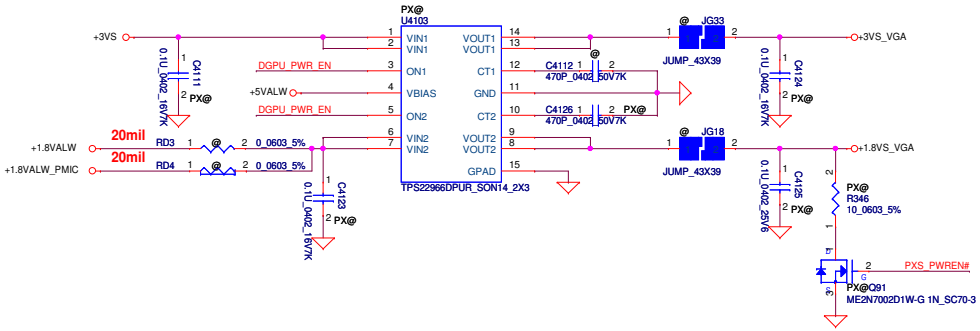
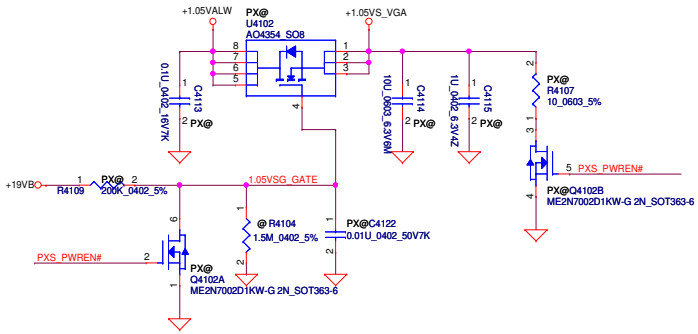
+1.5VS to +1.5VS_VGA (4A)

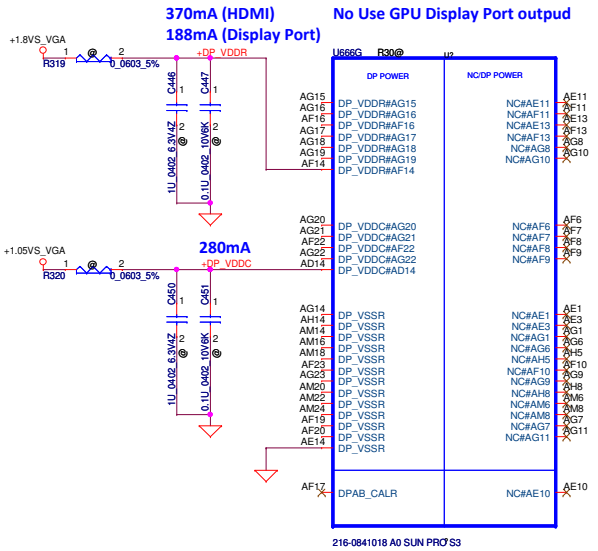


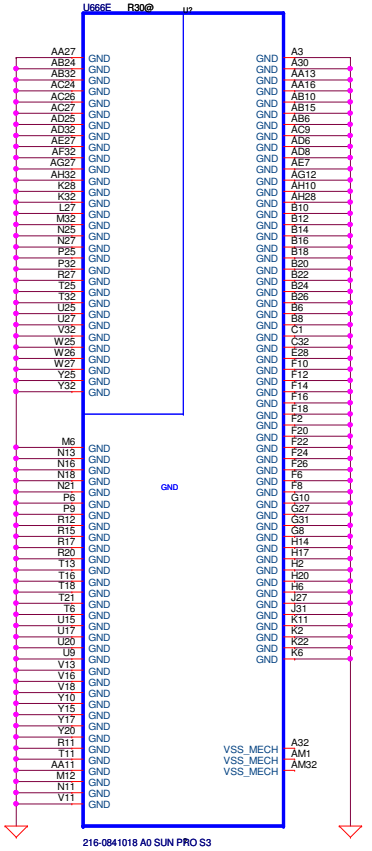
+3VS to +3VS_VGA (25mA)
+1.8VALW to +1.8VS_VGA (331mA)

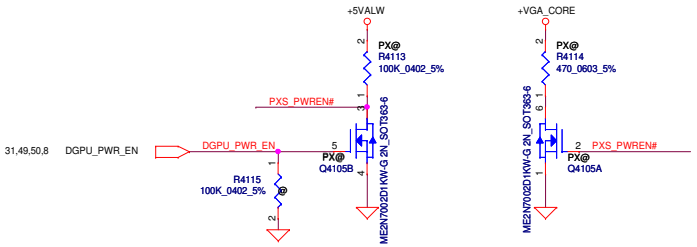


+1.05VALW to +1.05VGA (2A)









Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

Compal Electronics, Inc.

Title: SUN_Power/GND

Size: Custom | Document Number: LA-706P | Rev: 0.1

Date: Thursday, January 07, 2016 | Sheet 16 of 50

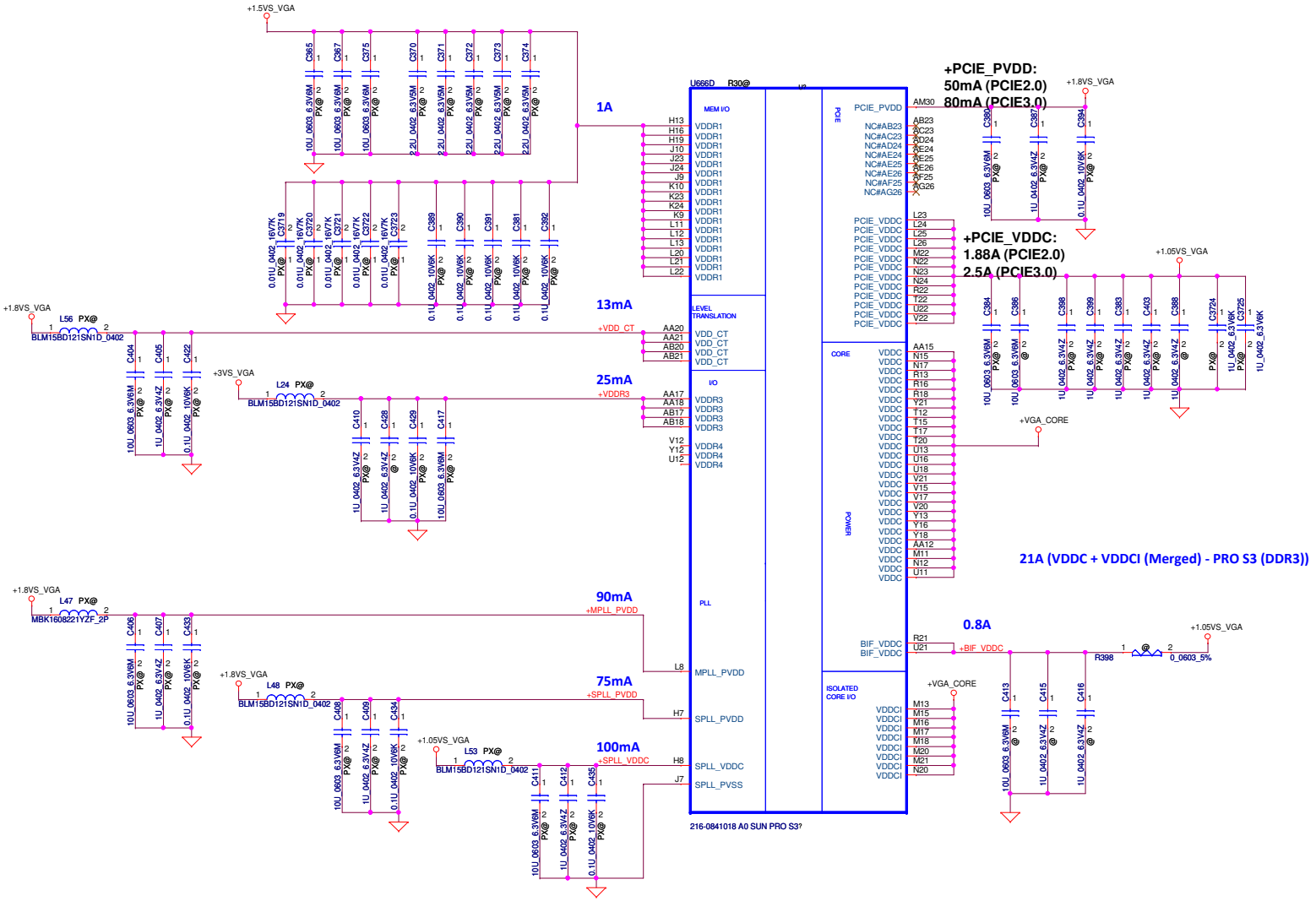
+VGA_CORE		10uF	1uF	0.1uF
VDDC	TBD	5 (1@)	10 (2@)	0
VDDCI	3.5A	1	3	0

+0.95VS_VGA		10uF	1uF	0.1uF
PCIE_VDDC	2.5A	2 (1@)	5 (1@)	0
BIF_VDDC	1.4A	0	0	0
SPLL_VDDC	100mA	1	1	1

+1.5VS_VGA		10uF	1uF	0.1uF
VDDR1	1.5A	3	5	5

+1.8VS_VGA		10uF	1uF	0.1uF
PCIE_PVDD	100mA	1	1	1
MPLL_PVDD	130mA	1	1	1
SPLL_PVDD	75mA	1	1	1
VDDR4	(300mA)	0	0	0
VDD_CT	13mA	1	1	1
+TSVDD	13mA	1	1	1
+DP_VDDR		0	0	0
+DP_VDDC		0	0	0

+3VS_VGA		10uF	1uF	0.1uF
VDDR3	25mA	0	2 (1@)	1



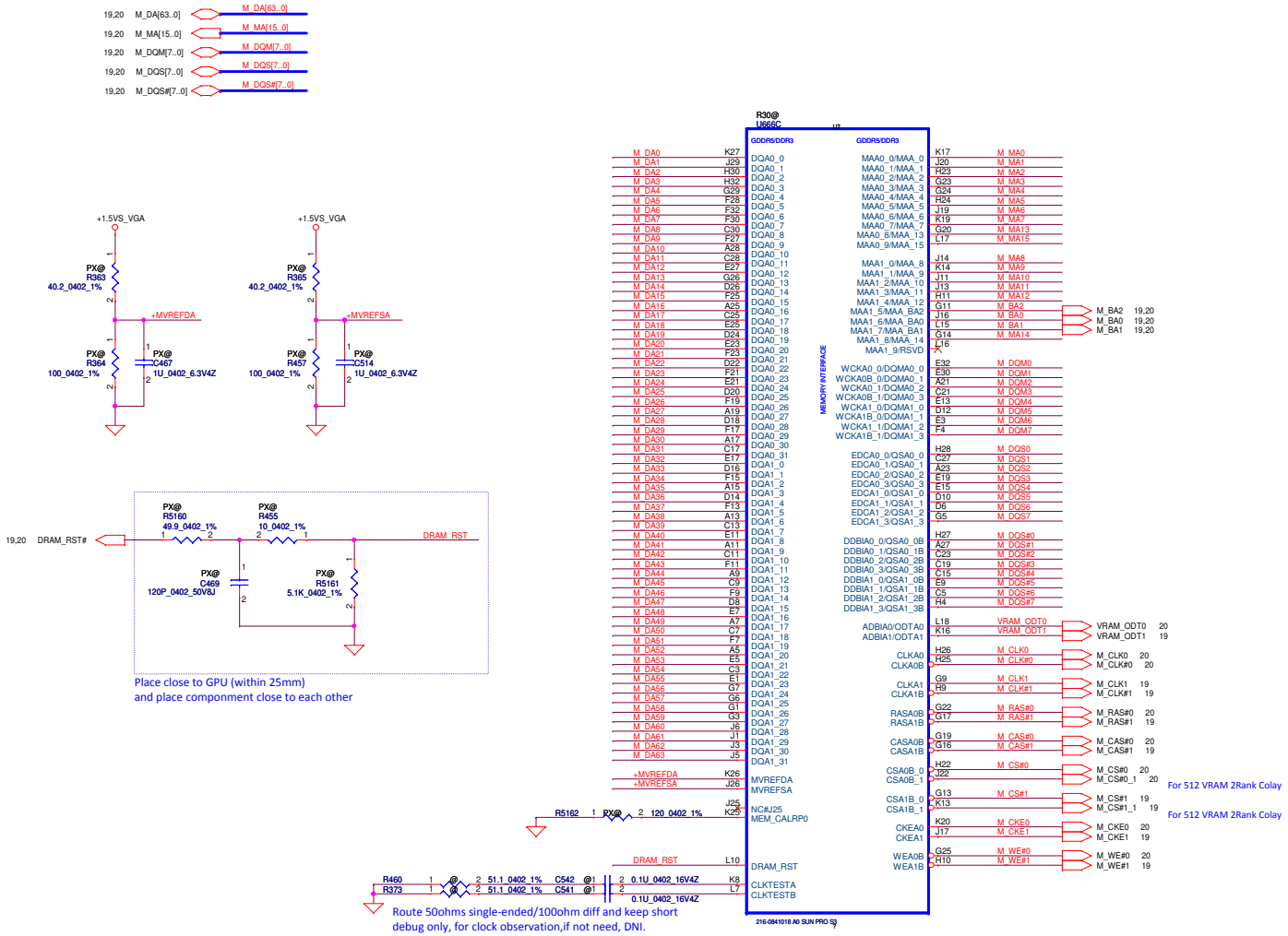
Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

Compal Electronics, Inc.

Title: SUN_Power

Size: Custom | Document Number: LA-706P | Rev: 0.1

Date: Thursday, January 07, 2016 | Sheet 17 of 50



Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

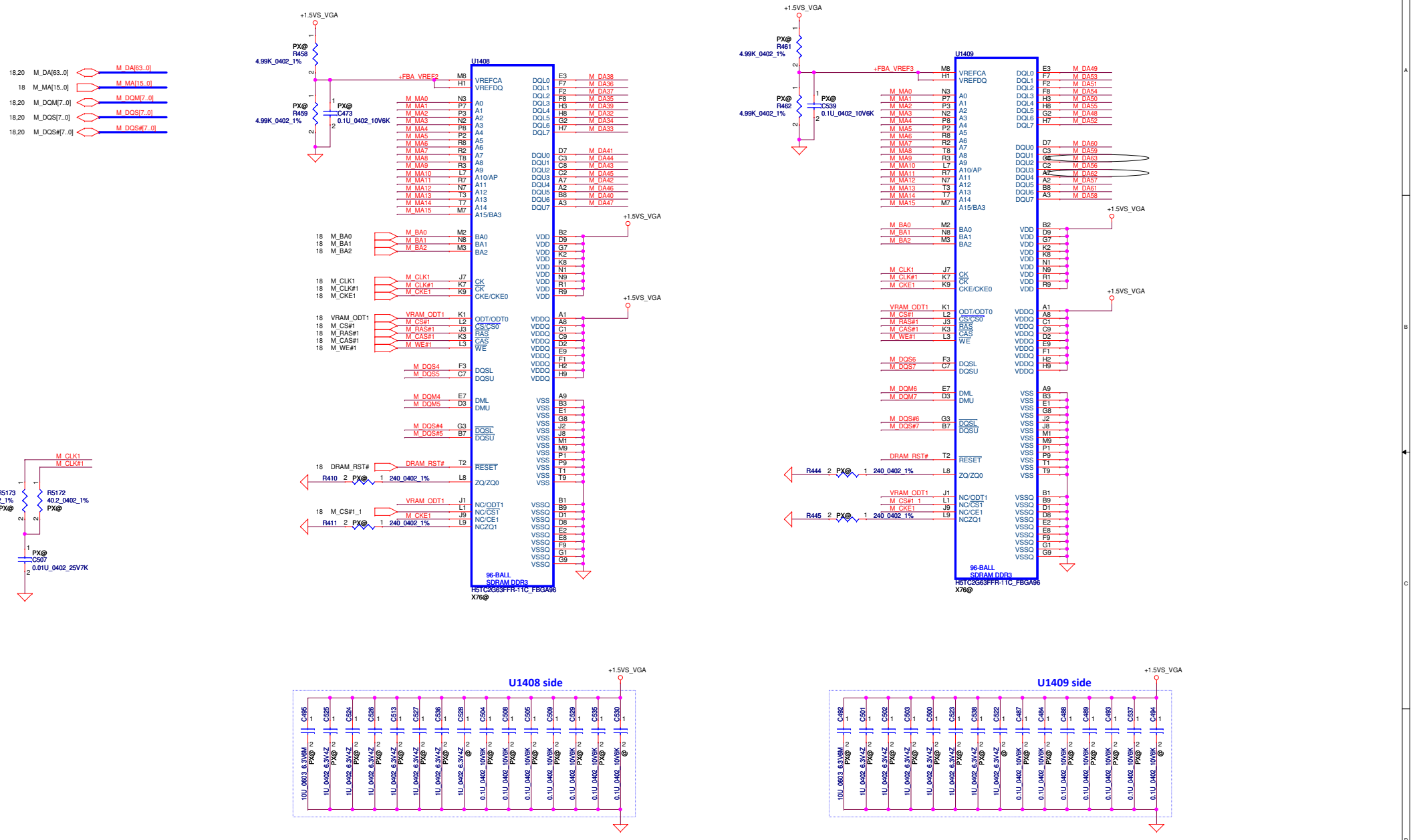
Compal Electronics, Inc.

Title: SUN_MEM

Size: C | Document Number: LA-706P | Rev: 0.1

Date: Thursday, January 07, 2016 | Sheet 18 of 50

Memory Partition A – Upper 32 bits



Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

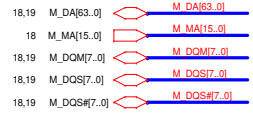
Compal Electronics, Inc.

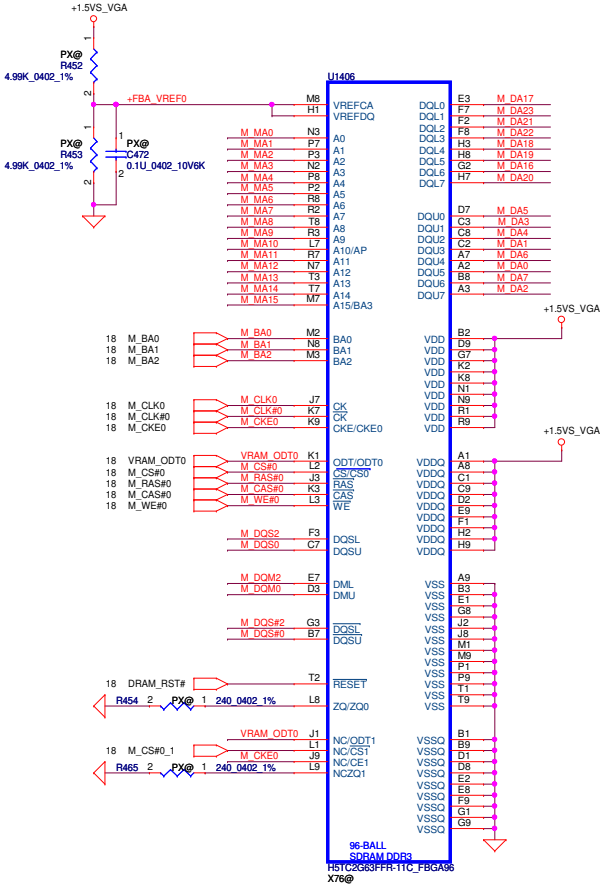
Title: SUN_VRAM A Upper

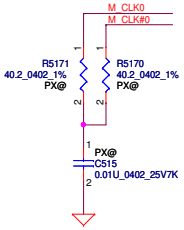
Size: Custom | Document Number: LA-706P | Rev: 0.1

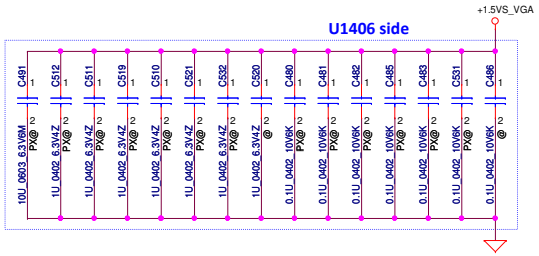
Date: Thursday, January 07, 2016 | Sheet 19 of 50

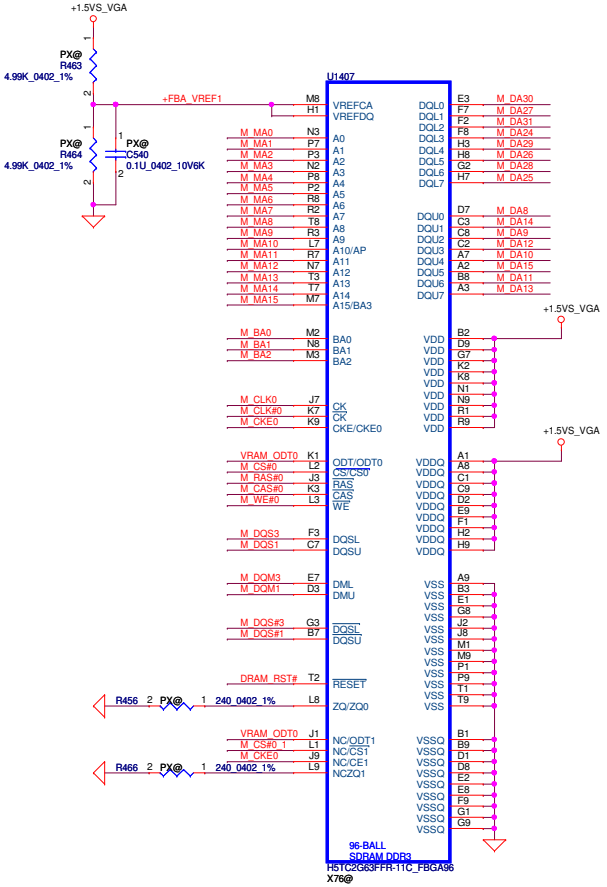
Memory Partition A - Lower 32 bits

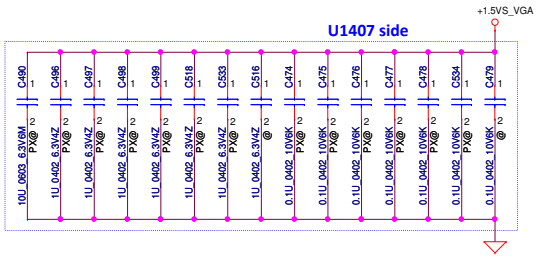












Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

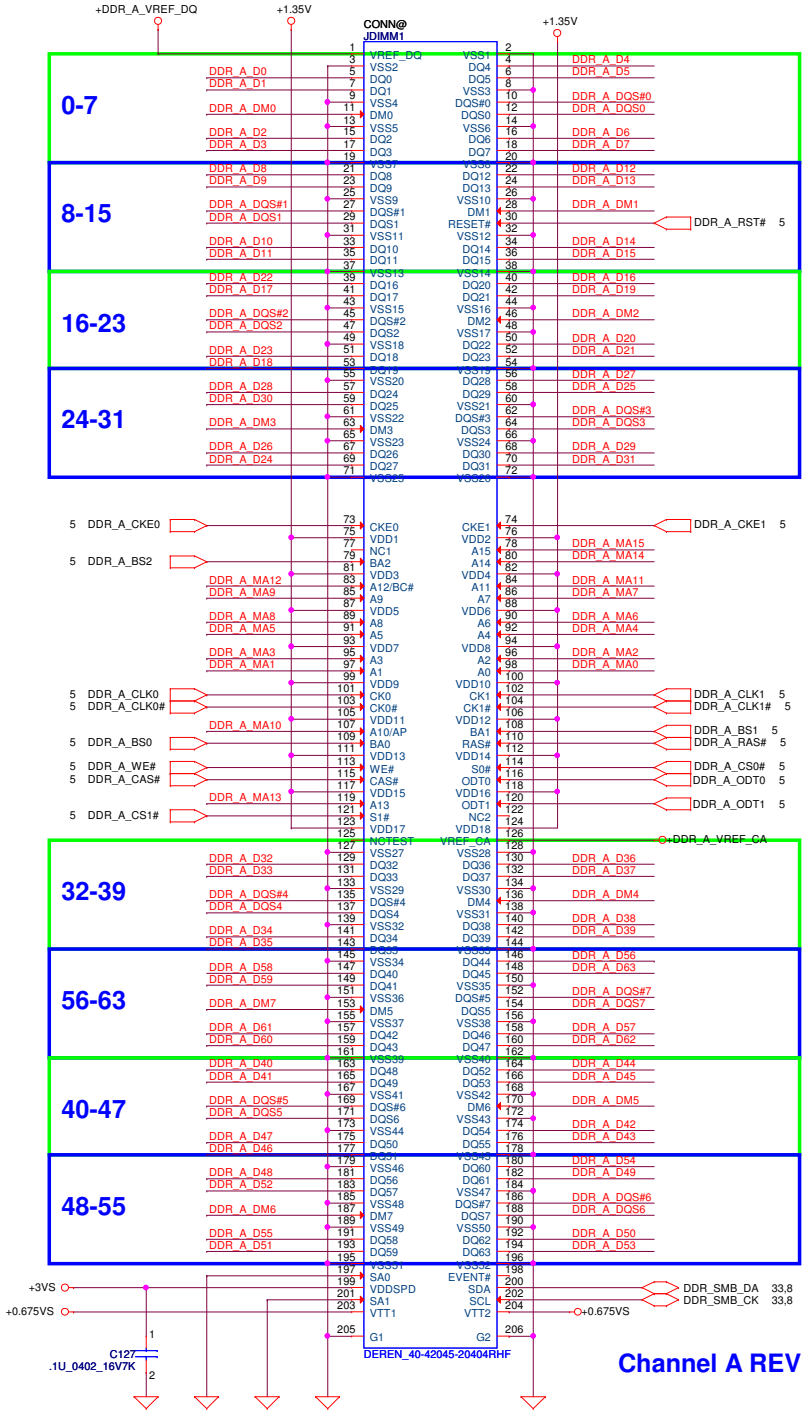
Compal Electronics, Inc.

Title: SUN_VRAM A Lower

Size: Custom | Document Number: LA-706P | Rev: 0.1

Date: Thursday, January 07, 2016 | Sheet 20 of 50

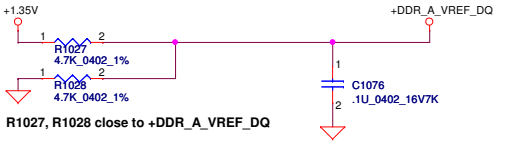
All VREF traces should have 10 mil trace width



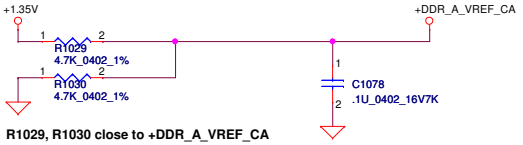
SA1: SA0 = 00
Address: A0h/10100000b

DDR_A_DQS#[0..7] 5
DDR_A_DQS[0..7] 5
DDR_A_D[0..63] 5
DDR_A_MA[0..15] 5
DDR_A_DM[0..7] 5

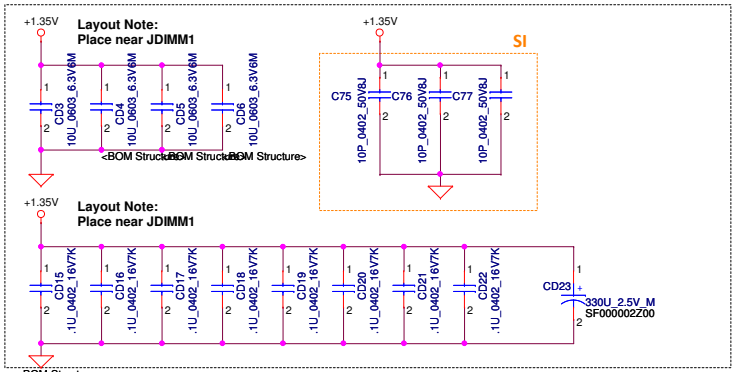
Signal voltage level = 0.675 V
PLACE TWO 4.7K RESISTORS CLOSE TO
DIMMS ON DIMM_VREF_CA / DIMM_VREF_DQ
Decoupling caps are needed; one 0.1 µF placed close to VREF pins of each DDR3 SODIMM.

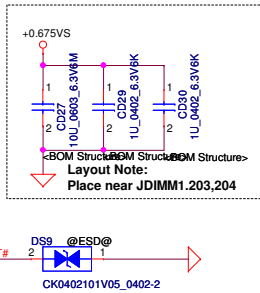


R1027, R1028 close to +DDR_A_VREF_DQ



R1029, R1030 close to +DDR_A_VREF_CA





Channel A REV

Security Classification	Compal Secret Data		
Issued Date	2014/07/07	Deciphered Date	2015/07/07

Compal Electronics, Inc.

Title: DDR3L DIMMA

Size: Custom | Document Number | Rev: 1.0

Date: Thursday, January 07, 2016 | Sheet 21 of 50

Channel B Rev

<Address: SA0:SA1=10 (A2H)>

DIMM_2 REV H:4mm

Security Classification	Compal Secret Data		
Issued Date	2014/08/21	Deciphered Date	2015/08/21

Compal Electronics, Inc.

Title: DDR3L DIMMB

Size	Document Number	Rev
Custom	LA-706P	0.1

Date: Thursday, January 07, 2016 Sheet 22 of 50

LCD Power Swtich

+3VS
UG1 SA00006Y800
VIN
VOUT
EN
GND
/OC
G524B1T11U_SOT23-5
CG1 1500P_0402_50V7K
4.7U_0603_6.3V6K CG2
0.1U_0402_16V7K CG3
+LCDVDD
6 DP_ENVDD
RG3 0_0402_5%

Camera

9 USB20_N2
9 USB20_P2
R170 0_0402_5%
L12 SM070003Y00
WCM-2012-900T_4P
R171 0_0402_5%
USB20_N2_R
USB20_P2_R

INVPWR_B+
+19VB
W=60mils
W=60mils
L1 EMI@ SM010014520 0_0805_5%
L2 EMI@ SM010014520 0_0805_5%
SM010014520 3000ma
220ohm@100mhz
DCR 0.04
@EMI@ C117 680P_0402_50V7K
C118 68P_0402_50V8J

Touch Screen

26 USB20_HUB_N1
26 USB20_HUB_P1
R172 0_0402_5%
L3 SM070003Y00
WCM-2012-900T_4P
R173 0_0402_5%
USB20_HUB_N1_R
USB20_HUB_P1_R

Touch Screen Power

+3VALW
+5VALW
RTS3 100K_0402_5%
TS@ RTS6 100K_0402_5%
RTS1 TS@ 1K_0402_5%
TS@ QTS1 2N7002_SOT23
TOUCH_ON# 31
CTS2 TS@ 0.047U_0402_16V7K
+VCC_TOUCH
20mil
TS@ QTS2 LP2301ALT1G 1P SOT-23-3
+VCC_TOUCH_R
20mil
RTS4 @ 0_0402_5% +3VS
RTS5 TS@ 0_0402_5% +5VS
CTS1 TS@ 0.1U_0402_16V4Z

CC119/110 close JLVDS1

EDP_AUXP_F
EDP_AUXN_F
C119 @ 10P_0402_50V8J
C120 @ 10P_0402_50V8J
C121 220P_0402_50V7K INVTPWM
C122 220P_0402_50V7K DISOFF#

+1.8VALW
RT12 10K_0402_5%
6 EDP_HPD#
Q85B 2N7002KDWH_SOT363-6
RT13 @ 220P_0402_50V7K
RT11 100K_0402_5%
EDP_HPD

<CPU CTRL>

6 INVT_PWM
R258 @ 0_0402_5% INVTPWM
R163 @ 100K_0402_5%
7 TS_GPIO_CPU
31 TS_GPIO_EC
R260 0_0402_5%
R261 0_0402_5%
TS_GPIO

LCD PANEL Conn.

CONN@ JLVDS1
STARC_107K40-000001-G2
SP01000XE00

EDP_LN1P
EDP_LN1N
EDP_LN0P
EDP_LN0N
EDP_AUXP_F
EDP_AUXN_F
+LCDVDD
EDP_HPD RT19 @ 0_0402_5% EDP_HPD_R
INVPWR_B+
+VCC_TOUCH
+3VS
Camera USB20_N2_R USB20_P2_R
29 D_MIC_L_CLK
29 D_MIC_L_DATA

<EC CTRL>

31 BKOFF#
RT24 @ 0_0402_5% DISOFF#

Touch Screen

R166 33_0402_5%
R1671 10K_0402_5%
USB20_HUB_P1_R
USB20_HUB_N1_R
DISPOFF#_R
INVTPWM
TS_GPIO

CC103~108 close JLVDS <1000mil

CC103 .1U_0402_16V7K EDP_AUXP_F
CC104 .1U_0402_16V7K EDP_AUXN_F
CC105 .1U_0402_16V7K EDP_LN0N
CC106 .1U_0402_16V7K EDP_LN0P
CC107 .1U_0402_16V7K EDP_LN1P
CC108 .1U_0402_16V7K EDP_LN1N
6 EDP_AUXP
6 EDP_AUXN
6 EDP_TXN0
6 EDP_TXP0
6 EDP_TXP1
6 EDP_TXN1

RT16/17 Close JLVDS1

RT16 @ 100K_0402_5%
RT17 @ 100K_0402_5%
+3VS

11/17 reserver for ESD request

DM9 @ESD@ SCA00001L00
USB20_N2_R
USB20_P2_R
DM10 @ESD@ SCA00001L00
USB20_HUB_P1_R
USB20_HUB_N1_R
DM11 @ESD@ L03ESDL5V0CG3-2_SOT-523-3 SCA00002A00
D_MIC_L_CLK
D_MIC_L_DATA

Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

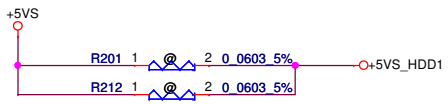
Compal Electronics, Inc.

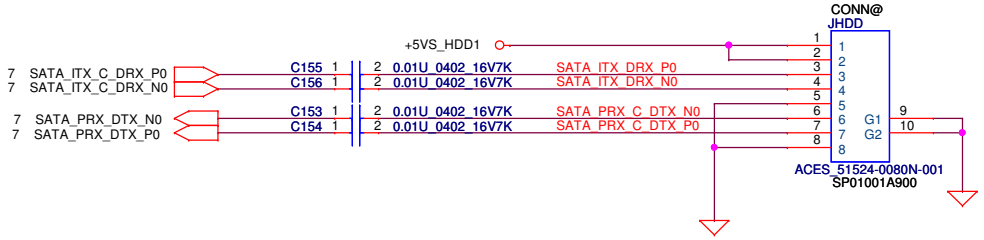
Title: LVDS Connector

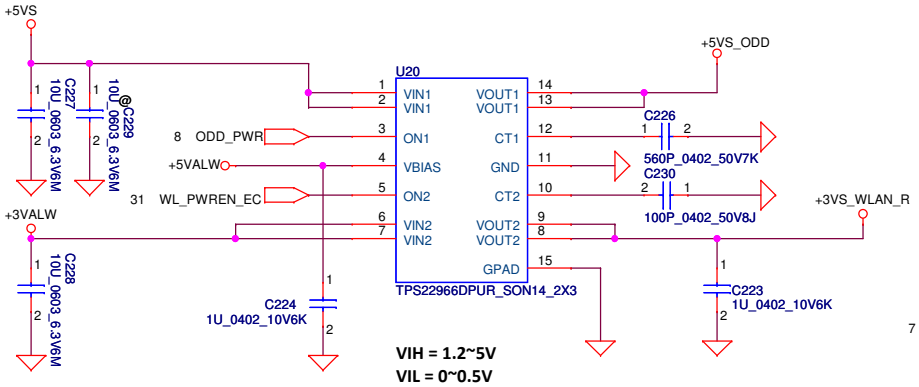
Size | Document Number | Rev 0.1

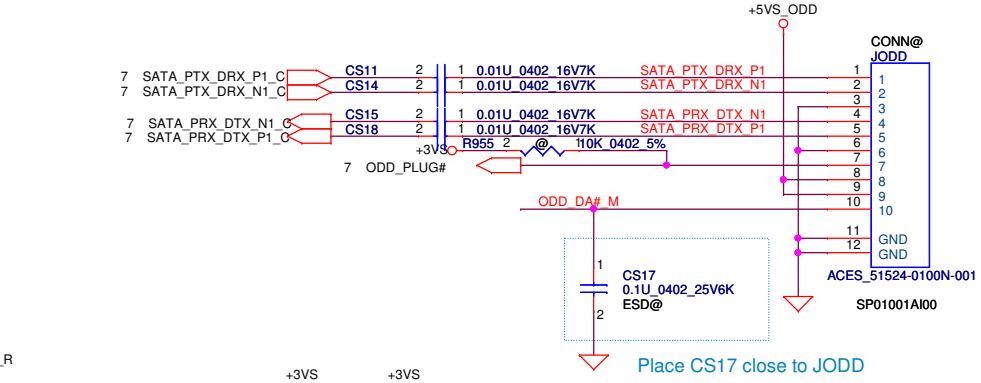
Date: Thursday, January 07, 2016 | Sheet 23 of 51

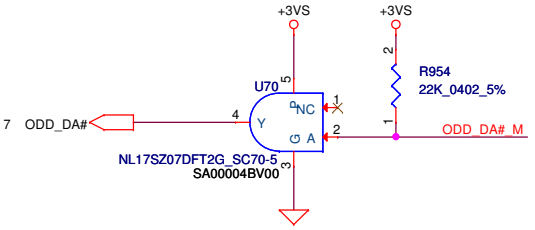
2.5" SATA HDD connector











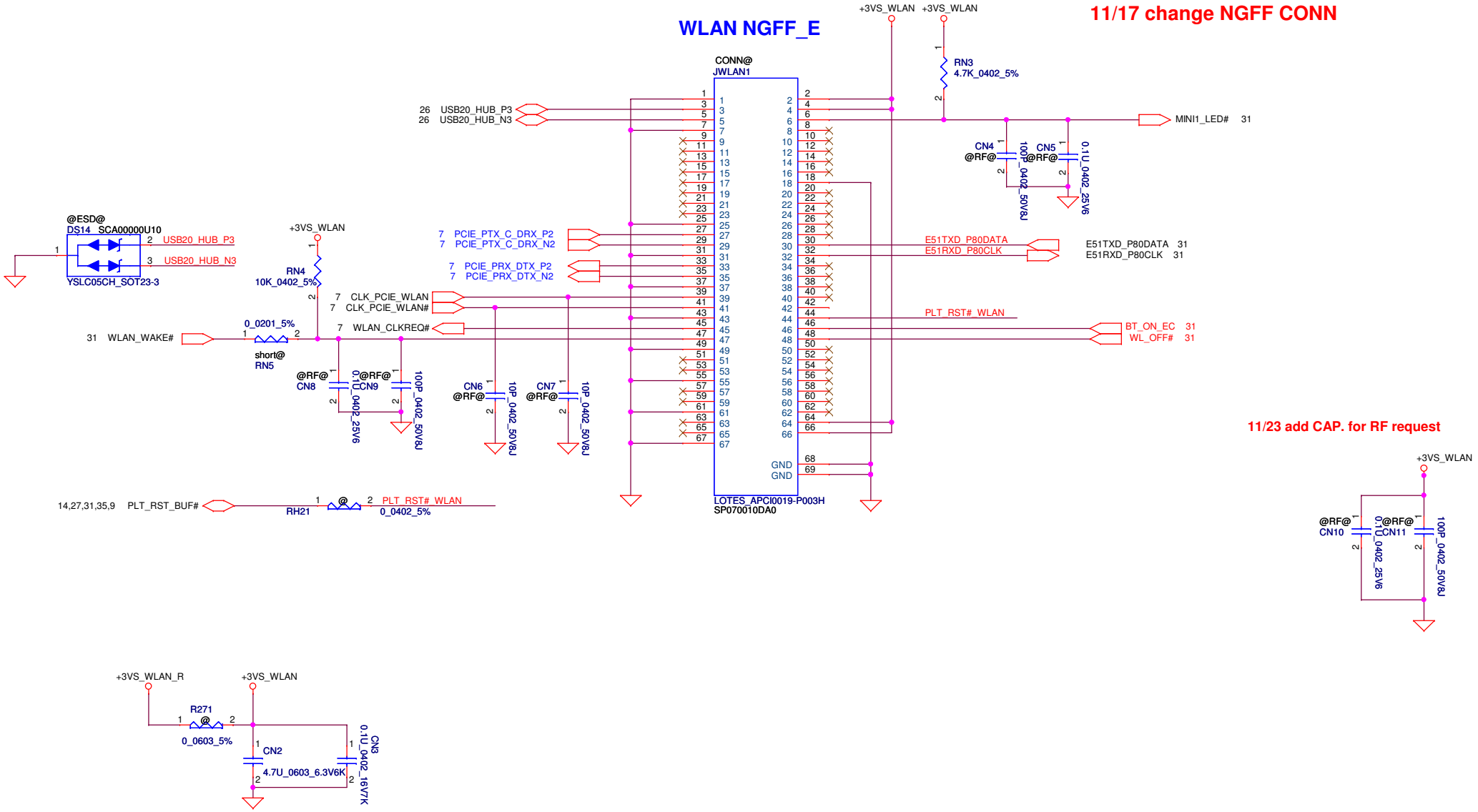
Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: ODD/SATA Conn

Size: B | Document Number: LA-706P | Rev: 0.1

Date: Thursday, January 07, 2016 | Sheet 24 of 51



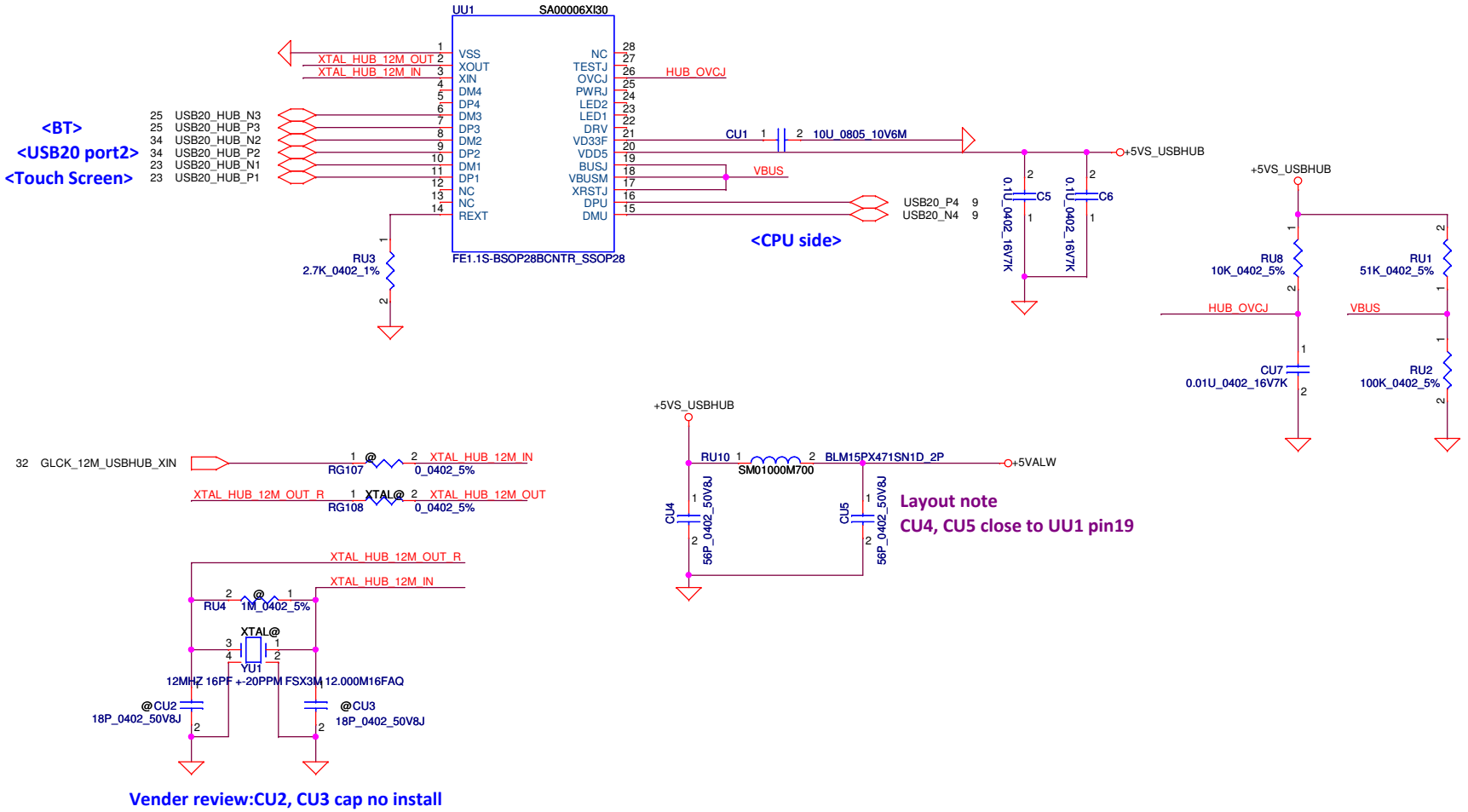
Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: **WLAN**

Size	Document Number	Rev
	LA-706P	0.1

Date: Thursday, January 07, 2016 Sheet 25 of 51



Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: USB2.0 Hub

Size: B | Document Number: LA-706P | Rev: 0.1

Date: Thursday, January 07, 2016 | Sheet 26 of 51

+LAN_VDD_3V3 Rising time
need>0.5mS and <100mS

	LDO mode	Switcing mode
LL1	SMT	@
CL21	SMT	@
LL2	@	SMT
CL8,CL23	@	SMT

CL14 & CL15 close UL1 Pin22
CL26 & CL27 close UL1 Pin30

Place CL11~CL13 close UL1 Pin 3, 8 , 22

LL2, CL8, CL23 for 8161
CL8 & CL18 close LL2

8111/8166 Co-Lay

+LAN_VDD_3V3=40mil
+VDDREG=40mil
+LAN_REGOUT=60mil

CL9 & CL5 close to UL1: Pin 11,32
CL19 close to UL1: Pin 32
CL20 close to UL1: Pin 11

CL10& CL16 close to UL1: Pin 23

RTL8166EH-CG

(SA000063500) 8166EH-CG 10/100
(SA000084T00) 8111HSH-CG Giga

Green CLK

SP050005L00 Footprint

Swap P/N 08/16

(SP050003P00) 10/100
(SP050008H00) Giga

11/26 change CONN.

1110_double check

1110_double check

powe rail need to check

YSUSB2.0-5_SOT-23-6-6
SC300002900

Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

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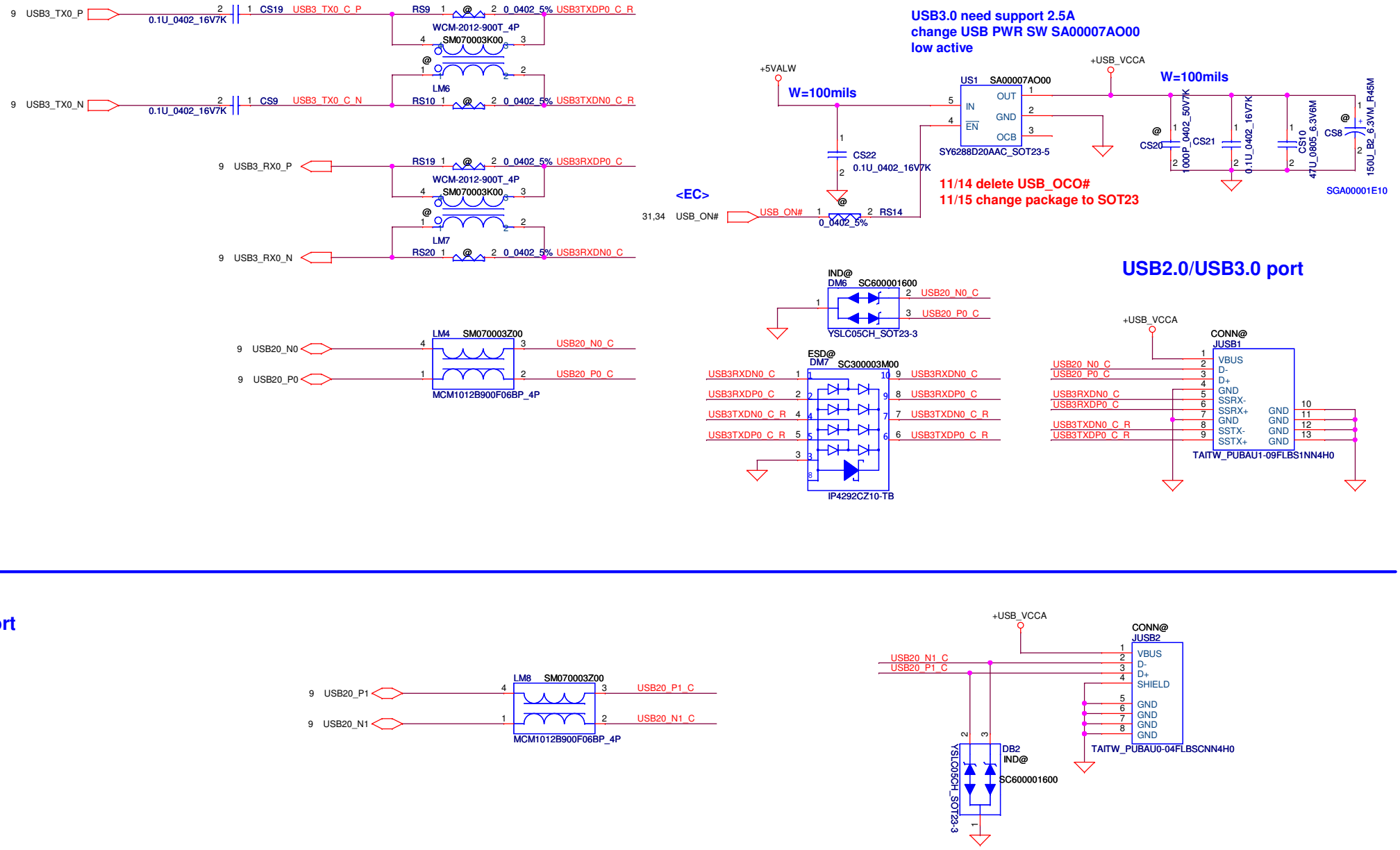
Compal Electronics, Inc.

Title: LAN 8111/8166

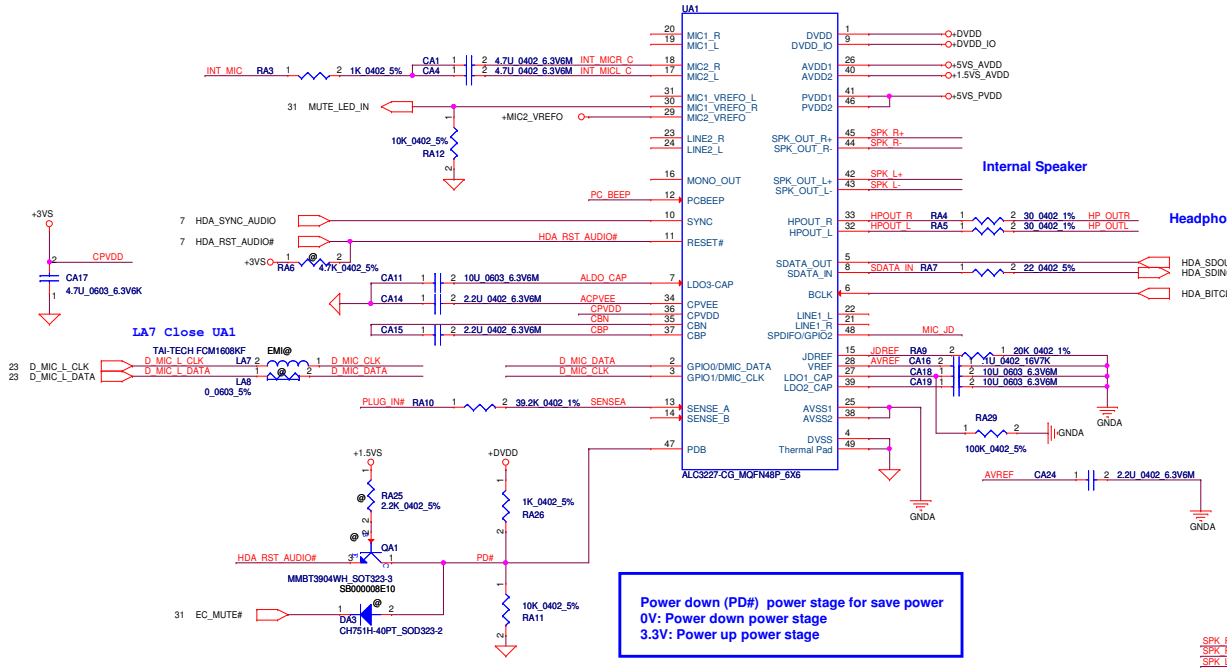
Size	Document Number	Rev
	LA-706P	0.1

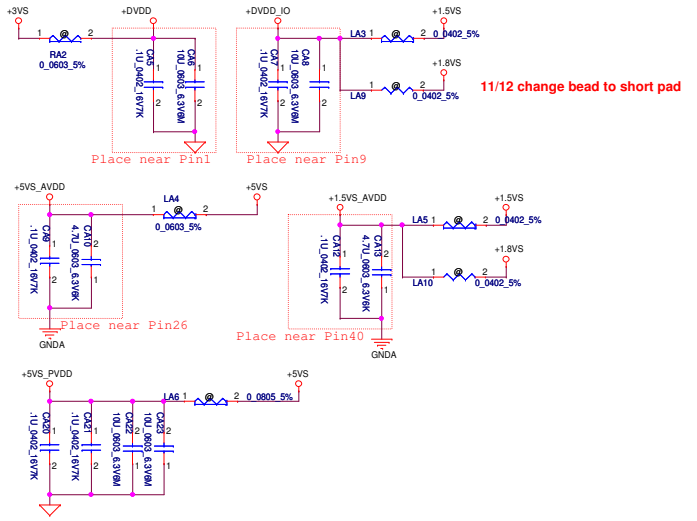
Date: Thursday, January 07, 2016 Sheet 27 of 51



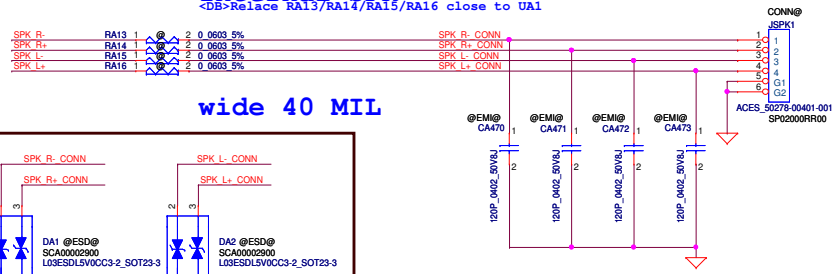
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/02/26	Deciphered Date	2015/07/08

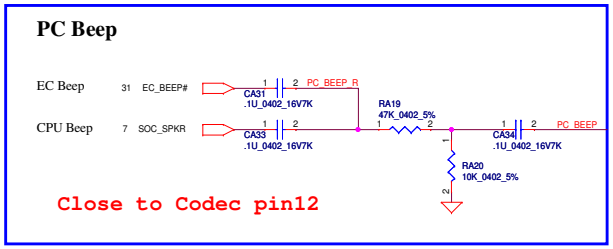
Title	USB 3.0/2.0 conn		
Size B	Document Number LA-706P		Rev 0.1
Date: Thursday, January 07, 2016	Sheet 28 of 51		

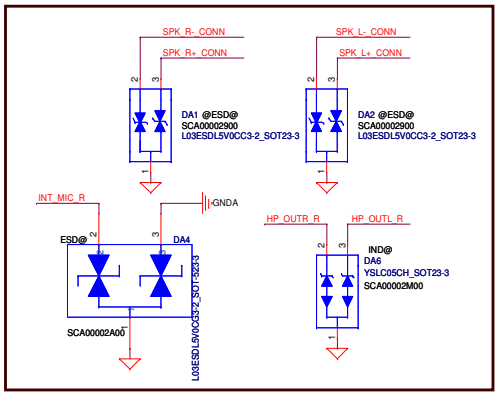


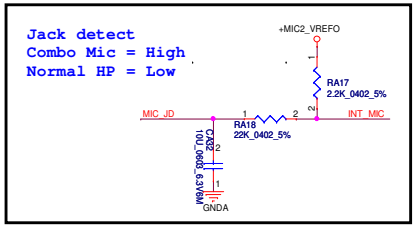


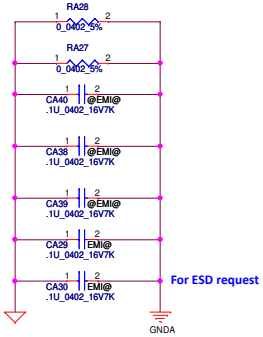
Reserve for ESD request.



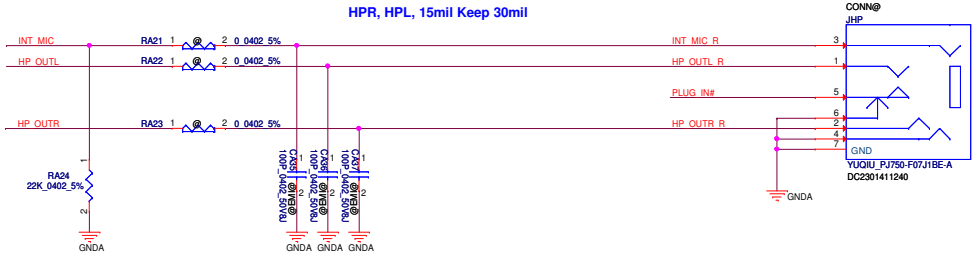


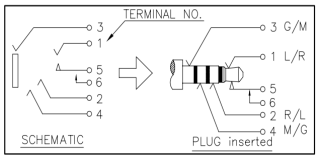






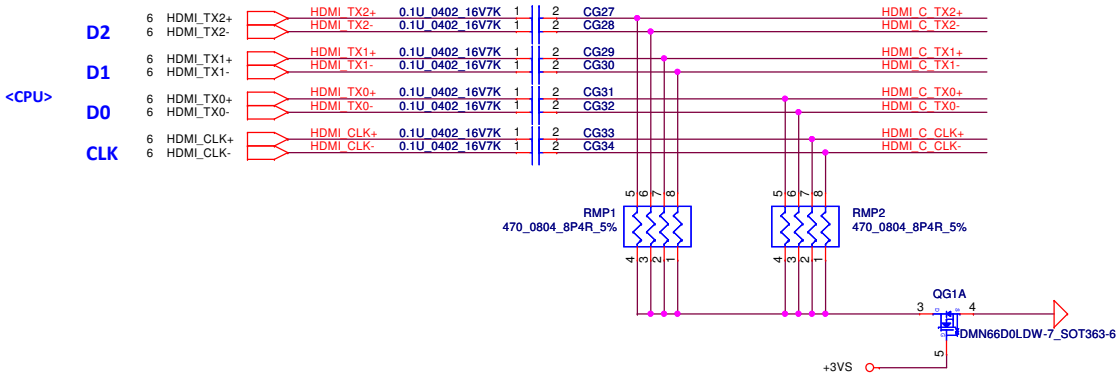
COMBO AUDIO JACK

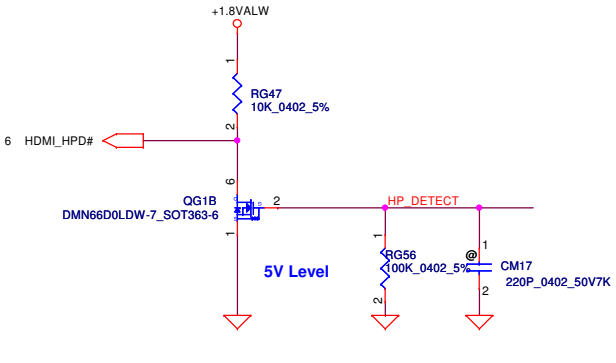


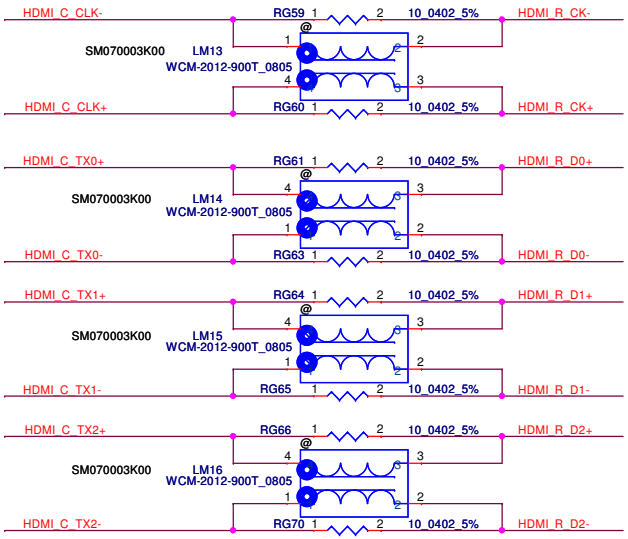


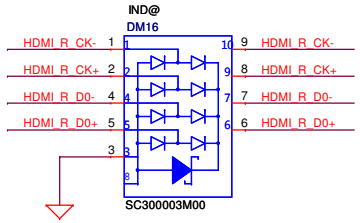
Security Classification	Compal Secret Data		
Issued Date	2013/01/04	Deciphered Date	2015/01/04

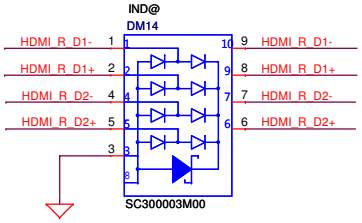
Compal Electronics, Inc.			
Title	AUDIO ALC259-VC2-CG		
Size C	Document Number LA-706P		Rev 0.1
Date: Thursday, January 07, 2016	Sheet 29 of 51		

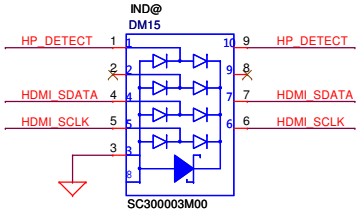


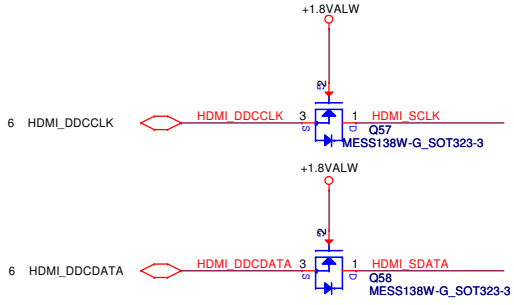


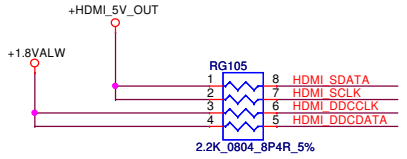




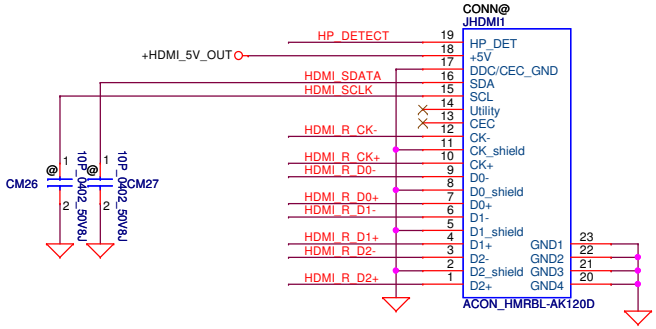


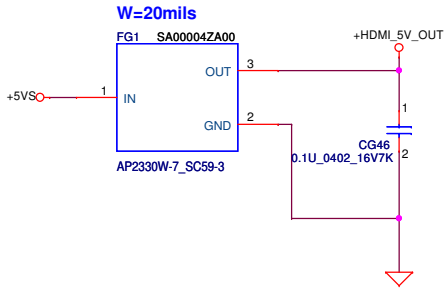






HDMI Conn.





Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: *HDMI_Conn/Level shift*

Size	Document Number	Rev
	LA-706P	0.1

Date: Thursday, January 07, 2016 | Sheet 30 of 51

NonTS	DB	SI	PV	MV
UMA R214	0 ohm	15k ohm	27K ohm	43K ohm
DIS R214	12k ohm	20k ohm	33k ohm	56k ohm

TS	DB	SI	PV	MV
UMA R214	75k ohm	130K ohm	200K ohm	270K ohm
DIS R214	100k ohm	160k ohm	240k ohm	330k ohm

Reserve EC_CLR_CMOS for clear CMOS

Latest design guide suggest change to 74LVC1G06.

ESD request

Pin117,123,127,121 For share ROM function

EC Image Loading into eFlash Mode

Security Classification	Compal Secret Data		
Issued Date	2014/08/21	Deciphered Date	2015/08/21

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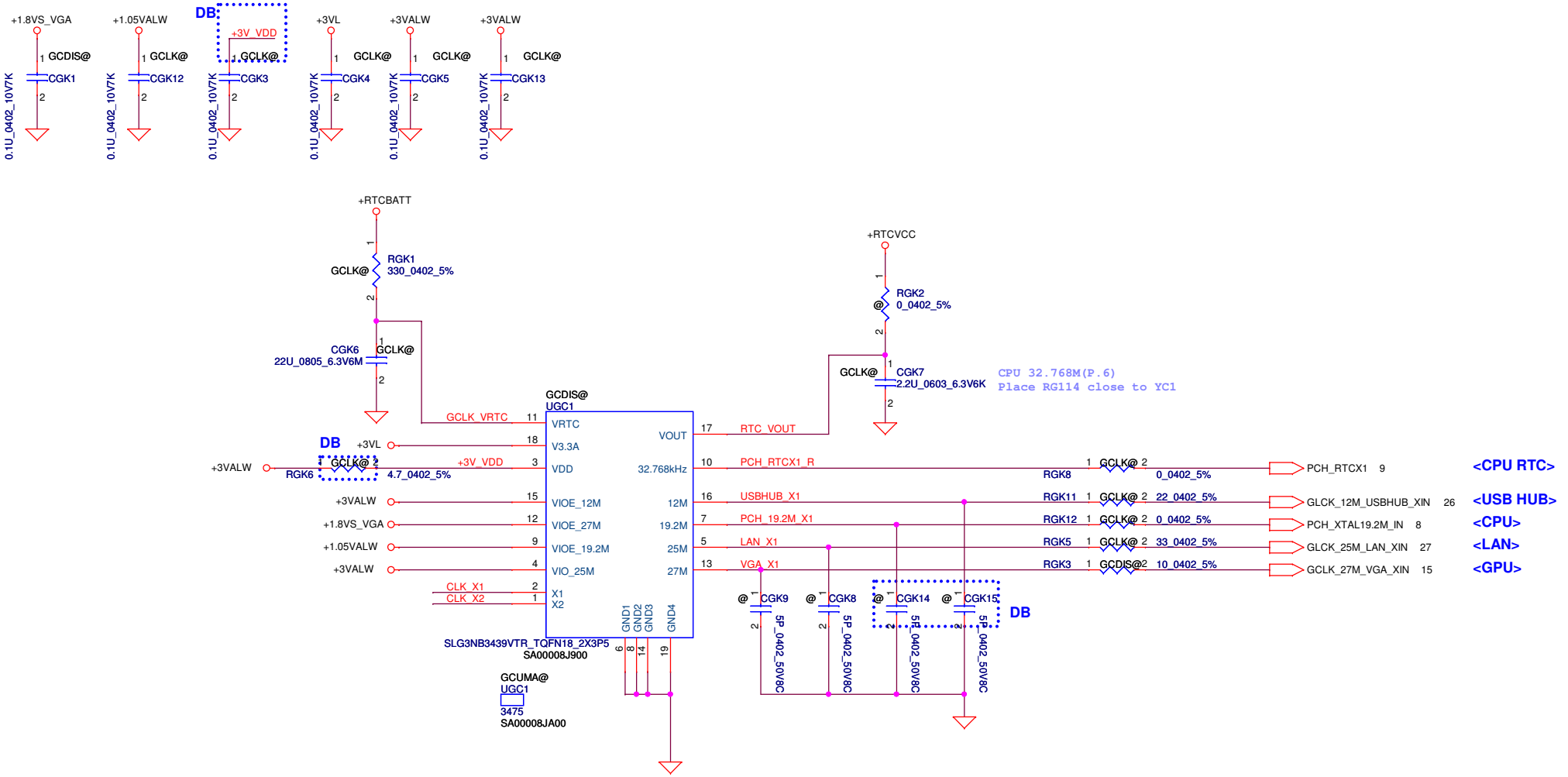
Compal Electronics, Inc.

Title: EC ENE KB9012/KB9022

Size	Document Number	Rev
C	LA-706P	0.1

Date: Thursday, January 07, 2016 | Sheet 31 of 51



Security Classification	Compal Secret Data		
Issued Date	2013/06/10	Deciphered Date	2014/07/01

Compal Electronics, Inc.

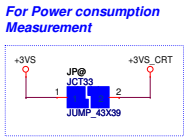
Title: **GCLK**

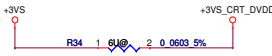
Size: | Document Number: **LA-706P** | Rev: 0.1

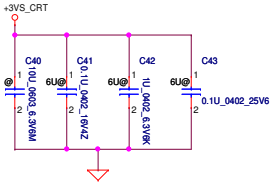
Date: Thursday, January 07, 2016 | Sheet 32 of 51

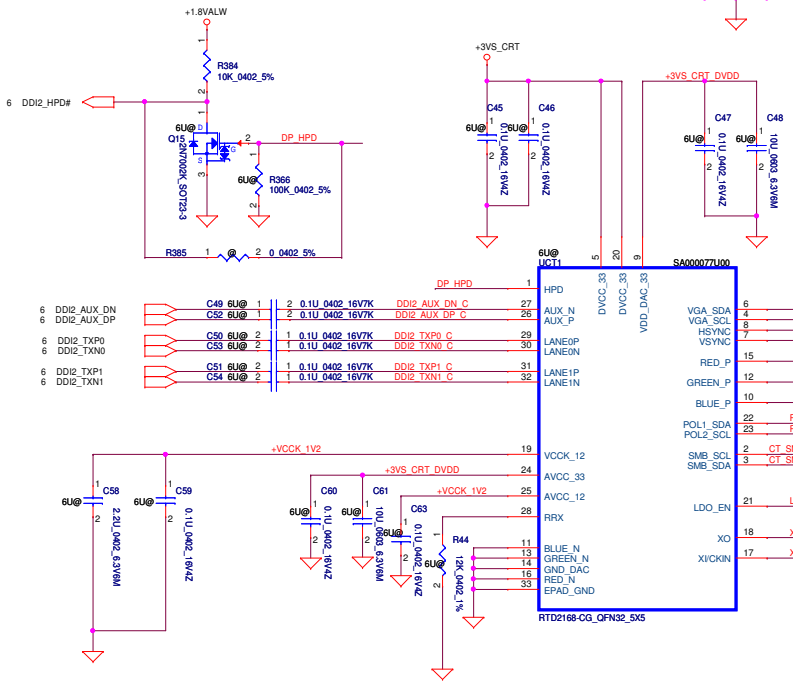
DP to CRT converter

For Power consumption Measurement

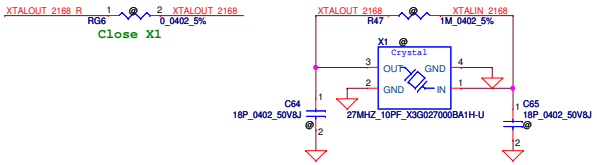


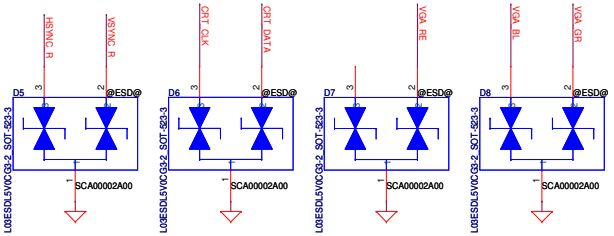






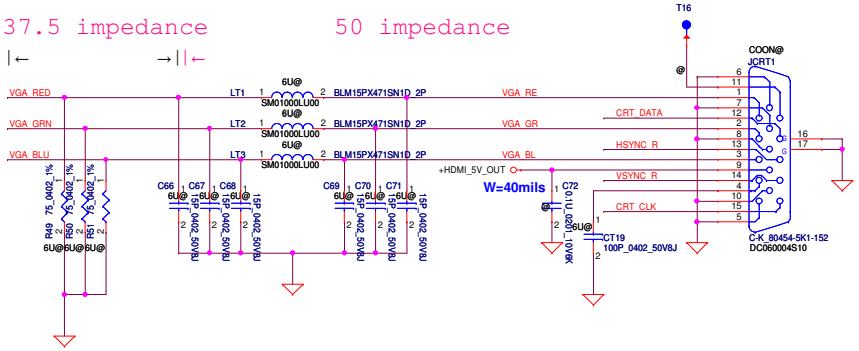
Close X1

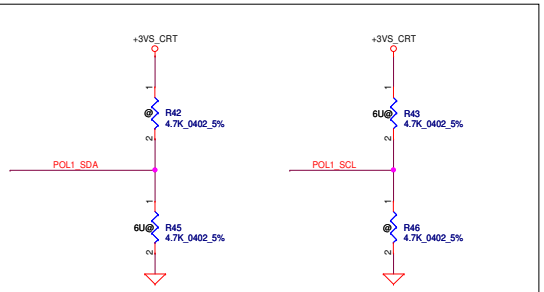




CRT Connector

37.5 impedance 50 impedance



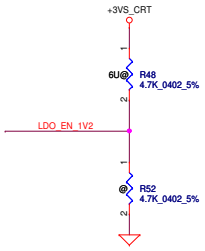


Mode Configure Table(Power On Latch)

		POL1_SDA(PIN22)	
		0	1
POL2_SCL(PIN23)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

RTD2168 Supports three operation mode for system design.
Reserve 4.7K resistor pull high/low for mode selection

ROM ONLY Mode : PIN22 pull low, PIN23 pull high
EP Mode : PIN22 pull high, PIN23 pull low
EEPROM Mode : PIN22 pull high, PIN23 pull high



Embedded LDO

Select VCCK_V12 source from external 1.2V or embedded LDO

LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO

Security Classification	Compal Secret Data		
Issued Date	2014/02/18	Deciphered Date	2015/02/20

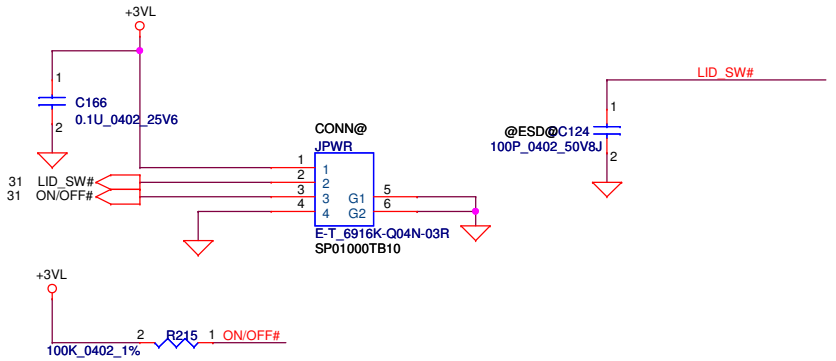
Compal Electronics, Inc.

Title: DP to CRT RTD2136

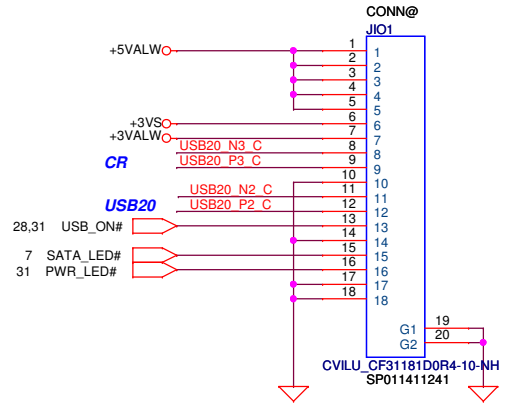
Size: C | Document Number: LA-706P | Rev: 0.1

Date: Thursday, January 07, 2016 | Sheet 33 of 51

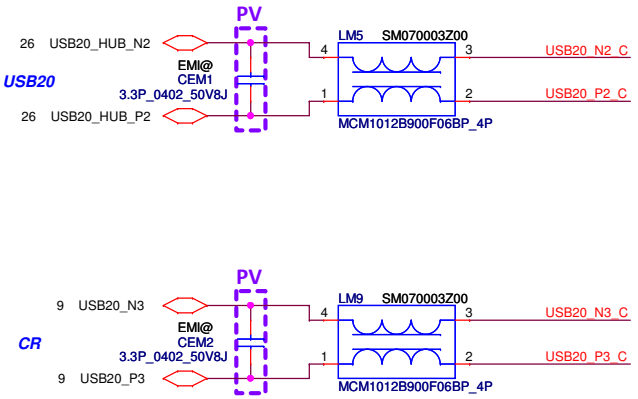
Powert Button Connector



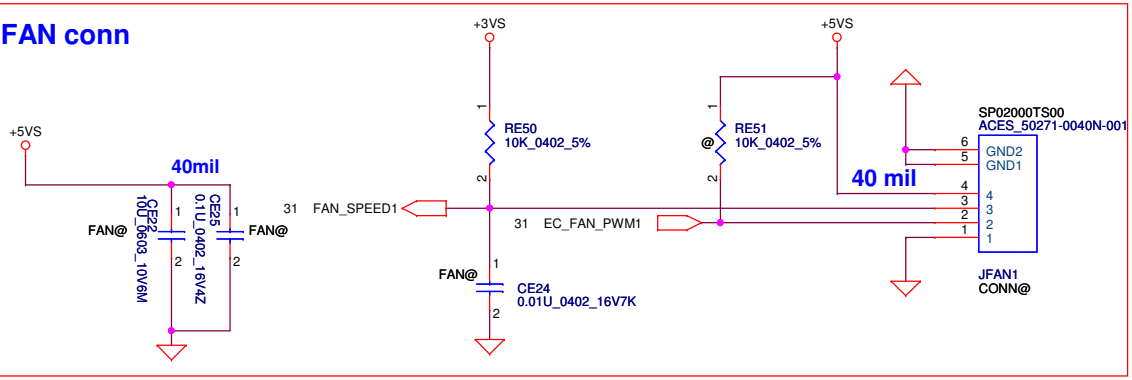
JIO S/B



CEM1,2 Close LM5/LM9



FAN conn

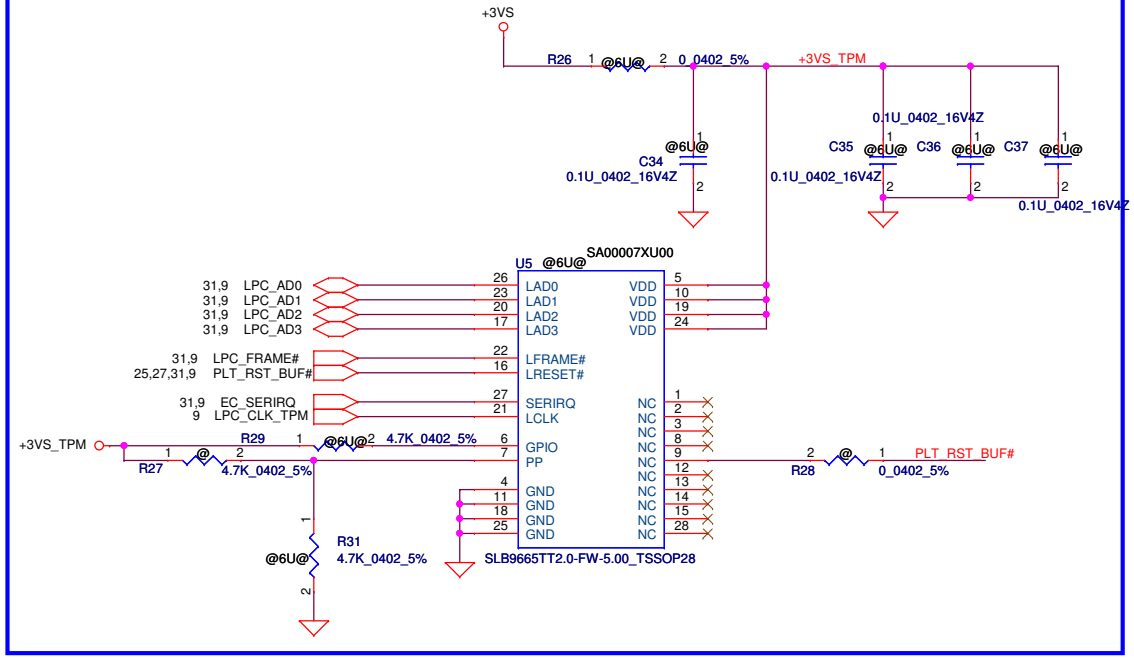


Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title	PWRBTN/FAN		
Size B	Document Number LA-706P		Rev 0.1
Date: Thursday, January 07, 2016	Sheet 34 of 51		

TPM2.0



H3 H_2P8 HOLEA
H4 H_2P5 HOLEA
H5 H_2P8 HOLEA
H6 H_2P5 HOLEA
H12 H_2P8 HOLEA
H8 H_2P5 HOLEA
H19 H_2P5 HOLEA
H20 H_2P5 HOLEA
H21 H_2P5 HOLEA
H24 H_2P4X3P0N HOLEA
H25 H_2P4X3P0N HOLEA
H26 H_2P4N HOLEA

VGA

H17 H_5P0 HOLEA
H18 H_5P0 HOLEA

CPU

H9 H_5P0 HOLEA
H10 H_5P0 HOLEA
H11 H_5P0 HOLEA
H13 H_5P0 HOLEA

FD1 FIDUCIAL_C40M80
FD2 FIDUCIAL_C40M80
FD3 FIDUCIAL_C40M80
FD4 FIDUCIAL_C40M80

Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

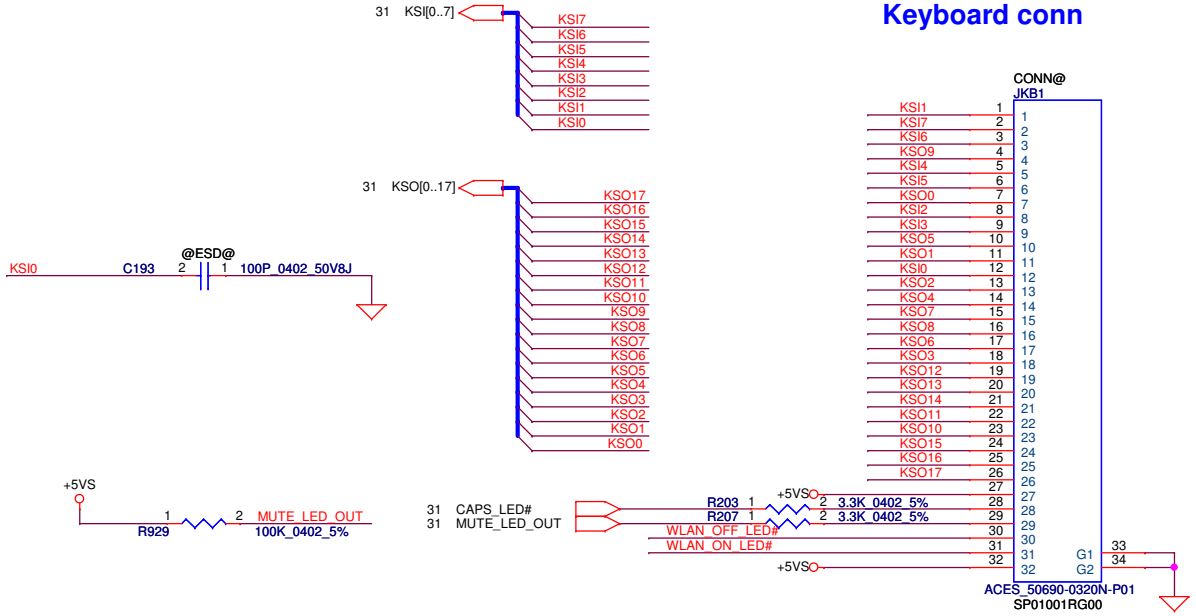
Compal Electronics, Inc.

Title: LED/Screw hole

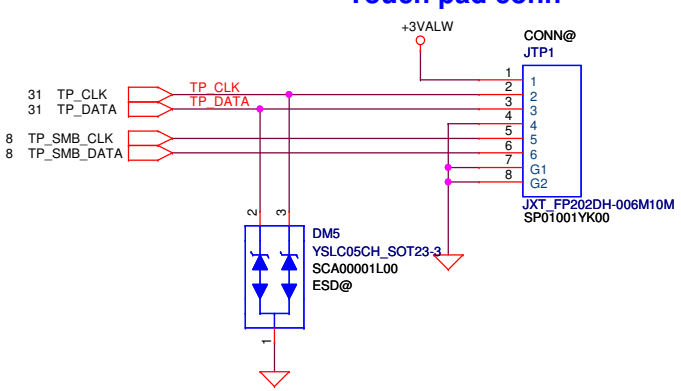
Size | Document Number: LA-706P | Rev: 0.1

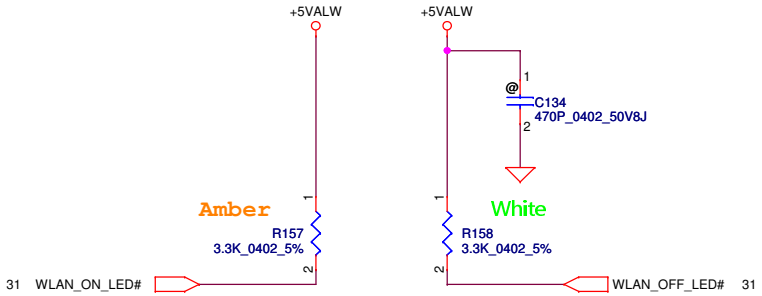
Date: Thursday, January 07, 2016 | Sheet 35 of 51

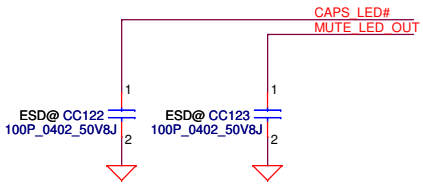
Keyboard conn



Touch pad conn







Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

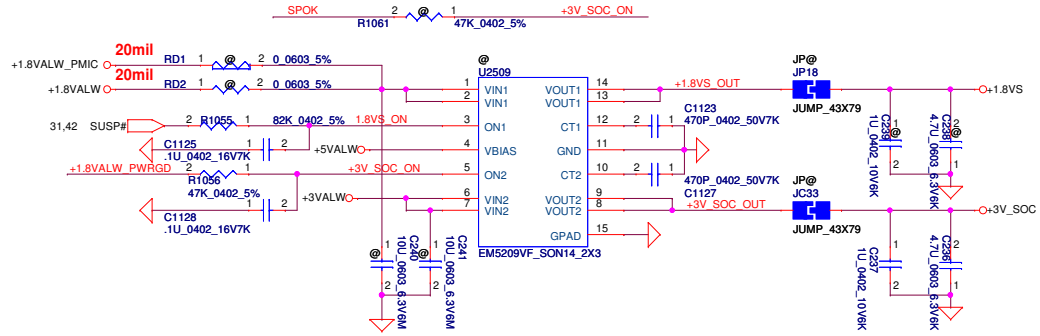
Compal Electronics, Inc.

Title: KB/TP

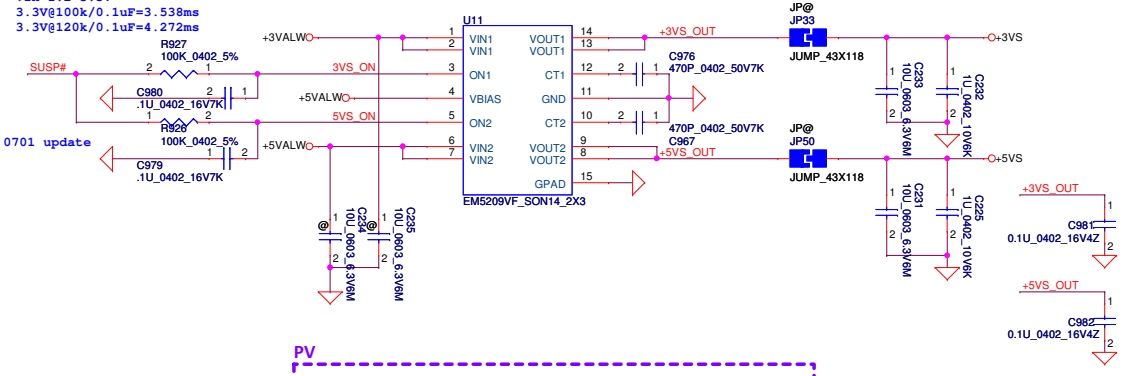
Size	Document Number	Rev
B	LA-706P	0.1

Date: Thursday, January 07, 2016 Sheet 36 of 51

VIH=1.2~5.5V
3.3V@82k/0.1uF=3.042ms
3.3V@47k/0.1uF=1.893ms

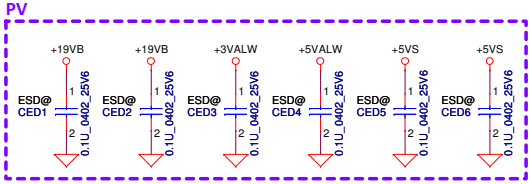


VIH=1.2~5.5V
3.3V@100k/0.1uF=3.538ms
3.3V@120k/0.1uF=4.272ms



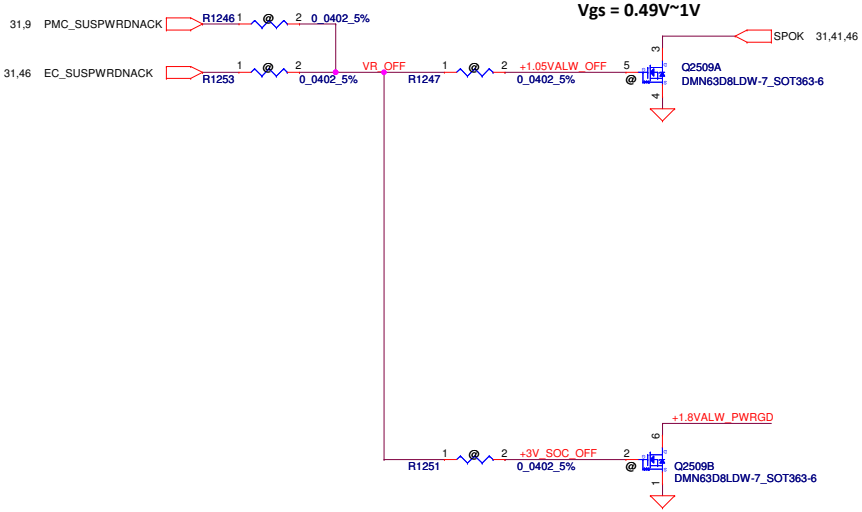
0701 update

PV

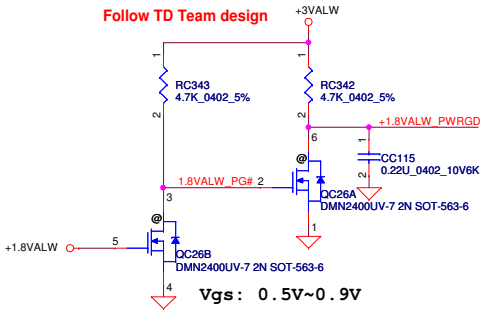


Power-off sequencing schematic

Q2509,Q2510,Q2511
Change to SB00000I200
Vgs = 0.49V~1V



Follow TD Team design



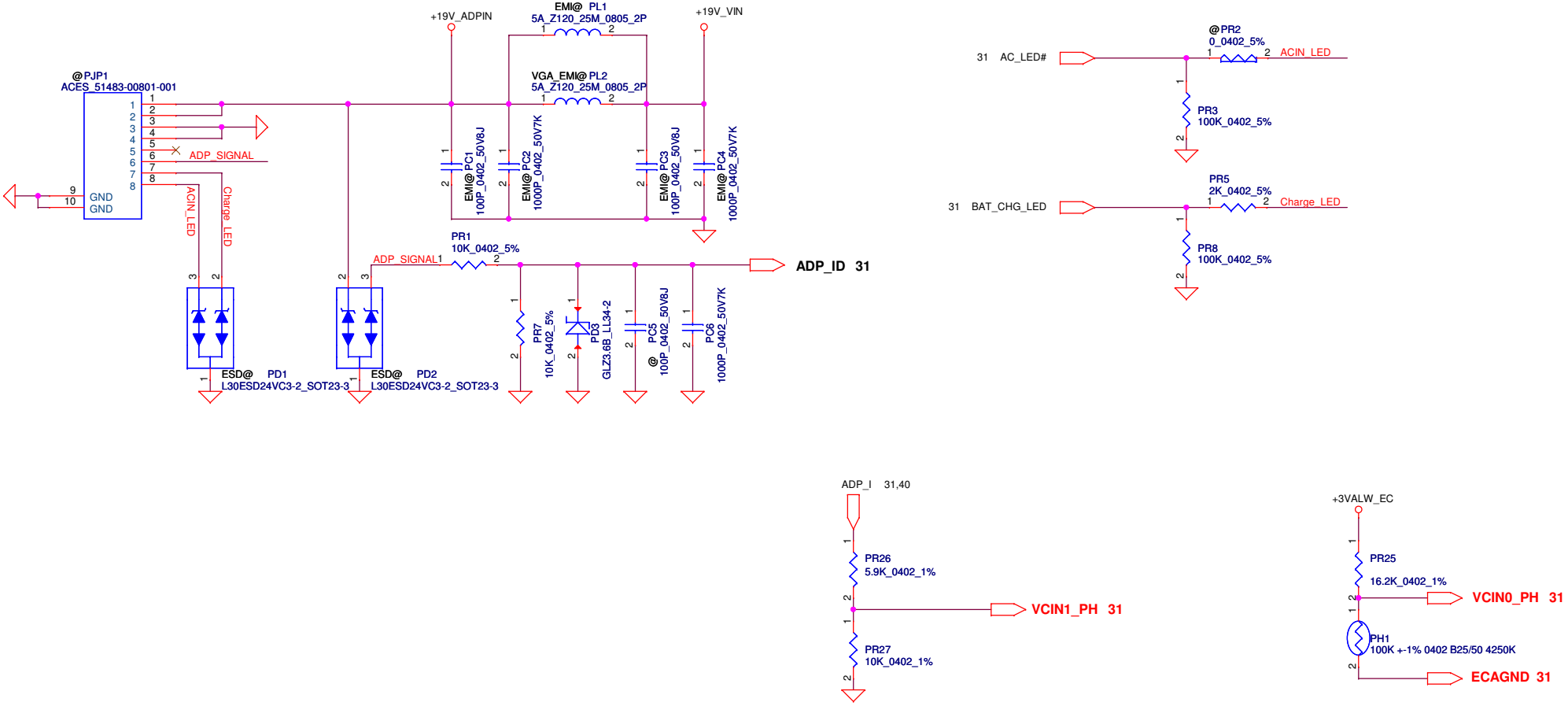
Security Classification	Compal Secret Data		
Issued Date	2014/07/07	Deciphered Date	2015/07/07

Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
Custom		0.1

Date: Thursday, January 07, 2016 Sheet 37 of 51



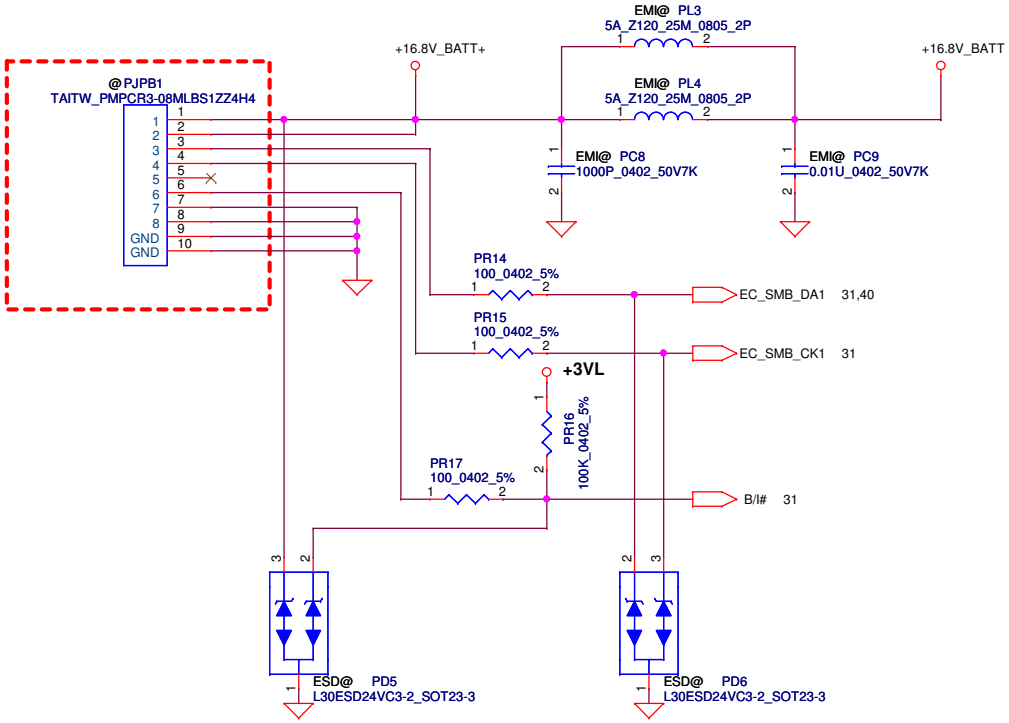
Security Classification	Compal Secret Data		
Issued Date	2015/10/08	Deciphered Date	2014/10/28

Compal Electronics, Inc.

Title: ***DC Conn***

Size | Document Number: **LA-C706P** | Rev: 0.1

Date: Thursday, January 07, 2016 | Sheet 38 of 52



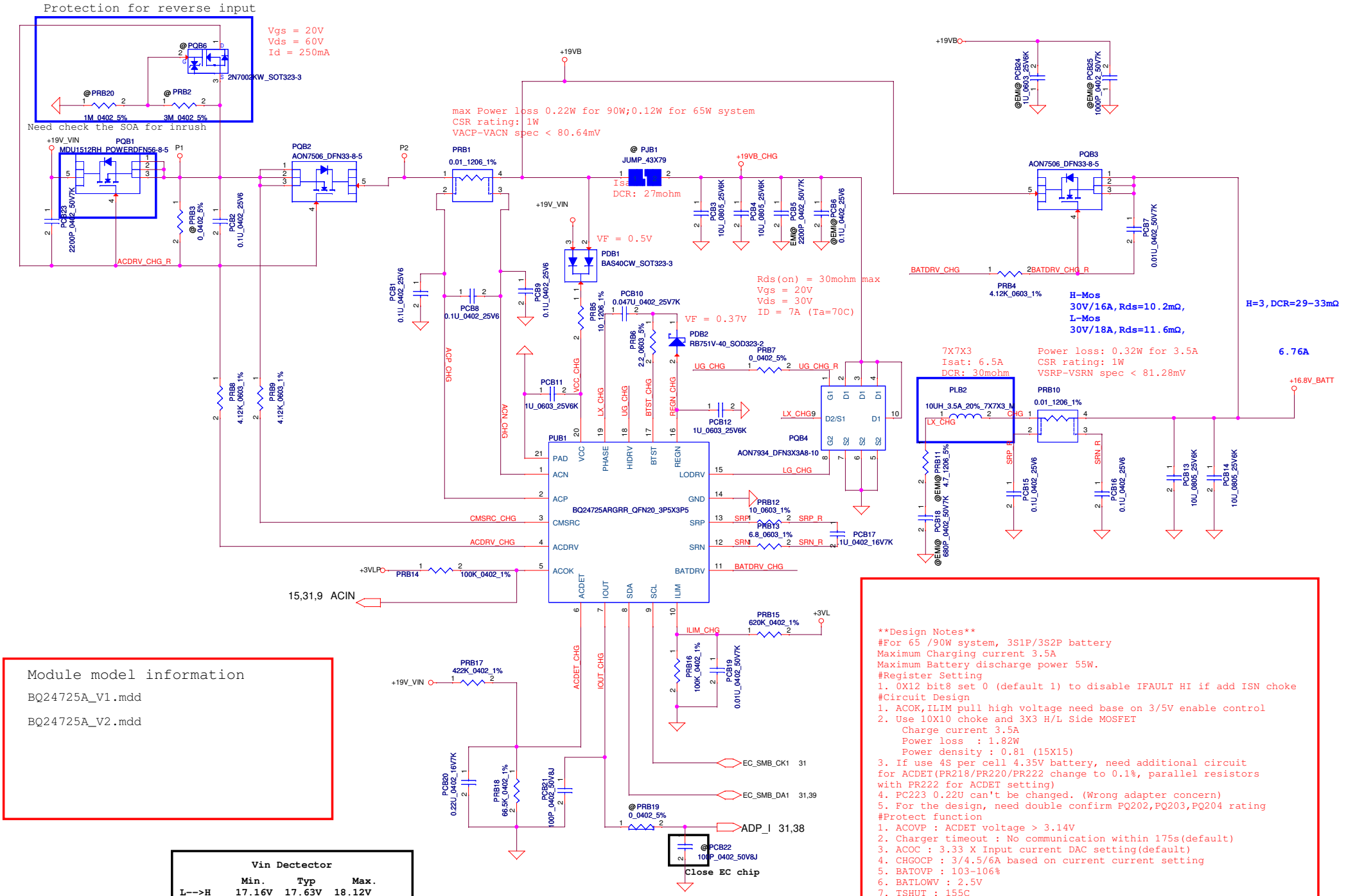
Security Classification	Compal Secret Data		
Issued Date	2015/10/08	Deciphered Date	2016/08/06

Compal Electronics, Inc.

Title: ***BATT Conn***

Size | Document Number: **LA-C706P** | Rev: 0.1

Date: Thursday, January 07, 2016 | Sheet 39 of 52



Module model information

BQ24725A_V1.mdd

BQ24725A_V2.mdd

Vin Dectector

	Min.	Typ	Max.
L-->H	17.16V	17.63V	18.12V
H-->L	16.76V	17.22V	17.70V

VILIM = 20*ILIM*Rsr
ILIM = 3.3*100/(100+107)/20/0.02
= 3.986 A

Design Notes
#For 65 /90W system, 3S1P/3S2P battery
Maximum Charging current 3.5A
Maximum Battery discharge power 55W.
#Register Setting
1. 0X12 bit8 set 0 (default 1) to disable IFAULT HI if add ISN choke
#Circuit Design
1. ACOK,ILIM pull high voltage need base on 3/5V enable control
2. Use 10X10 choke and 3X3 H/L Side MOSFET
Charge current 3.5A
Power loss : 1.82W
Power density : 0.81 (15X15)
3. If use 4S per cell 4.35V battery, need additional circuit for ACDET(PR218/PR220/PR222 change to 0.1%, parallel resistors with PR222 for ACDET setting)
4. PC223 0.22U can't be changed. (Wrong adapter concern)
5. For the design, need double confirm PQ202,PQ203,PQ204 rating
#Protect function
1. ACOVP : ACDET voltage > 3.14V
2. Charger timeout : No communication within 175s(default)
3. ACOC : 3.33 X Input current DAC setting(default)
4. CHGOCP : 3/4.5/6A based on current current setting
5. BATOVP : 103-106%
6. BATLOWV : 2.5V
7. TSHUT : 155C
8. IFAULT HI : 750mV (default)
9. IFAULT LOW : 150mV (default)

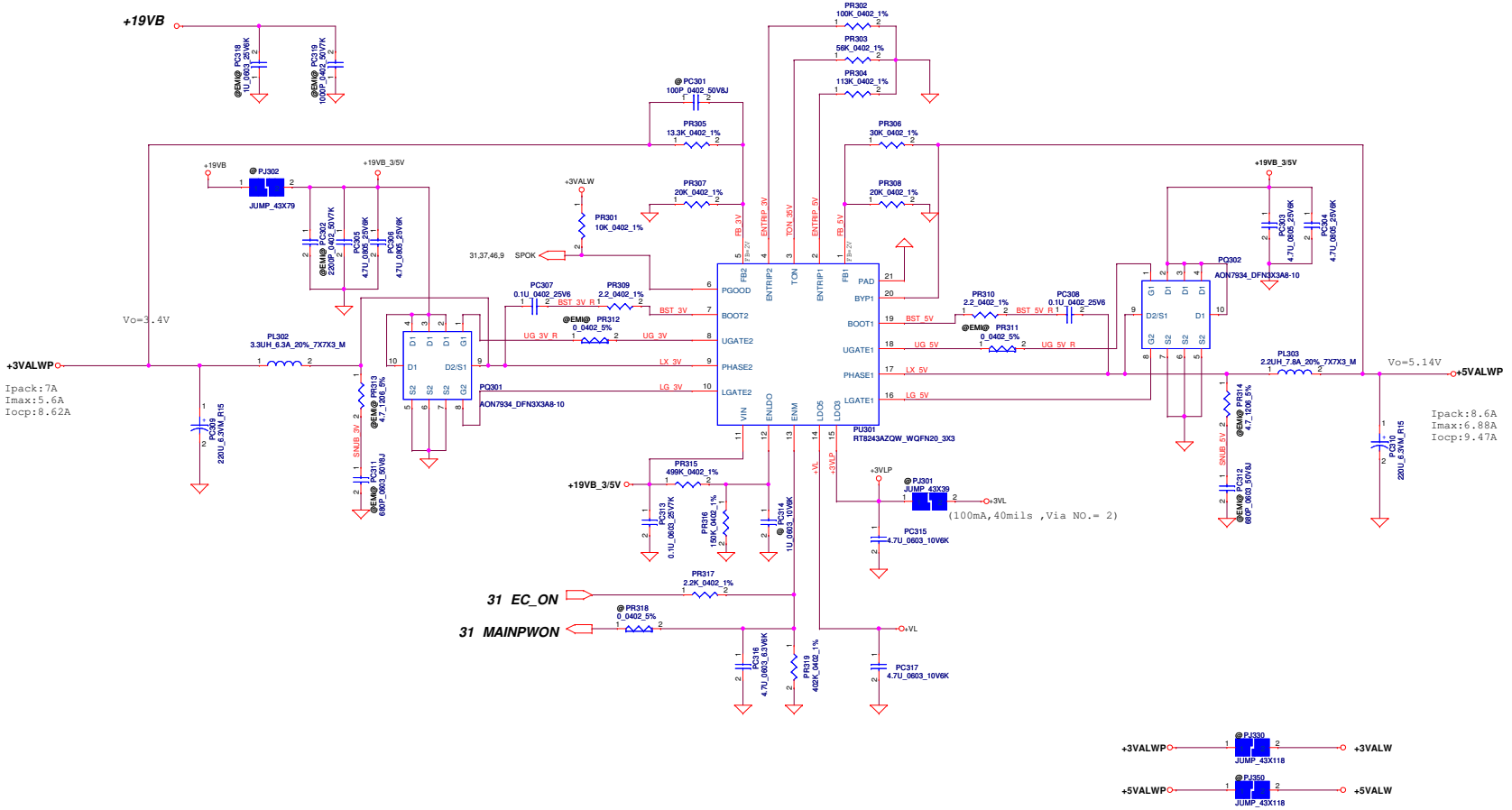
Security Classification	Compal Secret Data		
Issued Date	2015/10/08	Deciphered Date	2012/07/02

Compal Electronics, Inc.

Title: CHARGER

Size | Document Number: Intel / Braswell | Rev: 0.1

Date: Thursday, January 07, 2016 | Sheet 40 of 52

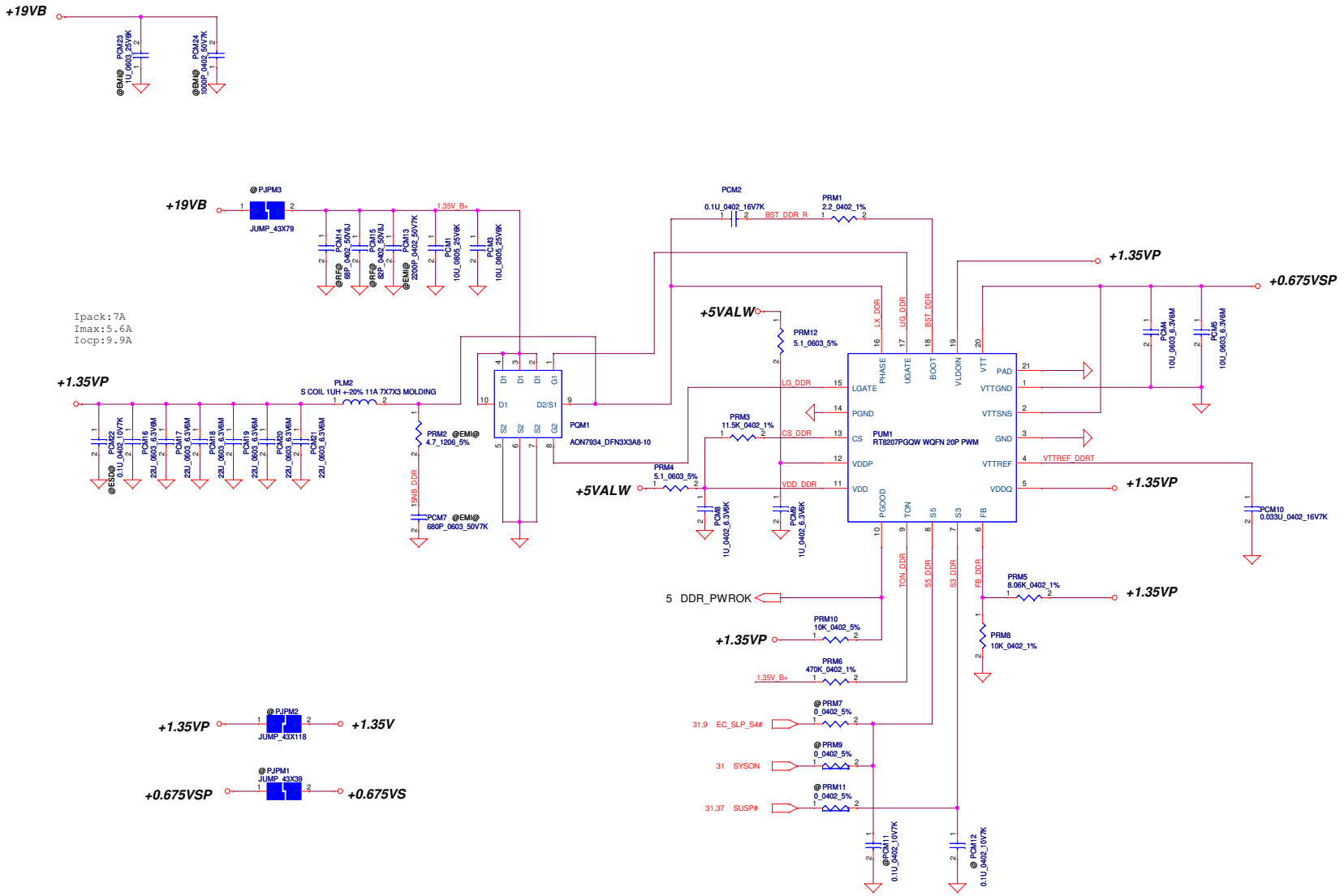


Security Classification	Compal Secret Data		
Issued Date	2015/10/08	Deciphered Date	2016/08/06

Compal Electronics, Inc.

Title: *3VALW/5VALW*

Size	Document Number	Rev
A2	*Intel / Braswell*	0.1
Date:	Sheet 41 of 52	



Security Classification	Compal Secret Data		
Issued Date	2015/10/08	Deciphered Date	2014/10/28

Compal Electronics, Inc.

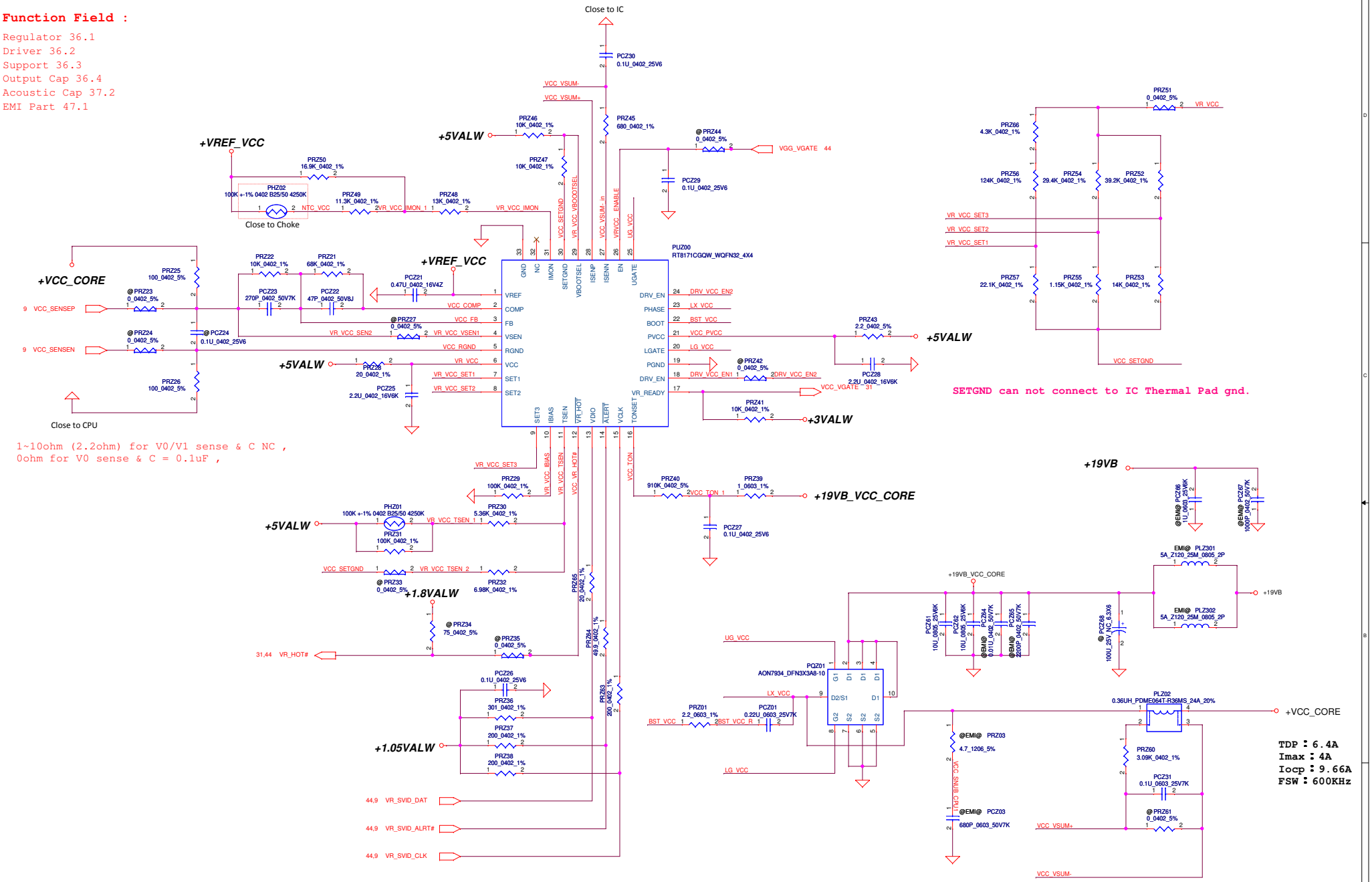
Title: 1.35V/0.675VS

Size: C | Document Number: Intel / Braswell | Rev: 0.1

Date: Thursday, January 07, 2016 | Sheet 42 of 52

Function Field :

Regulator 36.1
Driver 36.2
Support 36.3
Output Cap 36.4
Acoustic Cap 37.2
EMI Part 47.1



TDP : 6.4A
Imax : 4A
Iocp : 9.66A
FSW : 600KHz

Security Classification	Compal Secret Data		
Issued Date	2015/10/08	Deciphered Date	2013/07/10

Compal Electronics, Inc.

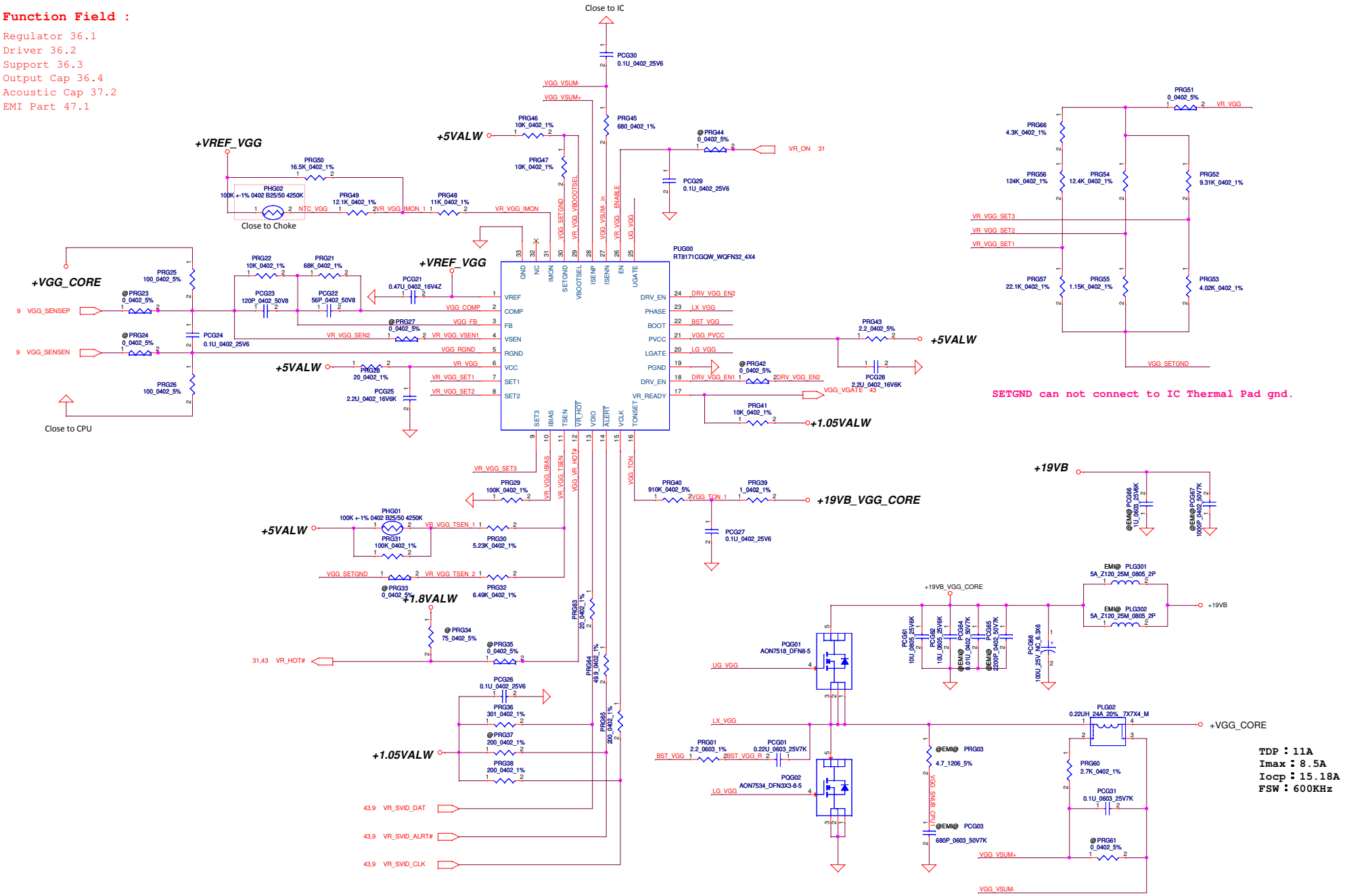
Title: *VCC_Core*

Size: C | Document Number: *Intel / Braswell* | Rev: 0.1

Date: | Sheet 43 of 52

Function Field :

Regulator 36.1
Driver 36.2
Support 36.3
Output Cap 36.4
Acoustic Cap 37.2
EMI Part 47.1



Security Classification	Compal Secret Data		
Issued Date	2015/10/08	Deciphered Date	2013/07/10

Compal Electronics, Inc.

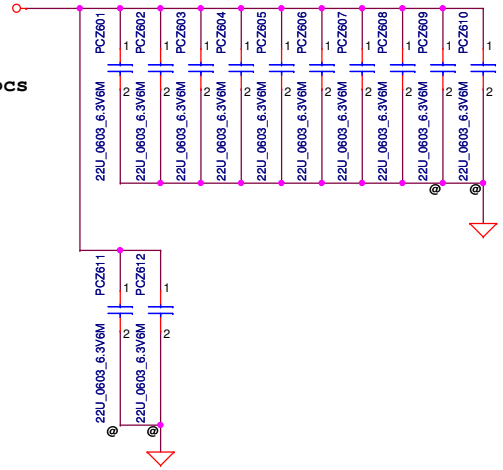
Title: *VGG_Core*

Size: C | Document Number: *Intel / Braswell* | Rev: 0.1

Date: | Sheet 44 of 52

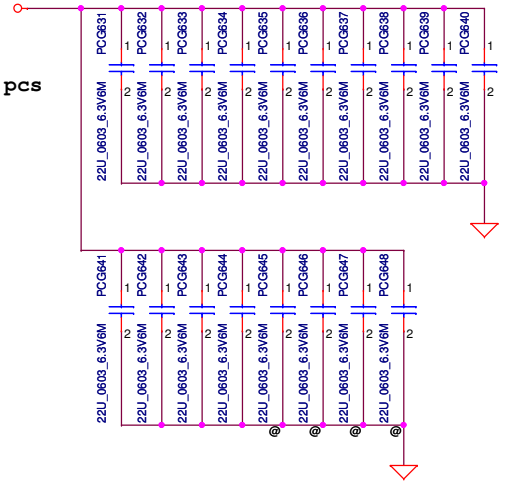
+VCC_CORE

22U_0603
8 pcs + @ x 4 pcs



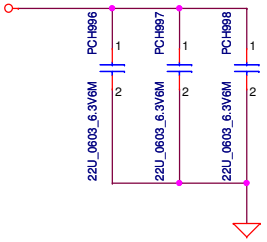
+VGG_CORE

22U_0603
14 pcs + @ x 4 pcs

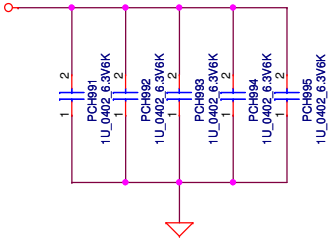


+1.05_VNN

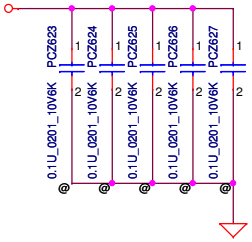
22U_0603 *3pcs



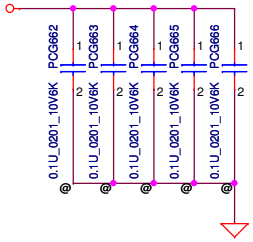
+1.05_VNN



+VCC_CORE



+VGG_CORE



Security Classification	Compal Secret Data		
Issued Date	2015/10/08	Deciphered Date	2015/07/08

Compal Electronics, Inc.

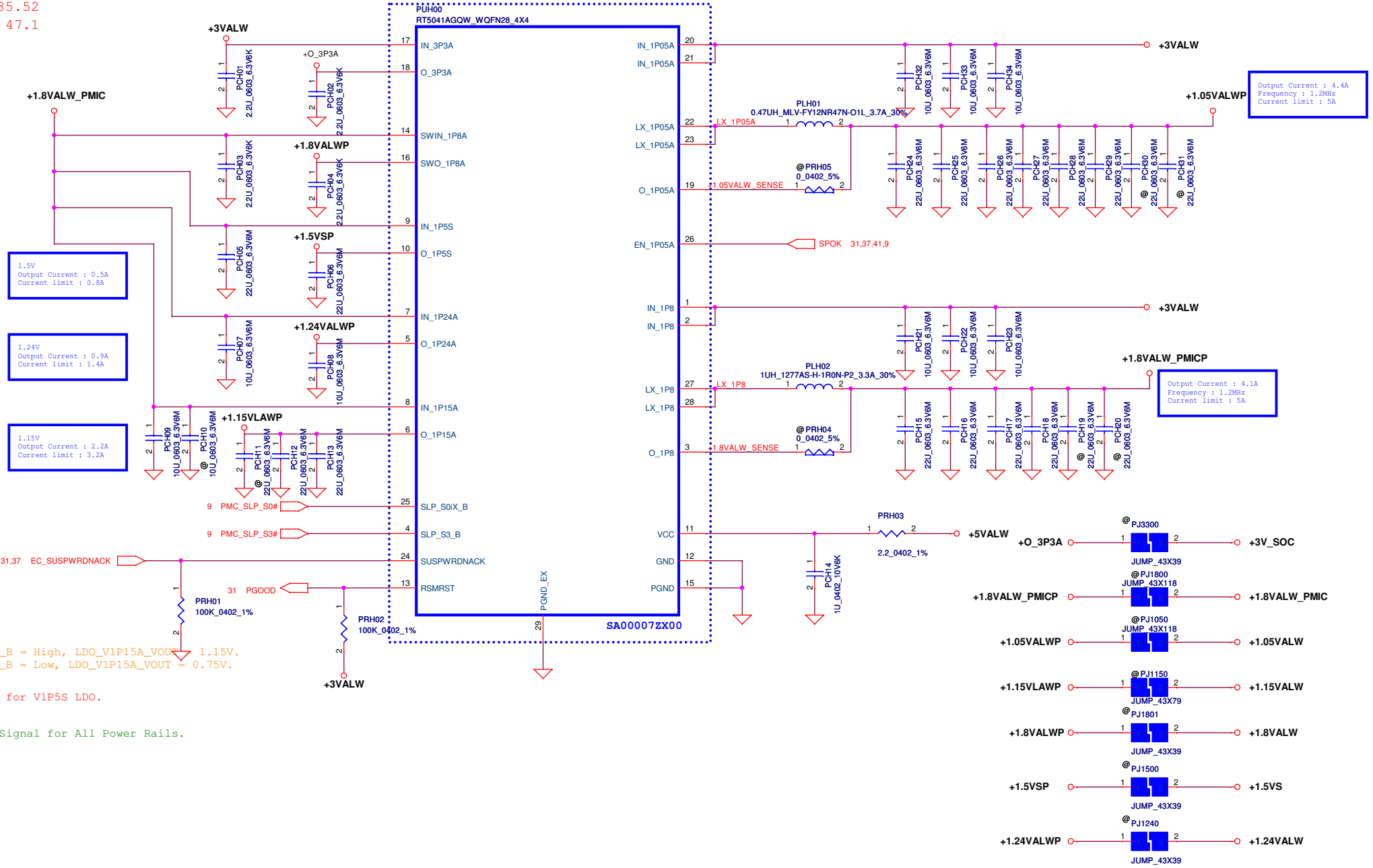
Title: PWR-PROCESSOR DECOUPLING

Size	Document Number	Rev
A3	LA-C706P	0.1

Date: Thursday, January 07, 2016 | Sheet 45 of 52

Function Field :

Regulator 35.51
Support 35.52
EMI Part 47.1



SLP_S0iX_B
When SLP_S0iX_B = High, LDO_V1P15A_VOUT = 1.15V.
When SLP_S0iX_B = Low, LDO_V1P15A_VOUT = 0.75V.

SLP_S3_B
Enable Signal for V1P5S LDO.

SUSPWRDNACK
HIGH:Disable Signal for All Power Rails.

Security Classification	Compal Secret Data		
Issued Date	2015/10/08	Deciphered Date	2013/09/17

Compal Electronics, Inc.

Title: PWR-MOIC SYSTEM

Size	Document Number	Rev
A3	LA-C706P	0.1

Date: Thursday, January 07, 2016 Sheet 46 of 52

APU_core
TDC 31A(1H1L) *2phase
Peak Current 46.5A
FSW=300kHz
DCR 0.98mohm +/-5%

Maximum Current: 28A(TDC)
load line:1m ohm
slew rate:50mV/uS

PHV2 is next to PLV2

PUV1 VGA@
RT8880CGQW_WQFN52_6X6

Security Classification	Compal Secret Data		
Issued Date	2015/10/08	Deciphered Date	2013/03/19

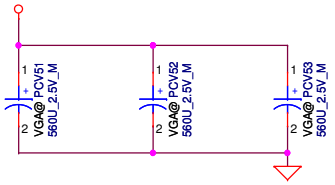
Compal Electronics, Inc.

Title: VGA_Core(RT8880AGQW)

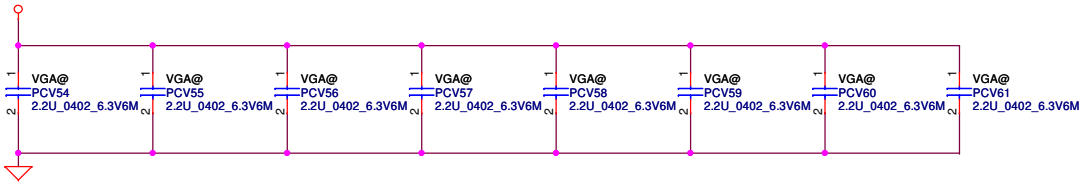
Size	Document Number	Rev
		0.1

Date: Thursday, January 07, 2016 Sheet 47 of 52

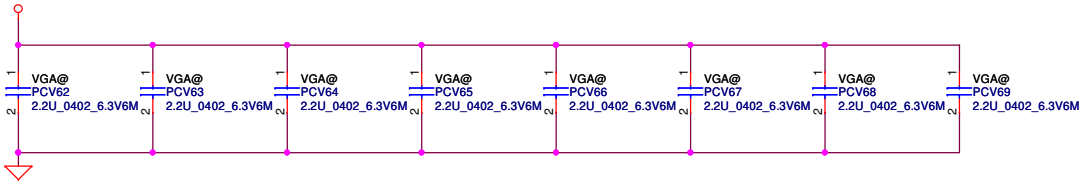
+VGA_CORE



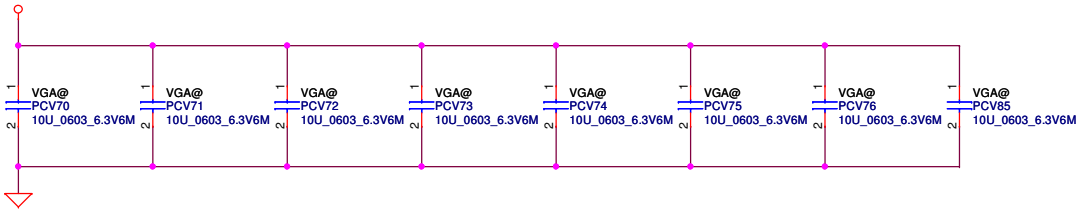
+VGA_CORE



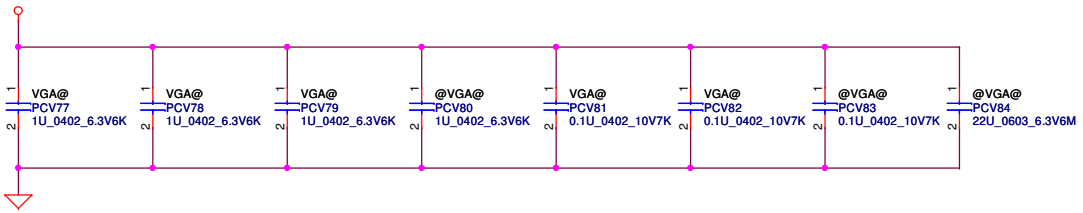
+VGA_CORE



+VGA_CORE



+VGA_CORE



Security Classification	Compal Secret Data		
Issued Date	2015/10/08	Deciphered Date	2016/09/30

Compal Electronics, Inc.

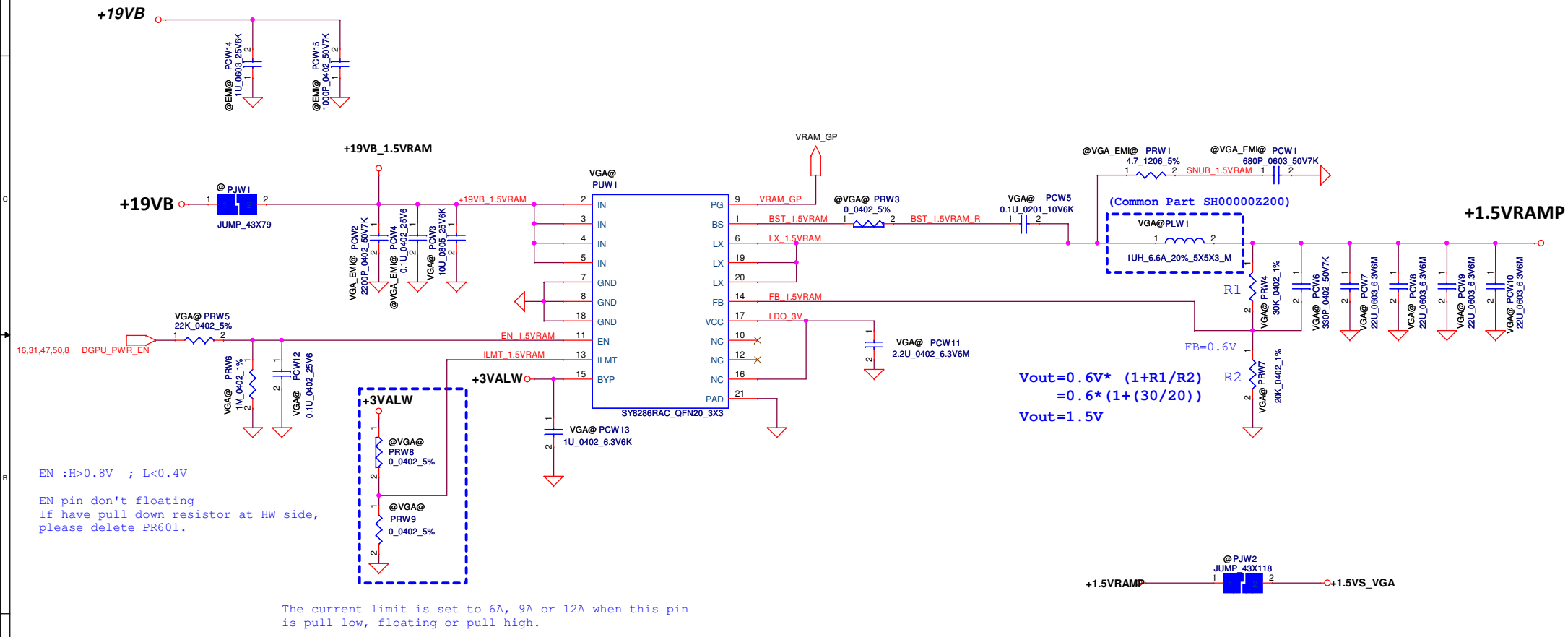
Title: *VGA CHIP DECOUPLING*

Size	Document Number	Rev
	LA-C706P	0.1

Date: Thursday, January 07, 2016 | Sheet 48 of 52

Module model information

SY8286_V1_single.mdd
SY8286_V1_dual.mdd



EN :H>0.8V ; L<0.4V

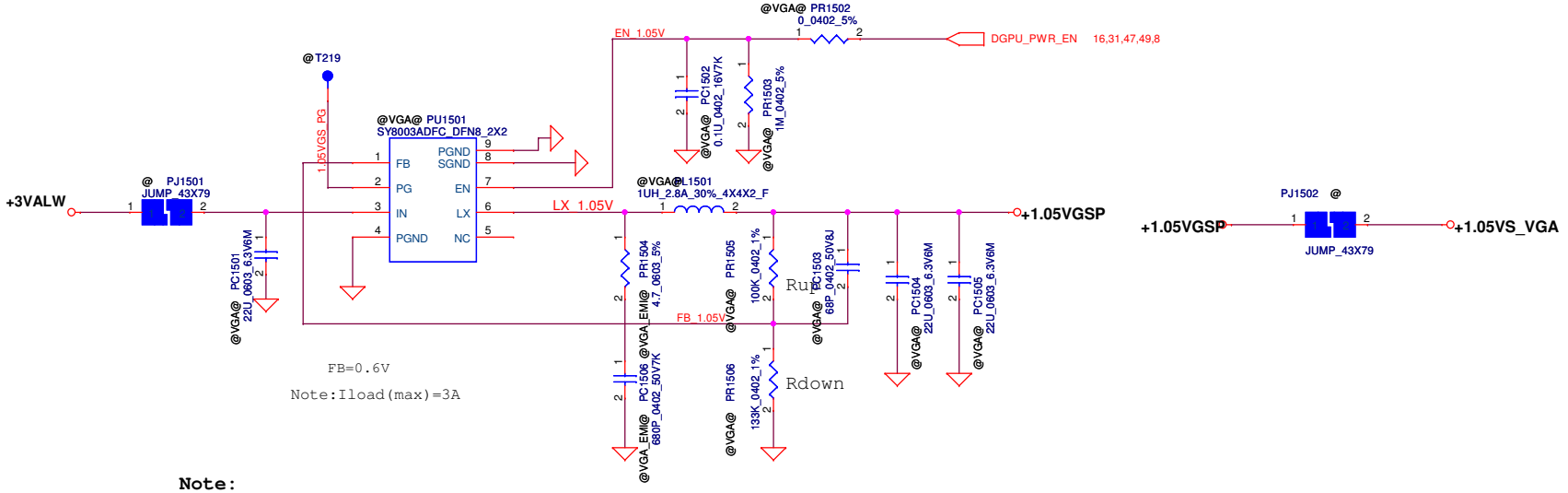
EN pin don't floating
If have pull down resistor at HW side, please delete PR601.

The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high.

Security Classification	Compal Secret Data			APS55 Compal Electronics, Inc.
Issued Date	2015/10/08	Deciphered Date	2014/05/26	Title: VRAM_1V5_GPU
				Size: A3 / Document Number: LA-C706P / Rev: 0.1
				Date: Thursday, January 07, 2016 / Sheet 49 of 52

Module model information

SY8003_V2.mdd



Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

Vout=0.6V* (1+Rup/Rdown)

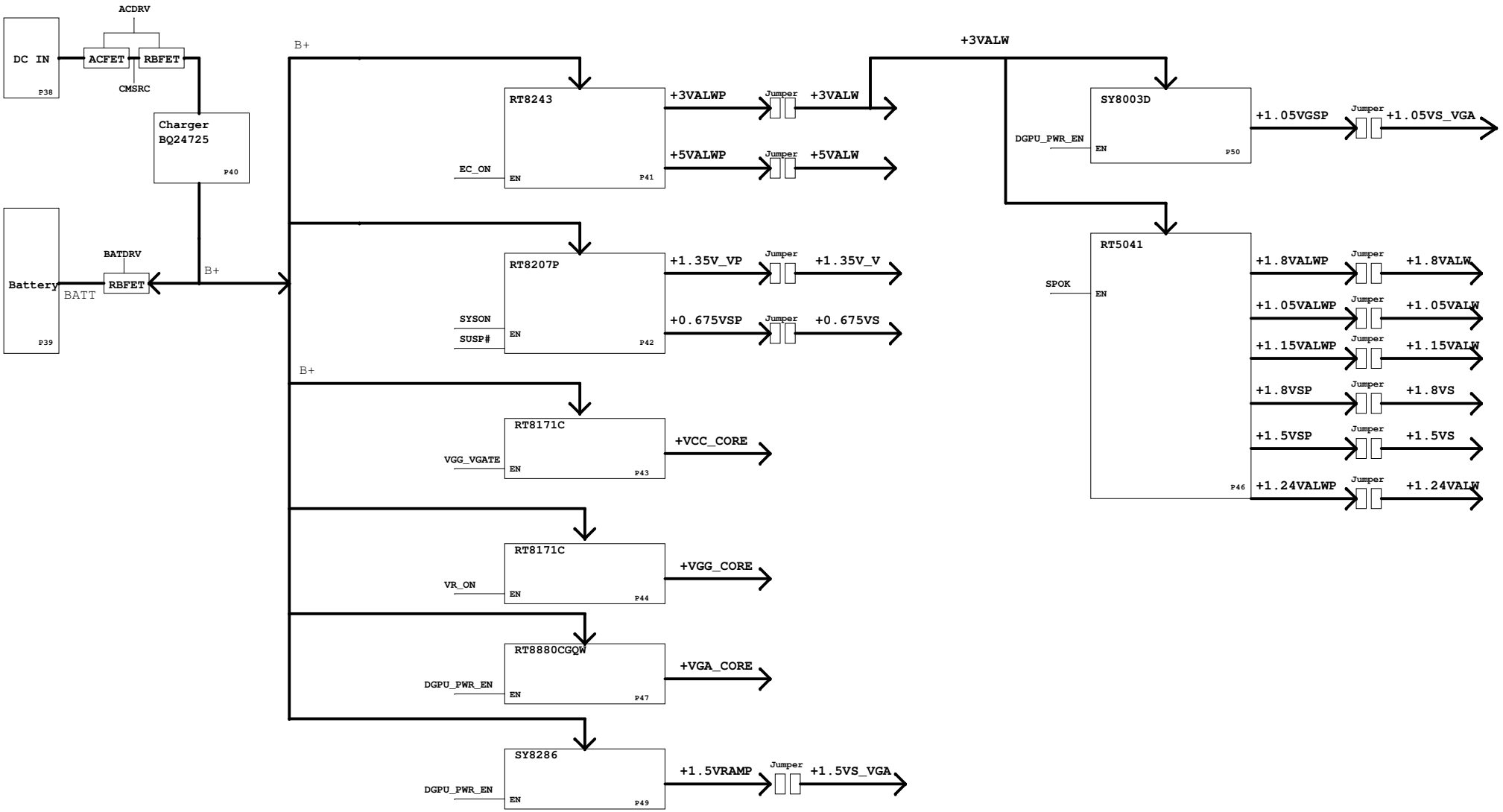
Note:Use VCCSA_SEL to switch High & Low Level for VID[1]
(ie. VCCSA_SEL) due to the VID[0] is don't care for this setting.

Security Classification	Compal Secret Data		
Issued Date	2015/10/08	Deciphered Date	2012/06/13

Title: **1.05V(SY8003)**

Size	Document Number	Rev
A3	*Intel / Braswell*	0.1

Date: Thursday, January 07, 2016 | Sheet 50 of 52



Security Classification	Compal Secret Data		
Issued Date	2015/10/08	Deciphered Date	2014/10/28

Compal Electronics, Inc.

Title: ***Power Block Diagram***

Size | Document Number: **LA-C706P** | Rev: 0.1

Date: Thursday, January 07, 2016 | Sheet 51 of 52

Version change list (P.I.R. List)

Item	Date	Page	Reason for change	Modify List	Phase
1	11/16	P47	EE request for VGA power debug	Change PRV61 to stuff & PRV1/PCV102 to Unpop	SI
2	11/16	P47	EE request for VGA power debug	Add PRV2 for EE debug sequence issue	SI
3	11/24	P44	EMI request for debug	remove PJG1 & add PLG301/ PLG302	SI
4	11/24	P52	EE request for VGA power debug	Change PRW5 0 ohm --> 22K & PCW12 0.1U to stuff	SI
5	11/24	P43	EMI request for debug	remove PJZ1 & add PLZ301/ PLZ302	SI
6	12/29	P47	Modify OCP value	Change PRV73 1K-->11K, PRV71 124K-->64.9K PRV75 2.8K-->8.66K	PV
7	12/29	P40,P42	Diner cost down item	Change PCB17, PCM4 0603 to 0402, PCM5 0805 to 0603	PV
8	12/30	P43, P44, P47	Change 0 ohm to short pad	PRZ51, PRG51, PRV28, PRV29, PRV45, PRV48, PRV50, PRV2	PV
9	1/7	P49	Change 0 ohm to short pad	PRW8	PV
10					
11					
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21					

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	
Title: PIR List			
Size: Custom	Document Number: Intel / Braswell		Rev: 0.1
Date: Thursday, January 07, 2016		Sheet 52 of 52	