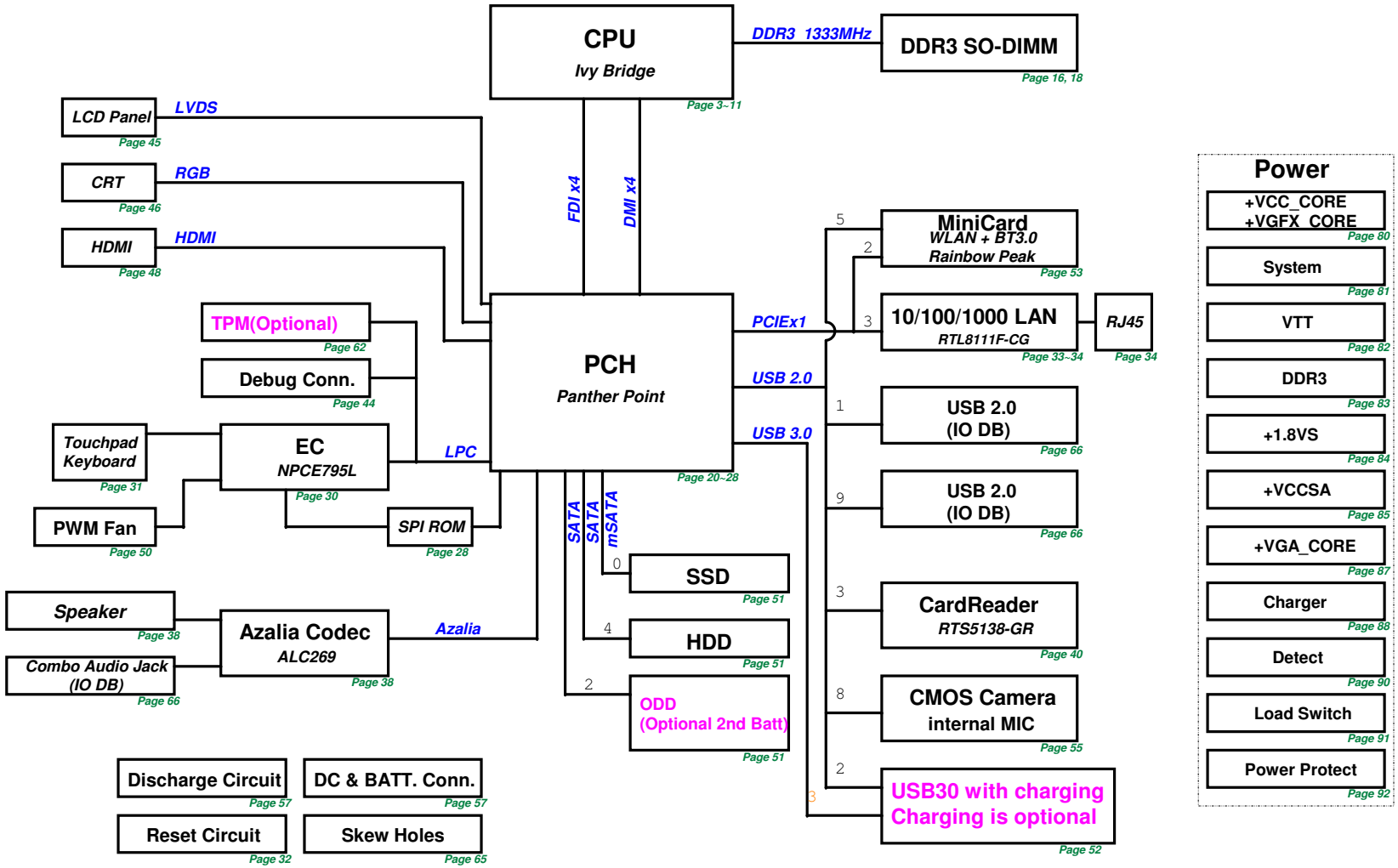
SYSTEM PAGE REF.

B34Y Chief River Platform(TACOMA FALL2) Rev 1.2

BLOCK DIAGRAM



PEGATRON Title : Block Diagram
BG1-HW RD Div.2-NB RD Dept.5 Engineer: Trunks Chen
Size: Custom | Project Name: B34 | Rev: 1.0
Date: Wednesday, February 01, 2012 | Sheet 1 of 59

PCH_CPT GPIO

PCH_CPT GPIO	Use As	Signal Name	Internal & External Pull-up/down	Power
GPIO 00				
GPIO 01				
GPIO [2:5]				
GPIO 06				
GPIO 07				
GPIO 08				
GPIO 09				
GPIO 10				
GPIO 11				
GPIO 12				
GPIO 13				
GPIO 14				
GPIO 15				
GPIO 16				
GPIO 17				
GPIO 18				
GPIO 19				
GPIO 20				
GPIO 21				
GPIO 22				
GPIO 23				
GPIO 24				
GPIO 25				
GPIO 26				
GPIO 27				
GPIO 28				
GPIO 29				
GPIO 30				
GPIO 31				
GPIO 32				
GPIO 33				
GPIO 34				
GPIO 35				
GPIO 36				
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GPIO 38				
GPIO 39				
GPIO 40				
GPIO 41				
GPIO 42				
GPIO 43				
GPIO 44				
GPIO 45				
GPIO 46				
GPIO 47				
GPIO 48				
GPIO 49				
GPIO 50				
GPIO 51				
GPIO 52				
GPIO 53				
GPIO 54				
GPIO 55				
GPIO 56				
GPIO 57				
GPIO 58				
GPIO 59				
GPIO 60				
GPIO 61				
GPIO 62				
GPIO 63				
GPIO 64				
GPIO 65				
GPIO 66				
GPIO 67				
GPIO 72				
GPIO 73				
GPIO 74				
GPIO 75				

EC NPCE795L

EC GPIO	Use As	Signal Name
GPA0		
GPA1		
GPA2		
GPA3		
GPA4		
GPA5		
GPA6		
GPA7		
GPB0		
GPB1		
GPB2		
GPB3		
GPB4		
GPB5		
GPB6		
GPB7		
GPC0		
GPC1		
GPC2		
GPC3		
GPC4		
GPC5		
GPC6		
GPC7		
GPD0		
GPD1		
GPD2		
GPD3		
GPD4		
GPD5		
GPD6		
GPD7		
GPE0		
GPE1		
GPE2		
GPE3		
GPE4		
GPE5		
GPE6		
GPE7		
GPF0		
GPF1		
GPF2		
GPF3		
GPF4		
GPF5		
GPF6		
GPF7		
GPG0		
GPG1		
GPG2		
GPG6		
GPH0		
GPH1		
GPH2		
GPH3		
GPH4		
GPH5		
GPH6		
GPI0		
GPI1		
GPI2		
GPI3		
GPI4		
GPI5		
GPI6		
GPI7		
GPJ0		
GPJ1		
GPJ2		
GPJ3		
GPJ4		
GPJ5		

SM_BUS ADDRESS :

SM-Bus Device	SM-Bus Address
SO-DIMM 0	1010000x (A0h)
SO-DIMM 1	1010001x (A4h)

PCIE 1	N/A
PCIE 2	Minicard WLAN
PCIE 3	N/A
PCIE 4	USB3.0
PCIE 5	N/A
PCIE 6	GLAN
PCIE 7	N/A
PCIE 8	N/A

SATA0	SATA HDD
SATA1	N/A
SATA2	SATA ODD
SATA3	N/A
SATA4	N/A
SATA5	N/A

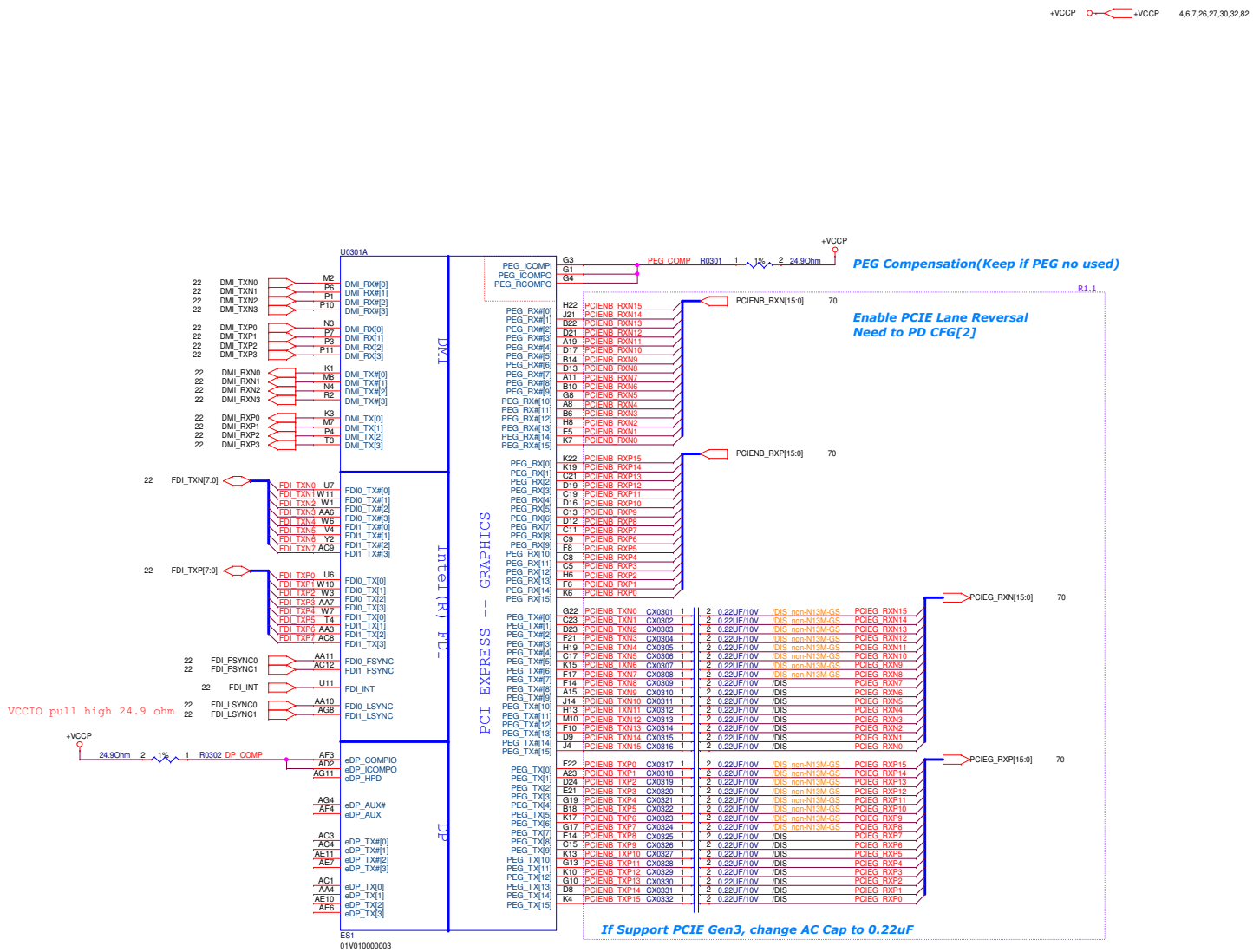
USB 0	USB Port (1)
USB 1	USB Port (2)
USB 2	USB 3.0 Port (3)
USB 3	USB Port (4)
USB 4	N/A
USB 5	N/A
USB 6	N/A
USB 7	N/A
USB 8	CMOS Camera
USB 9	WLAN
USB 10	Card Reader
USB 11	N/A
USB 12	N/A
USB 13	N/A

PEGATRON Title : System Setting

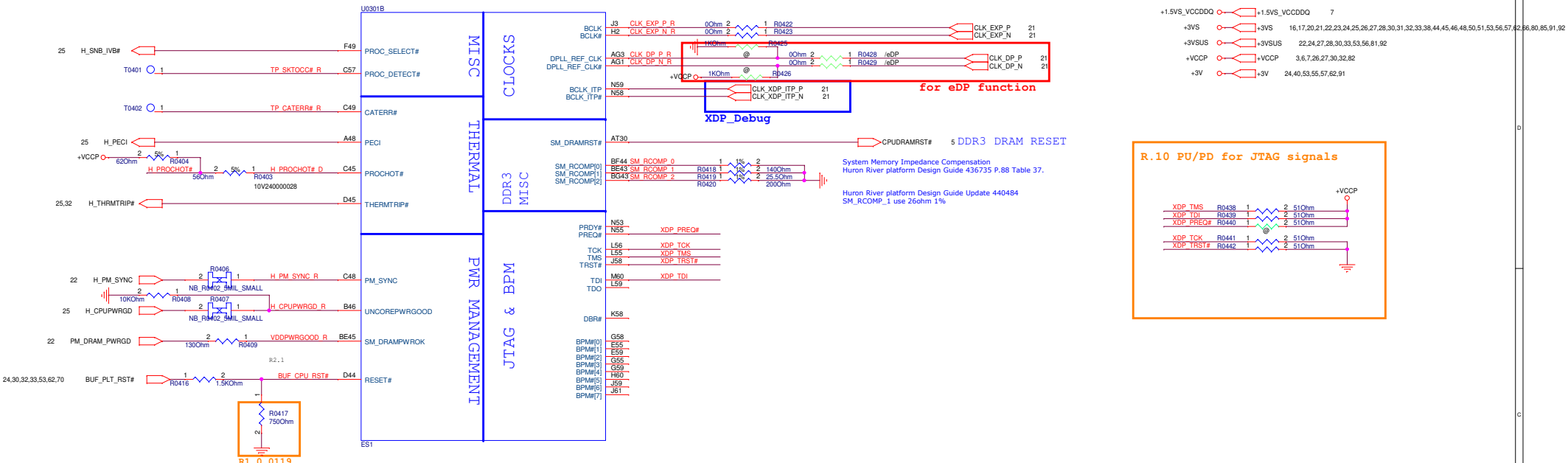
BG1-HW RD Div.2-NB RD Dept.5 Engineer: Trunks Chen

Size	Project Name	Rev
C	B34	1.0

Date: Wednesday, February 01, 2012 Sheet 2 of 59

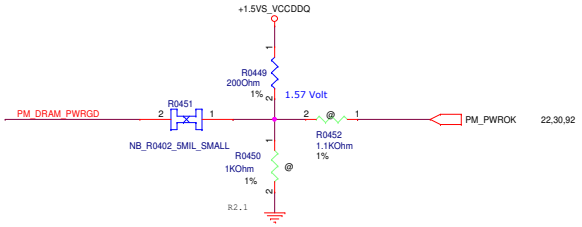


PEGATRON	Title : CPU(1)_DMI,DP,PEG,FDI		
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Trunks Chen		
Size: C	Project Name: B34		Rev: 1.0
Date: Wednesday, February 01, 2012	Sheet 3 of 59		



PM_SYS_PWRGD is the power good for +1.5V_VCCDDQ

Different from EVEREST

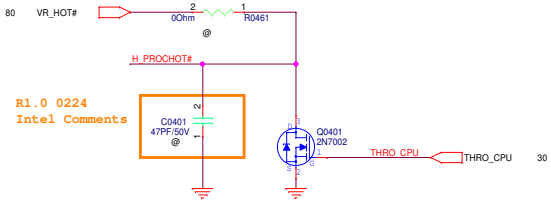


If don't support S3 power reduction
1. Unmount U0404, D0404, C0413, C0420, R0450, R0452, R0453, R0460
2. Change R0449 to 200ohm from 1kohm, change R0409 to 130ohm from 0ohm - Design Guide 1.0 page 106

3. Unmount Q0501, C0501, R0506, R0504, R0507
4. Mount R0501, change r0508 to 0ohm from 1kohm

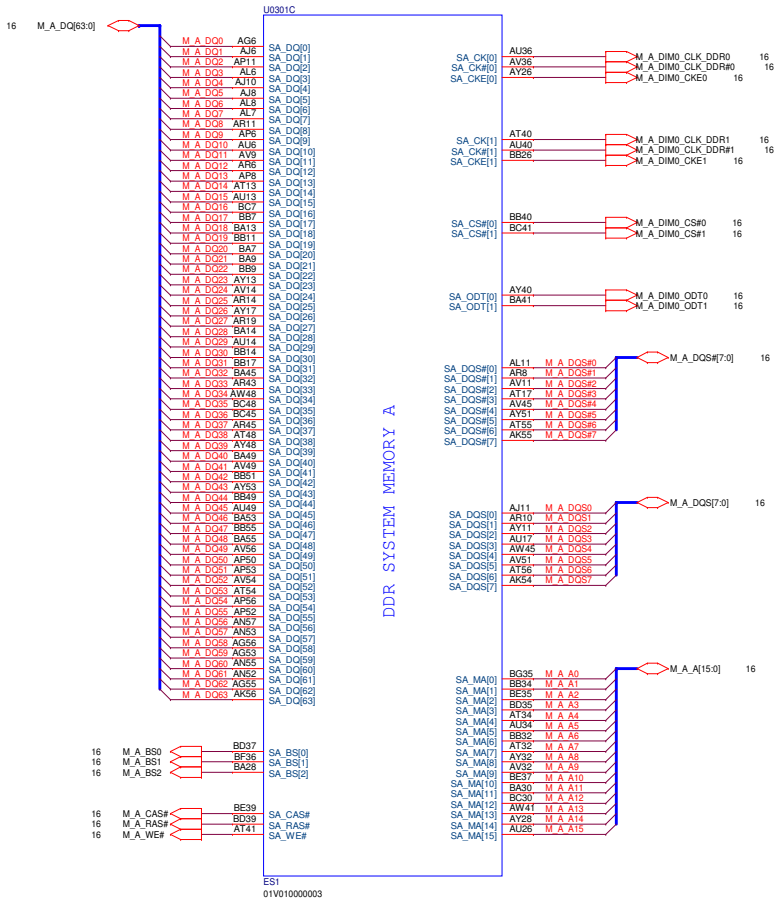
5 Unmount Q0701, R0703, R0705, Q0702
6. Mount R0702 and short JP0701

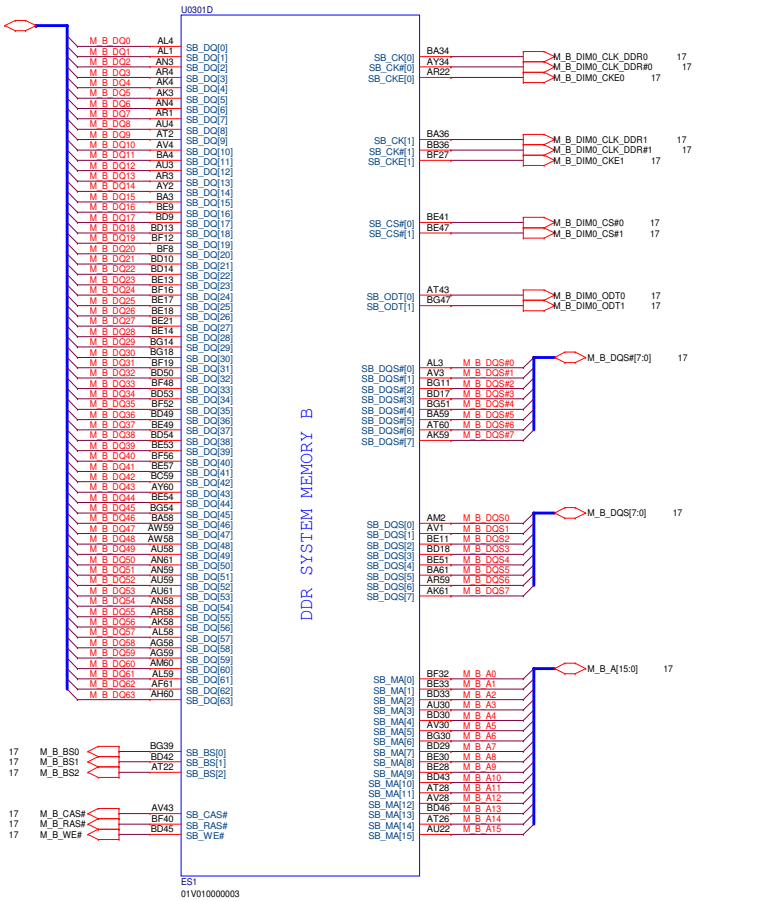
7. Unmount R2232, R2231, Q2203



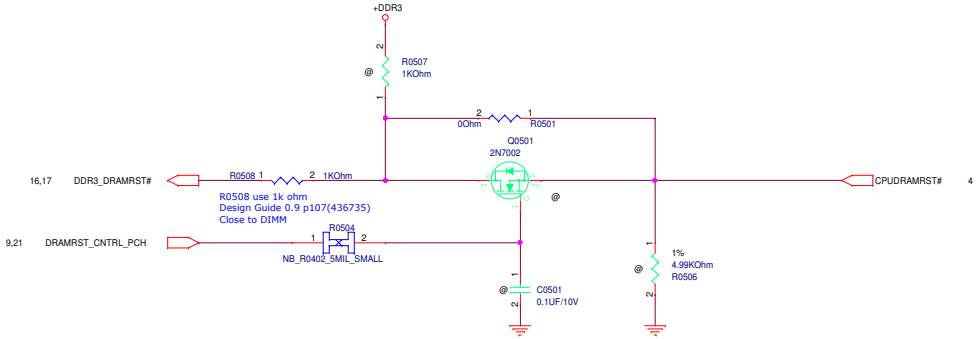
PEGATRON	Title : CPU(2)_CLK,MISC,JTAG		
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Trunks Chen		
Size: C	Project Name: B34	Rev: 1.0	
Date: Wednesday, February 01, 2012	Sheet 4 of 59		

+DDR3 +DDR3 7,16,17,18,57,83





R1.0 S3 circuit: DRAM_RST# to memory should be high during S3



PEGATRON Title : CPU(3)_DDR3

BG1-HW RD Div.2-NB RD Dept.5 Engineer: Trunks Chen

Size	Project Name	Rev
C	B34	1.0

Date: Wednesday, February 01, 2012 Sheet 5 of 59

+VCCP → +VCCP 3,4,7,26,27,30,32,82

+VCORE → +VCORE 9,11,80

Vcc for processor core
Voltage range: 0.3 – 1.52V

Voltage for the memory controller and shared cache defined at the motherboard VCCIO_SENSE and VSS_SENSE_VCCIO

U0301F

+VCORE

CORE SUPPLY

PEG AND DDR

POWER

QUIET RAILS

SVID

SENSE LINES

VCC: A26, A29, A31, A34, A35, A38, A39, A42, C26, C27, C32, C34, C37, C39, C42, D27, D32, D34, D37, D39, D42, E26, E28, E32, E34, E37, E38, F25, F26, F28, F32, F34, F37, F38, F42, G42, H25, H26, H28, H29, H32, H34, H35, H37, H38, H40, J25, J26, J28, J29, J32, J34, J35, J37, J38, J40, J42, K26, K27, K29, K32, K34, K35, K37, K39, K42, L25, L28, L33, L36, L40, N26, N30, N34, N38

VCC74, VCC73, VCC72, VCC71, VCC70, VCC69, VCC68, VCC67, VCC66, VCC65, VCC64, VCC63, VCC62, VCC61, VCC60, VCC59, VCC58, VCC57, VCC56, VCC55, VCC54, VCC53, VCC52, VCC51, VCC50, VCC49, VCC48, VCC47, VCC46, VCC45, VCC44, VCC43, VCC42, VCC41, VCC40, VCC39, VCC38, VCC37, VCC36, VCC35, VCC34, VCC33, VCC32, VCC31, VCC30, VCC29, VCC28, VCC27, VCC26, VCC25, VCC24, VCC23, VCC22, VCC21, VCC20, VCC19, VCC18, VCC17, VCC16, VCC15, VCC14, VCC13, VCC12, VCC11, VCC10, VCC9, VCC8, VCC7, VCC6, VCC5, VCC4, VCC3, VCC2, VCC1, VCC0

VCCIO34 AF46, VCCIO28 AG48, VCCIO27 AG50, VCCIO26 AG51, VCCIO23 AJ17, VCCIO22 AJ21, VCCIO21 AJ25, VCCIO20 AJ43, VCCIO19 AJ47, VCCIO18 AK50, VCCIO17 AK51, VCCIO16 AL14, VCCIO15 AL15, VCCIO14 AL16, VCCIO13 AL20, VCCIO12 AL22, VCCIO11 AL26, VCCIO10 AL45, VCCIO9 AL48, VCCIO8 AM16, VCCIO7 AM17, VCCIO6 AM21, VCCIO5 AM43, VCCIO4 AM47, VCCIO3 AN20, VCCIO2 AN42, VCCIO1 AN45, VCCIO0 AN48

+VCCP

C0628 1UF/6.3V, C0631 1UF/6.3V, C0632 1UF/6.3V, C0635 1UF/6.3V, C0634 1UF/6.3V, C0636 1UF/6.3V, C0637 1UF/6.3V, C0613 1UF/6.3V

C0610 1UF/6.3V, C0609 1UF/6.3V, C0606 1UF/6.3V, C0611 1UF/6.3V

remove 1UF C0614,C0616,C0623,C0607

vx_c0603_small: C0618 10UF/6.3V, C0619 10UF/6.3V, C0621 10UF/6.3V, C0620 10UF/6.3V, C0617 10UF/6.3V

Chief River

Decoupling guide from Intel (EE)

+VCCP 1uF * 18pcs
10uF * 10pcs
220uF *1pcs

VCCIO47 AA14, VCCIO46 AA15, VCCIO45 AB17, VCCIO44 AB20, VCCIO43 AC13, VCCIO42 AD16, VCCIO41 AD18, VCCIO40 AD21, VCCIO39 AE14, VCCIO38 AE15, VCCIO37 AF16, VCCIO36 AF18, VCCIO35 AF20, VCCIO34 AG15, VCCIO33 AG16, VCCIO32 AG17, VCCIO31 AG20, VCCIO30 AG21, VCCIO29 AJ14, VCCIO25 AJ15, VCCIO24 AJ15

+VCCP

remove 1UF C0612,C0615,C0608,C0624

C0625 1UF/6.3V, C0626 1UF/6.3V, C0627 1UF/6.3V, C0629 1UF/6.3V, C0630 1UF/6.3V, C0633 1UF/6.3V

vx_c0603_small: C0602 10UF/6.3V, C0603 10UF/6.3V, C0605 10UF/6.3V, C0604 10UF/6.3V, C0601 10UF/6.3V

CE0603 330UF/2.5V

change size 3528 2mm (08/12)

VCCIO49 W16, VCCIO48 W17 — +VCCIO_CPU_F — R0601 R2.1 NB_R0603_32MIL_SMALL — +VCCP

+3VA — R0615 10KOhm

VCCIO_SEL BC22 — VCCP_SEL

VCCIO_SEL	VCCSA
H	1.05V
L	1.00V

Cheif River

Filitered(BGA only)

VCCPQE1 AM25, VCCPQE0 AN22 — +VCCP — R0613 0Ohm — C0622 1UF/6.3V

Intel Comments

VIDALERT# A44 — H_CPU_SVIDALRT# — R0602 5% 43Ohm — R0603 75Ohm 1% Close to CPU — VR_SVID_ALERT# 80 — SP0601 — R0605 54.9Ohm 1% Close to VR — VR_SVID_CLK 80

VIDSCLK B43 — H_CPU_SVIDCLK

VIDSOUT C44 — H_CPU_SVIDDAT — R0607 130Ohm 1% Close to CPU — SP0602 — R0608 130Ohm 1% Close to VR — VR_SVID_DATA 80

VCC_SENSE F43 — VCC_SENSE_R — SP0603 NB_R0402_20MIL_SMALL — VCCSENSE — VCCSENSE 80

VSS_SENSE G43 — VSS_SENSE_R — SP0604 NB_R0402_20MIL_SMALL — VSSSENSE — VSSSENSE 80

VCCIO_SENSE AN16 — VCCP_SENSE_R — SP0605 NB_R0402_20MIL_SMALL — +VCCP_SENSE — +VCCP_SENSE 82

VSS_SENSE_VCCIO AN17 — VSSP_SENSE_R — SP0606 NB_R0402_20MIL_SMALL — +VSSP_SENSE — +VSSP_SENSE 82

ES1
01V010000003

PEGATRON Title : CPU(4)_PWR

BG1-HW RD Div.2-NB RD Dept.5 Engineer: Trunks Chen

Size	Project Name	Rev
C	B34	1.0

Date: Wednesday, February 01, 2012 Sheet 6 of 59

Decoupling guide from Intel PDDG R0.8
+VGFX_CORE
1uF * 11pcs
10uF * 6pcs
22uF * 6pcs

Graphics core voltage
Voltage range: 0 – 1.52V

+VGFX_CORE

C0725 1UF/6.3V, C0727 1UF/6.3V, C0731 1UF/6.3V, C0726 1UF/6.3V, C0732 1UF/6.3V, C0729 1UF/6.3V, C0730 1UF/6.3V, C0728 1UF/6.3V

C0717 1UF/6.3V, C0719 1UF/6.3V, C0722 1UF/6.3V

vx_c0603_small: C0790 10UF/6.3V, C0791 10UF/6.3V, C0788 10UF/6.3V, C0789 10UF/6.3V, C0787 10UF/6.3V, C0786 10UF/6.3V

C0738 22UF/6.3V, C0739 22UF/6.3V, C0740 22UF/6.3V, C0741 22UF/6.3V, C0742 22UF/6.3V, C0743 22UF/6.3V, CE0703 330UF/2.5V

change size from 0805 power request

U0301G

AA46 AB47 AB50 AB51 AB52 AB53 AB55 AB56 AB58 AB59 AC61 AD47 AD48 AD50 AD51 AD52 AD53 AD55 AD56 AD58 AD59 AE46 N45 P47 P48 P50 P51 P52 P53 P55 P56 P61 T48 T58 T59 T61 U46 V47 V48 V50 V51 V52 V53 V55 V56 V58 V59 W50 W51 W52 W53 W55 W56 W61 Y48 Y61

VAXG21 VAXG20 VAXG19 VAXG18 VAXG17 VAXG16 VAXG15 VAXG14 VAXG13 VAXG12 VAXG11 VAXG10 VAXG9 VAXG8 VAXG7 VAXG6 VAXG5 VAXG4 VAXG3 VAXG2 VAXG1 VAXG0 VAXG55 VAXG54 VAXG53 VAXG52 VAXG51 VAXG50 VAXG49 VAXG48 VAXG47 VAXG46 VAXG45 VAXG44 VAXG43 VAXG42 VAXG41 VAXG40 VAXG39 VAXG38 VAXG37 VAXG36 VAXG35 VAXG34 VAXG33 VAXG32 VAXG31 VAXG30 VAXG29 VAXG28 VAXG27 VAXG26 VAXG25 VAXG24 VAXG23 VAXG22

GRAPHICS

POWER

DDR3 – 1.5V RAILS

DDR3 Reference Voltage

+V_SM_REF 10mil

SM_VREF AY43 +V_SM_VREF

+V_SM_VREF
pull high in p.18
C0794 0.1UF/16V vx_c0603_small

VDDQ25 AJ28, VDDQ24 AJ33, VDDQ23 AJ36, VDDQ22 AJ40, VDDQ21 AL30, VDDQ20 AL34, VDDQ19 AL38, VDDQ18 AL42, VDDQ17 AM33, VDDQ16 AM36, VDDQ15 AM40, VDDQ14 AN30, VDDQ13 AN34, VDDQ12 AN38, VDDQ11 AR26, VDDQ10 AR28, VDDQ9 AR30, VDDQ8 AR32, VDDQ7 AR34, VDDQ6 AR36, VDDQ5 AR40, VDDQ4 AV41, VDDQ3 AW26, VDDQ2 BA40, VDDQ1 BB28, VDDQ0 BG33

MAX:10A

C0704 1UF/6.3V, C0709 1UF/6.3V, C0705 1UF/6.3V, C0706 1UF/6.3V, C0707 1UF/6.3V, C0708 1UF/6.3V, C0713 1UF/6.3V, C0710 1UF/6.3V, C0712 1UF/6.3V, C0711 1UF/6.3V

vx_c0603_small: C0775 10UF/6.3V, C0774 10UF/6.3V, C0772 10UF/6.3V, C0769 10UF/6.3V, C0767 10UF/6.3V, C0765 10UF/6.3V, C0770 10UF/6.3V, C0768 10UF/6.3V

CE0702 330UF/2V

+1.5VS_VCCDDQ, +DDR3

JP0701 3MM_OPEN_5MIL — ICCMAX_VDDQ 5A

change short pin footprint

Processor I/O supply voltage for DDR3 (DC + AC specification)

Chief River

Decoupling guide from Intel (EE)
+1.5VS_VCCDDQ
1uF * 10pcs
10uF * 8pcs
330uF * 1pcs

Filtered(BGA Only)

VCCDQ1 AM28, VCCDQ0 AN26 — +1.5VS_VCCDDQ — R0707 0Ohm — C0714 1UF/6.3V

QUIET RAILS

SP0706 NB_R0402_20MIL_SMALL — SP0707 NB_R0402_20MIL_SMALL

80 VCCGT_SENSE — VCCGT_SENSE — VCCGT_SENSE_R — F45 VAXG_SENSE
80 VSSGT_SENSE — VSSGT_SENSE — VSSGT_SENSE_R — G45 VSSAXG_SENSE

SENSE LINES

PLL supply voltage
(DC + AC specification)

+1.8VS

MAX:1.2A
TDC: 1.2A

CE0701 330UF/2V, C0761 1UF/6.3V, C0764 1UF/6.3V

BB3 VCCPLL2, BC1 VCCPLL1, BC4 VCCPLL0

1.8V RAIL

VDDQ_SENSE BC43, VSS_SENSE_VDDQ BA43 — T0701, T0702

SENSE LINES

+VCCSA

MAX:6A

vx_c0603_small: C0783 10UF/6.3V, C0781 10UF/6.3V, C0792 10UF/6.3V, C0777 10UF/6.3V, C0793 10UF/6.3V

C0735 1UF/6.3V, C0736 1UF/6.3V, C0733 1UF/6.3V, C0734 1UF/6.3V, C0737 1UF/6.3V

L17 VCCSA15, L21 VCCSA14, N16 VCCSA13, N20 VCCSA12, N22 VCCSA11, P17 VCCSA10, P20 VCCSA9, R16 VCCSA8, R18 VCCSA7, R21 VCCSA6, U15 VCCSA5, V16 VCCSA4, V17 VCCSA3, V18 VCCSA2, V21 VCCSA1, W20 VCCSA0

SA RAIL

VCCSA_SENSE U10 — R0704 0Ohm — VCCSA_SENSE — Close to CPU

VCCSA_VID[0] D48, VCCSA_VID[1] D49 — VCCSA_SEL0, VCCSA_SEL1 — 85

Chief River

+VCCSA_SEL0	+VCCSA_SEL1	VCCSA
L	L	0.9V
L	H	0.85V
H	L	0.725V
H	H	0.675V

ES1
01V010000003

Decoupling guide for A14 (EE)
+VCCSA
1uF * 5pcs
10uF * 5pcs

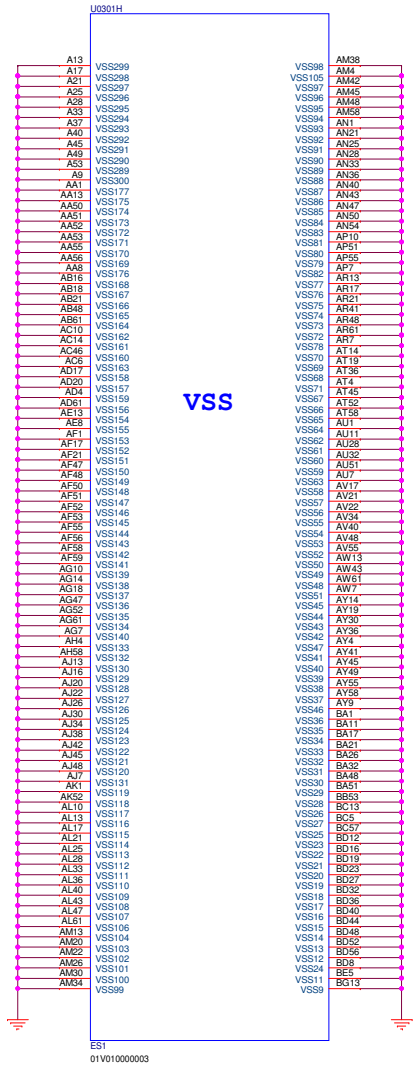
+VCCP	+VCCP	3,4,6,26,27,30,32,82
+DDR3	+DDR3	5,16,17,18,57,83
+VCCSA	+VCCSA	85
+1.8VS	+1.8VS	25,26,80,84
+VGFX_CORE	+VGFX_CORE	9,80
+1.5VS	+1.5VS	26,53,57,91
+V_SM_VREF	+V_SM_VREF	18,83

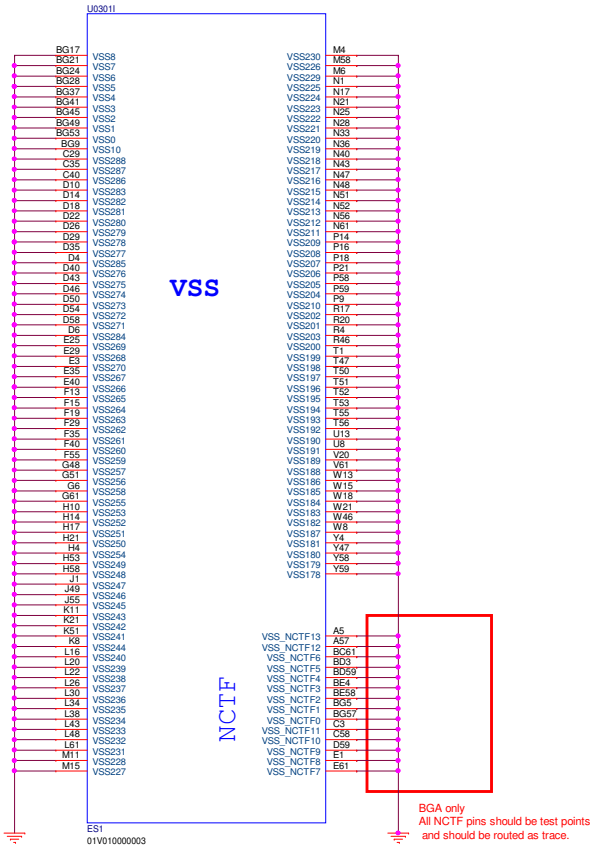
SUSB_EC#
+1.5V_VCCDDQ
+1.5V_VCCDDQ Power Good (U0404 pin 4)
+0.75VS
> 0
>100 ns

R1.0 0209
Intel Comments

+VCCP
R0708 1KOhm, R0709 1KOhm
VCCSA_SEL0
VCCSA_SEL1
R0701 1KOhm, R0702 1KOhm

PEGATRON Title : CPU(5)_GFX_PWR
BG1-HW RD Div.2-NB RD Dept.5 Engineer: Trunks Chen
Size C | Project Name B34 | Rev 1.0
Date: Wednesday, February 01, 2012 | Sheet 7 of 59





PEGATRON	Title : CPU(6)_GND		
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Trunks Chen		
Size: C	Project Name: B34		Rev: 1.0
Date: Wednesday, February 01, 2012	Sheet 8 of 59		

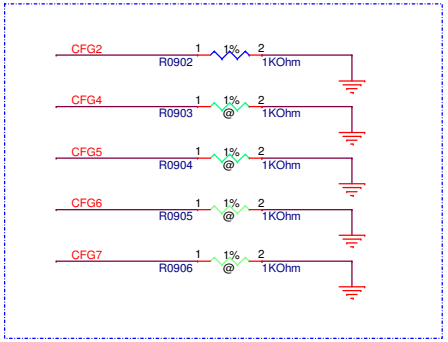
CFG strapping information:

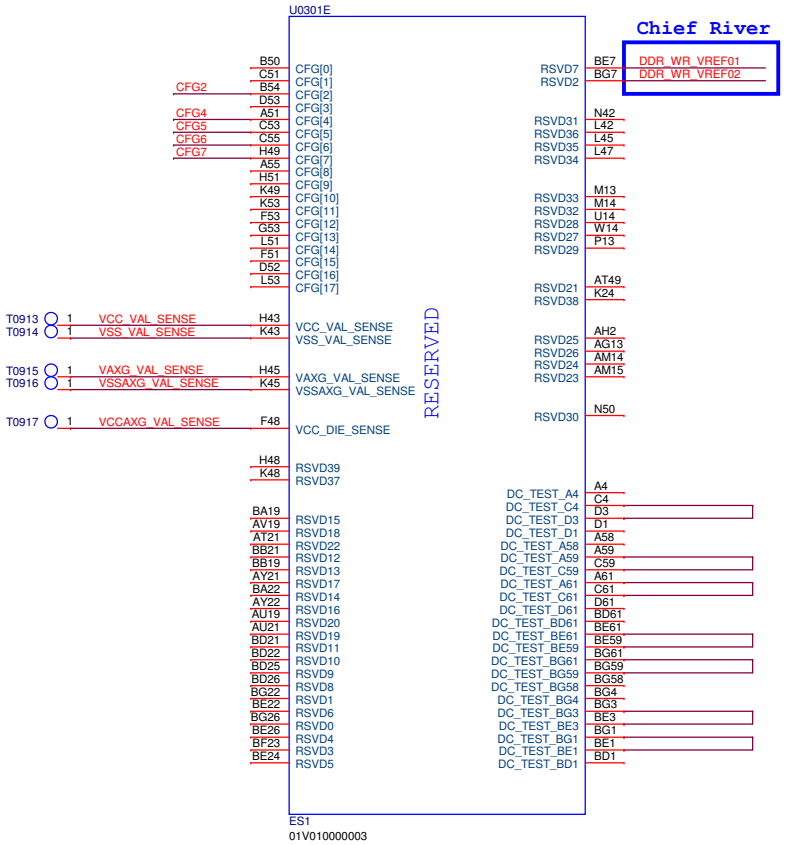
CFG[2]: PCIE Static Numbering Lane Reversal- CFG[2] is for the 16x
- 1: (Default) Normal Operation, Lane # definition matches sockect pin map definition
- 0: Lane Numbers Reversed

CFG[4]: Embedded DisplayPort Detection
- 1: (Default) Disabled ; No Physical Display Port attached to Embedded DisplayPort
- 0: Enabled ; An external Display Port device is connected to the Embedded Display Port

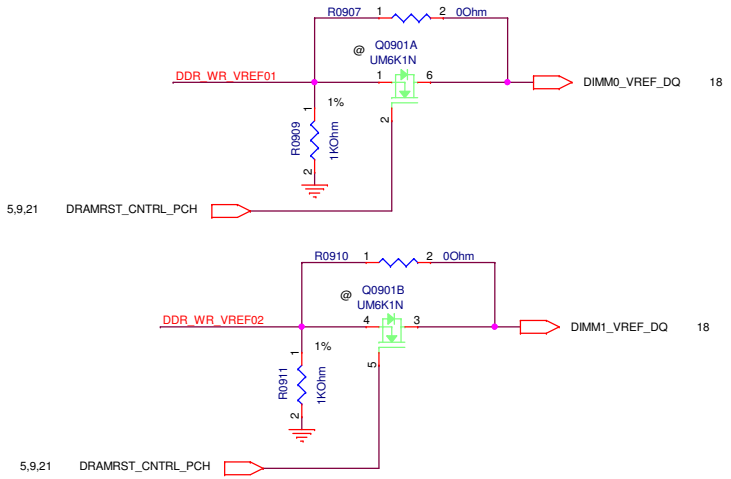
CFG[6:5]: PCI Express Port Bifurcation Straps
- 11 : (Default) x 1 6
- 10 : x 8 , x 8
- 01 : Reserved
- 00 : x 8 , x 4 , x 4

CFG[7]: PEG DEFER TRAINING
- 1: (Default) PEG Train immediately following xxRESETB de assertion
- 0: PEG Wait for BIOS training



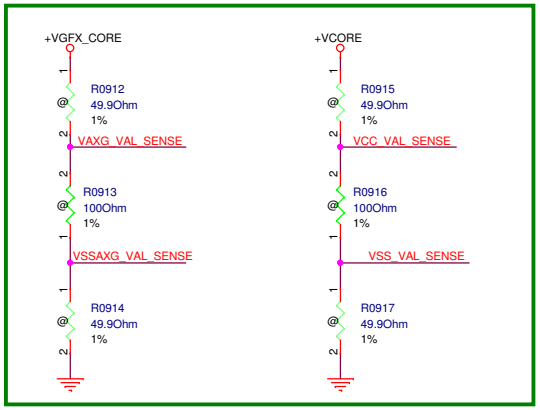


PROCESSOR DRIVEN Vref PATH WAS STUFFED BY DEFAULT:



For iFDIM testing
R0912~ R0917 close to pin < 1 inch

R1.1 0512



PEGATRON Title : CPU(7)_RSVD

BG1-HW RD Div.2-NB RD Dept.5 Engineer: Trunks Chen

Size	Project Name	Rev
Custom	B34	1.0

Date: Wednesday, February 01, 2012 Sheet 9 of 59

+VTT_PCH_ORG +VTT_PCH_ORG 22,26,27

+3VSUS +3VSUS 22,24,27,28,30,33,53,56,81,92

+VCCP +VCCP 3,4,6,7,26,27,30,32,82

+3VS +3VS 16,17,20,21,22,23,24,25,26,27,28,30,31,32,33,38,44,45,46,48,50,51,53,56,57,62,66,80,85,91,92

remove XDP connector

Check Connector

CPU XDP connector

PCH XDP connector

PEGATRON

Title : CPU_PCH_XDP

BG1-HW RD Div.2-NB RD Dept.5

Engineer: *Trunks Chen*

Size	Project Name	Rev
B	B34	1.0

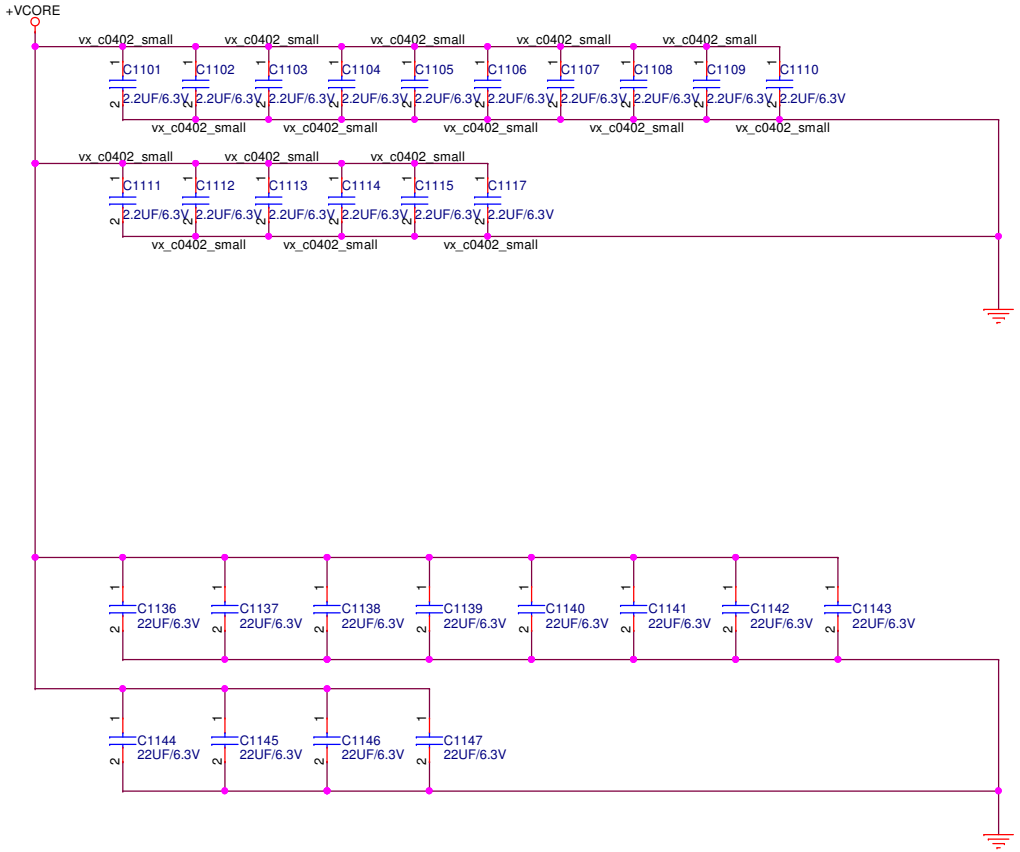
Date: Wednesday, February 01, 2012 Sheet 10 of 59

Chief River

Decoupling guide from Intel PDDG R0.8

+VCORE 2.2uF * 16 pcs

22uF * 12 pcs



PEGATRON	Title : CPU DECOUPLING	
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Trunks Chen	
Size: B	Project Name: B34	Rev: 1.0
Date: Wednesday, February 01, 2012	Sheet 11 of 59	

+DDR3 +DDR3 5,7,17,18,57,83

+0.75VS +0.75VS 17,57,83

+3VS +3VS 17,20,21,22,23,24,25,26,27,28,30,31,32,33,38,44,45,46,48,50,51,53,56,57,62,66,80,85,91,92

+V_VREF_CA_DIMM0 +V_VREF_CA_DIMM0 17,18

+V_VREF_DQ_DIMM0 +V_VREF_DQ_DIMM0 18

+DDR3 CE1603 220UF/4V @

+DDR3 Layout Note: Place these caps near SO DIMM 0

vx_c0603_small C1609 10UF/6.3V vx_c0603_small C1610 10UF/6.3V C1611 10UF/6.3V C1612 10UF/6.3V @ C1613 10UF/6.3V @ C1620 10UF/6.3V @

+0.75VS C1616 1UF/6.3V C1617 1UF/6.3V C1618 1UF/6.3V @ C1619 1UF/6.3V @

M_A_DIM0_CLK_DDR0 C1602 10PF/50V @ 1% 150Ohm R1603 @ M_A_DIM0_CLK_DDR#0

M_A_DIM0_CLK_DDR1 C1601 10PF/50V @ 1% 150Ohm R1604 @ M_A_DIM0_CLK_DDR#1

PLACE CLOSE TO SODIMM

5 M_A_A[15:0]

M_A_A0 98 M_A_A1 97 M_A_A2 96 M_A_A3 95 M_A_A4 92 M_A_A5 91 M_A_A6 90 M_A_A7 86 M_A_A8 89 M_A_A9 85 M_A_A10 107 M_A_A11 84 M_A_A12 83 M_A_A13 119 M_A_A14 80 M_A_A15 78

J1601A

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12/BC# A13 A14 A15

DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15 DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23 DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31 DQ32 DQ33 DQ34 DQ35 DQ36 DQ37 DQ38 DQ39 DQ40 DQ41 DQ42 DQ43 DQ44 DQ45 DQ46 DQ47 DQ48 DQ49 DQ50 DQ51 DQ52 DQ53 DQ54 DQ55 DQ56 DQ57 DQ58 DQ59 DQ60 DQ61 DQ62 DQ63

5 M_A_DQ0 7 M_A_DQ1 15 M_A_DQ6 17 M_A_DQ5 4 M_A_DQ4 6 M_A_DQ2 16 M_A_DQ3 18 M_A_DQ7 21 M_A_DQ13 23 M_A_DQ8 33 M_A_DQ10 35 M_A_DQ14 22 M_A_DQ9 24 M_A_DQ12 34 M_A_DQ15 36 M_A_DQ11 39 M_A_DQ16 41 M_A_DQ21 51 M_A_DQ23 53 M_A_DQ18 40 M_A_DQ20 42 M_A_DQ17 50 M_A_DQ22 52 M_A_DQ19 57 M_A_DQ29 59 M_A_DQ24 67 M_A_DQ26 69 M_A_DQ31 56 M_A_DQ30 58 M_A_DQ28 68 M_A_DQ25 70 M_A_DQ27 129 M_A_DQ39 131 M_A_DQ37 141 M_A_DQ33 143 M_A_DQ35 130 M_A_DQ32 132 M_A_DQ36 140 M_A_DQ38 142 M_A_DQ34 147 M_A_DQ45 149 M_A_DQ46 157 M_A_DQ47 159 M_A_DQ42 146 M_A_DQ40 148 M_A_DQ44 158 M_A_DQ41 160 M_A_DQ43 163 M_A_DQ53 165 M_A_DQ49 175 M_A_DQ55 177 M_A_DQ50 164 M_A_DQ52 166 M_A_DQ48 174 M_A_DQ51 176 M_A_DQ54 181 M_A_DQ58 183 M_A_DQ62 191 M_A_DQ57 193 M_A_DQ61 180 M_A_DQ63 182 M_A_DQ56 192 M_A_DQ60 194 M_A_DQ59

M_A_DQ[63:0] 5

0~7 8~15 16~23 24~31 32~39 40~47 48~55 56~63

5 M_A_DIM0_CLK_DDR1 5 M_A_DIM0_CLK_DDR#1 5 M_A_DIM0_CLK_DDR0 5 M_A_DIM0_CLK_DDR#0

102 CK1 104 CK1# 101 CK0 103 CK0#

5 M_A_DIM0_CS#1 5 M_A_DIM0_CS#0

121 S1# 114 S0#

5 M_A_DIM0_ODT1 5 M_A_DIM0_ODT0

120 ODT1 116 ODT0

5 M_A_WE# 5 M_A_RAS# 5 M_A_CAS#

113 WE# 110 RAS# 115 CAS#

5 M_A_BS2 5 M_A_BS1 5 M_A_BS0

79 BA2 108 BA1 109 BA0

5 M_A_DIM0_CKE1 5 M_A_DIM0_CKE0

74 CKE1 73 CKE0

SMBus Slave Address: A0H

R1601 1 2 10KOhm 201 SA1

R1602 1 2 10KOhm 197 SA0

M_A_DQS7 188 M_A_DQS#7 186 M_A_DQS6 171 M_A_DQS#6 169 M_A_DQS5 154 M_A_DQS#5 152 M_A_DQS4 137 M_A_DQS#4 135 M_A_DQS3 64 M_A_DQS#3 62 M_A_DQS2 47 M_A_DQS#2 45 M_A_DQS1 29 M_A_DQS#1 27 M_A_DQS0 12 M_A_DQS#0 10

DQS7 DQS#7 DQS6 DQS#6 DQS5 DQS#5 DQS4 DQS#4 DQS3 DQS#3 DQS2 DQS#2 DQS1 DQS#1 DQS0 DQS#0

5 M_A_DQS[7:0] 5 M_A_DQS#[7:0]

M_A_DM7 187 M_A_DM6 170 M_A_DM5 153 M_A_DM4 136 M_A_DM3 63 M_A_DM2 46 M_A_DM1 28 M_A_DM0 11

DM7 DM6 DM5 DM4 DM3 DM2 DM1 DM0

DM should connect to GND directly
Design Guide 0.9 p86 (436735)

17,28,31,53 SMB_CLK_S 202 SCL

17,28,31,53 SMB_DAT_S 200 SDA

RESET# 30 DDR3_DRAMRST# 5,17

DDR3_DIMM_204P

12V02GBRM000

M:1202-00EE000

S:1202-00KB000

+DDR3 MAX: 2.68A TDC: 2.68A

C1605 0.1UF/10V C1606 0.1UF/10V

J1601B

VDD1 VDD3 VDD5 VDD7 VDD9 VDD11 VDD13 VDD15 VDD17

VDD2 VDD4 VDD6 VDD8 VDD10 VDD12 VDD14 VDD16 VDD18

+DDR3 C1607 0.1UF/10V C1608 0.1UF/10V

Layout Note: Place these caps near SO DIMM 0

VSS1 VSS3 VSS5 VSS7 VSS9 VSS11 VSS13 VSS15 VSS17 VSS19 VSS21 VSS23 VSS25 VSS27 VSS29 VSS31 VSS33 VSS35 VSS37 VSS39 VSS41 VSS43 VSS45 VSS47 VSS49 VSS51

VSS2 VSS4 VSS6 VSS8 VSS10 VSS12 VSS14 VSS16 VSS18 VSS20 VSS22 VSS24 VSS26 VSS28 VSS30 VSS32 VSS34 VSS36 VSS38 VSS40 VSS42 VSS44 VSS46 VSS48 VSS50 VSS52

GND1 GND2

T1601 1 PM_EXTTS#0_DIM_A Reserve

EVENT# TEST

NC1 NC2

NP_NC1 NP_NC2

MAX: 0.75A TDC: 0.75A

VTT1 VTT2 +0.75VS

+3VS

VREFCA VREFDQ

VDDSPD

DDR3_DIMM_204P

12V02GBRM000

+V_VREF_CA_DIMM0 W/S=20/20

vx_c0402_small C1624 2.2UF/6.3V C1623 0.1UF/10V

+V_VREF_DQ_DIMM0 W/S=20/20

vx_c0402_small C1622 2.2UF/6.3V C1625 0.1UF/10V

C1615 0.1UF/10V C1614 vx_c0402_small 2.2UF/6.3V @

PEGATRON Title : DDR3(1)_SO-DIMM0

BG1-HW RD Div.2-NB RD Dept.5 Engineer: Trunks Chen

Size	Project Name	Rev
Custom	B34	1.0

Date: Wednesday, February 01, 2012 Sheet 16 of 59

+DDR3 +DDR3 5,7,16,18,57,83

+0.75VS +0.75VS 16,57,83

+3VS +3VS 16,20,21,22,23,24,25,26,27,28,30,31,32,33,38,44,45,46,48,50,51,53,56,57,62,66,80,85,91,92

+V_VREF_CA_DIMM1 +V_VREF_CA_DIMM1 16,18

+V_VREF_DQ_DIMM1 +V_VREF_DQ_DIMM1 18

+DDR3 CE1703 220UF/4V @

+DDR3 Layout Note: Place these caps near SO DIMM 1

C1709 22UF/6.3V, C1710 22UF/6.3V, C1711 22UF/6.3V, C1712 22UF/6.3V @, C1713 22UF/6.3V @, C1726 22UF/6.3V @

+0.75VS

C1716 1UF/6.3V, C1717 1UF/6.3V, C1718 1UF/6.3V @, C1719 1UF/6.3V @

M_B_DIM0_CLK_DDR0 — C1720 10PF/50V @ — 1% 150Ohm R1707 @ — M_B_DIM0_CLK_DDR#0

M_B_DIM0_CLK_DDR1 — C1721 10PF/50V @ — 1% 150Ohm R1708 @ — M_B_DIM0_CLK_DDR#1

PLACE CLOSE TO SODIMM

5 M_B_A[15:0]

M_B_A0 98, M_B_A1 97, M_B_A2 96, M_B_A3 95, M_B_A4 92, M_B_A5 91, M_B_A6 90, M_B_A7 86, M_B_A8 89, M_B_A9 85, M_B_A10 107, M_B_A11 84, M_B_A12 83, M_B_A13 119, M_B_A14 80, M_B_A15 78

J1701A

A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10/AP, A11, A12/BC#, A13, A14, A15

5 M_B_DIM0_CLK_DDR1 102 CK1
5 M_B_DIM0_CLK_DDR#1 104 CK1#
5 M_B_DIM0_CLK_DDR0 101 CK0
5 M_B_DIM0_CLK_DDR#0 103 CK0#

5 M_B_DIM0_CS#1 121 S1#
5 M_B_DIM0_CS#0 114 S0#

5 M_B_DIM0_ODT1 120 ODT1
5 M_B_DIM0_ODT0 116 ODT0

5 M_B_WE# 113 WE#
5 M_B_RAS# 110 RAS#
5 M_B_CAS# 115 CAS#

5 M_B_BS2 79 BA2
5 M_B_BS1 108 BA1
5 M_B_BS0 109 BA0

5 M_B_DIM0_CKE1 74 CKE1
5 M_B_DIM0_CKE0 73 CKE0

SMBus Slave Address: A4H

+3VS — RN1701B 4 10KOhm 3 — RN1701A 2 10KOhm 1 — 201 SA1, 197 SA0

M_B_DQS7 188, M_B_DQS#7 186, M_B_DQS6 171, M_B_DQS#6 169, M_B_DQS5 154, M_B_DQS#5 152, M_B_DQS4 137, M_B_DQS#4 135, M_B_DQS3 64, M_B_DQS#3 62, M_B_DQS2 47, M_B_DQS#2 45, M_B_DQS1 29, M_B_DQS#1 27, M_B_DQS0 12, M_B_DQS#0 10

DQS7, DQS#7, DQS6, DQS#6, DQS5, DQS#5, DQS4, DQS#4, DQS3, DQS#3, DQS2, DQS#2, DQS1, DQS#1, DQS0, DQS#0

5 M_B_DQS[7:0]
5 M_B_DQS#[7:0]

M_B_DM7 187, M_B_DM6 170, M_B_DM5 153, M_B_DM4 136, M_B_DM3 63, M_B_DM2 46, M_B_DM1 28, M_B_DM0 11

DM7, DM6, DM5, DM4, DM3, DM2, DM1, DM0

DM should connect to GND directly
Design Guide 1.0 P.88 (436735)

16,28,31,53 SMB_CLK_S 202 SCL
16,28,31,53 SMB_DAT_S 200 SDA

RESET# 30 DDR3_DRAMRST# 5,16

DDR3_DIMM_204P

M_B_DQ[63:0] 5

M_B_DQ0 5, M_B_DQ4 7, M_B_DQ2 15, M_B_DQ6 17, M_B_DQ5 4, M_B_DQ1 6, M_B_DQ3 16, M_B_DQ7 18, M_B_DQ12 21, M_B_DQ8 23, M_B_DQ10 33, M_B_DQ14 35, M_B_DQ13 22, M_B_DQ9 24, M_B_DQ11 34, M_B_DQ15 36, M_B_DQ20 39, M_B_DQ16 41, M_B_DQ18 51, M_B_DQ19 53, M_B_DQ22 40, M_B_DQ23 42, M_B_DQ17 50, M_B_DQ21 52, M_B_DQ28 57, M_B_DQ29 59, M_B_DQ31 67, M_B_DQ27 69, M_B_DQ24 56, M_B_DQ25 58, M_B_DQ26 68, M_B_DQ30 70, M_B_DQ37 129, M_B_DQ33 131, M_B_DQ34 141, M_B_DQ38 143, M_B_DQ36 130, M_B_DQ32 132, M_B_DQ39 140, M_B_DQ35 142, M_B_DQ41 147, M_B_DQ42 149, M_B_DQ46 157, M_B_DQ45 159, M_B_DQ40 146, M_B_DQ44 148, M_B_DQ43 158, M_B_DQ47 160, M_B_DQ53 163, M_B_DQ49 165, M_B_DQ50 175, M_B_DQ51 177, M_B_DQ48 164, M_B_DQ52 166, M_B_DQ54 174, M_B_DQ55 176, M_B_DQ56 181, M_B_DQ63 183, M_B_DQ58 191, M_B_DQ62 193, M_B_DQ61 180, M_B_DQ60 182, M_B_DQ59 192, M_B_DQ57 194

DQ0, DQ1, DQ2, DQ3, DQ4, DQ5, DQ6, DQ7, DQ8, DQ9, DQ10, DQ11, DQ12, DQ13, DQ14, DQ15, DQ16, DQ17, DQ18, DQ19, DQ20, DQ21, DQ22, DQ23, DQ24, DQ25, DQ26, DQ27, DQ28, DQ29, DQ30, DQ31, DQ32, DQ33, DQ34, DQ35, DQ36, DQ37, DQ38, DQ39, DQ40, DQ41, DQ42, DQ43, DQ44, DQ45, DQ46, DQ47, DQ48, DQ49, DQ50, DQ51, DQ52, DQ53, DQ54, DQ55, DQ56, DQ57, DQ58, DQ59, DQ60, DQ61, DQ62, DQ63

0 0~7
1 8~15
2 16~23
3 24~31
4 32~39
5 40~47
6 48~55
7 56~63

12V02GWSM000

M:1202-00FG000
S:1202-00K8000

H:5.2mm

+DDR3

J1701B

VDD1 75, VDD3 81, VDD5 87, VDD7 93, VDD9 99, VDD11 105, VDD13 111, VDD15 117, VDD17 123

VDD2 76, VDD4 82, VDD6 88, VDD8 94, VDD10 100, VDD12 106, VDD14 112, VDD16 118, VDD18 124

C1705 0.1UF/10V, C1706 0.1UF/10V

C1707 0.1UF/10V, C1708 0.1UF/10V

Layout Note: Place these caps near SO DIMM 1

VSS1 2, VSS3 8, VSS5 13, VSS7 19, VSS9 25, VSS11 31, VSS13 37, VSS15 43, VSS17 48, VSS19 54, VSS21 60, VSS23 65, VSS25 71, VSS27 127, VSS29 133, VSS31 138, VSS33 144, VSS35 150, VSS37 155, VSS39 161, VSS41 167, VSS43 172, VSS45 178, VSS47 184, VSS49 189, VSS51 195

VSS2 3, VSS4 9, VSS6 14, VSS8 20, VSS10 26, VSS12 32, VSS14 38, VSS16 44, VSS18 49, VSS20 55, VSS22 61, VSS24 66, VSS26 72, VSS28 128, VSS30 134, VSS32 139, VSS34 145, VSS36 151, VSS38 156, VSS40 162, VSS42 168, VSS44 173, VSS46 179, VSS48 185, VSS50 190, VSS52 196

T1701 1 PM_EXTTS#0_DIM_B — Reserve

EVENT# 198, TEST 125, NC1 77, NC2 122

GND1 207, GND2 208

NP_NC1 205, NP_NC2 206

VTT1 203, VTT2 204 — +0.75VS

VREFCA 126, VREFDQ 1

VDDSPD 199 — +3VS

+V_VREF_CA_DIMM1 — W/S=20/20

vx_c0402_small — C1724 2.2UF/6.3V @ — C1723 0.1UF/10V

C1715 0.1UF/10V — C1714 2.2UF/6.3V @ vx_c0402_small

+V_VREF_DQ_DIMM1 — W/S=20/20

vx_c0402_small — C1722 2.2UF/6.3V @ — C1725 0.1UF/10V

DDR3_DIMM_204P
12V02GWSM000

PEGATRON

Title : DDR3(2)_SO-DIMM1

BG1\HW1

Engineer: Trunks Chen

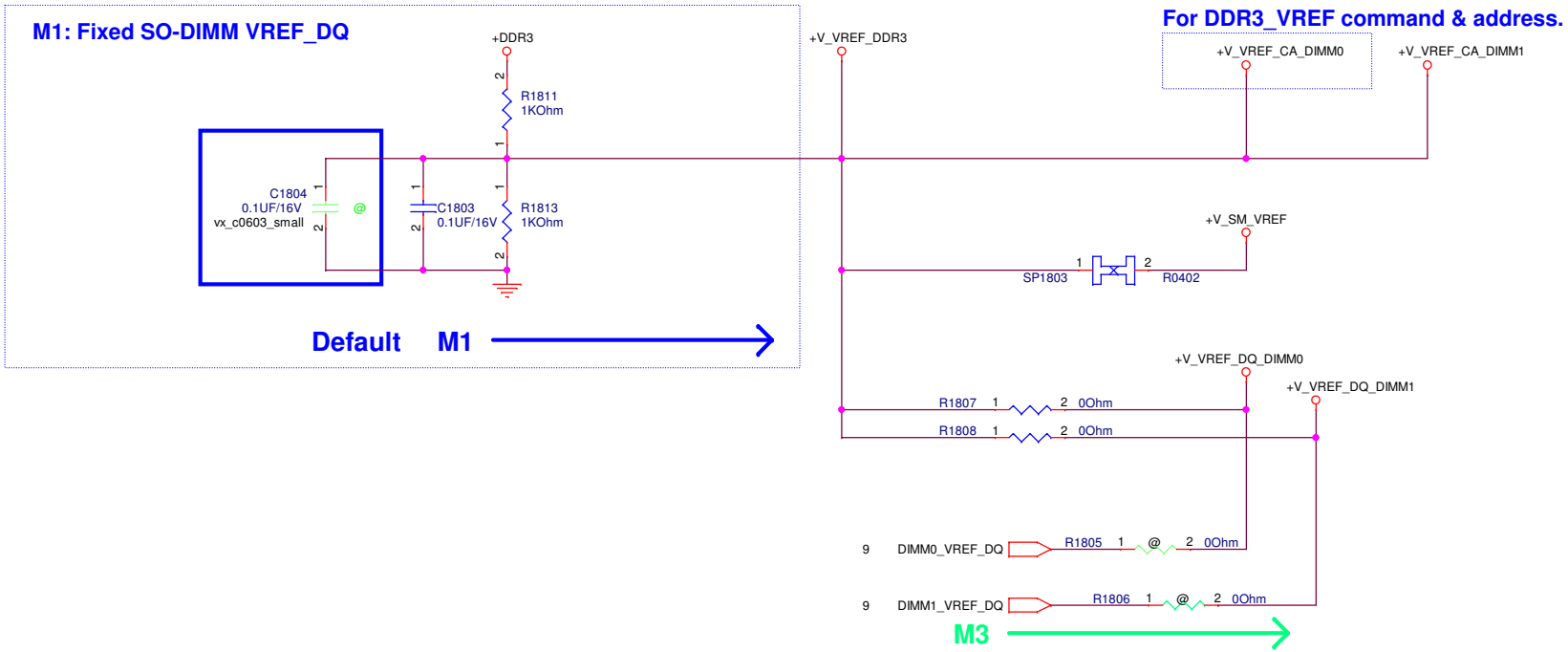
Size	Project Name	Rev
Custom	B34	2.1

Date: Wednesday, February 01, 2012 Sheet 17 of 98

DDR3 Vref

+DDR3 — +DDR3 5,7,16,17,57,83
+V_VREF_CA_DIMM0 — +V_VREF_CA_DIMM0 16,17
+V_VREF_DQ_DIMM0 — +V_VREF_DQ_DIMM0 16
+V_SM_VREF — +V_SM_VREF 7,83

+3V — +3V 24,40,53,55,57,62,91
+5VSUS — +5VSUS 27,52,81,91
+5VA — +5VA 50,52,56,81



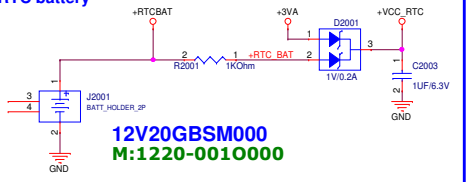
If support M3 :
1. Mount R1802,R1803,R1805,R1806,R1810,R1811,C1802
2. Un mount R1801,R1804

PEGATRON Title :DDR3(3)_CA/DQ Voltage
BG1-HW RD Div.2-NB RD Dept.5 Engineer: Trunks Chen

Size	Project Name	Rev
B	B34	1.0

Date: Wednesday, February 01, 2012 Sheet 18 of 59

RTC battery



12V20GBSM000
M:1220-001O000

Request by CSC for CMOS clear function

CMOS Settings	JRST2001
Clear CMOS	Shunt
Keep CMOS	Open (Default)

TPM Settings	JRST2002
Clear ME RTC Registers	Shunt
Keep ME RTC Registers	Open (Default)

+VCC_RTC RTCRST# RC delay should be 18ms~25ms

R2003 20KOhm, C2004 1UF/6.3V, JRST2001 SGL_JUMP @

R2004 20KOhm, R2005 1MOhm, C2005 1UF/6.3V, JRST2002 SGL_JUMP @

INTVRMEN: Integrated SUS 1.05V VRM Enables
Low: Enable External VRs
High:Enable Internal VRs

PCH_INTVRMEN R2030 330KOhm 1% @

PN change to 10V220000058

C2006 27PF/50V @

38 ACZ_BCLK_AUD_M R2046 33Ohm ACZ_BCLK

38 ACZ_SYNC_AUD_M R2008 1MOhm @ +12VS Q2010 2N7002 ACZ_SYNC_C R2057 33Ohm ACZ_SYNC

reference UB3 modify

38 ACZ_RST#_AUD_M R2058 33Ohm ACZ_RST#

38 ACZ_SDOUT_AUD_M R2059 33Ohm ACZ_SDOUT

C2001 18PF/50V, X2001 32.768KHZ, R2002 10MOhm, SP2005 NB_R0402_5MIL_SMALL

C2002 18PF/50V

T2015, T2011, T2012

+VCC_RTC 330KOhm 1% R2006

PN change to 10V220000058

38 SB_SPKR

38 ACZ_SDIN0

T2025, T2022

T2003 HDA_DOCK_EN#

T2002 HDA_DOCK_RST#

T2028 PCH_JTAG_TCK_BUF
T2029 PCH_JTAG_TMS
T2030 PCH_JTAG_TDI
T2031 PCH_JTAG_TDO

28 SPI_CLK
28 SPI_CS#0
T2004 SPI_CS#1
28 SPI_SI
28 SPI_SO

U2001A

RTC_X1	A20	RTCX1	RTC
RTC_X2	C20	RTCX2	
RTC_RST#	D20	RTCRST#	
SRTC_RST#	G22	SRTCRST#	
SM_INTRUDER#	K22	INTRUDER#	
PCH_INTVRMEN	C17	INTVRMEN	
ACZ_BCLK	N34	HDA_BCLK	LHDA
ACZ_SYNC	L34	HDA_SYNC	
	T10	SPKR	
ACZ_RST#	K34	HDA_RST#	
	E34	HDA_SDIN0	
	G34	HDA_SDIN1	
	C34	HDA_SDIN2	
	A34	HDA_SDIN3	
ACZ_SDOUT	A36	HDA_SDO	
	C36	HDA_DOCK_EN#/GPIO33	
	N32	HDA_DOCK_RST#/GPIO13	
	J3	JTAG_TCK	JTAG
	H7	JTAG_TMS	
	K5	JTAG_TDI	
	H1	JTAG_TDO	
	T3	SPI_CLK	SPI
	Y14	SPI_CS0#	
	T1	SPI_CS1#	
	V4	SPI_MOSI	
	U3	SPI_MISO	

COUGAR_POINT_ES1

	C38	FWH0/LAD0	LPC
	A38	FWH1/LAD1	
	B37	FWH2/LAD2	
	C37	FWH3/LAD3	
	D36	FWH4/LFRAME#	
	E36	LDRQ0#	
	K36	LDRQ1#/GPIO23	
	V5	SERIRQ	
	AM3	SATA0RXN	SATA_G6
	AM1	SATA0RXP	
	AP7	SATA0TXN	
	AP5	SATA0TXP	
	AM10	SATA1RXN	
	AM8	SATA1RXP	
	AP11	SATA1TXN	
	AP10	SATA1TXP	
	AD7	SATA2RXN	
	AD5	SATA2RXP	
	AH5	SATA2TXN	
	AH4	SATA2TXP	
	AB8	SATA3RXN	
	AB10	SATA3RXP	
	AF3	SATA3TXN	
	AF1	SATA3TXP	
	Y7	SATA4RXN	SATA
	Y5	SATA4RXP	
	AD3	SATA4TXN	
	AD1	SATA4TXP	
	Y3	SATA5RXN	
	Y1	SATA5RXP	
	AB3	SATA5TXN	
	AB1	SATA5TXP	
	Y11	SATAICOMPO	
	Y10	SATAICOMPI	
	AB12	SATA3RCOMPO	
	AB13	SATA3COMPI	
	AH1	SATA3RBIAS	
	P3	SATALED#	
	V14	SATA0GP/GPIO21	
	P1	SATA1GP/GPIO19	

LPC_AD0 30,44,62
LPC_AD1 30,44,62
LPC_AD2 30,44,62
LPC_AD3 30,44,62
LPC_FRAME# 30,44,62
T2024, T2023
SNN_PCH_DRQ#0
SNN_LPC_DRQ#1
INT_SERIRQ 30,44,62

HDD1_mSATA SSD
SATA_RXN0 51
SATA_RXP0 51
SATA_TXN0 51
SATA_TXP0 51

ODD R1.1
SATA_RXN2 51
SATA_RXP2 51
SATA_TXN2 51
SATA_TXP2 51

for 14" reserve
HDD2_7mm SATA SSD
SATA_RXN4 51
SATA_RXP4 51
SATA_TXN4 51
SATA_TXP4 51

R1.1
Intel Comments
R2007 = 37.4 ohm
R2047 = 49.9 ohm

SATA_COMP R2007 1 1% 2 37.4Ohm +VTT_PCH_VCCIO
SATA3_COMP R2047 1 1% 2 49.9Ohm +VTT_PCH_VCCIO
RBIAS_SATA3 R2048 1 1% 2 750Ohm GND

R2025 10KOhm +3VS
SATA_LED# SATA_LED# 56
SATA0GP
BBS_BIT0_R SP2003 NB_R0402_5MIL_SMALL BBS_BIT0 24

0200-00HU000 C.S 907552 A1 QMVY BGA942 INTEL/COUGAR POINT PCH

+VCC_RTC +VCC_RTC 22,27
+3VA +3VA 6,27,30,56,57,81,88,93
+3VS +3VS 16,17,21,22,23,24,25,26,27,28,30,31,32,33,38,44,45,46,48,50,51,53,56,57,62,66,80,85,91,92
+3VSUS_ORG +3VSUS_ORG 21,22,24,25,27
+VTT_PCH_VCCIO +VTT_PCH_VCCIO 26,27

Strap information:

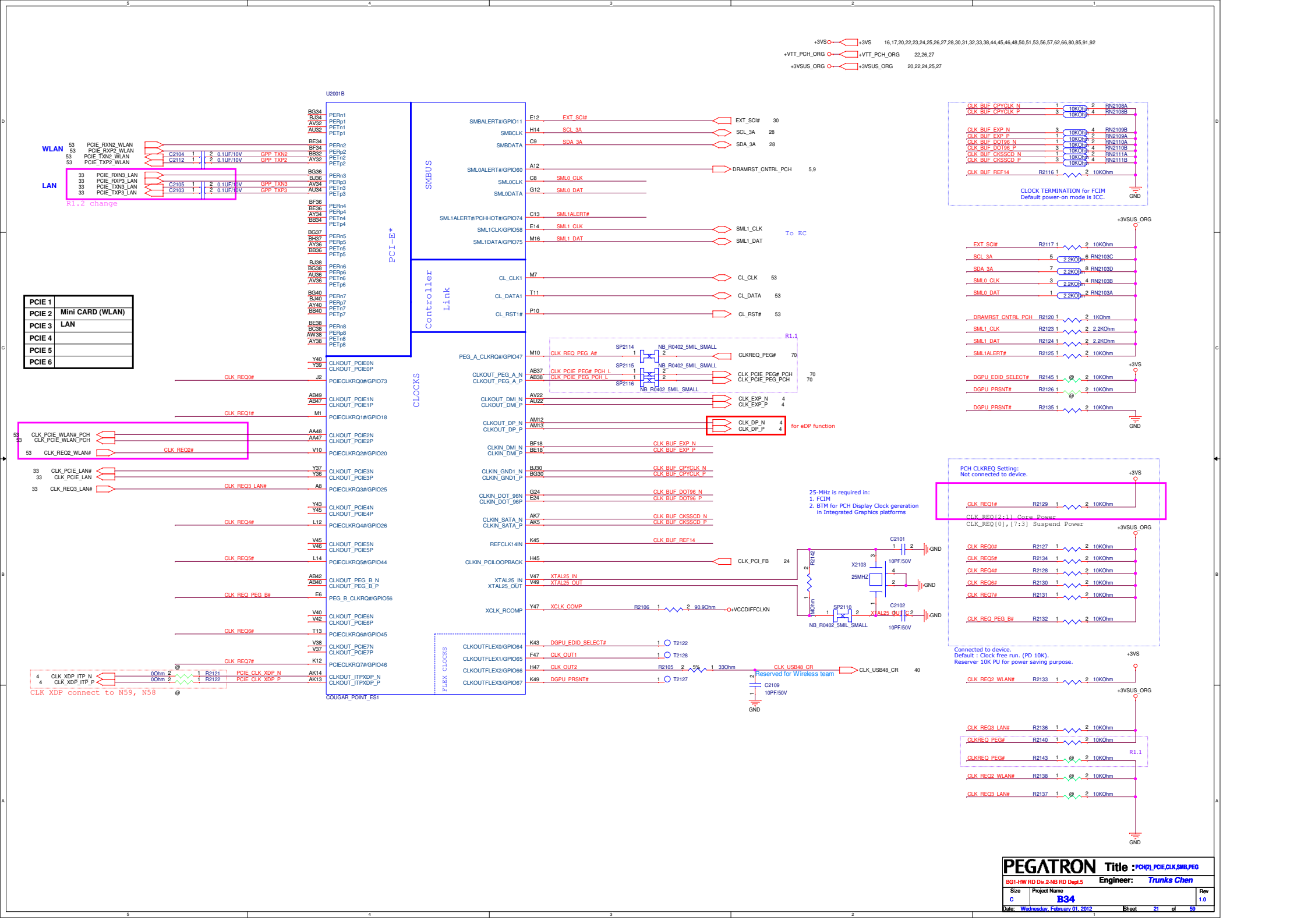
SB_SPKR: No reboot strap
Low: Disable (Default)
High:Enable
SB_SPKR R2020 1 @ 2 1KOhm +3VS

ACZ_SDOUT:
1.Flash descriptor security:
Sampled Low: in effect.
Sampled High: override
2.ACZ_SDOUTwhich sample high on the rising edge of PWROK
Will also disable Intel ME.
ACZ_SDOUT R2034 1 @ 2 1KOhm +3VSUS_ORG

ACZ_SYNC: On Die PLL VR voltage selector
Low: 1.8V (Default)
High: 1.5V
note : CRB has no strap
Hrron River Platform Schematic Design Checklist
(438390 page 48)
ACZ_SYNC R2036 1 2 1KOhm +3VSUS_ORG
VCCVRAM use +1.5VS in mobile

Pull High
+3VS
INT_SERIRQ R2026 10KOhm
SATA0GP R2027 10KOhm

PEGATRON Title : PCH(1)_SATA,HDA,RTC,LPC
BG1-HW RD Div.2-NB RD Dept.5 Engineer: Trunks Chen
Size C | Project Name B34 | Rev 1.0
Date: Wednesday, February 01, 2012 | Sheet 20 of 59


+3VS +3VS 16,17,20,22,23,24,25,26,27,28,30,31,32,33,38,44,45,46,48,50,51,53,56,57,62,66,80,85,91,92
+VTT_PCH_ORG +VTT_PCH_ORG 22,26,27
+3VSUS_ORG +3VSUS_ORG 20,22,24,25,27
U2001B
PCI-E*
SMBUS
Controller Link
CLOCKS
FLEX CLOCKS
COUGAR_POINT_ES1
WLAN
LAN
R1.2 change
PCIE_RXN2_WLAN
PCIE_RXP2_WLAN
PCIE_TXN2_WLAN
PCIE_TXP2_WLAN
PCIE_RXN3_LAN
PCIE_RXP3_LAN
PCIE_TXN3_LAN
PCIE_TXP3_LAN
C2104 0.1UF/10V GPP_TXN2
C2112 0.1UF/10V GPP_TXP2
C2105 0.1UF/10V GPP_TXN3
C2103 0.1UF/10V GPP_TXP3
PCIE 1
PCIE 2 Mini CARD (WLAN)
PCIE 3 LAN
PCIE 4
PCIE 5
PCIE 6
CLK_REQ0#
CLK_REQ1#
CLK_REQ2#
CLK_REQ3_LAN#
CLK_REQ4#
CLK_REQ5#
CLK_REQ_PEG_B#
CLK_REQ6#
CLK_REQ7#
CLK_PCIE_WLAN#_PCH
CLK_PCIE_WLAN_PCH
CLK_REQ2_WLAN#
CLK_PCIE_LAN#
CLK_PCIE_LAN
CLK_REQ3_LAN#
CLK_XDP_ITP_N
CLK_XDP_ITP_P
0Ohm
R2121
R2122
PCIE_CLK_XDP_N
PCIE_CLK_XDP_P
CLK XDP connect to N59, N58
SMBALERT#/GPIO11
SMBCLK
SMBDATA
SML0ALERT#/GPIO60
SML0CLK
SML0DATA
SML1ALERT#/PCHHOT#/GPIO74
SML1CLK/GPIO58
SML1DATA/GPIO75
EXT_SCI#
SCL_3A
SDA_3A
DRAMRST_CNTRL_PCH
SML0_CLK
SML0_DAT
SML1ALERT#
SML1_CLK
SML1_DAT
To EC
CL_CLK1
CL_DATA1
CL_RST1#
CL_CLK
CL_DATA
CL_RST#
PEG_A_CLKRQ#/GPIO47
CLK_REQ_PEG_A#
CLKREQ_PEG#
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLK_PCIE_PEG#_PCH_L
CLK_PCIE_PEG_PCH_L
CLK_PCIE_PEG#_PCH
CLK_PCIE_PEG_PCH
SP2114 NB_R0402_5MIL_SMALL
SP2115 NB_R0402_5MIL_SMALL
SP2116 NB_R0402_5MIL_SMALL
R1.1
CLKOUT_DMI_N
CLKOUT_DMI_P
CLK_EXP_N
CLK_EXP_P
CLKOUT_DP_N
CLKOUT_DP_P
CLK_DP_N
CLK_DP_P
for eDP function
CLKIN_DMI_N
CLKIN_DMI_P
CLK_BUF_EXP_N
CLK_BUF_EXP_P
CLKIN_GND1_N
CLKIN_GND1_P
CLK_BUF_CPYCLK_N
CLK_BUF_CPYCLK_P
CLKIN_DOT_96N
CLKIN_DOT_96P
CLK_BUF_DOT96_N
CLK_BUF_DOT96_P
CLKIN_SATA_N
CLKIN_SATA_P
CLK_BUF_CKSSCD_N
CLK_BUF_CKSSCD_P
REFCLK14IN
CLK_BUF_REF14
CLKIN_PCILOOPBACK
CLK_PCI_FB
XTAL25_IN
XTAL25_OUT
XCLK_COMP
R2106 90.9Ohm
VCCDIFFCLKN
25-MHz is required in:
1. FCIM
2. BTM for PCH Display Clock gereration in Integrated Graphics platforms
R2142 1MOhm
X2103 25MHZ
C2101 10PF/50V
C2102 10PF/50V
SP2110 NB_R0402_5MIL_SMALL
CLKOUTFLEX0/GPIO64
CLKOUTFLEX1/GPIO65
CLKOUTFLEX2/GPIO66
CLKOUTFLEX3/GPIO67
DGPU_EDID_SELECT#
CLK_OUT1
CLK_OUT2
DGPU_PRSNT#
T2122
T2128
T2127
R2105 5% 33Ohm
CLK_USB48_CR
Reserved for Wireless team
C2109 10PF/50V
CLK_BUF_CPYCLK_N
CLK_BUF_CPYCLK_P
CLK_BUF_EXP_N
CLK_BUF_EXP_P
CLK_BUF_DOT96_N
CLK_BUF_DOT96_P
CLK_BUF_CKSSCD_N
CLK_BUF_CKSSCD_P
CLK_BUF_REF14
R2116 10KOhm
RN2108A RN2108B RN2109B RN2109A RN2110A RN2110B RN2111A RN2111B
CLOCK TERMINATION for FCIM
Default power-on mode is ICC.
GND
+3VSUS_ORG
EXT_SCI# R2117 10KOhm
SCL_3A RN2103C
SDA_3A RN2103D
SML0_CLK RN2103B
SML0_DAT RN2103A
2.2KOhm
DRAMRST_CNTRL_PCH R2120 1KOhm
SML1_CLK R2123 2.2KOhm
SML1_DAT R2124 2.2KOhm
SML1ALERT# R2125 10KOhm
+3VS
DGPU_EDID_SELECT# R2145 10KOhm
DGPU_PRSNT# R2126 10KOhm
DGPU_PRSNT# R2135 10KOhm
PCH CLKREQ Setting:
Not connected to device.
CLK_REQ1# R2129 10KOhm
CLK_REQ[2:1] Core Power
CLK_REQ[0],[7:3] Suspend Power
CLK_REQ0# R2127 10KOhm
CLK_REQ5# R2134 10KOhm
CLK_REQ4# R2128 10KOhm
CLK_REQ6# R2130 10KOhm
CLK_REQ7# R2131 10KOhm
CLK_REQ_PEG_B# R2132 10KOhm
Connected to device.
Default : Clock free run. (PD 10K).
Reserver 10K PU for power saving purpose.
CLK_REQ2_WLAN# R2133 10KOhm
CLK_REQ3_LAN# R2136 10KOhm
CLKREQ_PEG# R2140 10KOhm
CLKREQ_PEG# R2143 10KOhm
CLK_REQ2_WLAN# R2138 10KOhm
CLK_REQ3_LAN# R2137 10KOhm
PEGATRON Title : PCH(2)_PCIE,CLK,SMB,PEG
BG1-HW RD Div.2-NB RD Dept.5 Engineer: Trunks Chen
Size C Project Name B34 Rev 1.0
Date: Wednesday, February 01, 2012 Sheet 21 of 59

+3VSUS_ORG — +3VSUS_ORG 20,21,24,25,27

+3VS — +3VS 16,17,20,21,23,24,25,26,27,28,30,31,32,33,38,44,45,46,48,50,51,53,56,57,62,66,80,85,91,92

+VTT_PCH_ORG — +VTT_PCH_ORG 26,27

+3VA — +3VA 6,20,27,30,56,57,81,88,93

+VCC_RTC — +VCC_RTC 20,27

+3VSUS — +3VSUS 24,27,28,30,33,53,56,81,92

U2001C

DMI_RXN0 3 — BC24 DMI0RXN
DMI_RXN1 3 — BE20 DMI1RXN
DMI_RXN2 3 — BG18 DMI2RXN
DMI_RXN3 3 — BG20 DMI3RXN

DMI_RXP0 3 — BE24 DMI0RXP
DMI_RXP1 3 — BC20 DMI1RXP
DMI_RXP2 3 — BJ18 DMI2RXP
DMI_RXP3 3 — BJ20 DMI3RXP

DMI_TXN0 3 — AW24 DMI0TXN
DMI_TXN1 3 — AW20 DMI1TXN
DMI_TXN2 3 — BB18 DMI2TXN
DMI_TXN3 3 — AV18 DMI3TXN

DMI_TXP0 3 — AY24 DMI0TXP
DMI_TXP1 3 — AY20 DMI1TXP
DMI_TXP2 3 — AY18 DMI2TXP
DMI_TXP3 3 — AU18 DMI3TXP

DMI

FDI_RXN0 — BJ14 — FDI_TXN0 3
FDI_RXN1 — AY14 — FDI_TXN1 3
FDI_RXN2 — BE14 — FDI_TXN2 3
FDI_RXN3 — BH13 — FDI_TXN3 3
FDI_RXN4 — BC12 — FDI_TXN4 3
FDI_RXN5 — BJ12 — FDI_TXN5 3
FDI_RXN6 — BG10 — FDI_TXN6 3
FDI_RXN7 — BG9 — FDI_TXN7 3

FDI_RXP0 — BG14 — FDI_TXP0 3
FDI_RXP1 — BB14 — FDI_TXP1 3
FDI_RXP2 — BF14 — FDI_TXP2 3
FDI_RXP3 — BG13 — FDI_TXP3 3
FDI_RXP4 — BE12 — FDI_TXP4 3
FDI_RXP5 — BG12 — FDI_TXP5 3
FDI_RXP6 — BJ10 — FDI_TXP6 3
FDI_RXP7 — BH9 — FDI_TXP7 3

FDI_INT — AW16 — FDI_INT 3
FDI_FSYNC0 — AV12 — FDI_FSYNC0 3
FDI_FSYNC1 — BC10 — FDI_FSYNC1 3
FDI_LSYNC0 — AV14 — FDI_LSYNC0 3
FDI_LSYNC1 — BB10 — FDI_LSYNC1 3

FDI

DMI_ZCOMP — BJ24
DMI_IRCOMP — BG25
DMI2RBIAS — BH21

+VTT_PCH_ORG — R2201 2 1% 1 49.9Ohm DMI_COMP_R
GND — R2202 2 1% 1 750Ohm RBIAS_CPY

DSWVRMEN — A18 — R2215 1 @ 2 330KOhm; R2214 1 1% 2 330KOhm; GND; +VCC_RTC
PN change to 10Y220000058
DSWODVREN - On Die DSW VR Enable
HIGH - Enabled(DEFAULT) ; LOW-Disabled

SUS_PWR_ACK_R — R2213 — SUSACK# C12
DPWROK — E22 — R2216 — PM_RSMRST_R
+3VS — R2205 2 1 10KOhm PM_SYSRST#_R — SYS_RESET# K3
WAKE# — B9 — PCIE_WAKE# 33,53
SYS_PWROK — SYS_PWROK P12
CLKRUN#/GPIO32 — N3 — PM_CLKRUN# 30,62
4,30,92 PM_PWROK — SP2212 NB_R0402_5MIL_SMALL — PM_PCH_PWROK_R — PWROK L22
SUS_STAT#/GPIO61 — G8 PM_SUS_STAT# — PM_SUS_STAT# 62
30 ME_PWROK — R2208 2 /SBA 1 0Ohm; R2217 2 1 0Ohm non-SBA — PM_APWROK_R — APWROK L10
SUSCLK/GPIO62 — N14 SUSCLK_C — SP2215 NB_R0402_5MIL_SMALL — SUSCLK 30
4 PM_DRAM_PWRGD — DRAMPWROK B13
SLP_S5#/GPIO63 — D10 SLP_S5# — T2204
PM_RSMRST# has pull down 10k ohm in EC
30 PM_RSMRST# — SP2213 NB_R0402_5MIL_SMALL — PM_RSMRST_R — RSMRST# C21
SLP_S4# — H4 — PM_SUSC# 30
30 ME_SUSPWRDNACK — R2211 2 /SBA 1 0Ohm — SUS_PWR_ACK_R — SUSWARN#/SUSPWRDNACK/GPIO30 K16
SLP_S3# — F4 — PM_SUSB# 30
30 PM_PWRBTN# — SP2214 NB_R0402_5MIL_SMALL — PWRBTN# E20
SLP_A# — G10 ME_PM_SLP_A# — R2210 2 /SBA 1 0Ohm — ME_PM_SLP_M# 30
30 ME_AC_PRESENT — R2212 2 /SBA 1 0Ohm — ME_AC_PRESENT_R — ACPRESENT/GPIO31 H20
SLP_SUS# — G16 SLP_DSW#_R — T2205
T2201 — BATLOW# — BATLOW#/GPIO72 E10
PMSYNCH — AP14 — H_PM_SYNC 4
T2202 — RI# — RI# A10
SLP_LAN#/GPIO29 — K14 GPIO29 — R2209 2 /SBA 1 0Ohm — ME_PM_SLP_LAN# 30

System Power Management

COUGAR_POINT_ES1

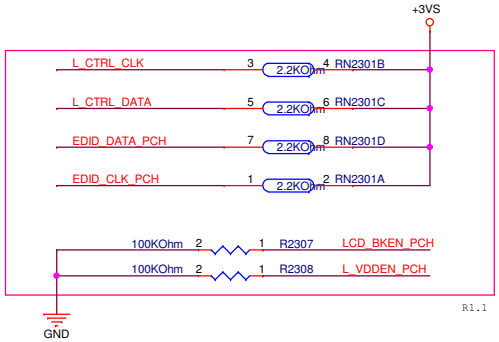
92 DELAY_VR_AND_ALL_SYS — SP2209 NB_R0402_5MIL_SMALL; SP2210 NB_R0402_5MIL_SMALL; PM_PWROK; U2201 (VCC, GND, Vcc=2~5.5); +3VSUS — SYS_PWROK

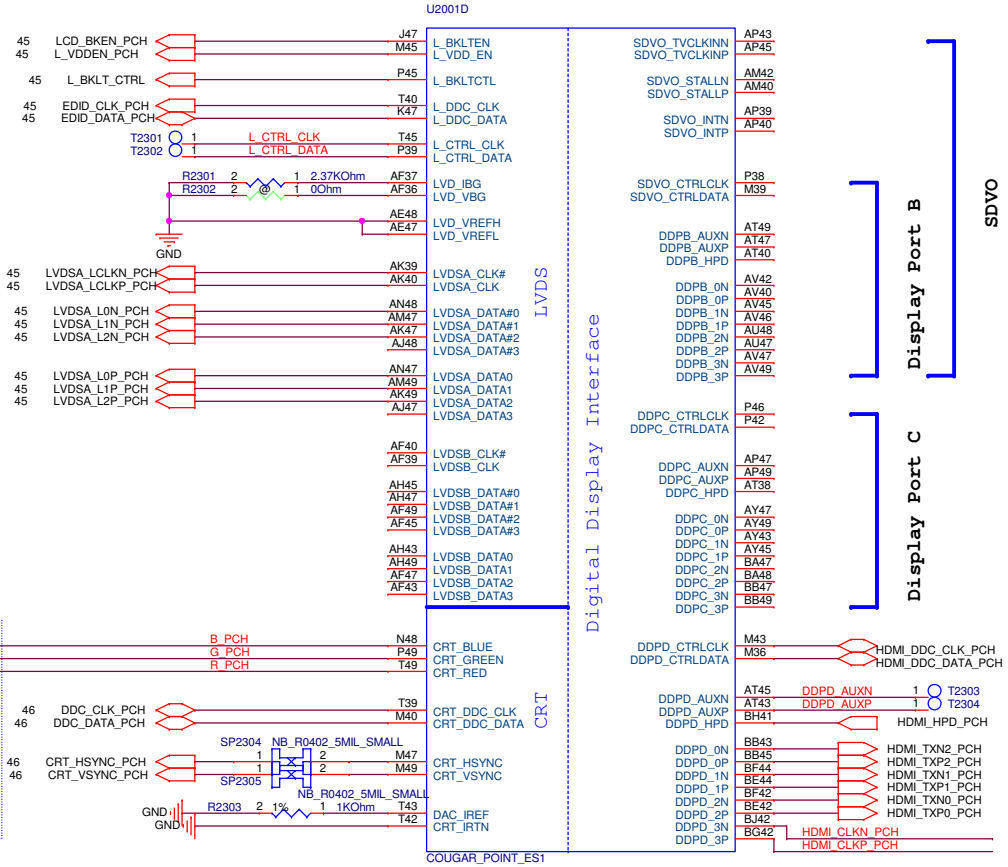
+3VSUS_ORG
RI# — R2223 1 2 10KOhm
BATLOW# — R2224 1 2 10KOhm
PCIE_WAKE# — R2225 1 2 1KOhm @
ME_PM_SLP_A# — R2230 1 2 10KOhm
SUS_PWR_ACK_R — R2227 1 2 10KOhm
ME_AC_PRESENT — R2228 1 2 10KOhm
GPIO29 — R2229 1 2 10KOhm

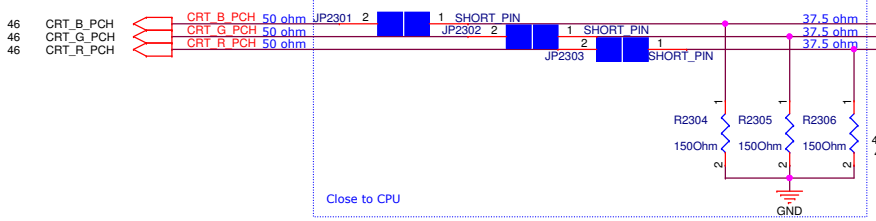
+3VS
PM_CLKRUN# — R2220 1 2 10KOhm
PM_PWROK — R2221 1 2 10KOhm
GND

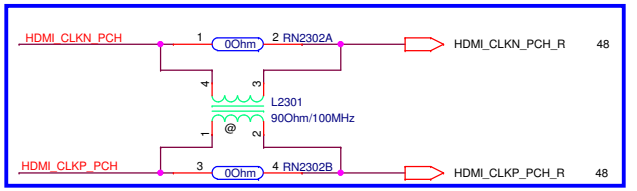
PEGATRON Title : PCH(3)_FDI,DMI,SYS PWR
BG1-HW RD Div.2-NB RD Dept.5 Engineer: Trunks Chen
Size: Custom | Project Name: B34 | Rev: 1.0
Date: Wednesday, February 01, 2012 | Sheet 22 of 59

+3VS +3VS 16,17,20,21,22,24,25,26,27,28,30,31,32,33,38,44,45,46,48,50,51,53,56,57,62,66,80,85,91,92









CRT Disable: (For discrete graphic)

1. NC:
   CRT_RED,CRT_GREEN,CRT_BLUE
   CRT_HSYCN,CRT_VSYNC
2. 1-kΩ ±0.5% pull-down to GND:
   DAC_IREF
3. Connected to GND:
   CRT_ITRN
4. Connect to +V3.3:
   VCCADAC

DisPlay Port Disable: (For UMA)

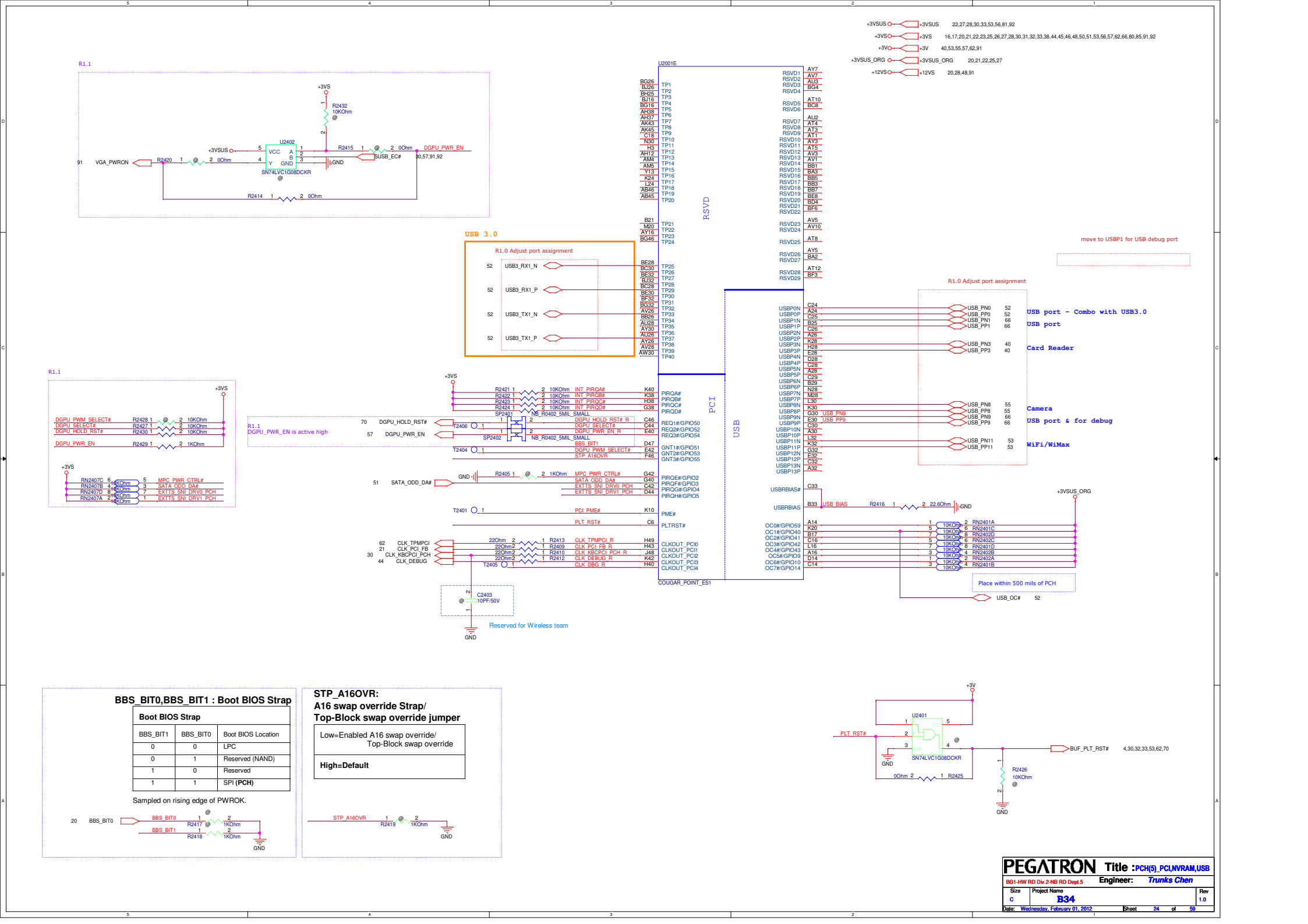
1. NC:
   ALL

PEGATRON Title : PCH(4)_DP,LVDS,CRT

BG1-HW RD Div.2-NB RD Dept.5 Engineer: Trunks Chen

Size	Project Name	Rev
Custom	B34	1.0

Date: Wednesday, February 01, 2012 Sheet 23 of 59


+3VSUS 22,27,28,30,33,53,56,81,92
+3VS 16,17,20,21,22,23,25,26,27,28,30,31,32,33,38,44,45,46,48,50,51,53,56,57,62,66,80,85,91,92
+3V 40,53,55,57,62,91
+3VSUS_ORG 20,21,22,25,27
+12VS 20,28,48,91
R1.1
U2001E
RSVD
USB 3.0
R1.0 Adjust port assignment
USB3_RX1_N
USB3_RX1_P
USB3_TX1_N
USB3_TX1_P
move to USBP1 for USB debug port
USB port - Combo with USB3.0
USB port
Card Reader
Camera
USB port & for debug
WiFi/WiMax
PCI
USB
COUGAR_POINT_ES1
R1.1
DGPU_PWR_EN is active high
Place within 500 mils of PCH
Reserved for Wireless team
BBS_BIT0,BBS_BIT1 : Boot BIOS Strap
Boot BIOS Strap
BBS_BIT1 BBS_BIT0 Boot BIOS Location
0 0 LPC
0 1 Reserved (NAND)
1 0 Reserved
1 1 SPI (PCH)
Sampled on rising edge of PWROK.
STP_A16OVR:
A16 swap override Strap/
Top-Block swap override jumper
Low=Enabled A16 swap override/
Top-Block swap override
High=Default
PEGATRON
Title : PCH(5)_PCI,NVRAM,USB
BG1-HW RD Div.2-NB RD Dept.5
Engineer: Trunks Chen
Size C
Project Name B34
Rev 1.0
Date: Wednesday, February 01, 2012
Sheet 24 of 59

+3VS +3VS 16,17,20,21,22,23,24,26,27,28,30,31,32,33,38,44,45,46,48,50,51,53,56,57,62,66,80,85,91,92

+3VSUS +3VSUS 22,24,27,28,30,33,53,56,81,92

+VCCP +VCCP 3,4,6,7,26,27,30,32,82

+3VSUS_ORG +3VSUS_ORG 20,21,22,24,27

+1.8VS +1.8VS 7,26,80,84

+3VS +3VS

R2525 10KOhm PCB_ID0

R2527 10KOhm PCB_ID1

R2526 10KOhm

R2528 10KOhm

GND GND

+3VS +3VS

R2534 10KOhm PROJECT_ID0

R2549 10KOhm PROJECT_ID1

R2533 10KOhm

R2530 10KOhm

GND GND

ID0	ID1	PCB Rev.
0	0	R1.1 (SR)
0	1	R1.2 (ER)
1	0	R2.0
1	1	R2.1

PROJECT _ID0	PROJECT _ID1	Model
0	0	B14 (UMA)
0	1	B34 (UMA / N13P-GL)
1	0	B74 (UMA / N13P-GS)
1	1	X

U2001F

GPIO0 T7 BMBUSY#/GPIO0

GPIO1 A42 TACH1/GPIO1

T2508 PROJECT_ID0 H36 TACH2/GPIO6

PROJECT_ID1 E38 TACH3/GPIO7

T2506 ICC_EN# C10 GPIO8

LAN_PHY_PWR_CTRL C4 LAN_PHY_PWR_CTRL/GPIO12

30,44 EXT_SMI# SP2501 NB_R0402_5MIL_SMALL G2 GPIO15

SATA_DET#4 U2 SATA4GP/GPIO16

74,75,85,91 DGPU_PWROK 0Ohm R2506 D40 TACH0/GPIO17

56 WLAN_LED T5 SCLOCK/GPIO22

53 AOAC_ON E8 GPIO24/MEM_LED

T2514 GPIO27 E16 GPIO27

53 WLAN_ON SP2502 NB_R0402_5MIL_SMALL P8 GPIO28

PLL_ODVR_EN K1 STP_PCI#/GPIO34

T2516 GPIO35 K4 GPIO35

51 SATA_ODD_PRSNT# V8 SATA2GP/GPIO36

FDI_OVRVLTG M5 SATA3GP/GPIO37

PCB_ID0 N2 SLOAD/GPIO38

PCB_ID1 M3 SDATAOUT0/GPIO39

53 BT_ON/OFF# V13 SDATAOUT1/GPIO48

38 OP_SD# PCH_GPIO49 V3 SATA5GP/GPIO49

56 BT_LED D6 GPIO57

GPIO

A4 Vss_NCTF1

A44 Vss_NCTF2

A45 Vss_NCTF3

A46 Vss_NCTF4

A5 Vss_NCTF5

A6 Vss_NCTF6

B3 Vss_NCTF7

B47 Vss_NCTF8

BD1 Vss_NCTF9

BD49 Vss_NCTF10

BE1 Vss_NCTF11

BE49 Vss_NCTF12

BF1 Vss_NCTF13

BF49 Vss_NCTF14

NCTF

TACH4/GPIO68 C40 SATA_ODD_PWRGT 51

TACH5/GPIO69 B41 R2511 1 2 1.5KOhm GND

TACH6/GPIO70 C41 R2512 1 2 1.5KOhm +3VS

TACH7/GPIO71 A40 R2513 1 2 1.5KOhm +3VS

A20GATE P4 A20GATE 30

PECI AU16 0Ohm R2514 43Ohm R2515 H_PECI 4 H_PECI_EC 30

RCIN# P5 RC_IN# 30

PROCPWRGD AY11 H_CPUPWRGD 4

THRMTRIP# AY10 PM_THRMTRIP# 390Ohm R2516 H_THRMTRIP# 4,32

INIT3_3V# T14 INIT3_3V# T2504

DF_TVS AY1 1KOhm R2548 /IVB /IVB R2547 2.2KOhm +1.8VS H_SNB_IVB# 4

SNB: unmount
IVB: mount 1k ohm

TS_VSS1 AH8

TS_VSS2 AK11

TS_VSS3 AH10

TS_VSS4 AK10

NC_1 P37

GND

TS Signal Disable Guideline
TS_VSS[1:4] should pull down to GND
Design Guide 0.9 (436735)

Vss_NCTF15 BG2

Vss_NCTF16 BG48

Vss_NCTF17 BH3

Vss_NCTF18 BH47

Vss_NCTF19 BJ4

Vss_NCTF20 BJ44

Vss_NCTF21 BJ45

Vss_NCTF22 BJ46

Vss_NCTF23 BJ5

Vss_NCTF24 BJ6

Vss_NCTF25 C2

Vss_NCTF26 C48

Vss_NCTF27 D1

Vss_NCTF28 D49

Vss_NCTF29 E1

Vss_NCTF30 E49

Vss_NCTF31 F1

Vss_NCTF32 F49

COUGAR_POINT_ES1

R1.1

+3VSUS_ORG

EXT_SMI# R2529 1 1% 2 1KOhm

ICC_EN# R2532 2 1 10KOhm

LAN_PHY_PWR_CTRL R2538 2 1 10KOhm

AOAC_ON R2541 2 /AOAC 1 10KOhm

RCIN# has pull high at EC side

R1.1

+3VS

Unused GPIO

PCH_GPIO49 R2539 2 @ 1 10KOhm

DGPU_PWROK R2540 2 1 10KOhm

GPIO0 R2536 2 1 10KOhm

GPIO1 R2545 2 1 10KOhm

STP_PCI# R2537 2 1 10KOhm

SATA_DET#4 R2546 2 1 10KOhm

+3VS R2518 1 1% @ 2 1KOhm FDI_OVRVLTG R2519 1 2 100KOhm GND

FDI TERMINATION VOLTAGE OVERRIDE
- GPIO37 (FDI_OVRVLTG)
LOW - TX, RX terminated to same voltage
(DC Couplong Mode)
DEFAULT

+3VS R2520 1 1% 2 200KOhm SATA_ODD_PRSNT#

DMI TERMINATION VOLTAGE OVERRIDE
- GPIO36 (SATA_ODD_PRSNT#)
LOW - TX, RX terminated to same voltage
(DC Couplong Mode)
DEFAULT

PCH_GPIO49 R2544 2 1 10KOhm

GPIO27 R2523 1 2 10KOhm

DGPU_PWROK R2542 2 @ 1 10KOhm

GND

PLL_ODVR_EN R2521 1 @ 2 1KOhm GND

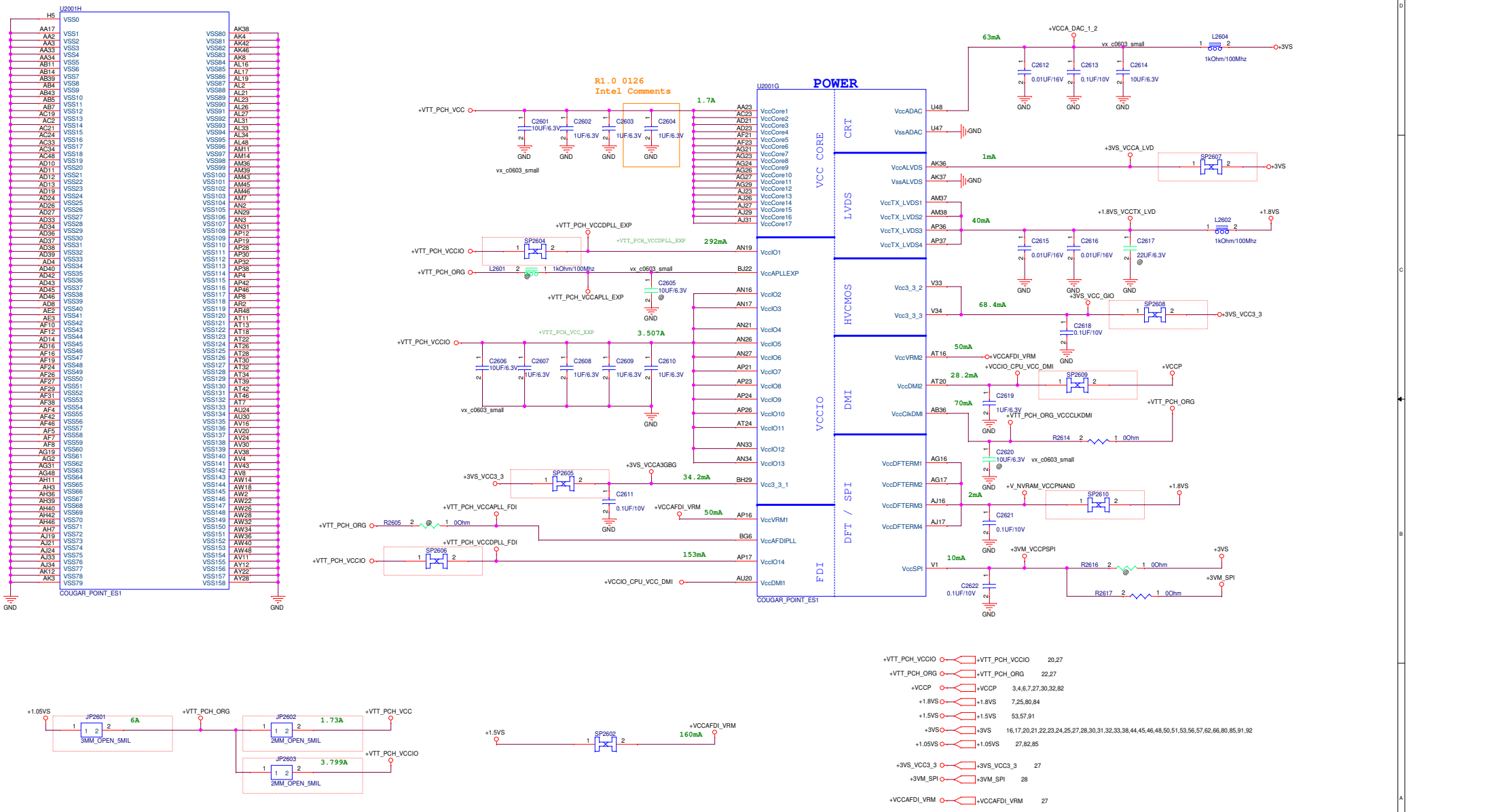
PLL ON DIE VR ENABLE
HIGH - DISABLED (DEFAULT)
LOW - ENABLED

PEGATRON Title : PCH(6)_CPU,GPIO,MISC

BG1-HW RD Div.2-NB RD Dept.5 Engineer: Trunks Chen

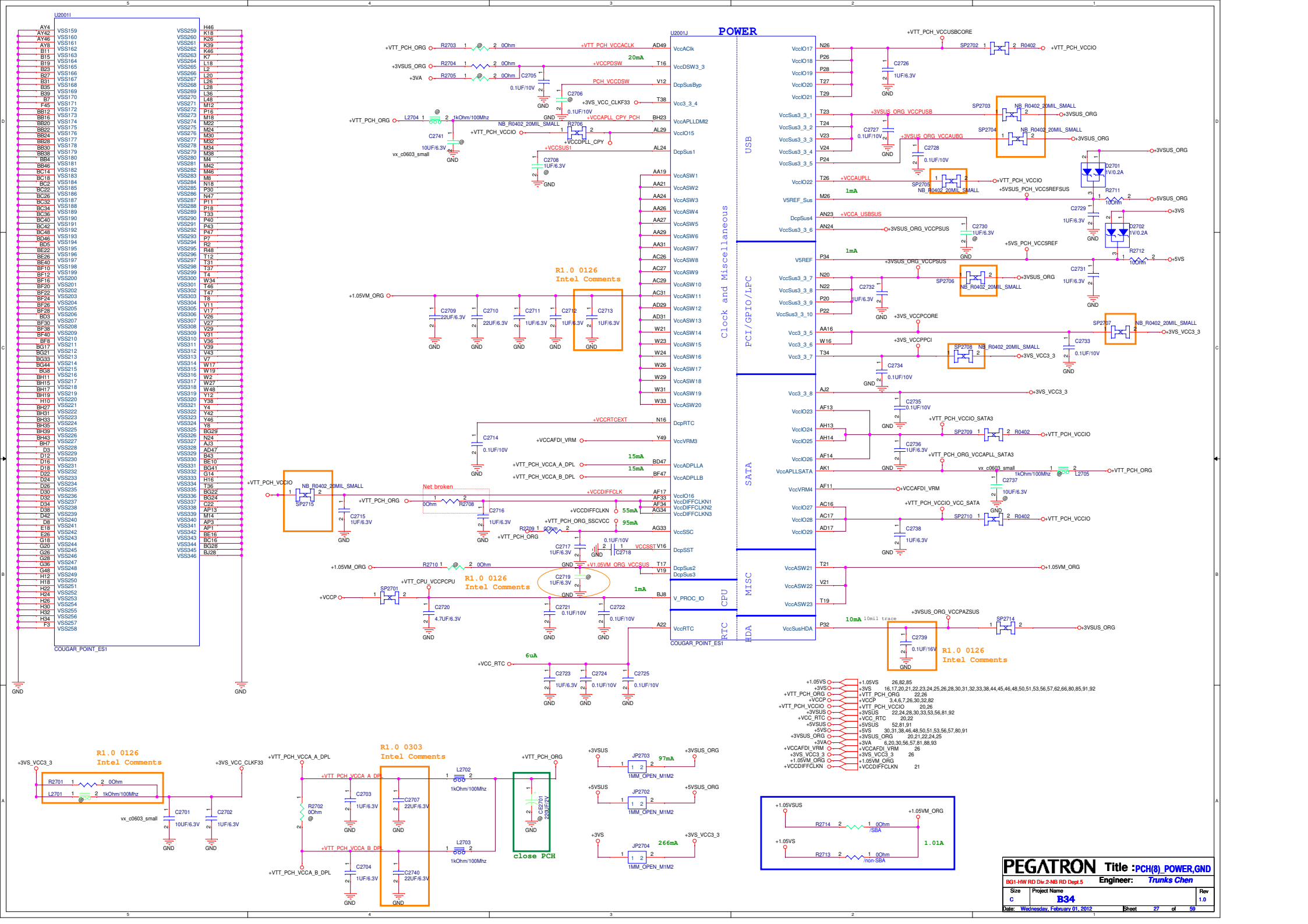
Size	Project Name	Rev
C	B34	1.0

Date: Friday, February 03, 2012 Sheet 25 of 59

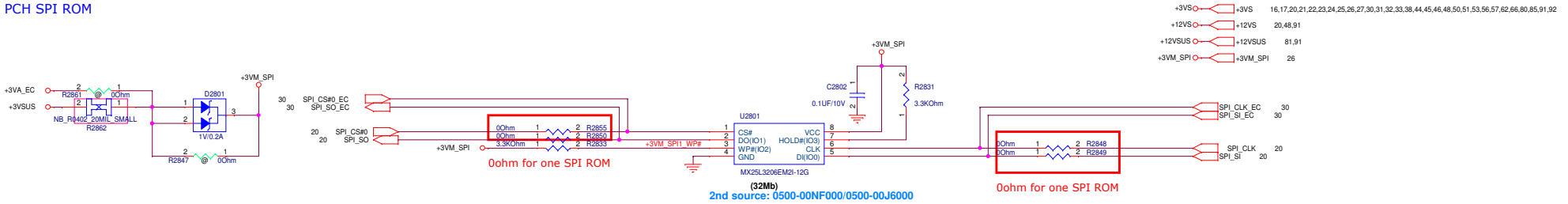


+VTT_PCH_VCCIO 20,27
+VTT_PCH_ORG 22,27
+VCCP 3,4,6,7,27,30,32,82
+1.8VS 7,25,80,84
+1.5VS 53,57,91
+3VS 16,17,20,21,22,23,24,25,27,28,30,31,32,33,38,44,45,46,48,50,51,53,56,57,62,66,80,85,91,92
+1.05VS 27,82,85
+3VS_VCC3_3 27
+3VM_SPI 28
+VCCAFDI_VRM 27

PEGATRON	Title : PCH(7)_POWER,GND		
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Trunks Chen		
Size: C	Project Name: B34		Rev: 1.0
Date: Wednesday, February 01, 2012	Sheet 26 of 59		


POWER
U2001I
COUGAR_POINT_ES1
U2001J
COUGAR_POINT_ES1
USB
Clock and Miscellaneous
PCI/GPIO/LPC
SATA
MISC
CPU
RTC
HDA
R1.0 0126
Intel Comments
R1.0 0303
Intel Comments
close PCH
+VTT_PCH_ORG
+3VSUS_ORG
+3VA
+VCCPDSW
20mA
PCH_VCCDSW
+3VS_VCC_CLKF33
+VCCAPLL_CPY_PCH
+VCCDPLL_CPY
+VCCSUS1
+VTT_PCH_VCCIO
+VCCACLK
+1.05VM_ORG
+VCCRTCEXT
+VCCAFDI_VRM
15mA
+VTT_PCH_VCCA_A_DPL
+VTT_PCH_VCCA_B_DPL
+VCCDIFFCLK
55mA
+VTT_PCH_ORG_SSCVCC
95mA
VCCSST
+1.05VM_ORG_VCCSUS
+VTT_CPU_VCCPCPU
+VCCP
1mA
+VCC_RTC
6uA
+3VSUS_ORG_VCCPUSB
+3VSUS_ORG_VCCAUBG
+VCCAUPLL
+5VSUS_PCH_VCC5REFSUS
+VCCA_USBSUS
+3VSUS_ORG_VCCPSUS
+5VS_PCH_VCC5REF
+3VS_VCCPCORE
+3VS_VCCPPCI
+3VS_VCC3_3
+VTT_PCH_VCCIO_SATA3
+VTT_PCH_ORG_VCCAPLL_SATA3
+VCCAFDI_VRM
+VTT_PCH_VCCIO_VCC_SATA
+3VSUS_ORG_VCCPAZSUS
10mA
10mil trace
+VTT_PCH_VCCUSBCORE
97mA
266mA
JP2703
JP2702
JP2704
1MM_OPEN_M1M2
+1.05VSUS
+1.05VM_ORG
1.01A
R2714
R2713
/SBA
/non-SBA
PEGATRON
Title : PCH(8)_POWER,GND
BG1-HW RD Div.2-NB RD Dept.5
Engineer: Trunks Chen
Size C
Project Name B34
Rev 1.0
Date: Wednesday, February 01, 2012
Sheet 27 of 59

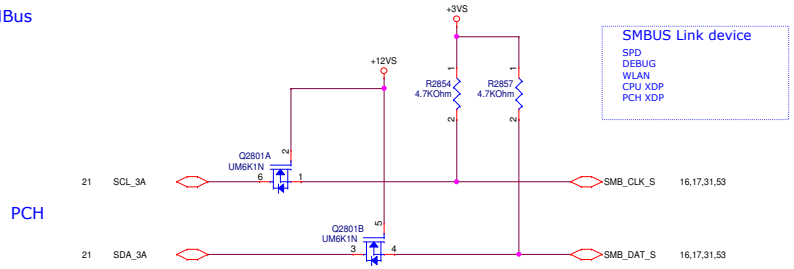
PCH SPI ROM



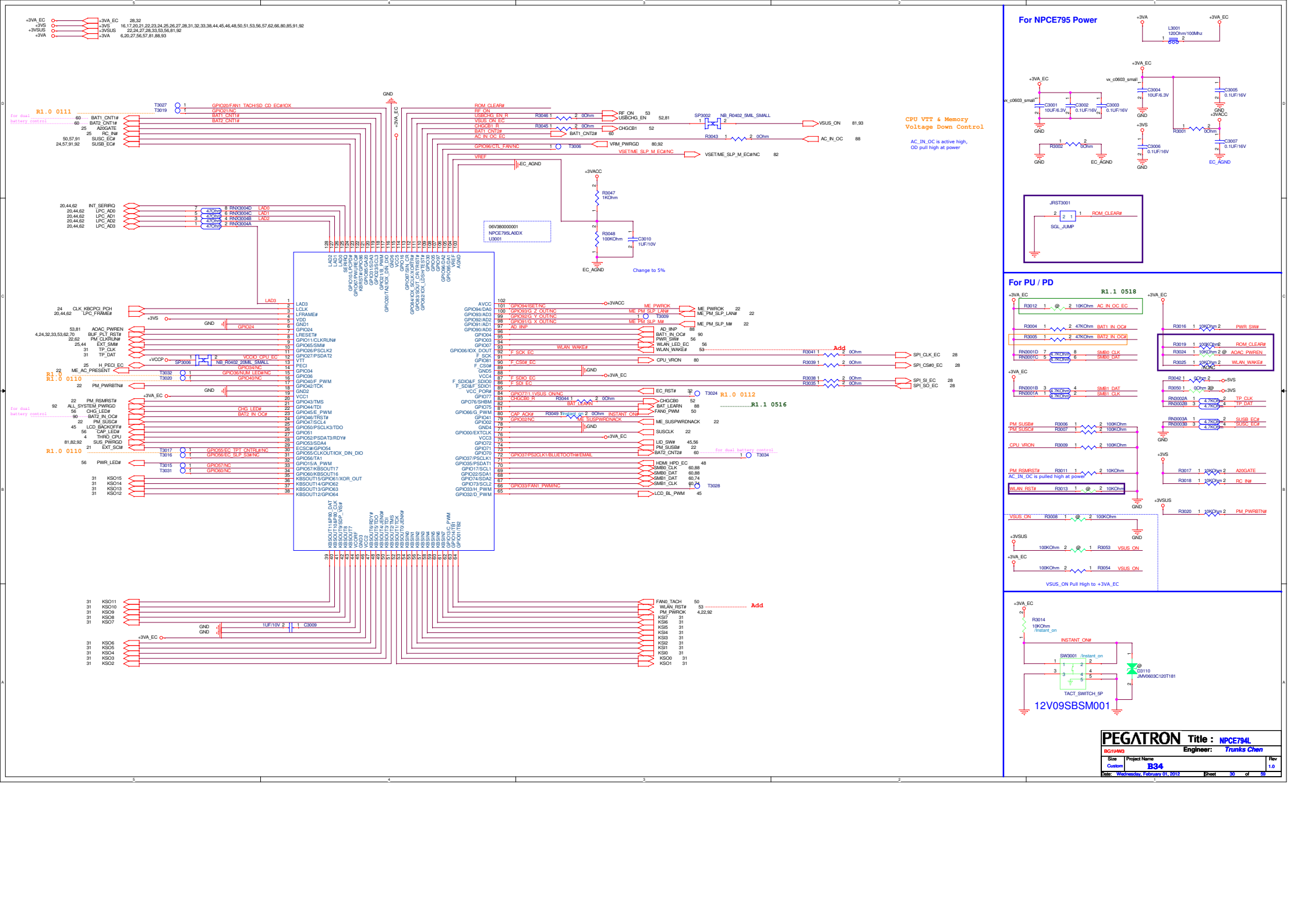
SPI Debug Connector

remove SPI connector

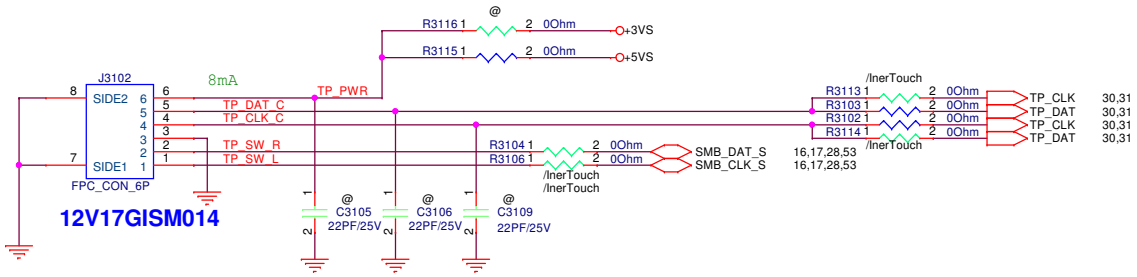
PCH SMBus



PEGATRON	Title : PCH(9)_SPI,SMB	
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Trunks Chen	
Size: C	Project Name: B34	Rev: 1.0
Date: Friday, February 03, 2012	Sheet 28 of 59	

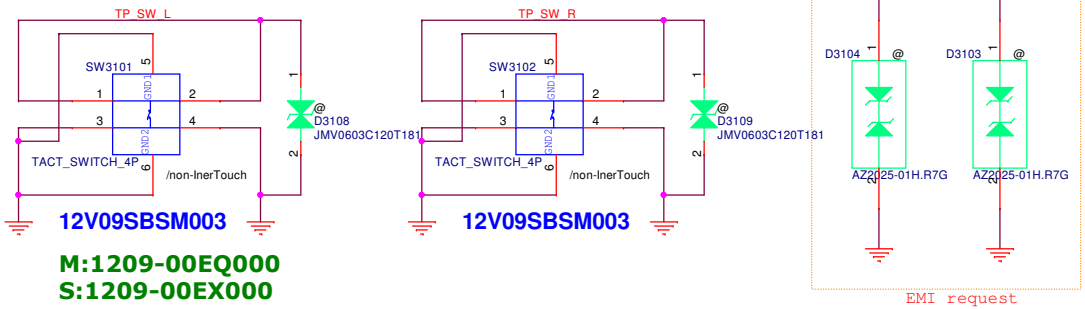

For NPCE795 Power
For PU / PD
CPU VTT & Memory Voltage Down Control
AC_IN_OC is active high, OD pull high at power
Change to 5%
VSUS_ON Pull High to +3VA_EC
12V09SBSM001
PEGATRON
Title : NPCE794L
Engineer: Trunks Chen
BG1/HW3
Size: Custom
Project Name: B34
Rev: 1.0
Date: Wednesday, February 01, 2012
Sheet 30 of 59

Touch Pad for inter touch & clear pad



12V17GISM014

M:1218-00C7000
S:1218-00W8000

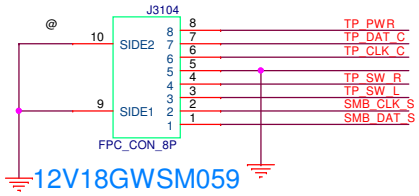


12V09SBSM003

M:1209-00EQ000
S:1209-00EX000

12V09SBSM003

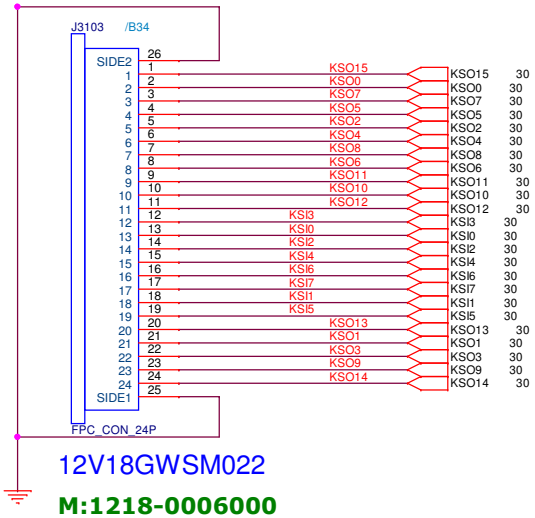
Touch Pad for inter touch & non- clear pad



12V18GWSM059

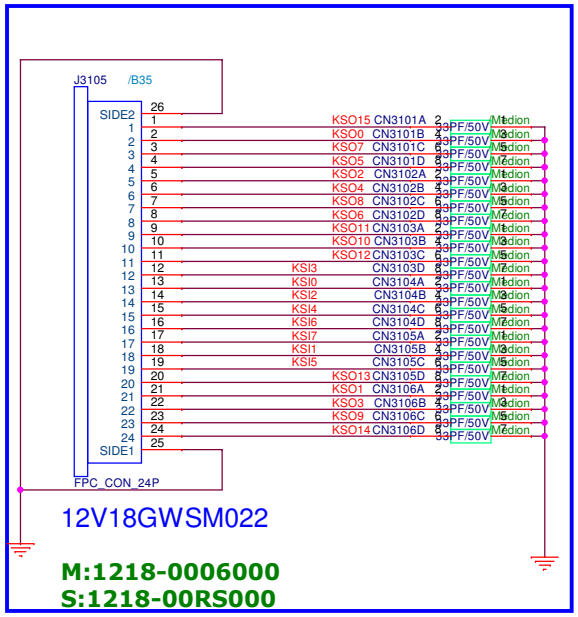
M:1218-006X000
S:1218-01JN000

Keyboard



12V18GWSM022

M:1218-0006000
S:1218-00RS000



12V18GWSM022

M:1218-0006000
S:1218-00RS000

PEGATRON

Title : KB/ TP

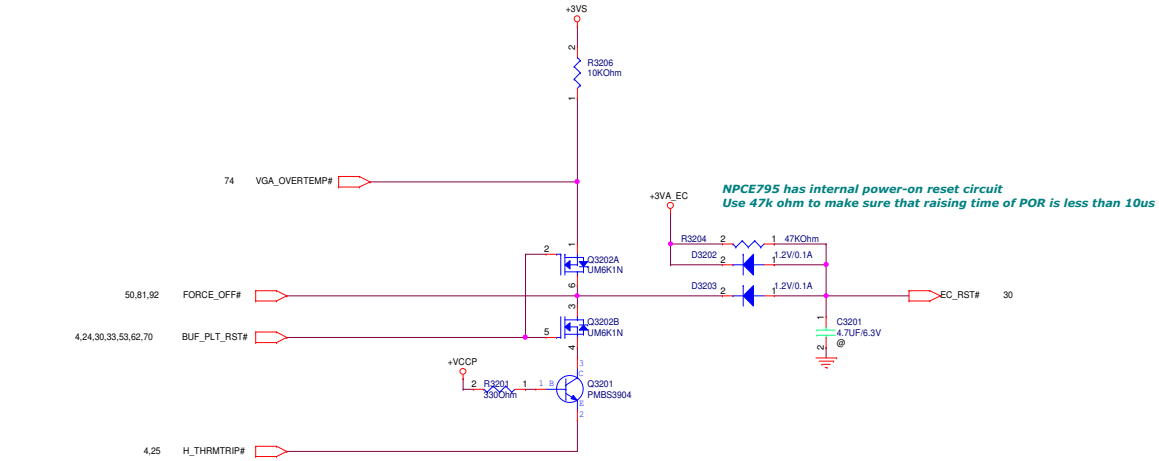
BG1-HW RD Div.2-NB RD Dept.5

Engineer: Trunks Chen

Size	Project Name	Rev
Custom	B34	1.0

Date: Wednesday, February 01, 2012 Sheet 31 of 59

Thermal Policy



Input Signal

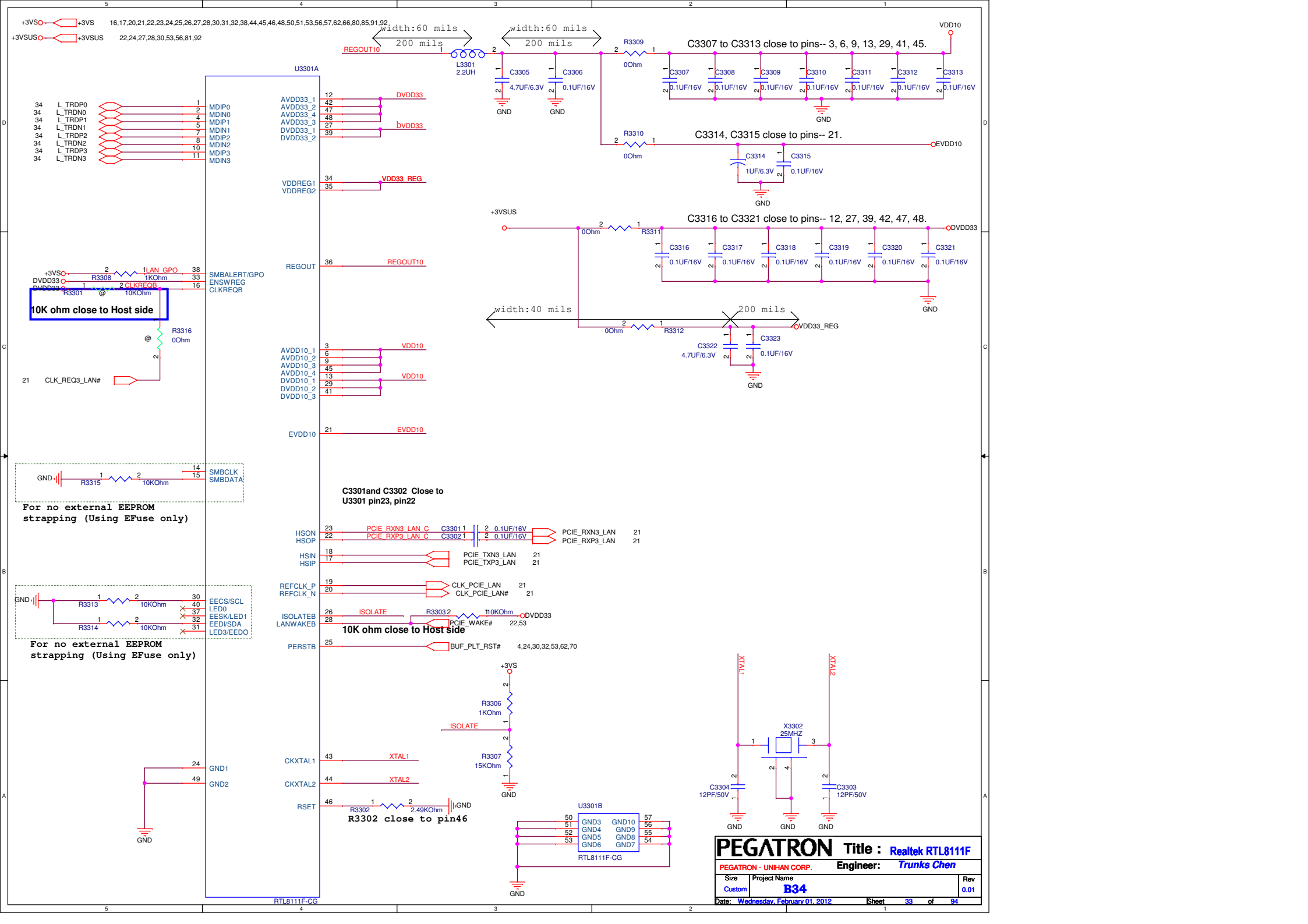
+VCCP	+VCCP	3,4,6,7,26,27,30,82
+3VA_EC	+3VA_EC	28,30
+3VS	+3VS	16,17,20,21,22,23,24,25,26,27,28,30,31,33,38,44,45,46,48,50,51,53,56,57,62,66,80,85,91,92

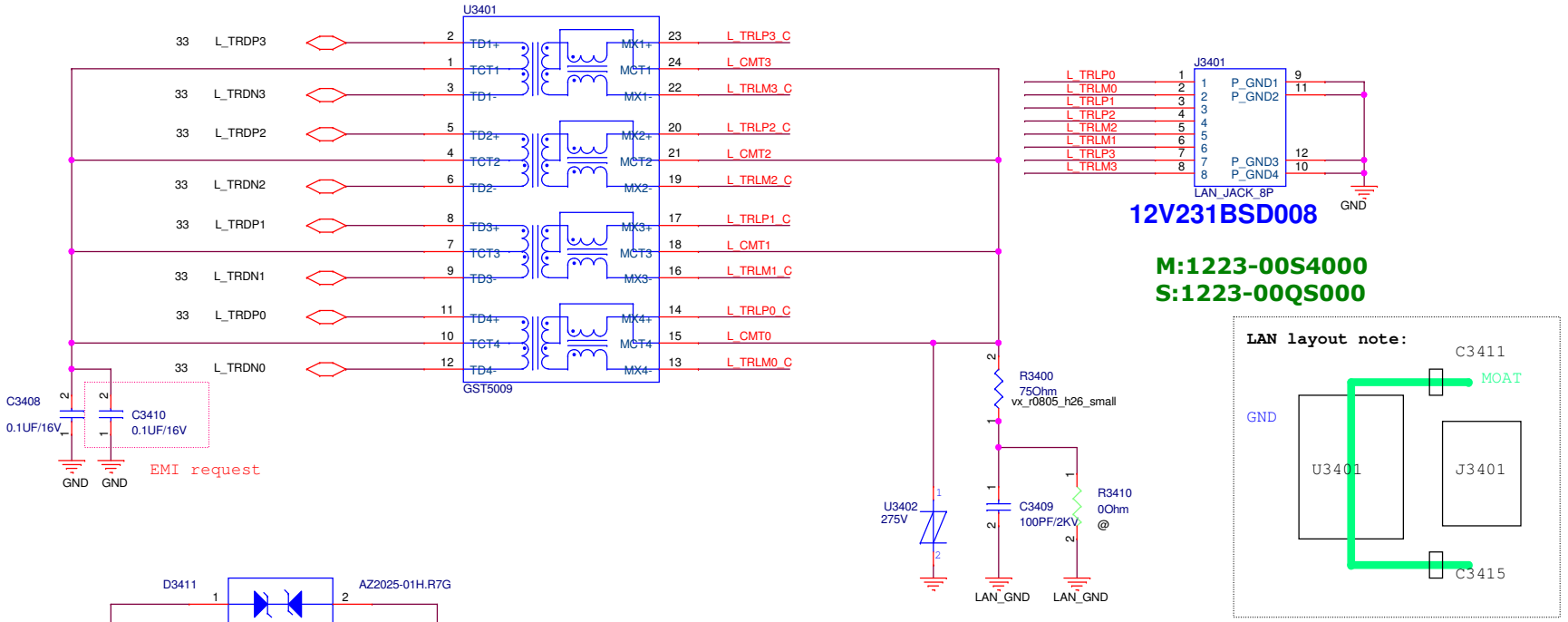
PEGATRON Title : RST_Reset Circuit

BG1-HW RD Div.2-NB RD Dept.5 Engineer: Trunks Chen

Size	Project Name	Rev
C	B34	1.0

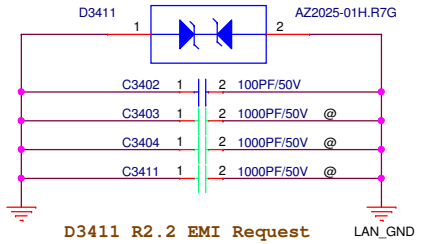
Date: Wednesday, February 01, 2012 Sheet 32 of 59


+3VS
+3VS 16,17,20,21,22,23,24,25,26,27,28,30,31,32,38,44,45,46,48,50,51,53,56,57,62,66,80,85,91,92
+3VSUS
+3VSUS 22,24,27,28,30,53,56,81,92
U3301A
width:60 mils
200 mils
REGOUT10
L3301
2.2UH
C3305
4.7UF/6.3V
C3306
0.1UF/16V
R3309
0Ohm
C3307 to C3313 close to pins-- 3, 6, 9, 13, 29, 41, 45.
C3307
C3308
C3309
C3310
C3311
C3312
C3313
VDD10
GND
R3310
C3314, C3315 close to pins-- 21.
C3314
1UF/6.3V
C3315
EVDD10
+3VSUS
R3311
C3316 to C3321 close to pins-- 12, 27, 39, 42, 47, 48.
C3316
C3317
C3318
C3319
C3320
C3321
DVDD33
width:40 mils
R3312
VDD33_REG
C3322
4.7UF/6.3V
C3323
L_TRDP0
L_TRDN0
L_TRDP1
L_TRDN1
L_TRDP2
L_TRDN2
L_TRDP3
L_TRDN3
MDIP0
MDIN0
MDIP1
MDIN1
MDIP2
MDIN2
MDIP3
MDIN3
AVDD33_1
AVDD33_2
AVDD33_4
AVDD33_3
DVDD33_1
DVDD33_2
VDDREG1
VDDREG2
VDD33_REG
REGOUT
REGOUT10
AVDD10_1
AVDD10_2
AVDD10_3
AVDD10_4
DVDD10_1
DVDD10_2
DVDD10_3
VDD10
EVDD10
LAN_GPO
R3308
1KOhm
CLKREQB
R3301
10KOhm
SMBALERT/GPO
ENSWREG
CLKREQB
10K ohm close to Host side
R3316
0Ohm
CLK_REQ3_LAN#
R3315
SMBCLK
SMBDATA
For no external EEPROM strapping (Using EFuse only)
C3301and C3302 Close to U3301 pin23, pin22
HSON
HSOP
PCIE_RXN3_LAN_C
PCIE_RXP3_LAN_C
C3301
C3302
0.1UF/16V
PCIE_RXN3_LAN
PCIE_RXP3_LAN
HSIN
HSIP
PCIE_TXN3_LAN
PCIE_TXP3_LAN
REFCLK_P
REFCLK_N
CLK_PCIE_LAN
CLK_PCIE_LAN#
ISOLATEB
LANWAKEB
ISOLATE
R3303
10KOhm
PCIE_WAKE#
22,53
10K ohm close to Host side
PERSTB
BUF_PLT_RST#
4,24,30,32,53,62,70
R3313
R3314
EECS/SCL
LED0
EESK/LED1
EEDI/SDA
LED3/EEDO
For no external EEPROM strapping (Using EFuse only)
R3306
1KOhm
R3307
15KOhm
CKXTAL1
CKXTAL2
XTAL1
XTAL2
RSET
R3302
2.49KOhm
R3302 close to pin46
GND1
GND2
U3301B
GND3
GND4
GND5
GND6
GND10
GND9
GND8
GND7
RTL8111F-CG
X3302
25MHZ
C3304
12PF/50V
C3303
12PF/50V
RTL8111F-CG
PEGATRON
Title : Realtek RTL8111F
PEGATRON · UNIHAN CORP.
Engineer: Trunks Chen
Size Custom
Project Name B34
Rev 0.01
Date: Wednesday, February 01, 2012
Sheet 33 of 94

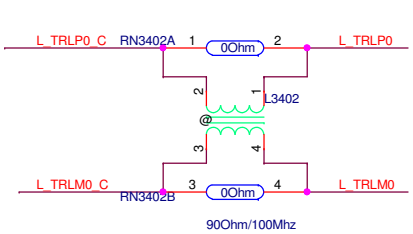


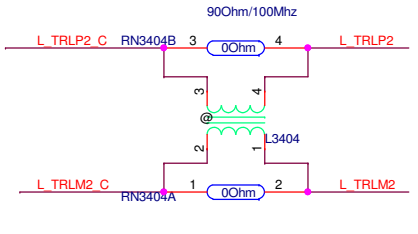
12V231BSD008

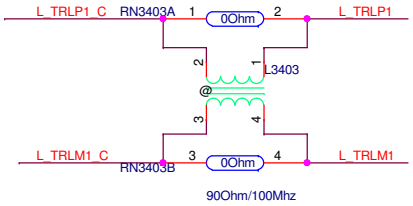
M:1223-00S4000
S:1223-00QS000

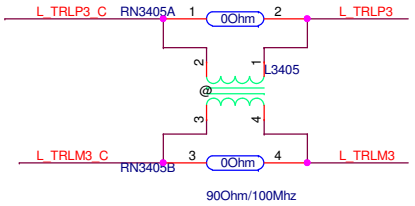


D3411 R2.2 EMI Request



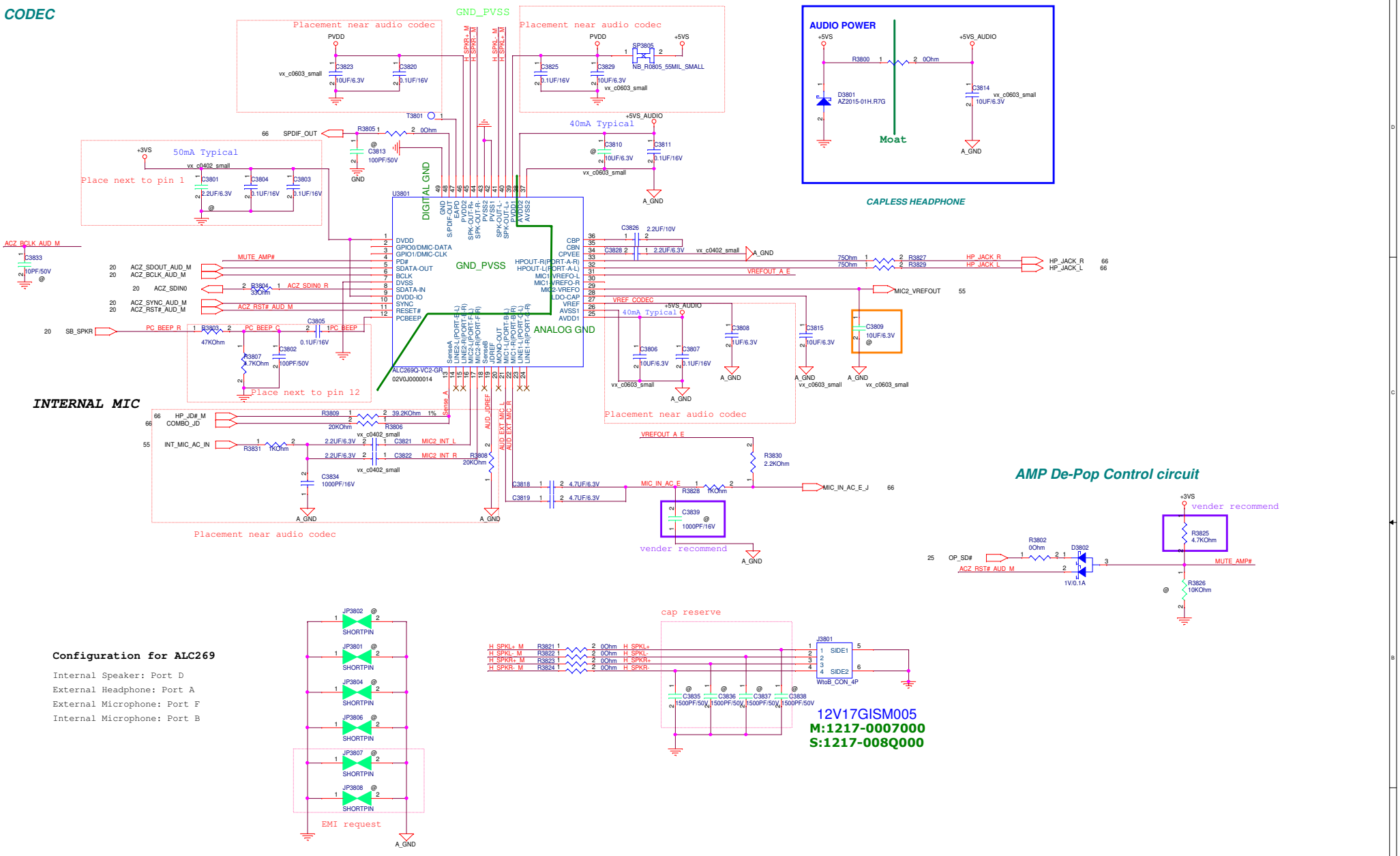






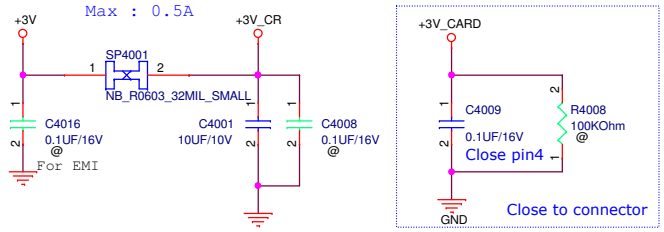
PEGATRON	Title : LAN I/O RJ-45	
PEGATRON · UNIHAN CORP.	Engineer: *Trunks Chen*	
Size: Custom	Project Name: B34	Rev: 0.01
Date: Wednesday, February 01, 2012	Sheet 34 of 94	

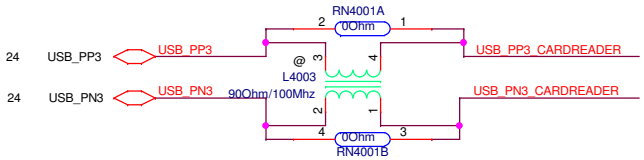
CODEC

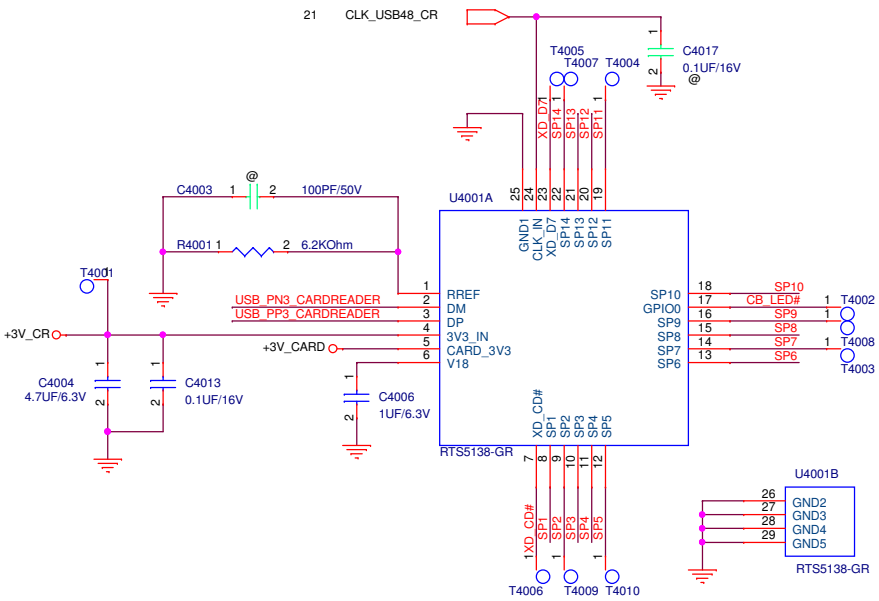


PEGATRON	Title : ALC269Q-VC2		
	Engineer: Trunks Chen		
ASUSTeK COMPUTER INC. NB1			
Size: C	Project Name: B34		Rev: 1.0
Date: Wednesday, February 01, 2012	Sheet 38 of 59		

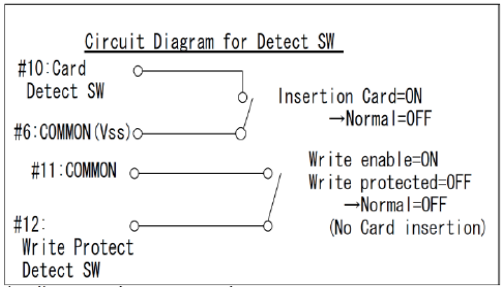
Cardreader





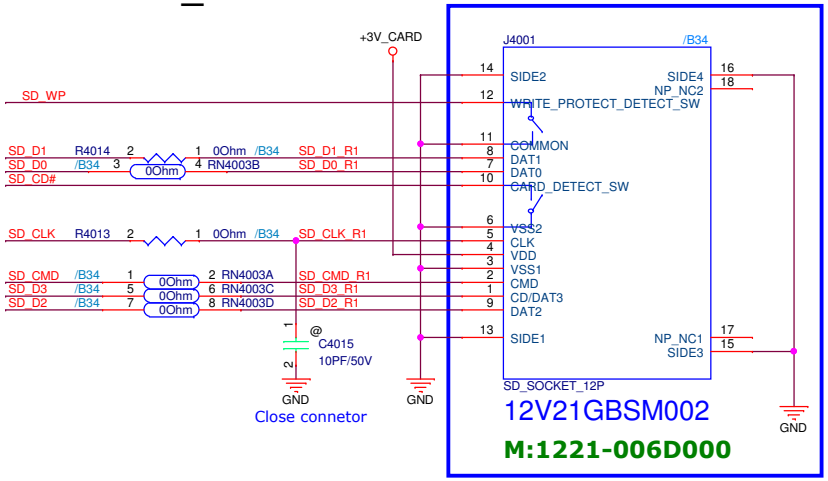


Pin No.	Name	Discription
# 1	CD/DAT3	Card Detect / Data Line
# 2	CMD	Command / Response
# 3	V_{SS1}	Supply voltage ground
# 4	V_{DD}	Supply voltage
# 5	CLK	Clock
# 6	V_{SS2}	Supply voltage ground
# 7	DAT0	Data Line
# 8	DAT1	Data Line
# 9	DAT2	Data Line

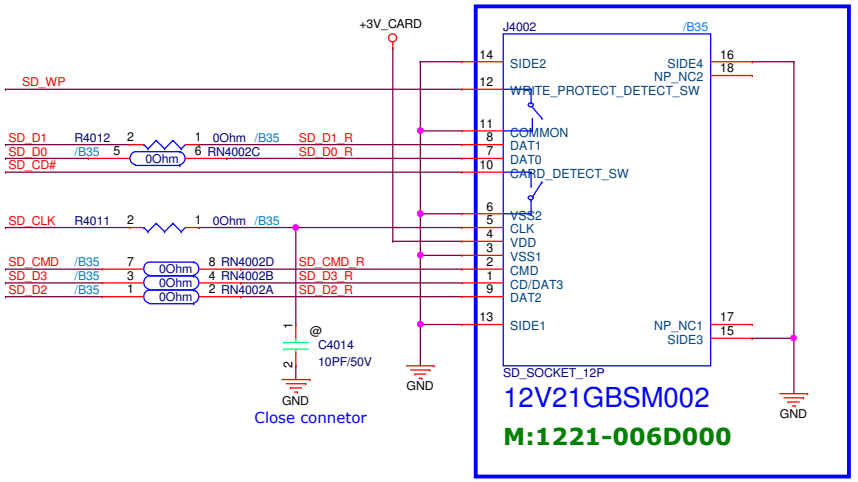


SP1 SD_WP MS_CLK
SP3 SD_D1
SP4 SD_D0
SP6 SD_CD#
SP8 SD_CLK MS_D2
SP10 SD_CMD
SP12 SD_D3 MS_D1
SP13 SD_D2

14" SD_SOCKET

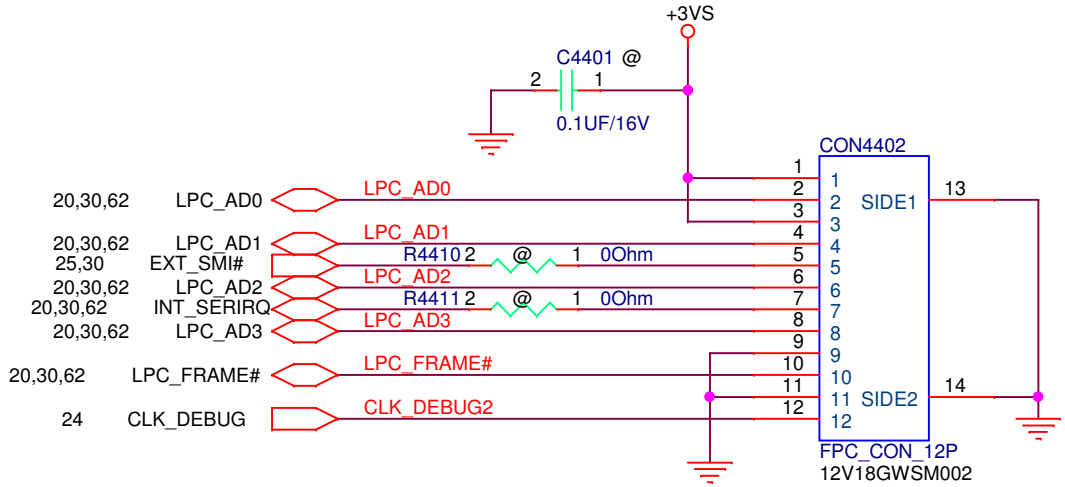


15" SD_SOCKET



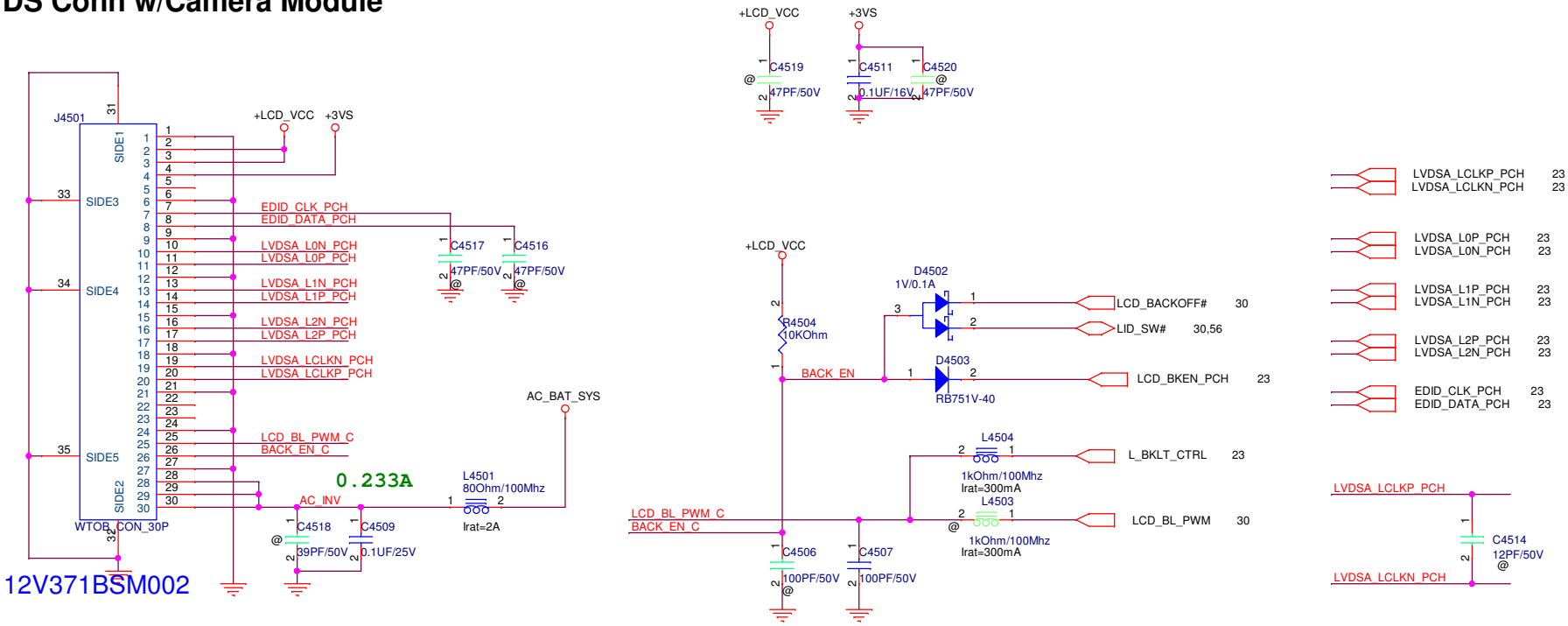
PEGATRON Title : ALCOR AU6433
BG1\HW1 Engineer: Trunks Chen
Size: Custom | Project Name: B34 | Rev: 1.0
Date: Wednesday, February 01, 2012 | Sheet 40 of 94

DEBUG CARD CONN.

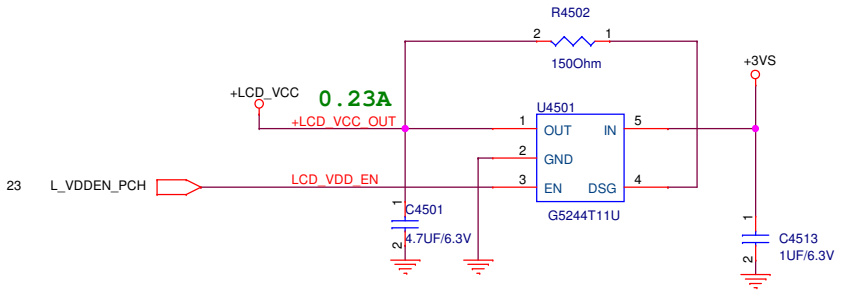


PEGATRON	Title : BUG_Debug	
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Trunks Chen	
Size: A	Project Name: B34	Rev: 1.0
Date: Wednesday, February 01, 2012	Sheet 44 of 59	

LVDS Conn w/Camera Module



LCD VDDEN / +LED_VCC



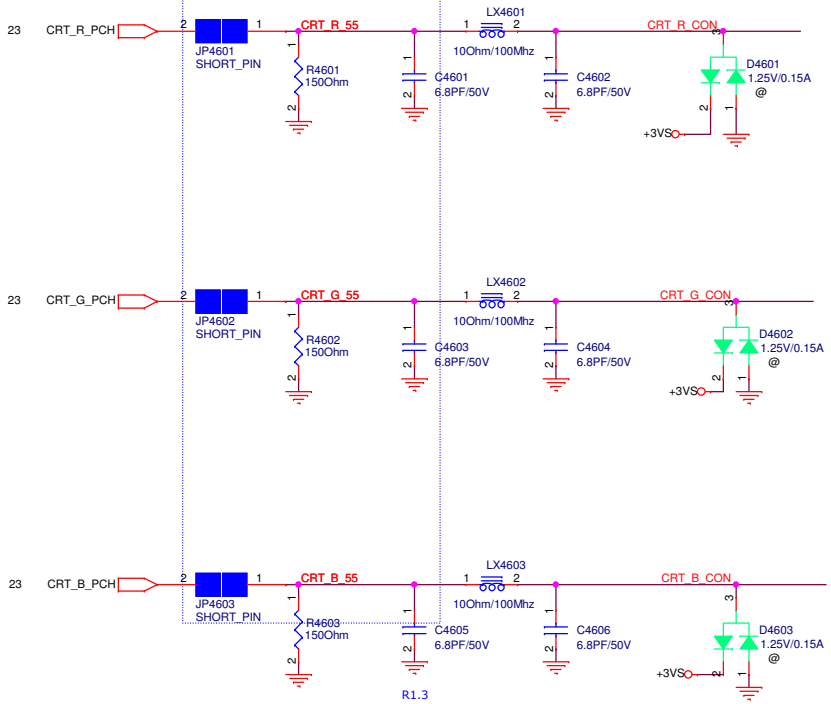
PEGATRON	Title : LVDS CONN	
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Trunks Chen	
Size: B	Project Name: B34	Rev: 1.0
Date: Wednesday, February 01, 2012	Sheet 45 of 59	

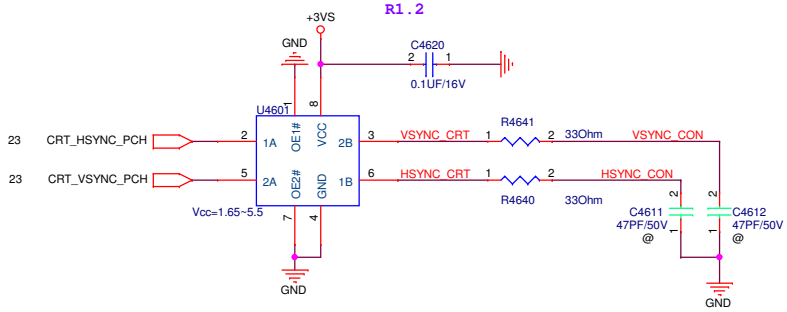
+3VS +3VS 16,17,20,21,22,23,24,25,26,27,28,30,31,32,33,38,44,45,48,50,51,53,56,57,62,66,80,85,91,92

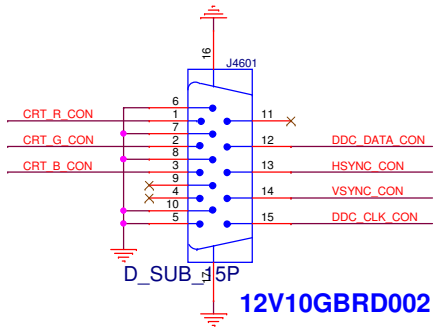
+5V +5V 52,55,56,57,66,91

+5VS +5VS 27,30,31,38,48,50,51,53,56,57,80,91

Change to NV optimus solution

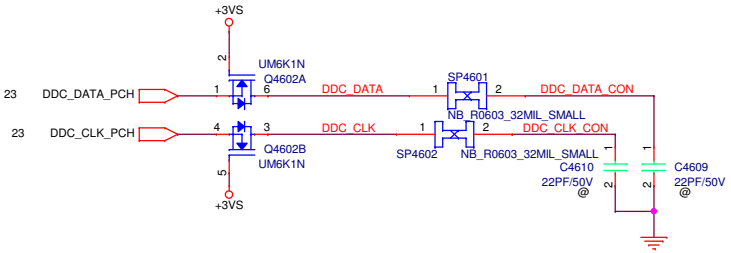


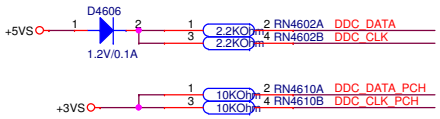


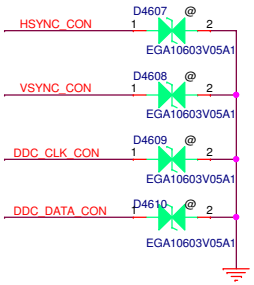


12V10GBRD002

M:1210-003A000
S:1210-00EH000
S:1210-00BS000







PEGATRON	Title : CRT(2)_D-Sub	
BG1\HW1	Engineer: Trunks Chen	
Size: Custom	Project Name: B34	Rev: 2.1
Date: Wednesday, February 01, 2012	Sheet 46 of 98	

+12VS → +12VS 20,28,91

+3VS → +3VS 16,17,20,21,22,23,24,25,26,27,28,30,31,32,33,38,44,45,46,50,51,53,56,57,62,66,80,85,91,92

+5VS → +5VS 27,30,31,38,46,50,51,53,56,57,80,91

23 HDMI_CLKP_PCH_R — C4832 0.1UF/10V — HDMI_CLKP
23 HDMI_CLKN_PCH_R — C4834 0.1UF/10V — HDMI_CLKN
23 HDMI_TXP0_PCH — C4833 0.1UF/10V — HDMI_TXP0
23 HDMI_TXN0_PCH — C4835 0.1UF/10V — HDMI_TXN0
23 HDMI_TXP1_PCH — C4828 0.1UF/10V — HDMI_TXP1
23 HDMI_TXN1_PCH — C4829 0.1UF/10V — HDMI_TXN1
23 HDMI_TXP2_PCH — C4830 0.1UF/10V — HDMI_TXP2
23 HDMI_TXN2_PCH — C4831 0.1UF/10V — HDMI_TXN2

R4826 R4829 R4825 R4828 R4824 R4827 R4823 R4822 R4827 680OHM

change to 680 ohm

HDMI_CLKP_M HDMI_CLKN_M HDMI_TXP0_M HDMI_TXN0_M HDMI_TXP1_M HDMI_TXN1_M HDMI_TXP2_M HDMI_TXN2_M

+3VS → Q4802 2N7002 → GND

HDMI_TXP2 — 0Ohm — RN4801A — HDMI_TXP2_CON
HDMI_TXN2 — 0Ohm — RN4801B — HDMI_TXN2_CON
L4801 90Ohm/100MHz
R4810 220Ohm @

HDMI_TXP1 — 0Ohm — RN4802B — HDMI_TXP1_CON
HDMI_TXN1 — 0Ohm — RN4802A — HDMI_TXN1_CON
L4802 90Ohm/100MHz
R4811 220Ohm @

HDMI_TXP0 — 0Ohm — RN4803A — HDMI_TXP0_CON
HDMI_TXN0 — 0Ohm — RN4803B — HDMI_TXN0_CON
L4803 90Ohm/100MHz
R4812 220Ohm @

HDMI_CLKP — 0Ohm — RN4804B — HDMI_CLKP_CON
HDMI_CLKN — 0Ohm — RN4804A — HDMI_CLKN_CON
L4804 90Ohm/100MHz
R4813 220Ohm @

R1.2 for EMI solution
R4810~R4813

+12VS
+5VS → Q4806 NDS351AN_NL → F4801 0.35A/6V → +5VS_HDMI

D4803 1V/0.1A

+3VS
R4833 2.2KOhm
R4832 2.2KOhm
R4830 2.2KOhm
R4831 2.2KOhm

+3VS → Q4801A UM6K1N
Q4801B UM6K1N → +3VS

23 HDMI_DDC_CLK_PCH — R4807 0Ohm — HDMI_SCL_VGA
23 HDMI_DDC_DATA_PCH — R4808 0Ohm — HDMI_SDA_VGA

EMI request

HDMI_SCL & HDMI_SDA : no via , trace length should be as short as possible

C4827 10PF/50V @
C4826 10PF/50V @

23 HDMI_HPD_PCH — R4805 0Ohm
30 HDMI_HPD_EC — R4806 @ 0Ohm

HDMI HPD EC reserve

+3VS → Q4809 PMBS3904
R4809 10KOhm
HDMI_HPD
R4854 100KOhm
R4855 100KOhm
D4802 1.25V/0.15A → +5VS

R1.2 HDMI HPD Design AMD recommendation_1227

J4801 HDMI_CON_19P

HDMI_TXP2_CON
HDMI_TXN2_CON
HDMI_TXP1_CON
HDMI_TXN1_CON
HDMI_TXP0_CON
HDMI_TXN0_CON
HDMI_CLKP_CON
HDMI_CLKN_CON
HDMI_SCL
HDMI_SDA
+5VS_HDMI
HDMI_HPD_CON

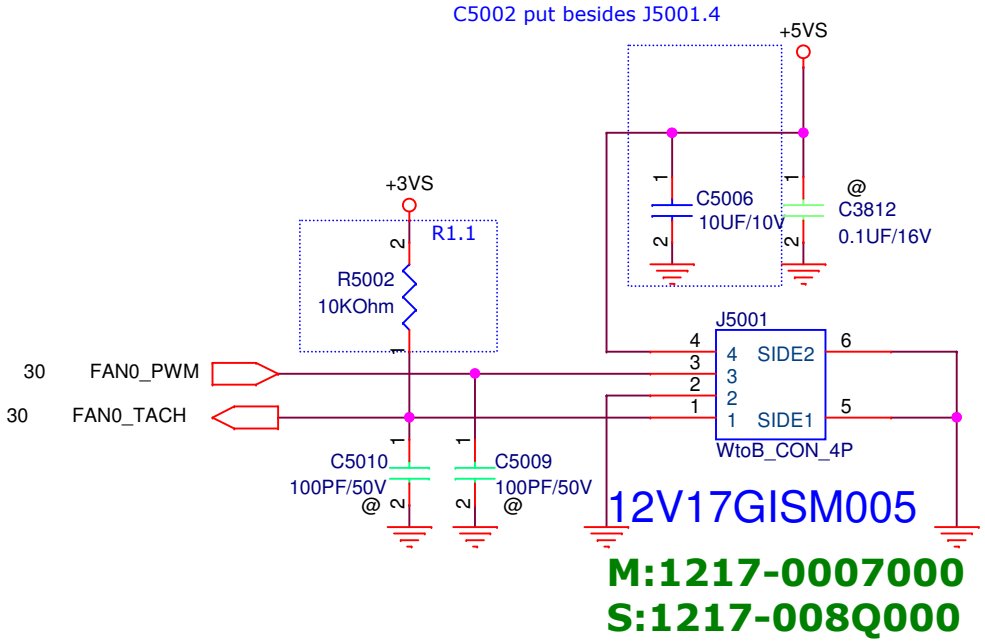
P_GND1 P_GND3 P_GND4 P_GND2

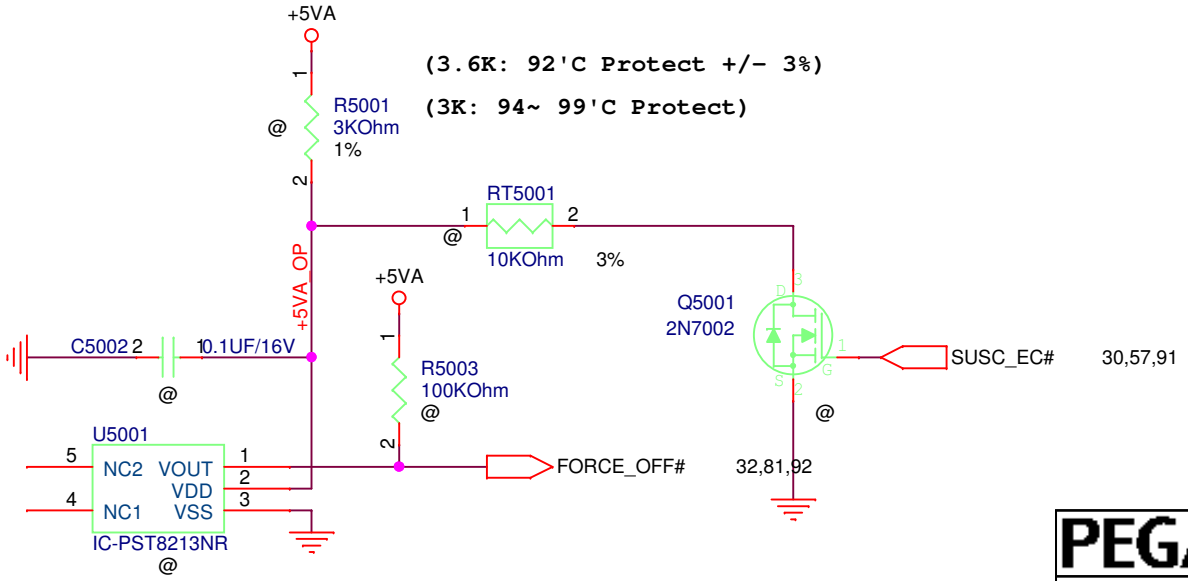
12V12GBRD000

M:1212-0081000

PEGATRON	Title : HDMI	
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Trunks Chen	
Size: C	Project Name: B34	Rev: 1.0
Date: Wednesday, February 01, 2012	Sheet 48 of 59	

PWM Fan

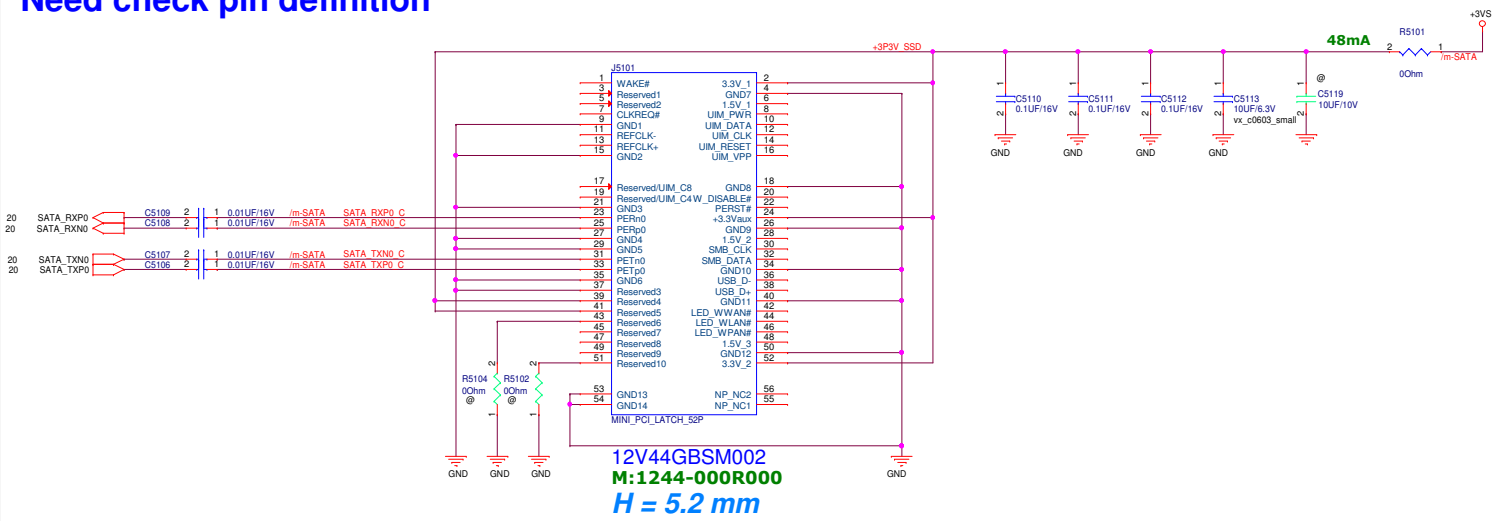




PEGATRON	Title : THERMAL/ FAN	
BG1-HW RD Div.2-NB RD Dept.5	Engineer: *Trunks Chen*	
Size: A	Project Name: B34	Rev: 1.0
Date: Wednesday, February 01, 2012	Sheet 50 of 59	

mSATA SSD mini card connector

Need check pin definition

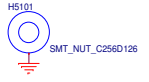


12V44GBSM002

M:1244-000R000

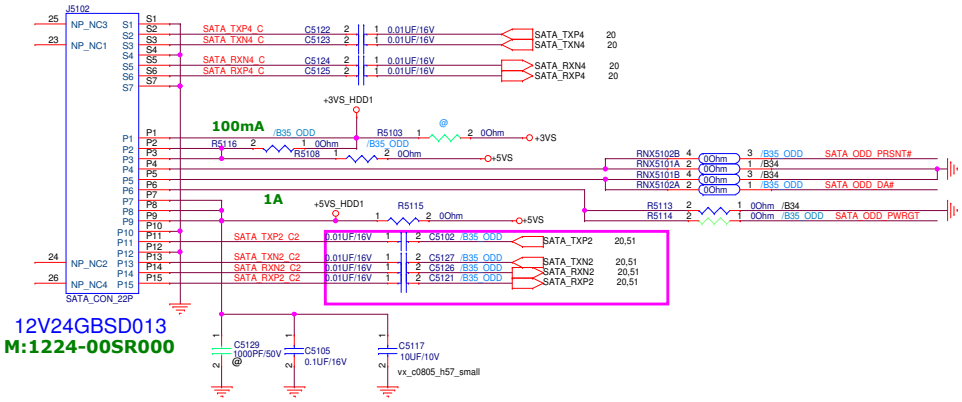
H = 5.2 mm

m-SATA NUT



NUT H=2.8mm
Drill 3.2mm
Top Ring 6.5mm
Bot Ring 6.5mm

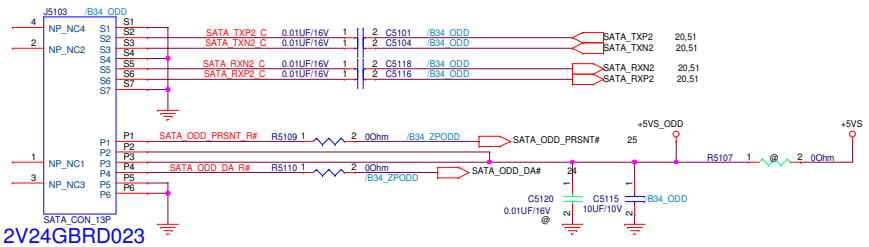
7mm SATA SSD connector



12V24GBSD013

M:1224-00SR000

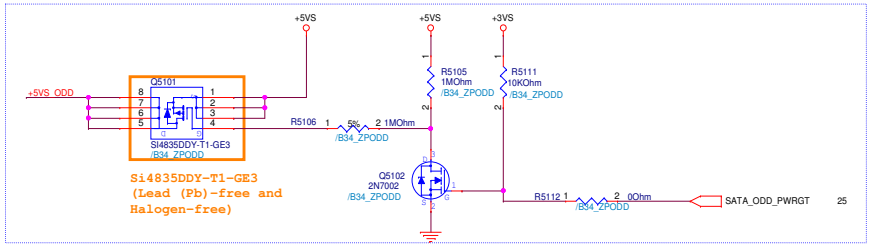
ODD



12V24GBRD023

M:1224-00U1000

Zero Power ODD Support



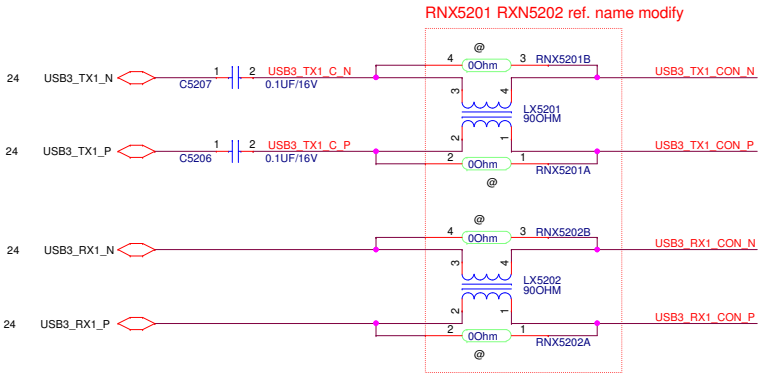
PEGATRON Title : mSATA SSD

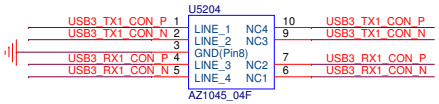
BG1-HW RD Div.2-NB RD Dept.5 Engineer: Trunks Chen

Size	Project Name	Rev
C	B34	1.0

Date: Wednesday, February 01, 2012 Sheet 51 of 59

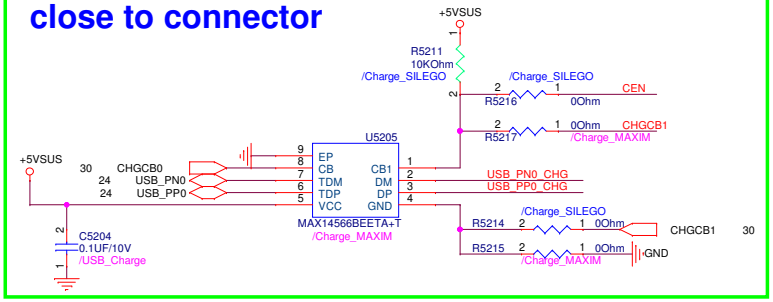
USB 3.0 & USB 2.0 Combo

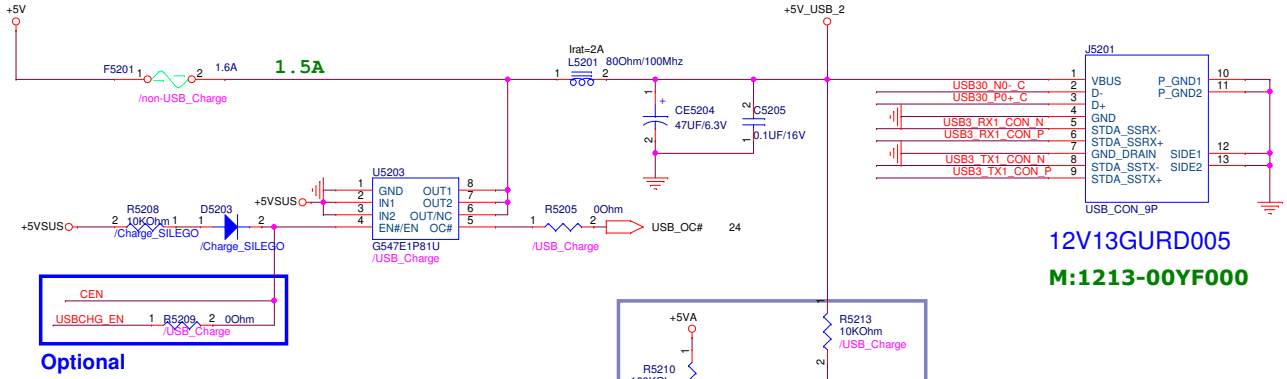




PLACE ESD Diodes near Connector

MAXIM USB Charger IC MAX14566BE
close to connector

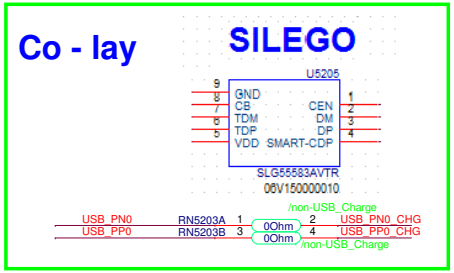


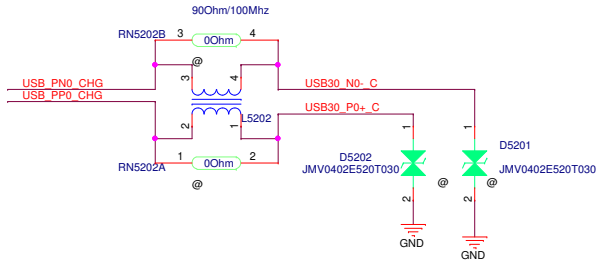


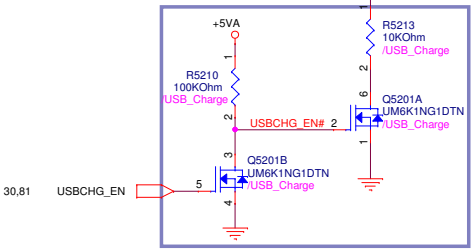
12V13GURD005

M:1213-00YF000

Co - lay







PEGATRON	Title :	USB2.0 / 3.0 COMBO Con.	
BG1-HW RD Div.2-NB RD Dept.5	Engineer:	Trunks Chen	
Size: Custom	Project Name: B34		Rev: 1.0
Date: Wednesday, February 01, 2012	Sheet 52 of 59		

WLAN+BT/WiMax

+3VS +3VS 16,17,20,21,22,23,24,25,26,27,28,30,31,32,33,38,44,45,46,48,50,51,56,57,62,66,80,85,91,92
+3VSUS +3VSUS 22,24,27,28,30,33,56,81,92
+1.5VS +1.5VS 26,57,91
+3V +3V 24,40,55,57,62,91

GPIO6
30 WLAN_WAKE# R5321 1 /AOAC 2 0Ohm
22,33 PCIE_WAKE# R5320 1 @ 2 0Ohm
BT Disable Low for CHICONY
BT_ON/OFF_C# R5315 1 2 0Ohm
21 CLK_REQ2_WLAN#
21 CLK_PCIE_WLAN#_PCH
21 CLK_PCIE_WLAN_PCH
21 PCIE_RXN2_WLAN
21 PCIE_RXP2_WLAN
21 PCIE_TXN2_WLAN
21 PCIE_TXP2_WLAN
+3VS_WLAN
21 CL_CLK
21 CL_DATA
21 CL_RST#
BT_ON/OFF_C#
BT Disable Low for Intel
MINI_PCI_52P
J5302
SIDE1 NP_NC1 SIDE2 NP_NC2
+1.5VS +3VS_WLAN
WLAN_ON_C
BUF_PLT_RST#_C
SMBC SMBD
RN5302A RN5302B RN5301A
SMB_CLK_S SMB_DAT_S 16,17,28,31
USB_PN11_C USB_PP11_C
L5301 90Ohm/100Mhz
USB_PN11 24
USB_PP11 24
RN5301B
R5334 100KOhm R5333 100KOhm
Q5308B UM6K1N
Q5308A UM6K1N
25 BT_ON/OFF#
R5335 100KOhm

12V44GISM001
M:1244-004W000
H = 6.5 mm

WLAN_PWR WLAN_PWR
R5329 100KOhm R5328 100KOhm
WLAN_ON_C
Q5303B UM6K1N
Q5303A UM6K1N
WLAN_RF
R5323 0Ohm /non-AOAC
WLAN_ON 25
/AOAC R5322 0Ohm
RF_ON 30

+3VS_WLAN WLAN_PWR
R5307 2 1 0Ohm
Q5307
SI4835DDY-T1-GE3
C5313 4700PF/50V
R5306 1MOhm 5%
R5330 /non-AOAC +3VS
R5325 +3V for AOAC
R5324 /AOAC +3VA_WLAN for AOAC & FFS DC mode
R5326 +3VSUS for AOAC & FFS
R1.1_0930
Q5306 2N7002
R5302 AOAC_ON 25
R5301 WLAN_RF
R5303 AOAC_PWREN 30,81
GPIO24

WLAN +1.5VS bypass capactor:
Place 0.1UF near pin 6,28,48.
Place 10UF near +1.5VS source side.
+1.5VS
C5329 10UF/6.3V C5330 0.1UF/10V C5304 0.1UF/10V @ C5328 0.1UF/10V @
vx_c0603_small

WLAN +3VS bypass capactor:
Place 0.1UF near pin 2,24,52,39 41.
Place 10UF near +3VS_WLAN source side.
+3VS_WLAN
C5312 10UF/6.3V C5308 0.1UF/10V C5309 0.1UF/10V C5310 0.1UF/10V @ C5311 0.1UF/10V @
vx_c0603_small

WLAN NUT
H5301
C220D130
NUT H=4mm
Drill 3.3mm
Top Ring 5.5mm
Bot Ring 5.5mm

+3VA_WLAN
+5VS
R5332 100KOhm /AOAC
R5331 100KOhm @
BUF_PLT_RST#_C
Q5305A UM6K1N @
Q5305B UM6K1N @
4,24,30,32,33,62,70 BUF_PLT_RST#
R5304 /non-AOAC
30 WLAN_RST#
GPIO14
D5304 1.2V/0.1A /AOAC
R2.0_1202

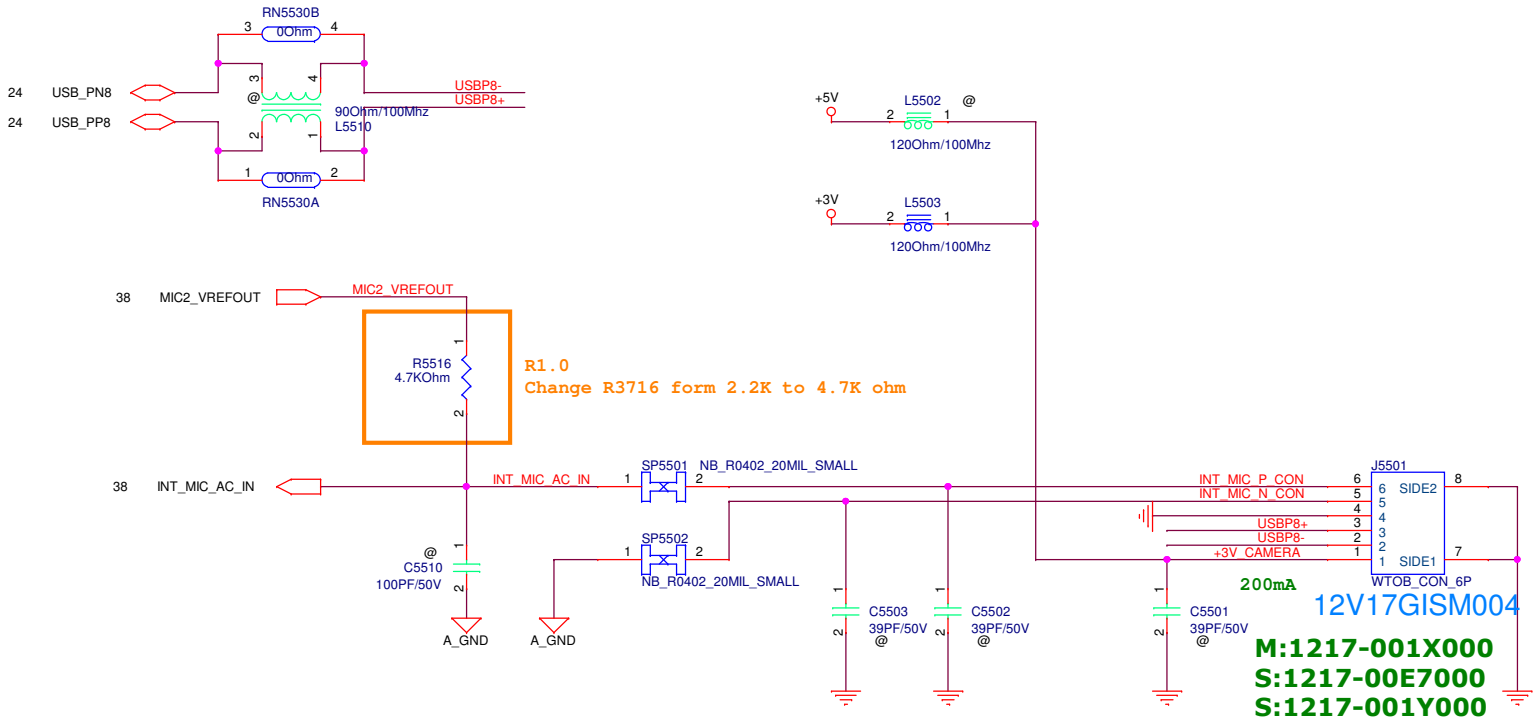
PEGATRON Title : WiFi / BT/ Wimax
BG1-HW RD Div.2-NB RD Dept.5 Engineer:
Size Custom | Project Name B34 | Rev 1.0
Date: Wednesday, February 01, 2012 Sheet 53 of 59

Camera

+3VS → +3VS 16,17,20,21,22,23,24,25,26,27,28,30,31,32,33,38,44,45,46,48,50,51,53,56,57,62,66,80,85,91,92

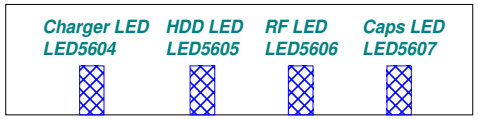
+3V → +3V 24,40,53,57,62,91

+5V → +5V 52,56,57,66,91



PEGATRON	Title : CAMERA	
BG1\HW1	Engineer: Trunks Chen	
Size: B	Project Name: B34	Rev: 2.0
Date: Wednesday, February 01, 2012	Sheet 55 of 94	

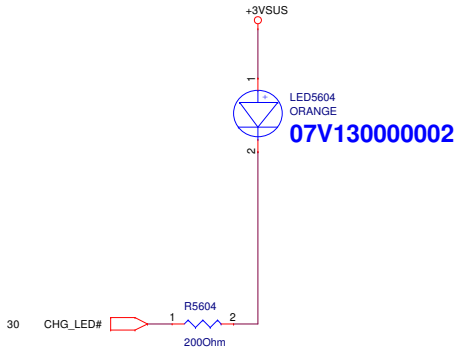
LED Side light



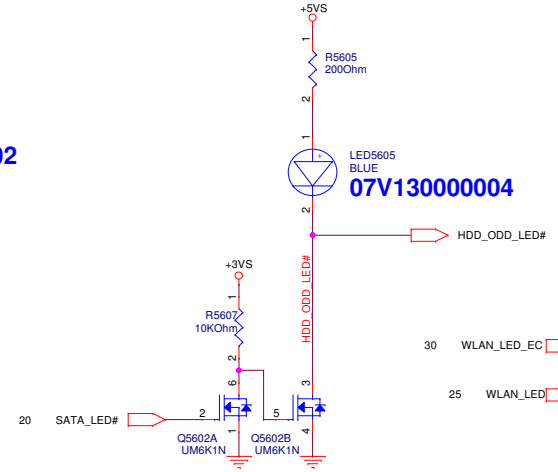
LED Placement
Left-->Right

Order of Indicator LEDs
Battery HDD/ODD WiFi Caps

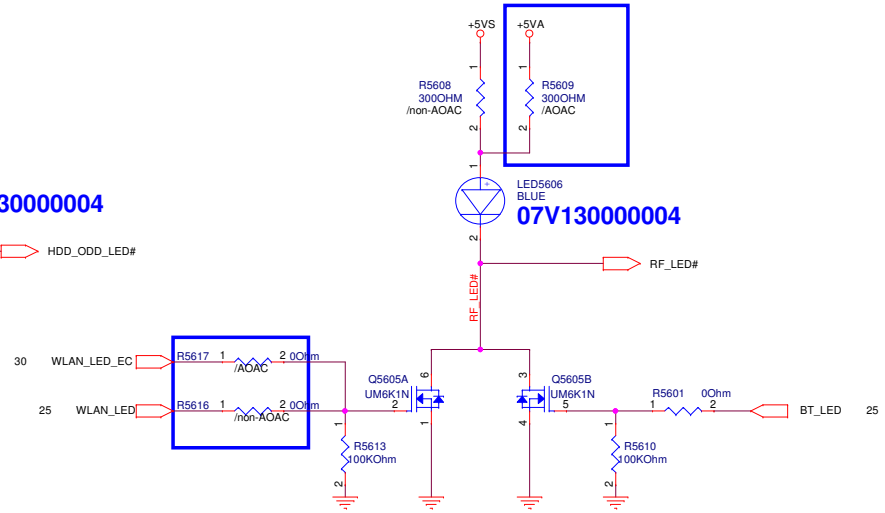
Battery



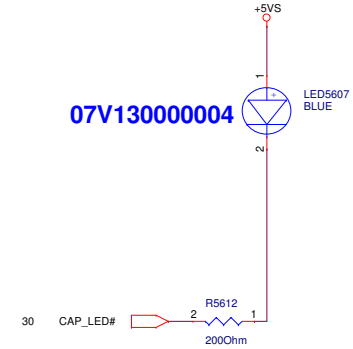
HDD/ODD



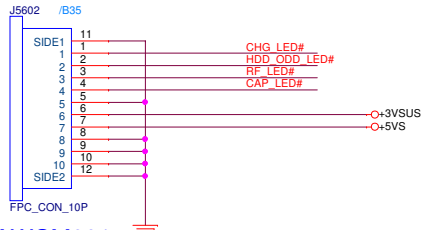
Connectivity (WLAN/BT/3G)



Caps Lock



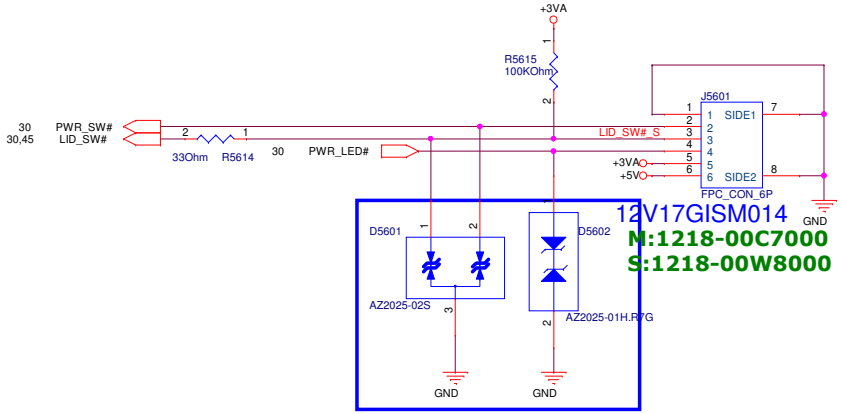
LED Board



12V18AWSM001

M:1218-006F000
S:1218-00A9000

Power Switch Board Conn

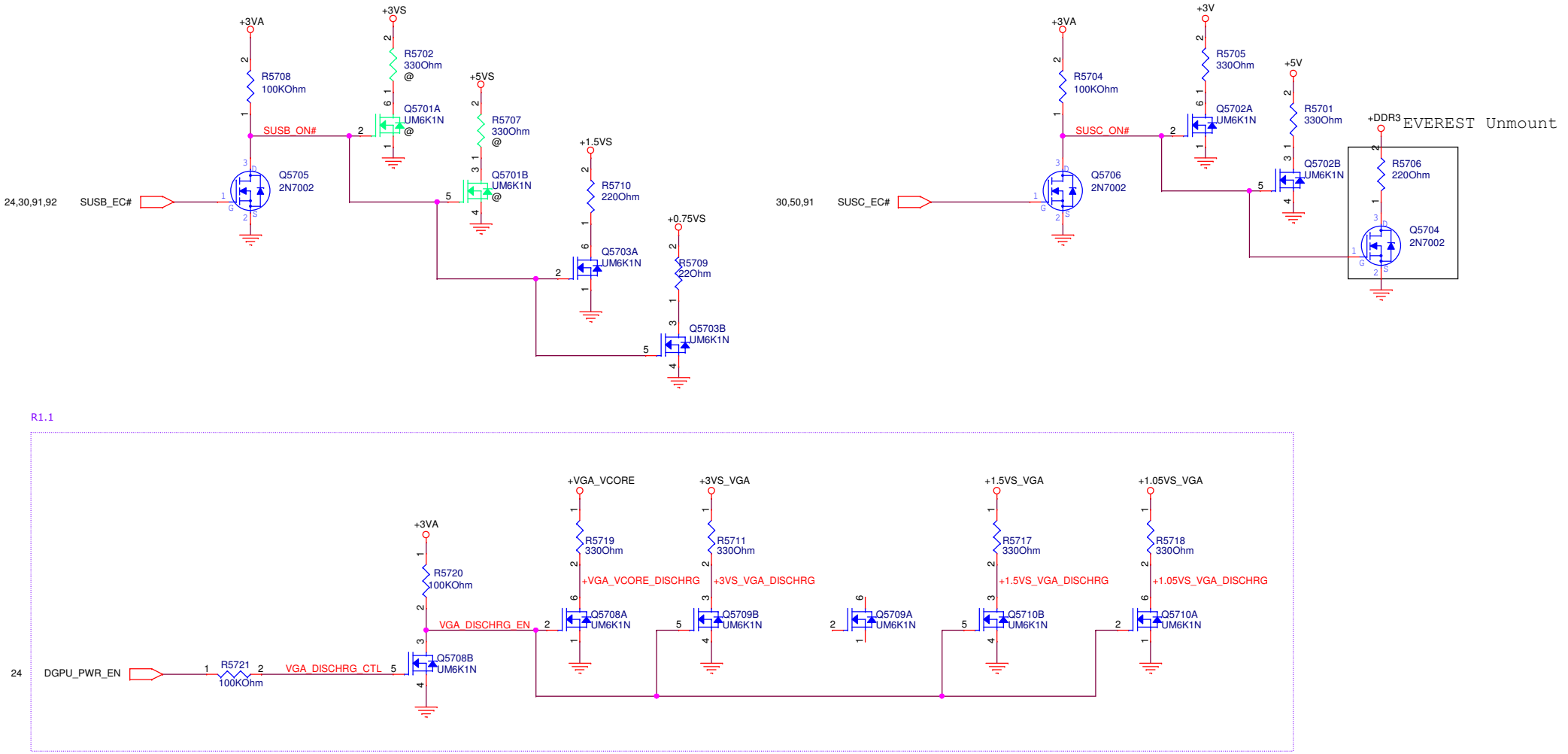


12V17GISM014

M:1218-00C7000
S:1218-00W8000

PEGATRON	Title : LED/ LID/ TP BTN	
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Trunks Chen	
Size: Custom	Project Name: B34	Rev: 1.0
Date: Wednesday, February 01, 2012	Sheet 56 of 99	

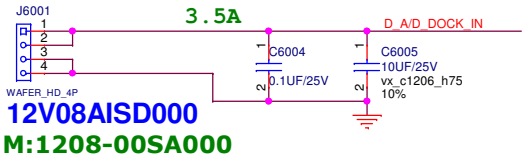
Discharge Circuit

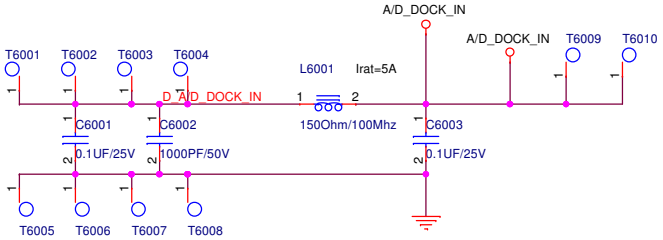


R1.1

PEGATRON	Title : DC-IN / Battery / Discharge	
BG1-HW RD Div.2-NB RD Dept.5	Engineer: *Trunks Chen*	
Size: B	Project Name: B34	Rev: 1.0
Date: Wednesday, February 01, 2012	Sheet 57 of 99	

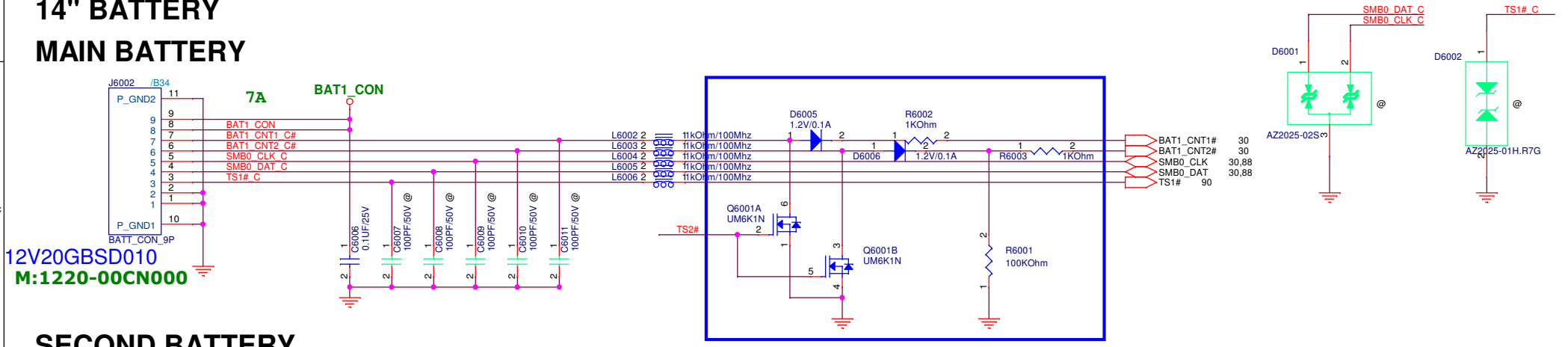
DC IN



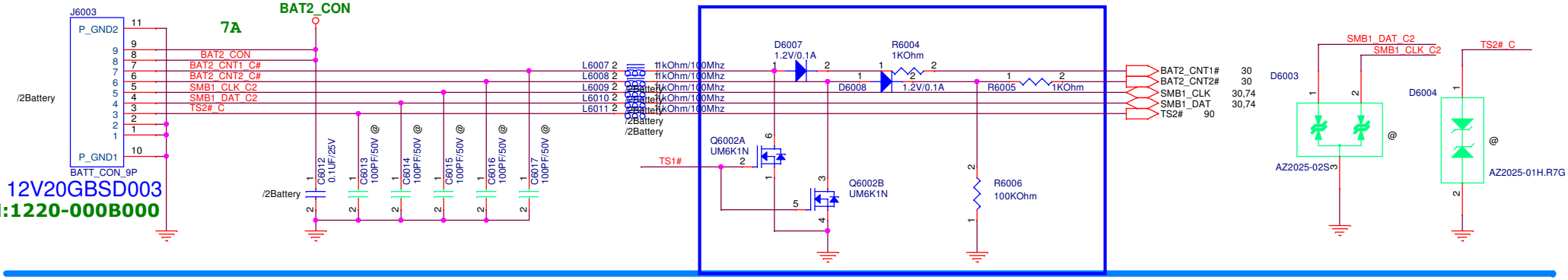


14" BATTERY

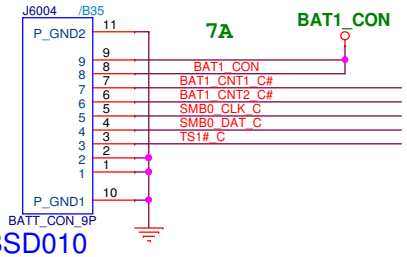
MAIN BATTERY

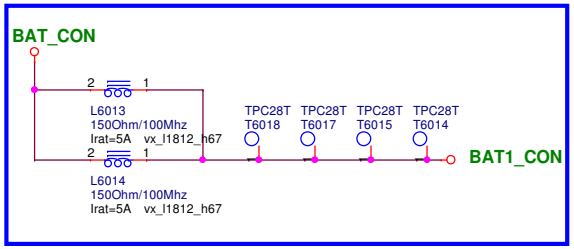


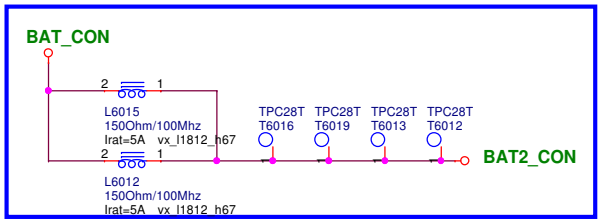
SECOND BATTERY



15" BATTERY

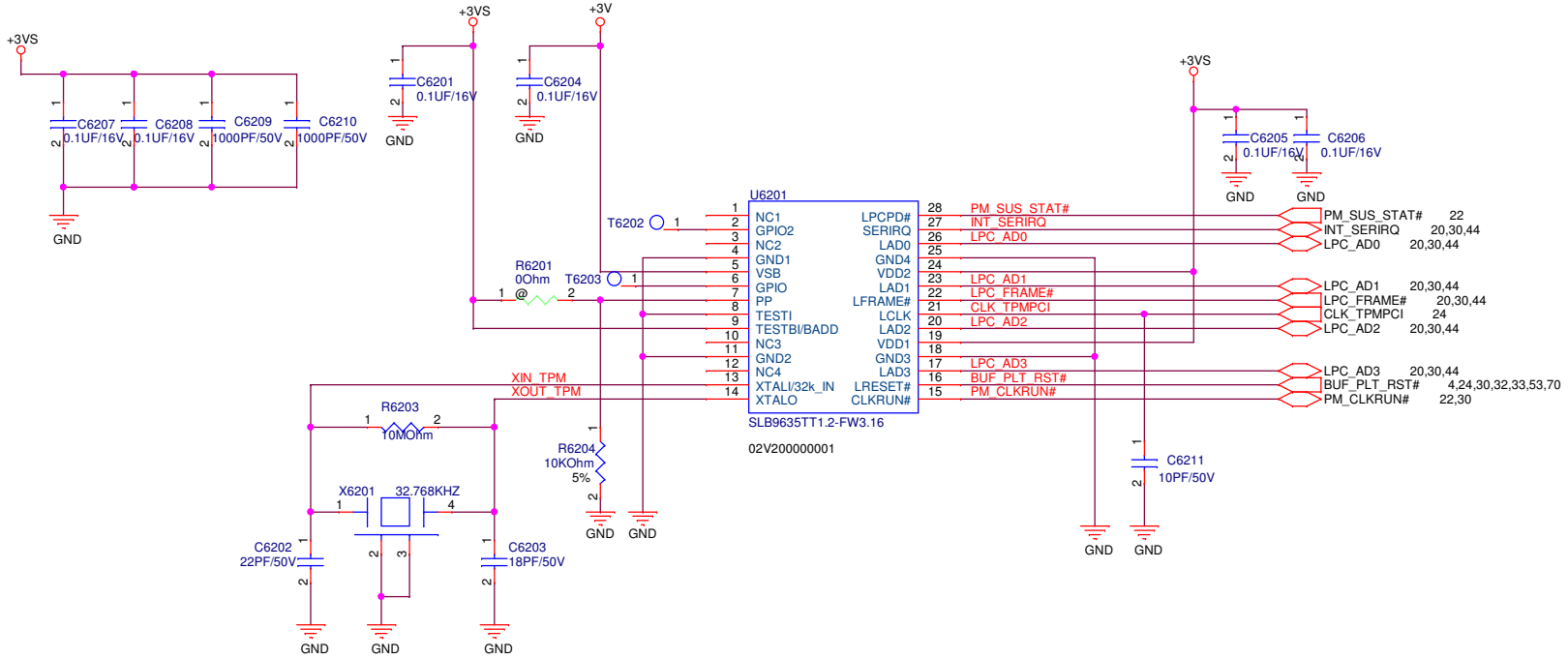




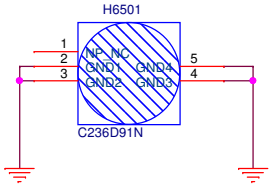


PEGATRON	Title : DC-IN / Battery	
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Trunks Chen	
Size: Custom	Project Name: B34	Rev: 1.0
Date: Wednesday, February 01, 2012	Sheet 60 of 99	

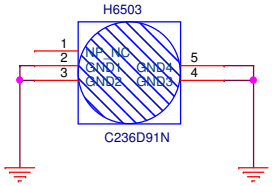
Infineon TPM Chip

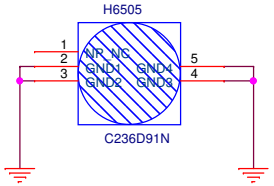


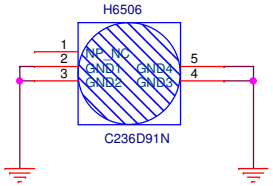
PEGATRON	Title : TPM_****	
BG1\HW1	Engineer: Trunks Chen	
Size: B	Project Name: B34	Rev: 2.1
Date: Wednesday, February 01, 2012	Sheet 62 of 98	

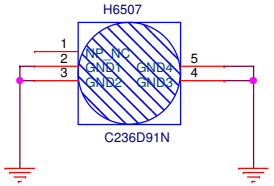


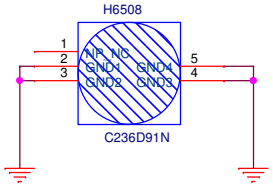
Screw Hole NPTH
Drill 2.3mm
Top Ring 7mm
Bot Ring 7mm

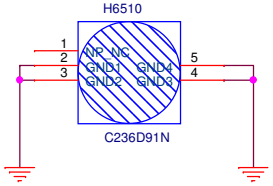


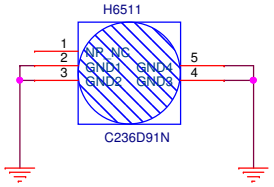






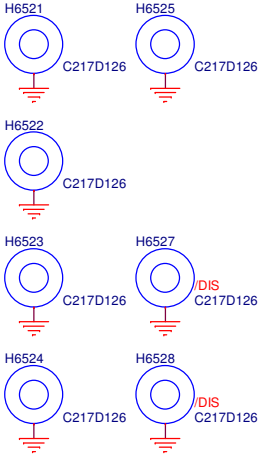






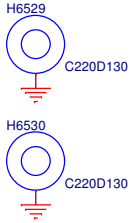
Screw Hole NPTH
Drill 2.3mm
Top Ring 6mm
Bot Ring 6mm

CPU & GPU & FAN

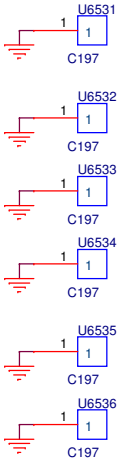


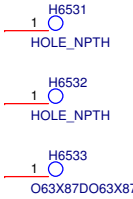
NUT
Drill 3.2mm(126)
Top Ring 5.5mm(217)
Bot Ring 5.5mm(217)

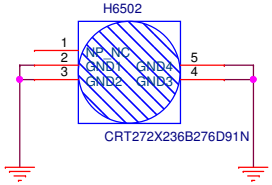
PCH

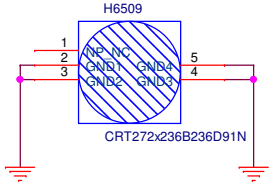


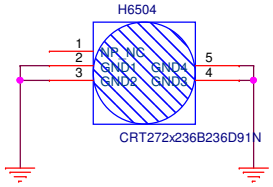
NUT H=4mm
Drill 3.3mm
Top Ring 5.5mm
Bot Ring 5.5mm







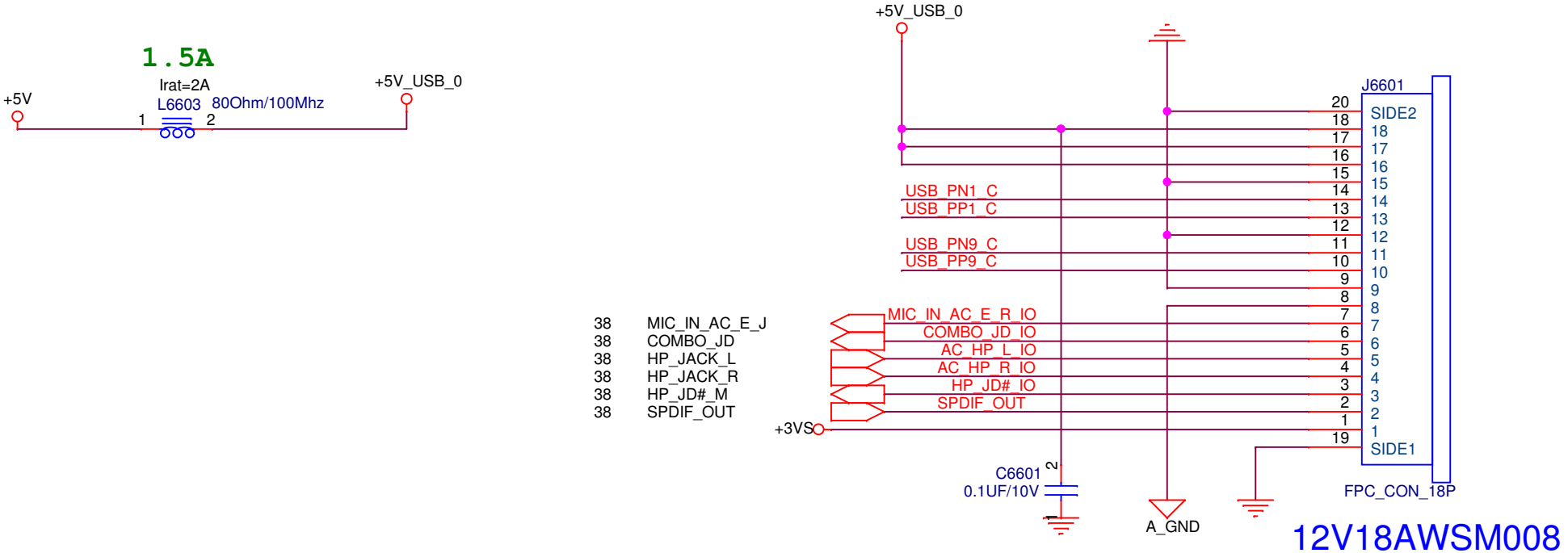




PEGATRON Title : ME_CONN,Skew Hole
Engineer: Trunks Chen

Size	Project Name	Rev
B	B34	1.0

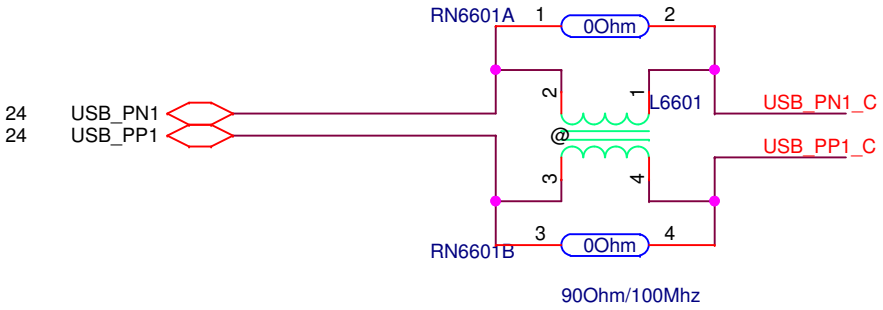
Date: Wednesday, February 01, 2012 Sheet 65 of 99

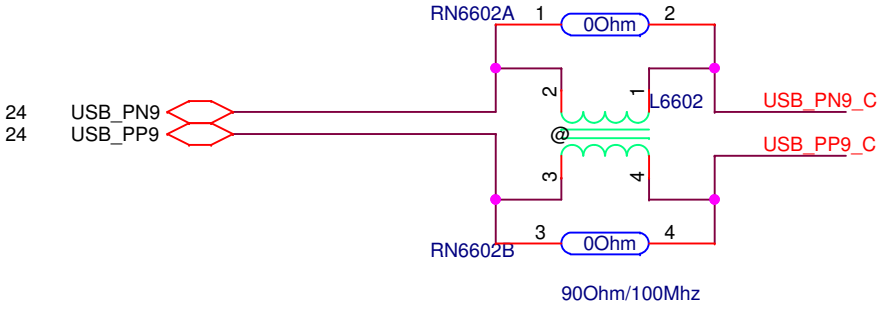


12V18AWSM008

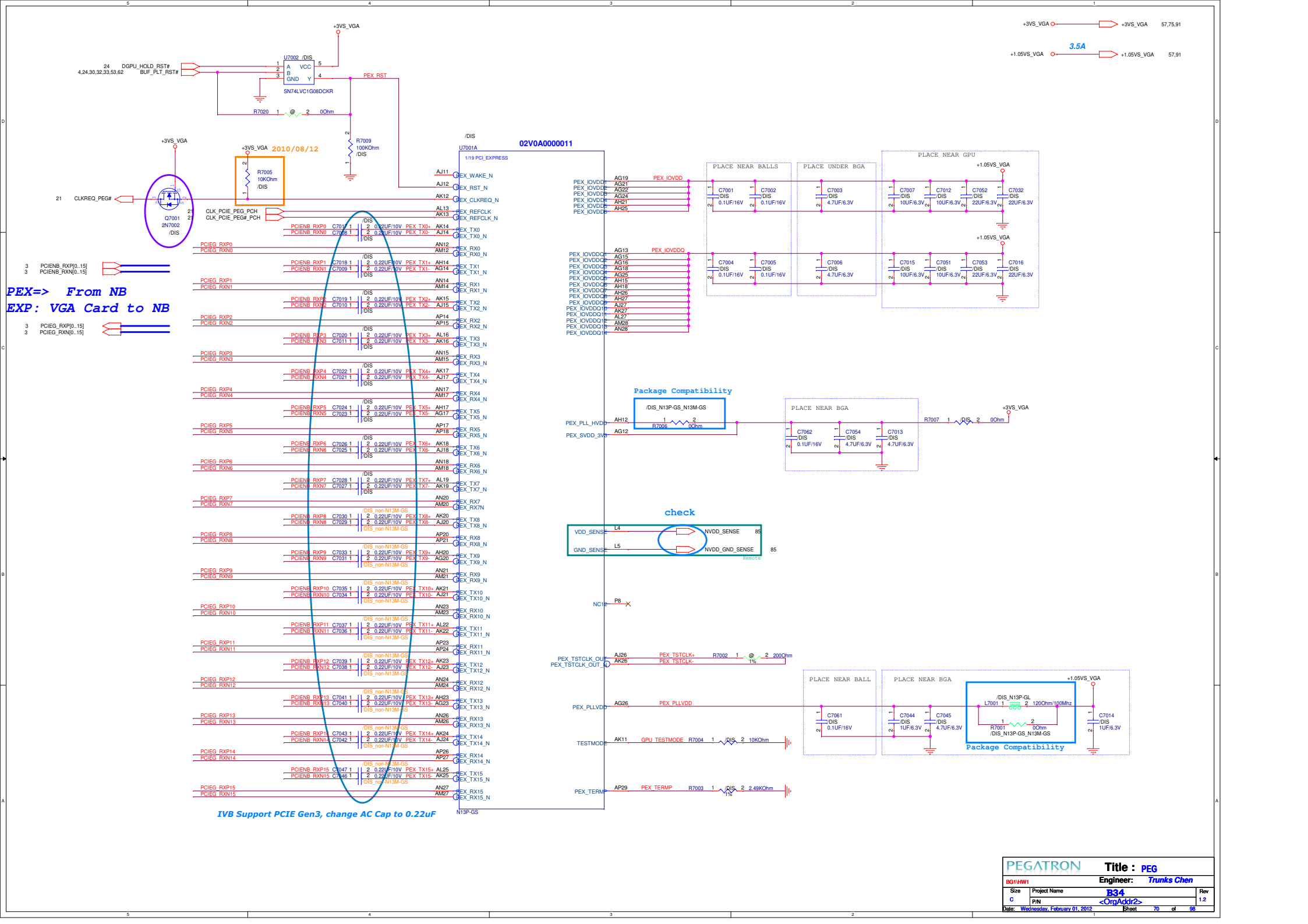
M:1218-0162000

S:1218-0189000





PEGATRON	Title : IO_BOARD_CONN.		
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Trunks Chen		
Size: A	Project Name: B34		Rev: 1.0
Date: Wednesday, February 01, 2012	Sheet 66 of 99		

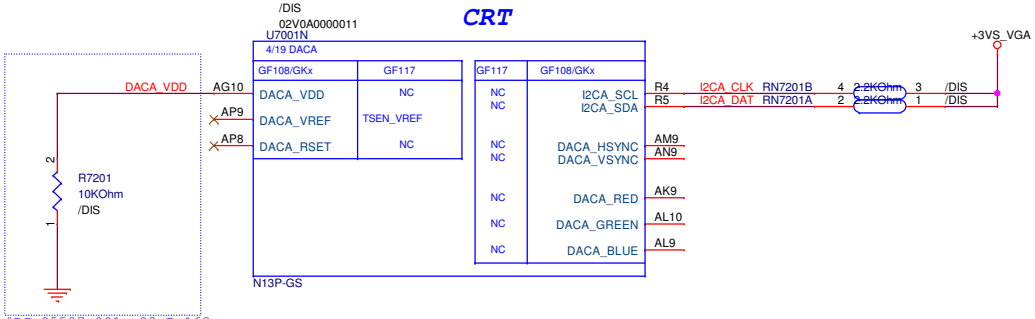


PEGATRON	Title : PEG	
BG1\HW1	Engineer: Trunks Chen	
Size: C	Project Name: B34	Rev: 1.2
	P/N: <OrgAddr2>	
Date: Wednesday, February 01, 2012	Sheet 70 of 98	


BOT SIDE
02V0A0000011
Package Compatibility
/DIS_N13P-GS_N13M-GS
PLACE CLOSE TO BALL
PLACE CLOSE TO GPU
PLACE NEAR BGA CLOSE TO CAPS
FBA_ODT
FBA_RST#
FBA_CKE
FBC_ODT
FBC_RST#
FBC_CKE
Place Near Balls
FBA
FBB
check
Main source :
Hynix DDR3 128M*16 900MHz / 1.5V
H5TQ2G63BFR-11C(0315-00ND000)
Hynix DDR3 64M*16 900MHz / 1.5V
H5TQ1G63DFR-11C(0315-00NF000)
Second source :
SAMSUNG DDR3 128M*16 900MHz / 1.5V
K4W2G1646C-HC11(0315-00NG000)
PEGATRON
Title : GPU F/B
Engineer: Trunks Chen
Project Name B34
P/N <OrgAddr2>
Rev 1.2
Date: Wednesday, February 01, 2012
Sheet 71 of 98

+3VS_VGA
+3VS_VGA 57,75,91
+1.05VS_VGA
+1.05VS_VGA 57,91

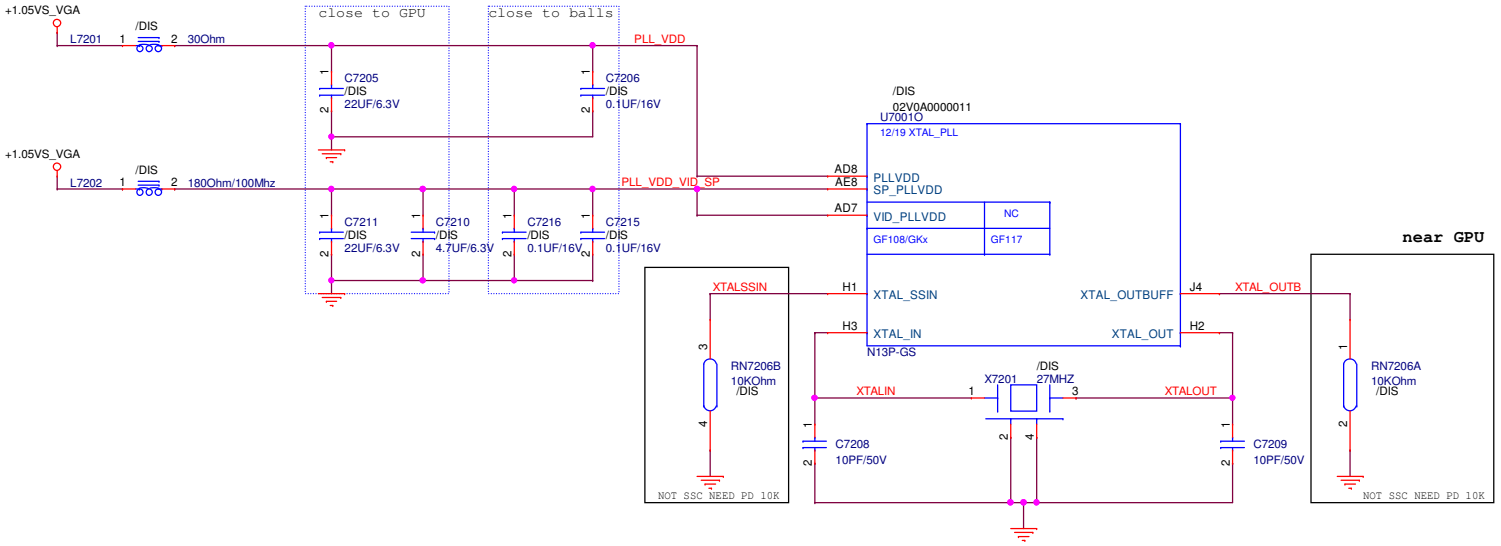
CRT



#DG-05587-001_v03 P.163
If a DAC interface is not required, it should be disabled by:
->Adding a pull-down to DACA_VDD with a 10KOhm to GND.
->All other DAC I/O pins (including DACA_VREF, DACA_RSET) can be left floating.

XTAL_IN , XTAL_OUT
3.3V tolerance

correspondent BGA balls must be
12mils and 16 mil wide



PEGATRON	Title : VGA-DACs, CLOCK GEN		
BG1\HW1	Engineer: Trunks Chen		
Size: Custom	Project Name: B34		Rev: 1.2
	P/N: <OrgAddr2>		
Date: Wednesday, February 01, 2012	Sheet 72 of 98		

+3VS_VGA → +3VS_VGA 57,75,91

+1.05VS_VGA → +1.05VS_VGA 57,91

LVDS

/DIS
02V0A0000011
U7001J
6/19 IFPAB

ALL PINS NC FOR GF117

AJ8	IFPAB_RSET	IFPA_TXC	AN6 / AM6
IFPAB_PLLVDD AH8	IFPAB_PLLVDD	IFPA_TXD0	AN3 / AP3
		IFPA_TXD1	AM5 / AN5
		IFPA_TXD2	AK6 / AL6
		IFPA_TXD3	AH6 / AJ6
		IFPB_TXC	AH9 / AJ9
IFPAB_IOVDD AG8	IFPA_IOVDD	IFPB_TXD4	AP5 / AP6
AG9	IFPB_IOVDD	IFPB_TXD5	AL7 / AM7
		IFPB_TXD6	AM8 / AN8
		IFPB_TXD7	AL8 / AK8
		GPIO14	N4

IFPAB

N13P-GS

RN7302B 10KOhm /DIS (3, 4)

RN7302A 10KOhm /DIS (1, 2)

HDMI

/DIS
02V0A0000011
U7001K
7/19 IFPC

ALL PINS NC FOR GF117

		DVI/HDMI		DP	
AF8	IFPC_RSET				
IFPC_PLLVDD AF7	IFPC_PLLVDD	I2CW_SDA / I2CW_SCL	IFPC_AUX_I2CW_SDA / IFPC_AUX_I2CW_SCL		AG2 / AG3
		TXC / TXC	IFPC_L3		AG4 / AG5
		TXD0 / TXD0	IFPC_L2		AH4 / AH3
		TXD1 / TXD1	IFPC_L1		AJ2 / AJ3
		TXD2 / TXD2	IFPC_L0		AJ1 / AK1
IFPC_IOVDD AF6	IFPC_IOVDD		GPIO15		P2

IFPC

N13P-GS

RN7304B 10KOhm /DIS (3, 4)

RN7301A 10KOhm /DIS (1, 2)

eDP

/DIS
02V0A0000011
U7001L
8/19 IFPD

ALL PINS NC FOR GF117

		DVI/HDMI		DP	
AN2	IFPD_RSET				
IFPD_PLLVDD AG7	IFPD_PLLVDD	I2CX_SDA / I2CX_SCL	IFPD_AUX_I2CX_SDA / IFPD_AUX_I2CX_SCL		AK2 / AK3
		TXC / TXC	IFPD_L3		AK5 / AK4
		TXD0 / TXD0	IFPD_L2		AL4 / AL3
		TXD1 / TXD1	IFPD_L1		AM4 / AM3
		TXD2 / TXD2	IFPD_L0		AM2 / AM1
IFPD_IOVDD AG6	IFPD_IOVDD		GPIO17		M6

IFPD

N13P-GS

RN7301B 10KOhm /DIS (3, 4)

RN7304A 10KOhm /DIS (1, 2)

IFPE / IFPF

/DIS
02V0A0000011
U7001M
9/19 IFPEF

ALL PINS NC FOR GF117

		DVI-DL	DVI-SL/HDMI	DP	
IFPE_PLLVDD AB8	IFPEF_PLLVDD				
AD6	IFPEF_RSET				
		I2CY_SDA / I2CY_SCL	I2CY_SDA / I2CY_SCL	IFPE_AUX_I2CY_SDA / IFPE_AUX_I2CY_SCL	AB4 / AB3
		TXC / TXC	TXC / TXC	IFPE_L3	AC5 / AC4
		TXD0 / TXD0	TXD0 / TXD0	IFPE_L2	AC3 / AC2
		TXD1 / TXD1	TXD1 / TXD1	IFPE_L1	AC1 / AD1
		TXD2 / TXD2	TXD2 / TXD2	IFPE_L0	AD3 / AD2
		HPD_E	HPD_E	GPIO18	R1
IFPE_IOVDD AC7	IFPE_IOVDD				
IFPF_IOVDD AC8	IFPF_IOVDD				
		I2CZ_SDA / I2CZ_SCL	I2CZ_SDA / I2CZ_SCL	IFPF_AUX_I2CZ_SDA / IFPF_AUX_I2CZ_SCL	AF2 / AF3
		TXC / TXC	TXC / TXC	IFPF_L3	AF1 / AG1
		TXD3 / TXD3	TXD0 / TXD0	IFPF_L2	AD5 / AD4
		TXD4 / TXD4	TXD1 / TXD1	IFPF_L1	AF5 / AF4
		TXD5 / TXD5	TXD2 / TXD2	IFPF_L0	AE4 / AE3
		HPD_F		GPIO19	P3

IFPE

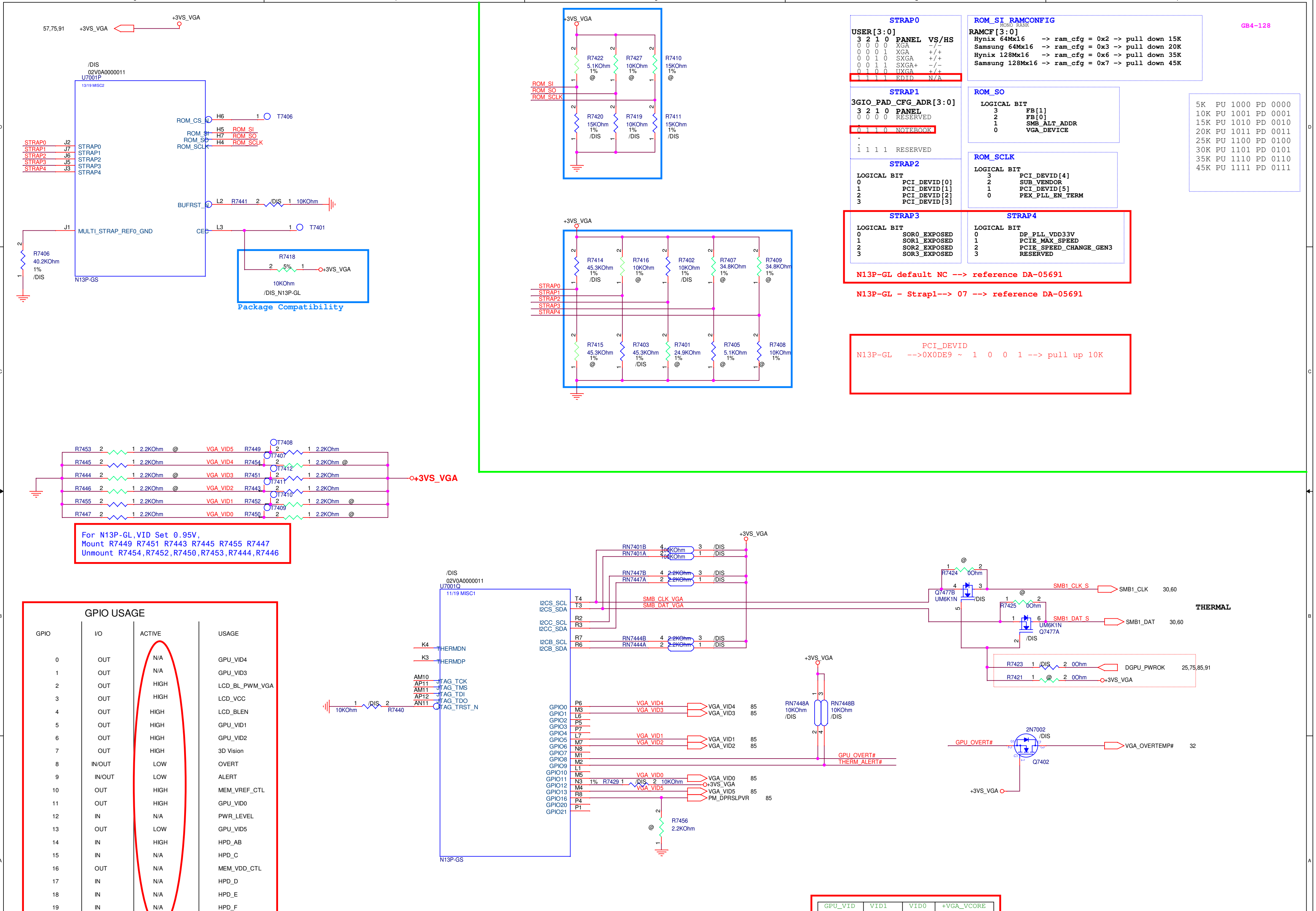
IFPF

N13P-GS

RN7303A 10KOhm /DIS (1, 2)

RN7303B 10KOhm /DIS (3, 4)

PEGATRON	Title : VGA-LVDS/TMDS		
BG1\HW1	Engineer: Trunks Chen		
Size: C	Project Name: B34		Rev: 1.2
	P/N: <OrgAddr2>		
Date: Wednesday, February 01, 2012	Sheet 73 of 98		



+3VS_VGA
57,75,91
U7001P
02V0A0000011
/DIS
13/19 MISC2
ROM_CS_N
ROM_SI
ROM_SO
ROM_SCLK
STRAP0
STRAP1
STRAP2
STRAP3
STRAP4
BUFRST_N
MULTI_STRAP_REF0_GND
CEC
N13P-GS
T7406
T7401
R7441 10KOhm
R7406 40.2KOhm 1% /DIS
R7418 5% 10KOhm /DIS_N13P-GL
Package Compatibility
R7422 5.1KOhm 1%
R7427 10KOhm 1%
R7410 15KOhm 1%
R7420 15KOhm 1% /DIS
R7419 10KOhm 1% /DIS
R7411 15KOhm 1% /DIS
R7414 45.3KOhm 1% /DIS
R7416 10KOhm 1%
R7402 10KOhm 1% /DIS
R7407 34.8KOhm 1%
R7409 34.8KOhm 1%
R7415 45.3KOhm 1%
R7403 45.3KOhm 1% /DIS
R7401 24.9KOhm 1%
R7405 5.1KOhm 1%
R7408 10KOhm 1%
STRAP0
USER[3:0]
3 2 1 0 PANEL VS/HS
0 0 0 0 XGA -/-
0 0 0 1 XGA +/+
0 0 1 0 SXGA +/+
0 0 1 1 SXGA+ -/-
0 1 0 0 UXGA +/+
1 1 1 1 EDID N/A
ROM_SI RAMCONFIG
MONO RANK
RAMCF[3:0]
Hynix 64Mx16 -> ram_cfg = 0x2 -> pull down 15K
Samsung 64Mx16 -> ram_cfg = 0x3 -> pull down 20K
Hynix 128Mx16 -> ram_cfg = 0x6 -> pull down 35K
Samsung 128Mx16 -> ram_cfg = 0x7 -> pull down 45K
GB4-128
STRAP1
3GIO_PAD_CFG_ADR[3:0]
3 2 1 0 PANEL
0 0 0 0 RESERVED
0 1 1 0 NOTEBOOK
1 1 1 1 RESERVED
ROM_SO
LOGICAL BIT
3 FB[1]
2 FB[0]
1 SMB_ALT_ADDR
0 VGA_DEVICE
5K PU 1000 PD 0000
10K PU 1001 PD 0001
15K PU 1010 PD 0010
20K PU 1011 PD 0011
25K PU 1100 PD 0100
30K PU 1101 PD 0101
35K PU 1110 PD 0110
45K PU 1111 PD 0111
STRAP2
LOGICAL BIT
0 PCI_DEVID[0]
1 PCI_DEVID[1]
2 PCI_DEVID[2]
3 PCI_DEVID[3]
ROM_SCLK
LOGICAL BIT
3 PCI_DEVID[4]
2 SUB_VENDOR
1 PCI_DEVID[5]
0 PEX_PLL_EN_TERM
STRAP3
LOGICAL BIT
0 SOR0_EXPOSED
1 SOR1_EXPOSED
2 SOR2_EXPOSED
3 SOR3_EXPOSED
STRAP4
LOGICAL BIT
0 DP_PLL_VDD33V
1 PCIE_MAX_SPEED
2 PCIE_SPEED_CHANGE_GEN3
3 RESERVED
N13P-GL default NC --> reference DA-05691
N13P-GL - Strap1--> 07 --> reference DA-05691
PCI_DEVID
N13P-GL -->0X0DE9 ~ 1 0 0 1 --> pull up 10K
R7453 2.2KOhm VGA_VID5 R7449 2.2KOhm T7408
R7445 2.2KOhm VGA_VID4 R7454 2.2KOhm T7407
R7444 2.2KOhm VGA_VID3 R7451 2.2KOhm T7412
R7446 2.2KOhm VGA_VID2 R7443 2.2KOhm T7411
R7455 2.2KOhm VGA_VID1 R7452 2.2KOhm T7410
R7447 2.2KOhm VGA_VID0 R7450 2.2KOhm T7409
+3VS_VGA
For N13P-GL,VID Set 0.95V,
Mount R7449 R7451 R7443 R7445 R7447
Unmount R7454,R7452,R7450,R7453,R7444,R7446
U7001Q
02V0A0000011
/DIS
11/19 MISC1
THERMDN
THERMDP
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_TRST_N
R7440 10KOhm /DIS
I2CS_SCL
I2CS_SDA
I2CC_SCL
I2CC_SDA
I2CB_SCL
I2CB_SDA
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
GPIO9
GPIO10
GPIO11
GPIO12
GPIO13
GPIO16
GPIO20
GPIO21
N13P-GS
RN7401B 10KOhm /DIS
RN7401A 10KOhm /DIS
RN7447B 2.2KOhm /DIS
RN7447A 2.2KOhm /DIS
RN7444B 2.2KOhm /DIS
RN7444A 2.2KOhm /DIS
SMB_CLK_VGA
SMB_DAT_VGA
VGA_VID4 85
VGA_VID3 85
VGA_VID1 85
VGA_VID2 85
VGA_VID0 85
+3VS_VGA
VGA_VID5 85
PM_DPRSLPVR 85
R7429 1% /DIS 10KOhm
R7456 2.2KOhm
RN7448A 10KOhm /DIS
RN7448B 10KOhm /DIS
GPU_OVERT#
THERM_ALERT#
R7424 0Ohm
Q7477B UM6K1N /DIS
SMB1_CLK_S
SMB1_CLK 30,60
R7425 0Ohm
SMB1_DAT_S
SMB1_DAT 30,60
UM6K1N Q7477A /DIS
THERMAL
R7423 /DIS 0Ohm
DGPU_PWROK 25,75,85,91
R7421 0Ohm
2N7002 /DIS Q7402
VGA_OVERTEMP# 32

GPIO USAGE

GPIO	I/O	ACTIVE	USAGE
0	OUT	N/A	GPU_VID4
1	OUT	N/A	GPU_VID3
2	OUT	HIGH	LCD_BL_PWM_VGA
3	OUT	HIGH	LCD_VCC
4	OUT	HIGH	LCD_BLEN
5	OUT	HIGH	GPU_VID1
6	OUT	HIGH	GPU_VID2
7	OUT	HIGH	3D Vision
8	IN/OUT	LOW	OVERT
9	IN/OUT	LOW	ALERT
10	OUT	HIGH	MEM_VREF_CTL
11	OUT	HIGH	GPU_VID0
12	IN	N/A	PWR_LEVEL
13	OUT	LOW	GPU_VID5
14	IN	HIGH	HPD_AB
15	IN	N/A	HPD_C
16	OUT	N/A	MEM_VDD_CTL
17	IN	N/A	HPD_D
18	IN	N/A	HPD_E
19	IN	N/A	HPD_F
20			RESERVED
21			RESERVED

GPU_VID	VID1	VID0	+VGA_VCORE
Low	0	0	
Med	0	1	
High	1	0	

PEGATRON

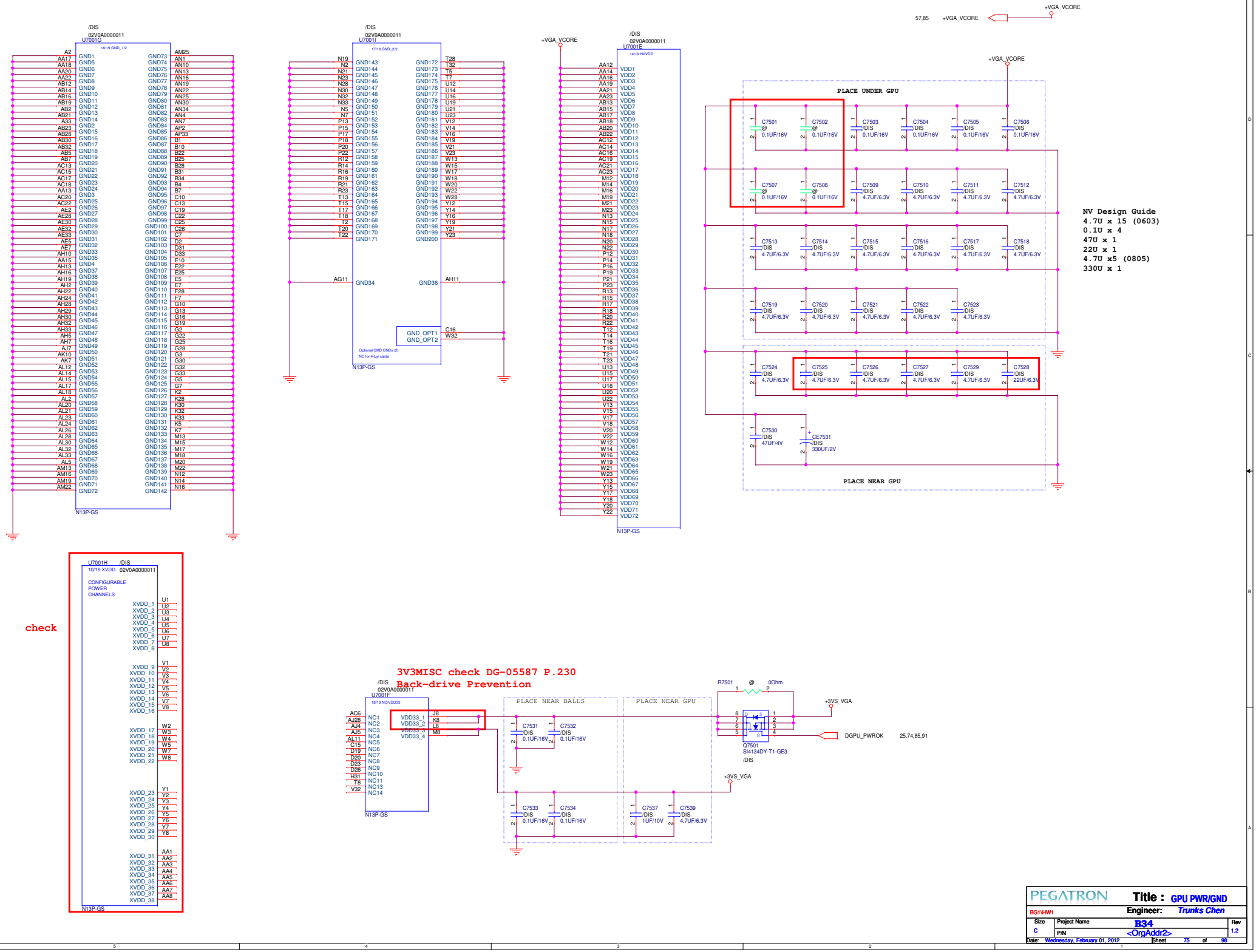
Title : VGA-STRAP, THERM, ROM

Engineer: Trunks Chen

BG1\HW1

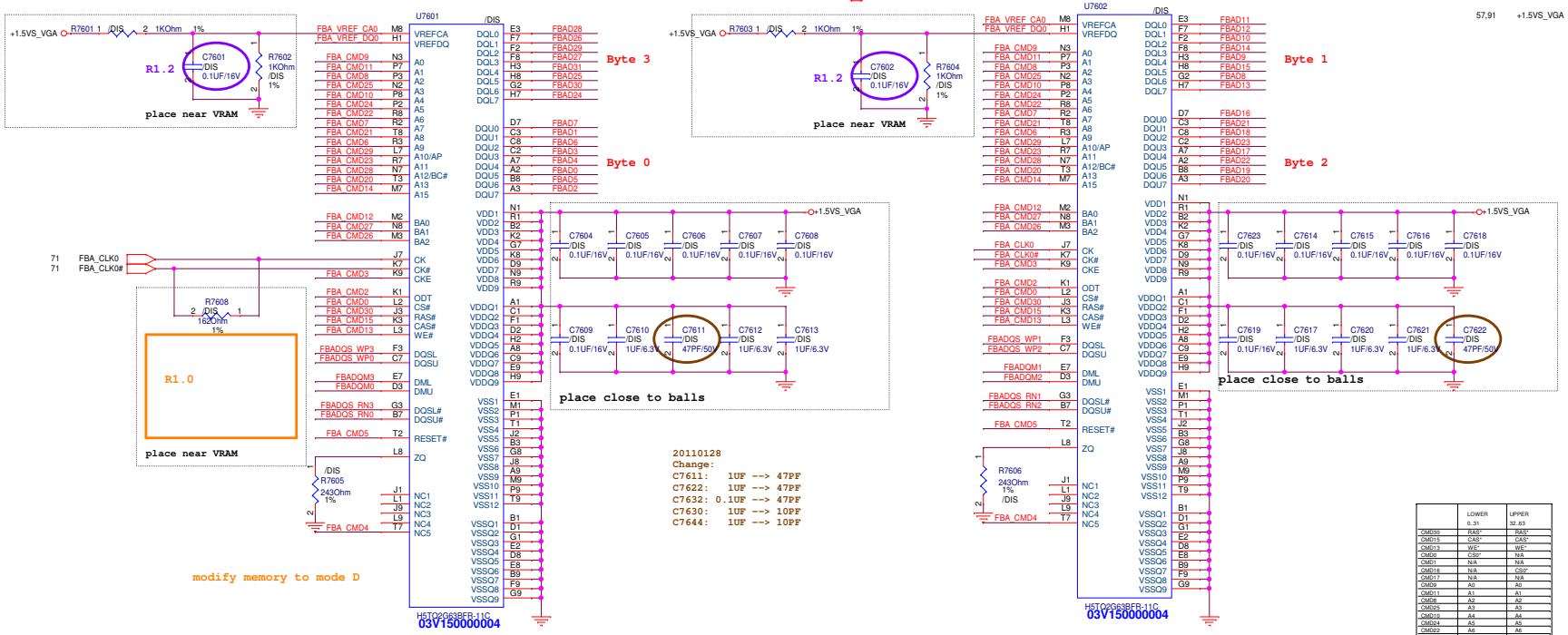
Size	Project Name	Rev
C	B34	1.2
	P/N <OrgAddr2>	

Date: Wednesday, February 01, 2012 Sheet 74 of 98


/DIS
02V0A0000011
U7001G
16/19 GND_1/2
N13P-GS
U7001I
17/19 GND_2/2
Optional CMD GNDs (2)
NC for 4-Lyr cards
U7001E
14/19 NVVDD
+VGA_VCORE
57,85
PLACE UNDER GPU
PLACE NEAR GPU
C7501 @ 0.1UF/16V
C7502 @ 0.1UF/16V
C7503 /DIS 0.1UF/16V
C7504 /DIS 0.1UF/16V
C7505 /DIS 0.1UF/16V
C7506 /DIS 0.1UF/16V
C7507 @ 0.1UF/16V
C7508 @ 0.1UF/16V
C7509 /DIS 4.7UF/6.3V
C7510 /DIS 4.7UF/6.3V
C7511 /DIS 4.7UF/6.3V
C7512 /DIS 4.7UF/6.3V
C7513 /DIS 4.7UF/6.3V
C7514 /DIS 4.7UF/6.3V
C7515 /DIS 4.7UF/6.3V
C7516 /DIS 4.7UF/6.3V
C7517 /DIS 4.7UF/6.3V
C7518 /DIS 4.7UF/6.3V
C7519 /DIS 4.7UF/6.3V
C7520 /DIS 4.7UF/6.3V
C7521 /DIS 4.7UF/6.3V
C7522 /DIS 4.7UF/6.3V
C7523 /DIS 4.7UF/6.3V
C7524 /DIS 4.7UF/6.3V
C7525 /DIS 4.7UF/6.3V
C7526 /DIS 4.7UF/6.3V
C7527 /DIS 4.7UF/6.3V
C7529 /DIS 4.7UF/6.3V
C7528 /DIS 22UF/6.3V
C7530 /DIS 47UF/4V
CE7531 /DIS 330UF/2V
NV Design Guide
4.7U x 15 (0603)
0.1U x 4
47U x 1
22U x 1
4.7U x5 (0805)
330U x 1
U7001H
10/19 XVDD
CONFIGURABLE POWER CHANNELS
check
3V3MISC check DG-05587 P.230
Back-drive Prevention
U7001F
18/19 NC/VDD33
PLACE NEAR BALLS
PLACE NEAR GPU
C7531 /DIS 0.1UF/16V
C7532 /DIS 0.1UF/16V
C7533 /DIS 0.1UF/16V
C7534 /DIS 0.1UF/16V
C7537 /DIS 1UF/10V
C7539 /DIS 4.7UF/6.3V
R7501 @ 0Ohm
Q7501 SI4134DY-T1-GE3
+3VS_VGA
DGPU_PWROK
25,74,85,91
PEGATRON
Title : GPU PWR/GND
BG1\HW1
Engineer: Trunks Chen
Size C
Project Name B34
P/N <OrgAddr2>
Rev 1.2
Date: Wednesday, February 01, 2012
Sheet 75 of 98

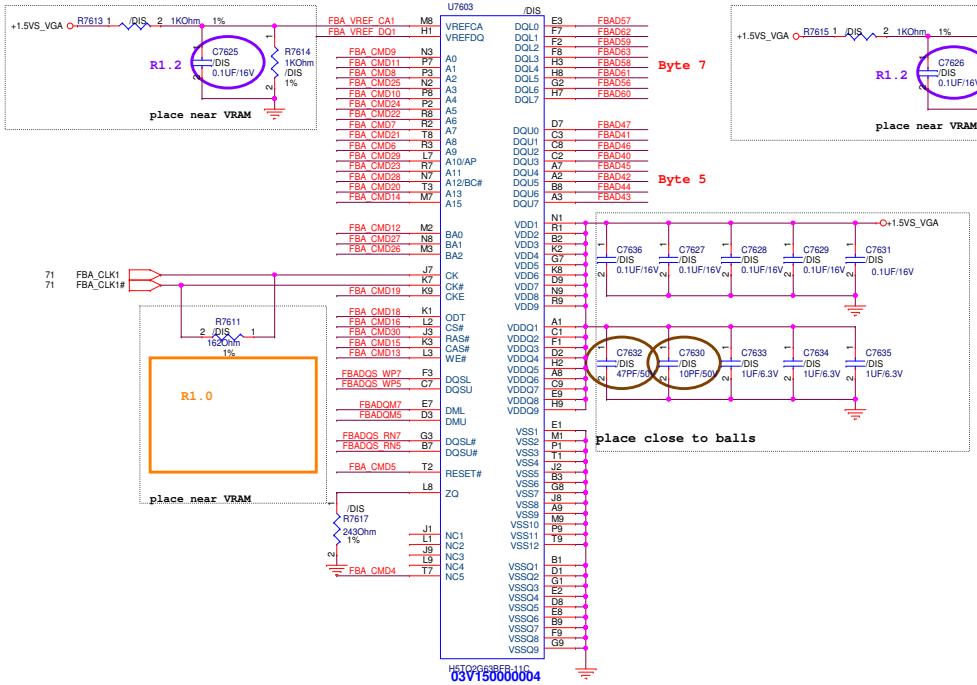
VRAM CH A

TOP SIDE --- M2

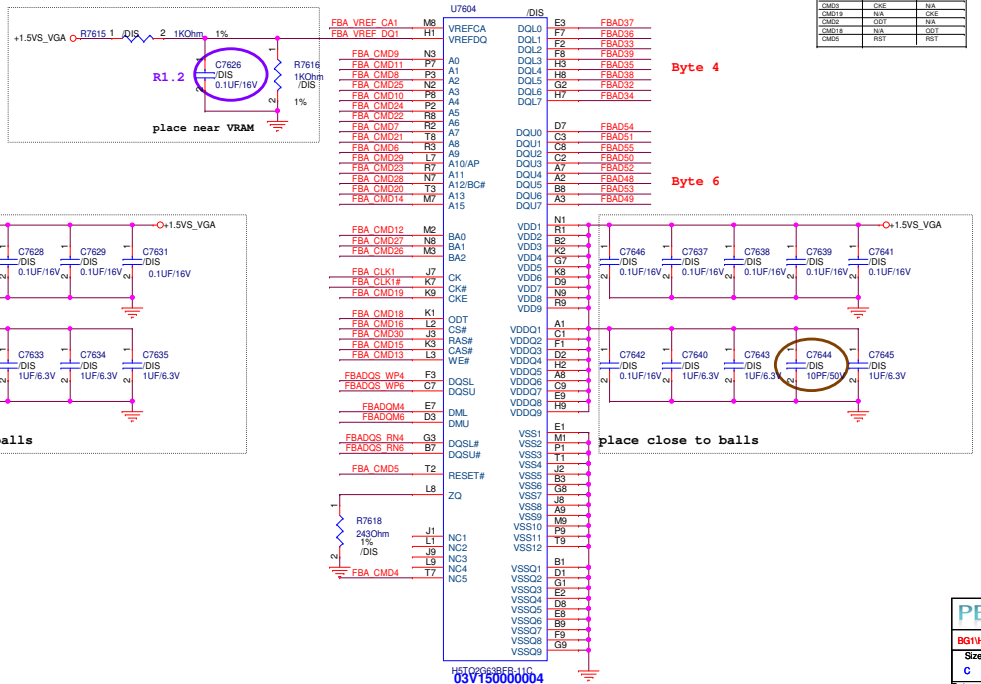


BOT SIDE --- M0

TOP SIDE --- M3



BOT SIDE --- M1



	LOWER 0..31	UPPER 32..63
CMD30	RAS*	RAS*
CMD15	CAS*	CAS*
CMD13	WE*	WE*
CMD0	CS0*	N/A
CMD1	N/A	N/A
CMD16	N/A	CS0*
CMD17	N/A	N/A
CMD9	A0	A0
CMD11	A1	A1
CMD8	A2	A2
CMD25	A3	A3
CMD10	A4	A4
CMD24	A5	A5
CMD22	A6	A6
CMD7	A7	A7
CMD21	A8	A8
CMD6	A9	A9
CMD29	A10	A10
CMD23	A11	A11
CMD28	A12	A12
CMD20	A13	A13
CMD4	A14	A14
CMD14	A15	A15
CMD12	BA0	BA0
CMD27	BA1	BA1
CMD26	BA2	BA2
CMD3	CKE	N/A
CMD2	N/A	ODT
CMD18	N/A	ODT
CMD5	RST	RST

PEGATRON

Title : FRAME BUFFER A

BG1\HW1

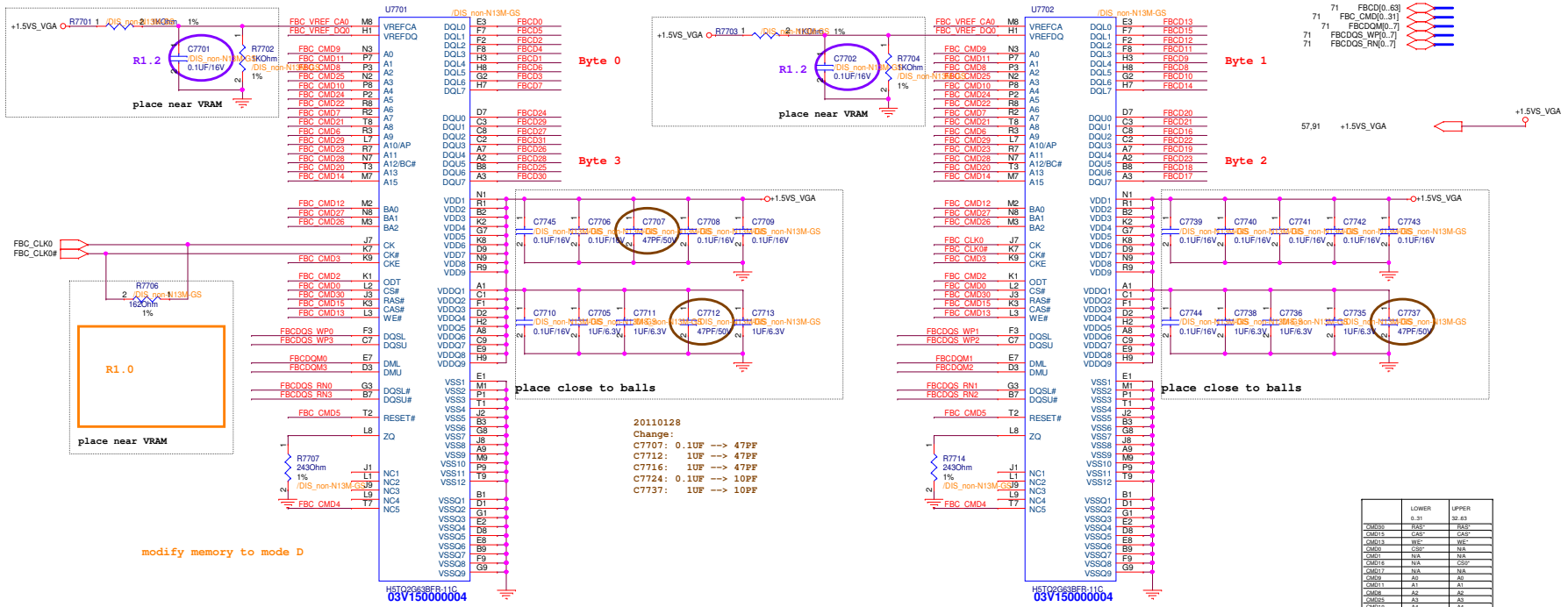
Engineer: Trunks Chen

Size	Project Name	Rev
C	B34	1.2
	P/N <OrgAddr2>	

Date: Wednesday, February 01, 2012 Sheet 76 of 98

VRAM CH C

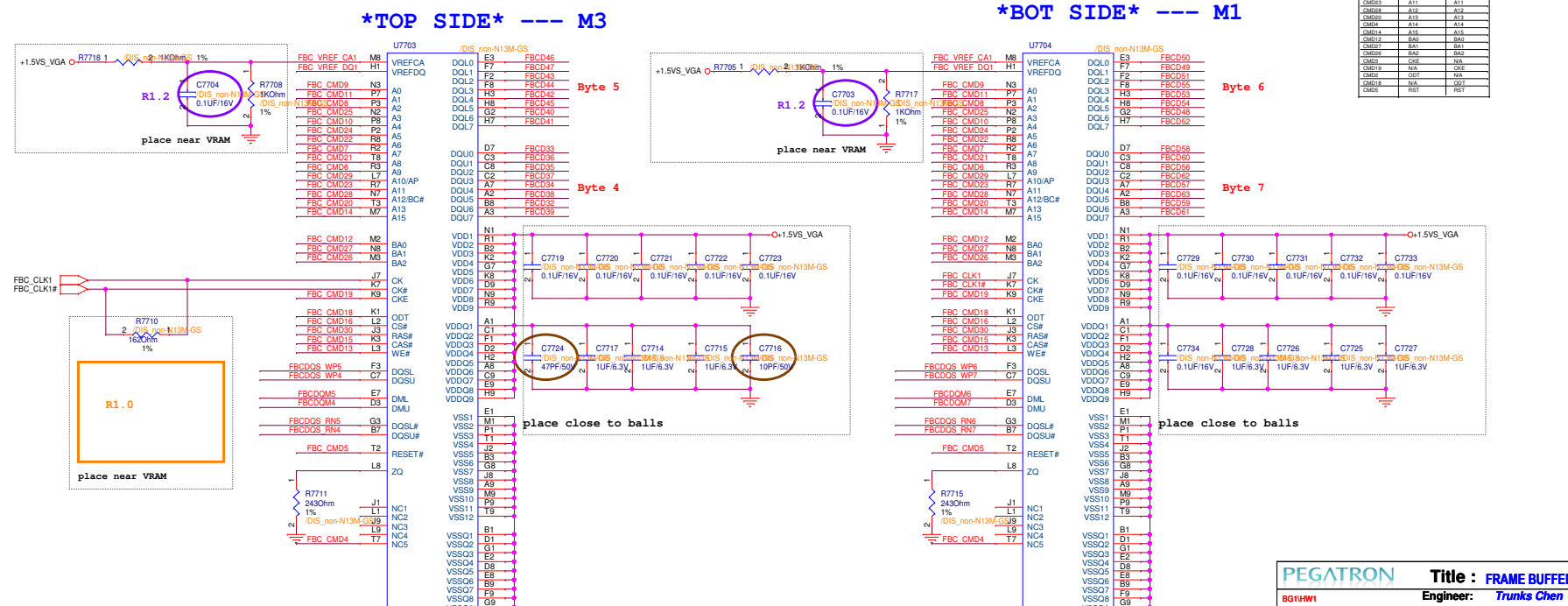
TOP SIDE --- M2



20110128
Change:
C7707: 0.1UF --> 47PF
C7712: 1UF --> 47PF
C7716: 1UF --> 47PF
C7724: 0.1UF --> 10PF
C7737: 1UF --> 10PF

BOT SIDE --- M0

TOP SIDE --- M3



BOT SIDE --- M1

	LOWER 0..31	UPPER 32..63
CMD30	RAS*	RAS*
CMD15	CAS*	CAS*
CMD13	WE*	WE*
CMD0	CS0*	N/A
CMD1	N/A	N/A
CMD16	N/A	CS0*
CMD17	N/A	N/A
CMD9	A0	A0
CMD11	A1	A1
CMD8	A2	A2
CMD25	A3	A3
CMD10	A4	A4
CMD24	A5	A5
CMD22	A6	A6
CMD7	A7	A7
CMD21	A8	A8
CMD6	A9	A9
CMD29	A10	A10
CMD23	A11	A11
CMD28	A12	A12
CMD20	A13	A13
CMD4	A14	A14
CMD14	A15	A15
CMD12	BA0	BA0
CMD27	BA1	BA1
CMD26	BA2	BA2
CMD3	CKE	N/A
CMD19	N/A	CKE
CMD2	ODT	N/A
CMD18	N/A	ODT
CMD5	RST	RST

PEGATRON	Title : FRAME BUFFER C		
BG1\HW1	Engineer: Trunks Chen		
Size: Custom	Project Name: B34		Rev: 1.2
	P/N: <OrgAddr2>		
Date: Wednesday, February 01, 2012	Sheet 77 of 98		

R1.0
delete Ventura.

PEGATRON

Title :VGA_VENTURA_INA219

PEGATRON COMPUTER INC

Engineer: Trunks Chen

Size	Project Name	Rev
B	B34	1.2
	P/N <OrgAddr2>	

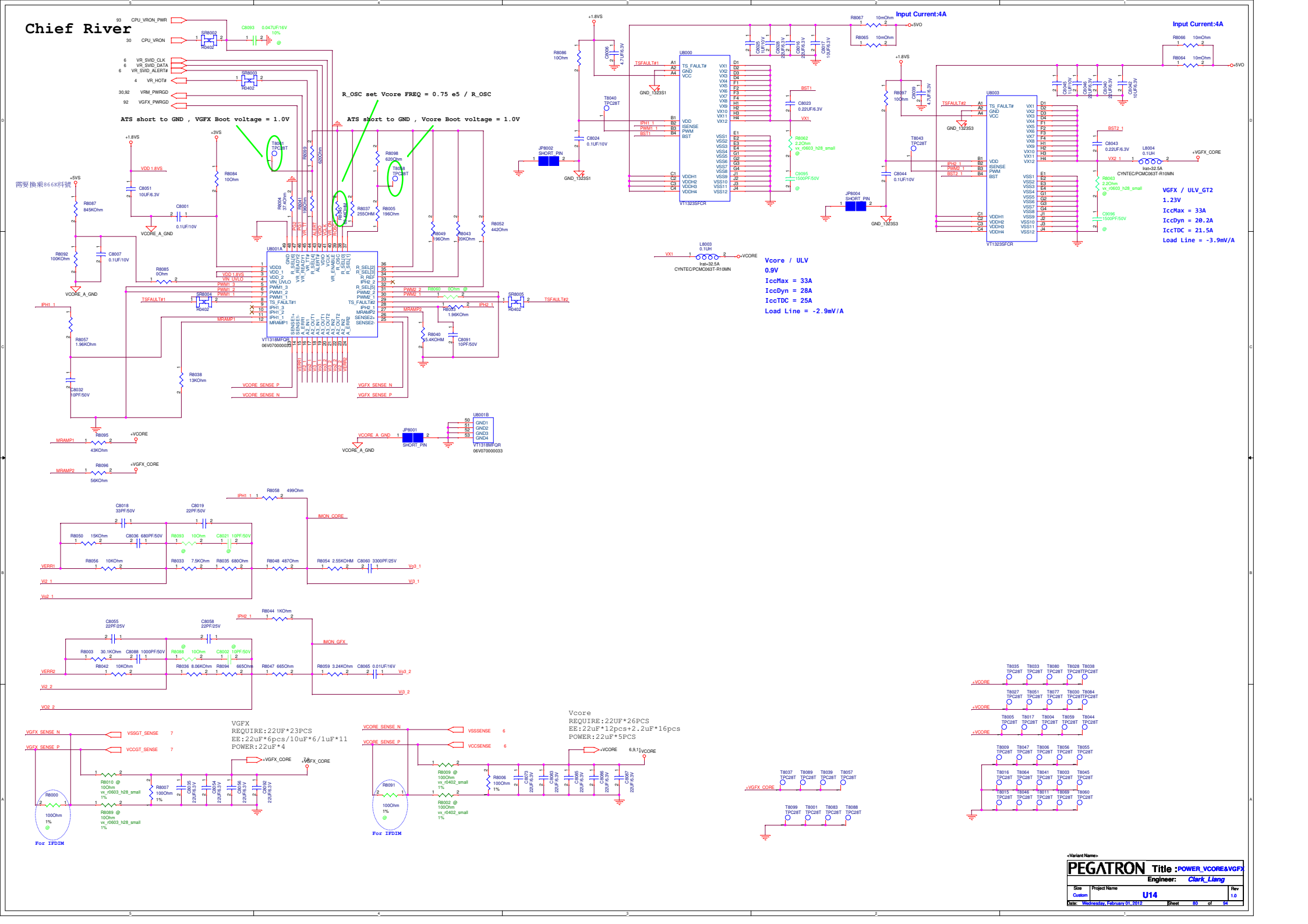
Date: Wednesday, February 01, 2012 Sheet 78 of 98

R1.0

delete GB3-128 additional schematic.

PEGATRON	Title : ADDITIOAL		
BG1\HW1	Engineer: *Trunks Chen*		
Size: A	Project Name: B34		Rev: 1.2
	P/N: <OrgAddr2>		
Date: Wednesday, February 01, 2012	Sheet 79 of 98		

Chief River



<Variant Name>

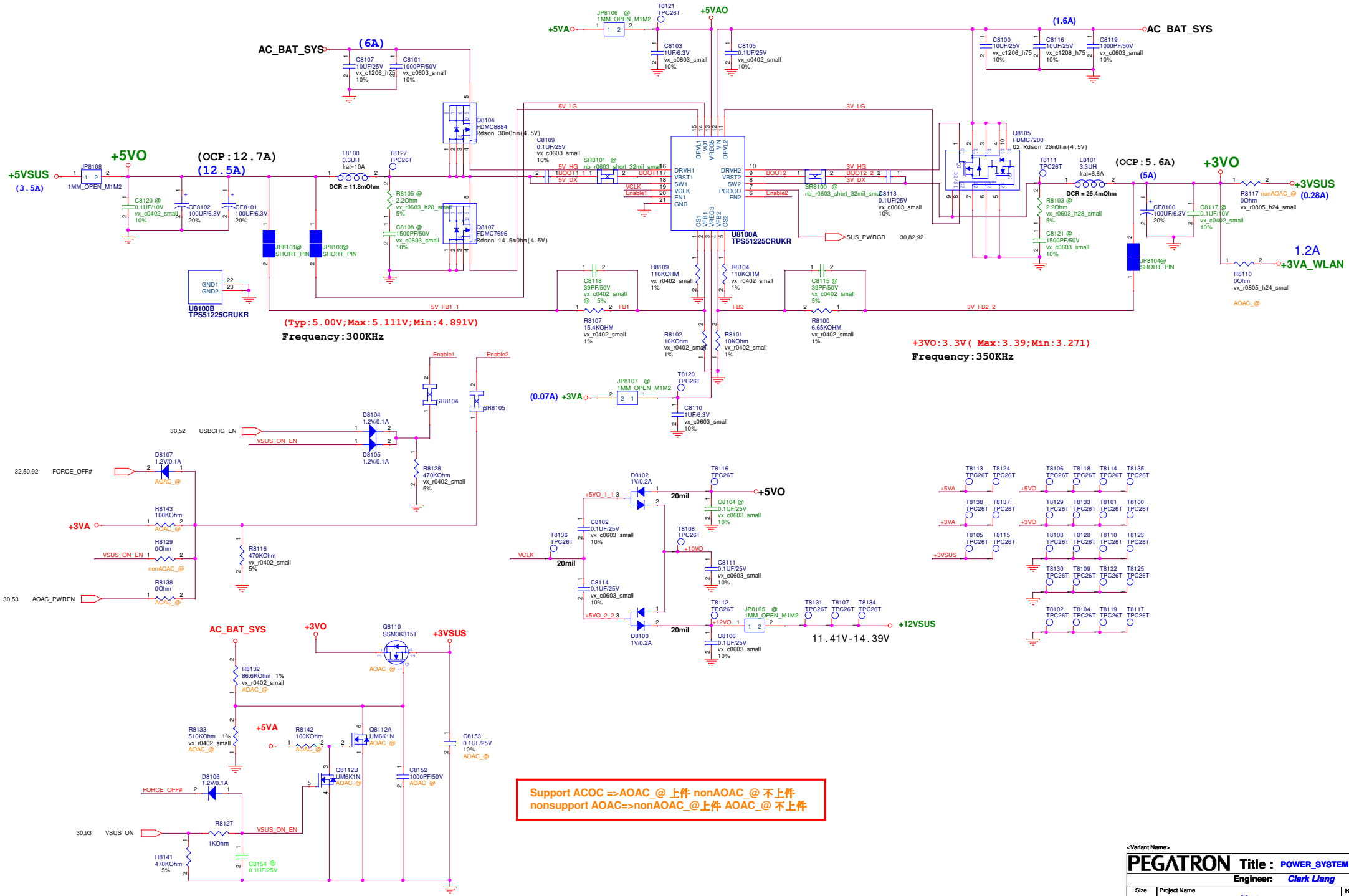
PEGATRON Title : POWER_VCORE&VGFX

Engineer: Clark_Liang

Size	Project Name	Rev
Custom	U14	1.0

Date: Wednesday, February 01, 2012 Sheet 80 of 94

+5VO & +3VO POWER SUPPLY



<Variant Name>

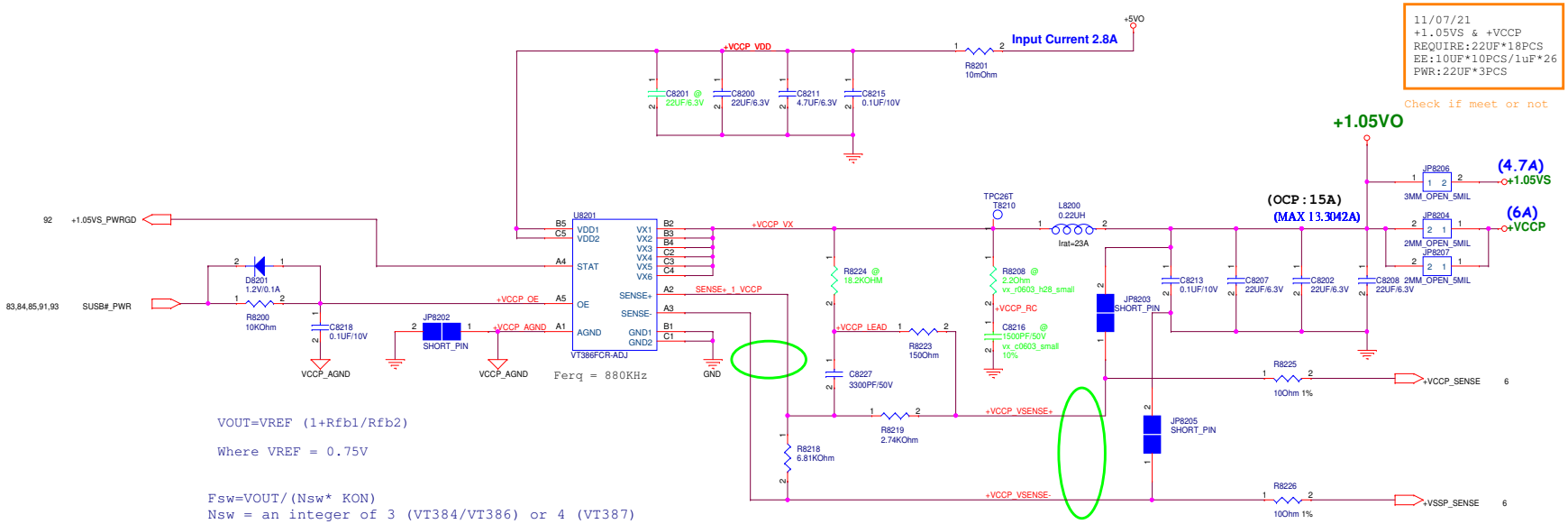
PEGATRON Title : POWER_SYSTEM

Engineer: Clark Liang

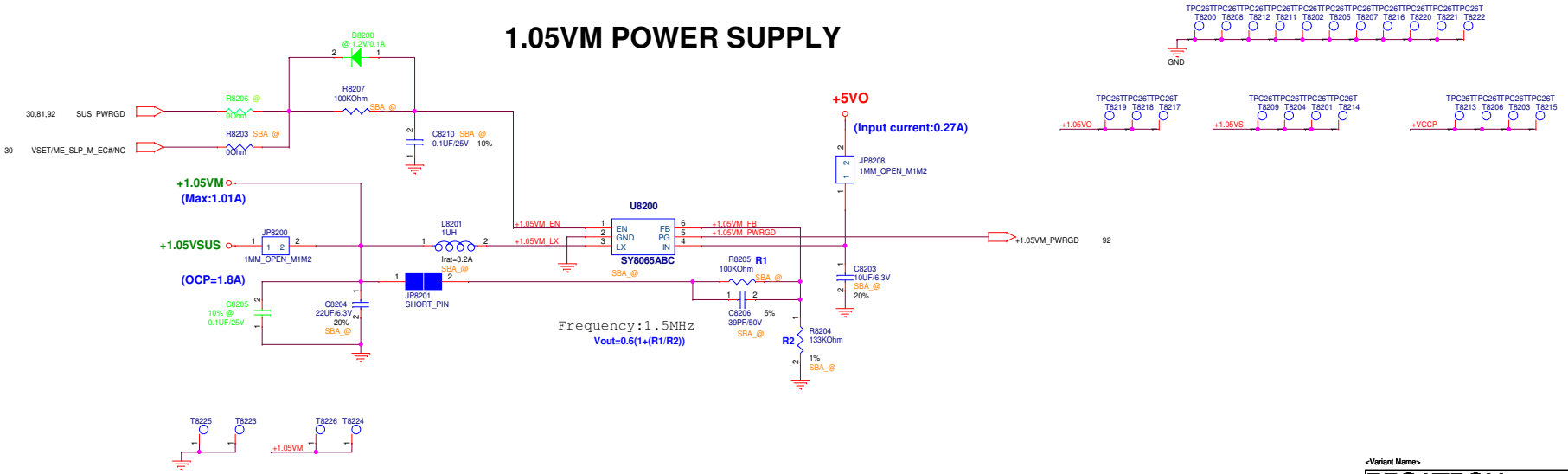
Size: Custom | Project Name: U14 | Rev: 1.0

Date: Wednesday, February 01, 2012 Sheet 81 of 94

+1.05VO POWER SUPPLY



1.05VM POWER SUPPLY



<Variant Name>

PEGATRON Title :POWER_+VCCP

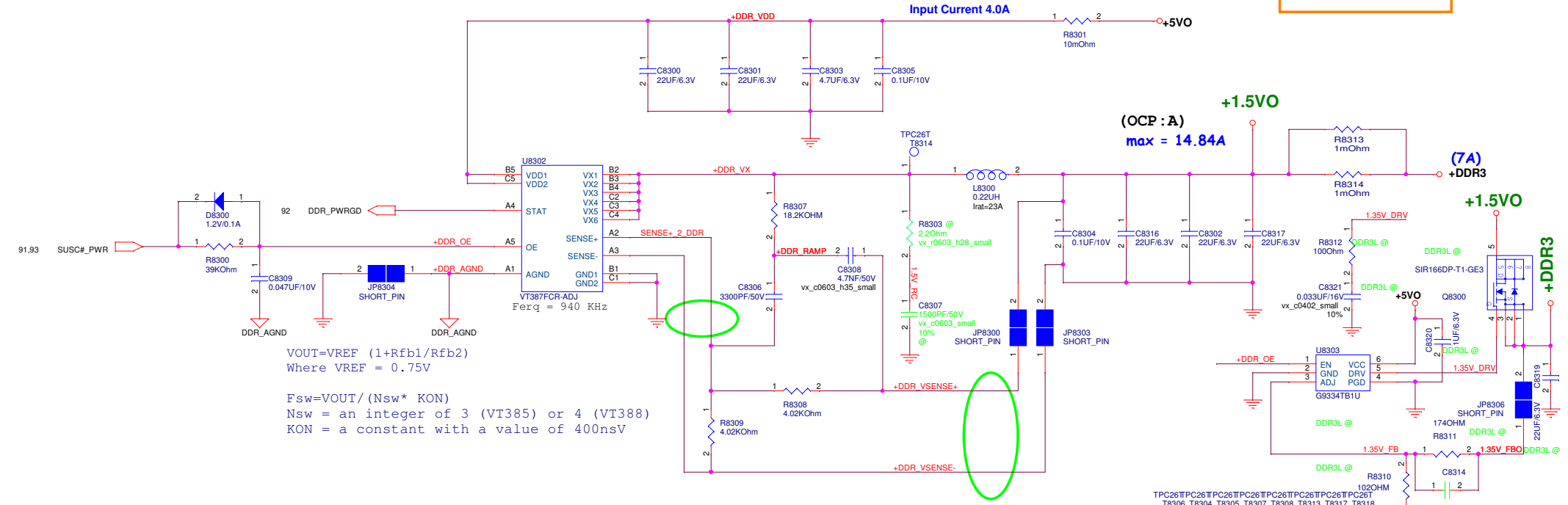
Engineer: Clark Liang

Size	Project Name	Rev
C	U14	1.0

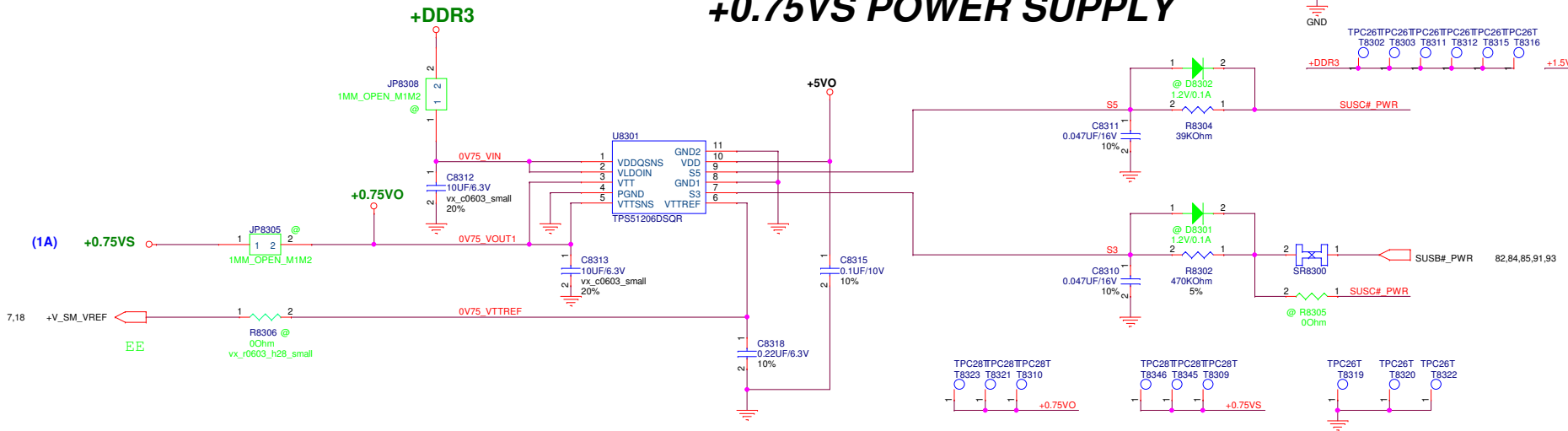
Date: Wednesday, February 01, 2012 Sheet 82 of 94

+1.5VO POWER SUPPLY

11/07/21
+1.5VO
REQUIRE:22UF*6PCS
EE:10UF*8PCS/1uF*10PCS
PWR:22UF*3PCS



+0.75VS POWER SUPPLY



PEGATRON

Title : POWER_DDR & VTT

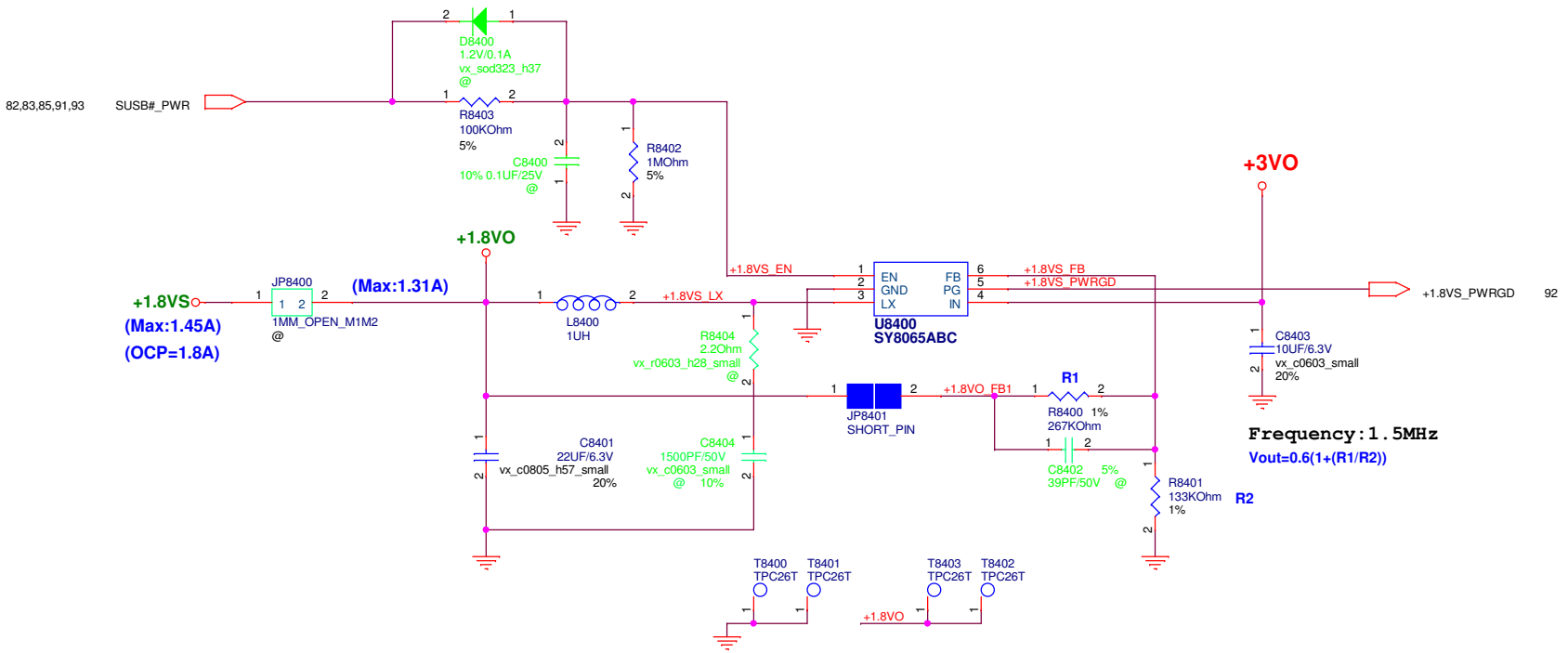
<OrgName>

Engineer: Clark Liang

Size	Project Name	Rev
Custom	U14	1.0

Date: Wednesday, February 01, 2012 Sheet 83 of 94

+1.8VS POWER SUPPLY



<Variant Name>

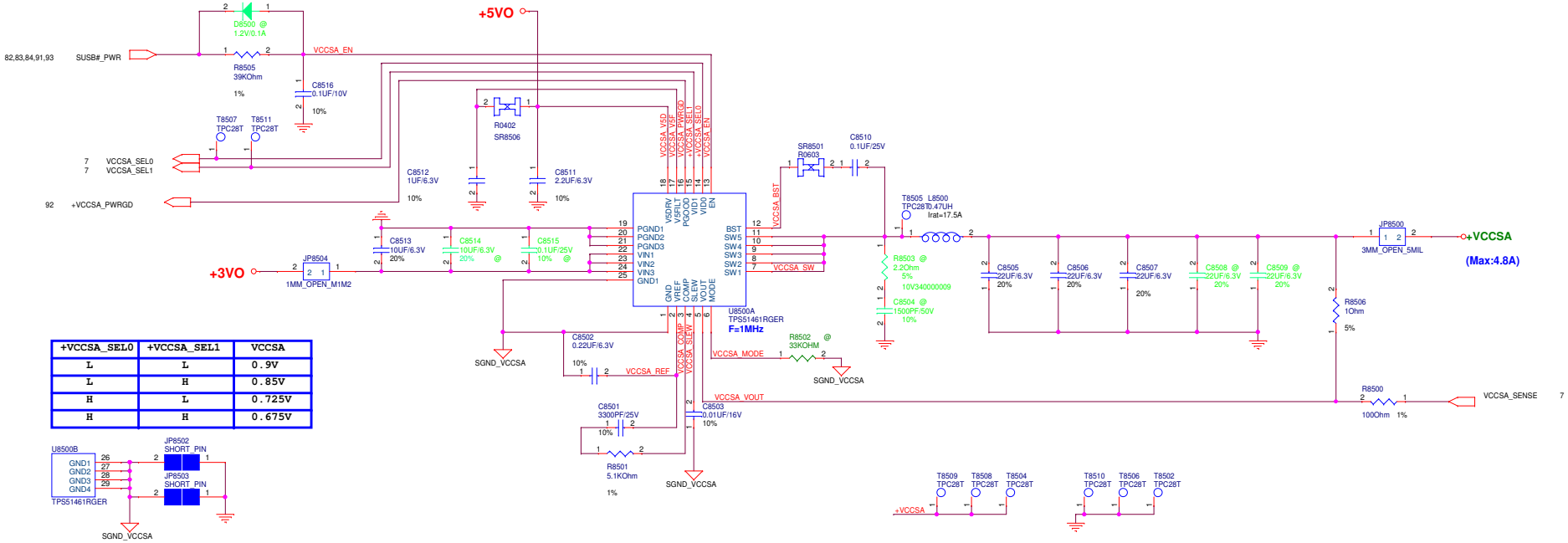
PEGATRON Title : POWER_+1.8VS

Engineer: Clark Liang

Size	Project Name	Rev
Custom	U14	1.0

Date: Wednesday, February 01, 2012 Sheet 84 of 94

IVB VCCSA POWER SUPPLY



+VCCSA_SEL0	+VCCSA_SEL1	VCCSA
L	L	0.9V
L	H	0.85V
H	L	0.725V
H	H	0.675V

<Variant Name>

PEGATRON Title : POWER_+VCCSA_0.85VS

Engineer: Clark Liang

Size	Project Name	Rev
C	U14	1.0

Date: Wednesday, February 01, 2012 Sheet 85 of 94

VID[6:0]= [0100111];V=1.0125V
PSI#=0;
PROC_DPRSLPVR=1;

PM_DPRSLPVR	MODE
L	2 Phase CCM
H	2 Phase DCM

Input Current:4.5A

(MAX : 44.16A)
+VGA_VCORE

VGA_CORE
REQUIRE:22UF*21PCS
EE:22UF*17PCS
PWR:22UF*4PCS

Input Current:4.5A

<Variant Name>

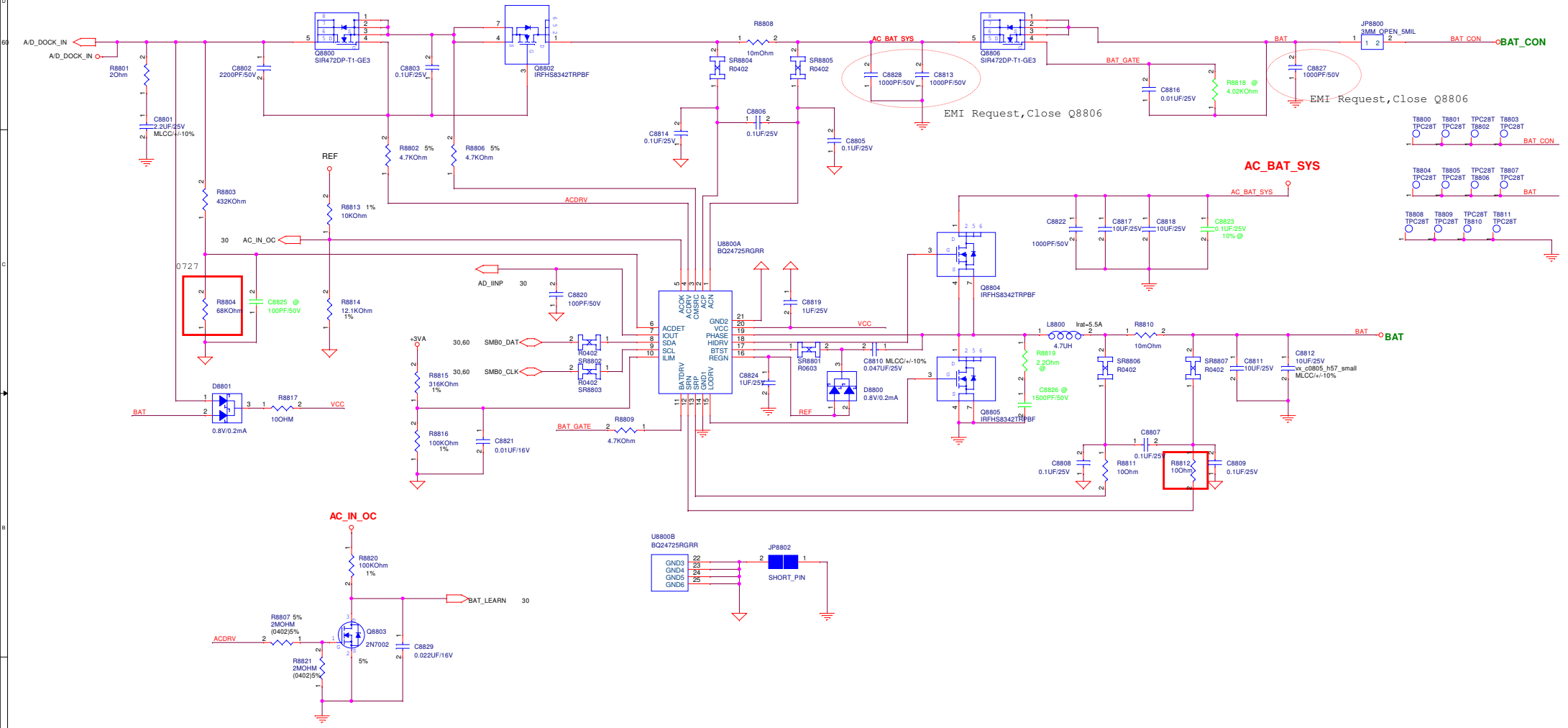
PEGATRON Title : POWER_VCORE

Engineer: Clark Liang

Size	Project Name	Rev
Custom	U14	2.0

Date: Wednesday, February 01, 2012 Sheet 85 of 94

BATTERY CHARGER



<Variant Name>

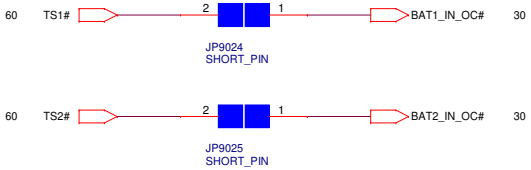
PEGATRON Title : POWER_CHARGER

Engineer: Clark Liang

Size	Project Name	Rev
Custom	U14	1.0

Date: Wednesday, February 01, 2012 Sheet 88 of 94

BATTERY IN DETECT



<Variant Name>

PEGATRON Title : POWER_DETECT

Engineer: Clark Liang

Size	Project Name	Rev
Custom	U14	1.0

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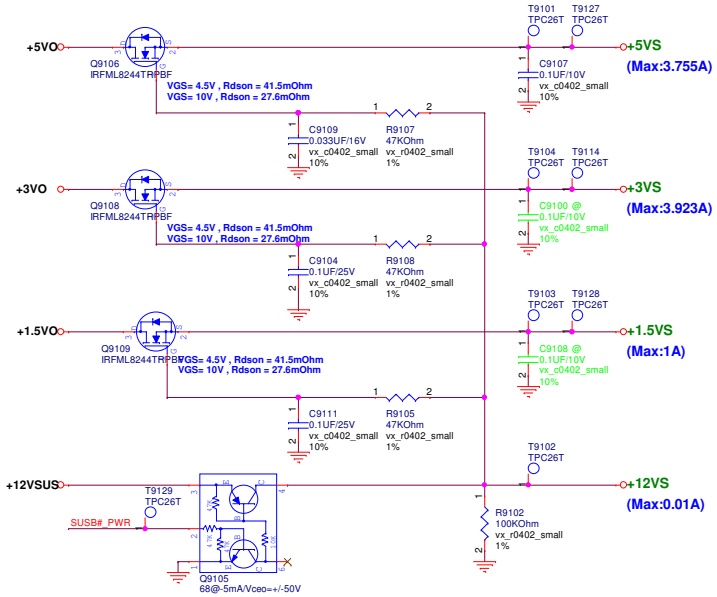
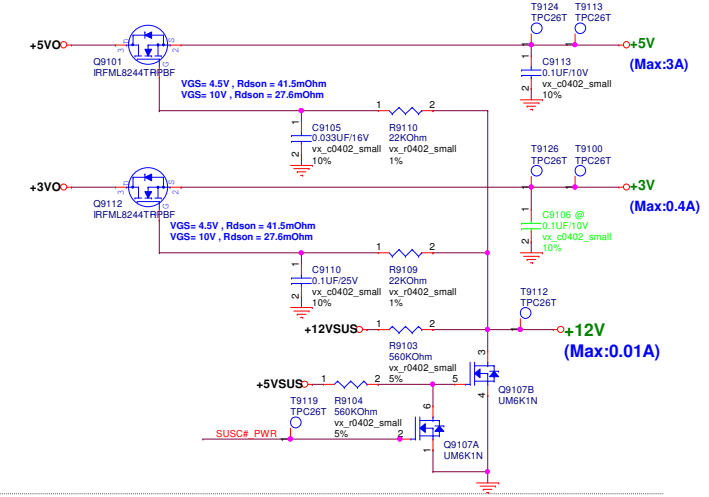
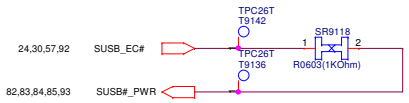
SUSB#_PWR POWER



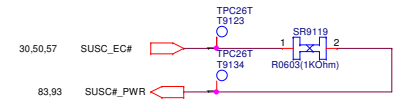
SUSC#_PWR POWER



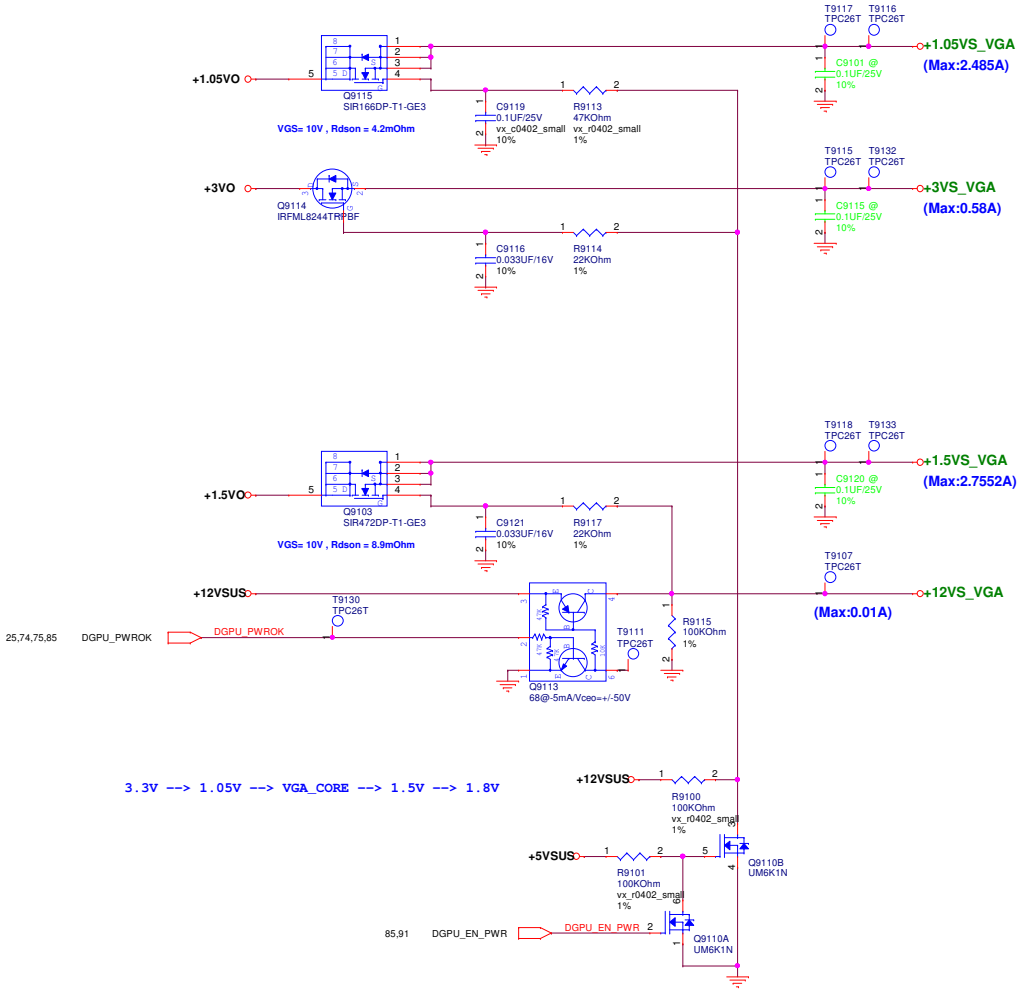
SUSB#_PWR POWER Control



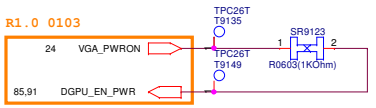
SUSB#_PWR POWER Control



DSC#_PWR POWER(dGPU)



DSC_VGA_PWR POWER Control



<Variant Name>

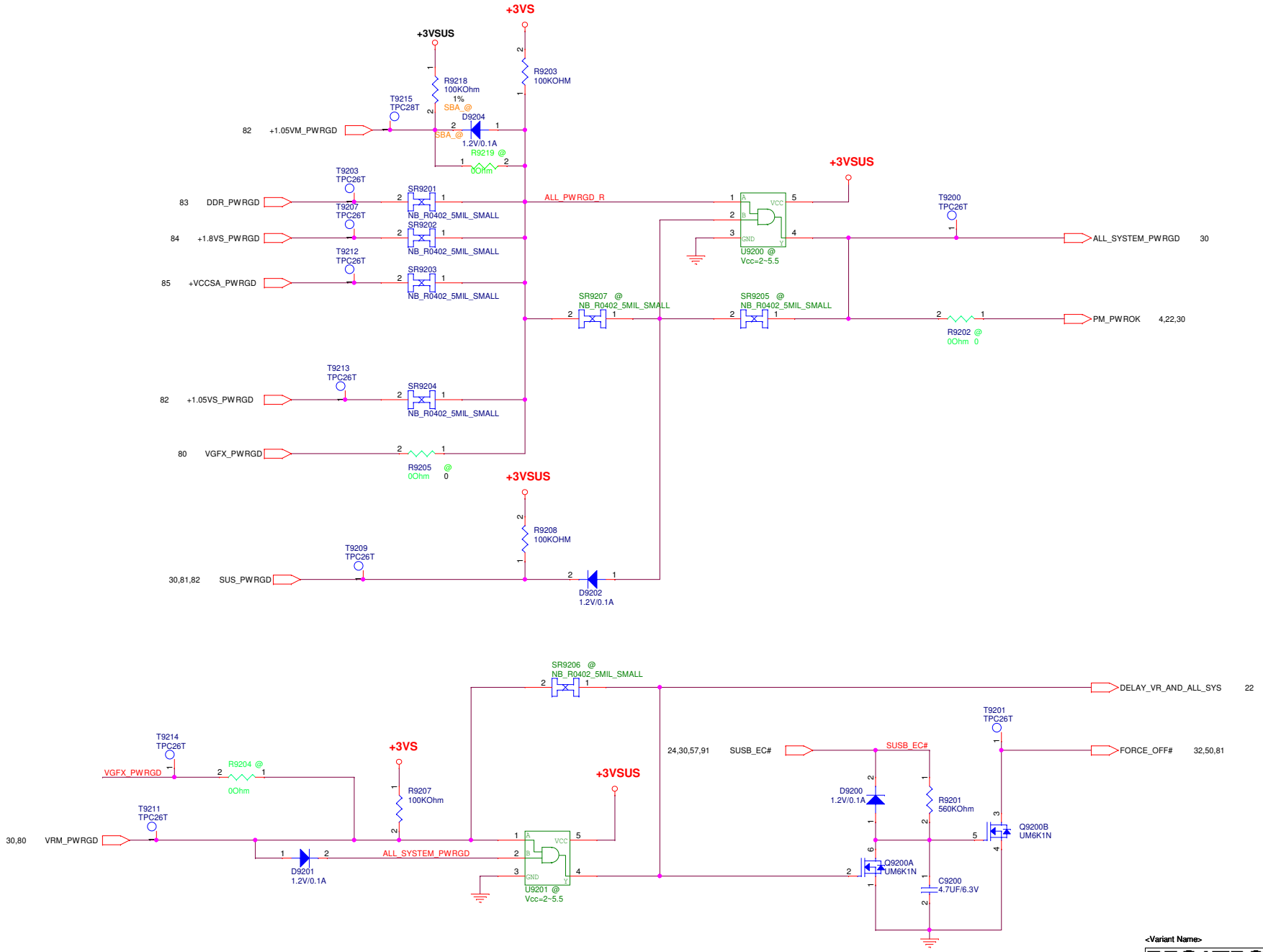
PEGATRON Title : POWER_LOAD SWITCH

Engineer: Clark Liang

Size	Project Name	Rev
Custom	U14	1.0

Date: Wednesday, February 01, 2012 Sheet 91 of 94

POWER GOOD DETECTER



<Variant Name>

PEGATRON Title :POWER_PROTECT

Engineer: Clark Liang

Size	Project Name	Rev
Custom	U14	1.0

Date: Wednesday, February 01, 2012 Sheet 92 of 94

AC_BAT_SYS — AC_BAT_SYS 45,81,88

BAT — BAT 88

BAT_CON — BAT_CON 60,88

BAT1_CON — BAT1_CON 60

BAT2_CON — BAT2_CON 60

+3VA — +3VA 6,20,27,30,56,57,81,88

+5VA — +5VA 50,52,56,81

+5VO — +5VO 80,81,82,83,85,91

+3VO — +3VO 81,84,85,91

+1.05VO — +1.05VO 82,91

+0.75VO — +0.75VO 83

+1.5VO — +1.5VO 83,91

+1.8VO — +1.8VO 84

+5VSUS — +5VSUS 27,52,81,91

+3VSUS — +3VSUS 22,24,27,28,30,33,53,56,81,92

+12VSUS — +12VSUS 81,91

+5V — +5V 52,55,56,57,66,91

+3V — +3V 24,40,53,55,57,62,91

+12V — +12V 91

+5VS — +5VS 27,30,31,38,46,48,50,51,53,56,57,80,91

+3VS — +3VS 16,17,20,21,22,23,24,25,26,27,28,30,31,32,33,38,44,45,46,48,50,51,53,56,57,62,66,80,85,91,92

+12VS — +12VS 20,28,48,91

+1.05VS — +1.05VS 26,27,82,85

+0.75VS — +0.75VS 16,17,57,83

+1.5VS — +1.5VS 26,53,57,91

+1.8VS — +1.8VS 7,25,26,80,84

+VCCSA — +VCCSA 7,85

+VCORE — +VCORE 6,9,11,80

+VGFX_CORE — +VGFX_CORE 7,9,80

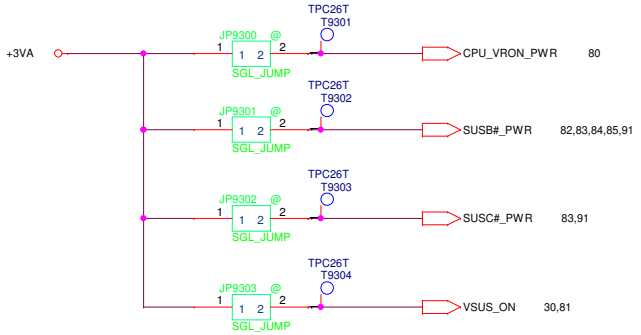
+12VS_VGA — +12VS_VGA 91

+1.5VS_VGA — +1.5VS_VGA 57,91

+1.05VS_VGA — +1.05VS_VGA 57,91

+3VS_VGA — +3VS_VGA 57,75,91

FOR POWER TEST



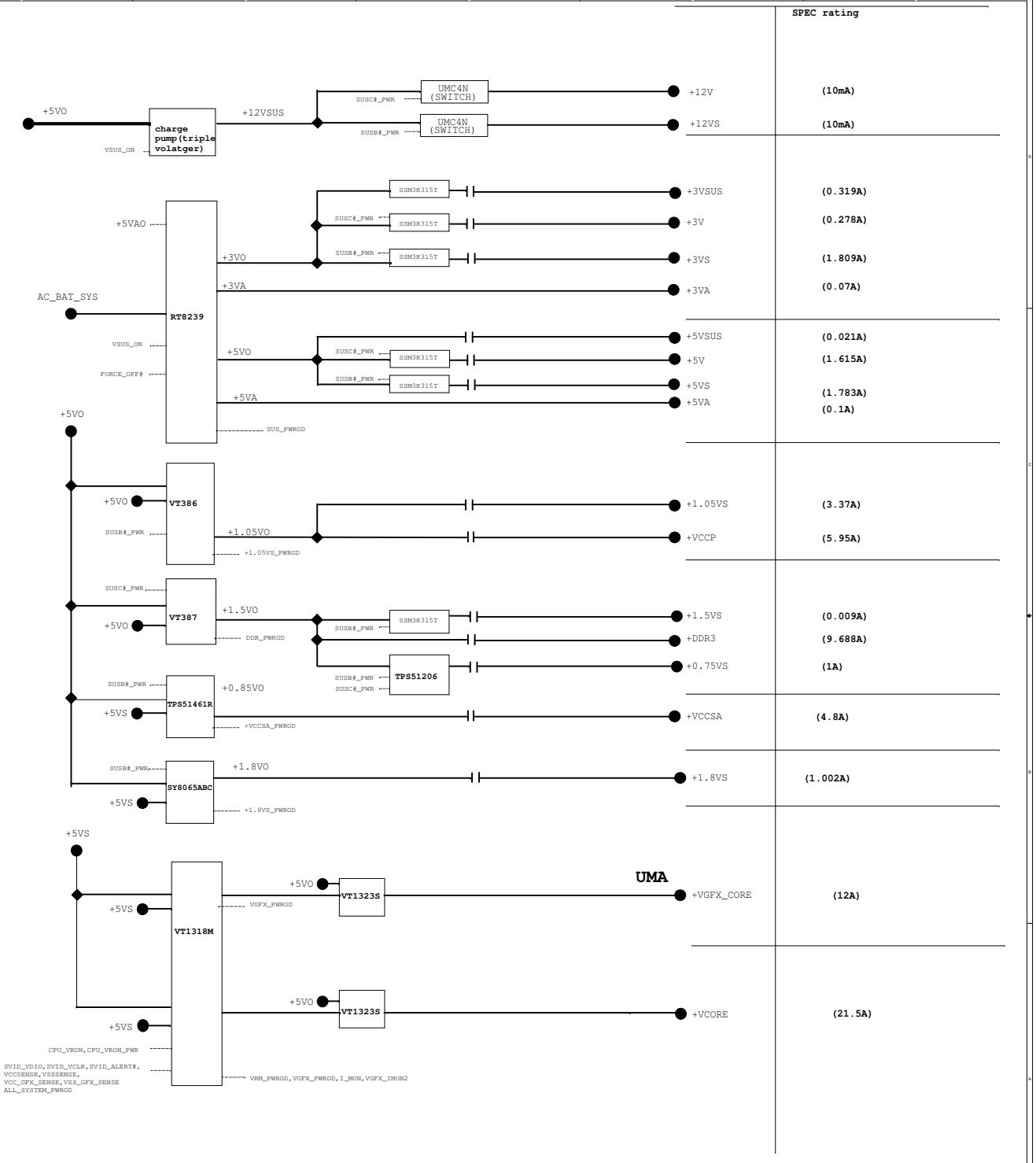
<Variant Name>

PEGATRON Title : POWER_SIGNAL

Engineer: Clark Liang

Size	Project Name	Rev
Custom	U14	1.0

Date: Wednesday, February 01, 2012 Sheet 93 of 94


SPEC rating
+5VO
charge pump(triple volatger)
VSUS_ON
+12VSUS
SUSC#_PWR
UMC4N (SWITCH)
SUSB#_PWR
UMC4N (SWITCH)
+12V
(10mA)
+12VS
(10mA)
+5VAO
AC_BAT_SYS
RT8239
VSUS_ON
FORCE_OFF#
+3VO
+3VA
+5VO
+5VA
SUS_PWRGD
SSM3K315T
+3VSUS
(0.319A)
+3V
(0.278A)
+3VS
(1.809A)
+3VA
(0.07A)
+5VSUS
(0.021A)
+5V
(1.615A)
+5VS
(1.783A)
+5VA
(0.1A)
VT386
+1.05VO
+1.05VS_PWRGD
+1.05VS
(3.37A)
+VCCP
(5.95A)
VT387
+1.5VO
DDR_PWRGD
+1.5VS
(0.009A)
+DDR3
(9.688A)
TPS51206
+0.75VS
(1A)
TPS51461R
+0.85VO
+VCCSA_PWRGD
+VCCSA
(4.8A)
SY8065ABC
+1.8VO
+1.8VS_PWRGD
+1.8VS
(1.002A)
VT1318M
VT1323S
VGFX_PWRGD
UMA
+VGFX_CORE
(12A)
VT1323S
+VCORE
(21.5A)
CPU_VRON,CPU_VRON_PWR
SVID_VDIO,SVID_VCLK,SVID_ALERT#,
VCCSENSE,VSSSENSE,
VCC_GFX_SENSE,VSS_GFX_SENSE
ALL_SYSTEM_PWRGD
VRM_PWRGD,VGFX_PWRGD,I_MON,VGFX_IMON2

modify notice R11 to R12

Version	Date	Description
	20120103	change SP604 to SP0605, SP605 to SP0606, JP3805 to SP3805, R2240 to SR2201 change SP5501,SP5502 to small size change SP2703~SP2708, SP2715 to small size Add R2208~R2212 P60 Add daul battery schematic P48 modify HPD schematic P22 modify SYS_PWRGD schematic change J4001,J4002 part change PCIE and SATA and USB2.0 and USB3.0 c
	20120105	change SP4001,SP4601,SP4602 to small size change SP2003,SP2005,SP2110,SP2114~SP2116,SP2209,SP2210,SP2212~SP2215 to small size change SP2304,SP2305,SP2401,SP2402,SP2501,SP2502,SP3002,SP3006 to small size change R5103 to 0805 modify P53 schematic
	20120109	add R4810~R4813 remove SP3101~SP3124
	20120110	add C0794
	20120111	add CN3101~CN3106
	20120112	add project ID R2530, R2533 add D5601,D5602,R2713,R2714
	20120113	add wifi LED R5609,R5616,R5617,T2517

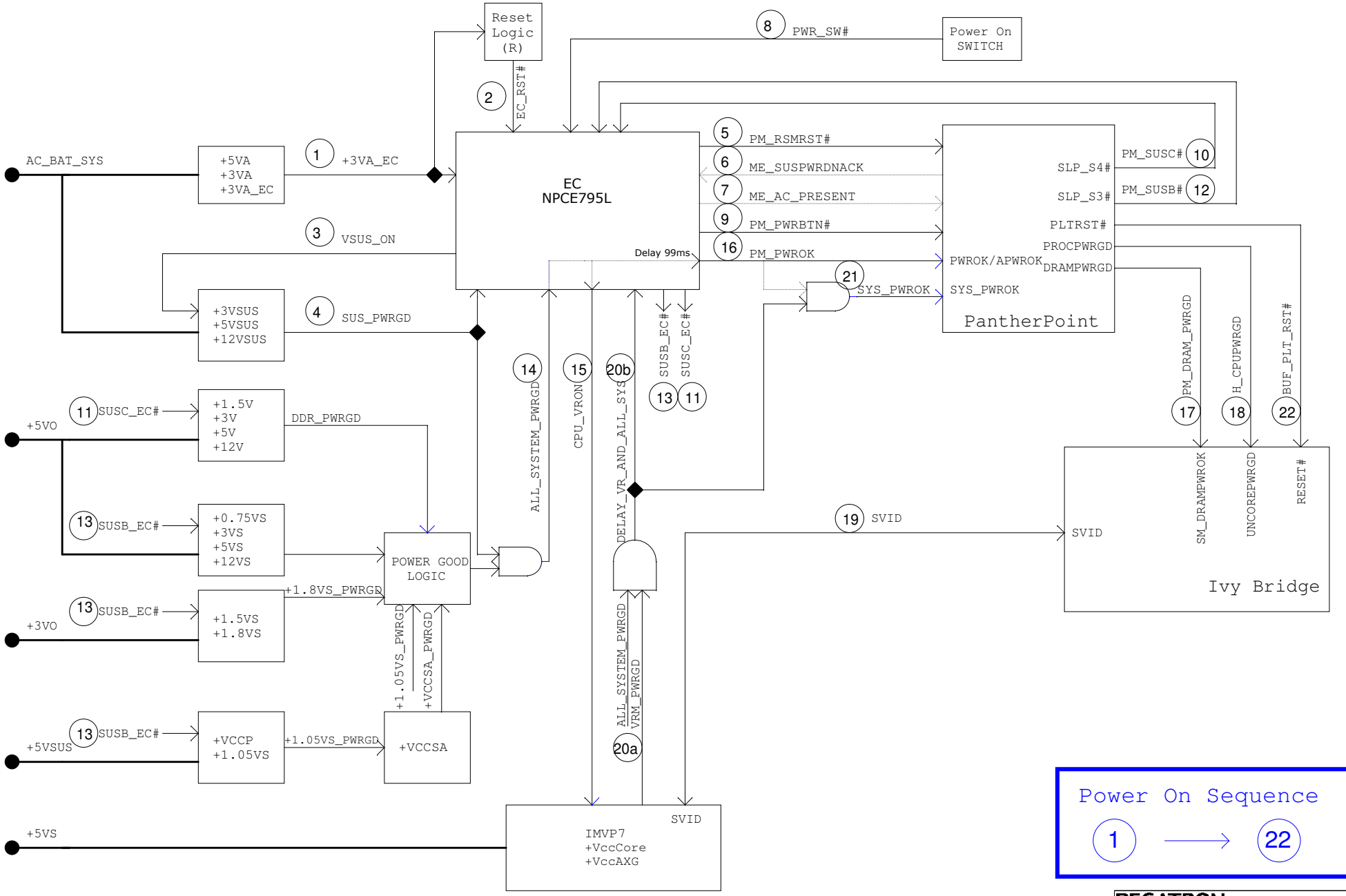
PEGATRON Title : SYSTEM History

<OrgName> Engineer: Trunks_Chen

Size	Project Name	Rev
Custom	B34	1.0

Date: Wednesday, February 01, 2012 Sheet 95 of 99

Power On Sequence Diagram G3-S0 R0.1 [Non-iAMT, Non-Deep Sx]

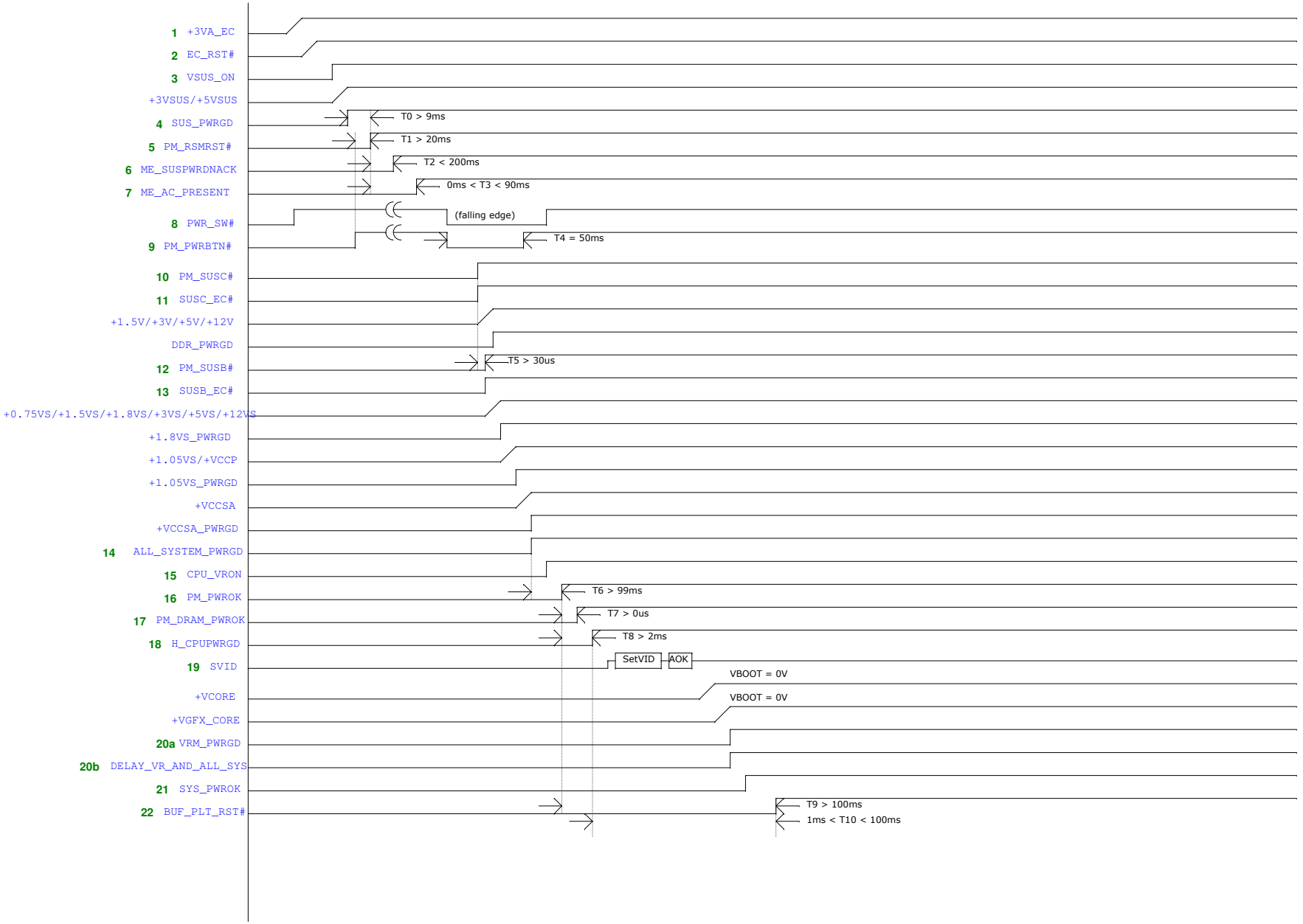


Power On Sequence

1 → 22

PEGATRON	Title : Power On Sequence	
BG1\HW1	Engineer: Penny1_Cheng	
Size: C	Project Name: B14Y	Rev: 1.2
Date: Wednesday, February 01, 2012	Sheet 98 of 99	

Power On Sequence Diagram G3-S0 R0.1 [Non-iAMT, Non-Deep Sx]



PEGATRON	Title : Power On Timing	
BG1\HW1	Engineer: Penny1_Cheng	
Size: C	Project Name: B14Y	Rev: 1.2
Date: Wednesday, February 01, 2012	Sheet 99 of 99	