MODEL NAME : VBW01
PROJECT CODE : ANRVBW0100
PCB NO : DA8000WL000 LA-9982P M/B
DA40001FO00 LS-9101P POWER BUTTON/B
DA40001FP00 LS-9102P USB/B
DA40001FQ00 LS-9103P TP BUTTON/B

Dell / Compal Confidential

Schematic Document

Intel Shark Bay ULT
OAK Mainstream2
UMA/DIS AMD Venus Pro

2013-05-29 Rev: 3.0

X76@ : 76 level
46@ : 46 level
@ : Nopop component
CONN@ : Connector component
XDP@ : XDP function
UMA@ : Only for UMA
DIS@ : Only for Discrete
VENUS@ : VENUS Pro,VENUS XT
VENUSXT@ : VENUS XT
VENUSPRO@ : VENUS Pro
@VENUS@ : VENUS nopop component
EMI@ : EMI parts
@EMI@ : Reserve EMI parts
ESD@ : ESD parts
RF@ : RF parts

BOM config
UMA : UMA@,EMI@,ESD@,RF@
DIS VENUS : VENUS@,VENUSPRO@,DIS@,EMI@,ESD@,RF

ZZZ R1@
PCB VBW01 LA9982P/LS9101P/LS9102P/LS9103P
DAZ0ZG00120

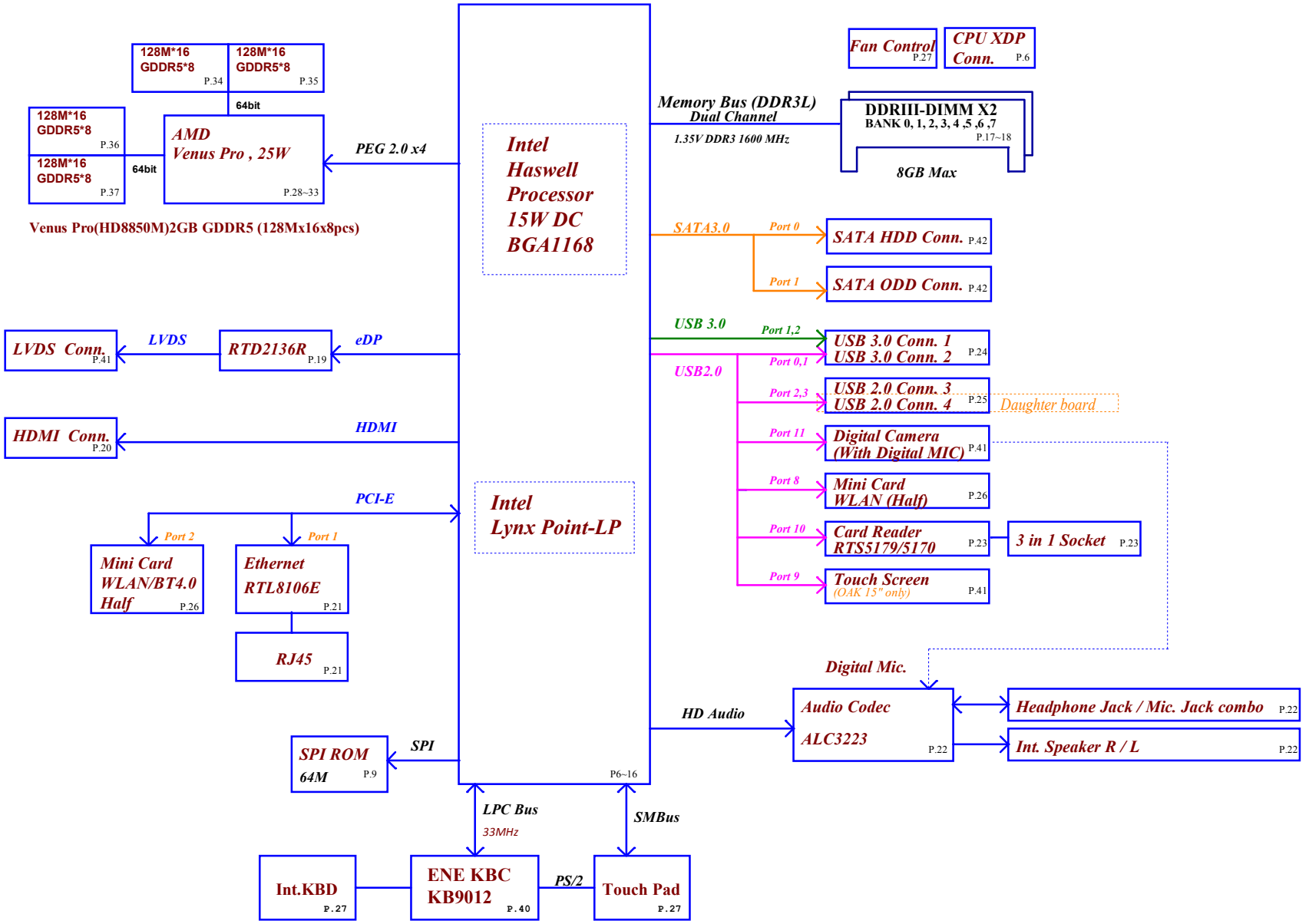
Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: Cover Page

Size	Document Number	Rev
Custom	LA-9982P	3.0

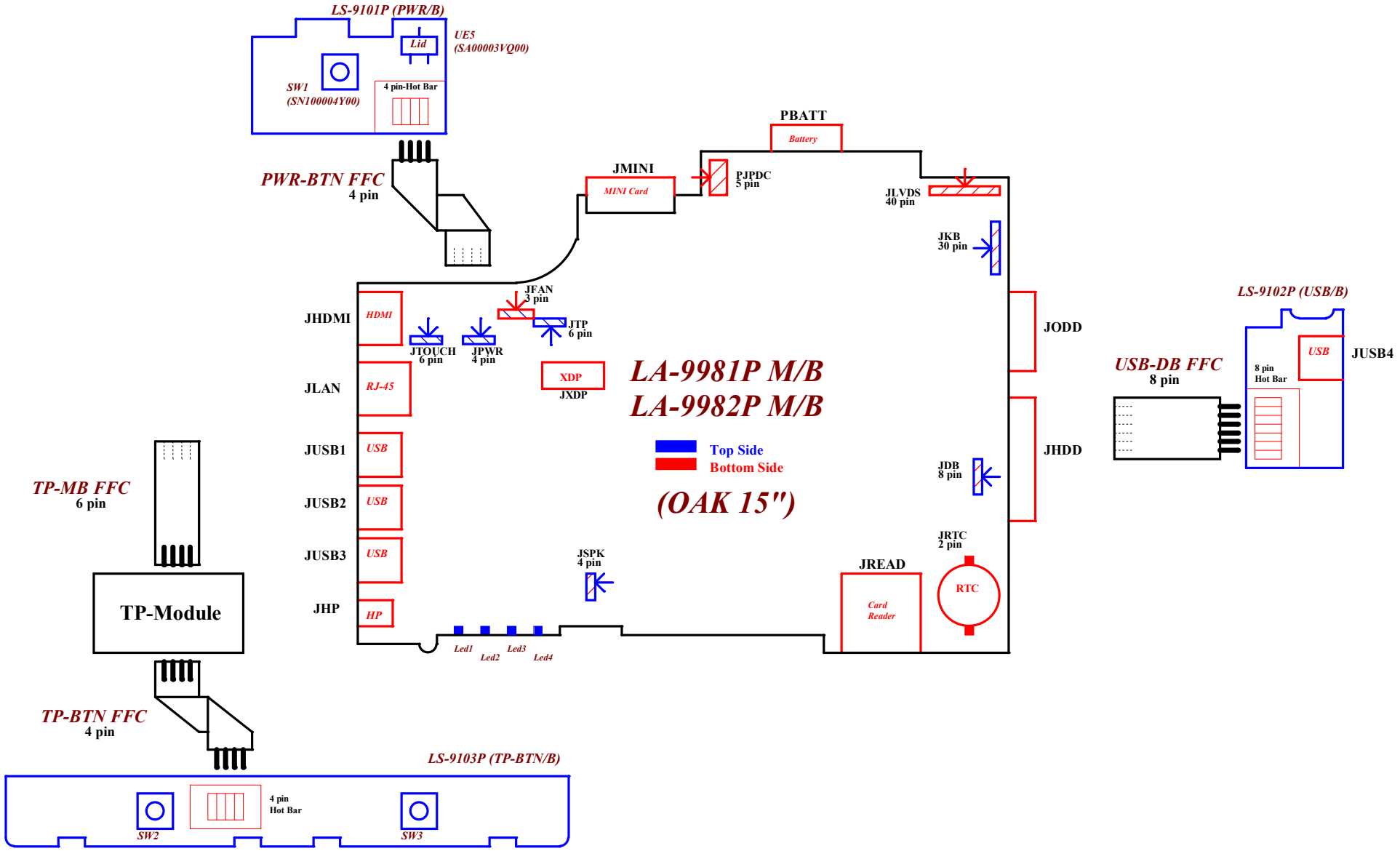
Date: Wednesday, May 29, 2013 Sheet 1 of 57



Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.			
Title: Block diagram			
Size	Document Number: LA-9982P		Rev: 3.0
Date: Wednesday, May 29, 2013	Sheet 2 of 57		

Compal Confidential
Project Code : VAW00 / VAW01
File Name : LA-9981P / LA-9982P



Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: DB block diagram

Size | Document Number: LA-9982P | Rev: 3.0

Date: Wednesday, May 29, 2013 | Sheet 3 of 57

Board ID Table for AD channel

Vcc	3.3V +/- 1%
Ra	100K +/- 1%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V	3.300V	0xE7 - 0xFF

SMBUS Control Table

	SOURCE	BATT	Charger	RTD2136S	VGA	DDR3L	XDP	WLAN mini card	Touch pad
EC_SMB_CK1 EC_SMB_DA1	KB9012	V	V						
EC_SMB_CK2 EC_SMB_DA2	KB9012			V	V				
SMBCLK SMBDATA	ULT					V	V	V	V
SML0CLK SML0DATA	ULT								
SML1CLK SML1DATA	ULT								

Link

Board ID TABLE

ID	PCB Revision			
	UMA	Sun XT	VenusPro	VenusXT
0	SSI&A02			
1		SSI&A02		
2			SSI&A02	
3				SSI&A02
4	PT			
5		PT		
6			PT	
7				PT
8	ST			
9		ST		
10			ST	
11				ST
12	XB			
13		XB		
14			XB	
15				XB
16	A01			
17		A01		
18			A01	
19				A01

Symbol Note :

: means Digital Ground

: means Analog Ground

CLOCK SIGNAL	
CLKOUT_PCIE0	
CLKOUT_PCIE1	
CLKOUT_PCIE2	10/100 LAN
CLKOUT_PCIE3	MINI Card (WLAN)
CLKOUT_PCIE4	dGPU
CLKOUT_PCIE5	

ULT	USB3.0	
	Port1	USB connector 2
	Port2	USB connector 1
	Port3	
	Port4	
	USB2.0	
	Port0	USB connector 2
	Port1	USB connector 1
	Port2	USB connector 3
	Port3	USB connector 4 (DB)
	Port4	MINI Card (WLAN)
	Port5	Touch Screen Panel
	Port6	Card Reader
	Port7	Camera
	PCI EXPRESS	
	Lane 1	
	Lane 2	
	Lane 3	10/100 LAN
	Lane 4	MINI Card (WLAN)
	Lane 5	PEG (N14P)
	Lane 6	PEG (N14P)
	SATA	
	SATA0	HDD
	SATA1	ODD
	SATA2	
	SATA3	

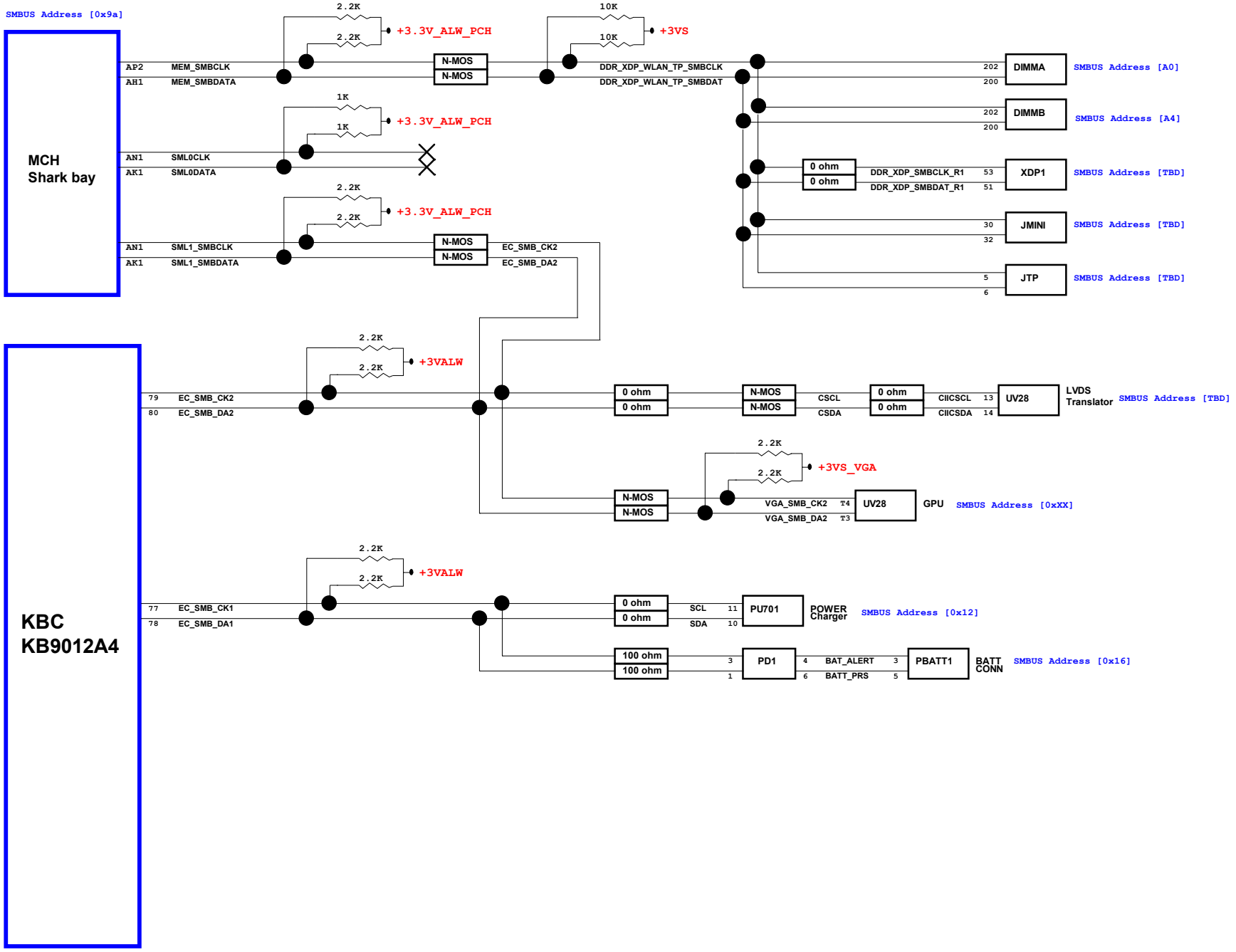
Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: Notes List

Size: | Document Number: LA-9982P | Rev: 3.0

Date: Wednesday, May 29, 2013 | Sheet 4 of 57



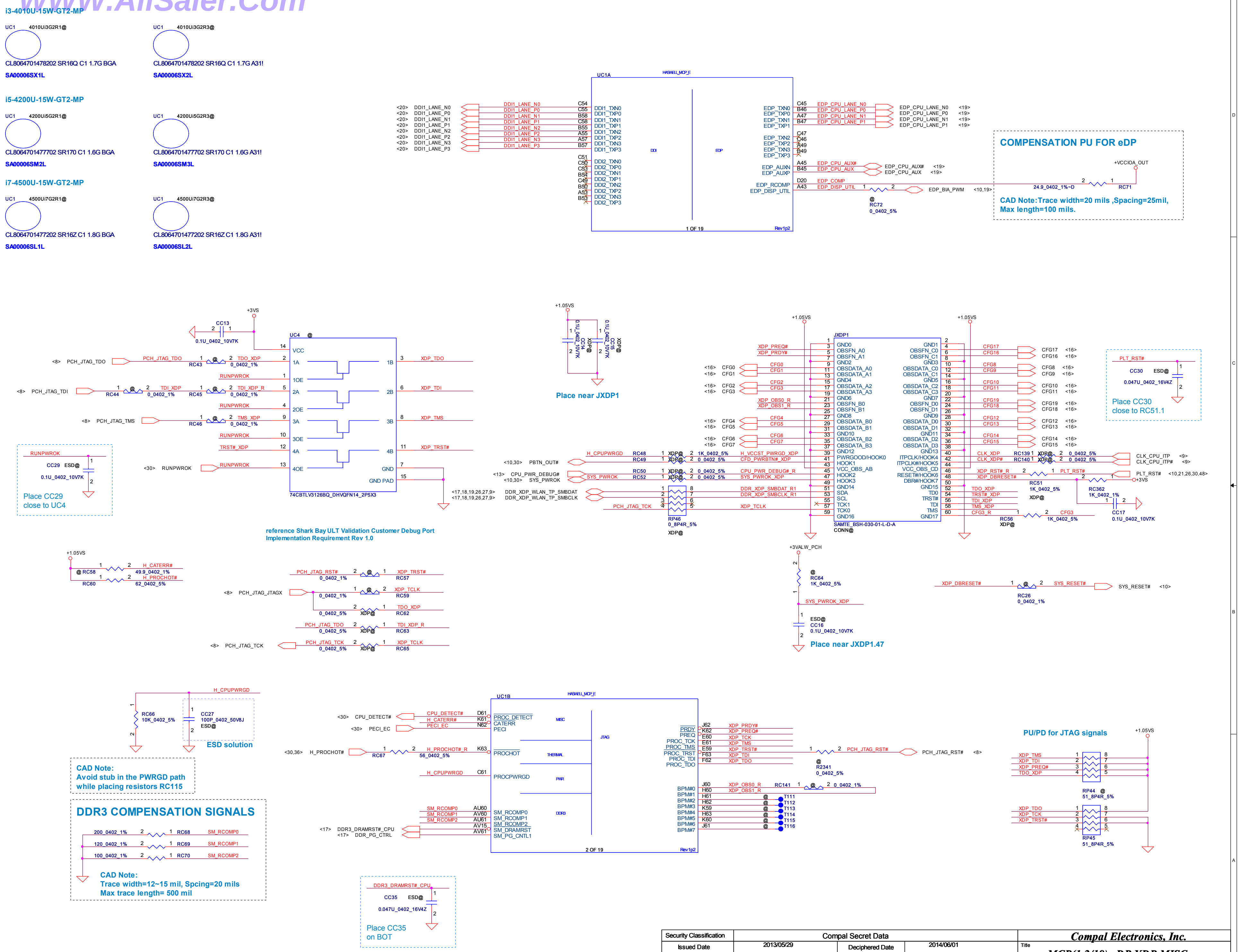
Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: SMBus block diagram

Size	Document Number	Rev
	LA-9982P	3.0

Date: Wednesday, May 29, 2013 Sheet 5 of 57

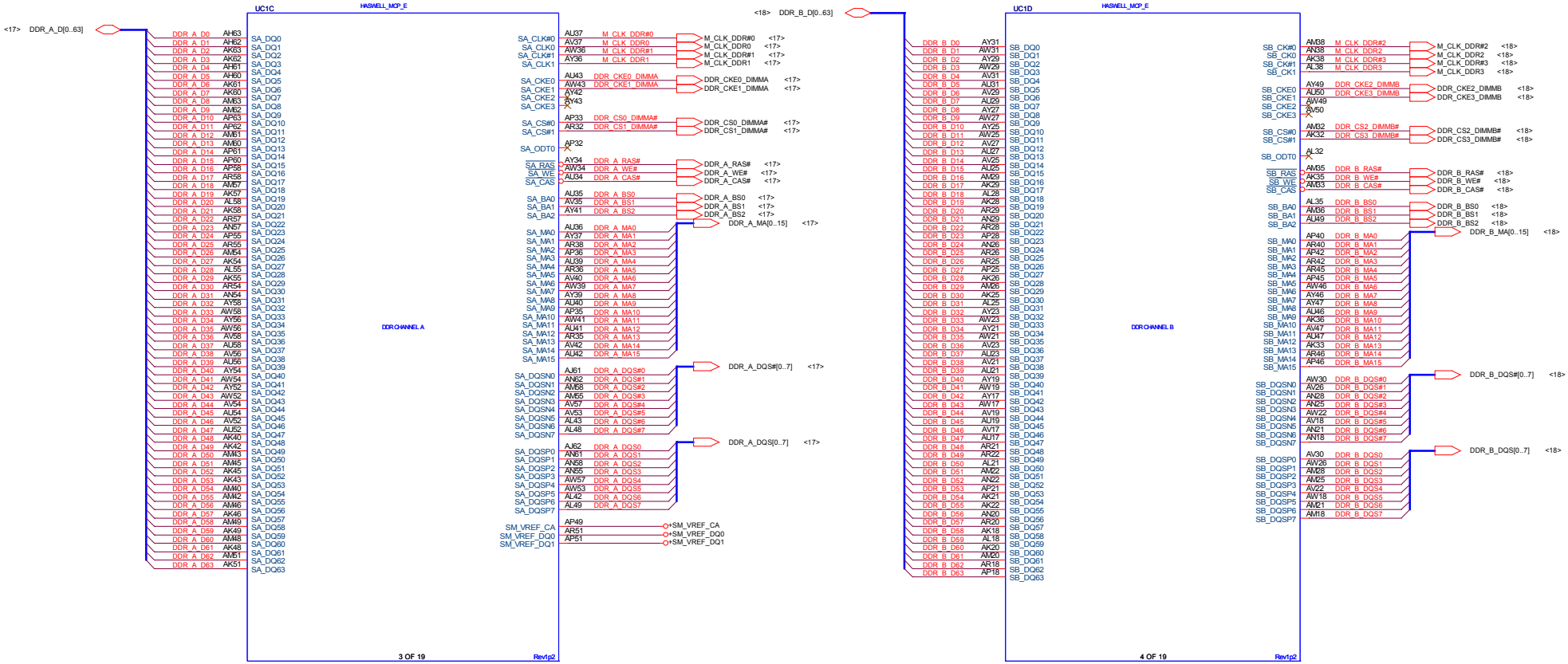


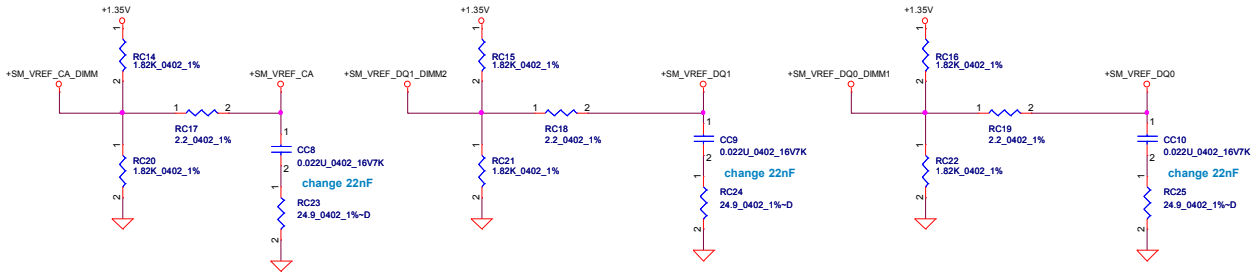
i3-4010U-15W-GT2-MP
UC1 4010Ui3G2R1@
CL8064701478202 SR16Q C1 1.7G BGA
SA00006SX1L
UC1 4010Ui3G2R3@
CL8064701478202 SR16Q C1 1.7G A31!
SA00006SX2L
i5-4200U-15W-GT2-MP
UC1 4200Ui5G2R1@
CL8064701477702 SR170 C1 1.6G BGA
SA00006SM2L
UC1 4200Ui5G2R3@
CL8064701477702 SR170 C1 1.6G A31!
SA00006SM3L
i7-4500U-15W-GT2-MP
UC1 4500Ui7G2R1@
CL8064701477202 SR16Z C1 1.8G BGA
SA00006SL1L
UC1 4500Ui7G2R3@
CL8064701477202 SR16Z C1 1.8G A31!
SA00006SL2L
UC1A
HASWELL_MCP_E
DDI1_LANE_N0
DDI1_LANE_P0
DDI1_LANE_N1
DDI1_LANE_P1
DDI1_LANE_N2
DDI1_LANE_P2
DDI1_LANE_N3
DDI1_LANE_P3
DDI1_TXN0
DDI1_TXP0
DDI1_TXN1
DDI1_TXP1
DDI1_TXN2
DDI1_TXP2
DDI1_TXN3
DDI1_TXP3
DDI2_TXN0
DDI2_TXP0
DDI2_TXN1
DDI2_TXP1
DDI2_TXN2
DDI2_TXP2
DDI2_TXN3
DDI2_TXP3
EDP_TXN0
EDP_TXP0
EDP_TXN1
EDP_TXP1
EDP_TXN2
EDP_TXP2
EDP_TXN3
EDP_TXP3
EDP_AUXN
EDP_AUXP
EDP_RCOMP
EDP_DISP_UTIL
EDP_CPU_LANE_N0
EDP_CPU_LANE_P0
EDP_CPU_LANE_N1
EDP_CPU_LANE_P1
EDP_CPU_AUX#
EDP_CPU_AUX
EDP_COMP
EDP_BIA_PWM
RC72
0_0402_5%
1 OF 19
Rev1p2
COMPENSATION PU FOR eDP
+VCCIOA_OUT
24.9_0402_1%~D
RC71
CAD Note:Trace width=20 mils ,Spacing=25mil, Max length=100 mils.
+3VS
CC13
0.1U_0402_10V7K
UC4
PCH_JTAG_TDO
PCH_JTAG_TDI
PCH_JTAG_TMS
RUNPWROK
TDO_XDP
TDI_XDP
TDI_XDP_R
TMS_XDP
TRST#_XDP
XDP_TDO
XDP_TDI
XDP_TMS
XDP_TRST#
RC43
RC44
RC45
RC46
0_0402_1%
74CBTLV3126BQ_DHVQFN14_2P5X3
CC29 ESD@
0.1U_0402_10V7K
Place CC29 close to UC4
reference Shark Bay ULT Validation Customer Debug Port Implementation Requirement Rev 1.0
+1.05VS
CC14
CC15
0.1U_0402_10V7K
XDP@
Place near JXDP1
JXDP1
SAMTE_BSH-030-01-L-D-A
CONN@
XDP_PREQ#
XDP_PRDY#
CFG0
CFG1
CFG2
CFG3
CFG4
CFG5
CFG6
CFG7
CFG8
CFG9
CFG10
CFG11
CFG12
CFG13
CFG14
CFG15
CFG16
CFG17
CFG18
CFG19
XDP_OBS0_R
XDP_OBS1_R
H_CPUPWRGD
H_VCCST_PWRGD_XDP
CFD_PWRBTN#_XDP
PBTN_OUT#
CPU_PWR_DEBUG#
CPU_PWR_DEBUG#_R
SYS_PWROK
SYS_PWROK_XDP
DDR_XDP_WLAN_TP_SMBDAT
DDR_XDP_WLAN_TP_SMBCLK
DDR_XDP_SMBDAT_R1
DDR_XDP_SMBCLK_R1
PCH_JTAG_TCK
XDP_TCLK
RC48
RC49
RC50
RC52
1K_0402_5%
0_0402_5%
RP46
0_8P4R_5%
CLK_XDP
CLK_XDP#
CLK_CPU_ITP
CLK_CPU_ITP#
RC139
RC140
XDP_RST#_R
XDP_DBRESET#
PLT_RST#
RC51
1K_0402_5%
RC362
1K_0402_1%
CC17
0.1U_0402_10V7K
RC56
CFG3_R
PLT_RST#
CC30 ESD@
0.047U_0402_16V4Z
Place CC30 close to RC51.1
+1.05VS
RC58
RC60
H_CATERR#
49.9_0402_1%
H_PROCHOT#
62_0402_5%
PCH_JTAG_RST#
XDP_TRST#
RC57
PCH_JTAG_TAGX
XDP_TCLK
RC59
TDO_XDP
RC62
RC63
PCH_JTAG_TDO
PCH_JTAG_TCK
RC65
+3VALW_PCH
RC64
1K_0402_5%
SYS_PWROK_XDP
CC16
0.1U_0402_10V7K
Place near JXDP1.47
XDP_DBRESET#
RC26
0_0402_1%
SYS_RESET#
H_CPUPWRGD
RC66
10K_0402_5%
CC27
100P_0402_50V8J
ESD@
ESD solution
CAD Note: Avoid stub in the PWRGD path while placing resistors RC115
DDR3 COMPENSATION SIGNALS
200_0402_1% RC68 SM_RCOMP0
120_0402_1% RC69 SM_RCOMP1
100_0402_1% RC70 SM_RCOMP2
CAD Note: Trace width=12~15 mil, Spcing=20 mils Max trace length= 500 mil
UC1B
HASWELL_MCP_E
CPU_DETECT#
PECI_EC
H_PROCHOT#
RC67
56_0402_5%
PROC_DETECT
CATERR
PECI
PROCHOT
PROCPWRGD
SM_RCOMP0
SM_RCOMP1
SM_RCOMP2
SM_DRAMRST
SM_PG_CNTL1
DDR3_DRAMRST#_CPU
DDR_PG_CTRL
PRDY
PREQ
PROC_TCK
PROC_TMS
PROC_TRST
PROC_TDI
PROC_TDO
BPM#0
BPM#1
BPM#2
BPM#3
BPM#4
BPM#5
BPM#6
BPM#7
XDP_PRDY#
XDP_PREQ#
XDP_TCK
XDP_TMS
XDP_TRST#
XDP_TDI
XDP_TDO
R2341
0_0402_5%
XDP_OBS0_R
XDP_OBS1_R
RC141
T111
T112
T113
T114
T115
T116
2 OF 19
Rev1p2
DDR3_DRAMRST#_CPU
CC35 ESD@
0.047U_0402_16V4Z
Place CC35 on BOT
PU/PD for JTAG signals
+1.05VS
RP44
51_8P4R_5%
RP45
51_8P4R_5%

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/05/29	Deciphered Date 2014/06/01	Title: MCP(1,2/19) eDP,XDP,MISC

Size | Document Number: LA-9982P | Rev 3.0

Date: Wednesday, May 29, 2013 | Sheet 6 of 57





confirm by intel request PDG P141

Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: MCP(3.4/19) DDR3

Size: | Document Number: LA-9982P | Rev: 3.0

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RTC Battery

+RTCBATT
+CHGRTC
RC10 1K_0402_5%
W=20mils
W=20mils
DC1 BAT54CW_SOT323-3
+RTCVCC
W=20mils
CC26 1U_0603_10V6K

JP12 JUMP_43X39
+CHGRTC — +3VLP

For GCLK
<29> PCH_RTCX1 — PCH_RTCX1

+RTCVCC
RC1 330K_0402_1%
PCH_INTVRMEN
RC2 330K_0402_1%

INTVRMEN - INTEGRATED SUS 1.05V VRM ENABLE
High - Enable Internal VRs
Low - Enable External VRs

+3VS
@ RC3 PCH_AZ_SDOUT 1K_0402_5%

FLASH DESCRIPTOR SECURITY OVERRIDE
LOW = DESABLED (DEFAULT)
HIGH = ENABLED

CC1 15P_0402_50V8J XTAL@
XTAL@ YC1 32.768KHZ_12.5PF_Q13FC1350000
XTAL@ RC4 10M_0402_5%
CC2 XTAL@ 15P_0402_50V8J
PCH_RTCX1
PCH_RTCX2
INTRUDER#
PCH_INTVRMEN
SRTCRST#
PCH_RTCRST#
+RTCVCC
RC7 1M_0402_5%
RC5 20K_0402_5%
RC6 20K_0402_5%

@ ME1 SHORT PADS~D CC3 1U_0402_6.3V6K
@ CMOS1 SHORT PADS~D CC4 1U_0402_6.3V6K

CMOS place near DIMM

UC1E HASWELL_MCP_E

RTC: RTCX1, RTCX2, INTRUDER, INTVRMEN, SRTCRST, RTCRST

AUDIO:
PCH_AZ_BITCLK — HDA_BCLK/I2S0_SCLK
PCH_AZ_SYNC — HDA_SYNC/I2S0_SFRM
PCH_AZ_RST# — HDA_RST/I2S_MCLK
PCH_AZ_CODEC_SDIN0 — HDA_SDI0/I2S0_RXD
<22> PCH_AZ_CODEC_SDIN0
<30> ME_EN — RC8 1K_0402_5% — PCH_AZ_SDOUT — HDA_SDO/I2S0_TXD
HDA_DOCK_EN/I2S1_TXD
HDA_DOCK_RST/I2S1_SFRM
I2S1_SCLK

JTAG:
<6> PCH_JTAG_RST# — PCH_JTAG_RST# — PCH_TRST
<6> PCH_JTAG_TCK — PCH_JTAG_TCK — PCH_TCK
<6> PCH_JTAG_TDI — PCH_JTAG_TDI — PCH_TDI
<6> PCH_JTAG_TDO — PCH_JTAG_TDO — PCH_TDO
<6> PCH_JTAG_TMS — PCH_JTAG_TMS — PCH_TMS
RSVD
RSVD
<6> PCH_JTAG_JTAGX — PCH_JTAG_JTAGX — JTAGX
RSVD

SATA:
SATA_RN0/PERN6_L3 — SATA_PRX_DTX_N0_C <32>
SATA_RP0/PERP6_L3 — SATA_PRX_DTX_P0_C <32>
SATA_TN0/PETN6_L3 — SATA_PTX_DRX_N0_C <32>
SATA_TP0/PETP6_L3 — SATA_PTX_DRX_P0_C <32>
SATA HDD
SATA_RN1/PERN6_L2 — SATA_PRX_DTX_N1_C <32>
SATA_RP1/PERP6_L2 — SATA_PRX_DTX_P1_C <32>
SATA_TN1/PETN6_L2 — SATA_PTX_DRX_N1_C <32>
SATA_TP1/PETP6_L2 — SATA_PTX_DRX_P1_C <32>
SATA ODD
SATA_RN2/PERN6_L1
SATA_RP2/PERP6_L1
SATA_TN2/PETN6_L1
SATA_TP2/PETP6_L1
SATA_RN3/PERN6_L0
SATA_RP3/PERP6_L0
SATA_TN3/PETN6_L0
SATA_TP3/PETP6_L0
PCH Rx side need use strap pin to update PCIE +/-

+3VS
RC107 10K_0402_5%
SATA0GP/GPIO34 — EC_SMI# — EC_SMI# <30>
SATA1GP/GPIO35 — ODD_DETECT# — ODD_DETECT# <32>
SATA2GP/GPIO36 — PCH_GPIO37
SATA3GP/GPIO37

SATA_IREF — SATA_IREF — RC126 1 @ 2 0_0603_1%
RSVD
RSVD
SATA_RCOMP — SATA_RCOMP — RC131 1 2 3.01K_0402_1%
SATALED — SATA_ACT# — SATA_ACT# <26>
+1.05VS_ASATA3PLL
within 500 mils

SATA Impedance Compensation
CAD note:
Place the resistor within 500 mils of the PCH. Avoid routing next to clock pins.
reference FFRD sch 0.5

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Rev1p2

+1.05VS
@ RC130 PCH_JTAG_JTAGX 1K_0402_1%
@ RC135 PCH_JTAG_TCK 51_0402_1%

+1.05VS
RP48 51_8P4R_5%
PCH_JTAG_TDI
PCH_JTAG_TDO
PCH_JTAG_TMS

CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

HDA for Codec

<22> PCH_AZ_CODEC_SDOUT — EMI@ R2356 33_0402_5% — PCH_AZ_SDOUT
<22> PCH_AZ_CODEC_SYNC — EMI@ R2357 33_0402_5% — PCH_AZ_SYNC
<22> PCH_AZ_CODEC_RST# — EMI@ R2358 33_0402_5% — PCH_AZ_RST#
<22> PCH_AZ_CODEC_BITCLK — EMI@ R2359 33_0402_5% — PCH_AZ_BITCLK
@EMI@ CC5 27P_0402_50V8J

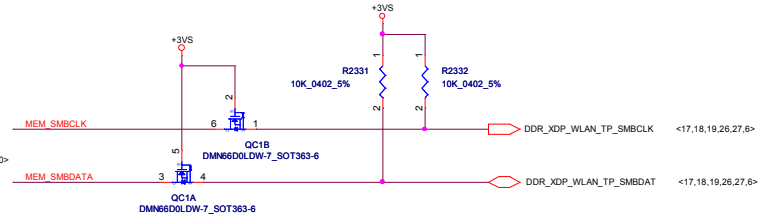
EMI depop location

+3VS
ODD_DETECT#
PCH_GPIO35
PCH_GPIO37
RP37 10K_8P4R_5%

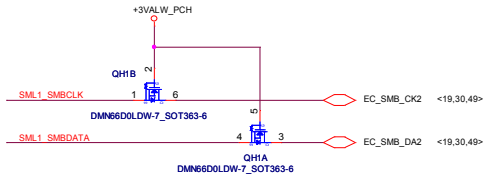
Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.
Title: MCP(5/19) RTC,SATA,HDA,JTAG
Size: — Document Number: LA-9982P — Rev: 3.0
Date: Wednesday, May 29, 2013 — Sheet 8 of 57

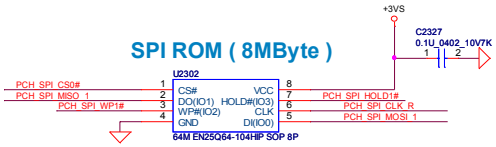
MEM Bus : DDR/XDP/WLAN/TP



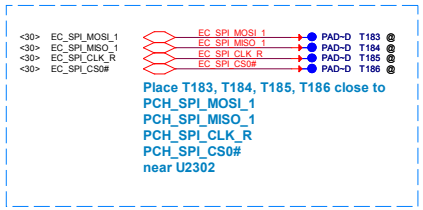
SML1 Bus : EC/Sensors

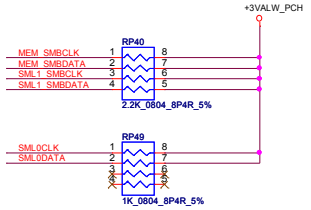


SPI ROM (8MByte)

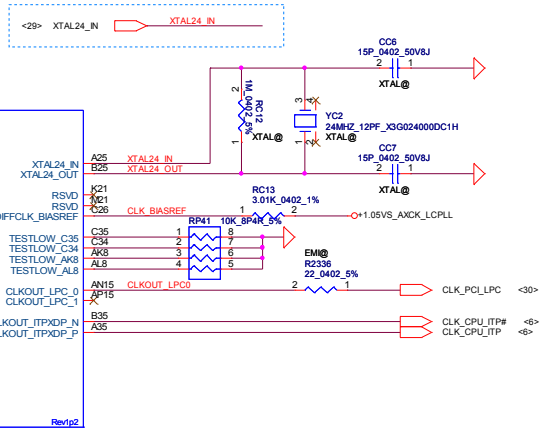


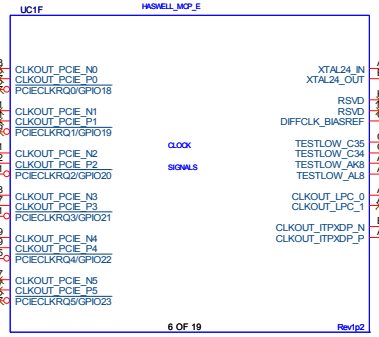
PN : SA000046400 ,64M,EN25Q64-104HIP

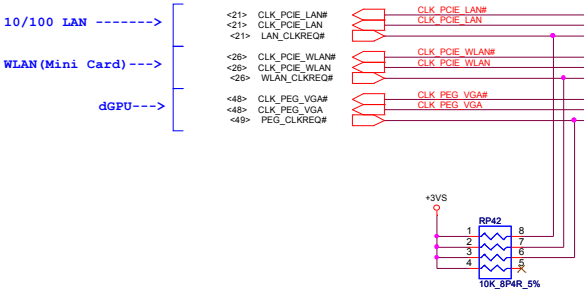


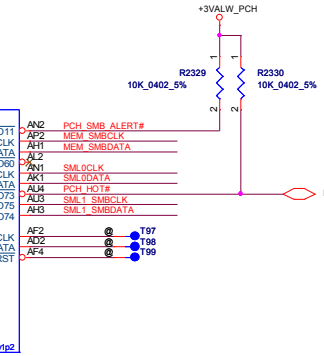


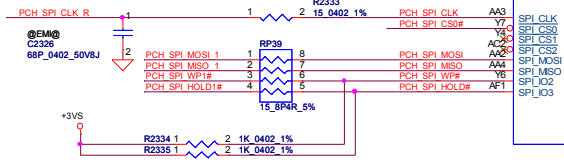
For GCLK











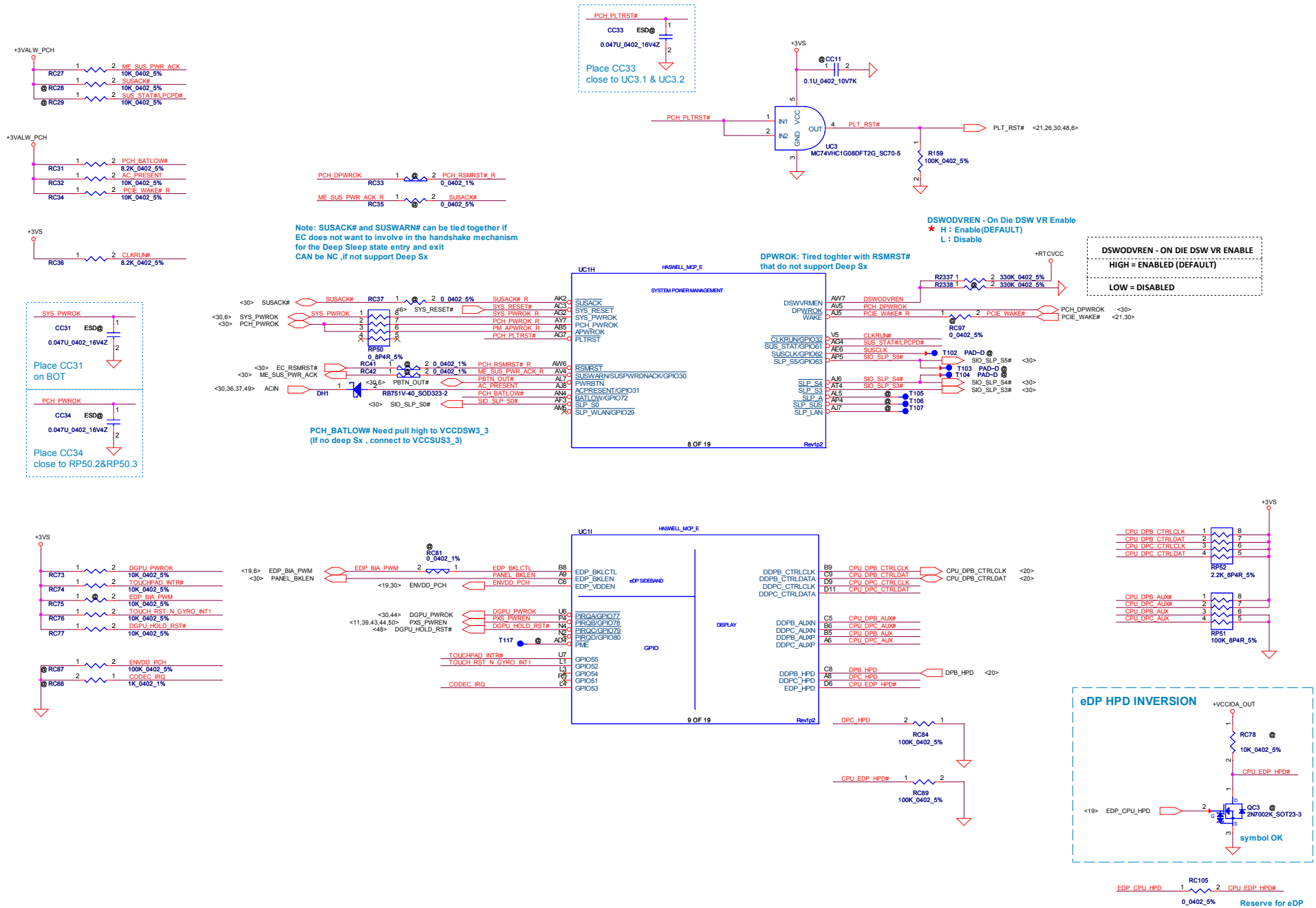
Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: MCP(6,7/19) CLK,SMB,SPI,LPC

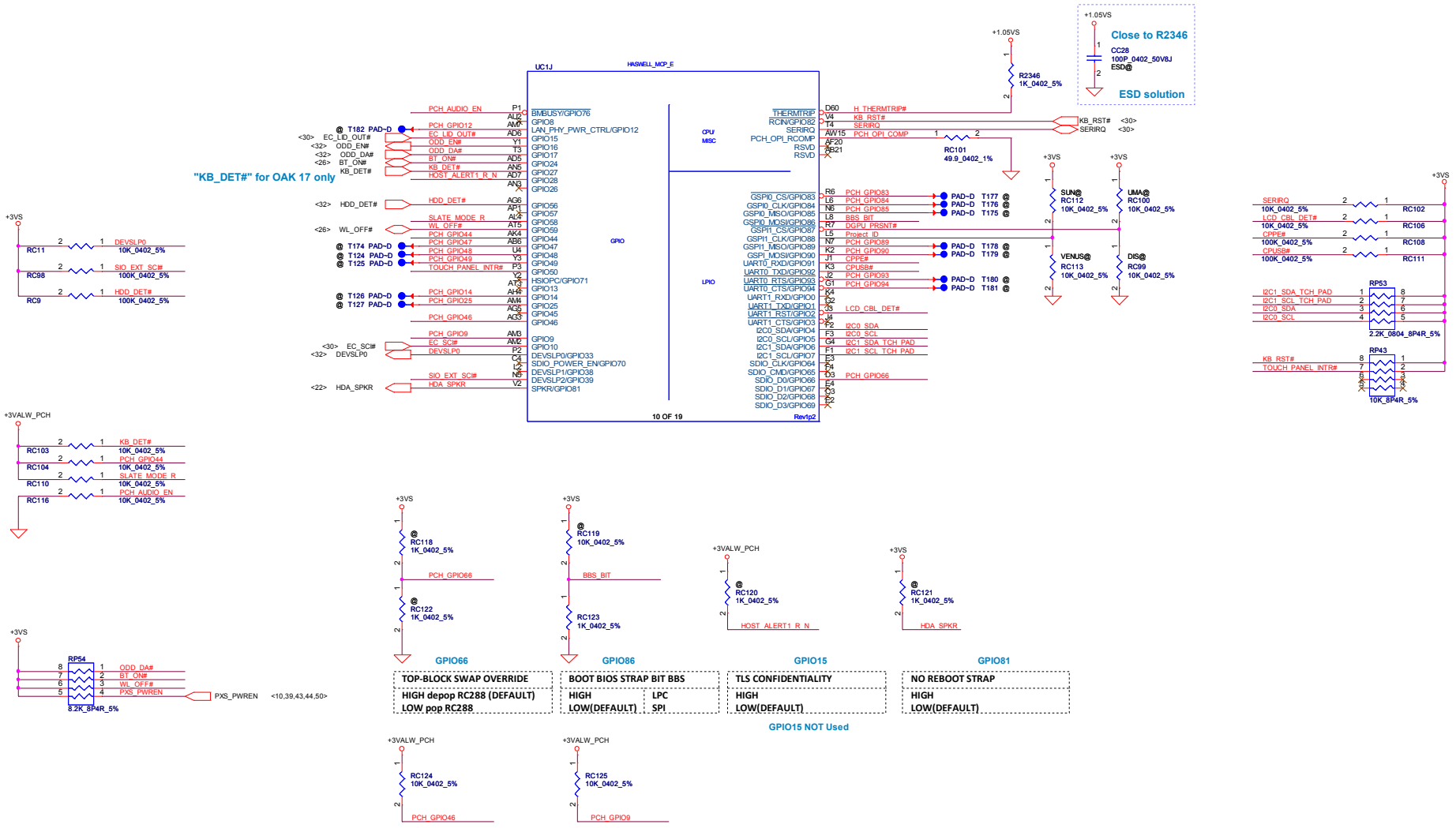
Size: | Document Number: LA-9982P | Rev: 3.0

Date: Wednesday, May 29, 2013 | Sheet 9 of 57



Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.			
Title: MCP(8,9/19) DDI,EDP,GPIO			
Size	Document Number: LA-9982P		Rev: 3.0
Date: Wednesday, May 29, 2013	Sheet 10 of 57		



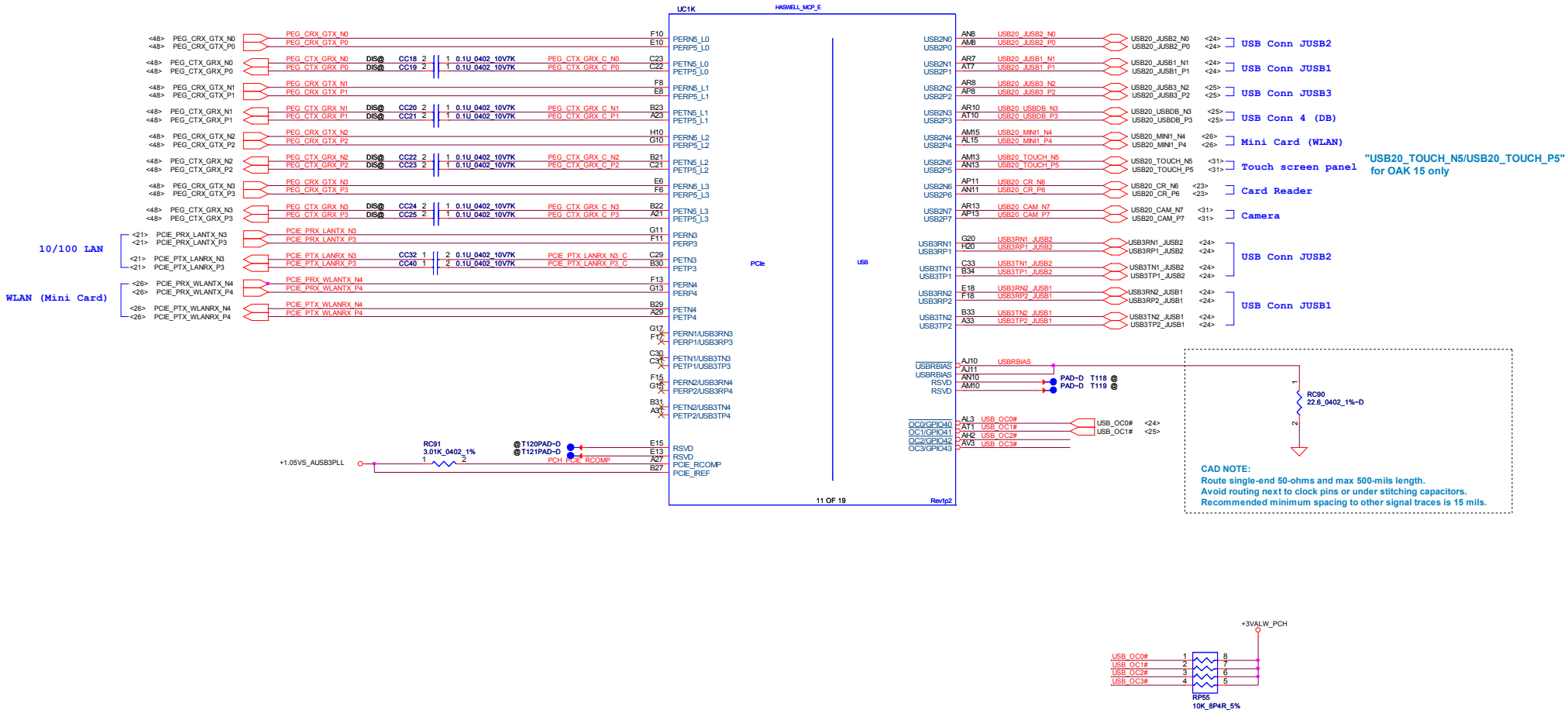
Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: MCP(10/19) GPIO,LPIO,MISC

Size	Document Number	Rev
	LA-9982P	3.0

Date: Wednesday, May 29, 2013 Sheet 11 of 57



Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: MCP(11/19) PCIE,USB

Size: | Document Number: LA-9982P | Rev: 3.0

Date: Wednesday, May 29, 2013 | Sheet 12 of 57

VCCST_PG_EC
C79 ESD@
220P_0402_50V8J
Place C79 between R286 and UC1
+1.05VS
R286 10K_0402_5%
<30> VCCST_PG_EC
VCCST_PG_EC
Define EC OD pin, need double confirm.

+CPU_CORE
+1.35V
C40
22U_0603_6.3V6M ESD@
ESD solution

SVID ALERT
+1.05VS
R252 75_0402_5%
Place the PU resistors close to CPU
R254 43_0402_1%
<42> VR_SVID_ALRT#
H_CPU_SVIDALRT#

SVID DATA
SVID_DAT need to pull-up double side (PWR_VR & CPU)
+1.05VS
Place the PU resistors close to CPU
R256 130_0402_1%
@ R257 0_0402_1%
<42> VR_SVID_DAT
H_CPU_SVIDDATA

VR_ON
C80 ESD@
0.1U_0402_10V7K
Place C80 close to R250.1

UC1L
HASWELL_MCP_E
+1.35V
+CPU_CORE
+VCCIO_OUT
+VCCIOA_OUT
R245 @ 0_0603_5%
VCCSENSE
+VCCIO_OUT_R
T38 @
12 OF 19
HSW ULT POWER
<42> VR_SVID_CLK
0_0402_1% R248
H_CPU_SVIDALRT#
H_CPU_SVIDCLK
H_CPU_SVIDDATA
VCCST_PG_EC
<30,42> VR_ON
<42> H_VR_READY
0_0402_5% R250
0_0402_1% R251
VR12.5_VR_ON_R
VR_READY_R
<6> CPU_PWR_DEBUG#
CPU_PWR_DEBUG#
RF
RF@ C5212 68P_0402_50V8J
H_CPU_SVIDCLK
+1.05VS
+CPU_CORE
Rev1p2

+1.05VS
@ R253 150_0402_1%
R253
INTEL Check list , XDP use only
CPU_PWR_DEBUG#
@ R255 10K_0402_5%

+CPU_CORE
R1 100_0402_1%
<42> VCCSENSE
VCCSENSE
CAD Note: PU resistor on HW side
<15,42> VSSSENSE
VSSSENSE
CAD Note: PD resistor on HW side
R2 100_0402_1%

+1.35V
VDDQ DECOUPLING
C35 2.2U_0402_6.3V6M
C36 2.2U_0402_6.3V6M
C37 2.2U_0402_6.3V6M
C38 2.2U_0402_6.3V6M
C39 10U_0603_6.3V6M
C41 10U_0603_6.3V6M
C72 10U_0603_6.3V6M
C42 10U_0603_6.3V6M
C45 10U_0603_6.3V6M
C74 10U_0603_6.3V6M
+1.35V : 470UF/2V/7343 *2 (PWR)
10UF/6.3V/0603 * 6
2.2UF/6.3V/0402 * 4

Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.
Title: MCP(12/19) Power
Size: Document Number: LA-9982P
Rev: 3.0
Date: Wednesday, May 29, 2013
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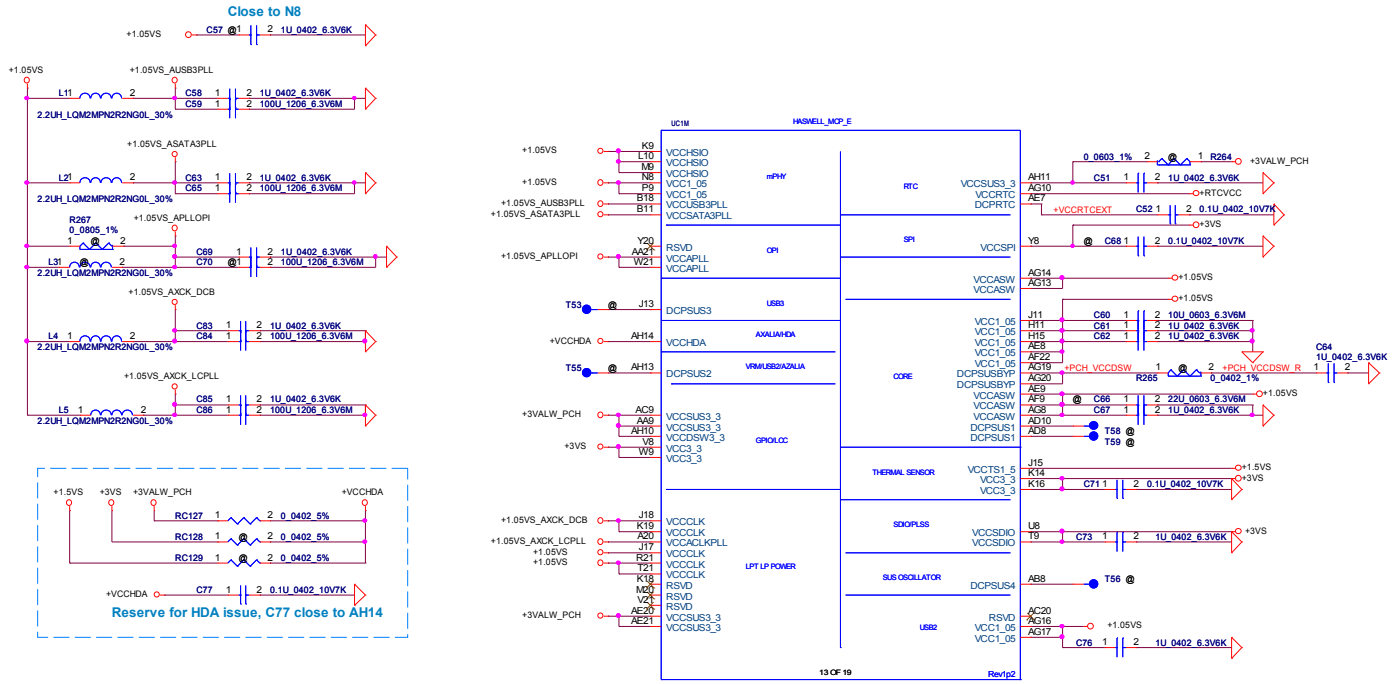
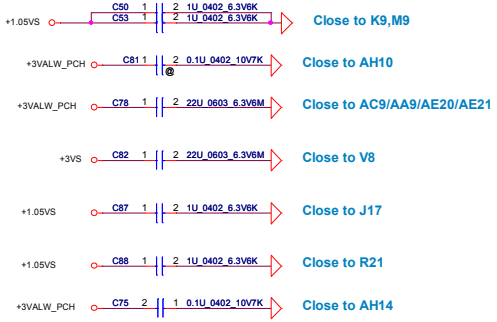




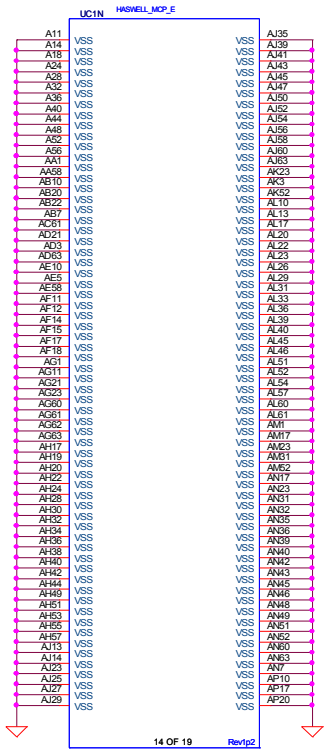
Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

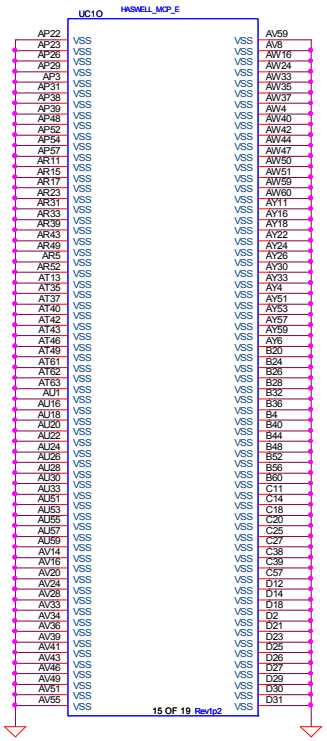
Compal Electronics, Inc.

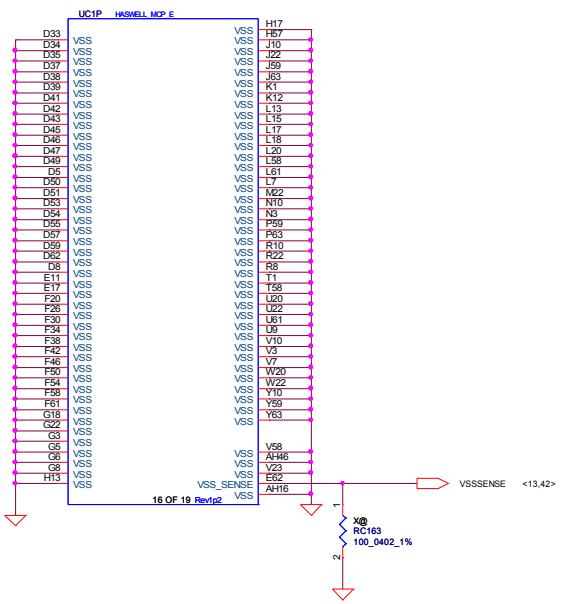
Title: MCP(13/19) Power

Size: | Document Number: LA-9982P | Rev: 3.0

Date: Wednesday, May 29, 2013 | Sheet 14 of 57







CAD Note: RC163 SHOULD BE PLACED CLOSE TO CPU

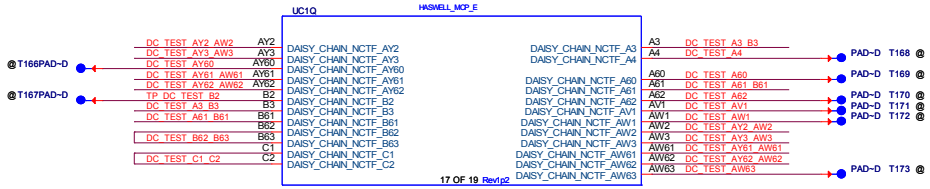
Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

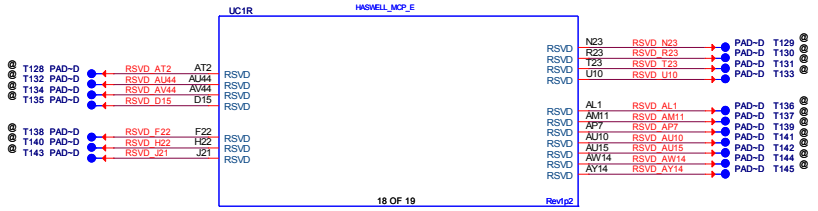
Compal Electronics, Inc.

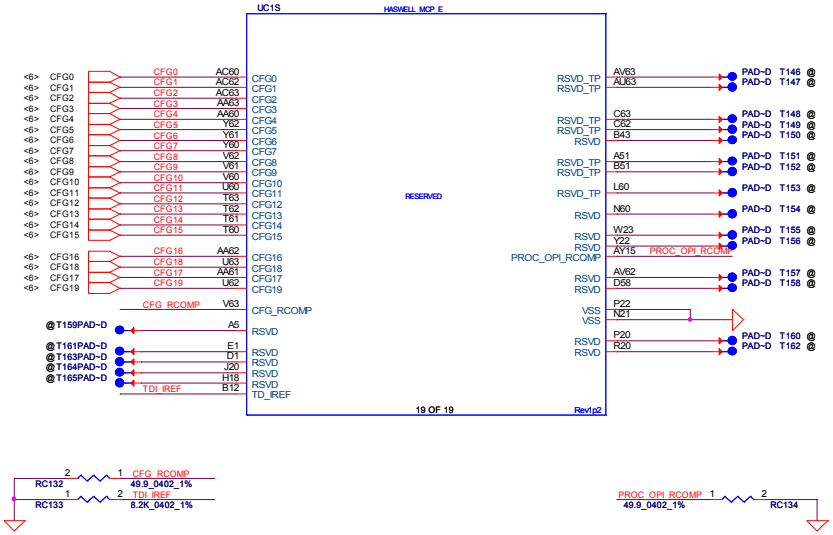
Title: MCP(14,15,16/19) VSS

Size	Document Number	Rev
	LA-9982P	3.0

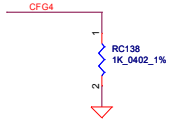
Date: Wednesday, May 29, 2013 Sheet 15 of 57







CFG STRAPS for CPU



Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: MCP(17,18,19/19) CFG,RSVD

Size: | Document Number: LA-9982P | Rev: 3.0

Date: Wednesday, May 29, 2013 | Sheet 16 of 57

H=4mm

2-3A to 1 DIMMs/channel

Populate RD1, De-Populate RD7 for Intel DDR3 VREFDQ multiple methods M1
Populate RD7, De-Populate RD1 for Intel DDR3 VREFDQ multiple methods M3

+DIMM1_VREF_DQ
+SM_VREF_DQ0_DIMM1
@ RD1 0_0402_1%
CD1 2.2U_0402_6.3V6M
CD2 0.1U_0402_10V7K

JDIMM1 CONN@

<7> DDR_A_DQS#[0..7]
<7> DDR_A_D[0..63]
<7> DDR_A_DQS[0..7]
<7> DDR_A_MA[0..15]

All VREF traces should have 10 mil trace width

Layout Note: Place near JDIMM1

Note: Check voltage tolerance of VREF_DQ at the DIMM socket

CD4 CD5 CD6 CD7 CD8 CD9 CD10 CD11 1U_0402_6.3V6K

CD12 CD13 CD14 CD15 CD16 CD17 CD18 CD19 CD20 CD21 10U_0603_6.3V6M
330U_D2_2V_R9M

Layout Note: Place near JDIMM1.203,204

CD23 CD24 CD25 CD26 CD27 CD28 0.1U_0402_10V7K
CD29 10U_0603_6.3V6M

RD6 10K_0402_5%
RD7 10K_0402_5%
+3VS
CD30 2.2U_0402_6.3V6M
CD31 0.1U_0402_10V7K
+0.675VS

ESD solution
CD62 22U_0603_6.3V6M ESD@

CAD NOTE
PLACE THE CAP NEAR TO DIMM RESET PIN

ESD@ CD3 0.1U_0402_10V7K

RD3 470_0402_5%
<18> DDR3_DRAMRST# DDR3_DRAMRST#_CPU <6>
@ RD5 0_0402_1%

DDR3L SODIMM ODT GENERATION

+5VALW +1.35V
QD2 BSS138-G_SOT23-3
R2347 220K_0402_5%~D
@ R2351 2M_0402_5%
M_ODT
R2348 66.5_0402_1% M_ODT0
R2349 66.5_0402_1% M_ODT1
R2350 66.5_0402_1% M_ODT2 <18>
R2352 66.5_0402_1% M_ODT3 <18>
0.675V_DDR_VTT_ON 0.675V_DDR_VTT_ON <41>

M_ODT
CD64 ESD@ 0.1U_0402_10V7K
Place CC31 between QD2 and R2349

<6> DDR_PG_CTRL
U2303 74AUP1G07GW_TSSOP5 (NC VCC A GND Y)
@ CD23 0.1U_0402_10V7K
0.675V_DDR_VTT_ON

Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: DDRIII DIMMA
Size: Document Number: LA-9982P
Rev: 3.0
Date: Wednesday, May 29, 2013 Sheet 17 of 57

H=4mm

2-3A to 1 DIMMs/channel

Populate RD4, De-Populate RD8 for Intel DDR3 VREFDQ multiple methods M1
Populate RD8, De-Populate RD4 for Intel DDR3 VREFDQ multiple methods M3

<7> DDR_B_DQS#[0..7]
<7> DDR_B_D[0..63]
<7> DDR_B_DQS[0..7]
<7> DDR_B_MA[0..15]

All VREF traces should have 10 mil trace width

Layout Note:
Place near JDIMM2

Note:
Check voltage tolerance of VREF_DQ at the DIMM socket

Layout Note:
Place near JDIMM2.203,204

For ME concern, CD51 uesd H1.4

CAD NOTE
PLACE THE CAP NEAR TO DIMM RESET PIN

JDIMM2
CONN@
LCN_DAN06-K4406-0102

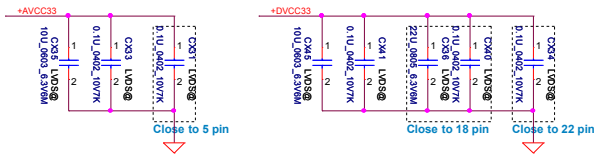
Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

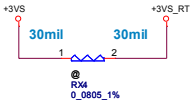
Compal Electronics, Inc.

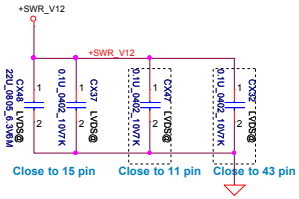
Title: DDRIII DIMMB

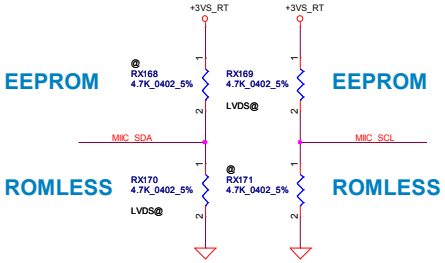
Size	Document Number	Rev
	LA-9982P	3.0

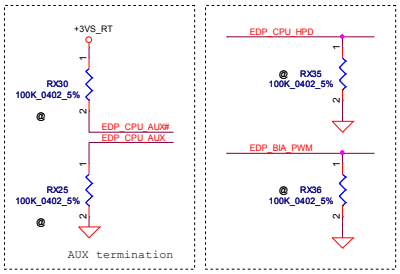
Date: Wednesday, May 29, 2013 Sheet 18 of 57

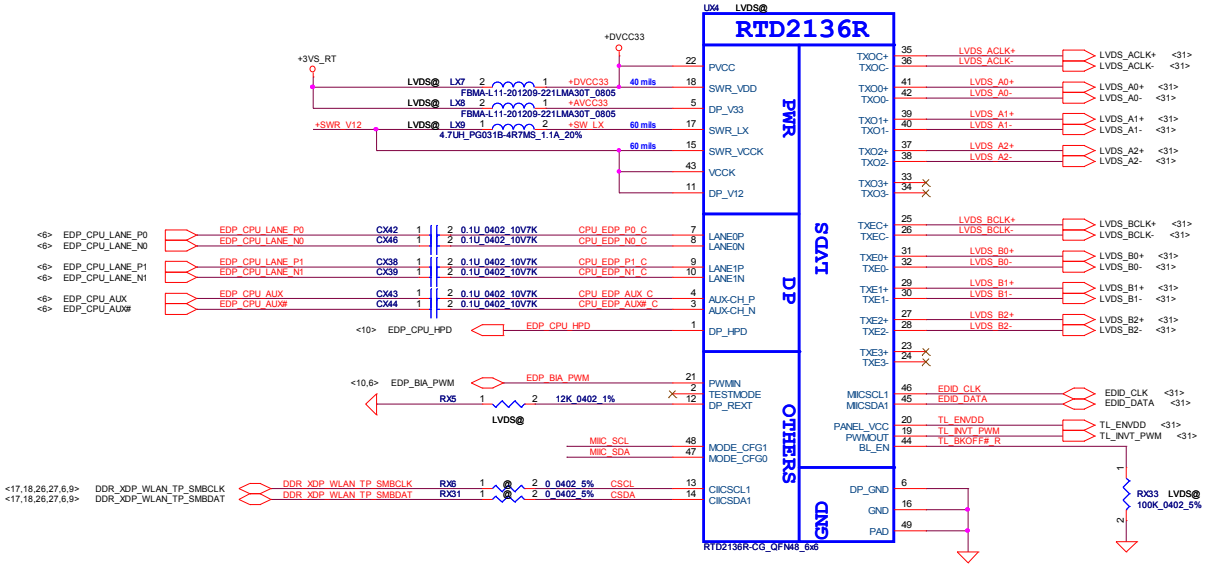




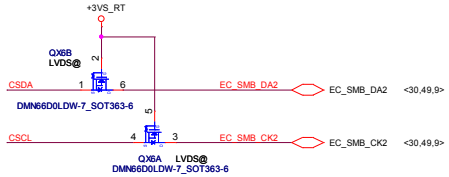


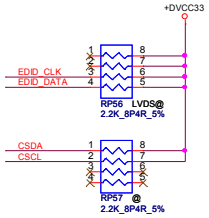




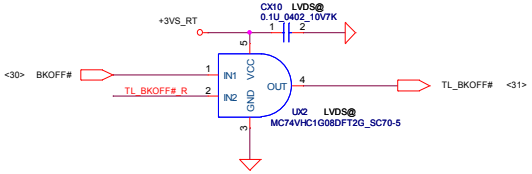


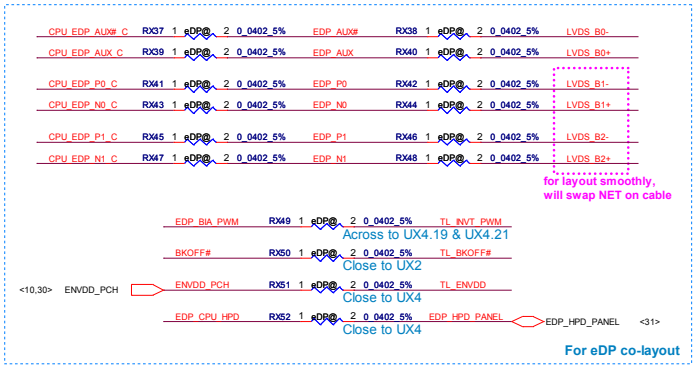
RTD2136S : SA00004NW10
RTD2136R : SA000067100





Vendor advise reserve it





Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.			
Title	eDP to LVDS converter		
Size	Document Number		Rev
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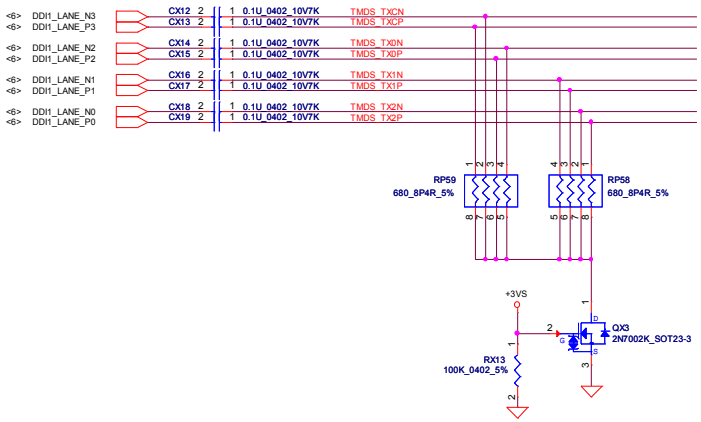
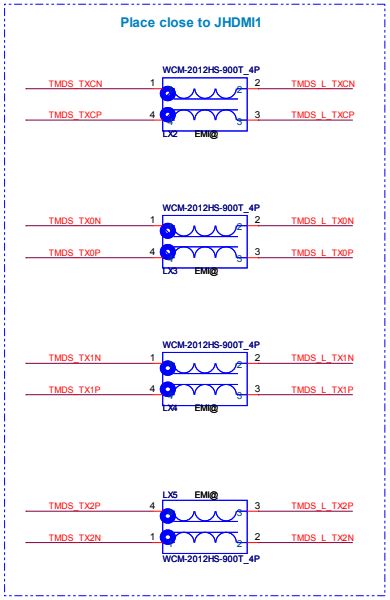
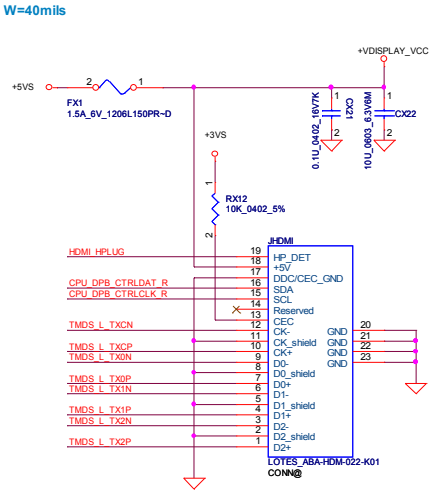
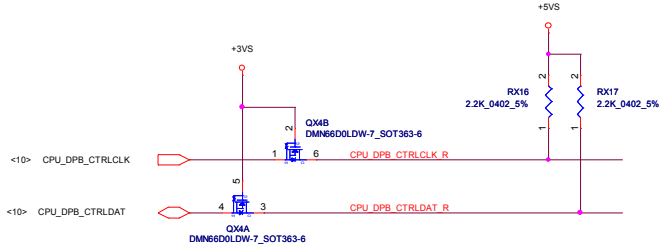
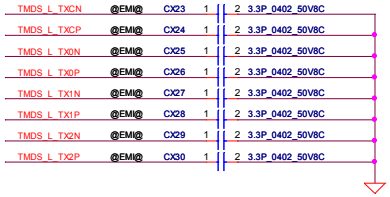
Date:	Wednesday, May 29, 2013	Sheet	19 of 57

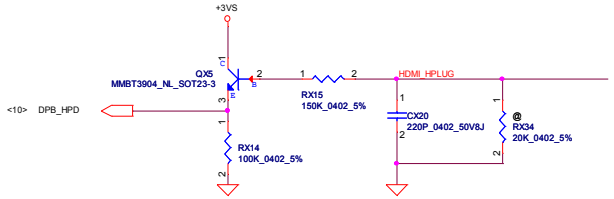












Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.			
Title: HDMI			
Size	Document Number: LA-9982P		Rev: 3.0
Date: Wednesday, May 29, 2013	Sheet 20 of 57		

W=40mils

JP3 @ 2MM

+3VALW

UL2 APL3512ABI-TRG_SOT23-5 (VIN, VOUT, GND, SS, EN)

CL39 1U_0402_6.3V6K

@ CL38 0.1U_0603_25V7K

APL3512 PIN 4 tire to VIN

<30> WOL_EN — WOL_EN — RL27 100K_0402_5%

W=40mils

W=40mils

+LAN_IO rising time : >1ms and <100ms

+LAN_IO — 1.5A — CL15 0.1U_0402_10V7K — CL19 0.1U_0402_10V7K

These caps close to Pin 23,32
For 8106E pop the capacitor close pin 23,32

SS table

Css	Tss
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS

+LAN_VDD — CL20 0.1U_0402_10V7K — CL22 0.1U_0402_10V7K — CL26 0.1U_0402_10V7K

These caps close to Pin 8,30
For 8106E pop capacitor close to pin 8,30

RL19 75_0603_5% — MCT0

RL20 75_0603_5% — MCT1

EMI@ CL33 10P_1206_2KV8J

Place close to TCT pin

TL1 XFORM_NS0014 (MDI1-, MDI1+, MDI0-, MDI0+, RD+, RD-, CT, NC, TD+, TD-, RX+, RX-, TX+, TX-, MDO1-, MDO1+, MCT0, MCT1, MDO0-, MDO0+)

CL41 0.01U_0402_16V7K

Change CPN to SP050007J00 only
Need CIS symbol

CL30, CL31 close to UL1 Pin 17, 18

UL1 RTL8106E-CG_QFN32_4X4

<12> PCIE_PRX_LANTX_P3 — CL30 0.1U_0402_10V7K — PCIE_PRX_LANTX_P3_C — HSOP
<12> PCIE_PRX_LANTX_N3 — CL31 0.1U_0402_10V7K — PCIE_PRX_LANTX_N3_C — HSON

<12> PCIE_PTX_LANRX_P3 — PCIE_PTX_LANRX_P3 — HSIP
<12> PCIE_PTX_LANRX_N3 — PCIE_PTX_LANRX_N3 — HSIN

<10,26,30,48,6> PLT_RST# — PERSTB

ISOLATEB — ISOLATEB

<10,30> PCIE_WAKE# — PCIE_WAKE# — LANWAKEB

PAD~D T96 @ — GPO

MDIP0 — MDI0+
MDIP1 — MDI1+
MDIN0 — MDI0-
MDIN1 — MDI1-

AVDD10 — +LAN_VDD
AVDD10
AVDD33 — +LAN_IO
DVDD33

REFCLK_P — CLK_PCIE_LAN <9>
REFCLK_N — CLK_PCIE_LAN# <9>

CLKREQB — LAN_CLKREQ# <9>
CKXTAL1 — XTLO
CKXTAL2 — XTLI

LED0 — @ T94 PAD~D
LED1 — @ T95 PAD~D

RSET — RL31 2.49K_0402_1%

GND

NC

+LAN_IO — RL34 10K_0402_5% — PCIE_WAKE#

For GCLK

<29> XTLI — XTLI

CL36 10P_0402_50V8J XTAL@ — XTLI

YL2 XTAL@ 25MHZ_10PF_7V25000014 (OSC, GND)

CL37 10P_0402_50V8J XTAL@ — XTLO

W=20mils

+LAN_VDD — CL34 0.1U_0402_10V7K — CL35 1U_0402_6.3V6K

JLAN SANTA_130456-311 CONN@ (PR4-, PR4+, PR2-, PR3-, PR3+, PR2+, PR1-, PR1+, MDO1-, MDO1+, MDO0-, MDO0+, SHLD1, SHLD2)

+3VS — RL33 1K_0402_5% — ISOLATEB — RL35 15K_0402_5%

+LAN_IO — @ RL37 10K_0402_5% — LAN_CLKREQ# — @ RL38 10K_0402_5% — WOL_EN

Reserve 10K pull LAN_IO

Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: LAN RTL8106E

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Reserve for HDA issue

CA71, CA51 place close to Pin 26

CA53, CA55 change Value from 10U_0603_6.3V6M~D to 4.7U_0603_6.3V6K

CA57,CA58 close to UA1 pin1

RA51, RA33 place close to UA1

JACK_PLUG Delay circutis

Reserve for cancel Delay circutis

Place on the moat between GND & GNDA.

SM01000BV00
need CIS symbol

EC Beep

MCU Beep

PC Beep

Close to UA1
Pin11,13,14,16

close to Codec

Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-
Speaker 4 ohm : 40mil
Speaker 8 ohm : 20mil

iPhone and Nokia type Combo Jack

40mil

40mil

Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

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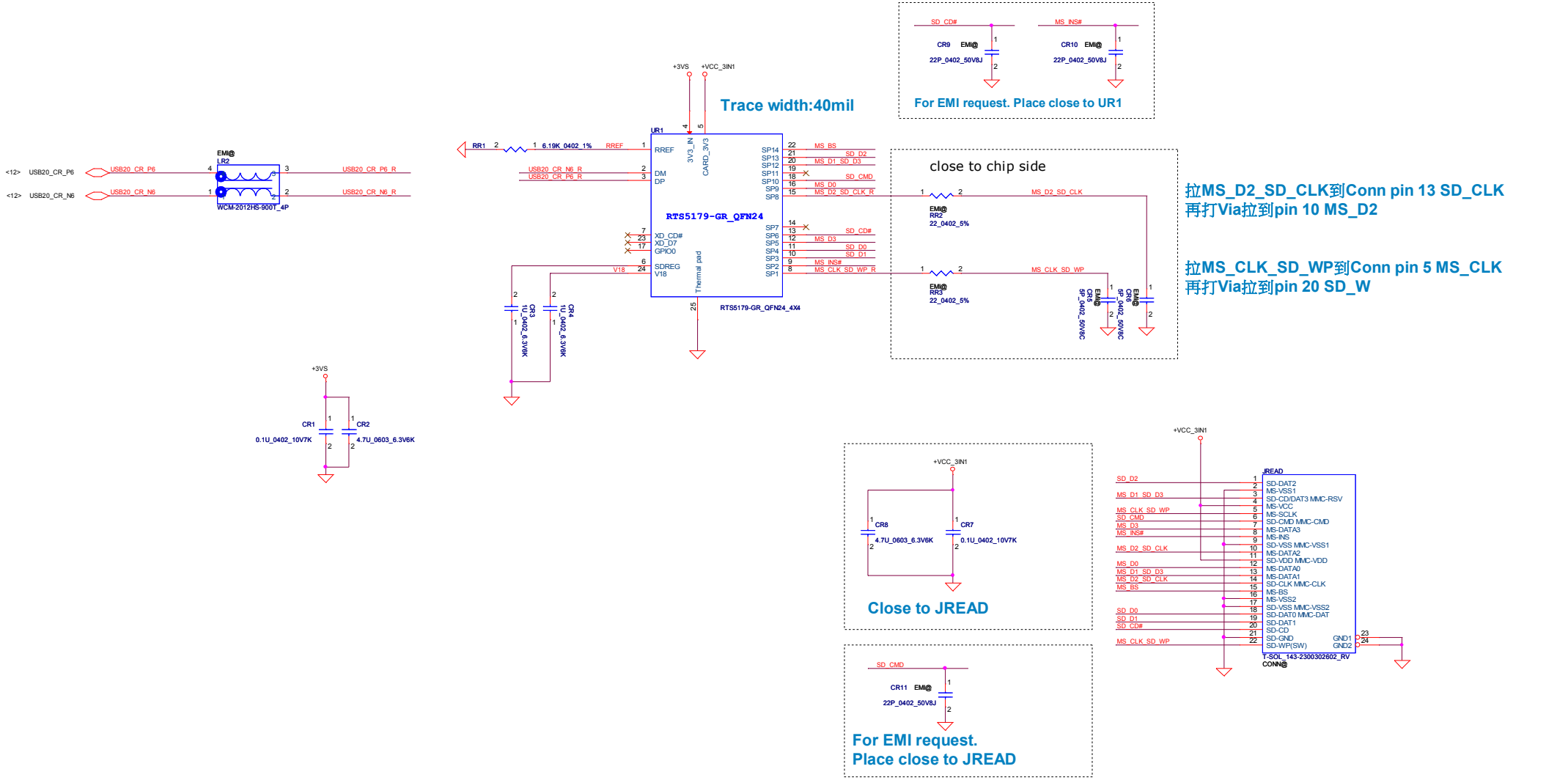
Compal Electronics, Inc.

Title: Audio Codec ALC3223

Size: | Document Number: LA-9982P | Rev: 3.0

Date: Wednesday, May 29, 2013 | Sheet 22 of 57



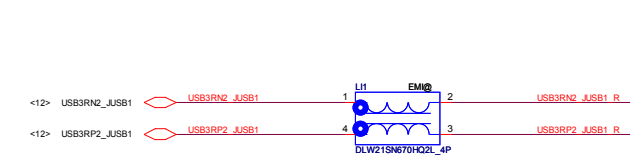
Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

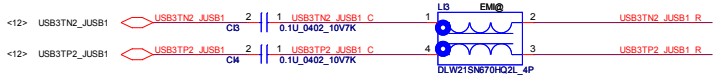
Compal Electronics, Inc.

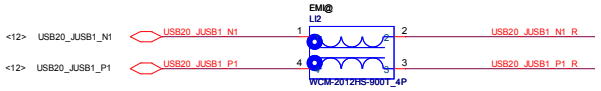
Title: Card Reader RTS5179

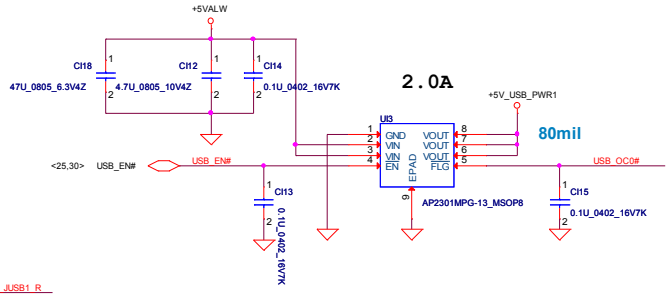
Size: | Document Number: LA-9982P | Rev: 3.0

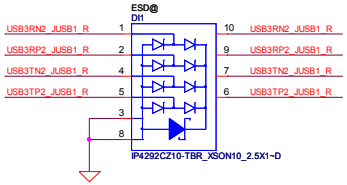
Date: Wednesday, May 29, 2013 | Sheet 23 of 57



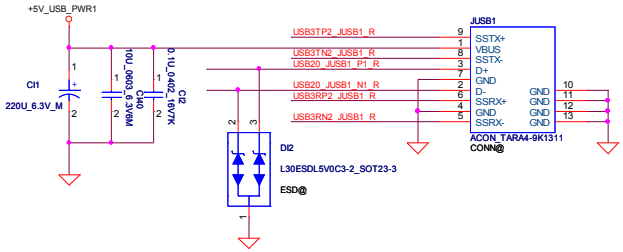


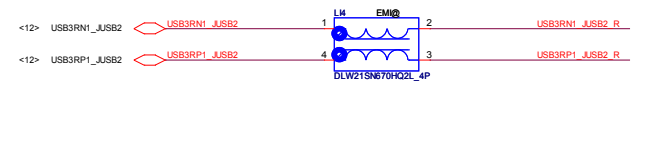


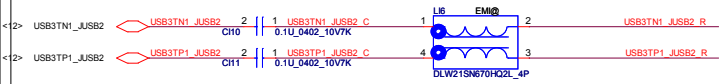


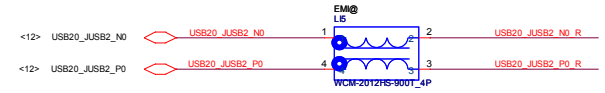


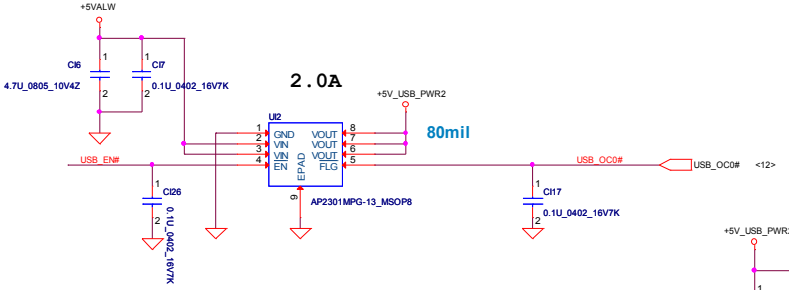
USB connector1
USB20 port1
USB30 port2

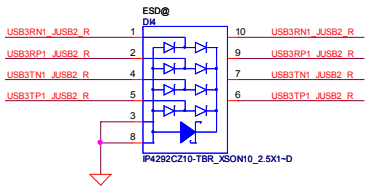




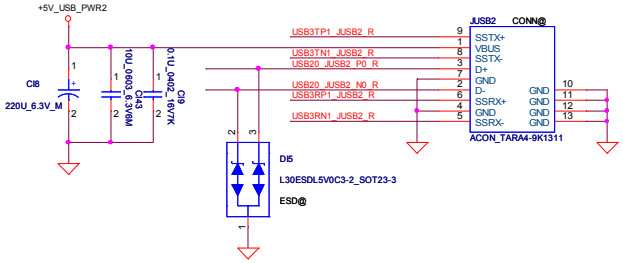








USB connector2
USB20 port0
USB30 port1



Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: USB3.0

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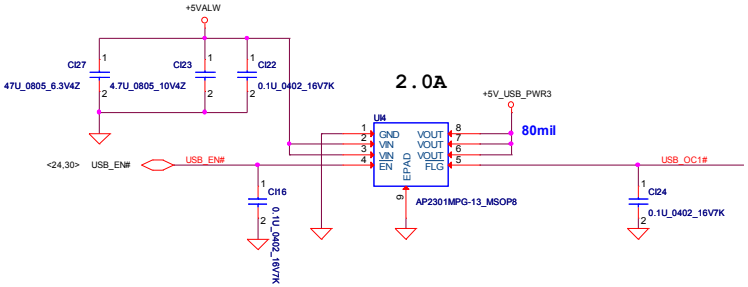
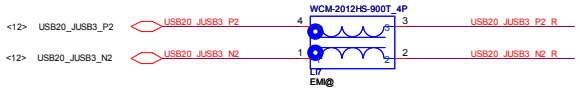
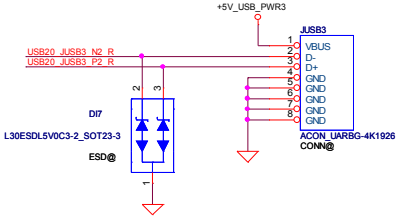
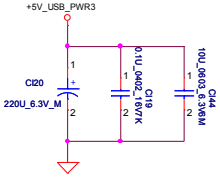


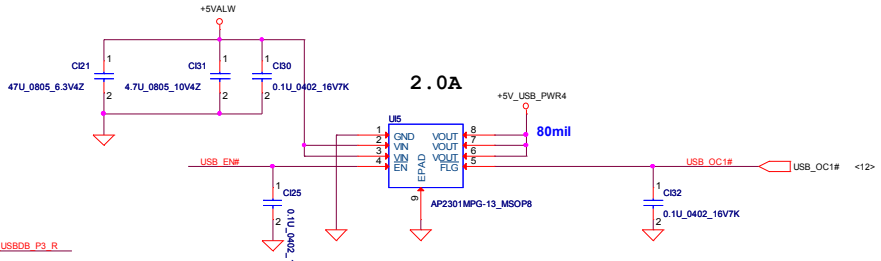


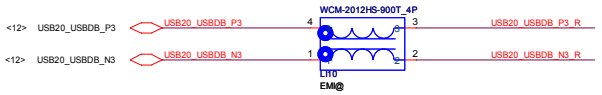
USB connector3
USB20 port2



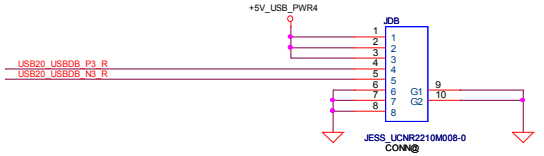


Place close to JUSB3





USB connector4
USB20 port3



2nd: SP01001EX00
Main: SP01001AA00
Change CONN symbol for DFB

Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: MB to USB2.0 DB

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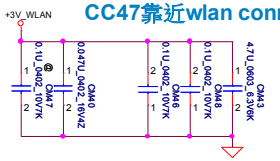
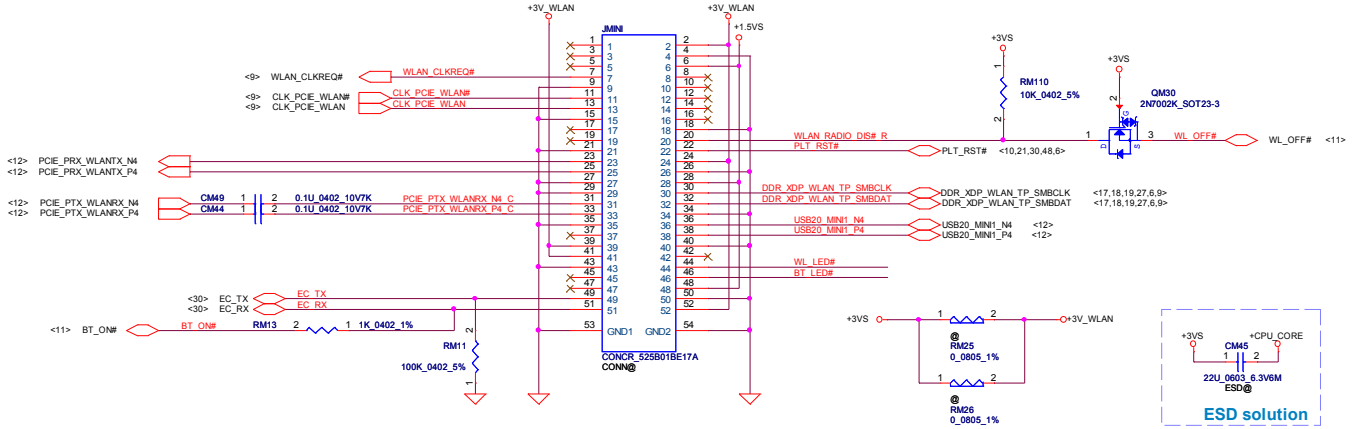
CC47靠近wlan connector

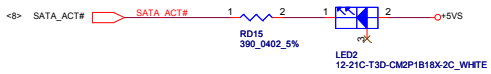


Mini WLAN/WIMAX H=6.7



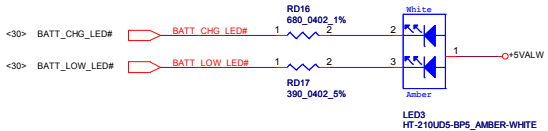
HDD LED

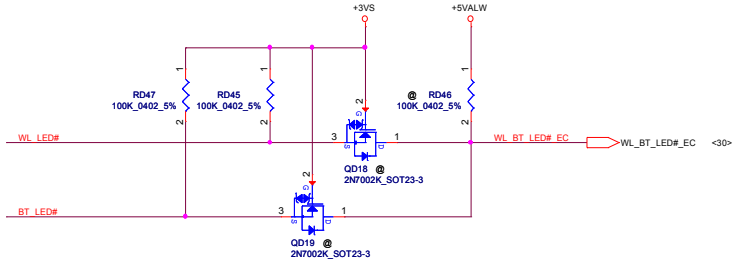
10mils, All pins

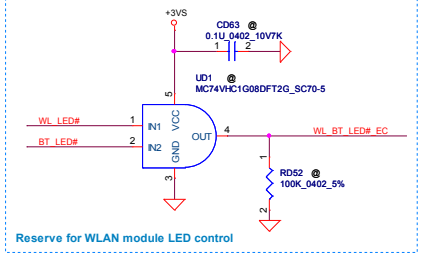


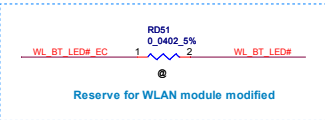
Power LED

Battery LED

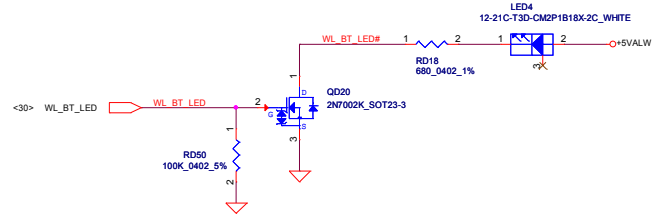








Wireless LED



Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.			
Title	Mini Card/LED		
Size	Document Number		Rev
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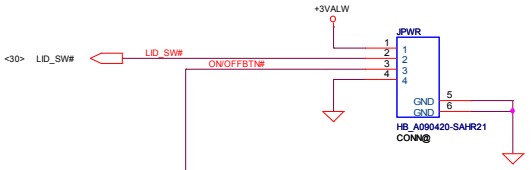
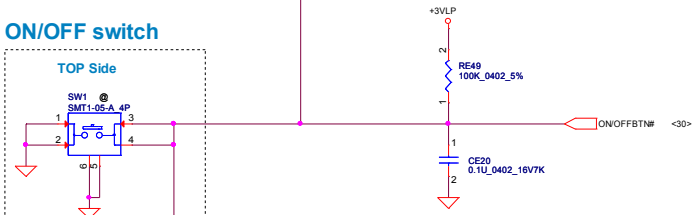
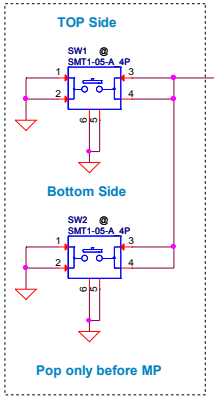
POWER/B



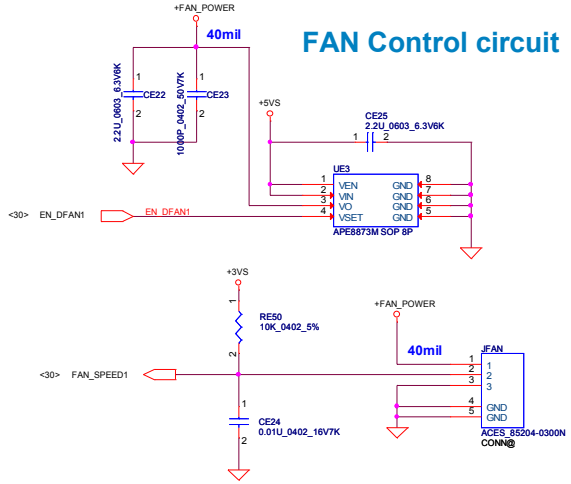
Power ON Circuit



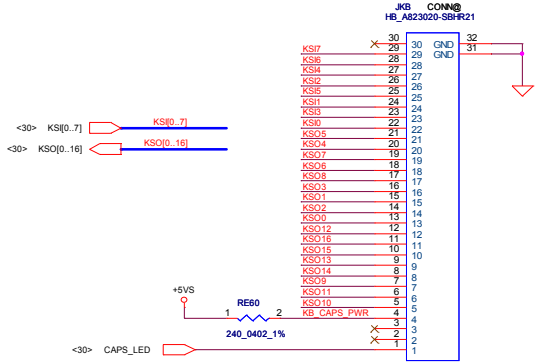
ON/OFF switch



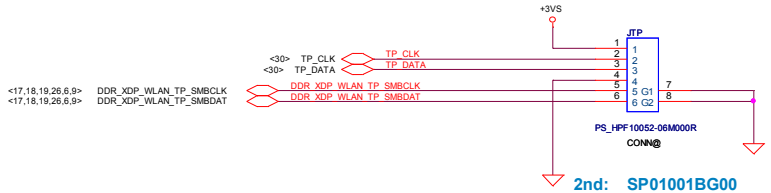
FAN Control circuit



INT_KBD Connector



Touch pad



2nd: SP01001BG00
Main: SP01000R910
Change CONN symbol for DFB

Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.			
Title	FAN/TP/PWR SW		
Size	Document Number		Rev
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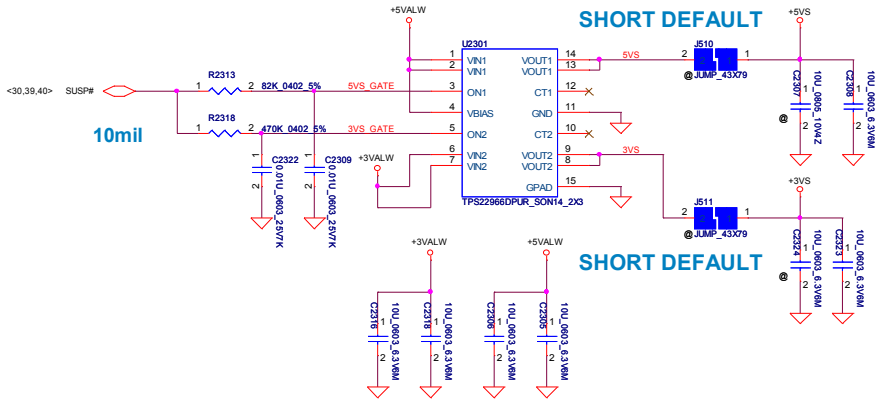
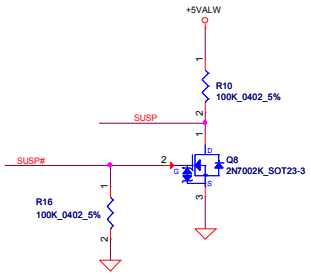
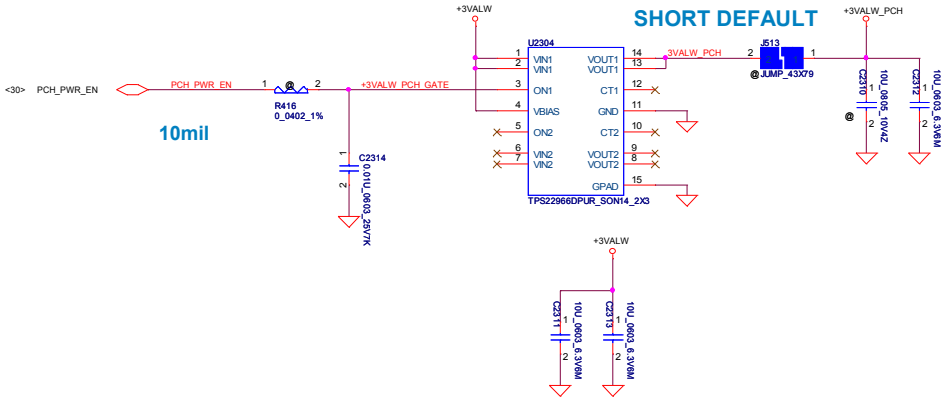
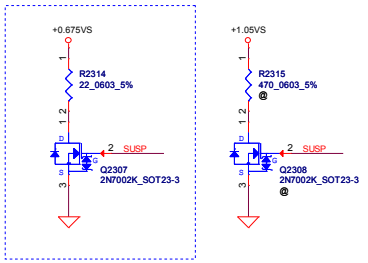
+5VS and +3VS switch





+3VALW_PCH switch





For Intel S3 Power Reduction

Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: DC/DC Interface

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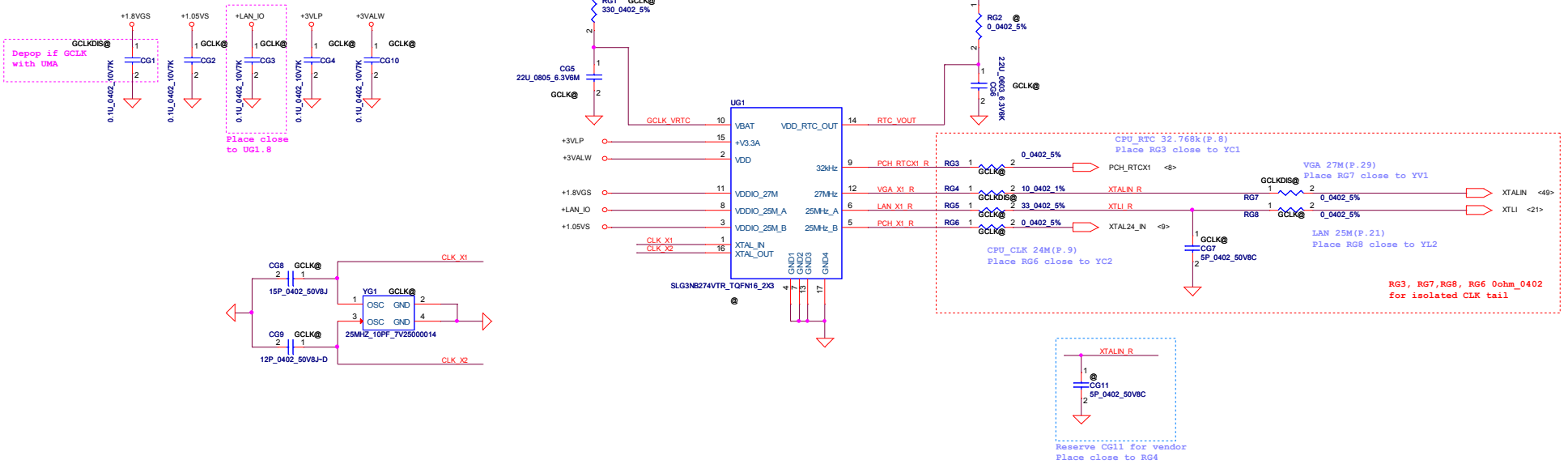
UG1 GCLKUMA@ SLG3NB244VTR TQFN 16P CLK GEN

UG2 GCLKDIS@ SLG3NB244VTR TQFN 16P CLK GEN

SLG3NB3374V is for DIS by output 24M*1,25M*1, 27M*1, 32K*1
SLG3NB3375V is for UMA by output 24M81, 25M*1, 32K*1



Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.			
Title: GCLK			
Size	Document Number: LA-9982P		Rev: 3.0
Date: Wednesday, May 29, 2013	Sheet 23 of 57		

SD028000080	0_0402_5%
SD034120280	12K_0402_1%
SD034100300	27K_0402_1%
SD034430280	43K_0402_1%
SD034560280	56K_0402_1%
SD034750280	75K_0402_1%
SD034100380	100K_0402_1%
SD034130380	130K_0402_1%
SD034160380	160K_0402_1%
SD034200380	200K_0402_1%
SD000001B80	240K_0402_1%
SD00000G280	270K_0402_1%
SD034330380	330K_0402_1%
SD028430380	430K_0402_1%

Board ID
Venus DIS@
UMA UMA@

RE5 DIS@ 270K_0402_1% SD00000G280

+3VALW Ra RE3 100K_0402_1% AD_BID0 Rb RE5 0_0402_5% UMA@ CE8 0.1U_0402_10V7K

PLT_RST# CE36 ESD@ 0.047U_0402_16V4Z
Place CC30 close to RC51.1

EMI@ LE1 FBMA-L11-160808-800LMT_0603

+3VALW CE1 0.1U_0402_10V7K CE2 0.1U_0402_10V7K @EMI@ CE5 1000P_0402_50V7K @EMI@ CE6 1000P_0402_50V7K +3VLP +EC_VCCA CE7 0.1U_0402_10V7K ECAGND

UE1 KB9012QF-A4_LQFP128_14X14

EC_VDD/AVCC EC_VDDVCC EC_VDDVCC EC_VDDVCC EC_VDDVCC EC_VDDVCC EC_VDDVCC

GATEA20/GPIO00 KBRST#/GPIO01 SERIRQ LPC_FRAME# LPC_AD3 LPC_AD2 LPC_AD1 LPC_AD0 CLK_PCI_EC PCIRST#/GPIO05 EC_RST# EC_SCI#/GPIO0E GPIO1D

PC & MISC

<26> WL_BT_LED WL_BT_LED
<11> KB_RST# KB_RST#
<11> SERIRQ SERIRQ
<9> LPC_LFRAME# LPC_LFRAME#
<9> LPC_LAD3 LPC_LAD3
<9> LPC_LAD2 LPC_LAD2
<9> LPC_LAD1 LPC_LAD1
<9> LPC_LAD0 LPC_LAD0
<9> CLK_PCI_LPC CLK_PCI_LPC
<10,21,26,48,6> PLT_RST# PLT_RST#
EC_RST# EC_RST#
<11> EC_SCI# EC_SCI#
<31> TOUCH_RST TOUCH_RST

@EMI@ CE12 0.1U_0402_10V7K @EMI@ R2354 0_0402_5% +3VALW RE8 47K_0402_5% CE11 0.1U_0402_10V7K

"TOUCH_RST" for OAK 15 only

"KB_LED_PWM" for OAK 17 only

PWM Output
GPIO0F KB_LED_PWM
BEEP#/GPIO10 BEEP# <22>
GPIO12 USB_EN# <24,25>
ACOFF/GPIO13 ACOFF <37>

AD Input
BATT_TEMP/GPIO38 BATT_TEMP
GPIO39 WL_BT_LED# EC <26>
ADP_I/GPIO3A ADP_I <36,37>
GPIO3B
GPIO42 AD_BID0
IMON/GPIO43 PANEL_BKLEN <10>

CE9 100P_0402_50V8J ECAGND
BATT_TEMP <36,37>
PCH_HOT# <9>
@ RE7 0_0402_5%

+3VS TP_CLK 4.7K_0402_5% RE9 TP_DATA 4.7K_0402_5% RE10

DA Output
DAC_BRIG/GPIO3C EN_INVPWR <31>
EN_DFAN1/GPIO3D EN_DFAN1 <27>
IREF/GPIO3E EC_ENVDD <31>
CHGVADJ/GPIO3F LCD_TEST <31>

PS2 Interface
EC_MUTE#/GPIO4A EC_MUTE# <22>
USB_EN#/GPIO4B SIO_SLP_S4# <10>
CAP_INT#/GPIO4C IMVP_PWRGD <42>
EAPD/GPIO4D SYS_PWROK <10,6>
TP_CLK/GPIO4E TP_CLK <27>
TP_DATA/GPIO4F TP_DATA <27>

SPI Device Interface
CPU1.5V_S3_GATE/GPXIOA00 SUSACK# <10>
WOL_EN/GPXIOA01 WOL_EN <21>
ME_EN/GPXIOA02 ME_EN <8>
VCIN0_PH/GPXIOD00 VCIN0_PH <36>

SPI Flash ROM
SPID/GPIO5B EC_SPI_MOSI_1 <9>
SPIDO/GPIO5C EC_SPI_MISO_1 <9>
SPICLK/GPIO5B EC_SPI_CLK_R <9>
SPICS#/GPIO5A EC_SPI_CS0# <9>

GPIO
ENBKL/GPIO40 ERP_LOT6 <36>
PECI_KB930/GPIO41 WL_BT_LED#_EC2 <26>
FSTCHG/GPIO50 SIO_SLP_S0# <10>
BATT_CHG_LED#/GPIO52 BATT_CHG_LED# <26>
CAPS_LED#/GPIO53 CAPS_LED <27>
PWR_LED#/GPIO54 PWR_PWM_LED# <26>
BATT_LOW_LED#/GPIO55 BATT_LOW_LED# <26>
SYSON/GPIO56 SYSON <41>
VR_ON/GPIO57 VR_ON_EC
PM_SLP_S4#/GPIO59 CPU_DETECT# <6>

RE11 100K_0402_5% +3VALW
RE12 0_0402_5% VR_ON <13,42>
@ RE1 10K_0402_5%
CE26 0.1U_0402_10V7K

GPO
EC_RSMRST#/GPXIOA03 EC_RSMRST# <10>
EC_LID_OUT#/GPXIOA04 EC_LID_OUT# <11>
PROCHOT_IN/GPXIOA05 VCIN1_PH <36>
H_PROCHOT#_EC/GPXIOA06 VCOUT1_PH <36>
VCOUT0_PH/GPXIOA07 VCOUT0_PH# <38>
BKOFF#/GPXIOA08 BKOFF# <19>
PBTN_OUT#/GPXIOA09 PBTN_OUT# <10,6>
PCH_APWROK/GPXIOA10 PCH_PWR_EN <28>
SA_PGOOD/GPXIOA11 ACIN_65W <49>
RE38 43_0402_1%
RE2 10K_0402_5%

GPI
AC_IN/GPXIOD01 ACIN <10,36,37,49>
EC_ON/GPXIOD02 EC_ON <38>
ON/OFFBTN#/GPXIOD03 ON/OFFBTN# <27>
LID_SW#/GPXIOD04 LID_SW# <27>
SUSP#/GPXIOD05 SUSP# <28,39,40>
GPXIOD06 65W/90W# <36>
PECI_KB9012/GPXIOD07 PECI_EC <6>
RE43 43_0402_1%

V18R +V18R
CE16 4.7U_0805_10V4Z

LE2 FBMA-L11-160808-800LMT_0603 ECAGND

20mil

Int. K/B Matrix
KSI[0..7] KSO[0..16]
KSI0/GPIO30 KSI1/GPIO31 KSI2/GPIO32 KSI3/GPIO33 KSI4/GPIO34 KSI5/GPIO35 KSI6/GPIO36 KSI7/GPIO37
KSO0/GPIO20 KSO1/GPIO21 KSO2/GPIO22 KSO3/GPIO23 KSO4/GPIO24 KSO5/GPIO25 KSO6/GPIO26 KSO7/GPIO27 KSO8/GPIO28 KSO9/GPIO29 KSO10/GPIO2A KSO11/GPIO2B KSO12/GPIO2C KSO13/GPIO2D KSO14/GPIO2E KSO15/GPIO2F KSO16/GPIO48 KSO17/GPIO49

<27> KSI[0..7] <27> KSO[0..16]
+3VALW RE71 10K_0402_5% LID_SW#
RP36 2.2K_0804_8P4R_5% EC_SMB_CK1 EC_SMB_DA1 EC_SMB_CK2 EC_SMB_DA2
<10> PCH_DPWROK RE37 0_0402_1%

SM Bus
EC_SMB_CK1/GPIO44 EC_SMB_DA1/GPIO45 EC_SMB_CK2/GPIO46 EC_SMB_DA2/GPIO47
<36,37> EC_SMB_CK1
<36,37> EC_SMB_DA1
<19,49,9> EC_SMB_CK2
<19,49,9> EC_SMB_DA2

GPIO
PM_SLP_S3#/GPIO04 PM_SLP_S5#/GPIO07 EC_SMI#/GPIO08 GPIO0A GPIO0B GPIO0C GPIO0D EC_INVT_PWM/GPIO11 FAN_SPEED1/GPIO14 EC_PME#/GPIO15 EC_TX/GPIO16 EC_RX/GPIO17 PCH_PWROK/GPIO18 SUSP_LED#/GPIO19 NUM_LED#/GPIO1A
<10> SIO_SLP_S3# SIO_SLP_S3#
<10> SIO_SLP_S5# SIO_SLP_S5#
<8> EC_SMI# EC_SMI#
<36> PS_ID PS_ID
<31> CE_EN CE_EN
<10,44> DGPU_PWROK DGPU_PWROK
<10,19> ENVDD_PCH ENVDD_PCH
<31> DBC_EN DBC_EN
<27> FAN_SPEED1 FAN_SPEED1
<10,21> PCIE_WAKE# PCIE_WAKE#
<26> EC_TX EC_TX
<26> EC_RX EC_RX
<10> PCH_PWROK PCH_PWROK
<10> ME_SUS_PWR_ACK ME_SUS_PWR_ACK
<6> RUNPWROK RUNPWROK

<40> +1.05V_PGOOD +1.05V_PGOOD
<13> VCCST_PG_EC VCCST_PG_EC

XCLKI/GPIO5D XCLKO/GPIO5E

GNDGND GNDGND GNDGND GNDGND GND AGND/AGND

Reserve for ESD
CE27 ESD@ 0.1U_0402_10V7K SIO_SLP_S3#
CE28 ESD@ 0.1U_0402_10V7K SIO_SLP_S5#
Please close to EC

PCH_PWROK RE18 10K_0402_5%

FAN_SPEED1 CE29 220P_0402_50V8J
Please close to EC

<42> VR_HOT# VR_HOT# @ RE44 0_0402_1%
<36,6> H_PROCHOT# H_PROCHOT#
UE2 SN74LVC1G06DCKR_SC70-5
+3VS CE15 0.1U_0402_10V7K
VCOUT1_PH RE47 100K_0402_5%
CE19 47P_0402_50V8J

VR_ON CE34 ESD@ 0.1U_0402_10V7K
Place CE34 between DE1 and RE12

VCCST_PG_EC CE35 ESD@ 220P_0402_50V8J
Place CE35 between DE1 and UE1

VR_ON VCCST_PG_EC DE1 @ESD@ L03ESDL5V0CG3-2_SOT-523-3
Place DE1 close to UE1

LID_SW# CE30 ESD@ 0.1U_0402_10V7K
PCH_PWROK CE31 ESD@ 0.1U_0402_10V7K
SYS_PWROK CE32 ESD@ 0.1U_0402_10V7K
CPU_DETECT# CE33 ESD@ 0.1U_0402_10V7K
Place CE30,CE31,CE32,CE33 close to UE1

ACIN CE18 100P_0402_50V8J

ME_FWP PCH has internal 20K PD.
(suspend power rail)
ME_EN RE326 1K_0402_5%

KB9012A3 change to
KB9012A4 SA00004OB30

Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.
Title: EC ENE-KB9012
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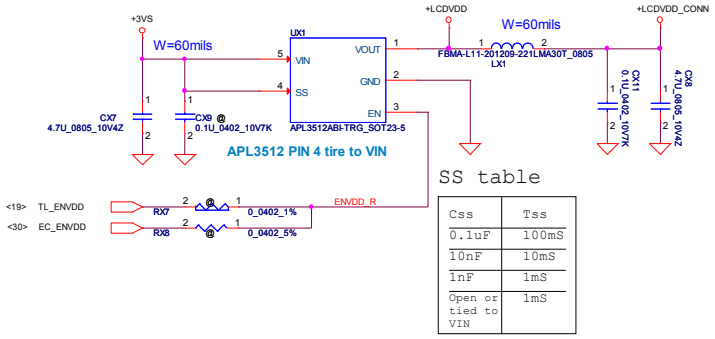
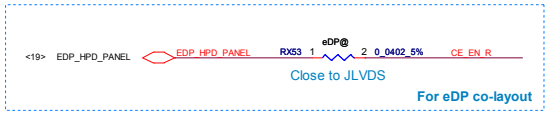
LCD PWR CTRL

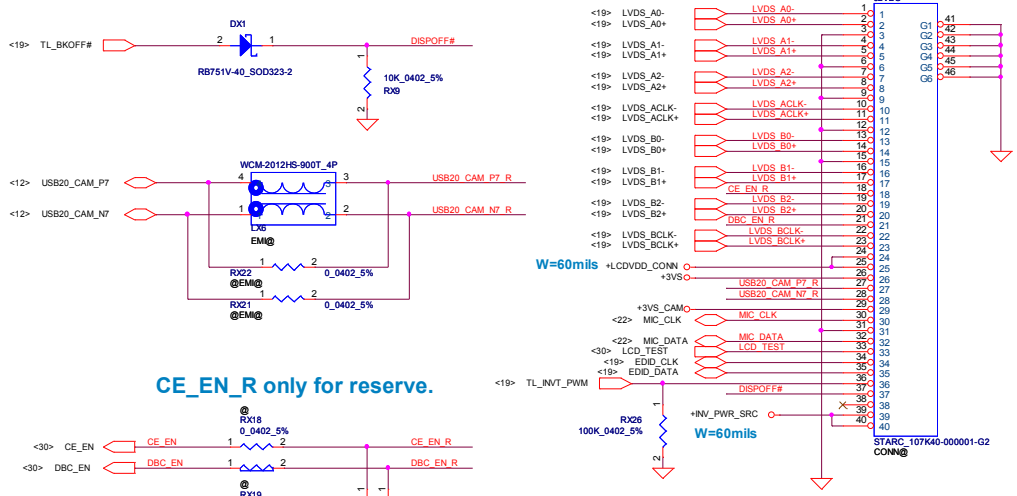


SS table

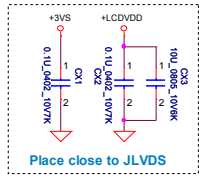
Css	Tss
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS



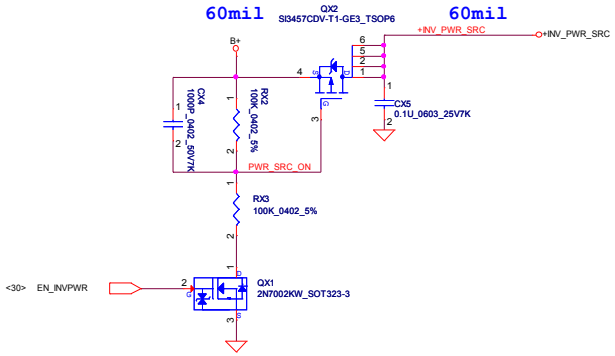
LVDS Connector



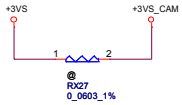
CE_EN_R only for reserve.



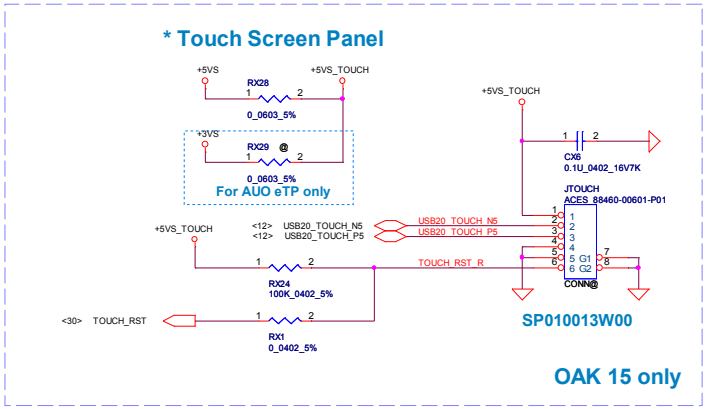
LCD backlight PWR CTRL



Webcam PWR CTRL



* Touch Screen Panel



Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.			
Title: LVDS/webcam/touch			
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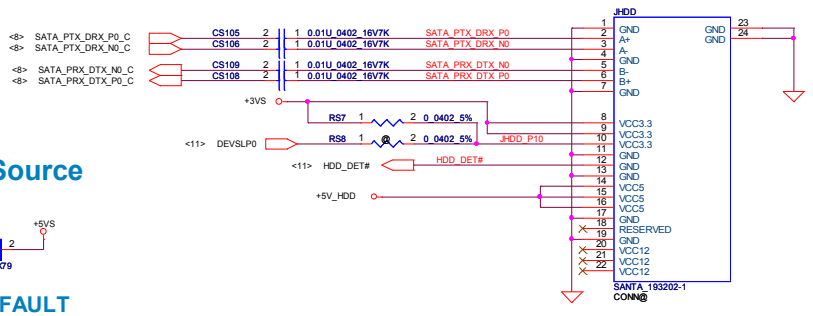
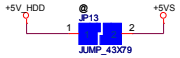
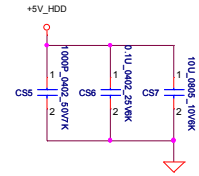
SATA HDD Connector



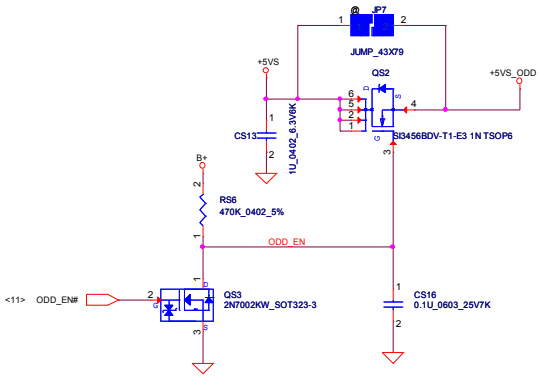
+5V_HDD Source



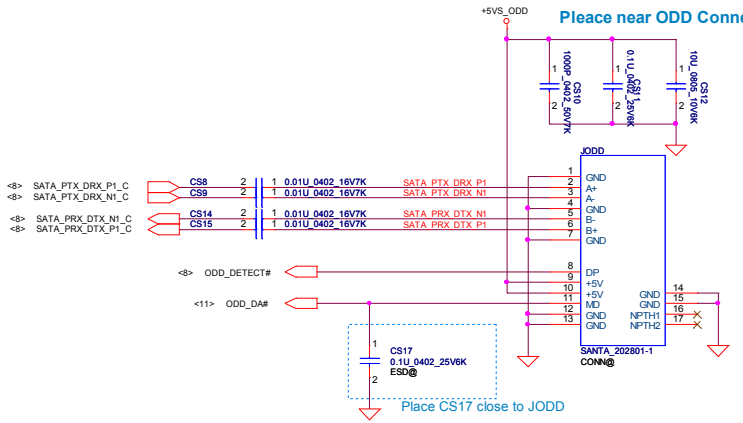
SHORT DEFAULT



ODD Power Control



SATA ODD Connector



Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.			
Title: HDD/ODD			
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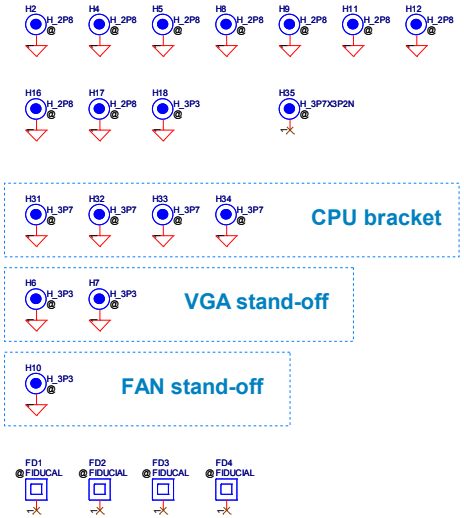
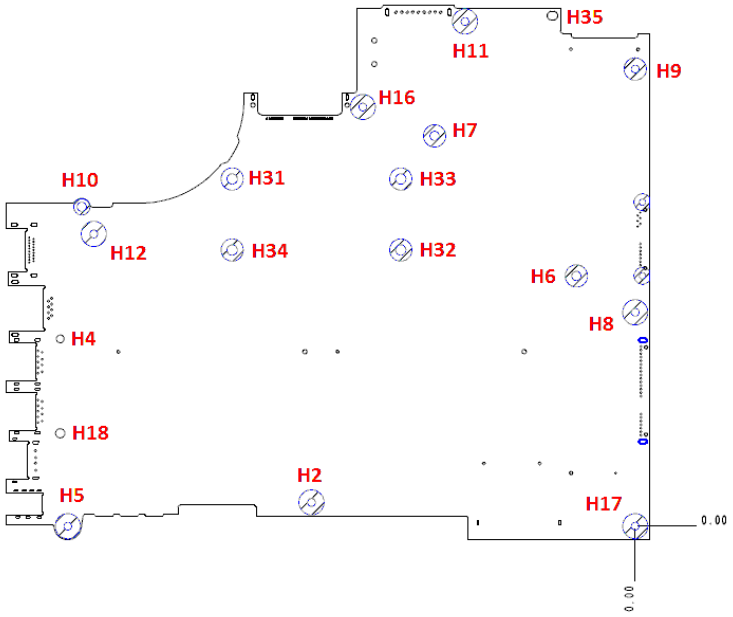
Screw Hole





Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.			
Title: Screw Hole			
Size	Document Number: LA-9982P		Rev: 3.0
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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	34	Card Reader	2012/04/27	HW	The Card reader USB signal is incorrect.	SWAP UR1 USB signal P/N	0.2
2							
3							
4							
5							
6							
7							
8							
9							
10							
11							
12							
13							
14							
15							
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35							
36							
37							
38							
39							
40							
41							

Compal Electronics, Inc.

Title: HW-PIR Page.1

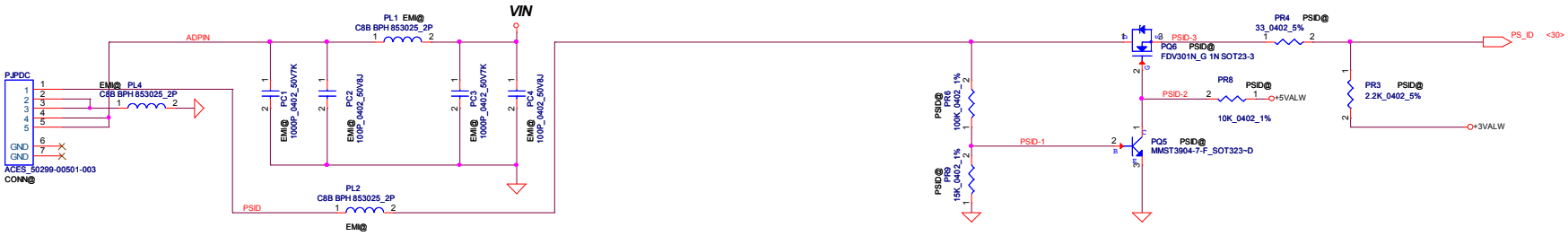
Size | Document Number: LA-9982P | Rev: 3.0

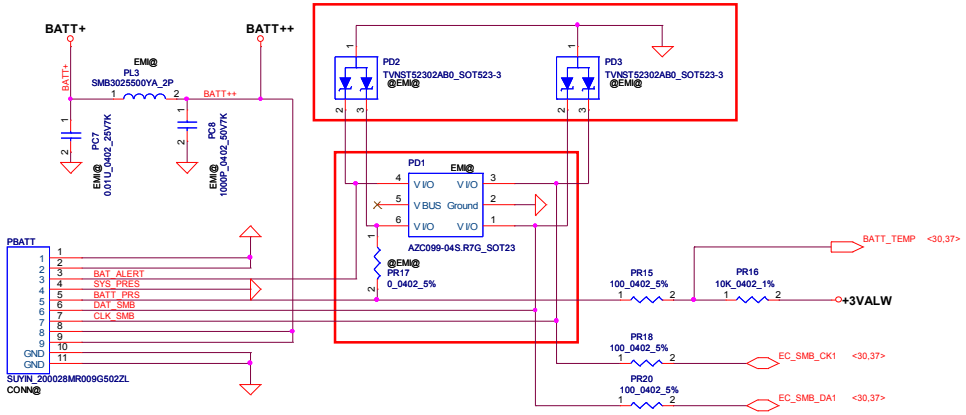
Date: Wednesday, May 29, 2013 | Sheet 34 of 57

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
40							
41							
42							
43							
44							
45							
46							
47							
48							
49							
50							
51							
52							
53							
54							

Compal Electronics, Inc.		
Title: HW-PIR Page.2		
Size	Document Number: LA-9982P	Rev: 3.0
Date: Wednesday, May 29, 2013	Sheet 35 of 57	

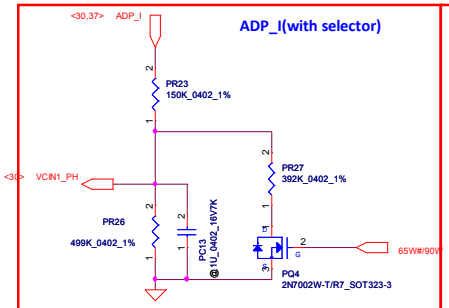




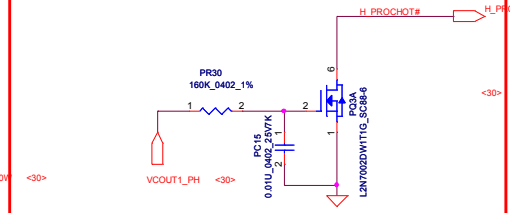
SMART Battery:
01.GND1
02.GND2
03.BAT_ALERT
04.SYS_PRES
05.BATT_PRS
06.DAT_SMB
07.CLK_SMB
08.BATT1+
09.BATT2+

Other component (37.1)

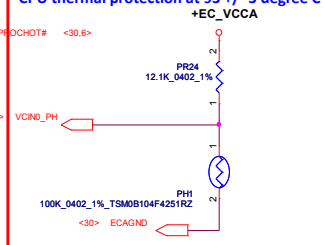
ADP_I(with selector)



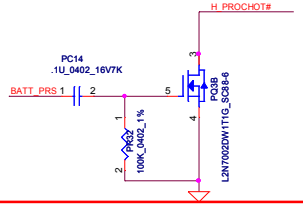
Delay adaptor OC H_PROCHOT# 2ms while hybrid power transition



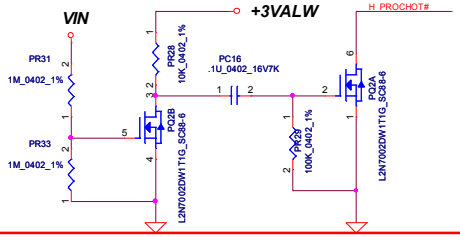
PH1 under CPU bottem side : CPU thermal protection at 93 +/- 3 degree C



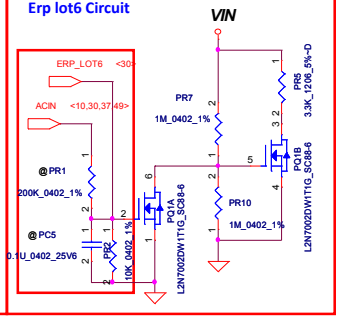
Adapter protection:
if battery removed, adaptor only, then trigger the H_PROCHOT#, keep @ in BOM since battery can not be removed by end user

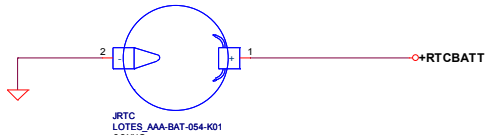


Battery protection:
asserts H_PROCHOT# when adaptor is unplugged, keep low for 10ms till SW PROCHOT# is issued by EC



Erp lot6 Circuit





Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: PWR_DCIN/BATT CONN/OTP

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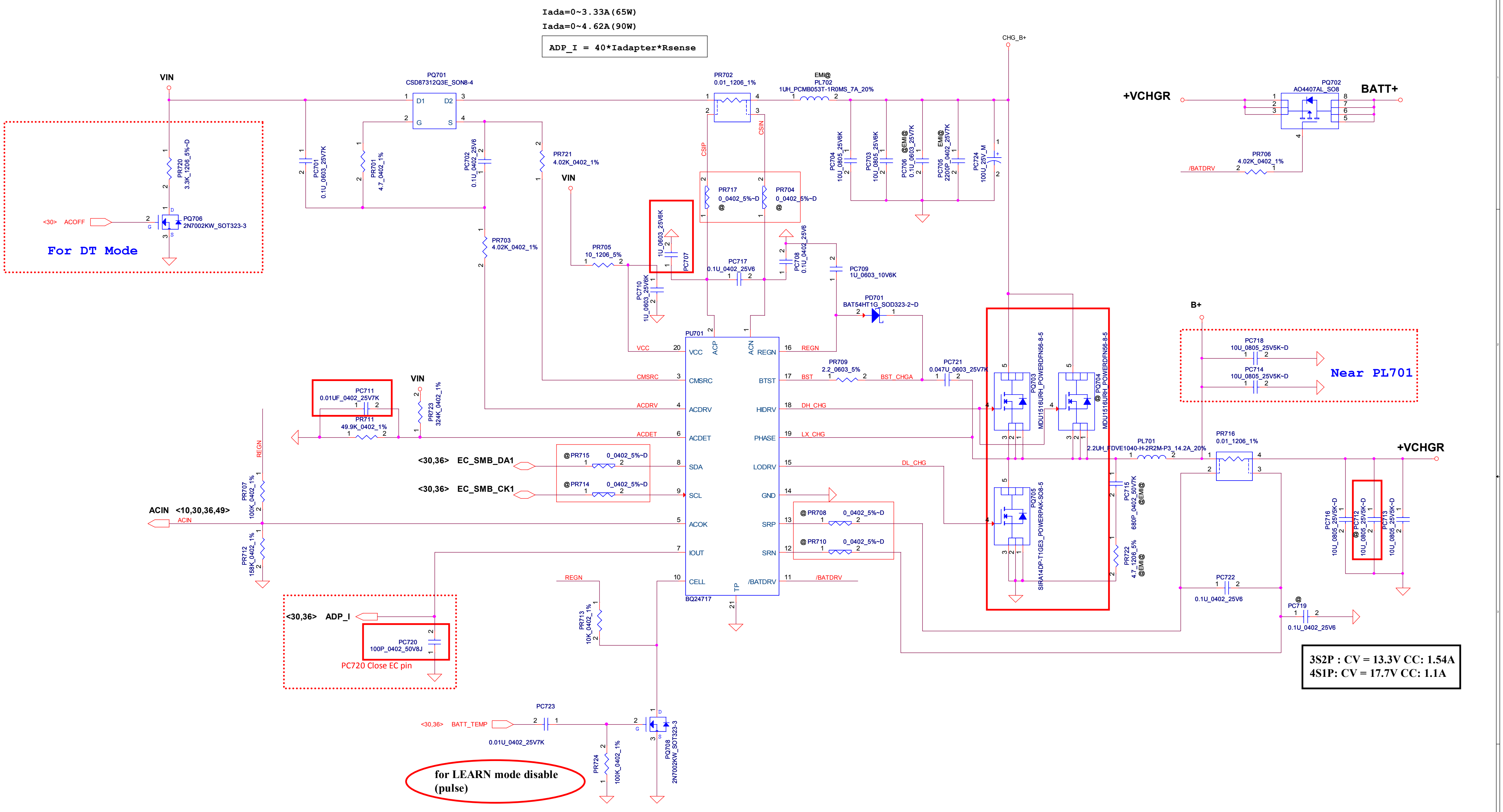

Iada=0~3.33A(65W)
Iada=0~4.62A(90W)
ADP_I = 40*Iadapter*Rsense
VIN
PQ701
CSD87312Q3E_SON8-4
PR702
0.01_1206_1%
EMI@
PL702
1UH_PCMB053T-1R0MS_7A_20%
CHG_B+
+VCHGR
PQ702
AO4407AL_SO8
BATT+
PR706
4.02K_0402_1%
/BATDRV
PR720
3.3K_1206_5%~D
PQ706
2N7002KW_SOT323-3
<30> ACOFF
For DT Mode
PC701
0.1U_0603_25V7K
PR701
4.7_0402_1%
PC702
0.1U_0402_25V6
PR721
4.02K_0402_1%
PR703
4.02K_0402_1%
PR705
10_1206_5%
PC707
1U_0603_25V6K
PC710
1U_0603_25V6K
PR717
0_0402_5%~D
PR704
0_0402_5%~D
PC717
0.1U_0402_25V6
PC708
0.1U_0402_25V6
PC709
1U_0603_10V6K
PC704
10U_0805_25V6K
PC703
10U_0805_25V6K
PC706
0.1U_0603_25V7K
PC705
2200P_0402_25V7K
PC724
100U_25V_M
CSIP
CSIN
PD701
BAT54HT1G_SOD323-2~D
PU701
BQ24717
VCC
CMSRC
ACDRV
ACDET
SDA
SCL
ACOK
IOUT
CELL
ACP
ACN
REGN
BTST
HIDRV
PHASE
LODRV
GND
SRP
SRN
/BATDRV
TP
PR709
2.2_0603_5%
BST_CHGA
DH_CHG
LX_CHG
DL_CHG
PC721
0.047U_0603_25V7K
PQ703
MDU1516URH_POWERDFN56-8-5
PQ704
MDU1516URH_POWERDFN56-8-5
PQ705
SIRA14DP-T1GE3_POWERPAK-SO8-5
B+
PC718
10U_0805_25V5K~D
PC714
10U_0805_25V5K~D
Near PL701
PL701
2.2UH_FDVE1040-H-2R2M-P3_14.2A_20%
PR716
0.01_1206_1%
PC715
680P_0402_50V7K
PR722
4.7_1206_5%
PC716
10U_0805_25V5K~D
PC712
10U_0805_25V5K~D
PC713
10U_0805_25V5K~D
PC722
0.1U_0402_25V6
PC719
0.1U_0402_25V6
3S2P : CV = 13.3V CC: 1.54A
4S1P: CV = 17.7V CC: 1.1A
PC711
0.01UF_0402_25V7K
PR711
49.9K_0402_1%
PR723
324K_0402_1%
<30,36> EC_SMB_DA1
<30,36> EC_SMB_CK1
PR715
0_0402_5%~D
PR714
0_0402_5%~D
PR708
0_0402_5%~D
PR710
0_0402_5%~D
ACIN <10,30,36,49>
PR707
100K_0402_1%
PR712
158K_0402_1%
<30,36> ADP_I
PC720
100P_0402_50V8J
PC720 Close EC pin
PR713
10K_0402_1%
PC723
<30,36> BATT_TEMP
0.01U_0402_25V7K
PR724
100K_0402_1%
PQ708
2N7002KW_SOT323-3
for LEARN mode disable (pulse)

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/05/29	Deciphered Date 2014/06/01	Title: PWR_CHARGER

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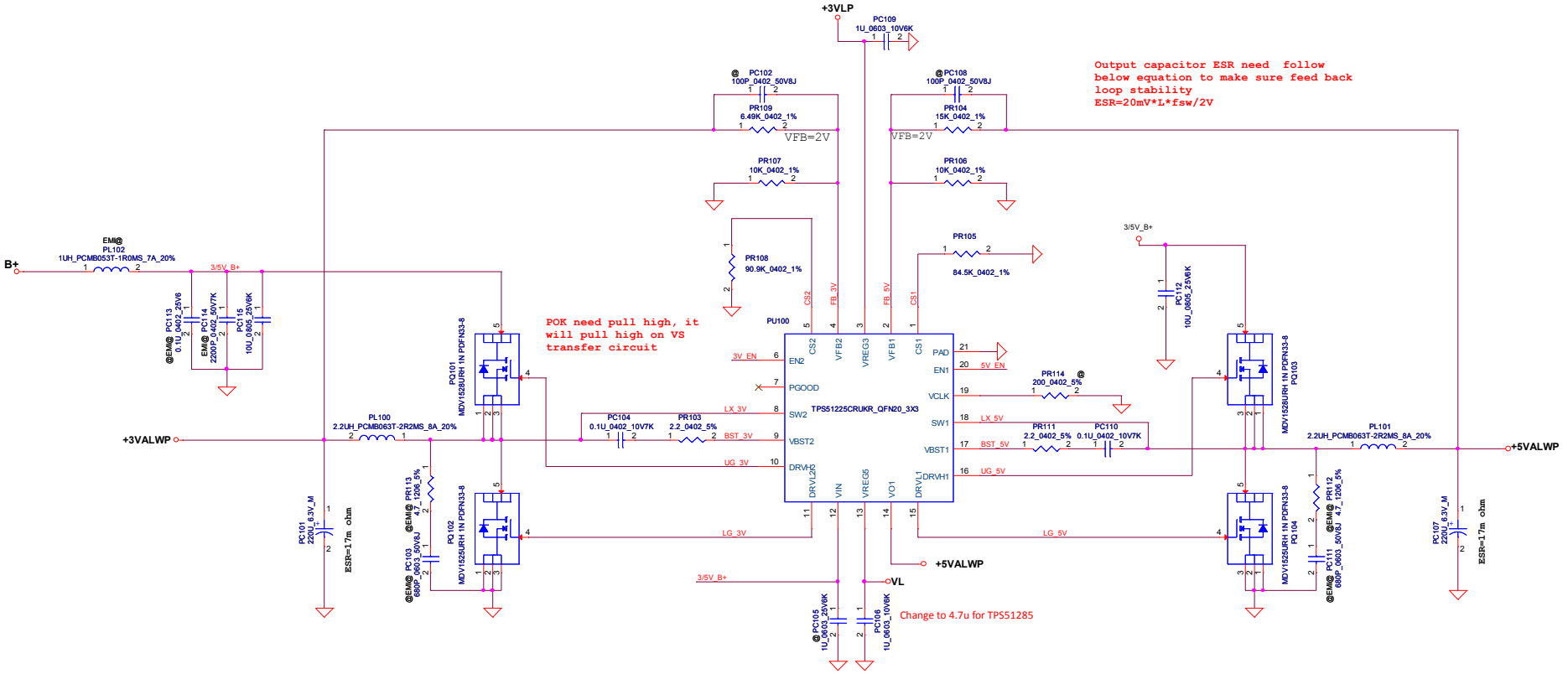
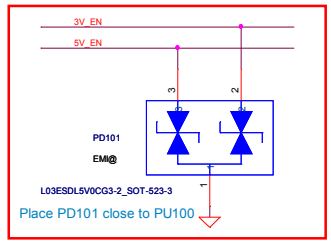
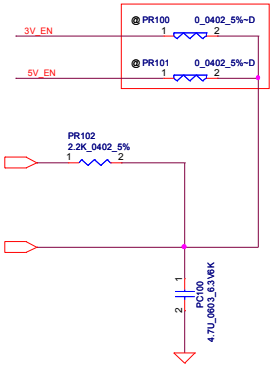
Date: Wednesday, May 29, 2013 | Sheet 37 of 57



3VALWP
TDC 5.95A
Peak Current 8.5A
OCP current 10.2A

	TYP	MAX
H/S Rds(on):	22mohm ,	30mohm
L/S Rds(on):	10.8mohm ,	13.6mohm





5VALWP
TDC 5.96A
Peak Current 8.51A
OCP current 10.2A

	TYP	MAX
H/S Rds(on):	22mohm ,	30mohm
L/S Rds(on):	10.8mohm ,	13.6mohm

Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: PWR_3.3VALWP/5VALWP

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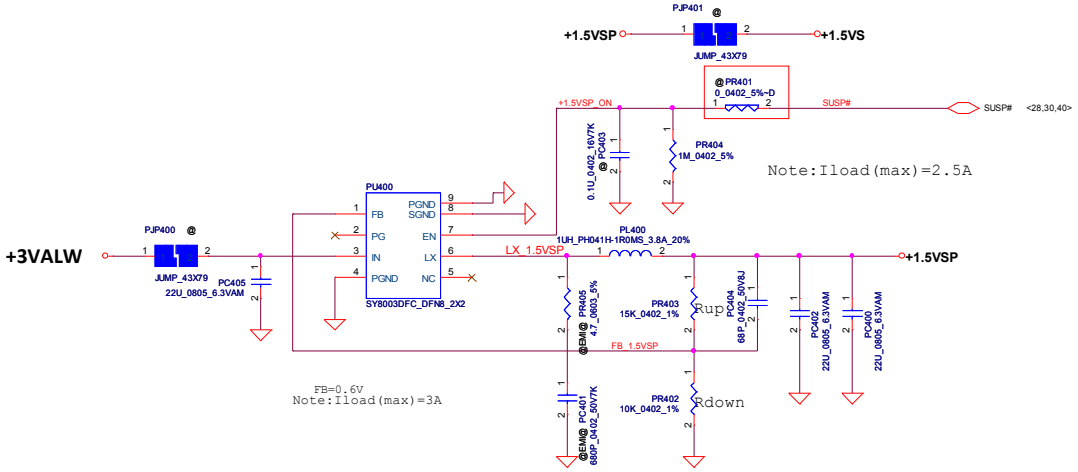
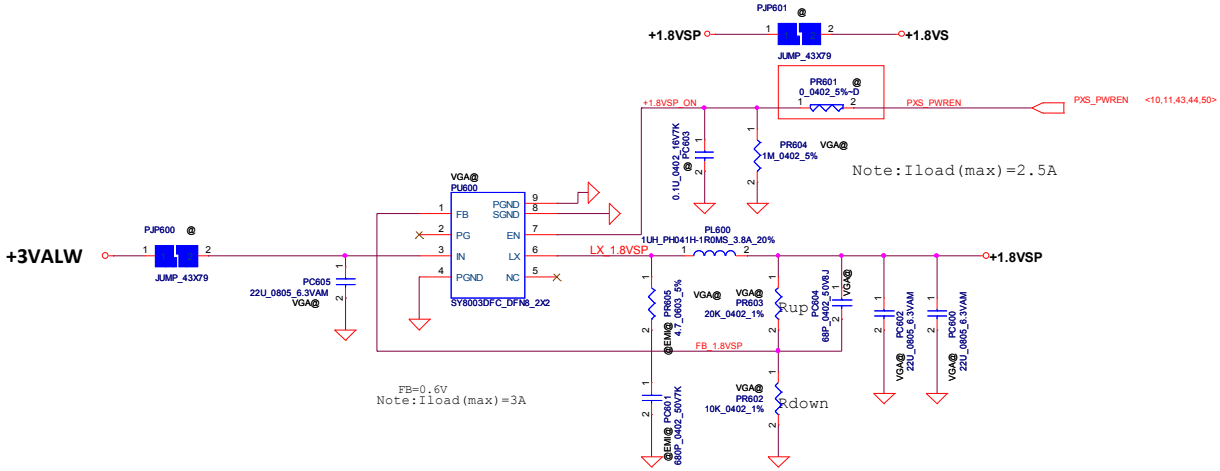




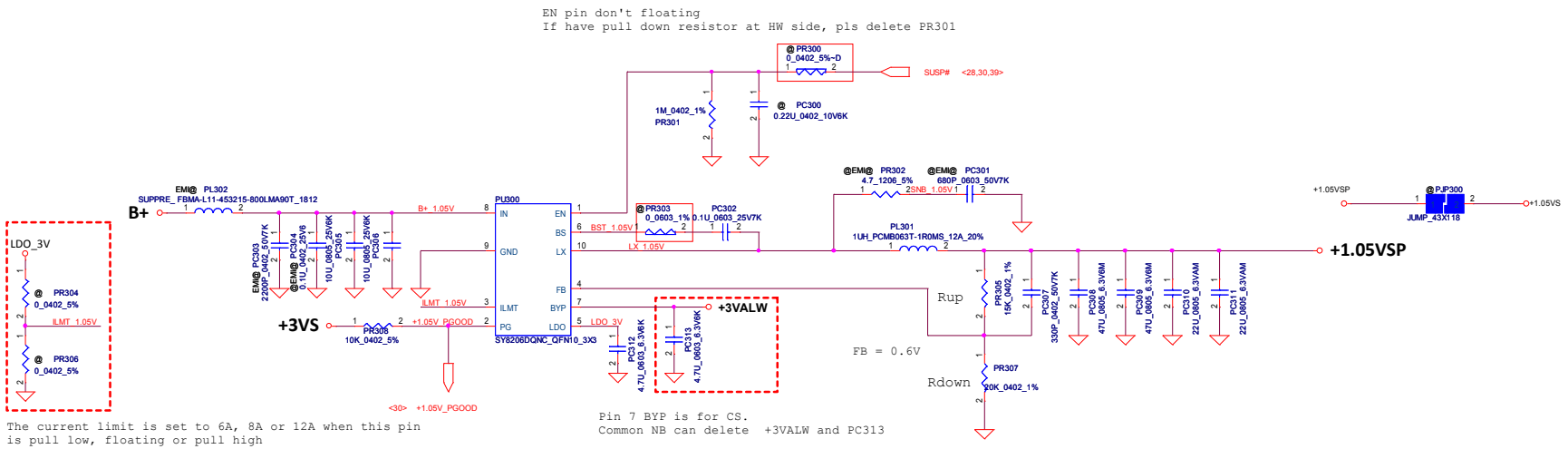
Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: PWR_1.5VSP/1.8VSP

Size: | Document Number: LA-9982P | Rev: 3.0

Date: Wednesday, May 29, 2013 | Sheet 39 of 57



Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: PWR_+VCCIO

Size: C | Document Number | Rev: 3.0

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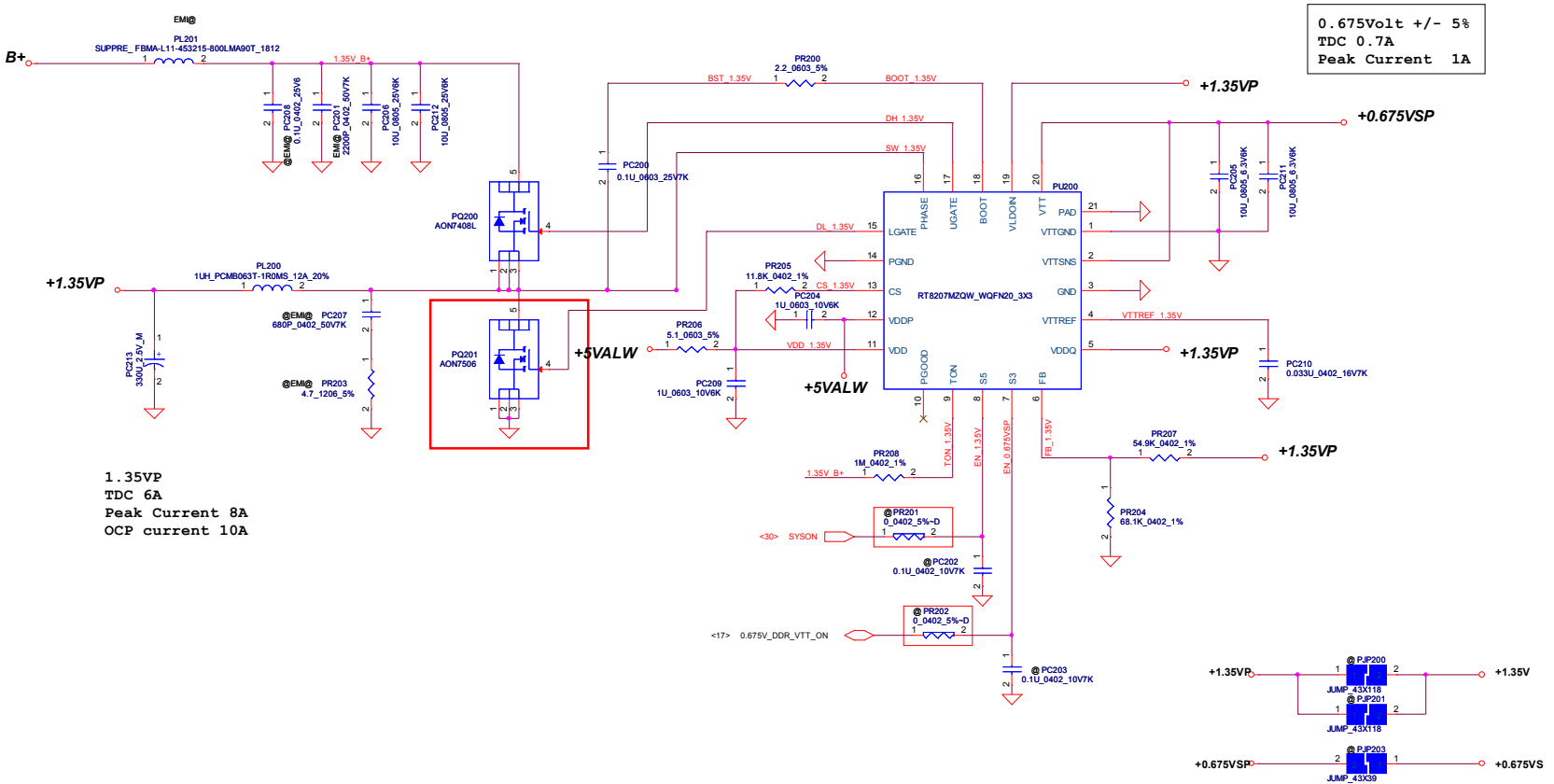

Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.		
Title	PWR_+1.35VP/0.675VSP	
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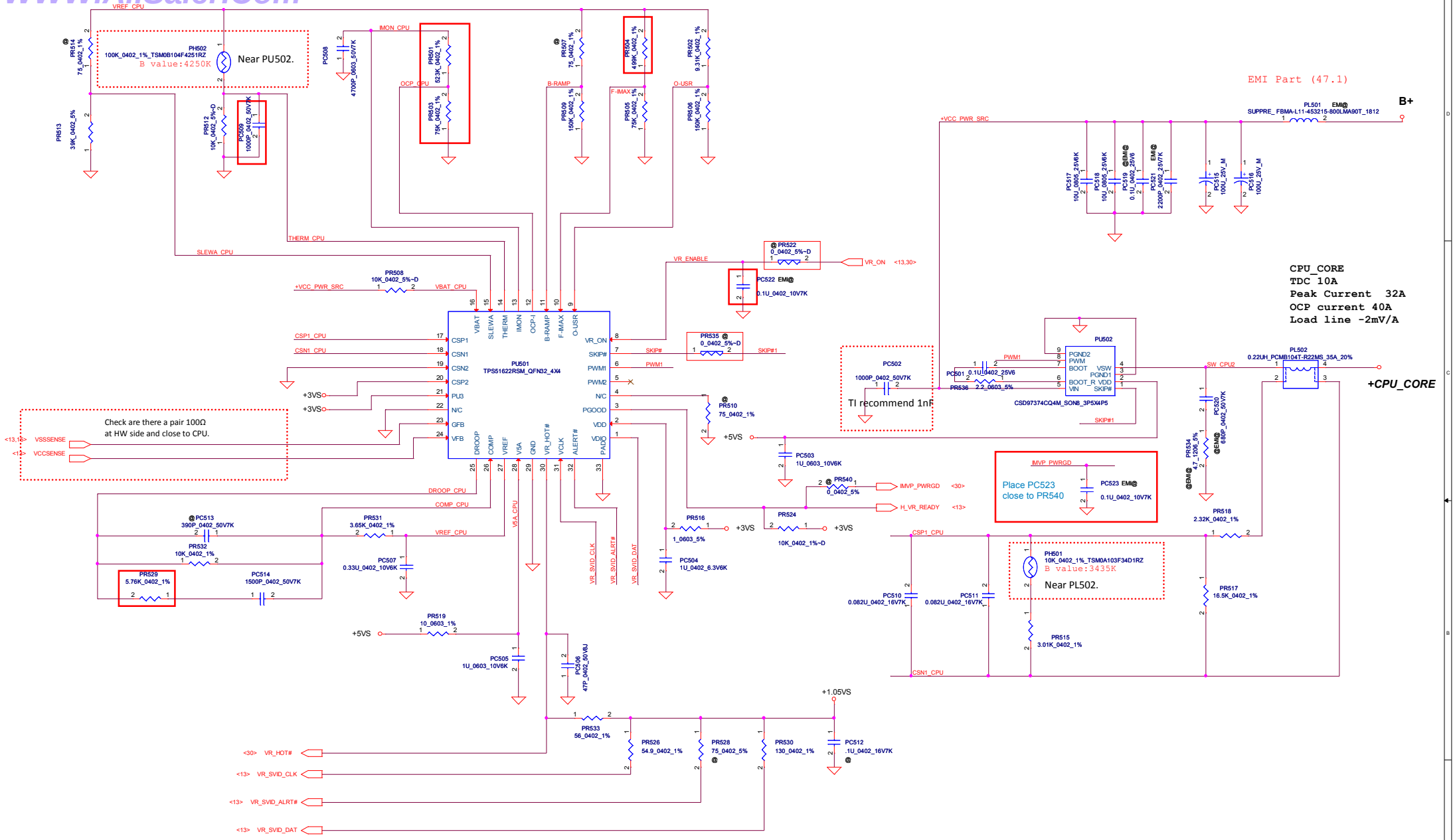

Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.			
Title: PWR_VCORE			
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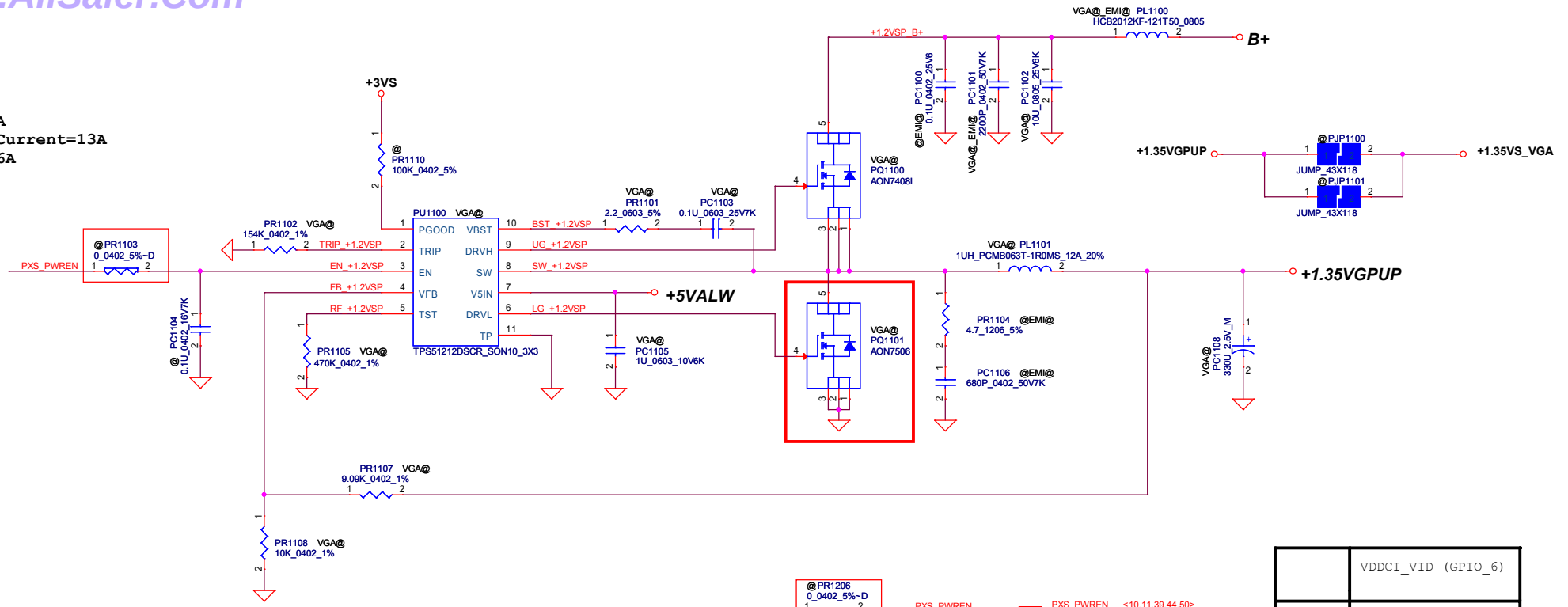
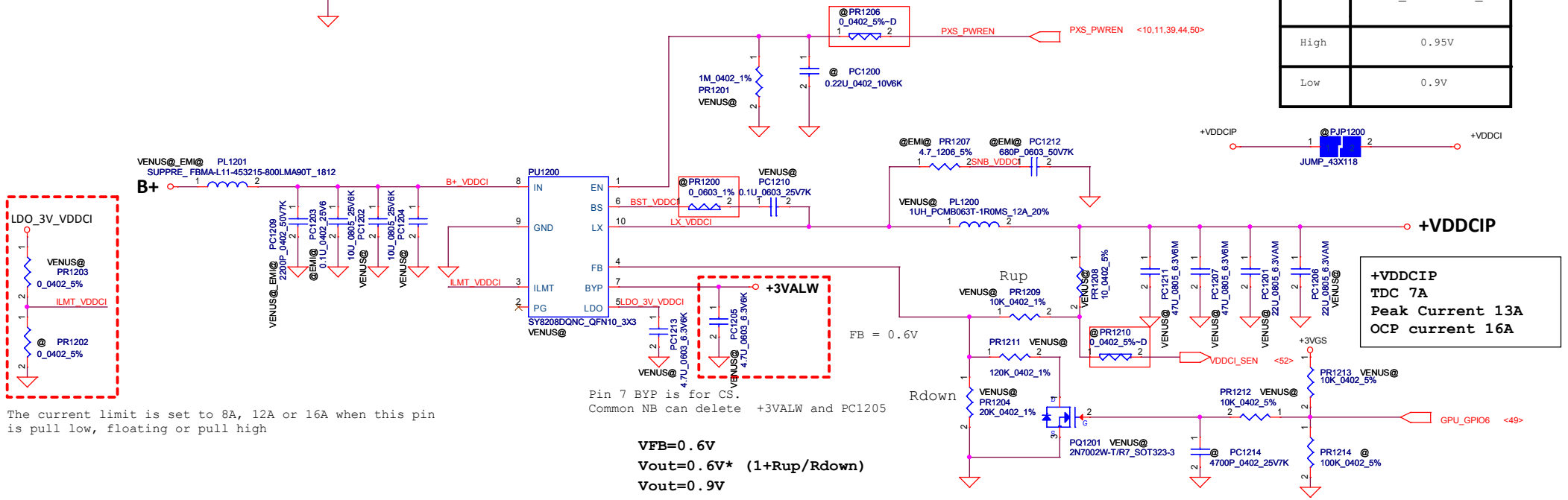
TDC=9A
Peak Current=13A
OCP=16A



	VDDCI_VID (GPIO_6)
High	0.95V
Low	0.9V



The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC1205

VFB=0.6V
Vout=0.6V* (1+Rup/Rdown)
Vout=0.9V

Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: PWR +1.35VGPU/VDDCIP

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	SUN XT	VENUS PRO/XT
Load line	No need	Need
PR824	pop	un-pop

	25W	32W
PR813	909	1.4K
PR821	97.6K	143K
PR825	976	1.5K

VGA_CORE
Frequency 300kHz
TDC 23A(25W)/33A(32W)
Peak Current 30A(25W)/47A(32W)
OCP current 36A(25W)/56A(32W)

	TYP	MAX
H/S Rds(on)	:12.2mohm ,	15mohm
L/S Rds(on)	:2.75mohm ,	3.5mohm

Choke DCR 1.1mohm(Typ)/1.3mohm(Max)
Load line : -1.5mV/A

PR813 32W@ 1.4K_0402_1%
PR821 32W@ 143K_0402_1%
PR825 32W@ 1.5K_0402_1%

GPU_VID5 (GPIO_10)	GPU_VID4 (GPIO_14)	GPU_VID3 (GPIO_15)	GPU_VID2 (GPIO_16)	GPU_VID1 (GPIO_20)	Core Voltage Level
0	1	1	0	0	1.2V
0	1	1	0	1	1.175V
0	1	1	1	0	1.15V
0	1	1	1	1	1.125V
1	0	0	0	0	1.1V
1	0	0	0	1	1.075V
1	0	0	1	0	1.05V
1	0	0	1	1	1.025V
1	0	1	0	0	1V
1	0	1	0	1	0.975V
1	0	1	1	0	0.95V
1	0	1	1	1	0.925V
1	1	0	0	0	0.9V
1	1	0	0	1	0.875V
1	1	0	1	0	0.85V
1	1	0	1	1	0.825V
1	1	1	0	0	0.8V
1	1	1	0	1	0.775V

Initial voltage:0.85V(Venus)
0.9V(Sun)

+VGA_PCIEP
TDC 3A
Peak Current 4.2A
OCP current 6A

Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.
Title: PWR_VGA_CORE/PCIE
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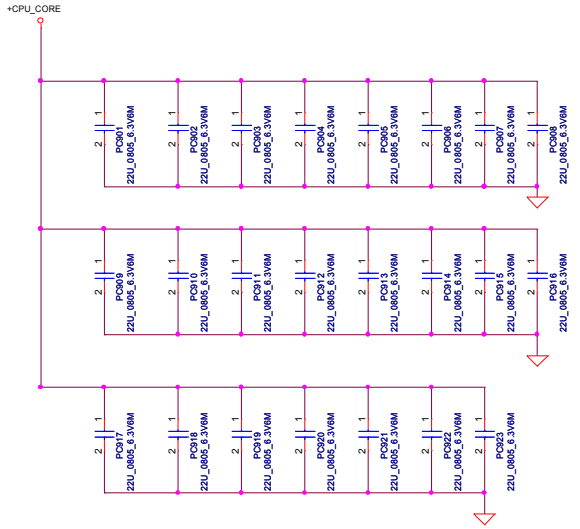

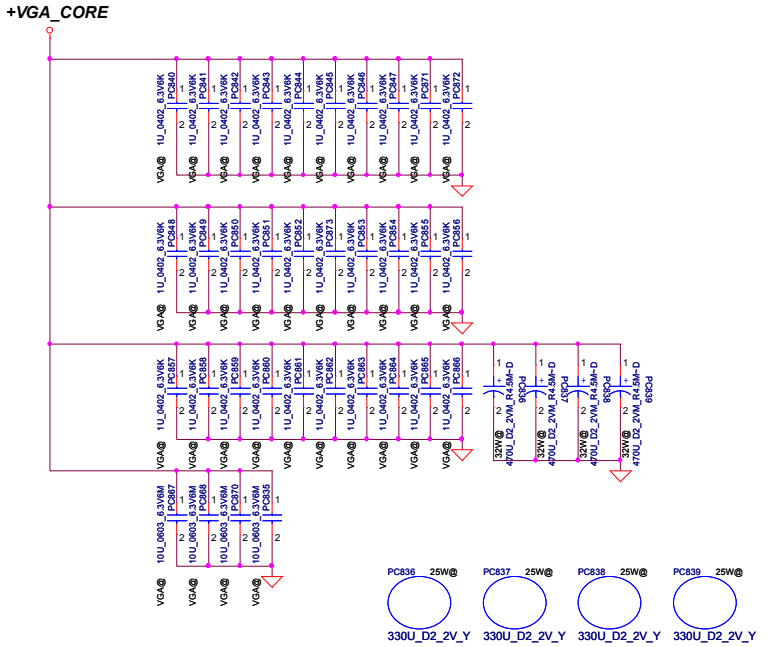

Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.	
Title	PWR_PROCESSOR DECOUPLING
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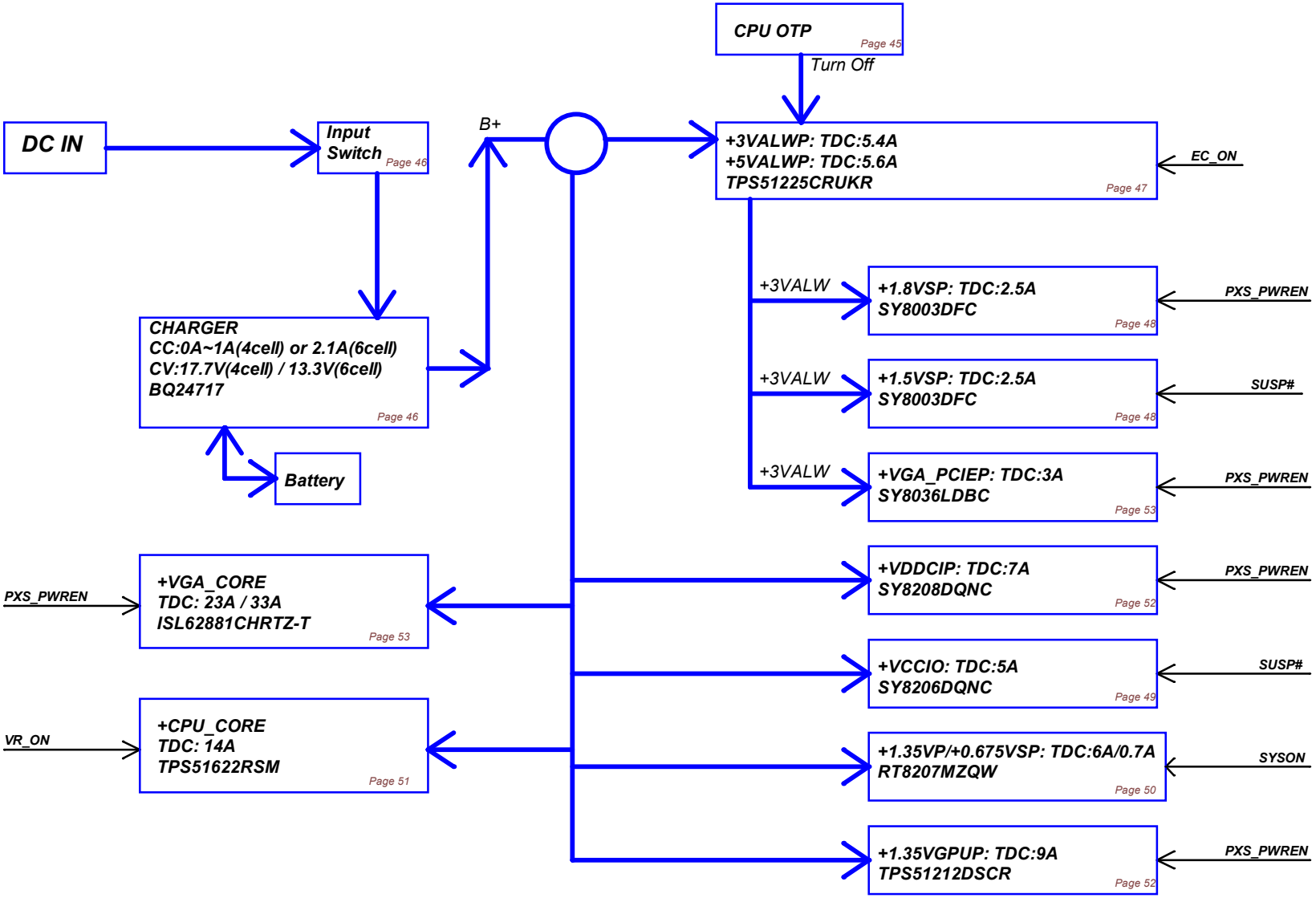
Power block



Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.			
Title	PWR_POWER BLOCK DIAGRAM		
Size	Document Number		Rev
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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	37	CHARGER	13/01/30	Morris	adjust design parameter from vendor recommend	delete PD702 change PC712 to unpop change PQ704 to unpop change PC707 from 0.1uF_0402 to 1uF_0603 change PC720 from 0.1uF to 100pF change PC711 from 1000pF to 0.01uF change PQ705 from SB00000SD00 to SB00000WY00	0.3
2	42	VCORE	13/01/30	Morris	adjust design parameter from vendor recommend	change PC509 from 0.1uF to 1000pF change PR529 from 3.83K to 5.76K change PR504 from 523K to 499K	0.3
3	36	DCIN/BATT CONN/OTP	13/01/30	Morris	change from ESD request	change PD1 from SC300002E00 to SC300001G00	0.3
4	38	3.3VALWP/5VALWP	13/02/01	Morris	add ESD diode from ESD request	add PD101(SCA00002A00)	0.3
5	42	VCORE	13/02/21	Morris	adjust design parameter from fine tune result	change PR501 from 422K to 523K change PR503 from 56K to 75K	0.3
6	44	VGA_CORE/PCIE	13/02/21	Morris	unpop from EE request	unpop PR808	0.3
7	44	VGA_CORE/PCIE	13/03/05	Morris	adjust output voltage from vender request	unpop PR826 and pop PR834 (only for Sun XT)	0.4
8	37 38 39 40 41 42	CHARGER 3.3VALWP/5VALWP 1.5VSP/1.8VSP +VCCIO +1.35VP/0.675VSP VCORE	13/03/28	Morris	verify function ok, so delete 0 ohm to short	unpop PR100,PR101,PR201,PR202,PR300,PR303,PR401,PR522,PR535, PR704,PR708,PR710,PR714,PR715,PR717	1.0
9	36	DCIN/BATT CONN/OTP	13/04/09	Morris	design change for solve issue	unpop PR1 and PC5	2.0
10	41 43	+1.35VP/0.675VSP +1.35VGPU/VDDCI	13/04/09	Morris	part shortage issue	change PQ201 and PQ1101 from SB00000T600 to SB000010A00	2.0
11	39 43 44	1.5VSP/1.8VSP +1.35VGPU/VDDCI VGA_CORE/PCIE	13/04/09	Morris	verify function ok, so delete 0 ohm to short	unpop PR601,PR802,PR803,PR814,PR823,PR830,PR845,PR846, PR1103,PR1200,PR1206,PR1210	2.0
12	43	+1.35VGPU/VDDCI	13/04/09	Morris	unpop VDDCI parts from vendor recommend and EEverify ok only for Sun XT	unpop PL1200,PL1201,PU1200,PQ1201,PR1201,PR1203,PR1204,PR1208,PR1209, PR1211,PR1212,PR1213,PC1201,PC1202,PC1204,PC1205,PC1206,PC1207, PC1209,PC1210,PC1211,PC1213 (only for Sun XT)	2.0
13	44	VGA_CORE/PCIE	13/04/12	Morris	part shortage issue	change PL1300 from SH00000GQ00 to SH00000PK00	2.0
14	36	DCIN/BATT CONN/OTP	13/04/12	Morris	customer request	add PR2 10Kohm	2.0
15	42	VCORE	13/04/15	Morris	EMI request	pop PC522 and add PC523 0.1uF	2.0
16	36	DCIN/BATT CONN/OTP	13/05/22	Morris	reserve parts from ESD request	reserve PD2,PD3,PR17 and unpop PR17	3.0

Compal Electronics, Inc.			
Title	PWR-PIR		
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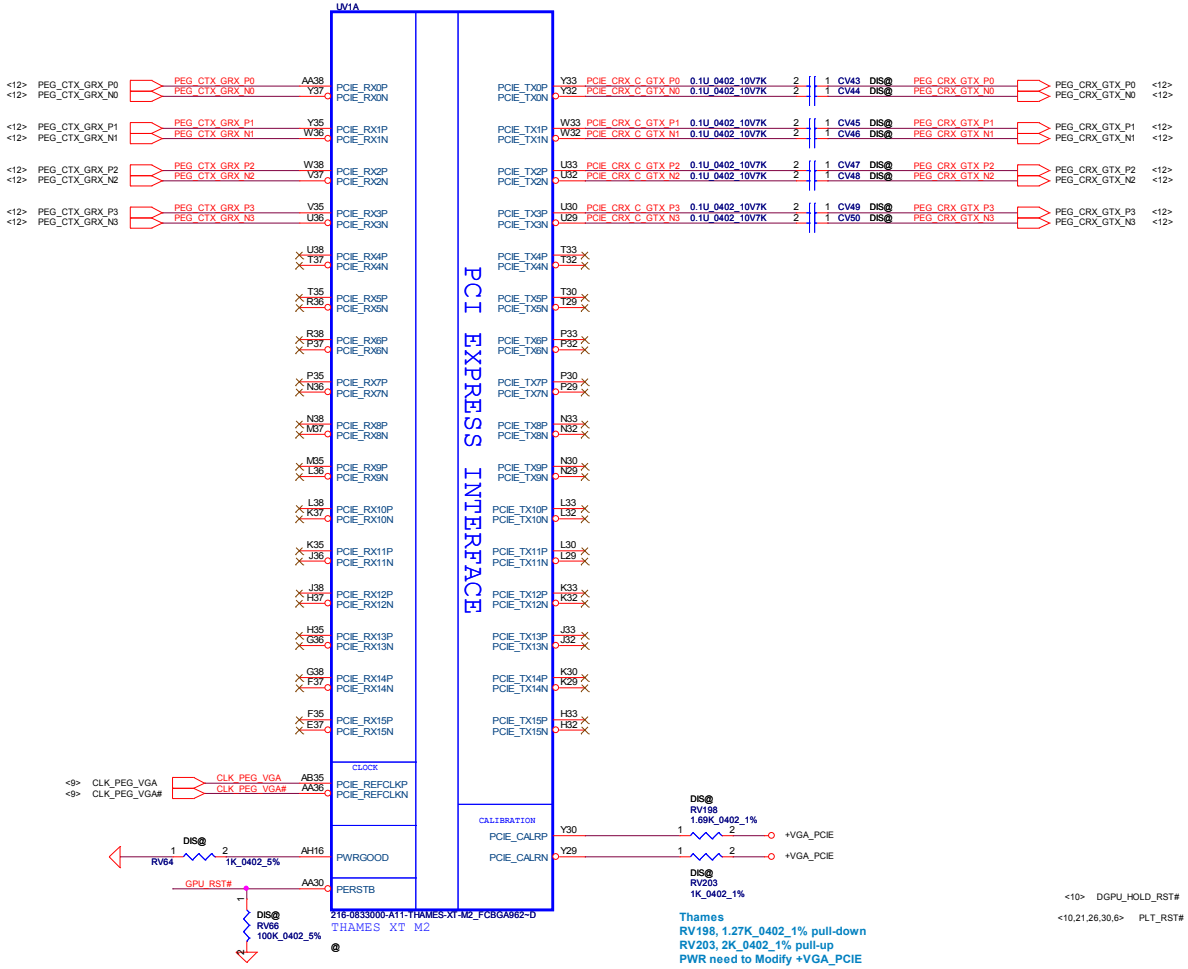
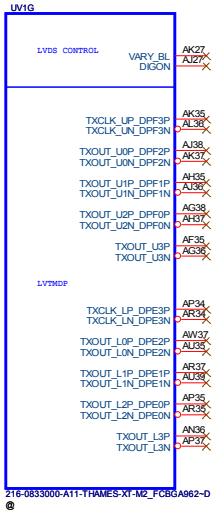
GFX PCIE LANE REVERSAL

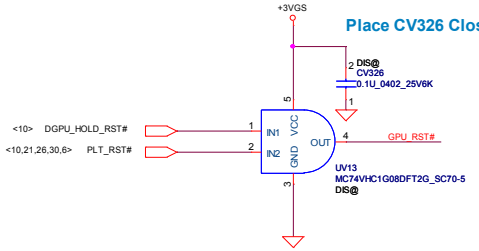


Thames
RV198, 1.27K_0402_1% pull-down
RV203, 2K_0402_1% pull-up
PWR need to Modify +VGA_PCIE

LVDS Interface



Place CV326 Close to UV13



UV1 VENUSXT@

216-0846000 A1 VENUS XT M2 FCBGA 962P 0FD

SA00006KW0L

UV1 VENUSPRO@

216-0846009 A1 VENUS PRO M2 FCBGA 962P 0FD

SA00006MW0L

Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.	
Title	ATI_Venus Pro_M2_PCIE/LVDS
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CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0: 50% swing 1: Full swing X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS	0: disable 1: enable X
RSVD	GPIO2	Advertises PCIE speed when compliance test	0: 2.5GT/s 1: 5GT/s 0
RSVD	GPIO8	RESERVED	0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0: disable 1: enable X
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XXX
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD	H2SYNC		0
RSVD	GENERICC		0
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET

GPIO21	H2SYNC	GENERICC	GPIO2	GPIO8

TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50%Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Defailt setting for desktop)

Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2
128Mx16bits (64Mx32bits) GDDR5 Hynix 2Gb SA00004GD1L(R1) SA00004GD2L(R3)	RV67 1	RV69 1	RV71 1
128Mx16bits (64Mx32bits) GDDR5 Samsung 2Gb SA00005B70L(R1) SA00005B71L(R3)	RV68 0	RV69 1	RV71 1
	RV67 1	RV70 0	RV71 1
128MX16bits DDR3 Hynix 2Gb SA00006H40L(R1) SA00006H41L(R3)			
128MX16bits DDR3 Samsung 2Gb SA00005SH0L(R1) SA00005SH1L(R3)			
128MX16bits DDR3 Micron 2Gb SA00005XB0L(R1) SA00005XB1L(R3)			

SUN MLPs PS_3	RV241	RV242	Bits [3:1]
Hynix	NC	4.75k	000
Samsung	8.45k	2k	001
Micron	4.75k	NC	111

VENUS MLPs
PS_3 used default

STRAPS

For DGPU output display Debug (For Venus ASIC)

For DGPU output display Debug (For Venus ASIC)

VGA Thermal Sensor SMB

SUN internal VGA Thermal Sensor
Address 0x714

External Thermal Sensor EMC1402-2-ACZL-TR

Closed to GPU

Address:100_1101b
Main : SA00001Z710
2nd : SA00003PU00

NC_TSVSSQ should be tied to GND

0.60 V level, Please VREFG Divider ans cap close to ASIC

XTALIN Voltage Swing: 1.8 V

Add 12/6 for MLPS

For GCLK

Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

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Compal Electronics, Inc.

Title: ATI_Venus Pro_M2_Main_MSIC

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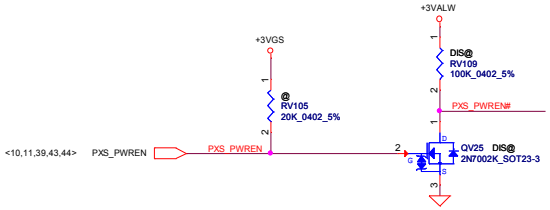
PX_MODE=1 for Normal Operation
PX_MODE=0 for BACO mode to shut down power rails expcept VDDR3,PCIE_VDDC and 1.8V rail

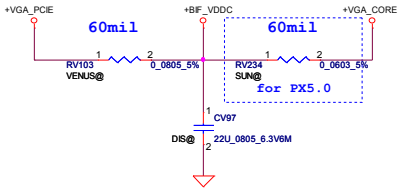
Note:

PX4.0 +VGA_CORE,VDDCI,+1.5VGS ON
PX4.0 +3VGS, +1.0VGS,+1.8VGS OFF
PX5.0 +3VGS,+VGA_CORE,VDDCI,+1.5VGV,+1.0VGS,+1.8VGS OFF

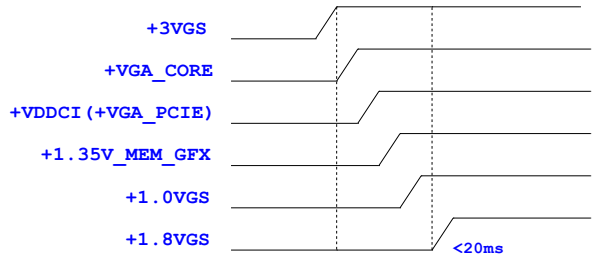


for PX4.0 and PX5.0

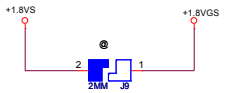
Switch circuits in BACO desingns for Thames/Seymour only 55mA@1.0V, in BACO mode



Power seguence of Sun XT,Venus Pro,Venus XT

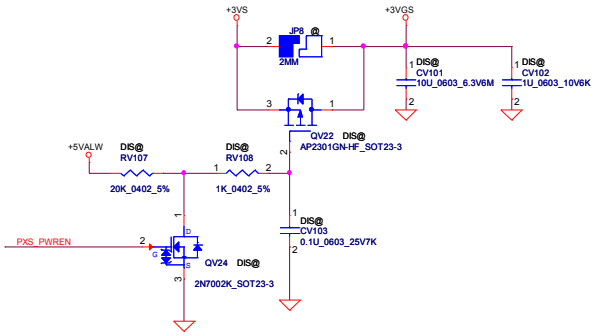


+1.8VS TO +1.8VGS

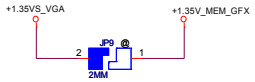


SHORT DEFAULT

+3VS TO +3VGS



+1.35VS_VGA TO +1.35V_MEM_GFX



SHORT DEFAULT

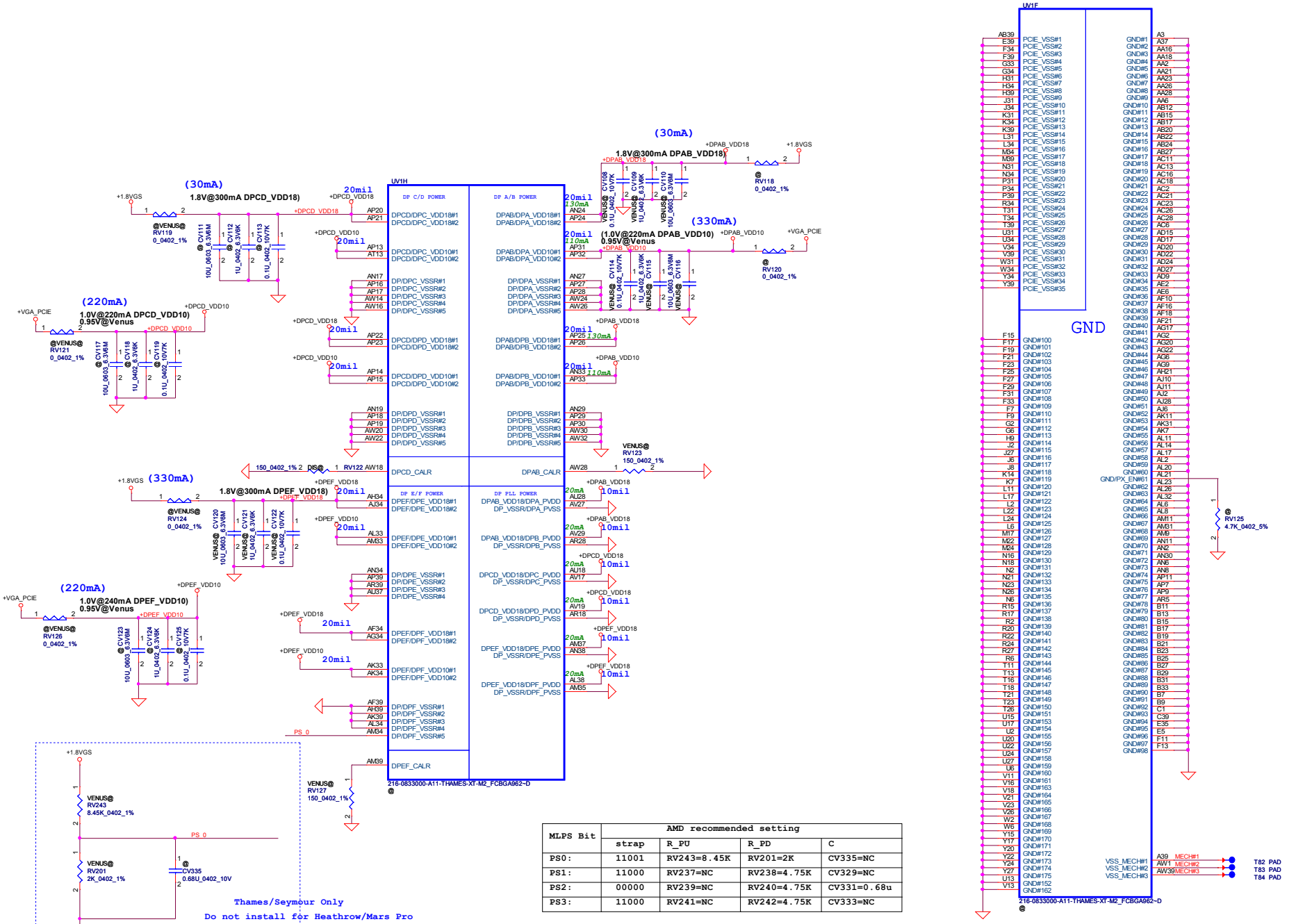
Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: ATI_Venus Pro_M2_BACO POWER

Size	Document Number	Rev
	LA-9982P	3.0

Date: Wednesday, May 29, 2013 Sheet 50 of 57



MLPS Bit	AMD recommended setting			
	strap	R_PU	R_PD	C
PS0:	11001	RV243=8.45K	RV201=2K	CV335=NC
PS1:	11000	RV237=NC	RV238=4.75K	CV329=NC
PS2:	00000	RV239=NC	RV240=4.75K	CV331=0.68u
PS3:	11000	RV241=NC	RV242=4.75K	CV333=NC

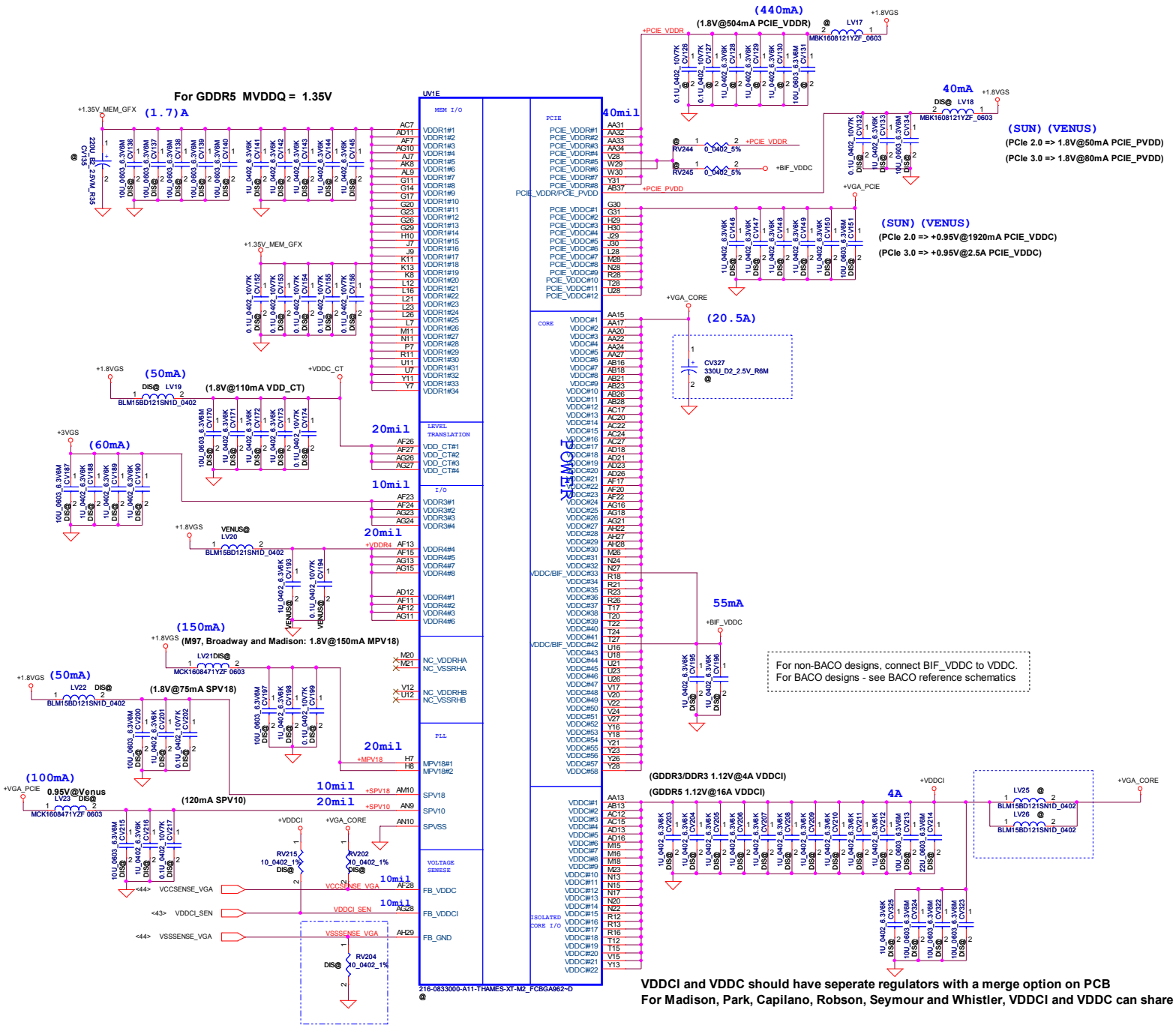
Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: ATI_Venus Pro_M2_PWR_GND

Size: | Document Number: LA-9982P | Rev: 3.0

Date: Wednesday, May 29, 2013 | Sheet 51 of 57



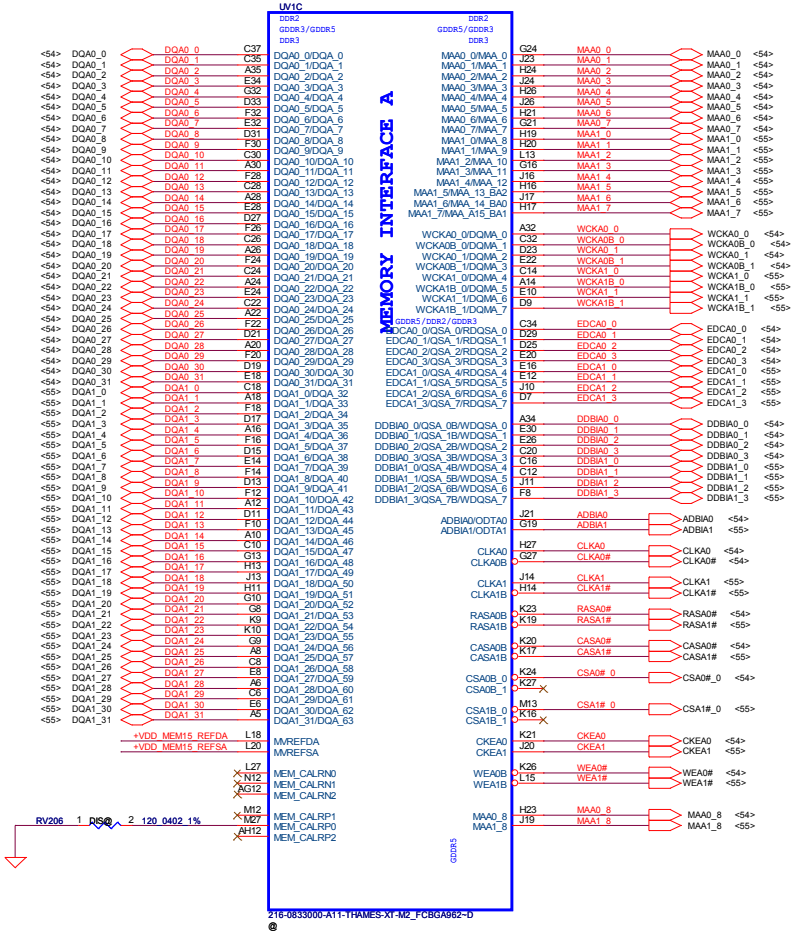
Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: ATI_Venus Pro_M2_Power

Size	Document Number	Rev
	LA-9982P	3.0

Date: Wednesday, May 29, 2013 Sheet 52 of 57

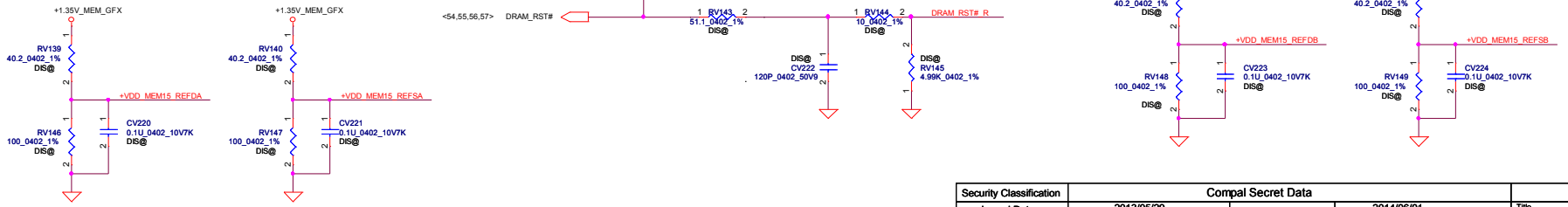


GDDR5 CMD Mapping Table

<0..31>	<32..63>	Memory
CMD12	CMD28	RAS#
CMD15	CMD31	CAS#
CMD5	CMD20	WE#
CMD0	CMD16	CS#
CMD8	CMD24	ABI#
CMD10	CMD26	A0_A10
CMD11	CMD27	A1~A9
CMD2	CMD18	A2~BA0
CMD1	CMD17	A3~BA3
CMD3	CMD19	A4~BA2
CMD4	CMD20	A5~BA1
CMD7	CMD23	A6~A11
CMD6	CMD22	A7~A8
CMD9	CMD25	A1Z_FRU
CMD14	CMD30	CKE#
CMD13	CMD29	RESET#

This basic topology should be used for DRAM_RST for DDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.
Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

route 50ohms single-ended/100ohms diff and keep short
Debug only, for clock observation, if not needed, DNI 5mil 5mil



Security Classification	Compal Secret Data		
Issued Date	2013/05/29	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: ATI_Venus Pro_M2_MEM IF

Size	Document Number	Rev
	LA-9982P	3.0

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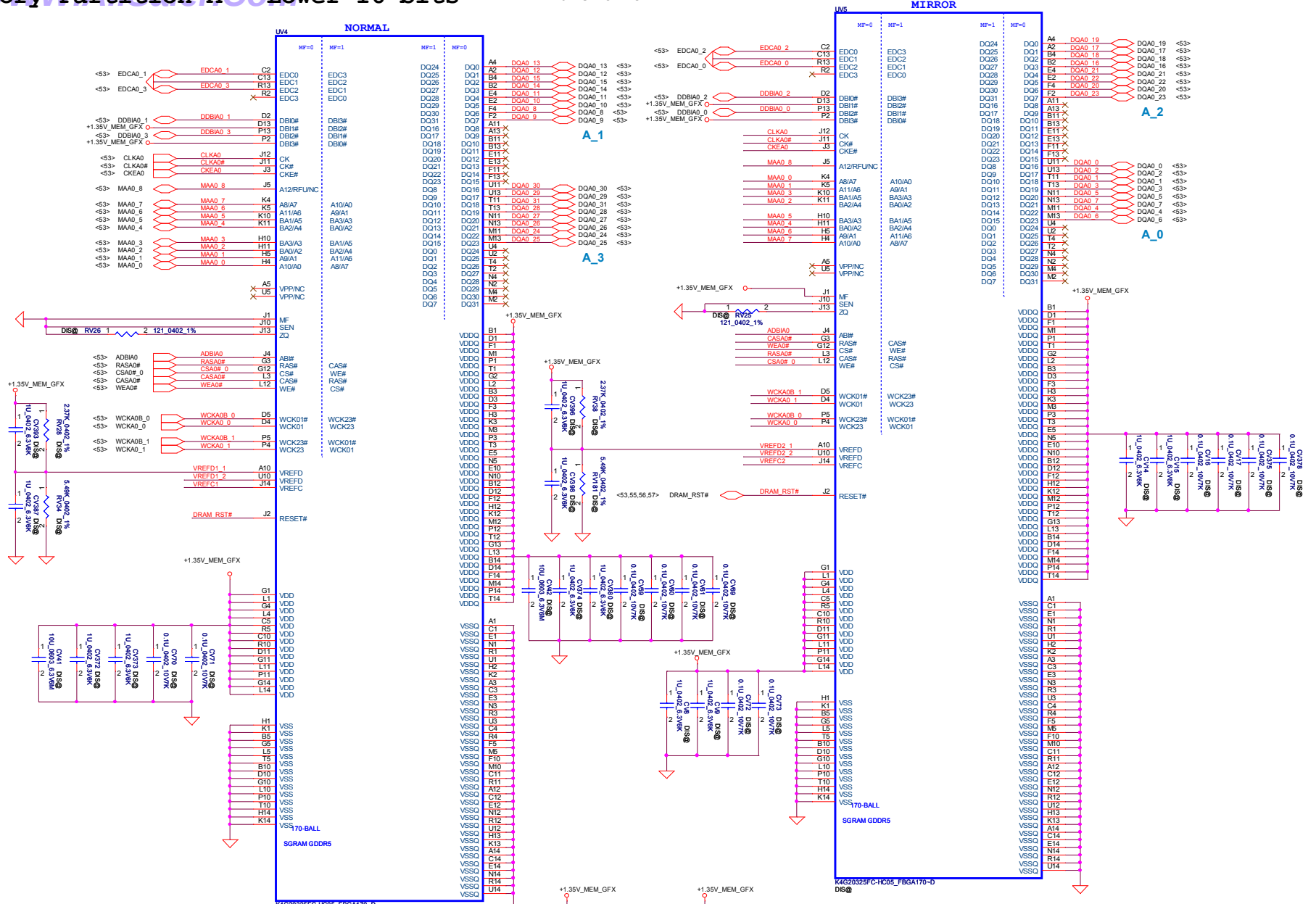
Memory Partition A - Lower 16 bits

64X32 GDDR5



Compal Electronics, Inc.	
Title	VRAM_A Lower_UV4,UV5
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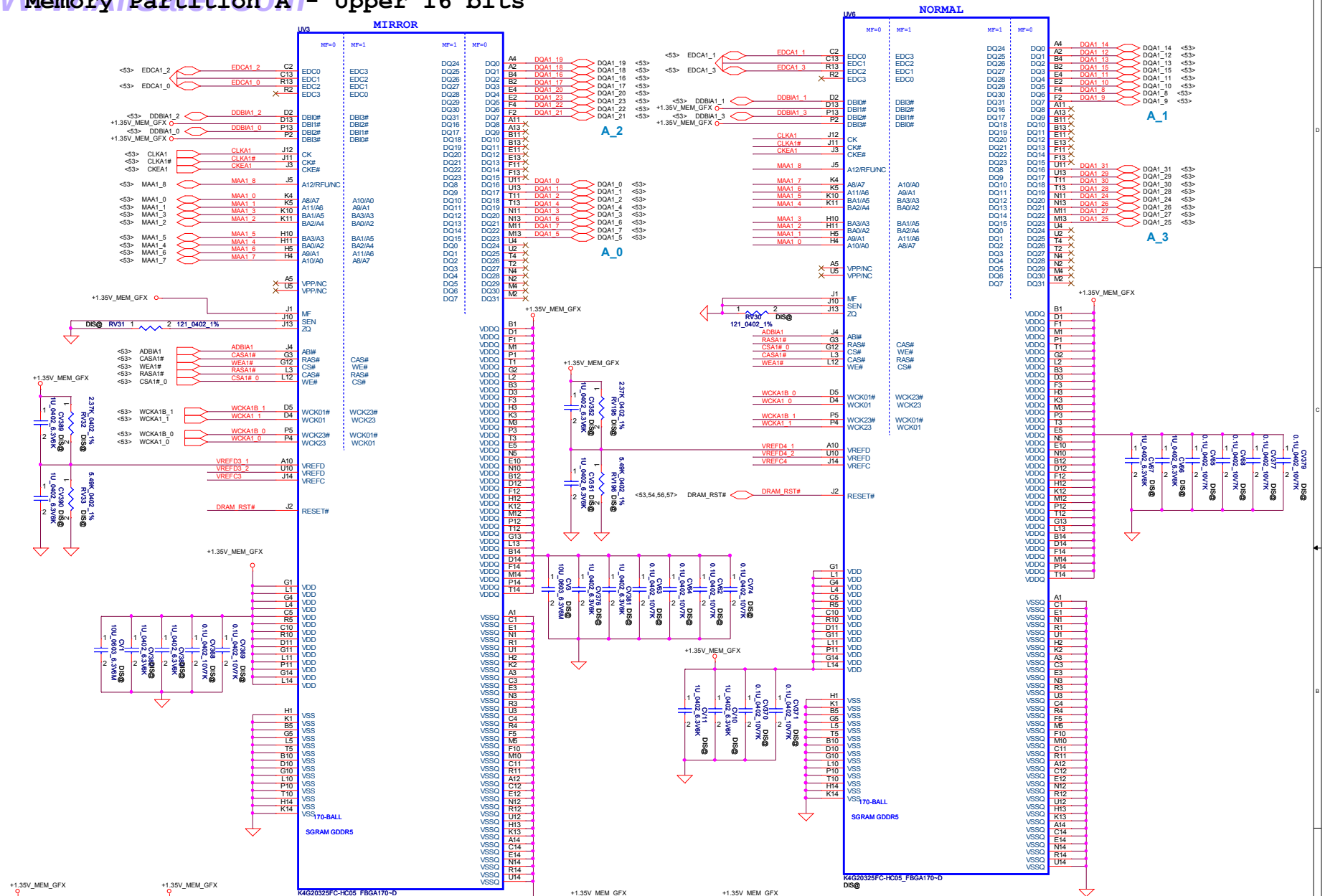
Memory Partition A - Upper 16 bits



Compal Electronics, Inc.

Title: MARX-VRAM_A Upper_UV3,UV6

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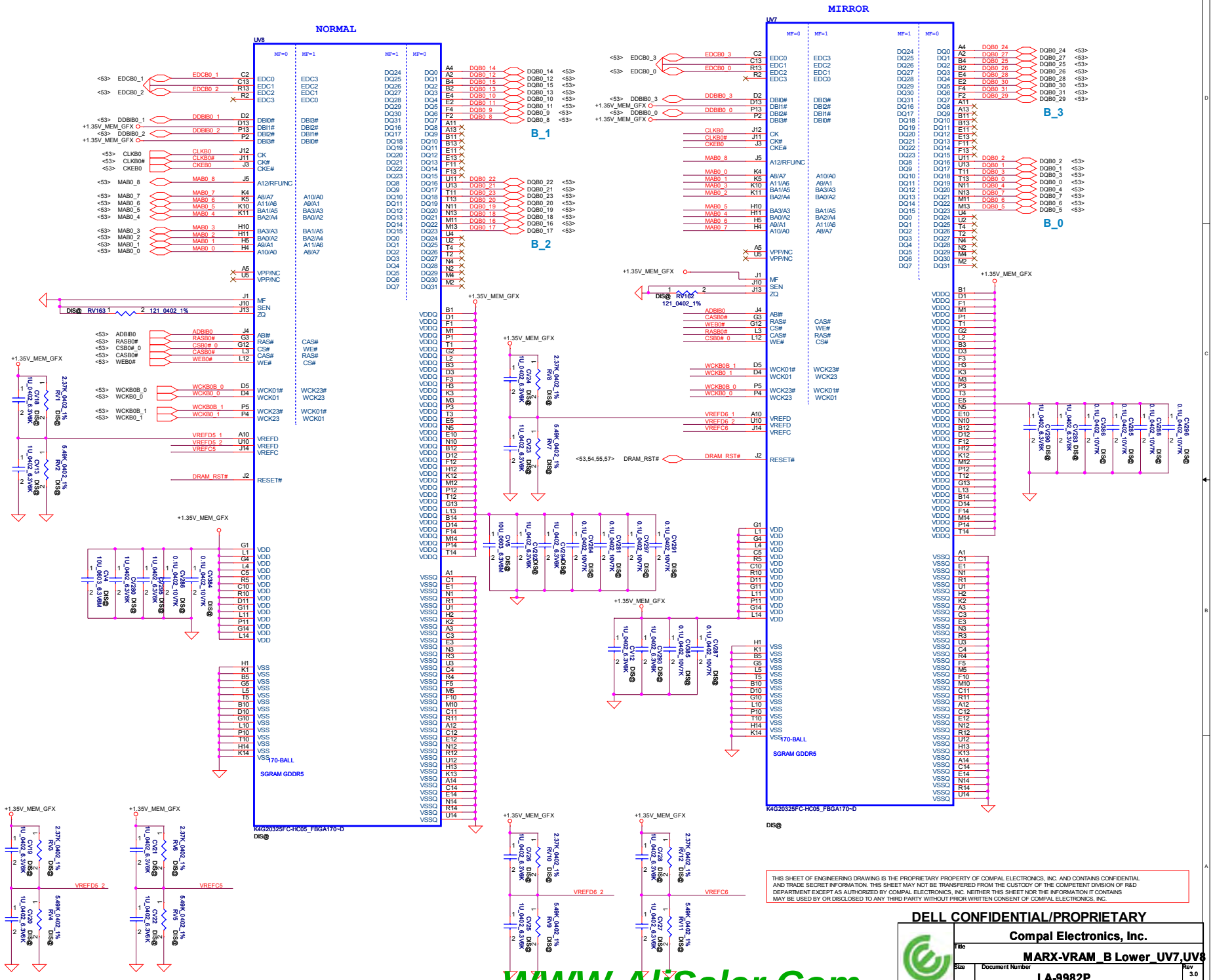
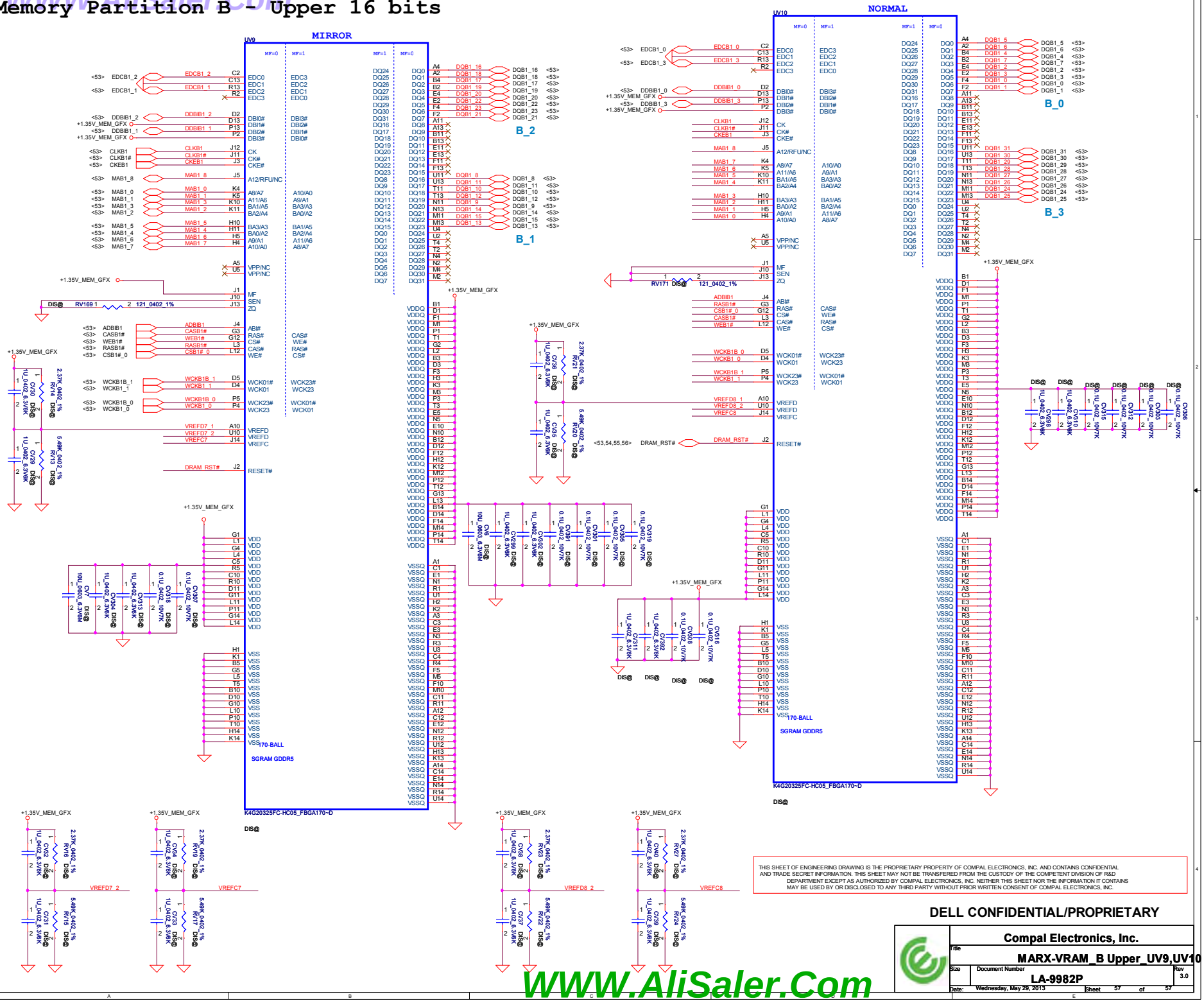
Memory Partition B - Lower 16 bits



Memory Partition B - Upper 16 bits



Compal Electronics, Inc.	
Title	MARX-VRAM_B Upper_UV9,UV10
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