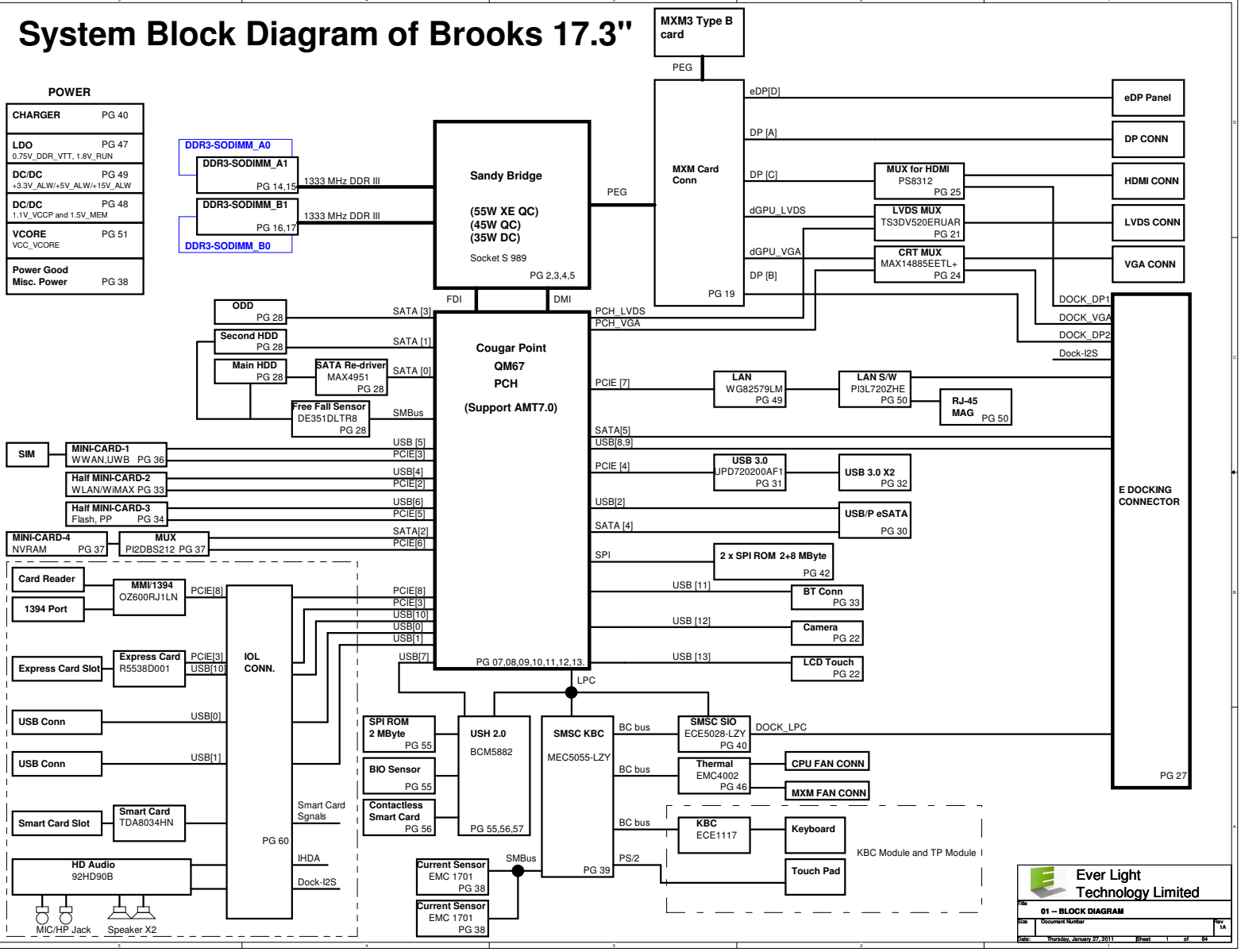
System Block Diagram of Brooks 17.3"



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File	01 -- BLOCK DIAGRAM	
Size	Document Number	Rev 1A
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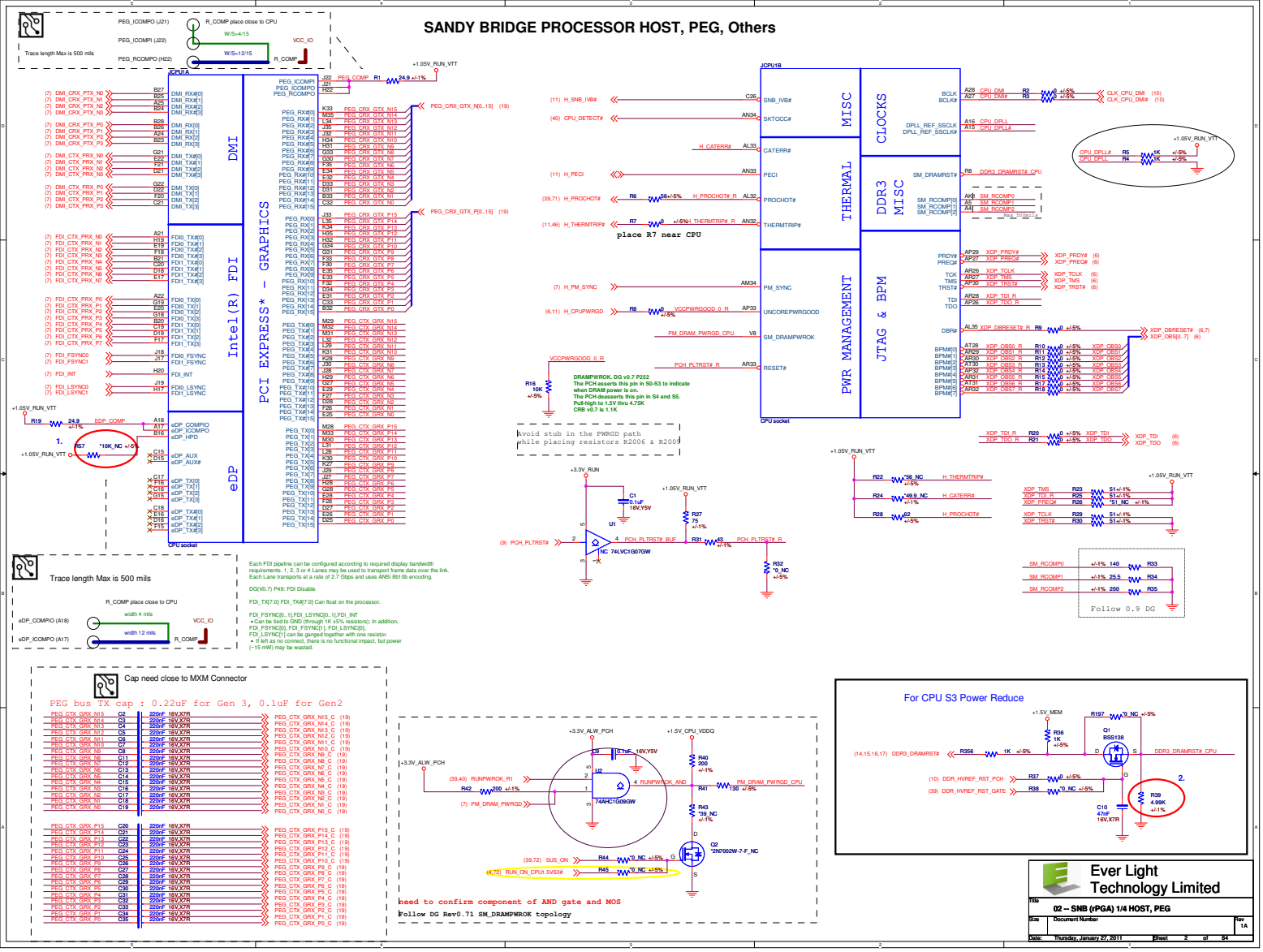
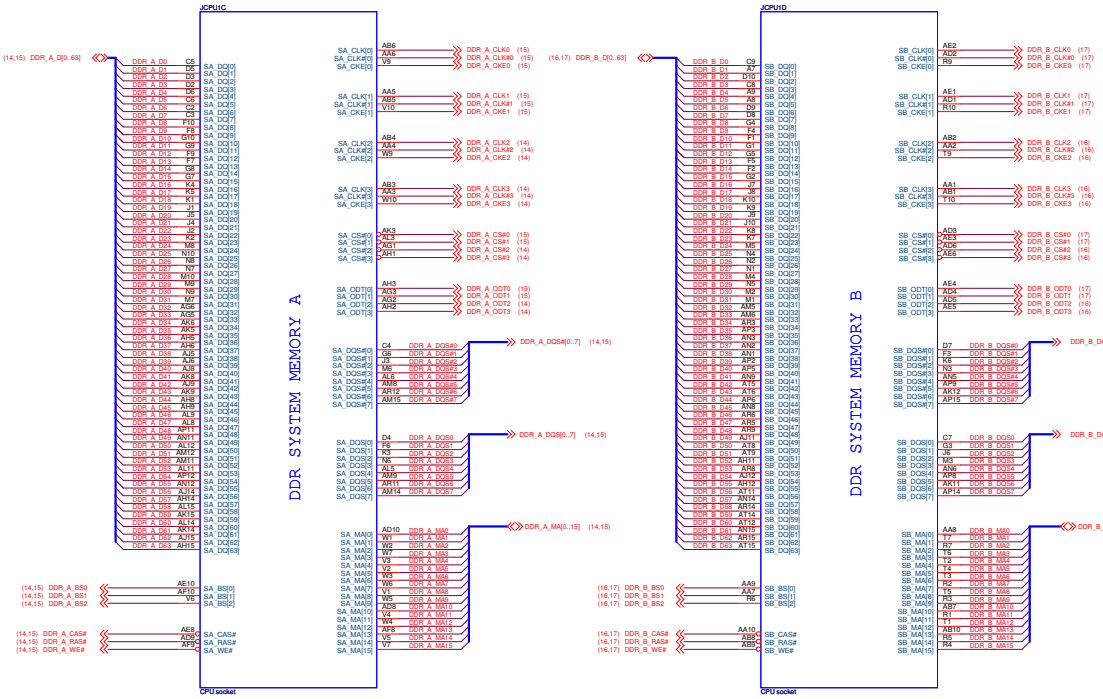
SANDY BRIDGE PROCESSOR HOST, PEG, Others



SANDY BRIDGE PROCESSOR (DDR3)



Ever Light Technology Limited	
Title	03 -- SNB (rPGA) 2/4 DDR
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SANDY BRIDGE PROCESSOR (POWER)

SANDY BRIDGE PROCESSOR (GRAPHICS POWER)

POWER

JCPU1F

CPU socket

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

POWER

JCPU1G

SENSE LINES

VAXG_SENSE (71)
VSSAXG_SENSE (71)

VREF

SM_VREF

DDR3 -1.5V RAILS

SA RAIL

1.8V RAIL

MISC

GRAPHICS

CPU socket

22uF x 16
470uF x 2 on VR side

+V_SM_VREF should have 10 mil trace width.

10uF x 6
330uF x 1

10uF x 2, NC x 2

For CPU S3 Power Reduce

Power page :
22uF x 3
EE page :
330uF x 1, NC x 1
22uF x 12, NC x 7

Intel DG :
330uF x 2 near CPU
22uF x 5, NC x 5 Bottom Socket Cavity
22uF x 7, NC x 2 Top Socket Cavity
for 2012 capable designs
330 µF x3

CPU Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	0.65~1.3	53
VCCIO	1.05	8.5
VAXG	0.0~1.1	26
VCCPLL	1.8	3
VDDQ	1.5	5
VCCSA	0.65~0.9	6
+1.5V_MEM	1.5	12~16 *

* Description
5A to Mem controller(+1.5V_CPU_VDDQ)
5~6A to 2 DIMMs/channel
2~5A to +1.5V_RUN & +0.75V_DDR_VTT

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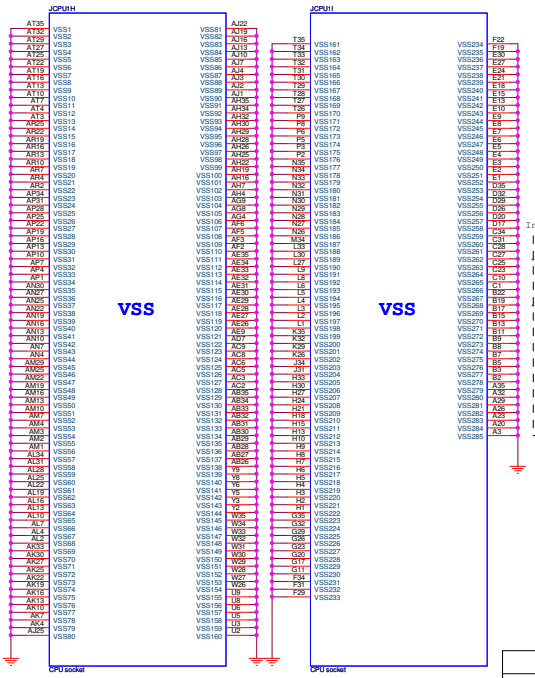
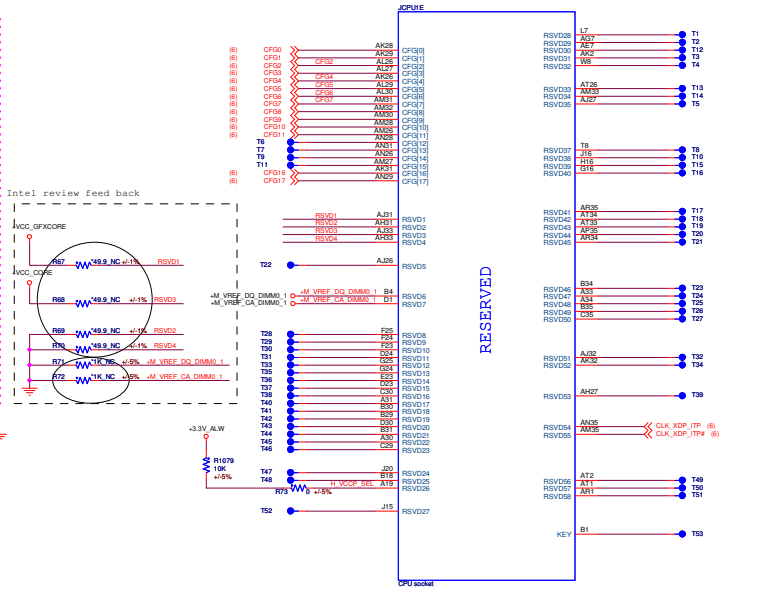
Title	04 – SNB (rPGA) 3/4 POWER		
Size	Document Number		Rev 1A
Date:	Thursday, January 27, 2011	Sheet 4 of 84	

SANDY BRIDGE PROCESSOR (GND)



SANDY BRIDGE PROCESSOR(RESERVED, CFG)



	1	0
CFG2 (PEG Static Lane Reversal)	Lan# definition matches socket pin map definition (Default Value)	Lan Reversed
CFG4 (Display Port Presence strap)	Disabled; No Physical Display Port attached to Embedded Display Port (Default Value)	Enabled; An external Display port device is connected to the Embedded Display port
CFG[6:5]		
CFG7 (PEG Defer Training)	PEG Train immediately following xxRESETB de assertion (Default Value)	PEG Wait for BIOS for training

CFG[6:5] (PCIe Port Bifurcation Straps)	11	x16 - Device 1 functions 1 and 2 disable (Default Value)
	10	x8, x8 - Device 1 function 1 enable; function 2 disable
	01	Reserved - (Device 1 function 1 disable; function 2 enable)
	00	x8, x8, x4 - Device 1 function 1 and 2 enable

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Title	05 -- SNB (rPGA) 4/4(GND)	
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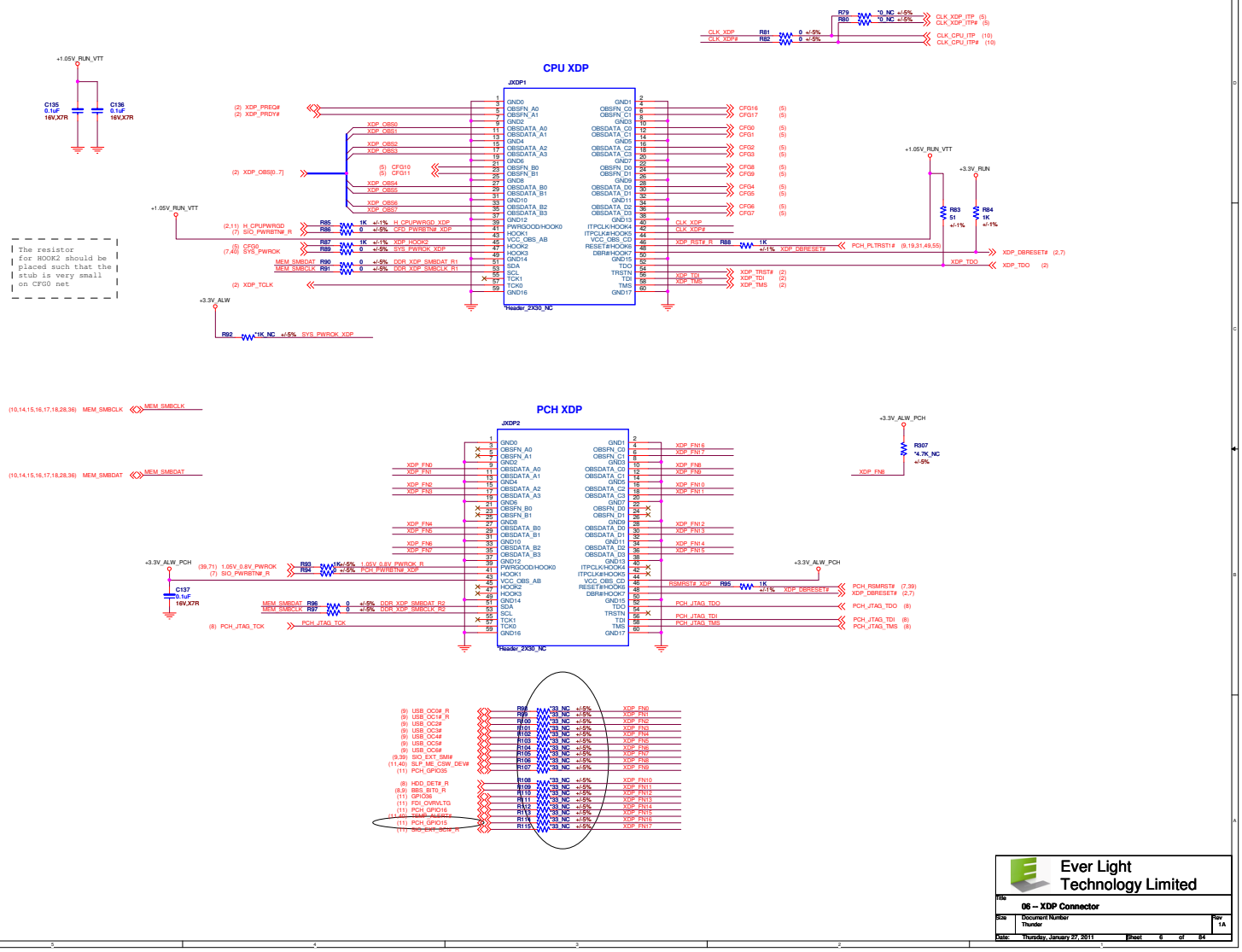

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Title	06 -- XDP Connector		
Size	Document Number: Thunder		Rev: 1A
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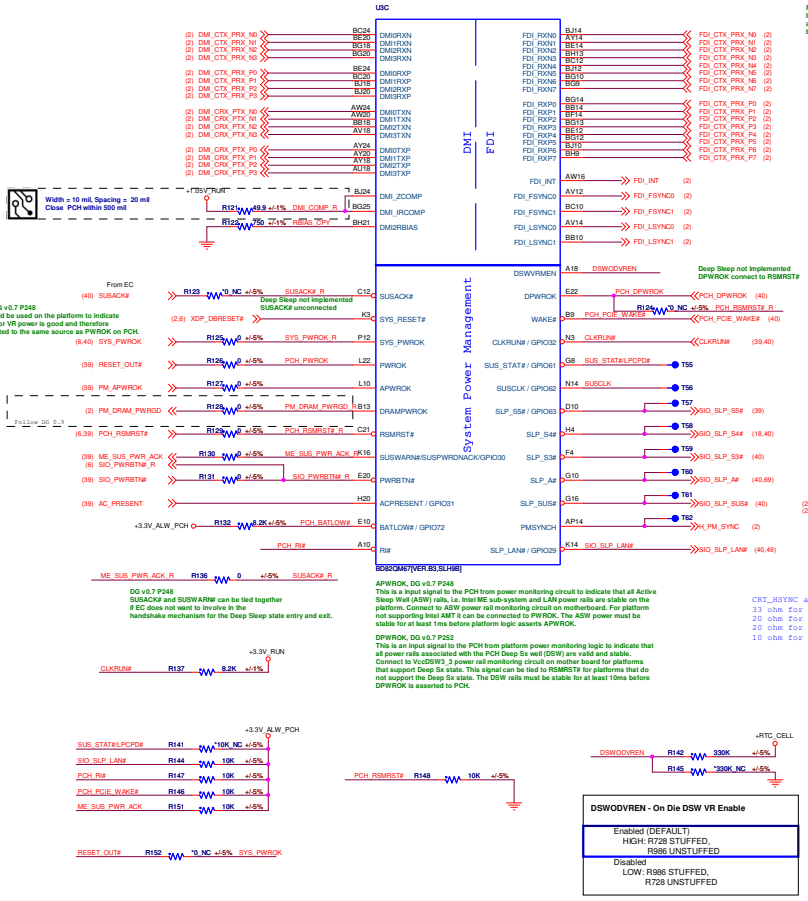
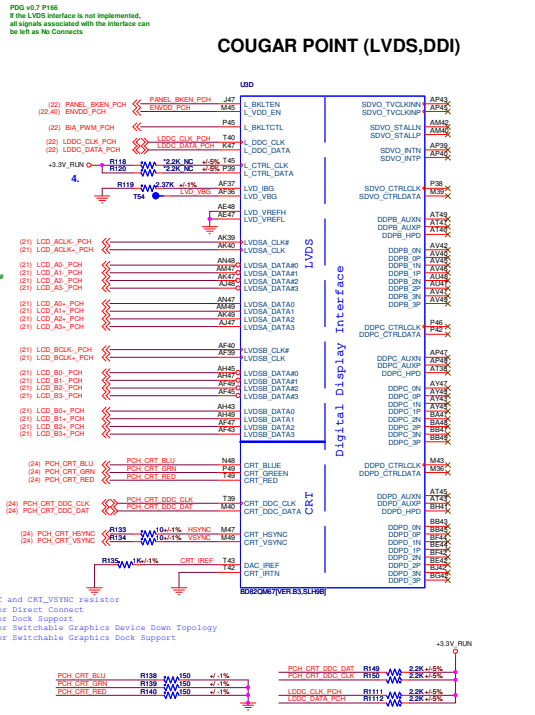
COUGAR POINT (DMI,FDI,GPIO)



COUGAR POINT (LVDS,DDI)



Title	07 – CBT 1/6 (DMI&VIDEO)
Size	Document Number
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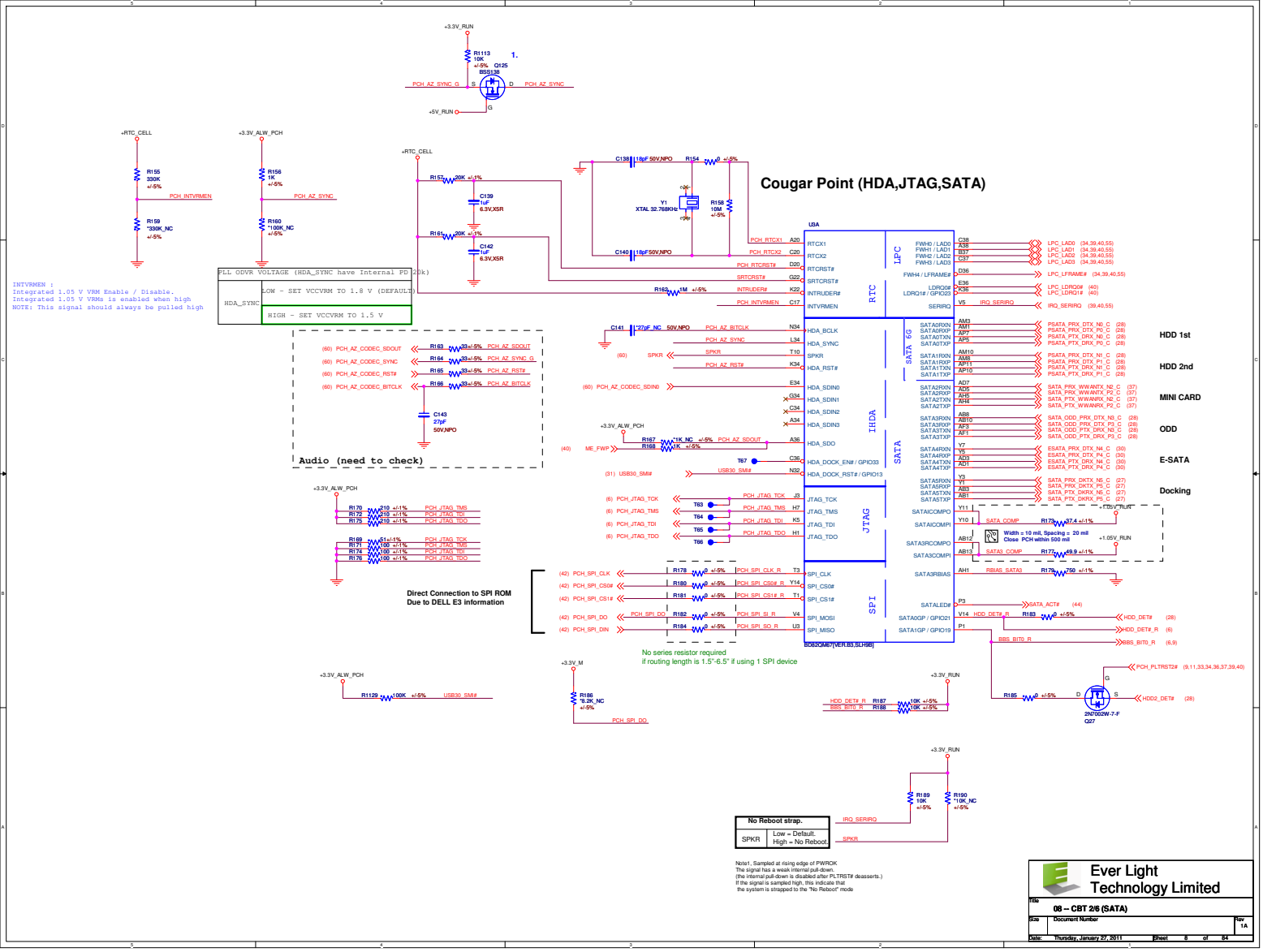
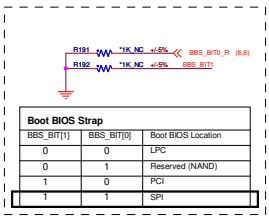
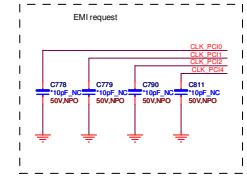


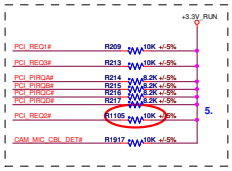
Cougar Point (PCI,USB,NVRAM)

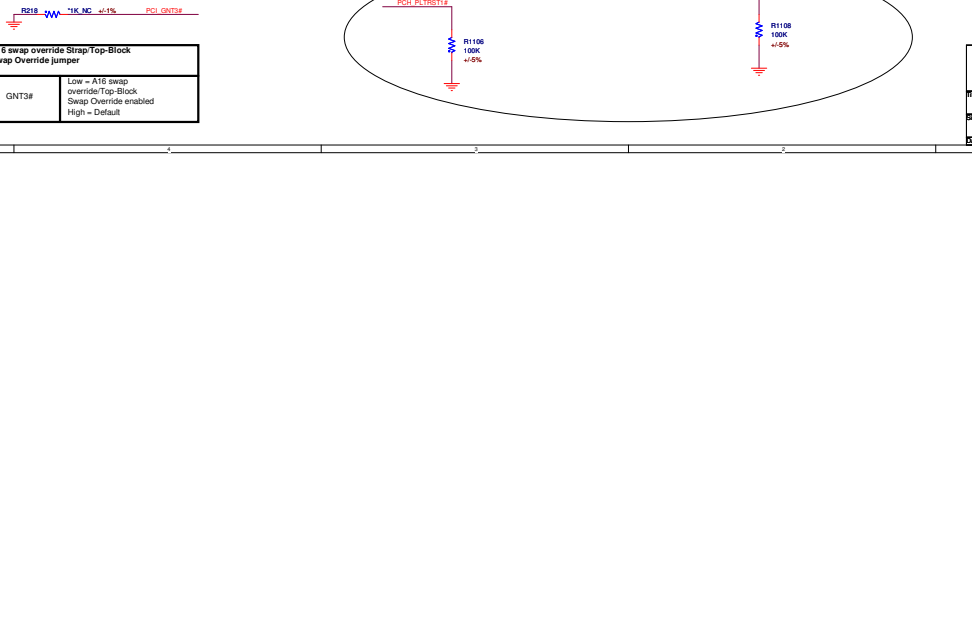


Boot BIOS Strap

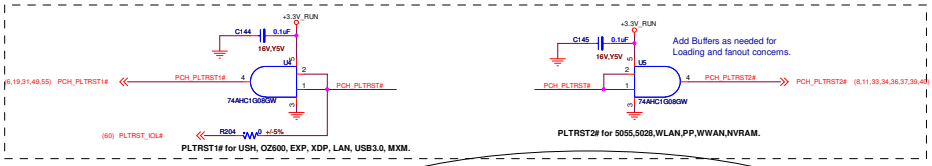
BBS_BIT[1]	BBS_BIT[0]	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI



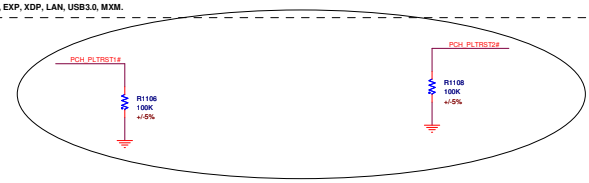




Right Side pair top
Right Side pair bottom
Back Side
AUX module (Removed)
2nd Mini Card (WLAN/WIMAX)
1st Mini Card (WWAN)
3rd Mini Card
USH
DOCK
DOCK
Express Card
BlueTooth
Camera
LCD Touch or Nvidia 3D IR



A16 swap override Strap/Top-Block Swap Override jumper	
GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default



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Title	09 -- CBT 3/6 (USB, PCI, NVRAM)	
Size	Document Number	Rev 1A
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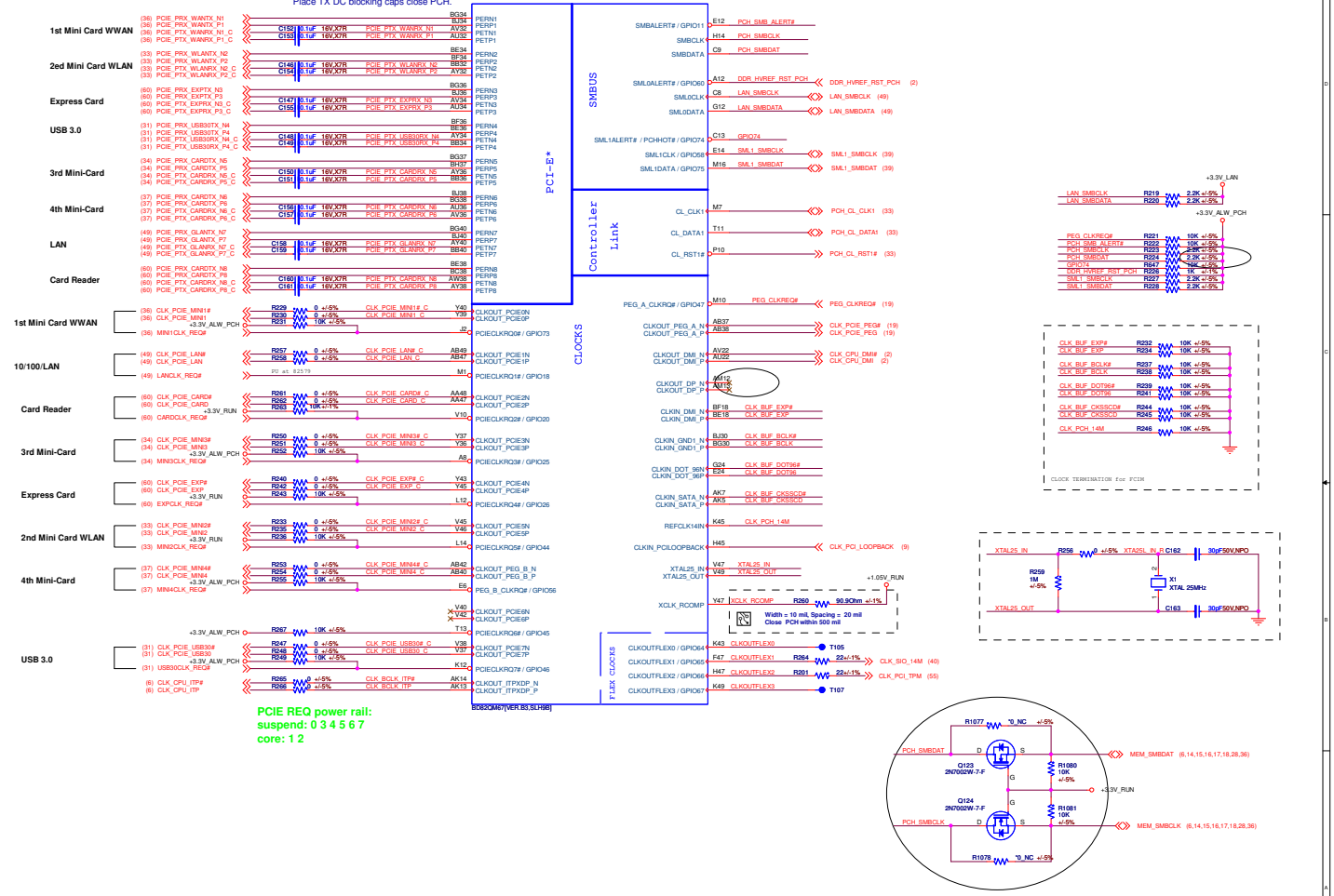
Cougar Point (PCI-E,SMBUS,CLK)

Place TX DC blocking caps close PCH.



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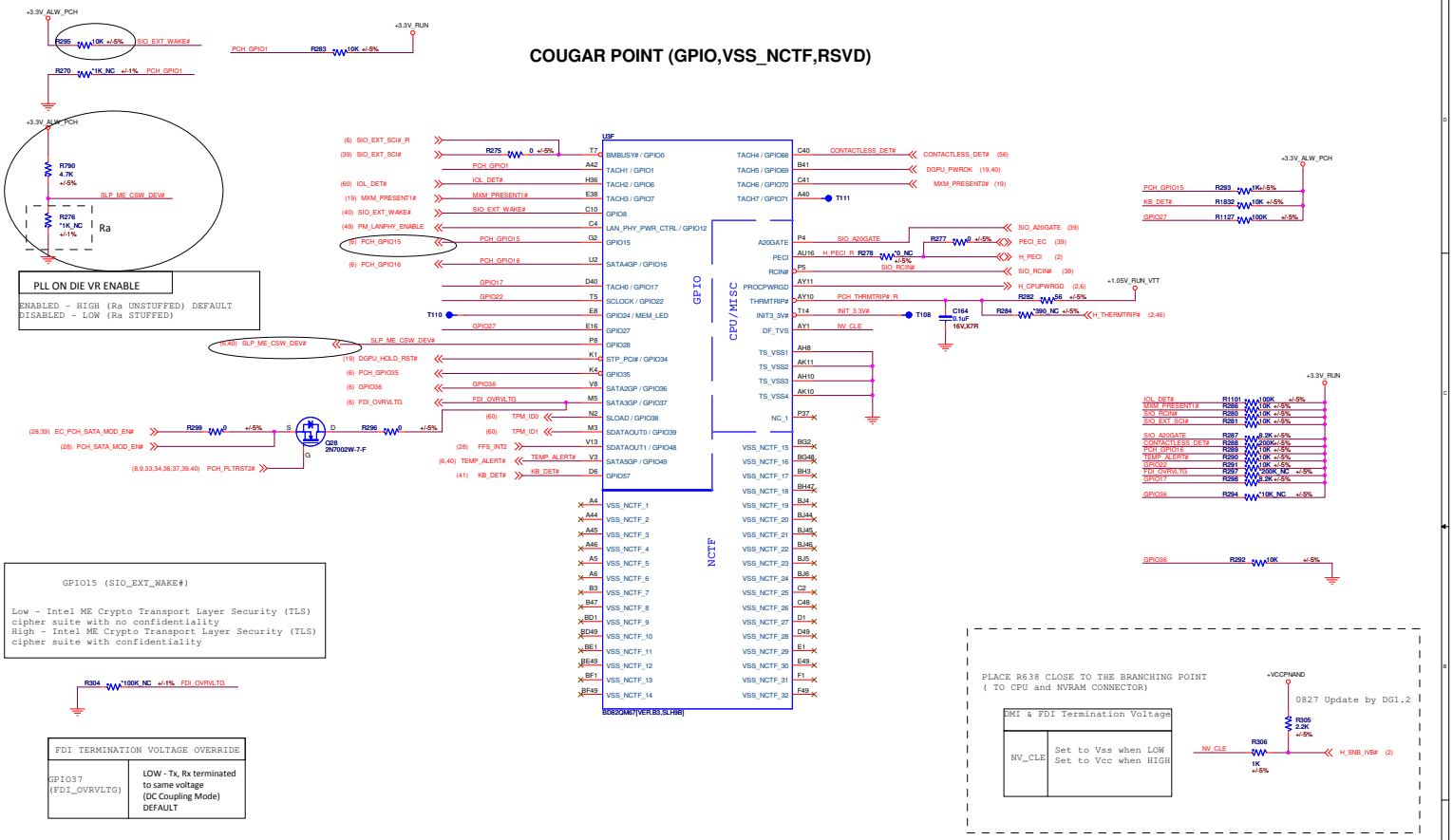
Title	10 – CBT 4/7 (PCIE, CLK)
Size	Document Number / Rev 1A
Date: Thursday, January 27, 2011	Sheet 10 of 84

COUGAR POINT (GPIO,VSS_NCTF,RSVD)



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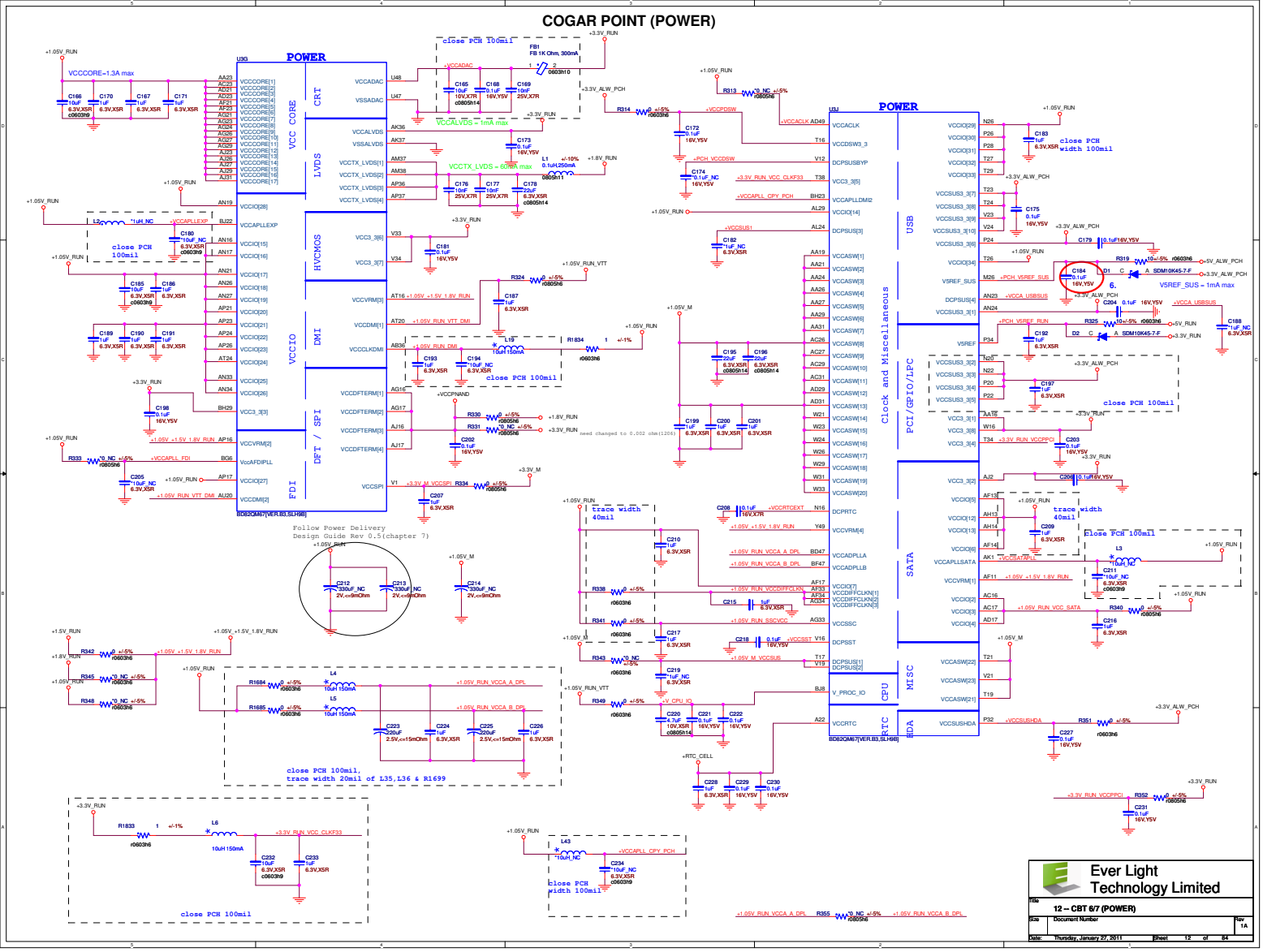
Title	11 -- CBT 5/7 (GPIO)	
Size	Document Number	Rev 1A
Date: Thursday, January 27, 2011	Sheet 11 of 84	

COGAR POINT (POWER)



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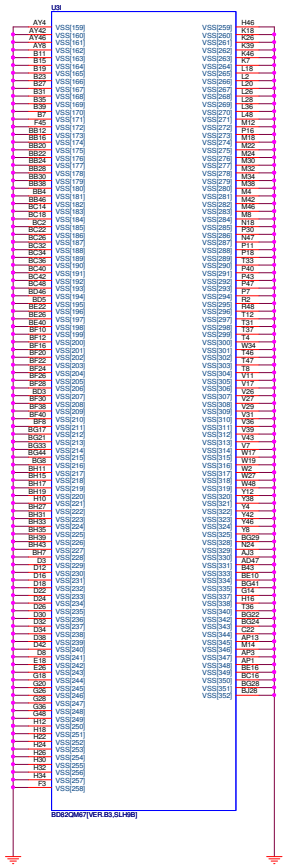
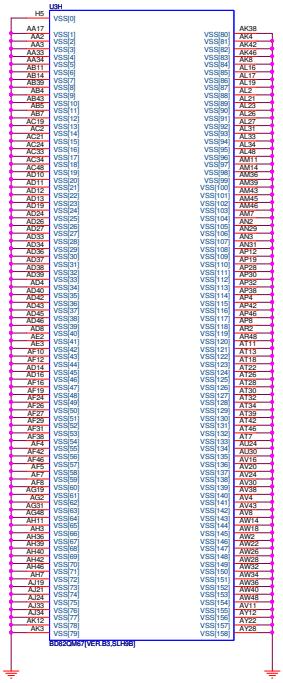
Title	12 – CBT 67 (POWER)		
Size	Document Number		Rev 1A
Date:	Thursday, January 27, 2011	Sheet 12 of 84	

Cougar Point (GND)





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Title	13 – CBT 7/7 (GND)	
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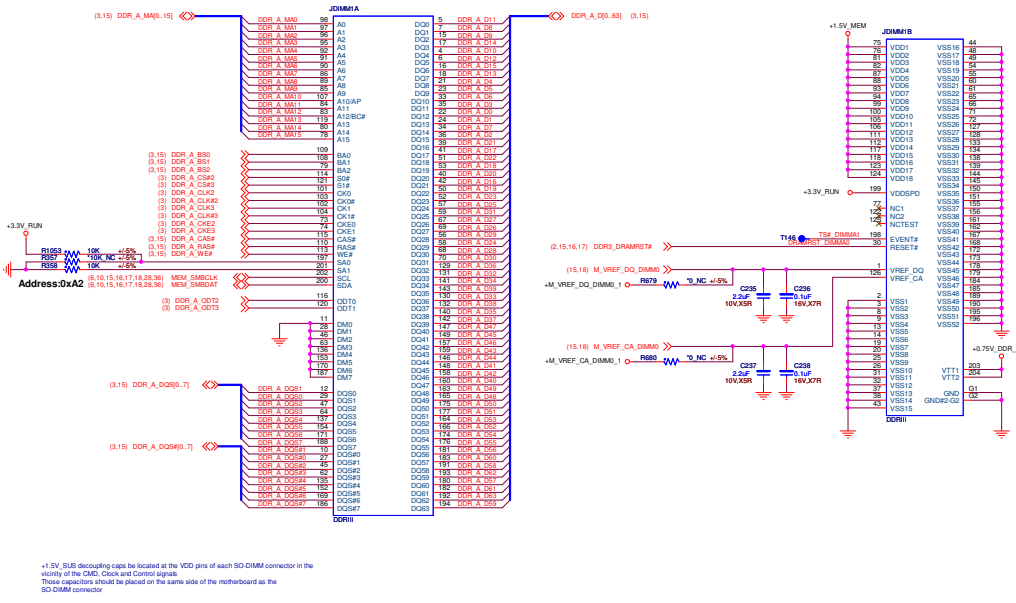
DDR3 Length Matching Formulas		
Signal Group	Min Length	Max Length
Control-to-Clock	Clock - 0.5"	Clock - 0.0"
Command-to-Clock	Clock - 0.5"	Clock - 0.5"
Strobe-to-Clock	Clock - 0.5"	Clock - 1.0"
Data-to-Strobe (per byte lane)	Strobe - 20 mils	Strobe + 20 mils

CHA_DIMM1_TOP_SIDE

JDIMM1 is RVS type.(H=100)

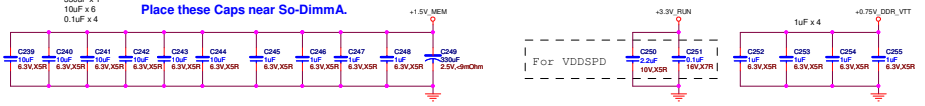


	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

+1.5V_SUS decoupling caps be located at the VDD pins of each SO-DIMM connector in the vicinity of the CMD, Clock and Control signals
Those capacitors should be placed on the same side of the motherboard as the SO-DIMM connector

330uF x 1
10uF x 6
0.1uF x 4

Place these Caps near So-DimmA.



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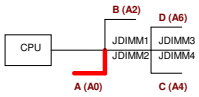
Title: 15 -- SODIMM-204P-A1

Size | Document Number: Thunder | Rev: 1A

Date: Thursday, January 27, 2011 | Sheet 14 of 84

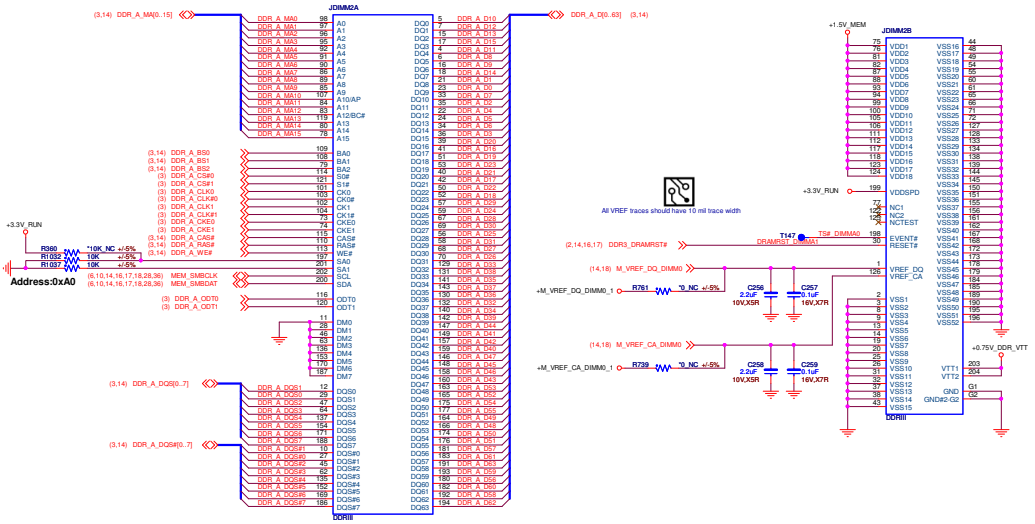


CHA_DIMM0_BOT_SIDE

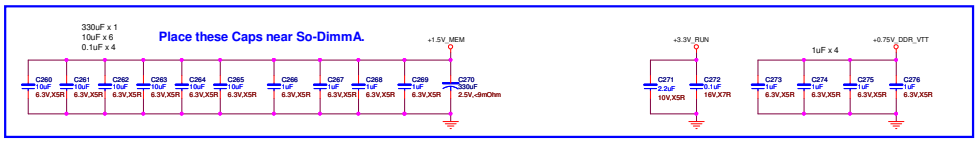
JDIMM2 is RVS type.

0510GC: CIS OK

DDR3 Length Matching Formulas		
Signal Group	Min Length	Max Length
Control-to-Clock	Clock - 0.5"	Clock - 0.0"
Command-to-Clock	Clock - 0.5"	Clock - 0.5"
Strobe-to-Clock	Clock - 0.5"	Clock - 1.0"
Data-to-Strobe (per byte lane)	Strobe - 20 mils	Strobe + 20 mils

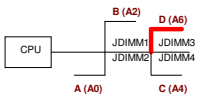


+1.5V_SUS decoupling caps be located at the VDD pins of each SO-DIMM connector in the vicinity of the CMD, Clock and Control signals
Those capacitors should be placed on the same side of the motherboard as the SO-DIMM connector



Ever Light Technology Limited

Title	14 -- SODIMM-204P-A0	
Size	Document Number: Thunder	Rev: 1A
Date: Thursday, January 27, 2011	Sheet 15 of 84	

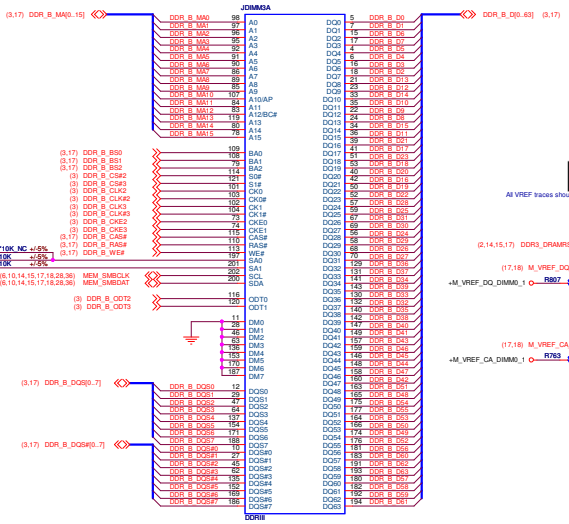


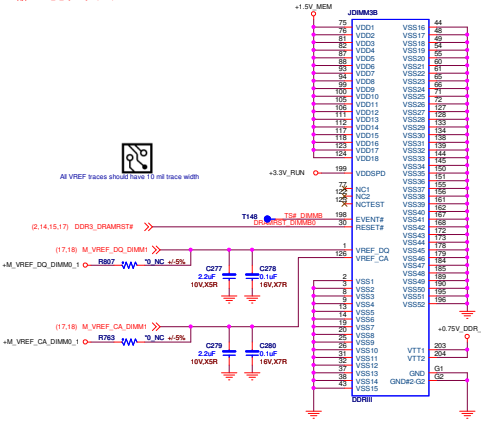
CHB_DIMM1_TOP_SIDE

DDR3 Length Matching Formulas		
Signal Group	Min Length	Max Length
Control-to-Clock	Clock - 0.5"	Clock - 0.0"
Command-to-Clock	Clock - 0.5"	Clock - 0.5"
Strobe-to-Clock	Clock - 0.5"	Clock - 1.0"
Data-to-Strobe (per byte lane)	Strobe - 20 mils	Strobe + 20 mils

JDIMM3 is RVS type.

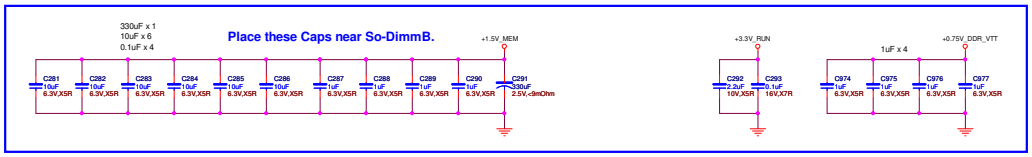
0526GC: change to RVS type





	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

+1.5V_SUS decoupling caps be located at the VDD pins of each SO-DIMM connector in the vicinity of the CMD, Clock and Control signals
Those capacitors should be placed on the same side of the motherboard as the SO-DIMM connector



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Title	17 -- SODIMM-204P-B0	
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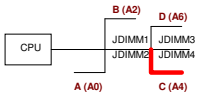
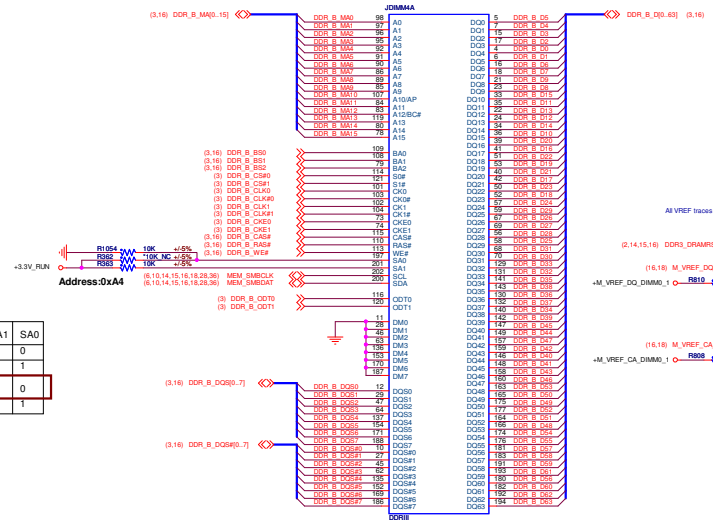


CHB_DIMM0_BOT_SIDE

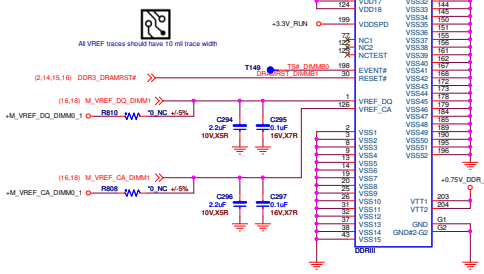
DDR3 Length Matching Formulas		
Signal Group	Min Length	Max Length
Control-to-Clock	Clock - 0.5"	Clock - 0.0"
Command-to-Clock	Clock - 0.5"	Clock - 0.5"
Strobe-to-Clock	Clock - 0.5"	Clock - 1.0"
Data-to-Strobe (per byte lane)	Strobe - 20 mils	Strobe + 20 mils

JDIMM4 is STD type.

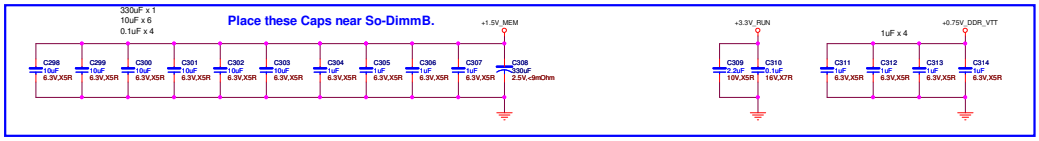
0510GC: CIS OK



	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1



+1.5V_SUS decoupling caps be located at the VDD pins of each SO-DIMM connector in the vicinity of the CMD, Clock and Control signals
Those capacitors should be placed on the same side of the motherboard as the SO-DIMM connector



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Title	16 -- SODIMM-204P-B0	
Size	Document Number: Thunder	Rev: 1A
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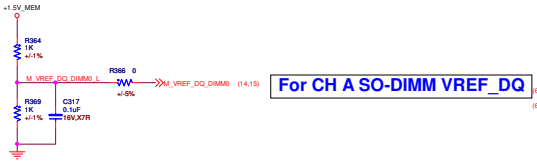
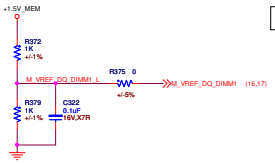
M1: Fixed SO-DIMM VREF_DQ (Default)

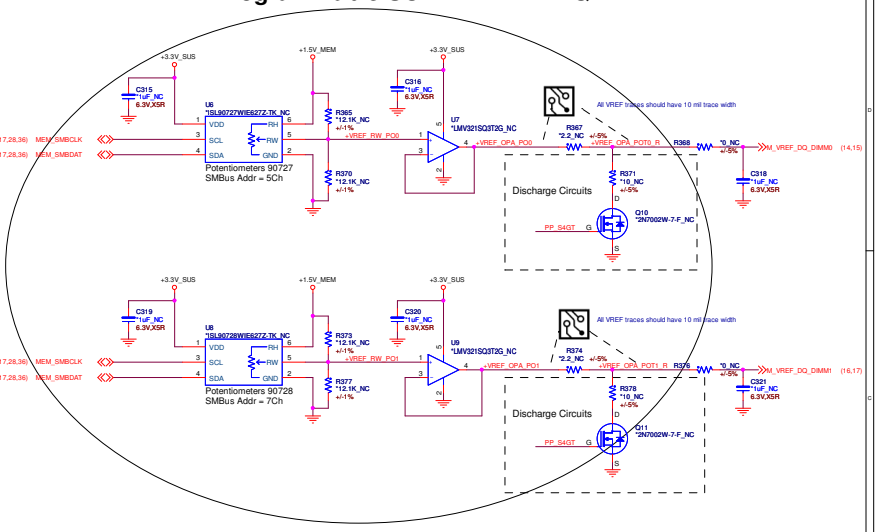


For CH A SO-DIMM VREF_DQ

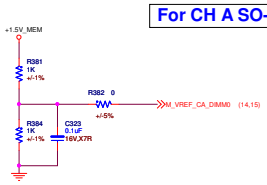


For CH B SO-DIMM VREF_DQ

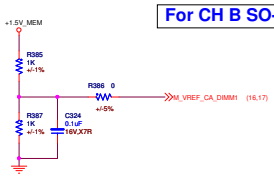
M2: Programmable SODIMM VREFDQ

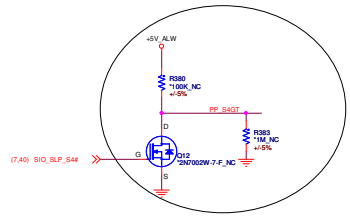


For CH A SO-DIMM VREF_CA



For CH B SO-DIMM VREF_CA





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Title	18 -- DDR3 VREF	
Size	Document Number: Thunder	Rev: 1A
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MXM 3.0 CONNECTOR

MXM SPEC:
7~20V, Up to 10A

2.5 A

0524GC: CIS OK

PEX swing slect
0: High swing
NC: Lowing swing

CEC MXM Internal PU

Mechanical Key

CONN-PCI-X

1.Whole TX & RX AC decoupling Cap(64 pcs) need to place within 0.5" of MXM Conn
2.TX cap at CPU Side

MXM PEG SPEC
Length Low swing: 7 inches High swing: 10 inches

To GPIO module side is GND

GPU internal PU.

DOCK DP1
MB HDMI

eDP Panel

DOCK DP2

MB DP Port

PU at PCH.

DPA and DPC output on MXM3.0 is must
DPB and DPD output is optional.

Thermal Trip

Thermal Alert

From 5048

Ever Light Technology Limited

Title	19 – MXM3.0 Connector	
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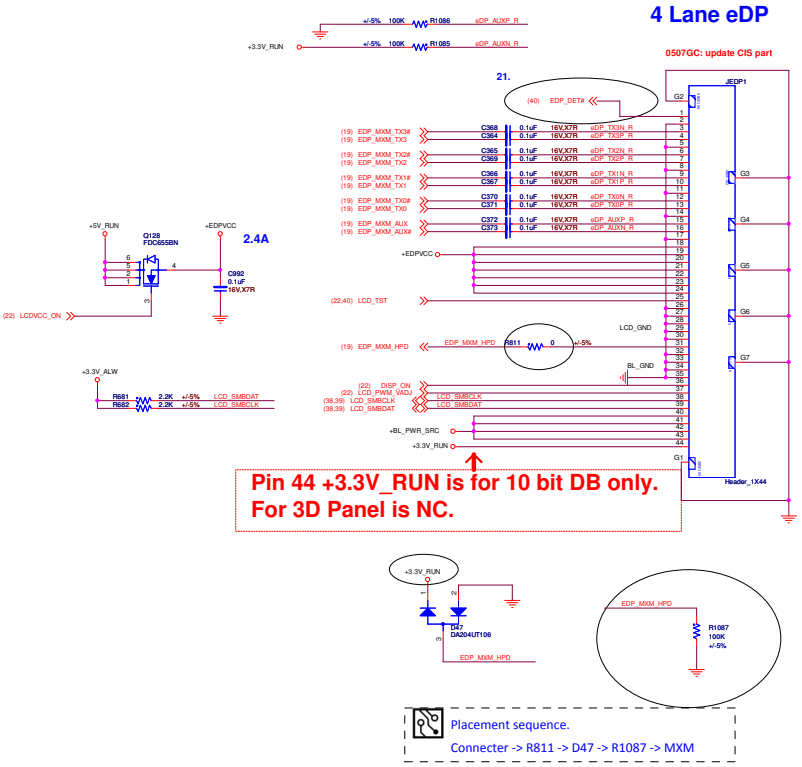

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Title	20 – 17" eDP for PANEL
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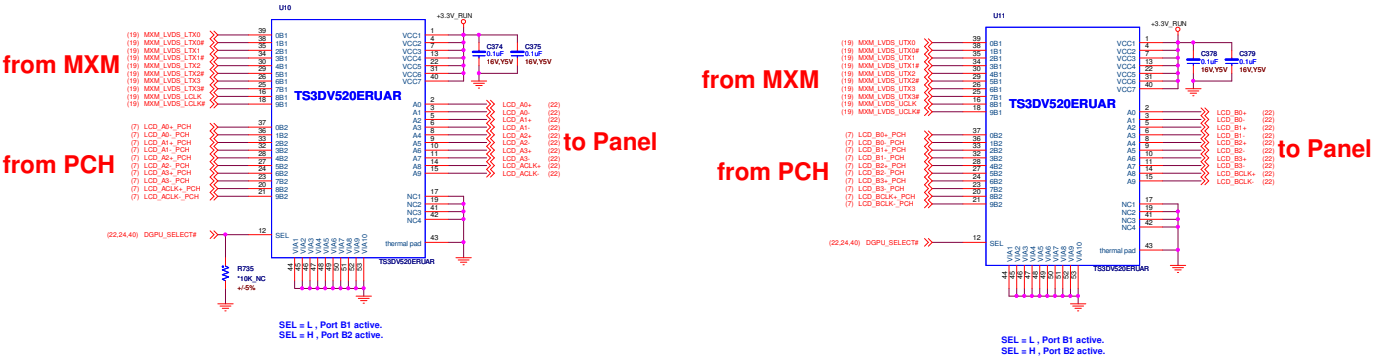
LVDS MUX for Panel



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Title	21 -- LVDS MUX for PANEL	
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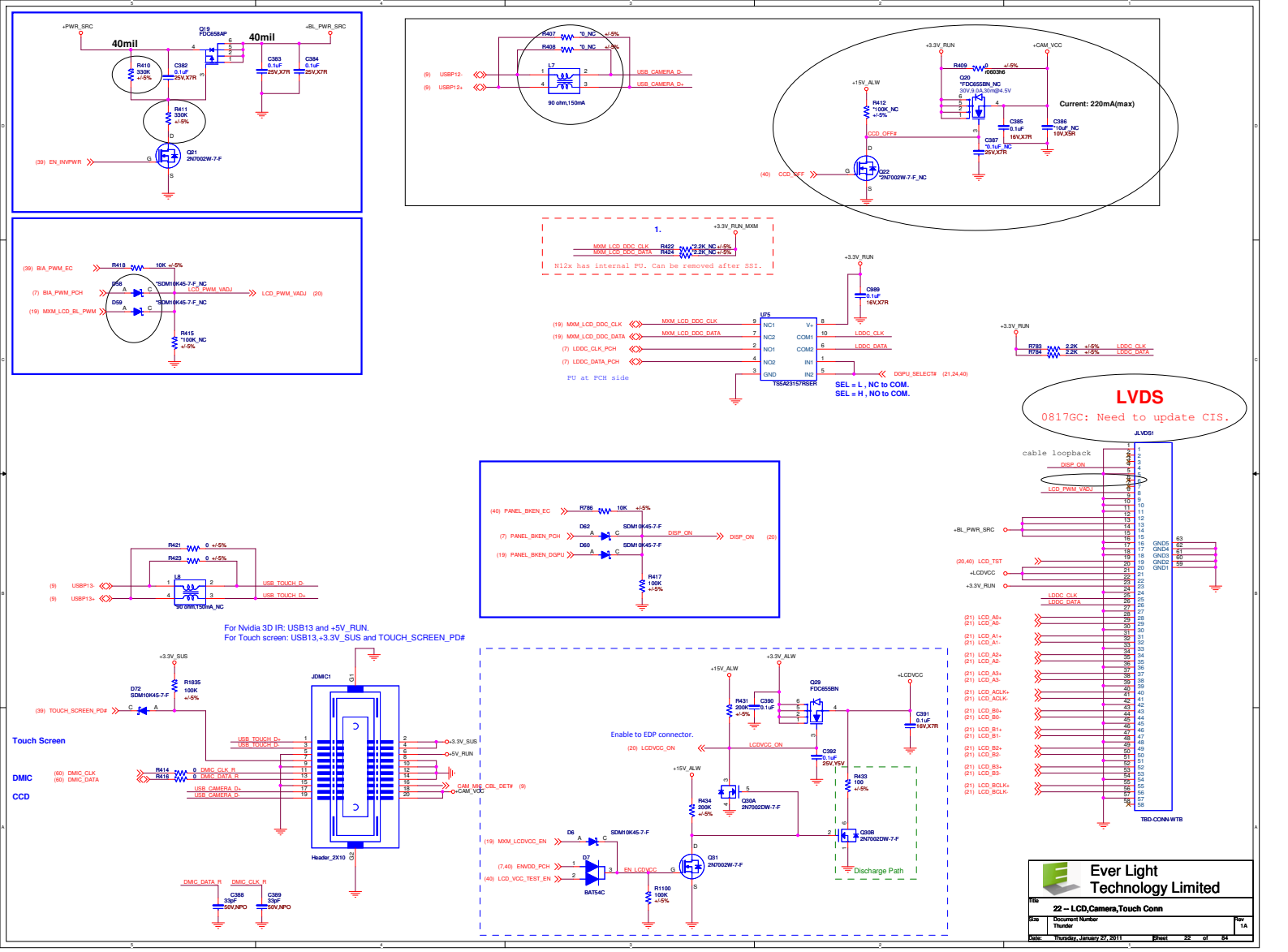
+PWR_SRC
40mil
Q19
FDC658AP
40mil
+BL_PWR_SRC
R416
330K
+/-5%
C382
0.1uF
25V,X7R
C383
0.1uF
25V,X7R
C384
0.1uF
25V,X7R
R411
330K
+/-5%
Q21
2N7002W-7-F
(39) EN_INVPWR
R1407
*0_NC
+/-5%
R408
*0_NC
+/-5%
L7
90 ohm,150mA
(9) USBP12-
(9) USBP12+
USB_CAMERA_D-
USB_CAMERA_D+
+3.3V_RUN
+CAM_VCC
R409
0
+/-5%
r0603n6
Q20
*FDC655BN_NC
30V,9.6A,30m@4.5V
Current: 220mA(max)
C385
0.1uF
16V,X7R
C386
*10uF_NC
10V,X5R
C387
*0.1uF_NC
25V,X7R
+15V_ALW
R412
*100K_NC
+/-5%
CCD_OFF#
Q22
*2N7002W-7-F_NC
(40) CCD_OFF
(39) BIA_PWM_EC
R418
10K +/-5%
D58
*SDM10K45-7-F_NC
D59
*SDM10K45-7-F_NC
(7) BIA_PWM_PCH
(19) MXM_LCD_BL_PWM
LCD_PWM_VADJ
LCD_PWM_VADJ (20)
R415
*100K_NC
+/-5%
1.
+3.3V_RUN_MXM
MXM_LCD_DDC_CLK
MXM_LCD_DDC_DATA
R422
*2.2K_NC +/-5%
R424
*2.2K_NC +/-5%
N12x has internal PU. Can be removed after SSI.
+3.3V_RUN
C989
0.1uF
16V,X7R
(19) MXM_LCD_DDC_CLK
(19) MXM_LCD_DDC_DATA
(7) LDDC_CLK_PCH
(7) LDDC_DATA_PCH
PU at PCH side
U75
NC1
NC2
NO1
NO2
GND
V+
COM1
COM2
IN1
IN2
TS5A23157RSER
LDDC_CLK
LDDC_DATA
DGPU_SELECT# (21,24,40)
SEL = L , NC to COM.
SEL = H , NO to COM.
+3.3V_RUN
R783
R784
2.2K
2.2K
+/-5%
+/-5%
LDDC_CLK
LDDC_DATA
LVDS
0817GC: Need to update CIS.
JLVDS1
cable loopback
DISP_ON
LCD_PWM_VADJ
+BL_PWR_SRC
(20,40) LCD_TST
+LCDVCC
+3.3V_RUN
LDDC_CLK
LDDC_DATA
(21) LCD_A0+
(21) LCD_A0-
(21) LCD_A1+
(21) LCD_A1-
(21) LCD_A2+
(21) LCD_A2-
(21) LCD_A3+
(21) LCD_A3-
(21) LCD_ACLK+
(21) LCD_ACLK-
(21) LCD_B0+
(21) LCD_B0-
(21) LCD_B1+
(21) LCD_B1-
(21) LCD_B2+
(21) LCD_B2-
(21) LCD_B3+
(21) LCD_B3-
(21) LCD_BCLK+
(21) LCD_BCLK-
GND5
GND4
GND3
GND2
GND1
TBD-CONN-WTB
(40) PANEL_BKEN_EC
R786
10K +/-5%
D62
SDM10K45-7-F
D60
SDM10K45-7-F
(7) PANEL_BKEN_PCH
(19) PANEL_BKEN_DGPU
DISP_ON
DISP_ON (20)
R417
100K
+/-5%
R421
0 +/-5%
R423
0 +/-5%
L8
90 ohm,150mA_NC
(9) USBP13-
(9) USBP13+
USB_TOUCH_D-
USB_TOUCH_D+
For Nvidia 3D IR: USB13 and +5V_RUN.
For Touch screen: USB13,+3.3V_SUS and TOUCH_SCREEN_PD#
+3.3V_SUS
R1935
100K
+/-5%
D72
SDM10K45-7-F
(39) TOUCH_SCREEN_PD#
Touch Screen
DMIC
CCD
JDMIC1
Header_2X10
USB_TOUCH_D-
USB_TOUCH_D+
+3.3V_SUS
+5V_RUN
CAM_MIC_CBL_DET# (9)
+CAM_VCC
R414
R416
0
0
DMIC_CLK_R
DMIC_DATA_R
(60) DMIC_CLK
(60) DMIC_DATA
USB_CAMERA_D+
USB_CAMERA_D-
DMIC_DATA_R
DMIC_CLK_R
C388
33pF
50V,NPO
C389
33pF
50V,NPO
Enable to EDP connector.
(20) LCDVCC_ON
LCDVCC_ON
+3.3V_ALW
+15V_ALW
R431
200K
+/-5%
C390
0.1uF
Q29
FDC655BN
+LCDVCC
C391
0.1uF
16V,X7R
C392
0.1uF
25V,Y5V
R434
200K
+/-5%
Q30A
2N7002DW-7-F
R433
100
+/-5%
Q30B
2N7002DW-7-F
Discharge Path
(19) MXM_LCDVCC_EN
(7,40) ENVDD_PCH
(40) LCD_VCC_TEST_EN
D6
SDM10K45-7-F
D7
BAT54C
EN_LCDVCC
Q31
2N7002W-7-F
R1100
100K
+/-5%
Ever Light
Technology Limited
Title
22 -- LCD,Camera,Touch Conn
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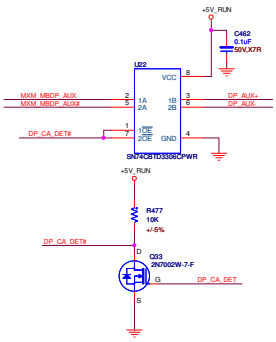
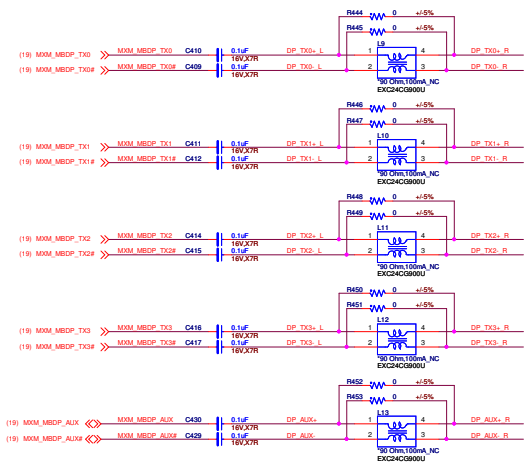
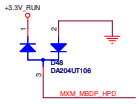
FOR Dongle

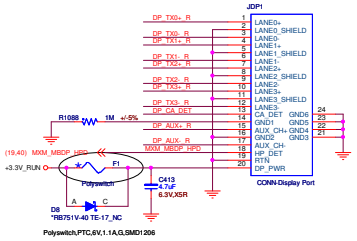


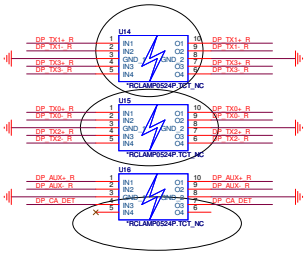
Display Port



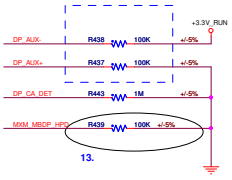


0524GC: CIS OK





Put close to connecter.



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Title	22 -- Display Port & Re-Driver	
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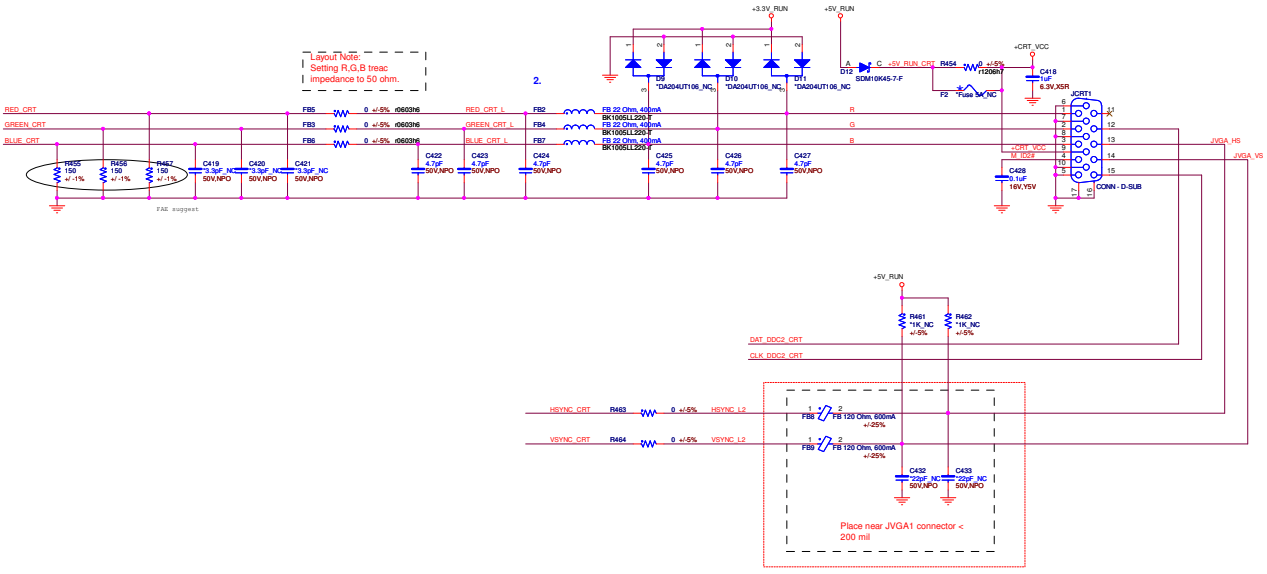
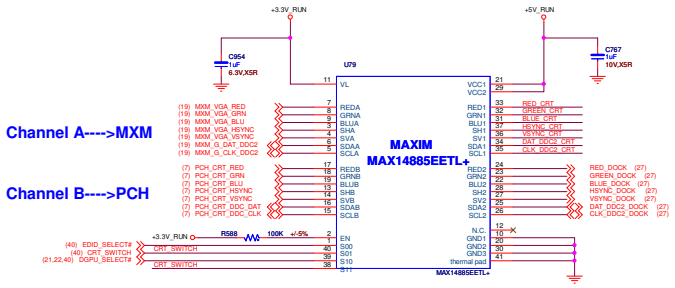
CRT





Truth table

	A-->Port 1	B-->Port 1	A-->Port 2	B-->Port 2
S01/S11 (CRT_SWITCH)	0	0	1	1
S10 (DGPU_SELECT#)	0	1	0	1
S00 (EDID_SELECT#)	0	1	0	1

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Title	23 -- CRT & MUX	
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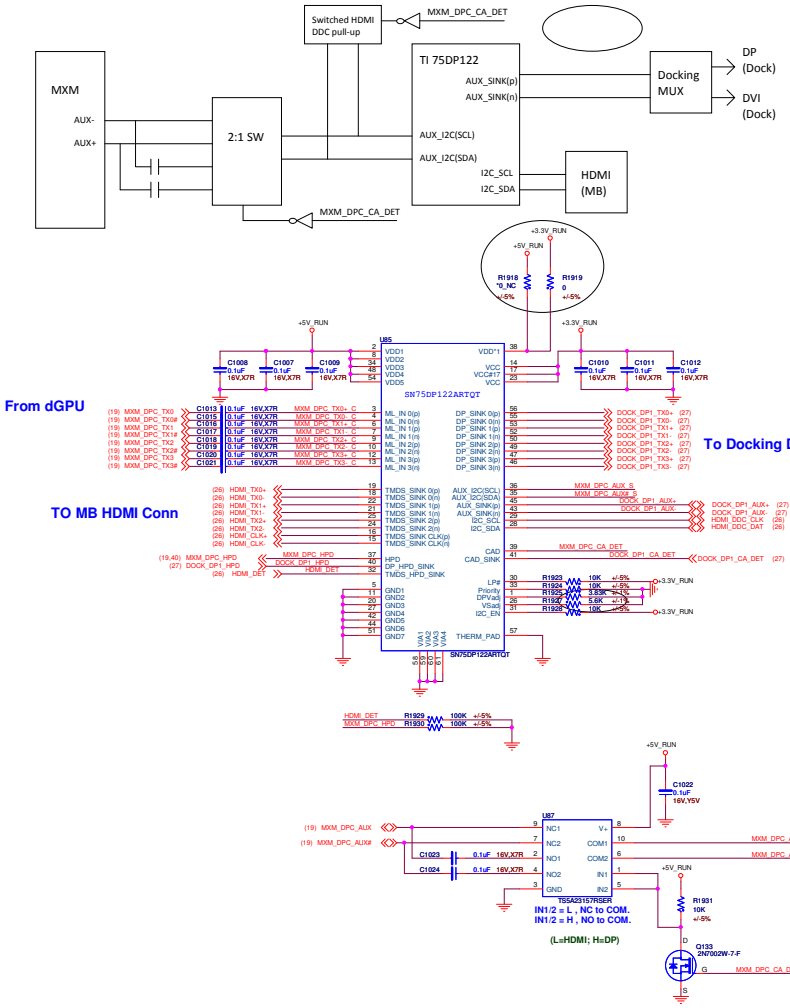

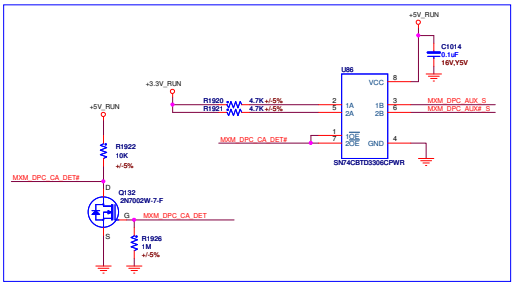

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Title	24 -- MUX for HDMI
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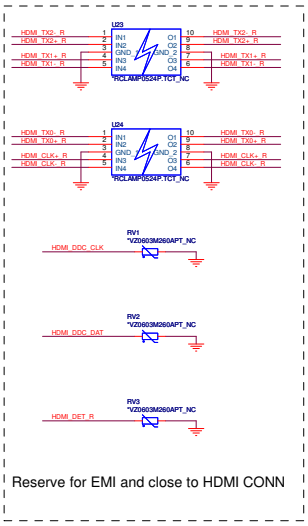
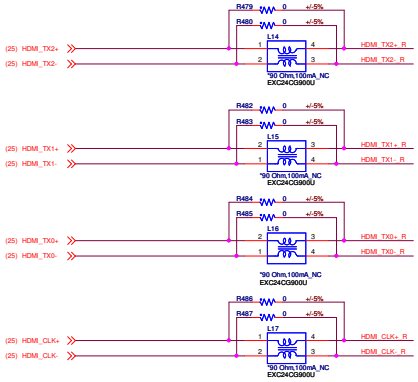
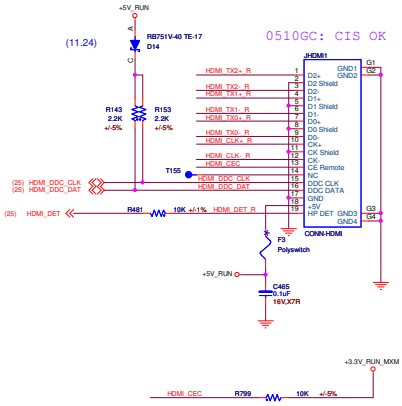
HDMI CONN







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Title	25 -- HDMI	
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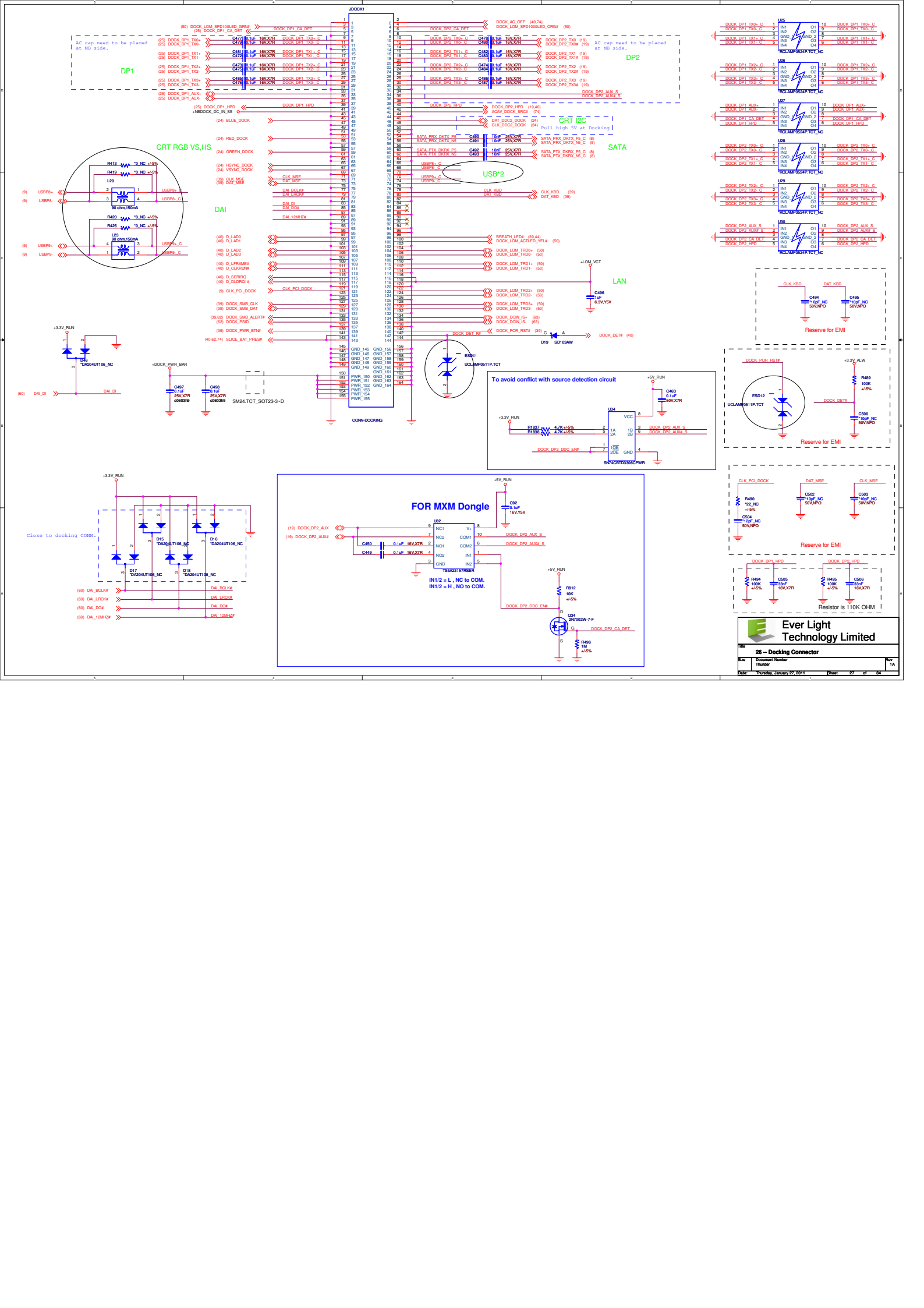
JDOCK1
CONN-DOCKING
DP1
DP2
AC cap need to be placed at MB side.
CRT RGB VS,HS
DAI
CRT I2C
Pull high 5V at Docking
SATA
USB*2
LAN
Reserve for EMI
To avoid conflict with source detection circuit
FOR MXM Dongle
IN1/2 = L , NC to COM.
IN1/2 = H , NO to COM.
Close to docking CONN.
Resistor is 110K OHM
Ever Light Technology Limited
26 -- Docking Connector
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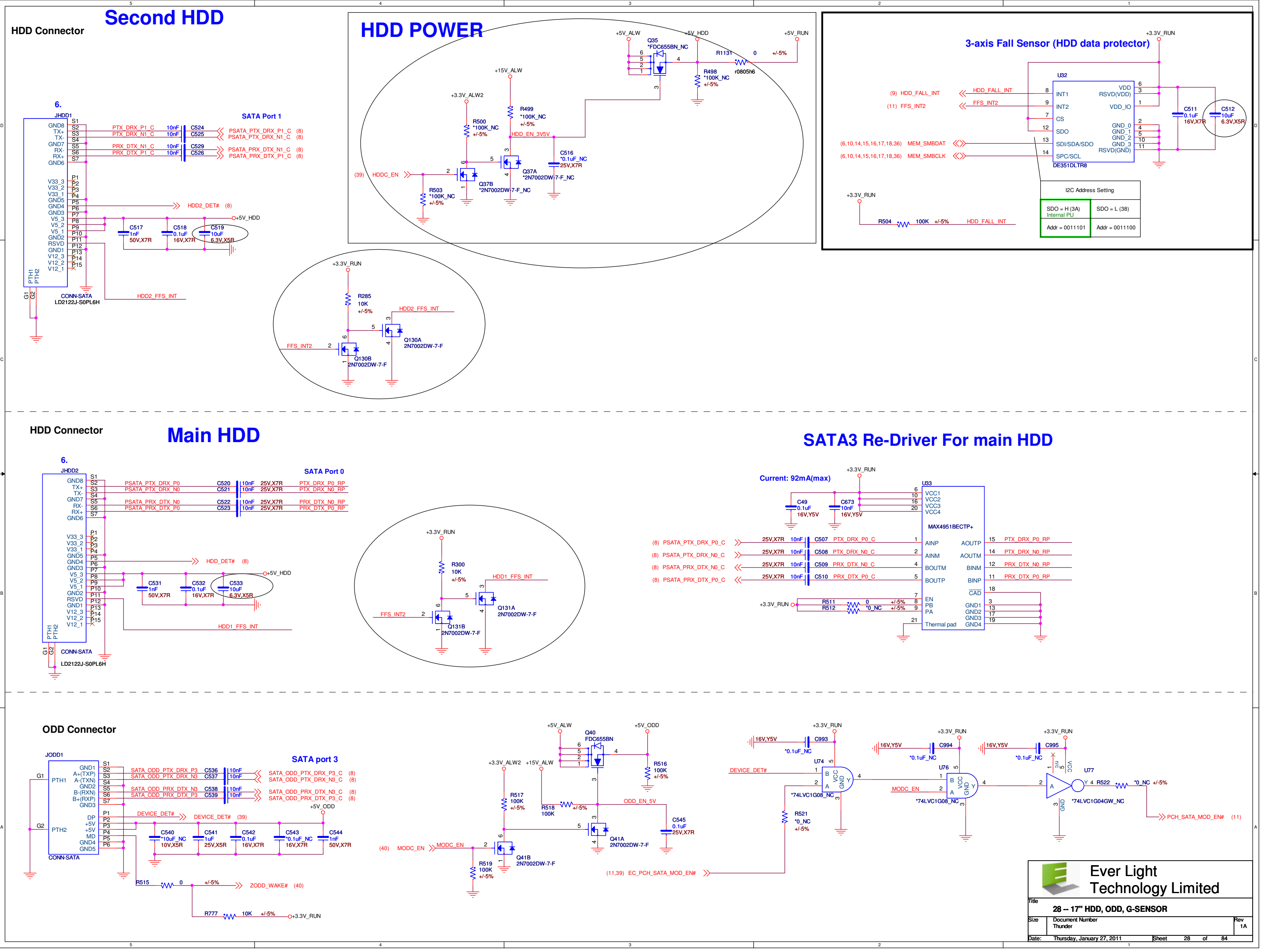
Second HDD
HDD Connector
HDD POWER
3-axis Fall Sensor (HDD data protector)
I2C Address Setting
SDO = H (3A)
Internal PU
SDO = L (38)
Addr = 0011101
Addr = 0011100
SATA Port 1
Main HDD
HDD Connector
SATA Port 0
SATA3 Re-Driver For main HDD
Current: 92mA(max)
MAX4951BECTP+
ODD Connector
SATA port 3
CONN-SATA
LD2122J-S0PL6H
DE351DLTR8
Ever Light
Technology Limited
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28 -- 17" HDD, ODD, G-SENSOR
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Technology Limited

Title	29 -- 15" HDD, ODD, G-SENSOR	
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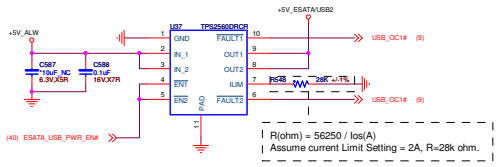
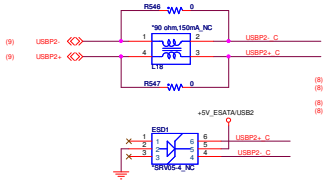
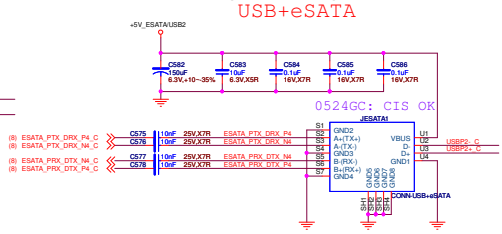
USB Power





USB(Back Side)

USB+eSATA



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Title	29 -- eSATA/USB, USB x 2		
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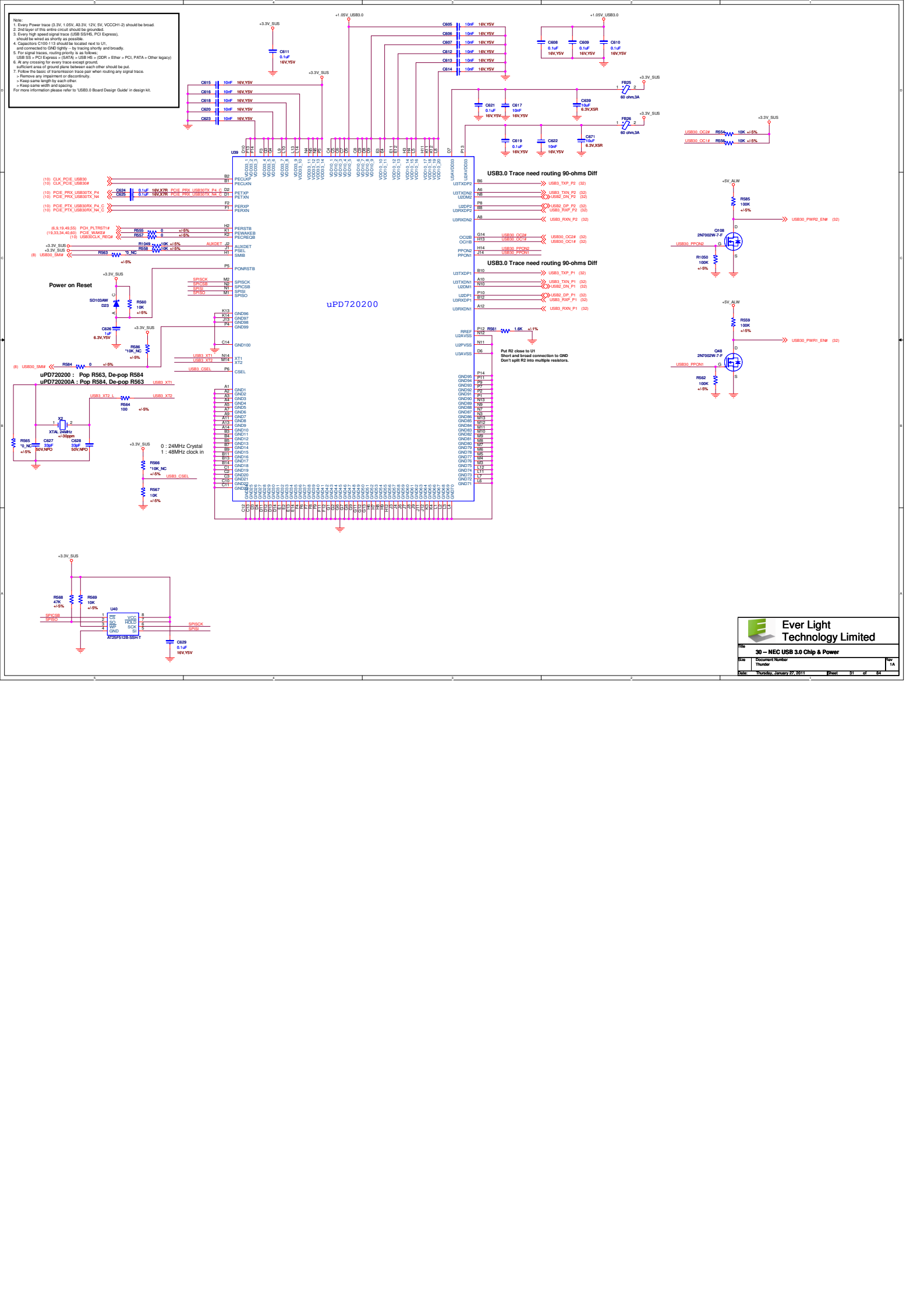
Note:
1. Every Power trace (3.3V, 1.05V, A0,3V, 12V, 5V, VCCCH1-2) should be broad.
2. 2nd layer of this entire circuit should be grounded.
3. Every high speed signal trace (USB SS/HS, PCI Express), should be wired as shortly as possible.
4. Capacitors C100-113 should be located next to U1, and connected to GND tightly - by tracing shortly and broadly.
5. For signal traces, routing priority is as follows; USB SS > PCI Express > (SATA) > USB HS > (DDR > Ether > PCI, PATA > Other legacy)
6. At any crossing for every trace except ground, sufficient area of ground plane between each other should be put.
7. Follow the basic of transmission trace pair when routing any signal trace.
> Remove any impairment or discontinuity.
> Keep same length by each other.
> Keep same width and spacing.
For more information please refer to 'USB3.0 Board Design Guide' in design kit.
uPD720200
USB3.0 Trace need routing 90-ohms Diff
USB3.0 Trace need routing 90-ohms Diff
Power on Reset
uPD720200 : Pop R563, De-pop R584
uPD720200A : Pop R584, De-pop R563
0 : 24MHz Crystal
1 : 48MHz clock in
Put R2 close to U1
Short and broad connection to GND
Don't split R2 into multiple resistors.
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30 -- NEC USB 3.0 Chip & Power
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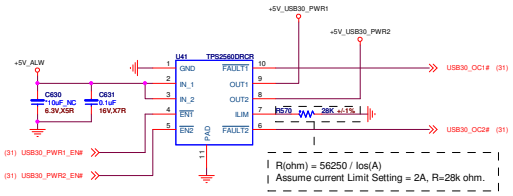

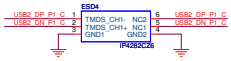

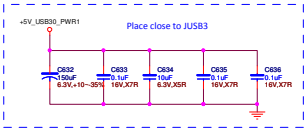

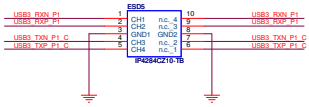

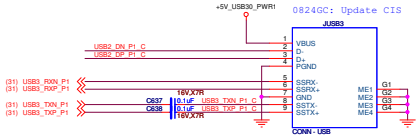

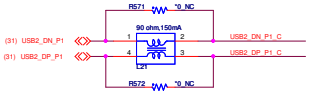

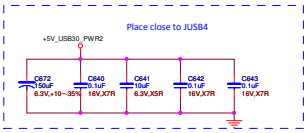

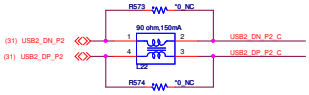

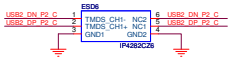

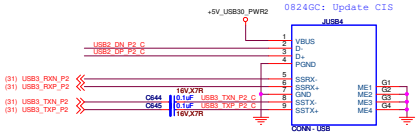

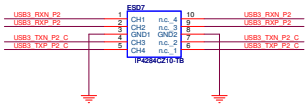

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Title	31 -- USB 3.0 Connector x 2	
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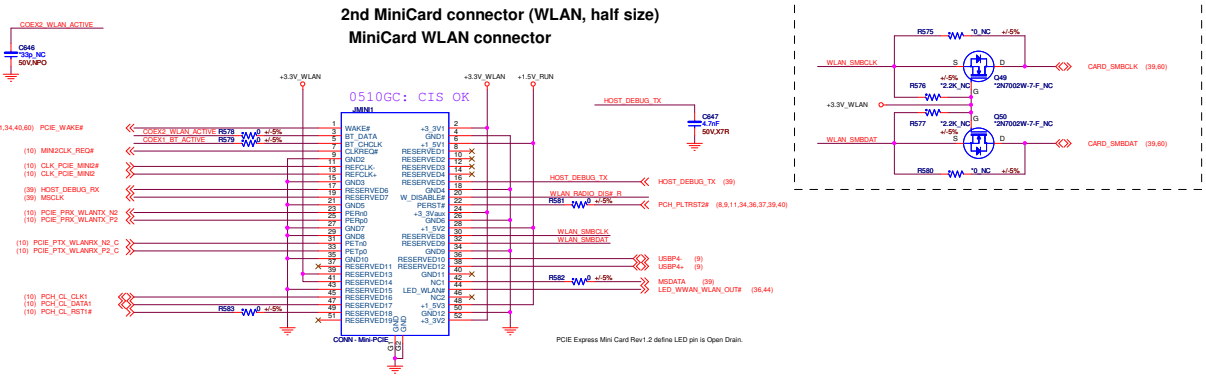
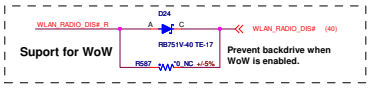
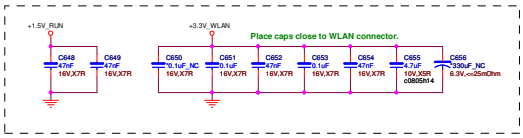
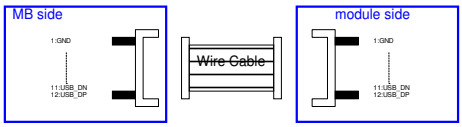
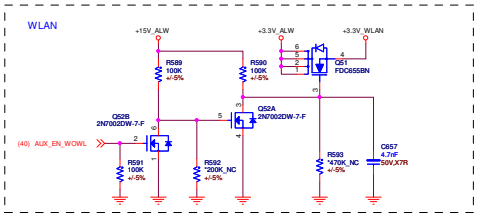
2nd MiniCard connector (WLAN, half size)
MiniCard WLAN connector

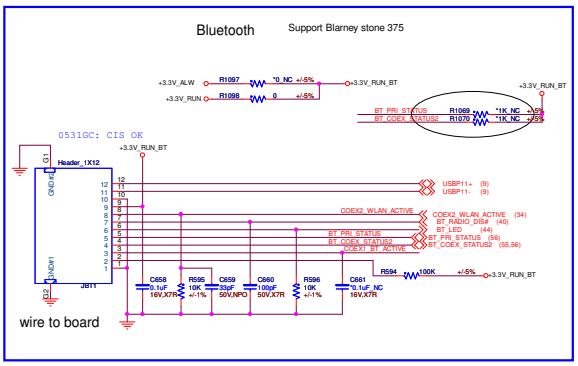








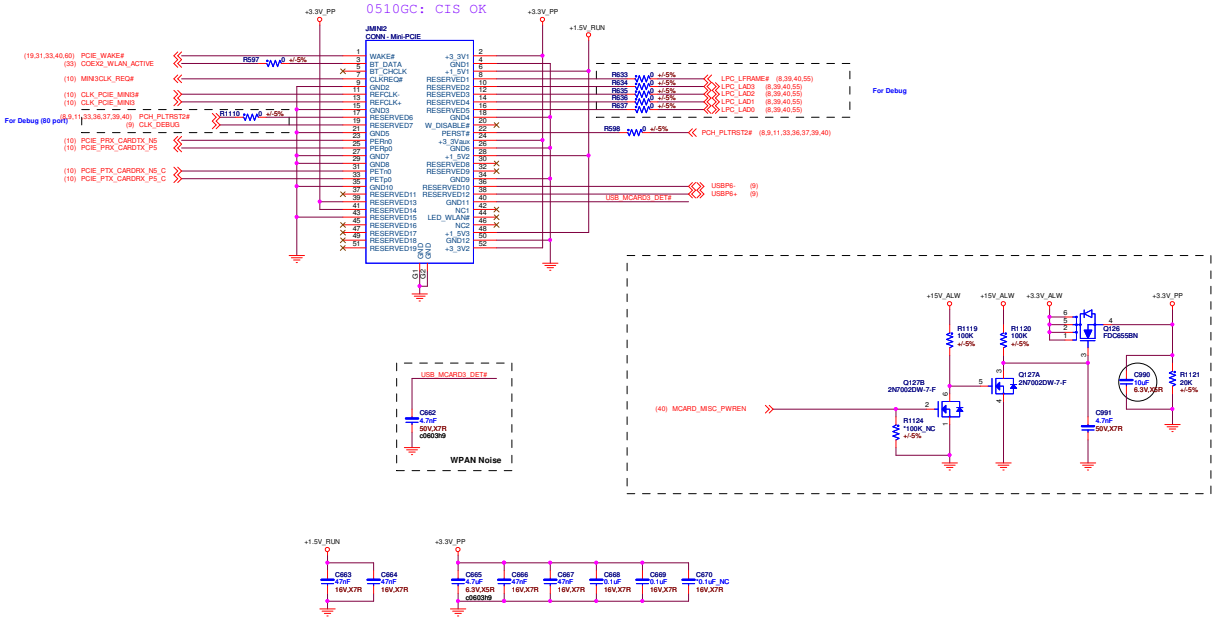




Ever Light Technology Limited	
Title	33 -- WLAN(1/2 Mini cad), BT
Size	Document Number: Thunder — Rev: 1A
Date: Thursday, January 27, 2011	Sheet 33 of 84

3rd MiniCard connector (Flash, half size)

MiniCard connector



Ever Light Technology Limited	
Title	34 -- Flash /PP(1/2Mini cad)
Size	Document Number: Thunder; Rev: 1A
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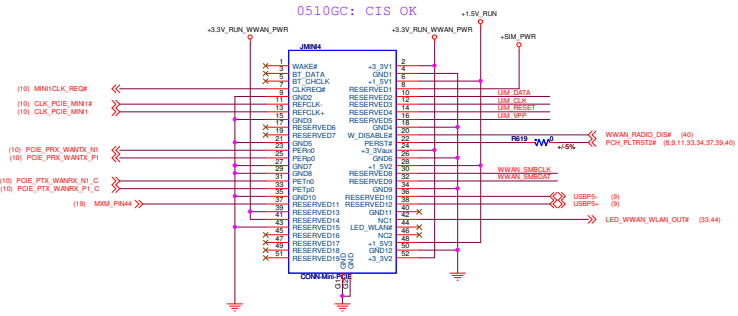
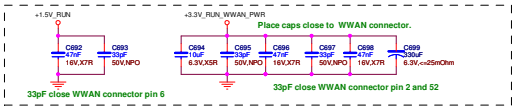
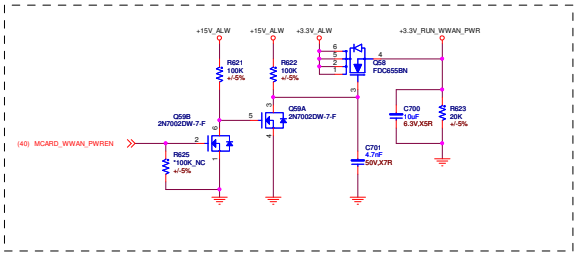
Technology Limited

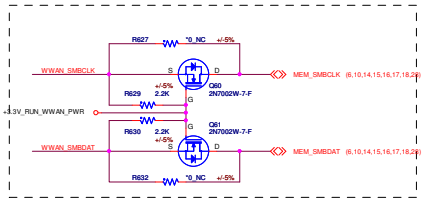
Title	35 -- 15" WWAN- SIM+MUX	
Size	Document Number	Rev 1A
Date: Thursday, January 27, 2011	Sheet 35 of 84	

MiniCard WWAN connector

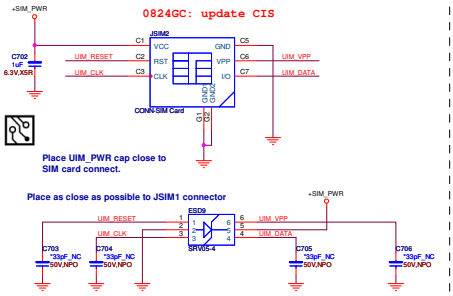








SIM CARD



Ever Light Technology Limited			
Title	36 – 17" WWAN- SIM		
Size	Document Number		Rev 1A
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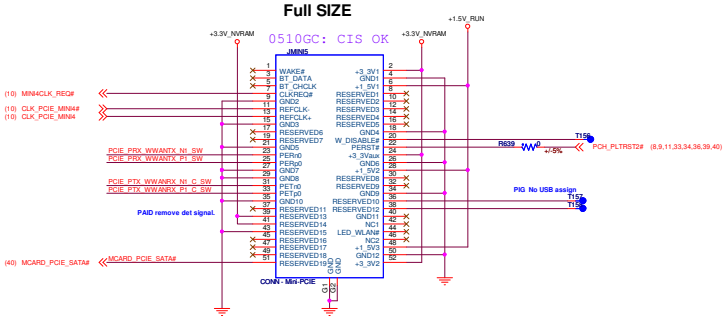
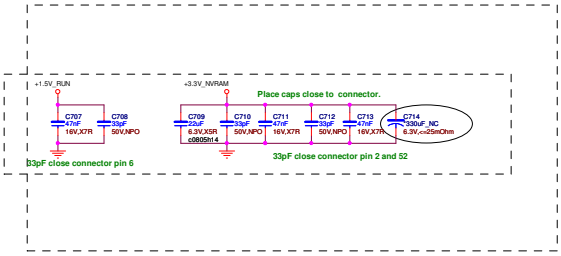
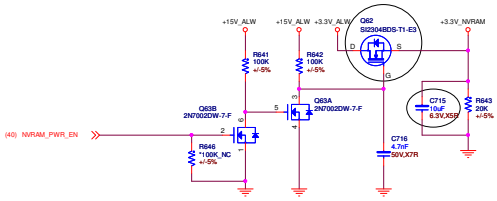
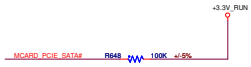
4th MiniCard connector (NVRAM, full size)

NVRAM connector
Full SIZE

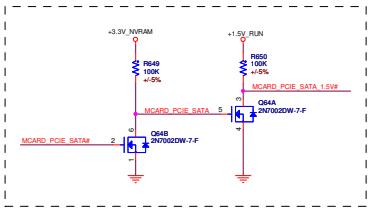






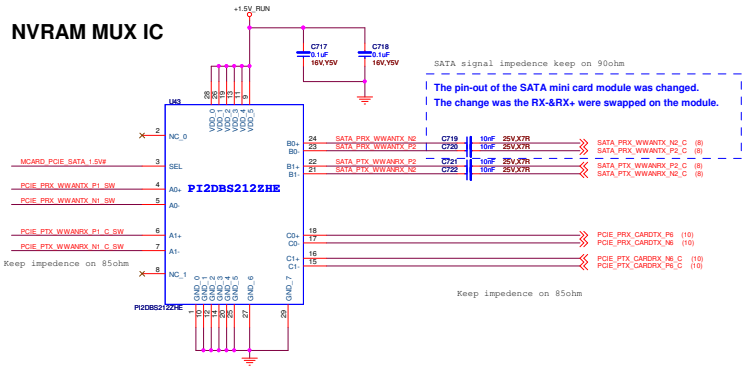


PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+-9%	1000	750	
	+-9%	330	250	250 (wake enable) 5 (Not wake enable)
+1.5V	+-5%	500	375	NA



Function	SEL
Port A to Port B	0
Port A to Port C	1

NVRAM MUX IC



The pin-out of the SATA mini card module was changed.
The change was the RX-&RX+ were swapped on the module.

DS_0412: follow PIG,SATA Port 2

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Title	37 – 17" NVRAM+MUX		
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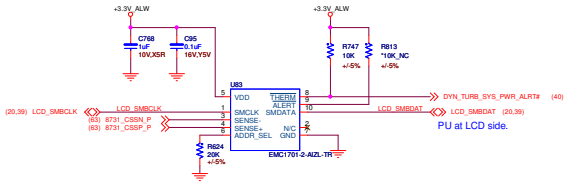
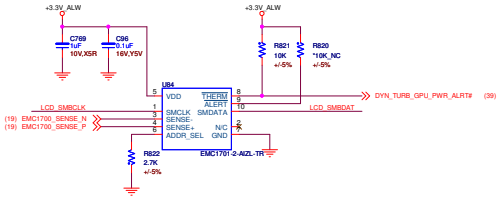
Monitor Charger current



RESISTOR (5%)	SMBUS ADDRESS	RESISTOR (5%)	SMBUS ADDRESS	
0	1001_100(r/w)	1600	0101_000(r/w)	
100	1001_101(r/w)	2000	0101_001(r/w)	
180	1001_110(r/w)	2700	0101_010(r/w)	U84
300	1001_111(r/w)	3600	0101_011(r/w)	
430	1001_000(r/w)	5600	0101_100(r/w)	
560	1001_001(r/w)	9100	0101_100(r/w)	
750	1001_010(r/w)	20000	0101_101(r/w)	U83
1270	1001_011(r/w)	Open	0111_000(r/w)	

Monitor PWR_SRC_MXM



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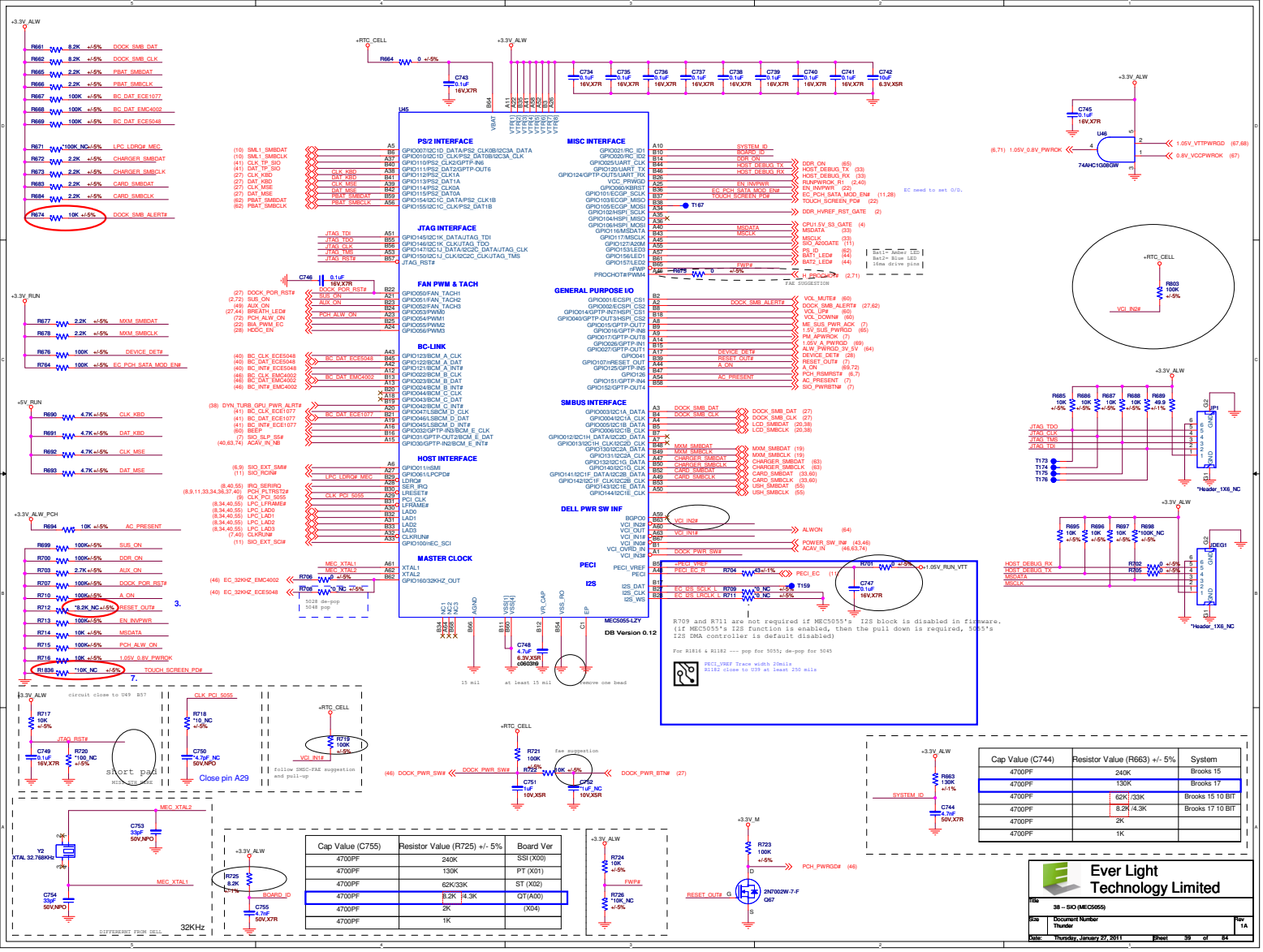
Title	38 -- Express Card & Power	
Size	Document Number: Thunder	Rev: 1A
Date: Thursday, January 27, 2011	Sheet 38 of 84	


PS/2 INTERFACE
JTAG INTERFACE
FAN PWM & TACH
BC-LINK
HOST INTERFACE
MASTER CLOCK
MISC INTERFACE
GENERAL PURPOSE I/O
SMBUS INTERFACE
DELL PWR SW INF
PECI
I2S
MEC5055-LZY
DB Version 0.12
R709 and R711 are not required if MEC5055's I2S block is disabled in firmware.
(if MEC5055's I2S function is enabled, then the pull down is required, 5055's I2S DMA controller is default disabled)
For R1816 & R1182 --- pop for 5055; de-pop for 5045
PECI_VREF Trace width 20mils
R1182 close to U39 at least 250 mils
short pad
Close pin A29
follow SMSC-FAE suggestion and pull-up
fae suggestion
DIFFERENT FROM DELL
32KHz
Cap Value (C744)
Resistor Value (R663) +/- 5%
System
4700PF
240K
Brooks 15
4700PF
130K
Brooks 17
4700PF
62K /33K
Brooks 15 10 BIT
4700PF
8.2K /4.3K
Brooks 17 10 BIT
4700PF
2K
4700PF
1K
Cap Value (C755)
Resistor Value (R725) +/- 5%
Board Ver
4700PF
240K
SSI (X00)
4700PF
130K
PT (X01)
4700PF
62K/33K
ST (X02)
4700PF
8.2K /4.3K
QT(A00)
4700PF
2K
(X04)
4700PF
1K
Ever Light Technology Limited
38 – SIO (MEC5055)
Document Number
Thunder
Rev 1A
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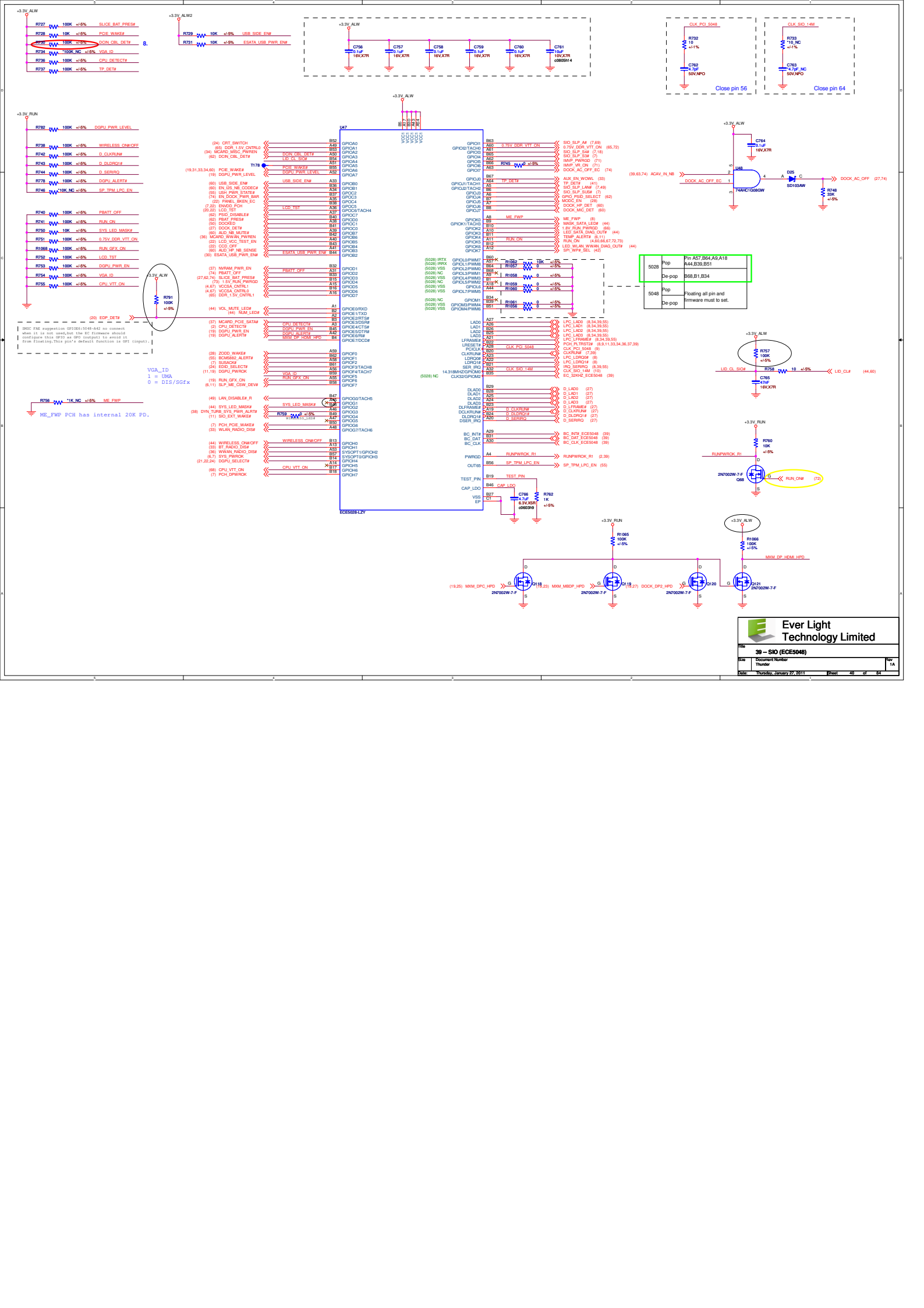
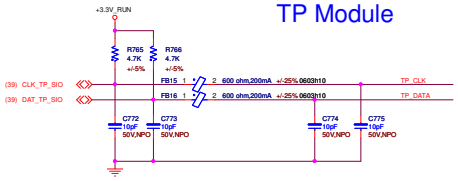
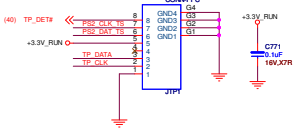

+3.3V_ALW
+3.3V_RUN
U47
ECE5028-LZY
Close pin 56
Close pin 64
Ever Light Technology Limited
39 -- SIO (ECE5048)
Thursday, January 27, 2011

TP Module

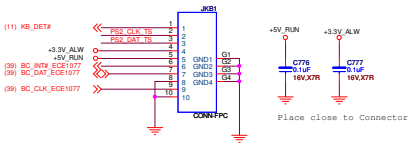


0524GC: CIS OK



Keyboard Module

1116 update to CIS



Ever Light Technology Limited

Title	40 -- ECE1099+KB+TP		
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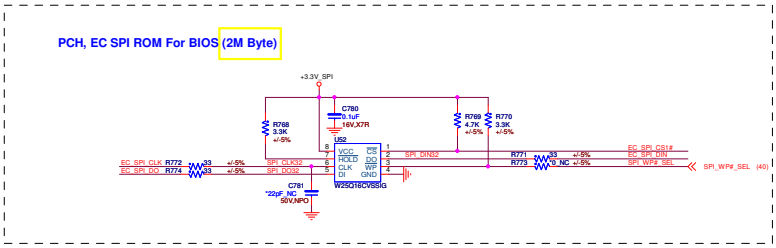

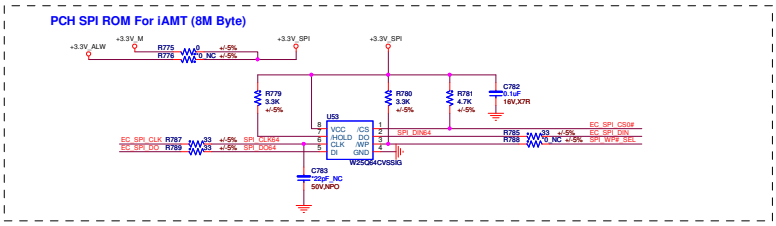

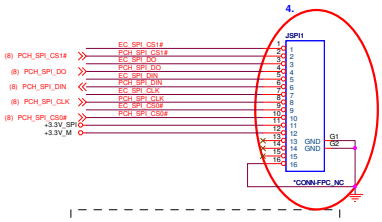

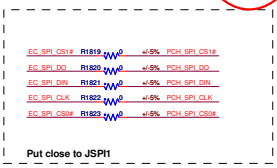

Ever Light Technology Limited

Title	41 -- BIOS ROM(4M+8M)	
Size	Document Number: Thunder	Rev: 1A
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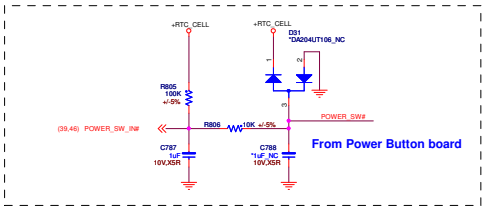
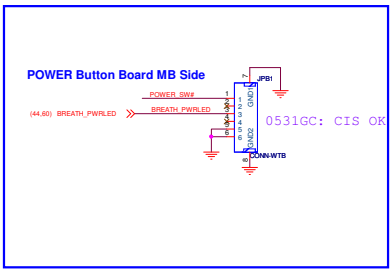
For AUX Module Conn

Remove AUX Module

7.





Ever Light Technology Limited		
Title	43 -- DB Connector x 7	
Size	Document Number: Thunder	Rev: 1A
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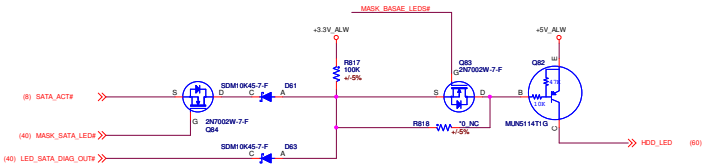
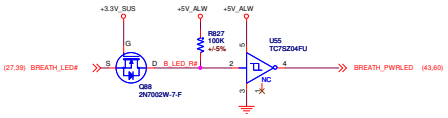
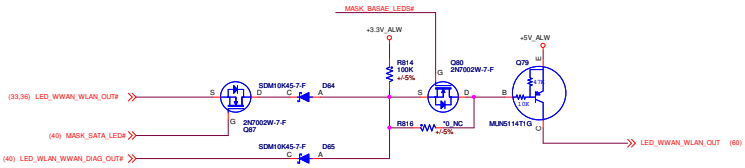
HDD

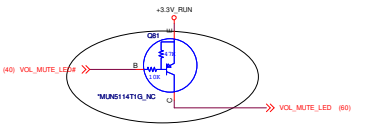


BREATH PWRLED

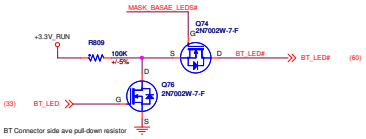


WWAN/WLAN

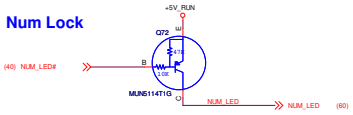




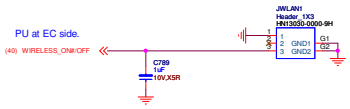
BT



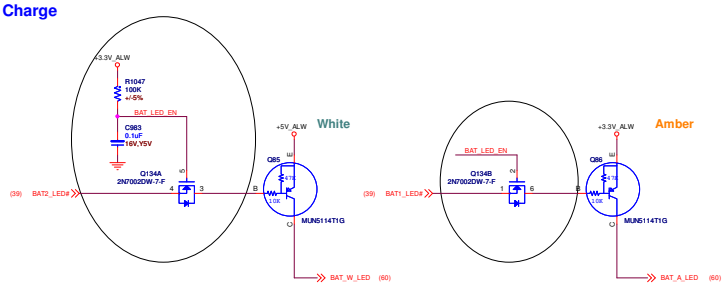
Num Lock

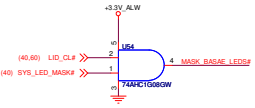


Wireless ON/OFF switch



Charge





Ever Light Technology Limited

Title	44 -- LED+Control, Wirele	
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DS_0412: should be on touch Pad module.

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Title	45 -- Hall sensor	
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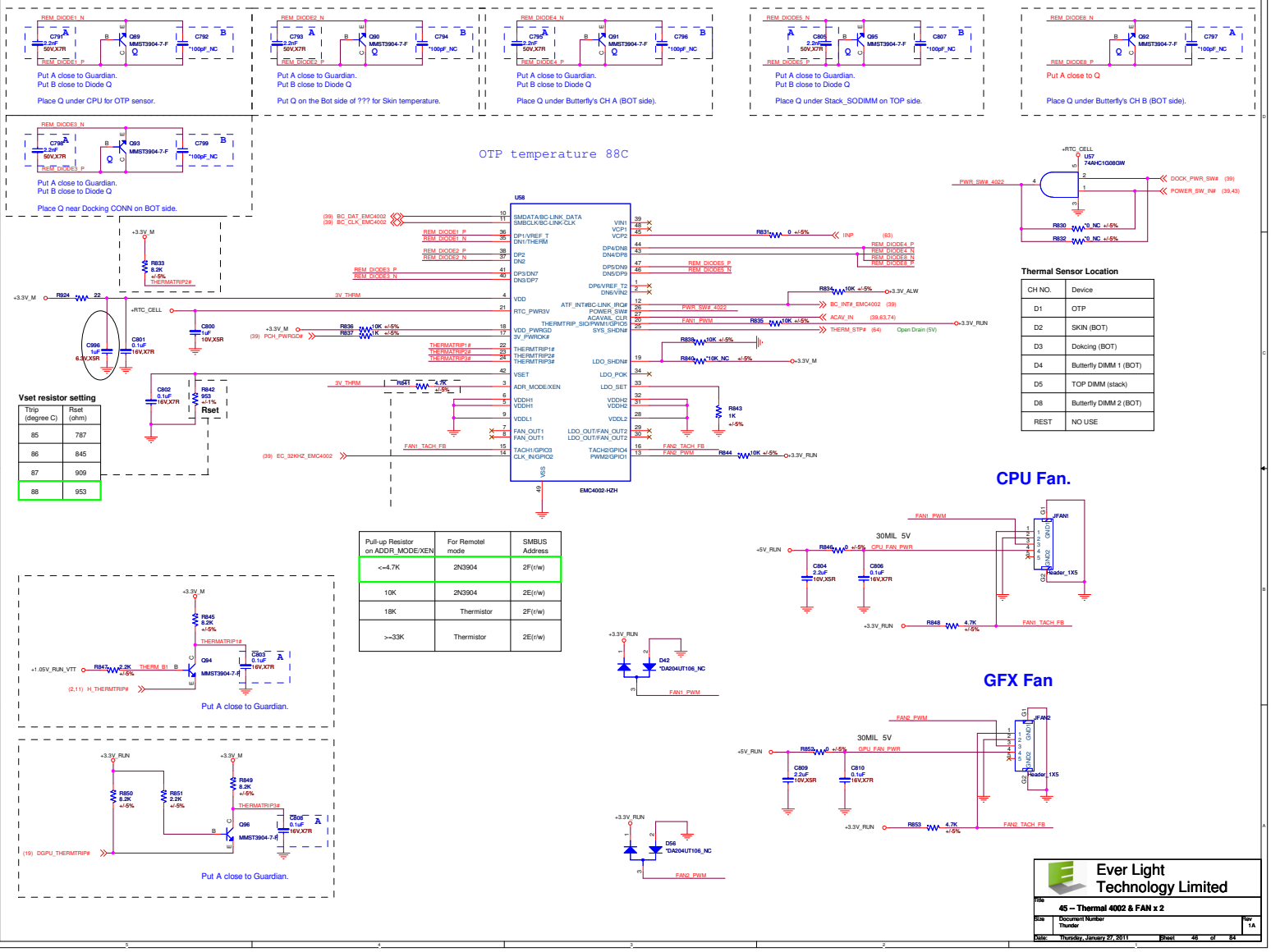
REM_DIODE1_N
C791 2.2nF 50V,X7R
Q89 MMST3904-7-F
C792 *100pF_NC
REM_DIODE1_P
Put A close to Guardian.
Put B close to Diode Q
Place Q under CPU for OTP sensor.
REM_DIODE2_N
C793 2.2nF 50V,X7R
Q90 MMST3904-7-F
C794 *100pF_NC
REM_DIODE2_P
Put A close to Guardian.
Put B close to Diode Q
Put Q on the Bot side of ??? for Skin temperature.
REM_DIODE4_N
C795 2.2nF 50V,X7R
Q91 MMST3904-7-F
C796 *100pF_NC
REM_DIODE4_P
Put A close to Guardian.
Put B close to Diode Q
Place Q under Butterfly's CH A (BOT side).
REM_DIODE5_N
C805 2.2nF 50V,X7R
Q95 MMST3904-7-F
C807 *100pF_NC
REM_DIODE5_P
Put A close to Guardian.
Put B close to Diode Q
Place Q under Stack_SODIMM on TOP side.
REM_DIODE8_N
C797
Q92 MMST3904-7-F
C798 *100pF_NC
REM_DIODE8_P
Put A close to Q
Place Q under Butterfly's CH B (BOT side).
REM_DIODE3_N
C796 2.2nF 50V,X7R
Q93 MMST3904-7-F
C799 *100pF_NC
REM_DIODE3_P
Put A close to Guardian.
Put B close to Diode Q
Place Q near Docking CONN on BOT side.
OTP temperature 88C
U58
EMC4002-HZH
+RTC_CELL
U57 74AHC1G08GW
PWR_SW#_4022
DOCK_PWR_SW# (39)
POWER_SW_IN# (39,43)
R830 *0_NC +/-5%
R832 *0_NC +/-5%
Thermal Sensor Location
CH NO. | Device
D1 | OTP
D2 | SKIN (BOT)
D3 | Dokcing (BOT)
D4 | Butterfly DIMM 1 (BOT)
D5 | TOP DIMM (stack)
D8 | Butterfly DIMM 2 (BOT)
REST | NO USE
Vset resistor setting
Trip (degree C) | Rset (ohm)
85 | 787
86 | 845
87 | 909
88 | 953
Pull-up Resistor on ADDR_MODE/XEN | For Remotel mode | SMBUS Address
<=4.7K | 2N3904 | 2F(r/w)
10K | 2N3904 | 2E(r/w)
18K | Thermistor | 2F(r/w)
>=33K | Thermistor | 2E(r/w)
CPU Fan.
JFAN1
Header_1X5
30MIL 5V
GFX Fan
JFAN2
Header_1X5
30MIL 5V
D42 *DA204UT106_NC
D56 *DA204UT106_NC
Ever Light Technology Limited
Title: 45 -- Thermal 4002 & FAN x 2
Size: Document Number: Thunder
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Title	47 -- AUDIO(92HD90B)+SPK+JACK	
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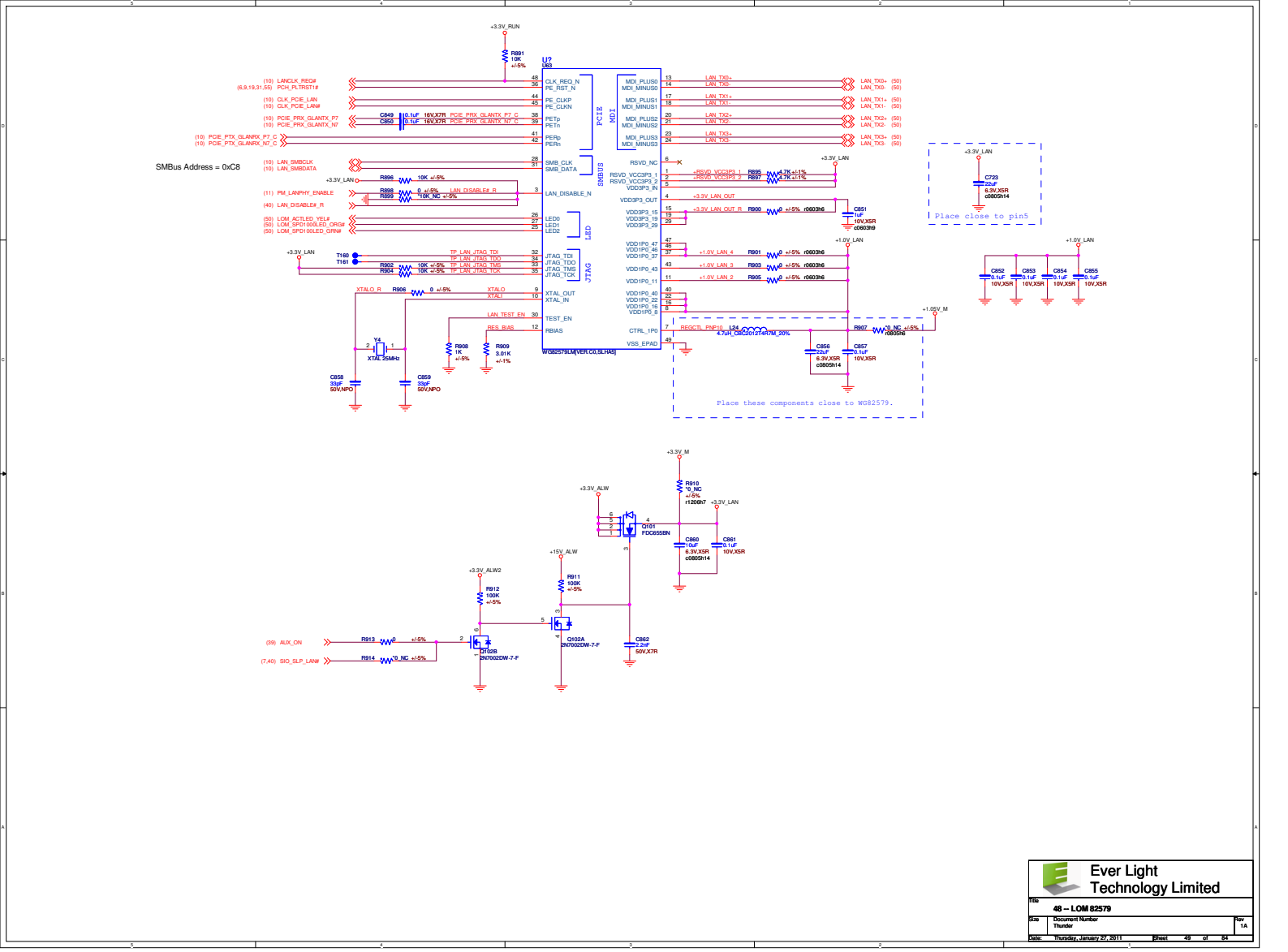
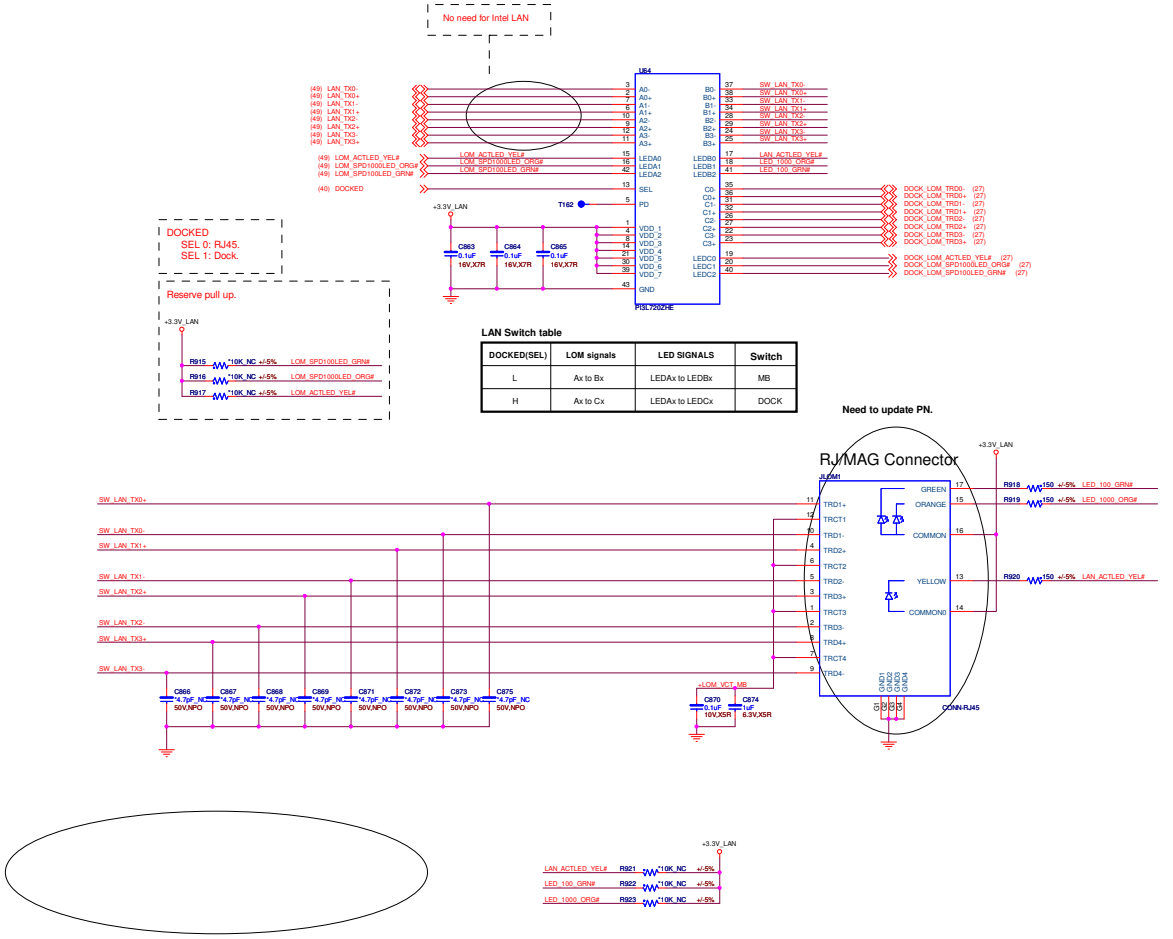
Title	48 -- AUDIO for Docking+Crystal	
Size	Document Number Thunder	Rev 1A
Date: Thursday, January 27, 2011	Sheet 48 of 84	



Ever Light Technology Limited	
Title	48 -- LOM 82579
Size	Document Number: Thunder; Rev: 1A
Date: Thursday, January 27, 2011	Sheet 49 of 84



LAN Switch table

DOCKED(SEL)	LOM signals	LED SIGNALS	Switch
L	Ax to Bx	LEDAx to LEDBx	MB
H	Ax to Cx	LEDAx to LEDCx	DOCK

Need to update PN.

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Title	49 -- RJ45+MID, MUX Switch	
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Title	50 – TPM for China	
Size	Document Number Thunder	Rev 1A
Date: Thursday, January 27, 2011	Sheet 51 of 84	

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Technology Limited

Title	51 -- Card Reader & Conn	
Size	Document Number Thunder	Rev 1A
Date: Thursday, January 27, 2011	Sheet 52 of 84	

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Technology Limited

Title	52 – 15" 1394 Conn	
Size	Document Number <Doc>	Rev 1A
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Title	53 – 17" 1394 Conn+ Power	
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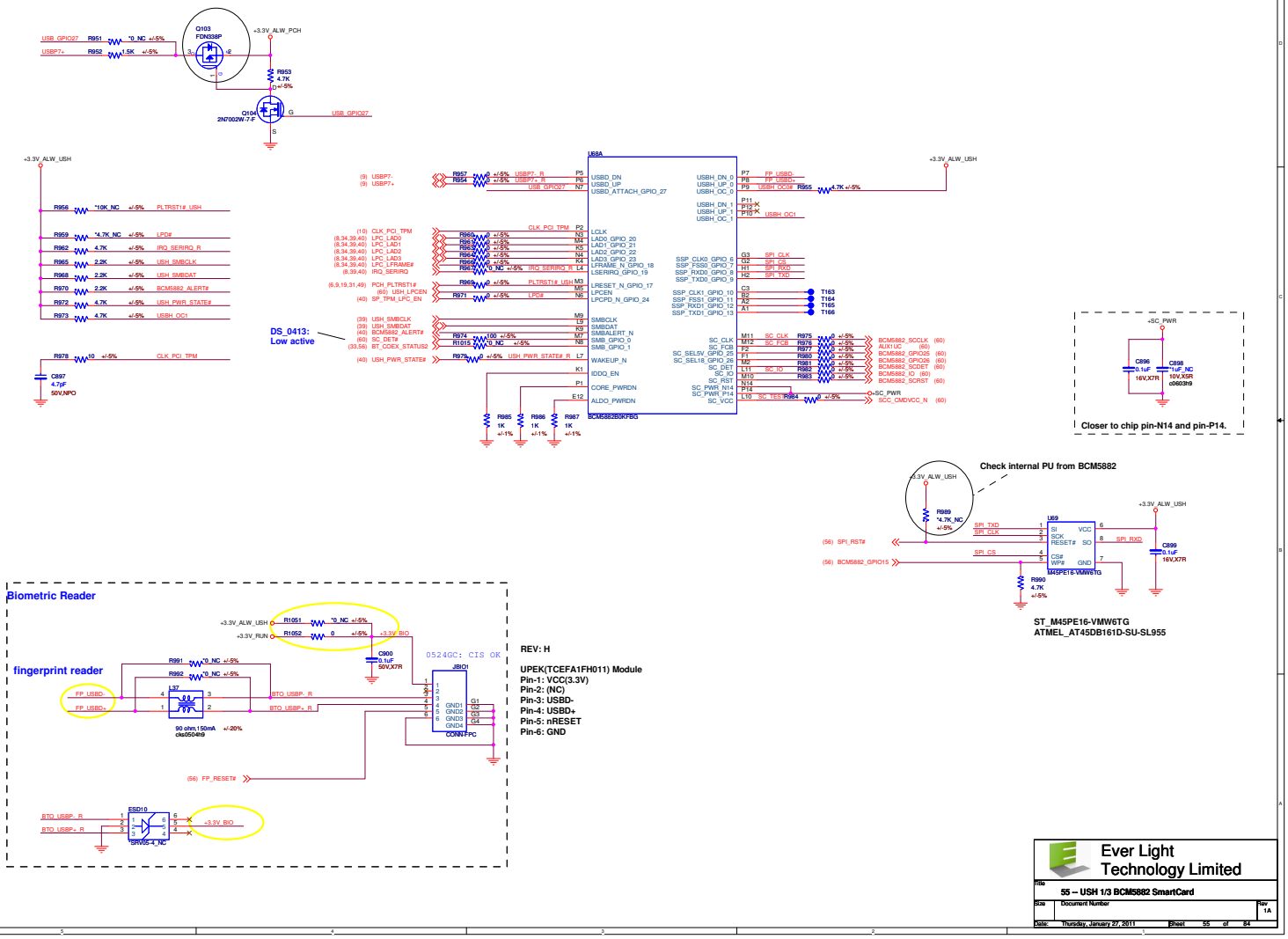
Q103
FDN338P
+3.3V_ALW_PCH
USB_GPIO27
R951 *0_NC +/-5%
USBP7+
R952 1.5K +/-5%
R953 4.7K +/-5%
Q104
2N7002W-7-F
USB_GPIO27
+3.3V_ALW_USH
R956 *10K_NC +/-5% PLTRST1#_USH
R959 *4.7K_NC +/-5% LPD#
R962 4.7K +/-5% IRQ_SERIRQ_R
R965 2.2K +/-5% USH_SMBCLK
R968 2.2K +/-5% USH_SMBDAT
R970 2.2K +/-5% BCM5882_ALERT#
R972 4.7K +/-5% USH_PWR_STATE#
R973 4.7K +/-5% USBH_OC1
R978 10 +/-5% CLK_PCI_TPM
C897 4.7pF 50V,NPO
DS_0413:
Low active
U69A
BCM5882B0KFBG
USBD_DN
USBD_UP
USBD_ATTACH_GPIO_27
R957 0 +/-5% USBP7_R
R954 0 +/-5% USBP7+_R
USB_GPIO27
USBH_DN_0
USBH_UP_0
USBH_OC_0
USBH_DN_1
USBH_UP_1
USBH_OC_1
FP_USBD-
FP_USBD+
USBH_OC0#
R955 4.7K +/-5%
+3.3V_ALW_USH
CLK_PCI_TPM
R960 0 +/-5%
R961 0 +/-5%
R963 0 +/-5%
R964 0 +/-5%
R966 0 +/-5%
R967 *0_NC +/-5% IRQ_SERIRQ_R
LCLK
LAD0_GPIO_20
LAD1_GPIO_21
LAD2_GPIO_22
LAD3_GPIO_23
LFRAME_N_GPIO_18
LSERIRQ_GPIO_19
R969 0 +/-5% PLTRST1#_USH
R971 0 +/-5% LPD#
LRESET_N_GPIO_17
LPCPD_N_GPIO_24
LPCEN
SSP_CLK0_GPIO_6
SSP_FSS0_GPIO_7
SSP_RXD0_GPIO_8
SSP_TXD0_GPIO_9
SPI_CLK
SPI_CS
SPI_RXD
SPI_TXD
SSP_CLK1_GPIO_10
SSP_FSS1_GPIO_11
SSP_RXD1_GPIO_12
SSP_TXD1_GPIO_13
T163
T164
T165
T166
SMBCLK
SMBDAT
SMBALERT_N
SMB_GPIO_0
SMB_GPIO_1
R974 100 +/-5%
R1015 *0_NC +/-5%
R975 0 +/-5% BCM5882_SCCLK (60)
R976 0 +/-5% AU41UC (60)
R977 0 +/-5% BCM5882_GPIO25 (60)
R980 0 +/-5% BCM5882_GPIO26 (60)
R981 0 +/-5% BCM5882_SCDET (60)
R982 0 +/-5% BCM5882_IO (60)
R983 0 +/-5% BCM5882_SCRST (60)
R984 0 +/-5%
+SC_PWR
SCC_CMDVCC_N (60)
SC_CLK
SC_FCB
SC_SEL5V_GPIO_25
SC_SEL18_GPIO_26
SC_DET
SC_IO
SC_RST
SC_PWR_N14
SC_PWR_P14
SC_VCC
SC_TES
R971 0 +/-5% LPD#
R972 0 +/-5% USH_PWR_STATE#_R
WAKEUP_N
IDDQ_EN
CORE_PWRDN
ALDO_PWRDN
R985 1K +/-1%
R986 1K +/-1%
R987 1K +/-1%
+SC_PWR
C896 0.1uF 16V,X7R
C898 1uF_NC 10V,X5R c0603h9
Closer to chip pin-N14 and pin-P14.
Check internal PU from BCM5882
+3.3V_ALW_USH
R989 *4.7K_NC +/-5%
U69
M45PE16-VMW6TG
SPI_TXD
SPI_CLK
SPI_RST#
SPI_CS
BCM5882_GPIO15
SPI_RXD
C899 0.1uF 16V,X7R
R990 4.7K +/-5%
ST_M45PE16-VMW6TG
ATMEL_AT45DB161D-SU-SL955
Biometric Reader
fingerprint reader
+3.3V_ALW_USH
+3.3V_RUN
R1051 *0_NC +/-5%
R1052 0 +/-5%
+3.3V_BIO
C900 0.1uF 50V,X7R
0524GC: CIS OK
R991 *0_NC +/-5%
R992 *0_NC +/-5%
JBIO1
CONN-FPC
FP_USBD-
FP_USBD+
L37
BTO_USBP-_R
BTO_USBP+_R
90 ohm,150mA +/-20%
cis0504h9
(56) FP_RESET#
ESD10
SRV05-4_NC
REV: H
UPEK(TCEFA1FH011) Module
Pin-1: VCC(3.3V)
Pin-2: (NC)
Pin-3: USBD-
Pin-4: USBD+
Pin-5: nRESET
Pin-6: GND
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55 -- USH 1/3 BCM5882 SmartCard
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JTAG_TDI_USH R994 *0_NC +/-5% JTAG_CLK_USH

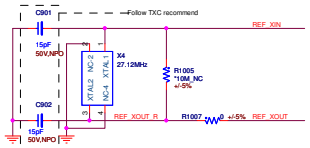
JTAG_TMS_USH R995 *0_NC +/-5% JTAG_TDO_USH

JTCE_USH R996 *0_NC +/-5% JTAG_RST#_USH

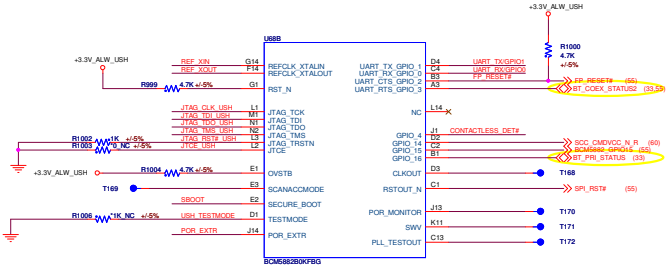
HF_RX_TEST1 R997 *0_NC +/-5% HF_RX_TEST0

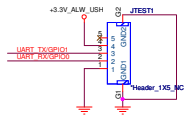
HF_RX_TEST3 R998 *0_NC +/-5% HF_RX_TEST2

27.12Mhz regardless support RFID or not.



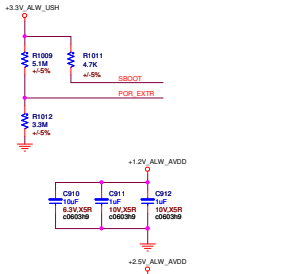
* XTAL CIRCUIT (COMPONENTS + WIRING) SHOULD BE ON TOP LAYER ONLY, TO CONTROL INTERFERENCE

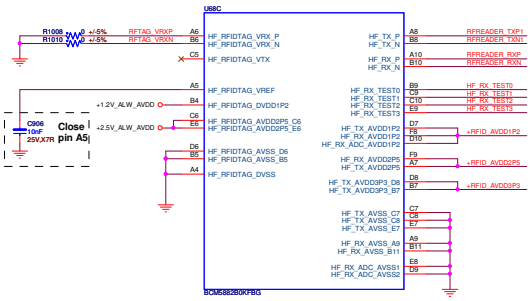


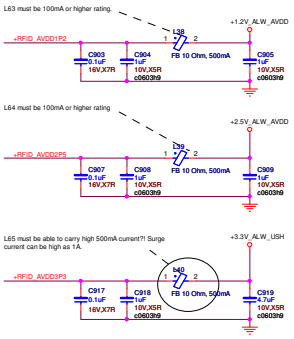


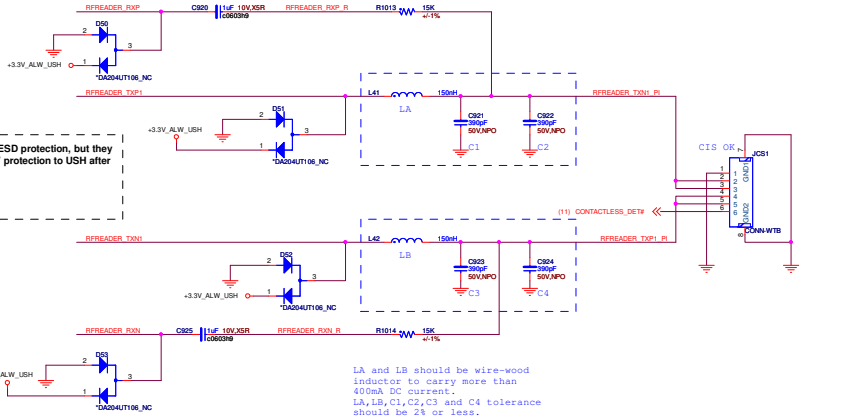
UART_TX/GPIO1, UART_RX_GPIO0, 3.3V_ALW_USH and GND to a connector. This is required for BIOS/FW debugging and EVMCo certification test.

Connector should be placed in place to be easy access by opening cover. Connector can be depop for production.









BRCM : D87, D88, D89, D90 are required for ESD protection, but they could be removed if ODM can guarantee 8kV protection to USH after contacted ESD test.

Note: USH only protect upto 2kV at I/O pins.

LA and LB should be wire-wood inductor to carry more than 400mA DC current.
LA,LB,C1,C2,C3 and C4 tolerance should be 2% or less.

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Title	56 -- USH 2/3 BCM5882 RFID	
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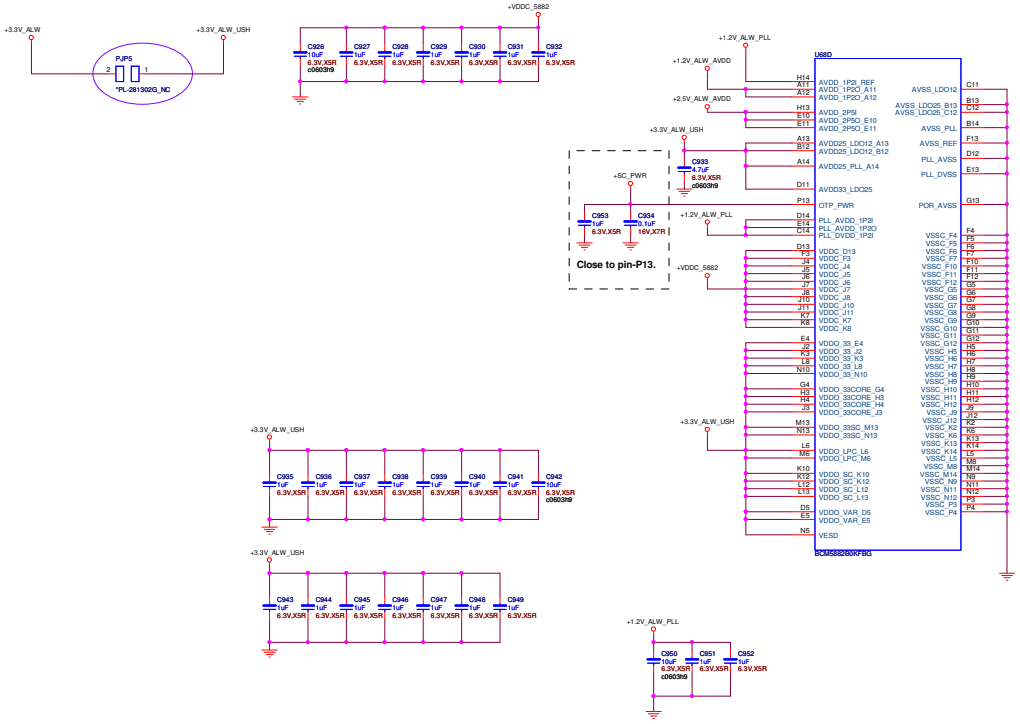

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Title	57 -- USH 3/3 BCM5882 Power	
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Title: 58 -- Smart Card IC & Conn

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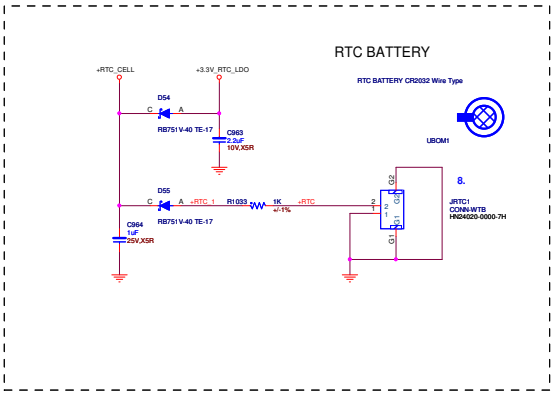

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Title	58 -- System Reset, RTC	
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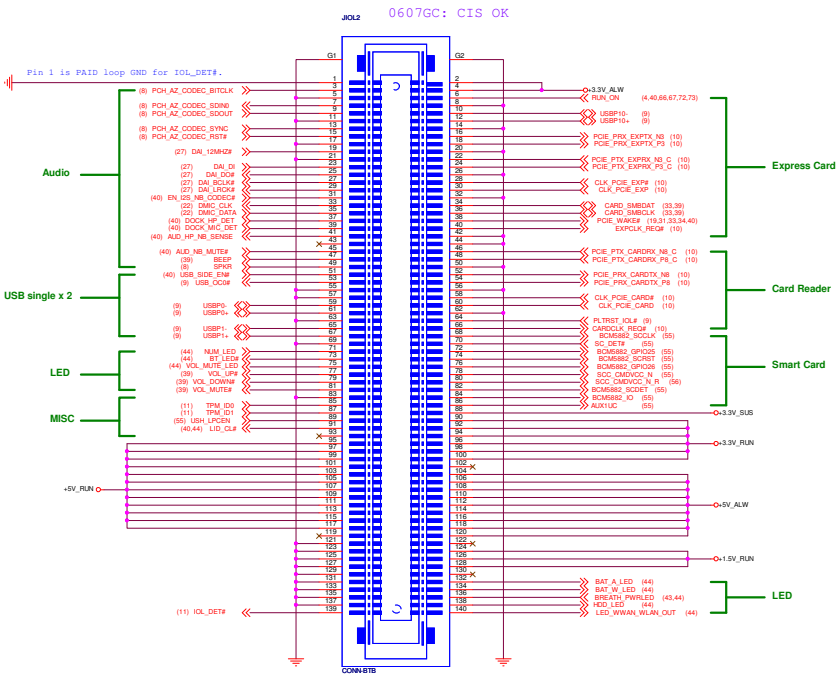

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Title	76 -- Blank Page	
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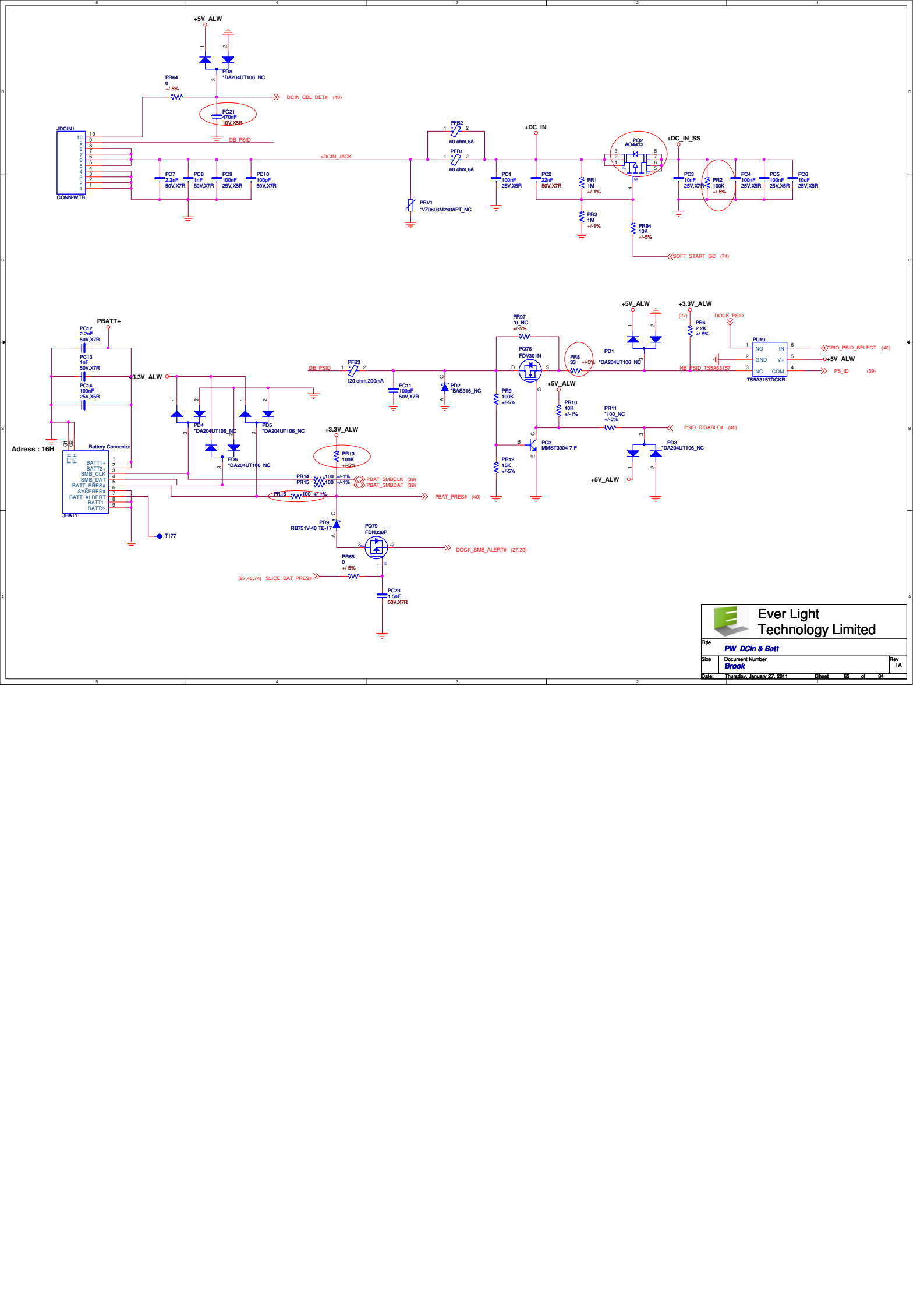
+5V_ALW
PD8
*DA204UT106_NC
PR64
0
+/-5%
DCIN_CBL_DET# (40)
PC21
470nF
10V,X5R
DB_PSID
JDCIN1
CONN-WTB
+DCIN_JACK
PC7
2.2nF
50V,X7R
PC8
1nF
50V,X7R
PC9
100nF
25V,X5R
PC10
100pF
50V,X7R
PFB2
60 ohm,6A
PFB1
60 ohm,6A
PRV1
*VZ0603M260APT_NC
+DC_IN
PC1
100nF
25V,X5R
PC2
22nF
50V,X7R
PR1
1M
+/-1%
PR3
1M
+/-1%
PQ2
AO4413
+DC_IN_SS
PC3
10nF
25V,X7R
PR2
100K
+/-5%
PC4
100nF
25V,X5R
PC5
100nF
25V,X5R
PC6
10uF
25V,X5R
PR94
10K
+/-5%
SOFT_START_GC (74)
PBATT+
PC12
2.2nF
50V,X7R
PC13
1nF
50V,X7R
PC14
100nF
25V,X5R
+3.3V_ALW
Adress : 16H
Battery Connector
JBAT1
BATT1+
BATT2+
SMB_CLK
SMB_DAT
BATT_PRES#
SYSPRES#
BATT_ALBERT
BATT1-
BATT2-
T177
PD4
*DA204UT106_NC
PD5
*DA204UT106_NC
PD6
*DA204UT106_NC
DB_PSID
PFB3
120 ohm,200mA
PC11
100pF
50V,X7R
PD2
*BAS316_NC
PR97
*0_NC
+/-5%
PQ76
FDV301N
PR8
33
+/-5%
PD1
*DA204UT106_NC
+5V_ALW
PR9
100K
+/-5%
PR10
10K
+/-1%
PR11
*100_NC
+/-5%
PSID_DISABLE# (40)
PQ3
MMST3904-7-F
PR12
15K
+/-5%
PD3
*DA204UT106_NC
+5V_ALW
+3.3V_ALW
(27)
PR6
2.2K
+/-5%
DOCK_PSID
PU19
NO
GND
NC
IN
V+
COM
TS5A3157DCKR
GPIO_PSID_SELECT (40)
+5V_ALW
PS_ID (39)
NB_PSID_TS5A63157
+3.3V_ALW
PR13
100K
+/-5%
PR14
100
+/-1%
PR15
100
+/-1%
PBAT_SMBCLK (39)
PBAT_SMBDAT (39)
PR16
100
+/-1%
PBAT_PRES# (40)
PD9
RB751V-40 TE-17
PQ79
FDN338P
DOCK_SMB_ALERT# (27,39)
PR65
0
+/-5%
(27,40,74) SLICE_BAT_PRES#
PC23
1.5nF
50V,X7R
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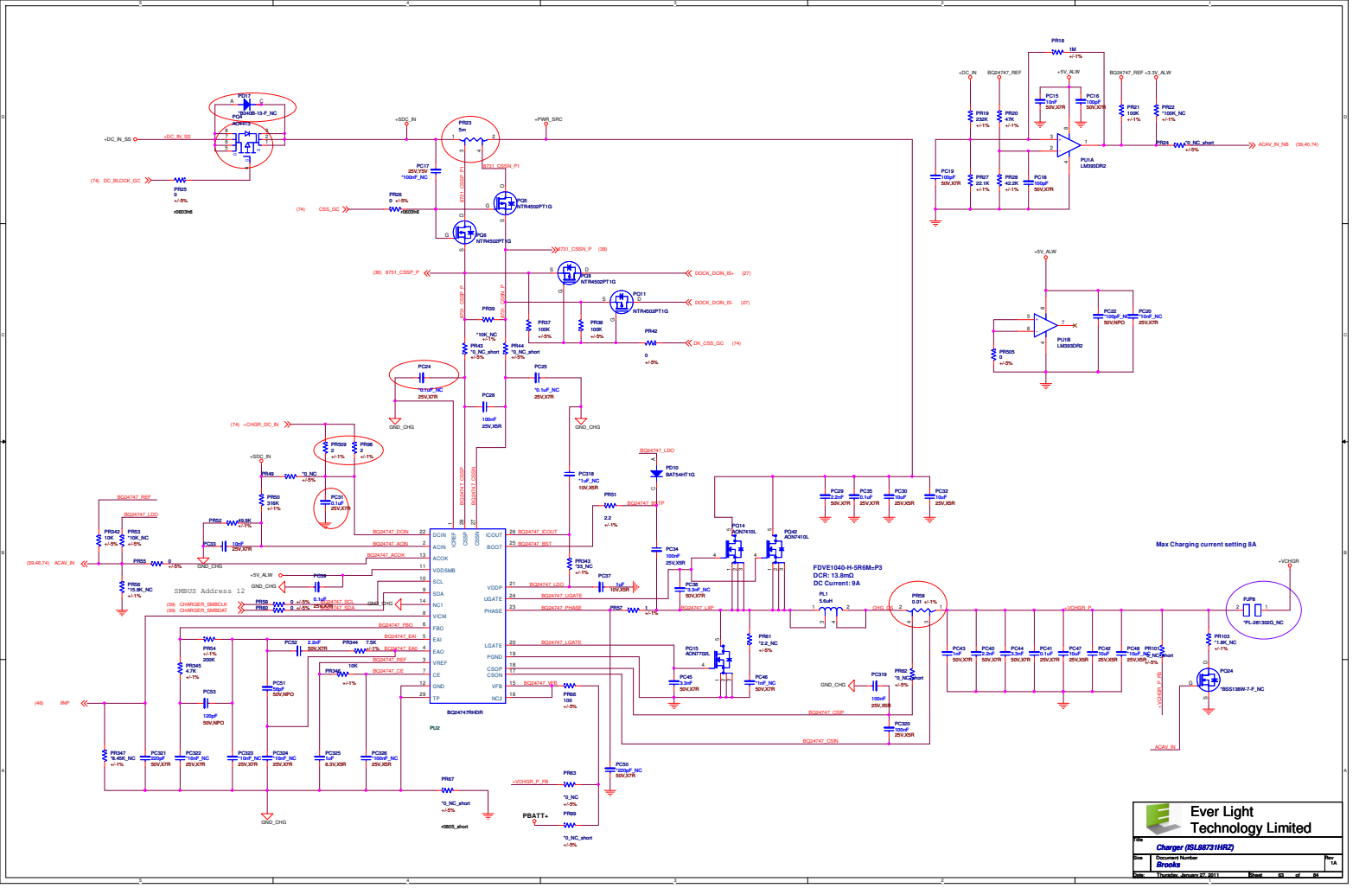
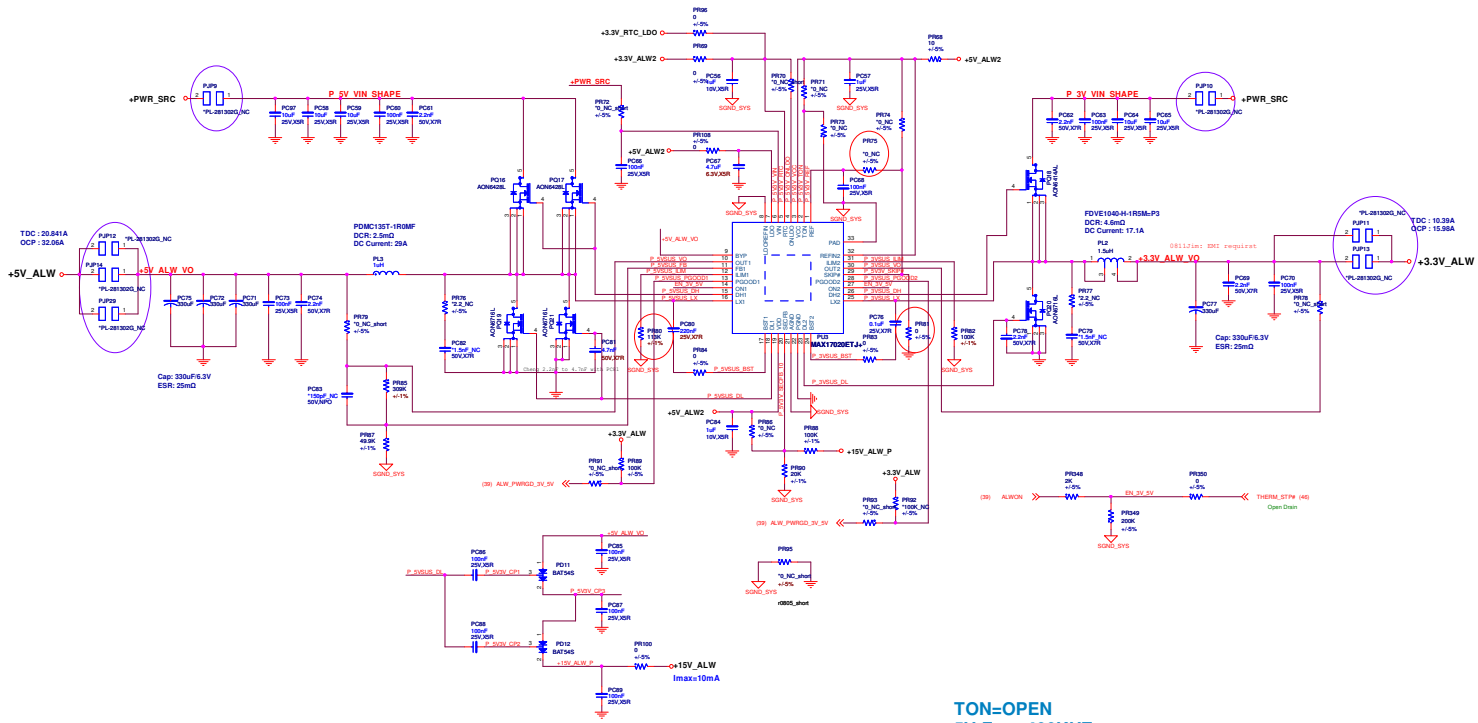

Max Charging current setting 8A
FDVE1040-H-5R6M=P3
DCR: 13.8mΩ
DC Current: 9A
SMBUS Address 12
BQ24747RHDR
Ever Light
Technology Limited
Charger (ISL88731HRZ)
Brooks
Thursday, January 27, 2011

+5V_ALW / +3.3V_ALW POWER SUPPLY



TON=OPEN
5V:Fsw=400KHZ
3V:Fsw=300KHZ
SKIP#=VCC=>Forced-PWM mode
SKIP#=REF=>Ultrasonic mode
SKIP#=GND=>Pulse-skipping mode

<Variant Name>

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File: PW_SYSTEM(MAX17020)

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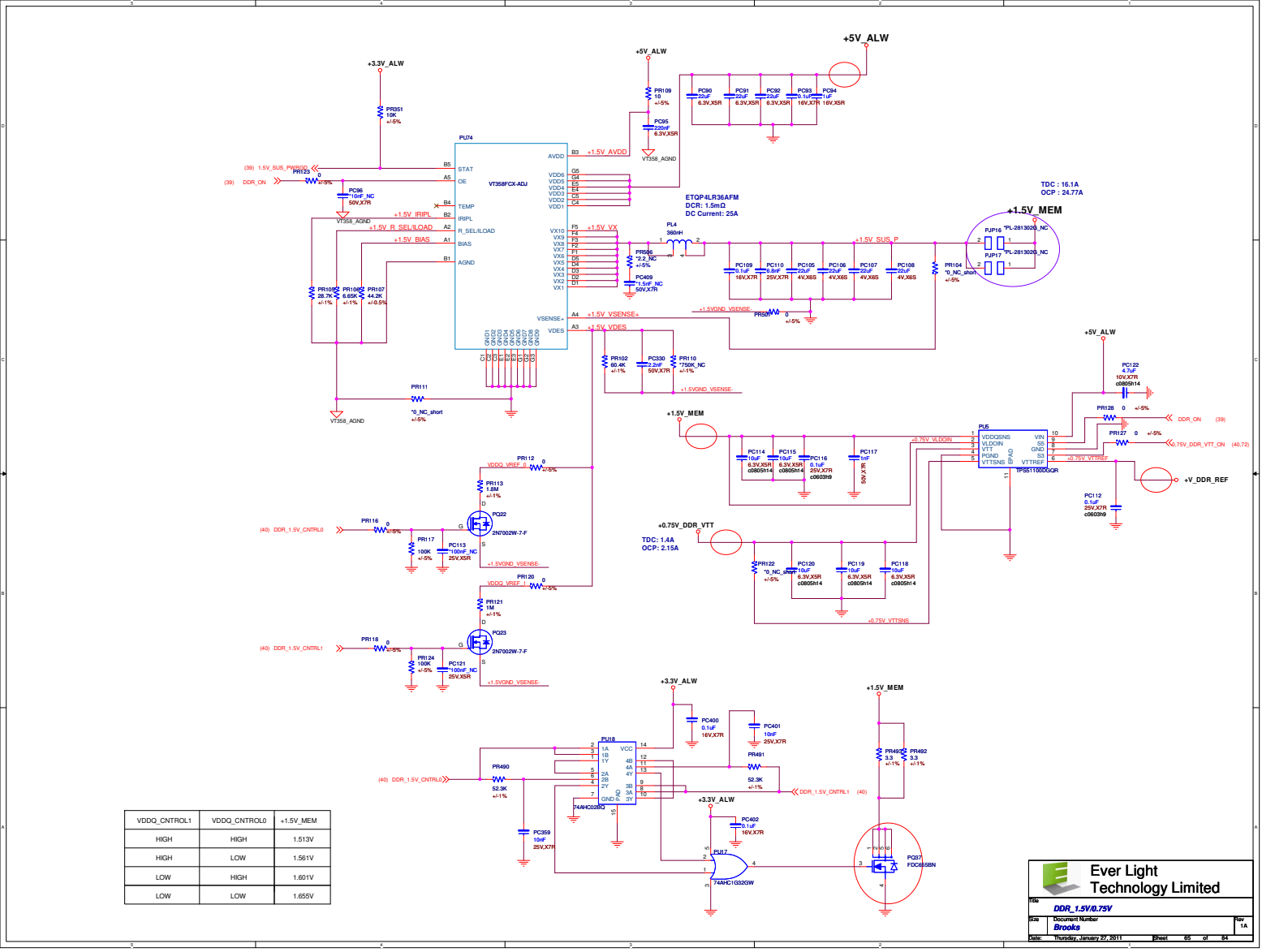

VDDQ_CNTROL1	VDDQ_CNTROL0	+1.5V_MEM
HIGH	HIGH	1.513V
HIGH	LOW	1.561V
LOW	HIGH	1.601V
LOW	LOW	1.655V

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Title	DDR_1.5V/0.75V	
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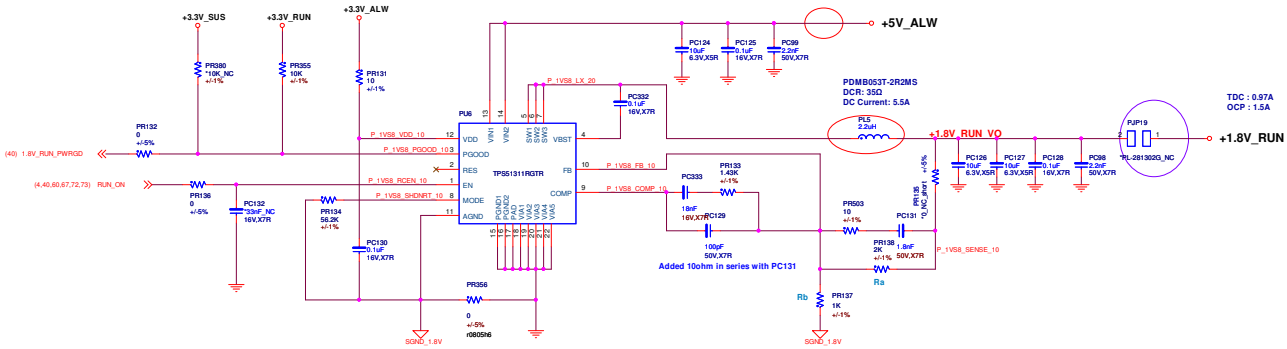
+1.8V_RUN POWER SUPPLY



<Variant Name>

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Title	PW_SW_+1.8V(TPS51311)	
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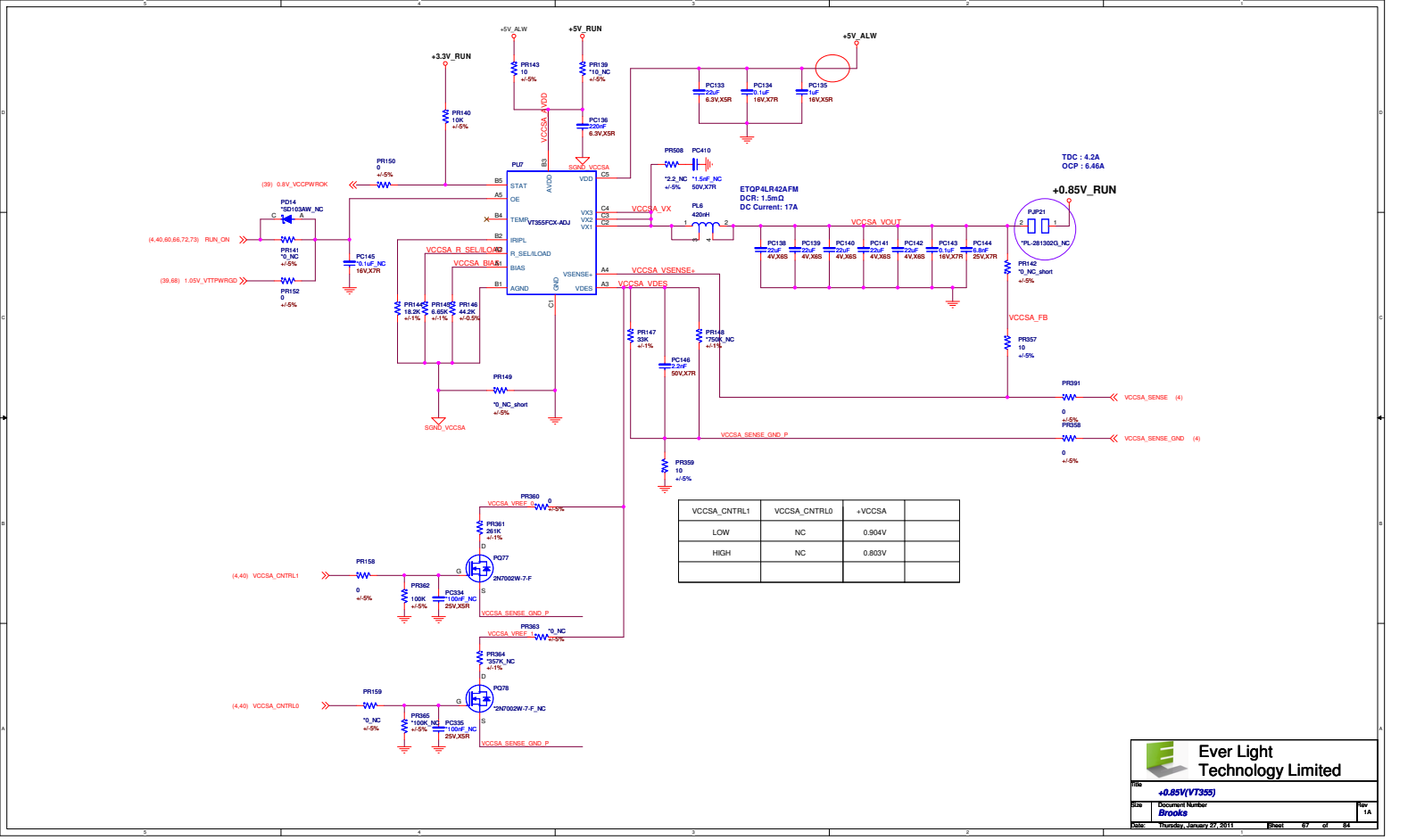

VCCSA_CNTRL1	VCCSA_CNTRL0	+VCCSA	
LOW	NC	0.904V	
HIGH	NC	0.803V	

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Title	+0.85V(VT355)	
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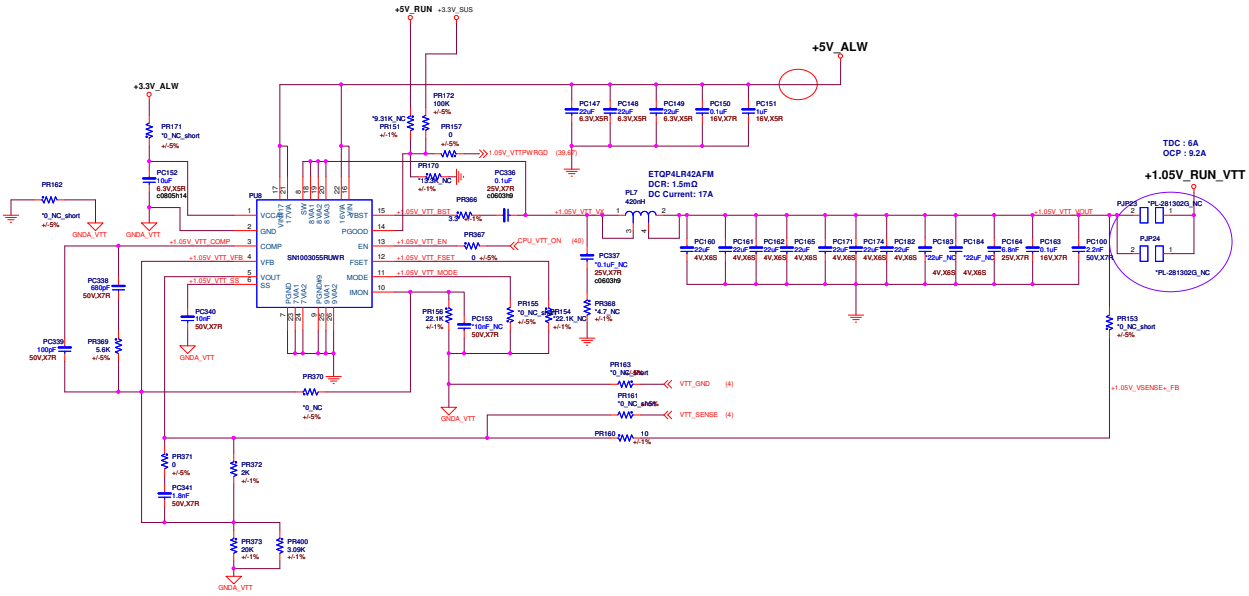

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Title	PW_+1.05V_VTT(SN1003055RUWR)	
Size	Document Number: Brooks	Rev: 1A
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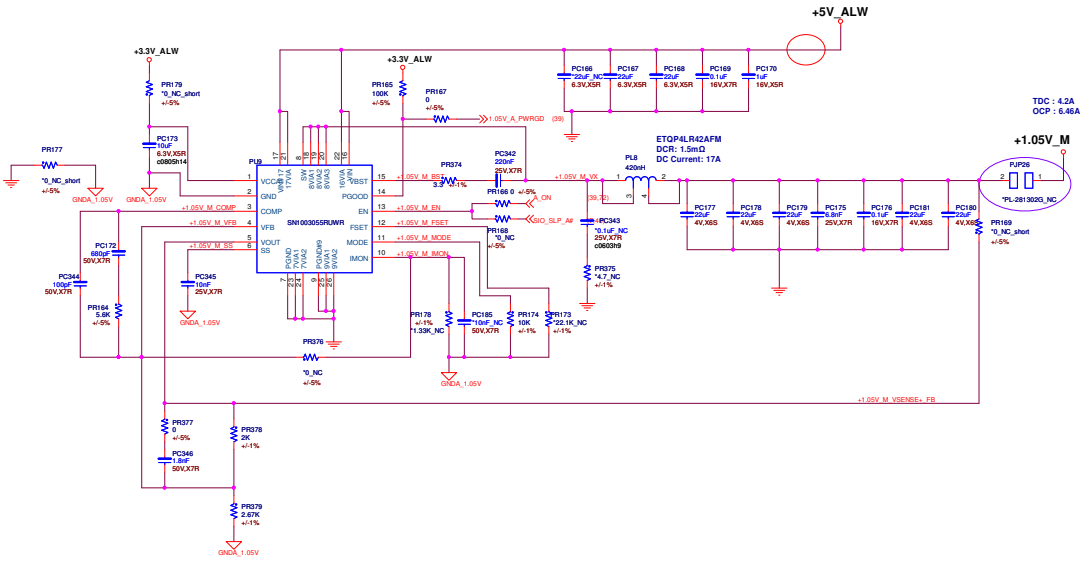

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Title	PW_+1.05VM(VT355)	
Size	Document Number: Brooks	Rev: 1A
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Title	<Title>
Size: A	Document Number: <Doc>
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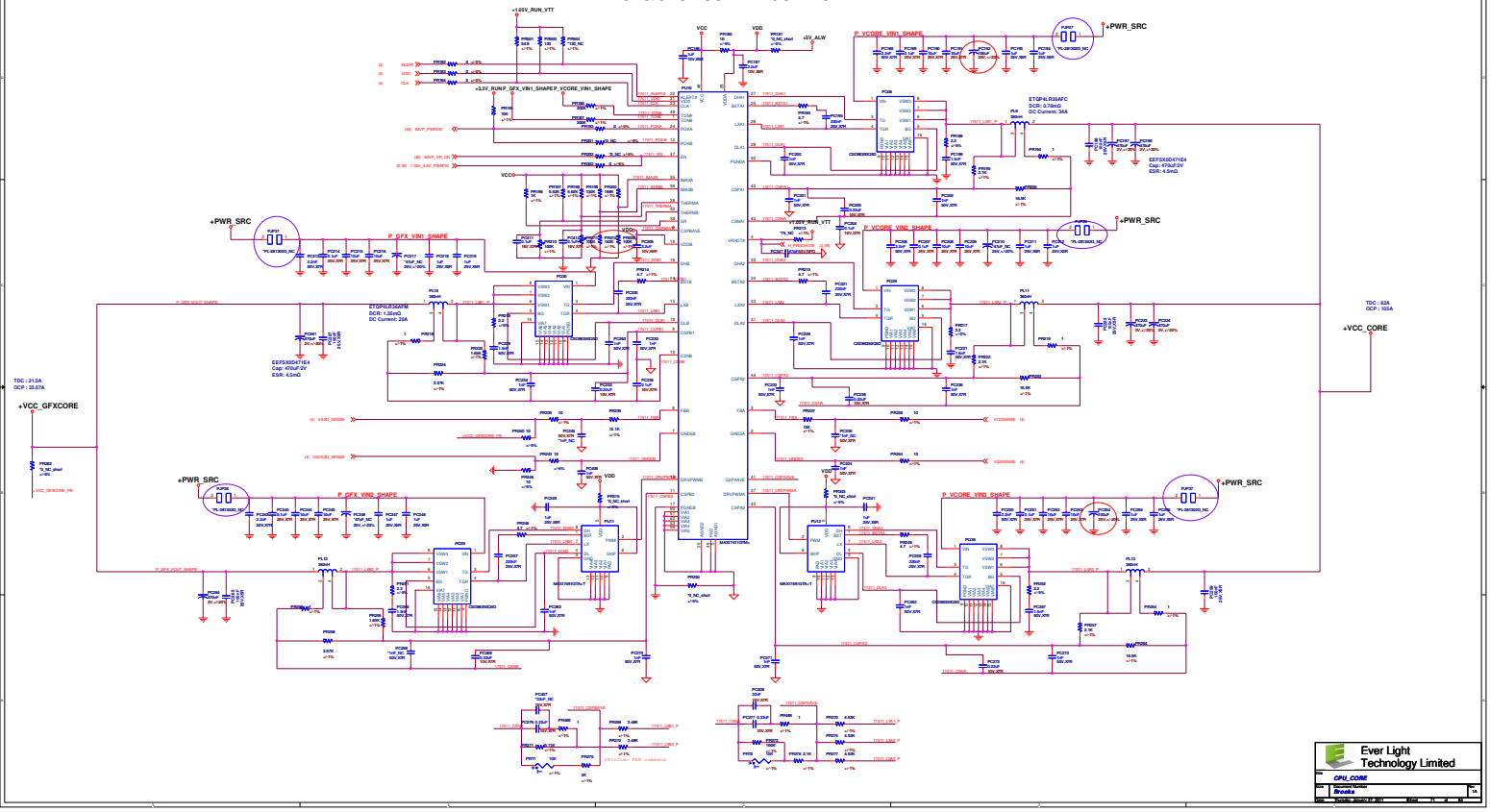
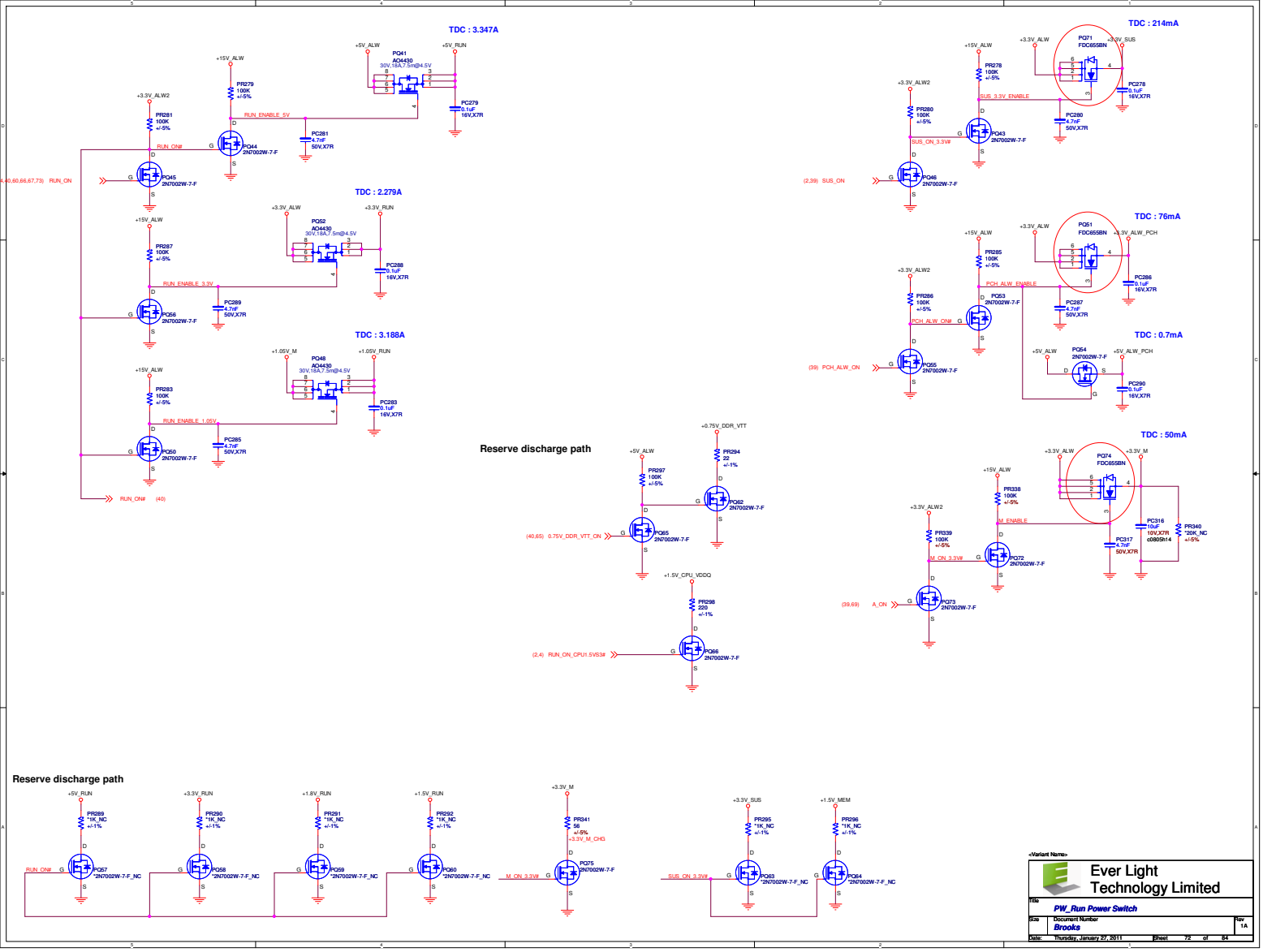
IMVP7 CPU/GPU VCORE REGULATOR





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Title	PW_Run Power Switch	
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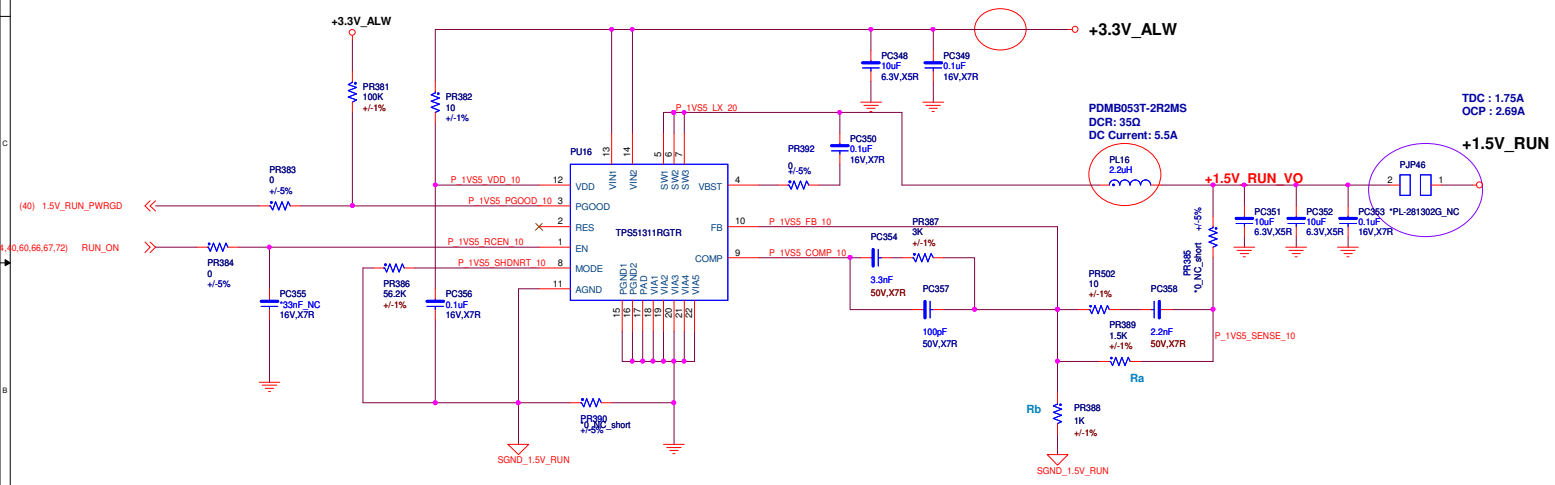
+1.5V_RUN POWER SUPPLY



<Variant Name>

Ever Light Technology Limited

Title	PW_SW_+1.8V(TPS51311)	
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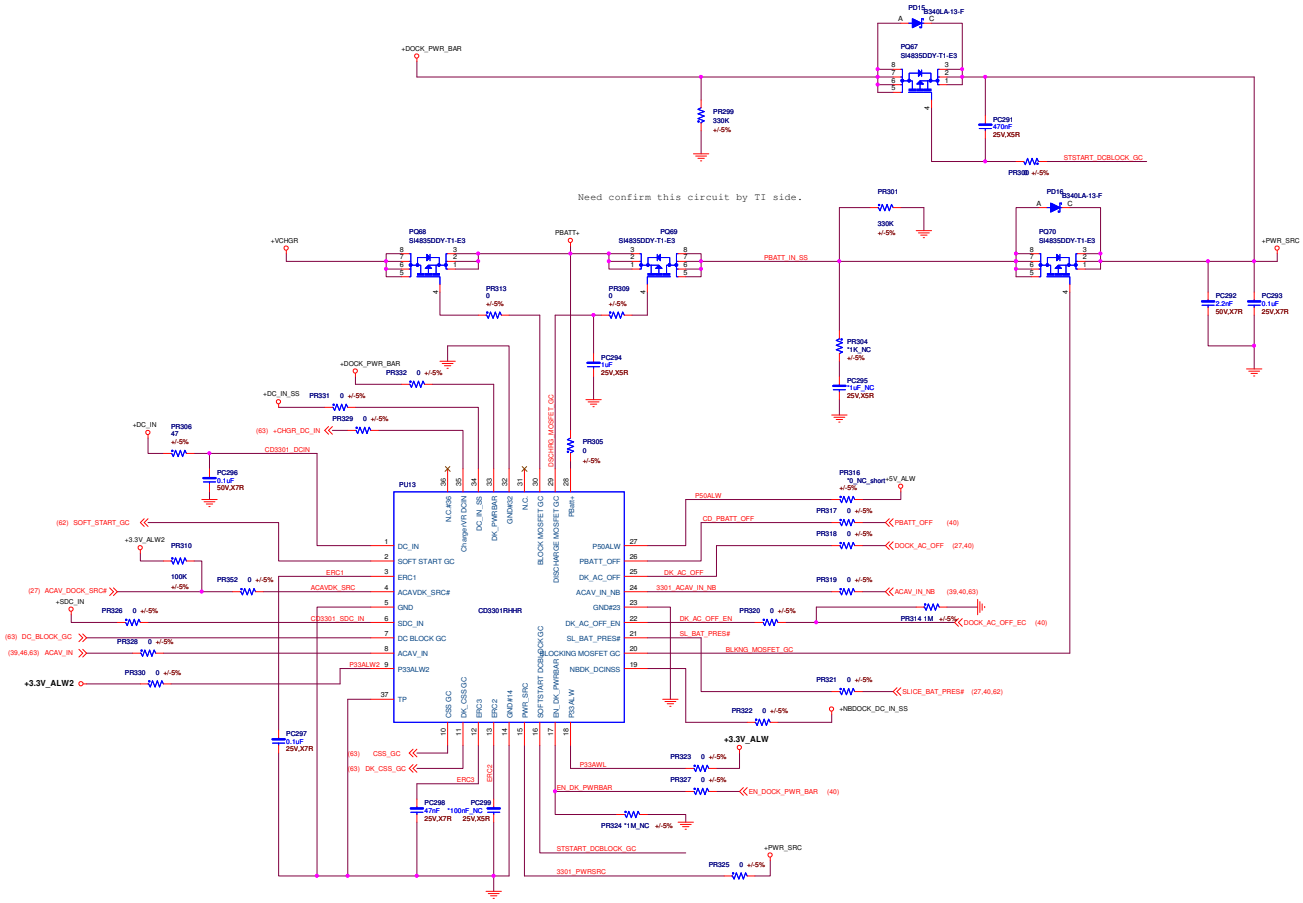

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Title	Docking Selector(CD3301)	
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Title: +12V_1394(MAX688)

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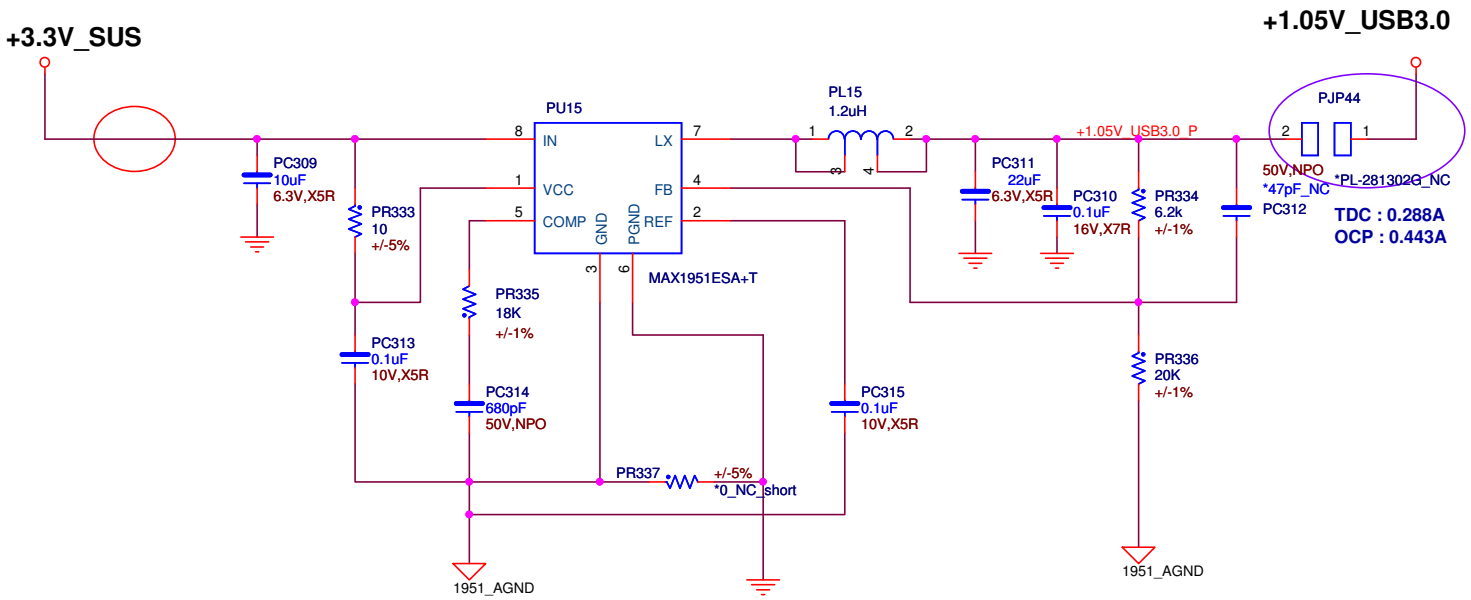

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Title	*+1.05V_USB3.0*	
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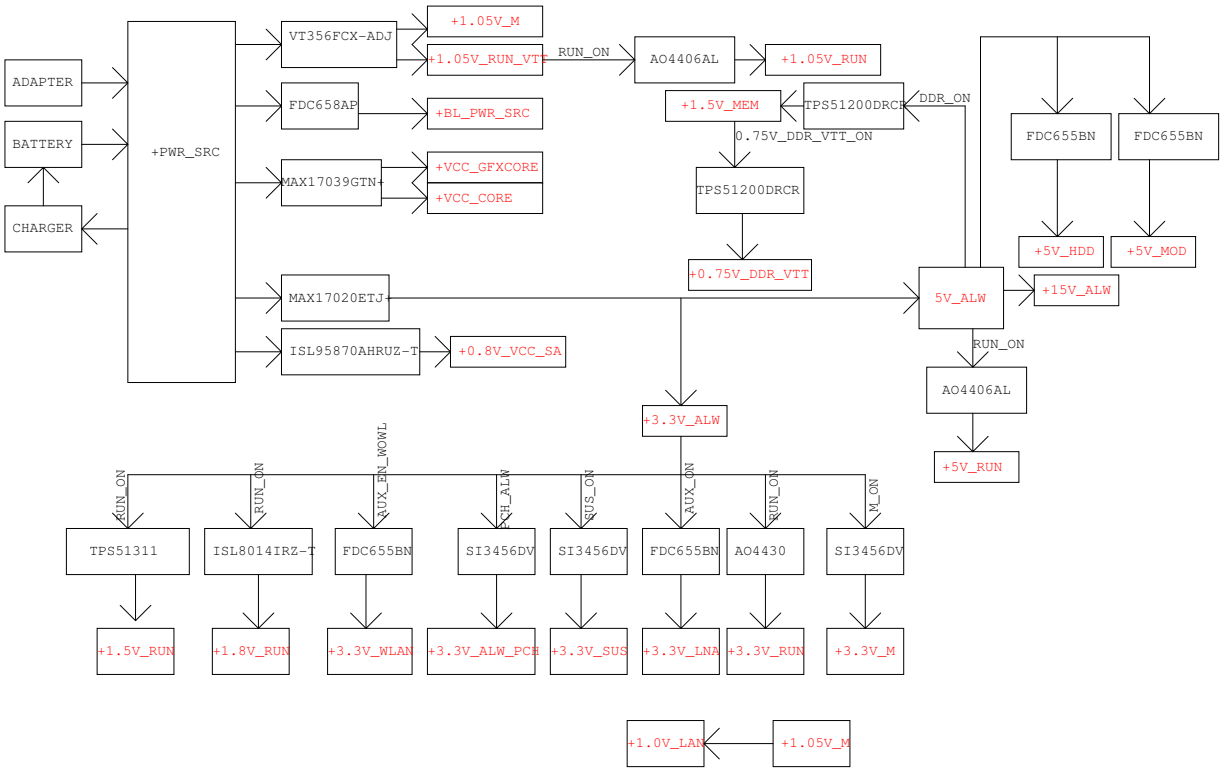

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Title	99 -- Media Control	
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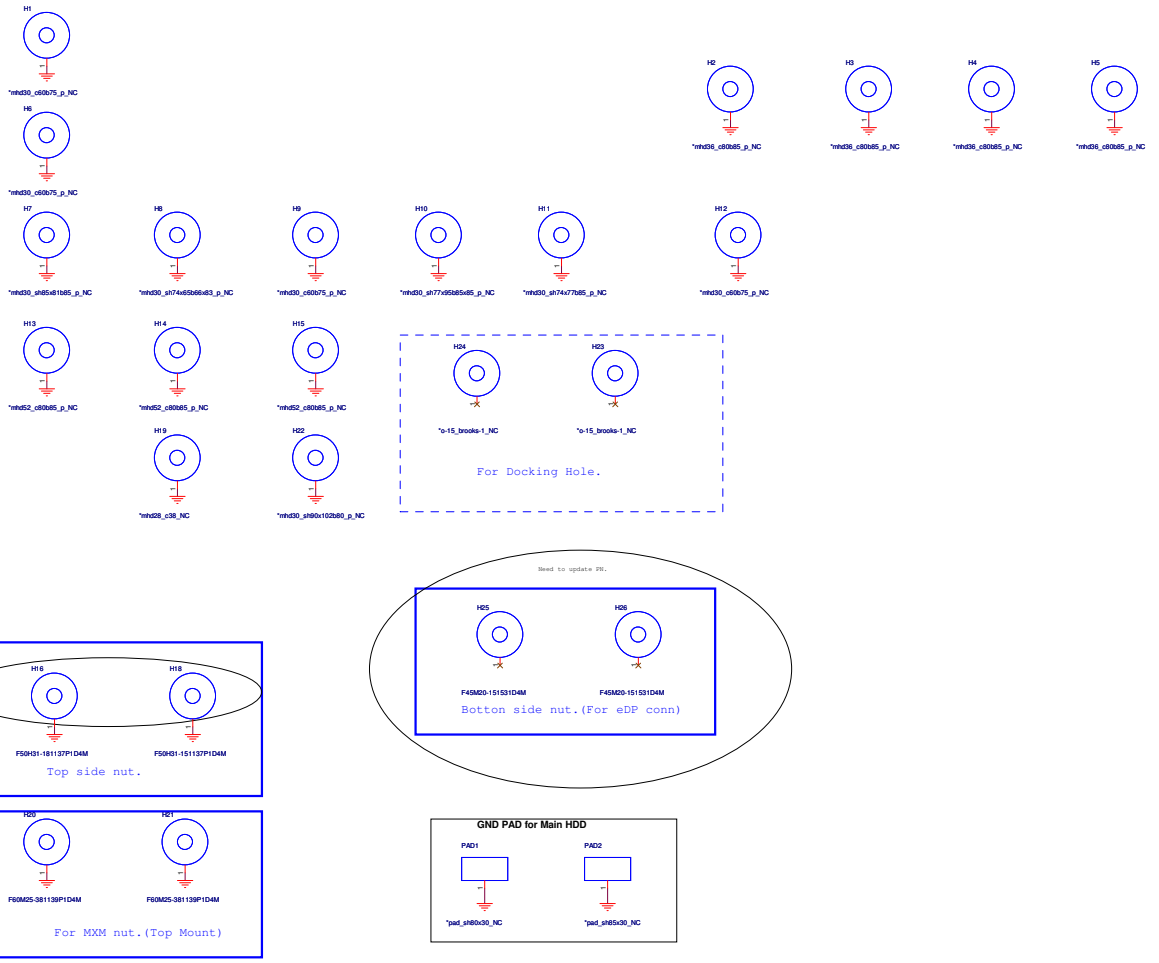

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Title	71 -- PAD,SCREW & Stiching CAPs	
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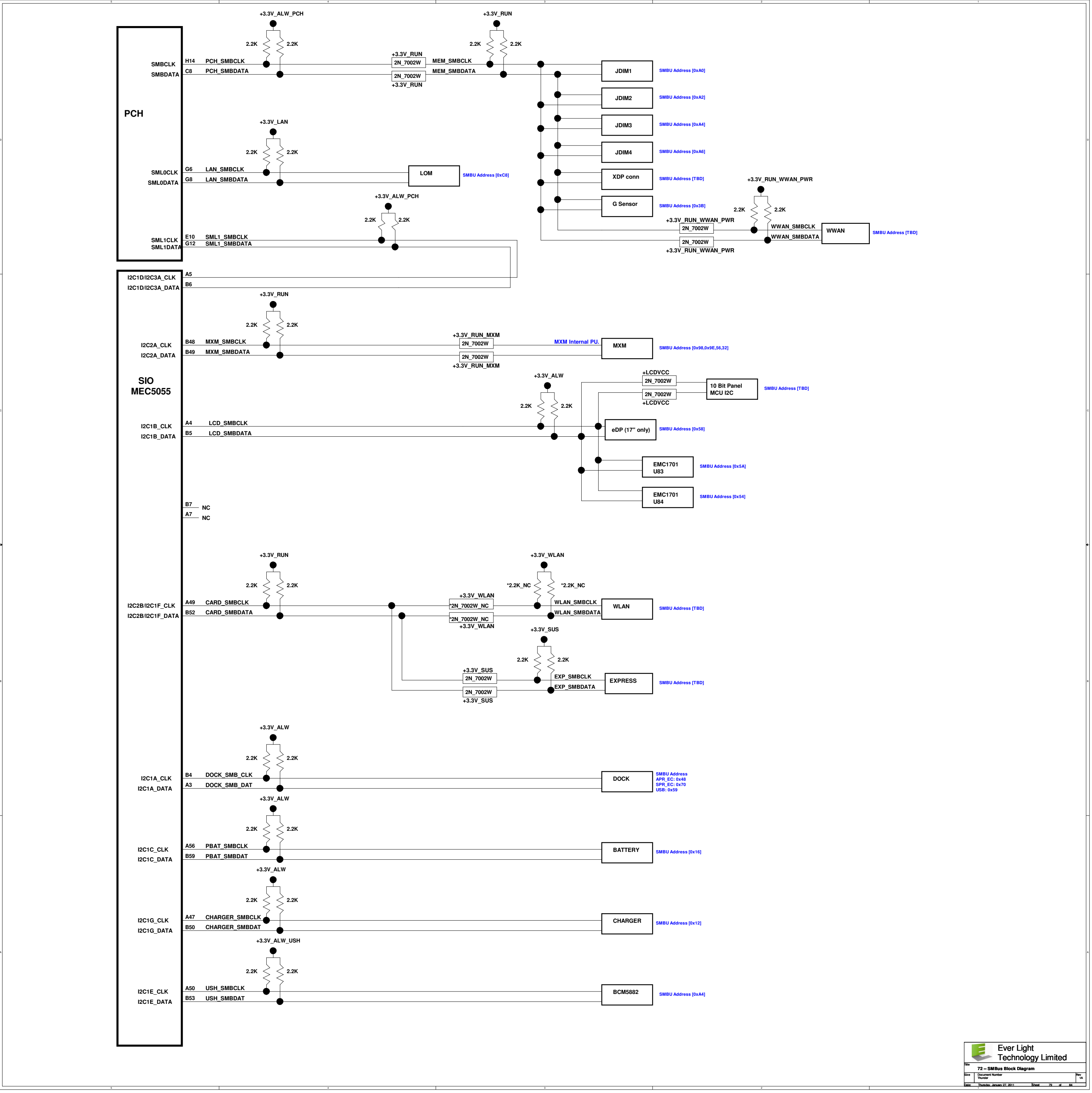

PCH
SMBCLK
SMBDATA
SML0CLK
SML0DATA
SML1CLK
SML1DATA
H14 PCH_SMBCLK
C8 PCH_SMBDATA
G6 LAN_SMBCLK
G8 LAN_SMBDATA
E10 SML1_SMBCLK
G12 SML1_SMBDATA
+3.3V_ALW_PCH
+3.3V_RUN
+3.3V_LAN
2.2K
2N_7002W
MEM_SMBCLK
MEM_SMBDATA
JDIM1
JDIM2
JDIM3
JDIM4
XDP conn
G Sensor
LOM
WWAN
WWAN_SMBCLK
WWAN_SMBDATA
+3.3V_RUN_WWAN_PWR
SMBU Address [0xA0]
SMBU Address [0xA2]
SMBU Address [0xA4]
SMBU Address [0xA6]
SMBU Address [TBD]
SMBU Address [0x3B]
SMBU Address [0xC8]
SIO
MEC5055
A5 I2C1D/I2C3A_CLK
B6 I2C1D/I2C3A_DATA
I2C2A_CLK
I2C2A_DATA
B48 MXM_SMBCLK
B49 MXM_SMBDATA
+3.3V_RUN_MXM
MXM Internal PU.
MXM
SMBU Address [0x98,0x9E,56,32]
I2C1B_CLK
I2C1B_DATA
A4 LCD_SMBCLK
B5 LCD_SMBDATA
+3.3V_ALW
+LCDVCC
10 Bit Panel MCU I2C
eDP (17" only)
SMBU Address [0x58]
EMC1701 U83
SMBU Address [0x5A]
EMC1701 U84
SMBU Address [0x54]
B7 NC
A7 NC
I2C2B/I2C1F_CLK
I2C2B/I2C1F_DATA
A49 CARD_SMBCLK
B52 CARD_SMBDATA
+3.3V_WLAN
*2.2K_NC
*2N_7002W_NC
WLAN_SMBCLK
WLAN_SMBDATA
WLAN
+3.3V_SUS
EXP_SMBCLK
EXP_SMBDATA
EXPRESS
I2C1A_CLK
I2C1A_DATA
B4 DOCK_SMB_CLK
A3 DOCK_SMB_DAT
DOCK
SMBU Address
APR_EC: 0x48
SPR_EC: 0x70
USB: 0x59
I2C1C_CLK
I2C1C_DATA
A56 PBAT_SMBCLK
B59 PBAT_SMBDAT
BATTERY
SMBU Address [0x16]
I2C1G_CLK
I2C1G_DATA
A47 CHARGER_SMBCLK
B50 CHARGER_SMBDAT
CHARGER
SMBU Address [0x12]
+3.3V_ALW_USH
I2C1E_CLK
I2C1E_DATA
A50 USH_SMBCLK
B53 USH_SMBDAT
BCM5882
SMBU Address [0xA4]
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72 -- SMBus Block Diagram

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Title	73 -- Power Sequency Diagram	
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POWER SATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0(Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3(Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to HDD) / M1	LOW	LOW	HIGH	LOW	HIGH	ON	ON	OFF	OFF	OFF
S5 (Soft off) / M1	LOW	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3(Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	ON	ON	OFF	OFF
S4 (Suspend to HDD) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (Soft off) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State \ Power Plane	+15V_ALW +5V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF	OFF	OFF

	USB PORT#	DESTINATION
PCH	0	Right Side top
	1	Right Side bot
	2	Back Side
	3	NC
	4	2nd Mini Card (WLAN/WIMAX)
	5	1st Mini Card (WWAN)
	6	3rd Mini Card
	7	USH
	8	DOCKING
	9	DOCKING
	10	Express Card
	11	BlueTooth
	12	Camera
	13	LCD Touch or Nvidia 3D IR

USH	0	BIO
	1	NC

	PCI EXPRESS	DESTINATION
PCH	Lane 1	1st Mini Card WWAN
	Lane 2	2nd Mini Card WLAN
	Lane 3	Express Card
	Lane 4	USB 3.0
	Lane 5	3rd Mini-Card
	Lane 6	4th Mini-Card
	Lane 7	LAN
	Lane 8	Card Reader

	SATA	DESTINATION
PCH	SATA 0	HDD 1st
	SATA 1	HDD 2nd
	SATA 2	MINI CARD
	SATA 3	ODD
	SATA 4	E-SATA
	SATA 5	Docking

	MXM PORT	CONNECTION
MXM Graphics Module	PORT A	MB DP Port
	PORT B	DOCK DP2
	PORT C	DOCK DP1 and MB HDMI
	PORT D	eDP Panel

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Title	99 -- Media Control	
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