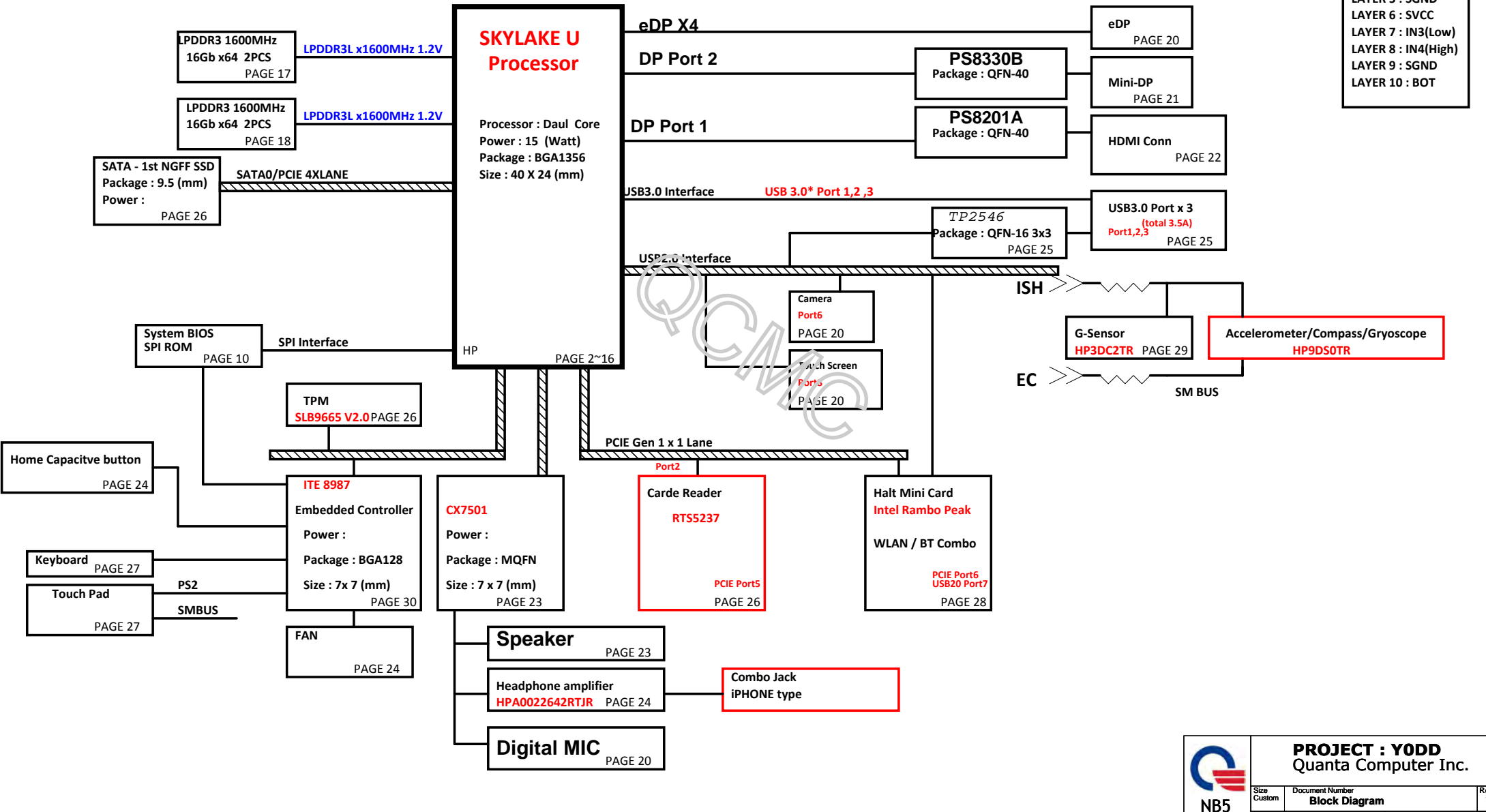


Pike Intel SKYLAKE ULT Platform Block Diagram

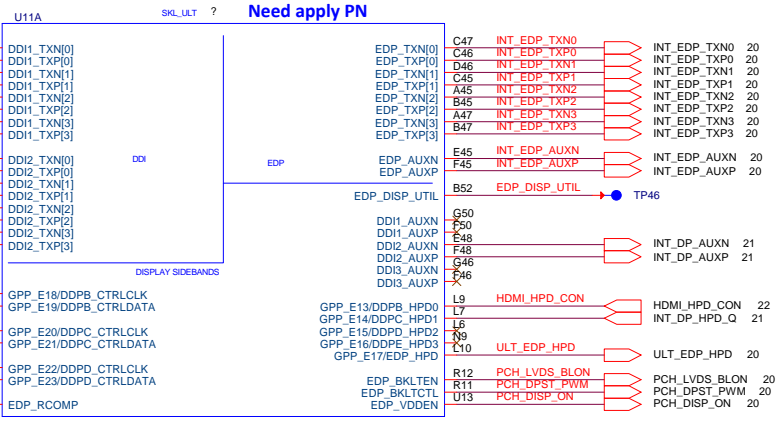
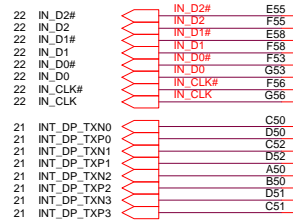
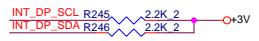
PCB 10L STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1(High)
- LAYER 4 : IN2(High)
- LAYER 5 : SGND
- LAYER 6 : SVCC
- LAYER 7 : IN3(Low)
- LAYER 8 : IN4(High)
- LAYER 9 : SGND
- LAYER 10 : BOT

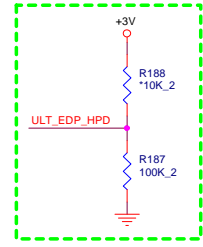


+3V 4,10,11,12,13,14,15,20,22,23,26,27,29,30,31,37,38
 +1.0V 4,6,30,36
 +VCCSTPLL 5,6,9,36,38
 +VCCIO 6,16,36

HDMI

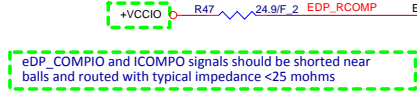
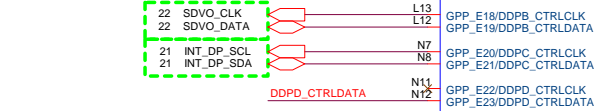
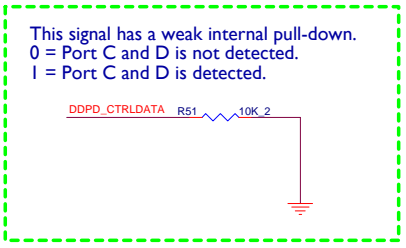


Reserve EDP_HPD opposites circuit!



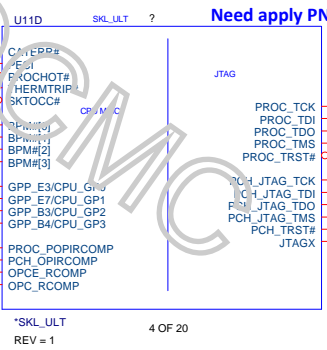
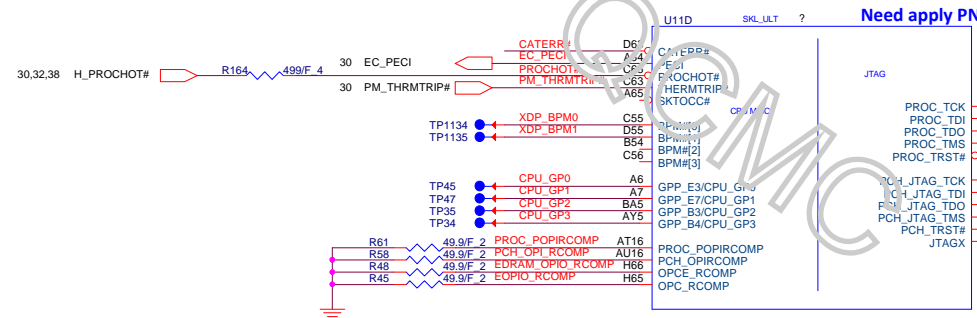
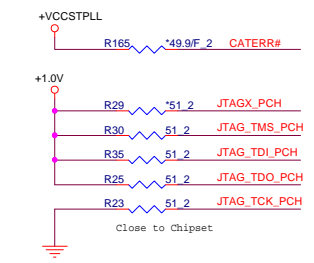
Mini-DP

DDPB_CTRLDATA/ GPP_E19
 Display Port B Detected
 This signal has a weak internal pull-down.
 0 = Port B is not detected.
 1 = Port B is detected.

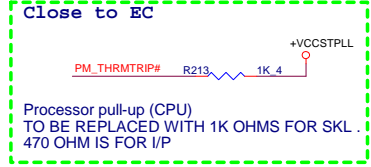


eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

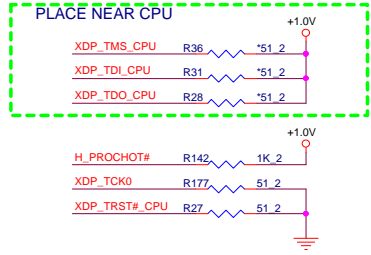
*SKL_ULT
 REV = 1 1 OF 20 ?



*SKL_ULT
 REV = 1 4 OF 20



Processor pull-up (CPU)
 TO BE REPLACED WITH 1K OHMS FOR SKL
 470 OHM IS FOR I/P



PLACE NEAR CPU

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	Quanta Computer Inc.		
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SkyLake ULT Processor (DDR3L)

Need apply PN



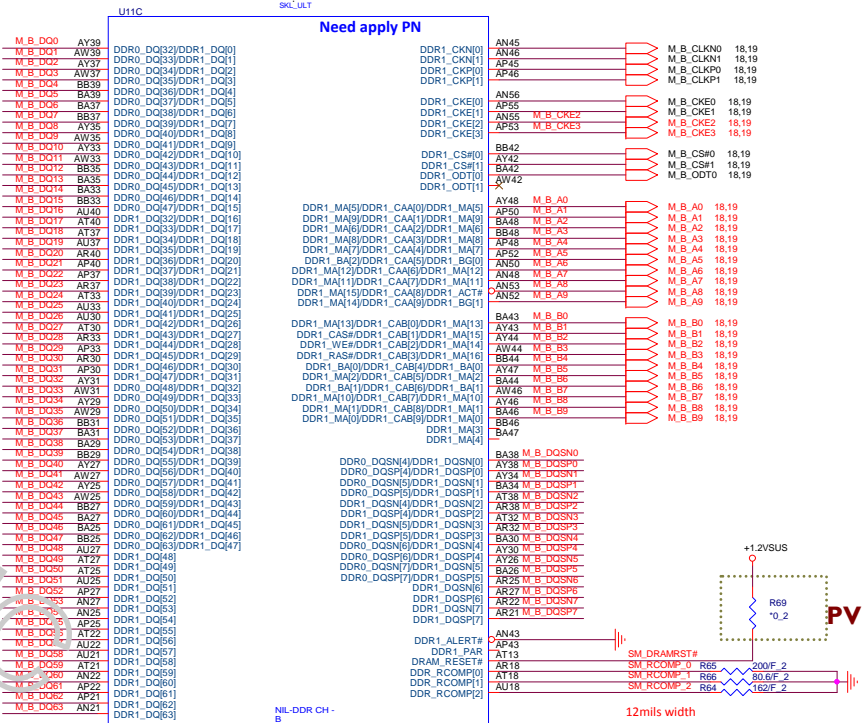
SKL_ULT REV = 1 2 OF 20

NIL-DDR CH - A

20mils width

Place near CPU

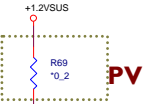
Need apply PN



SKL_ULT REV = 1 3 OF 20

NIL-DDR CH - B

12mils width



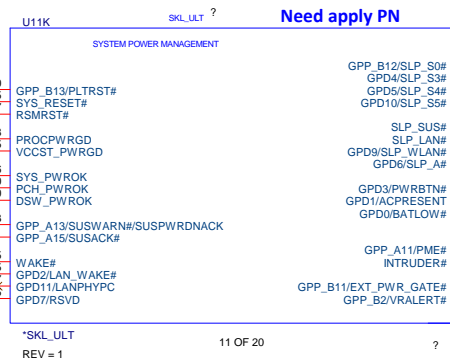
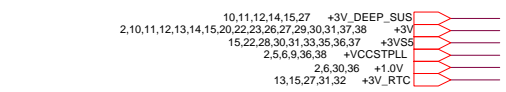
12mils width

PROJECT : YODD
Quanta Computer Inc.

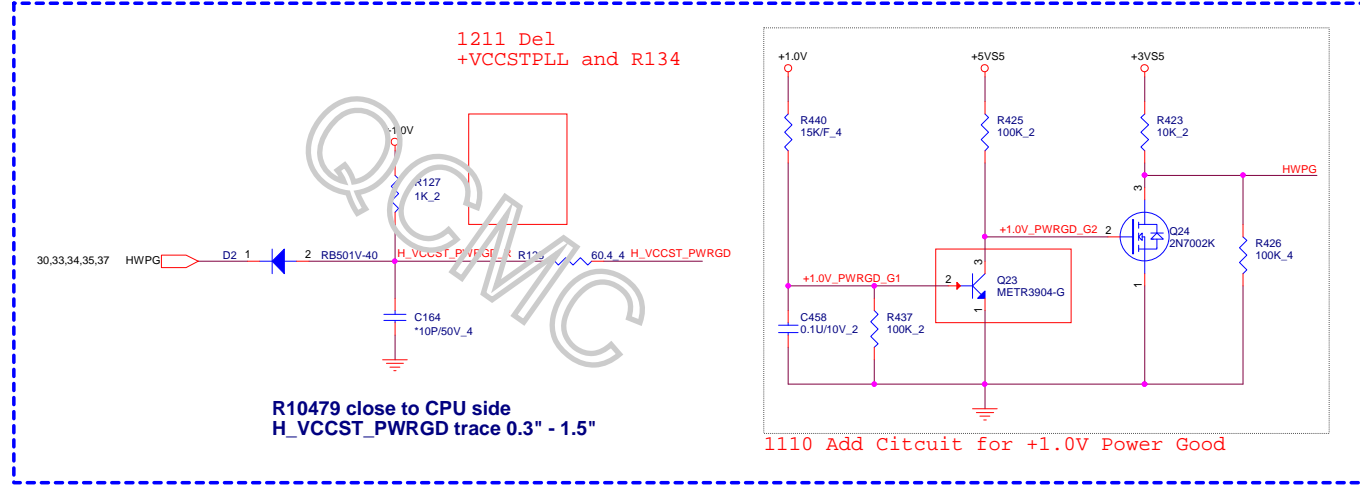
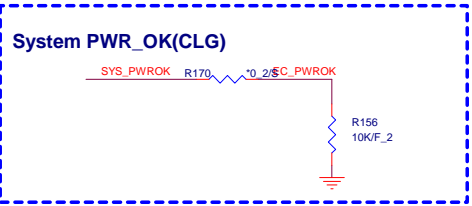
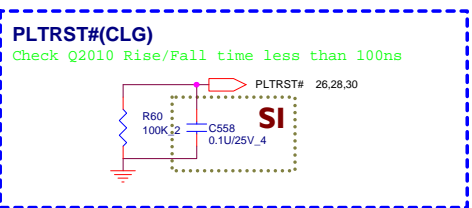
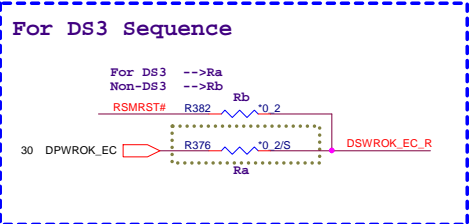
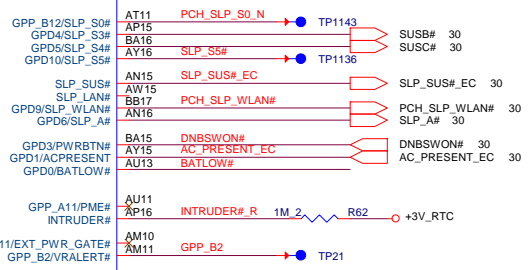
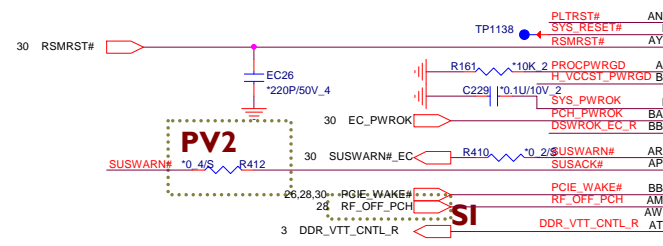
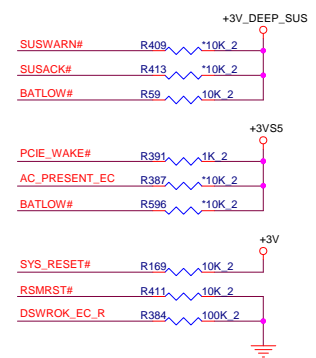
Rev 1A

Document Number: SKL U (2/14)

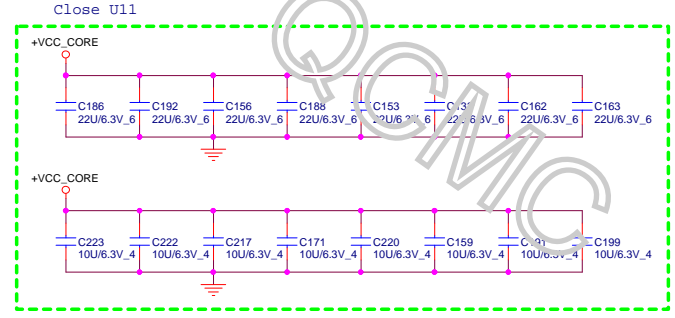
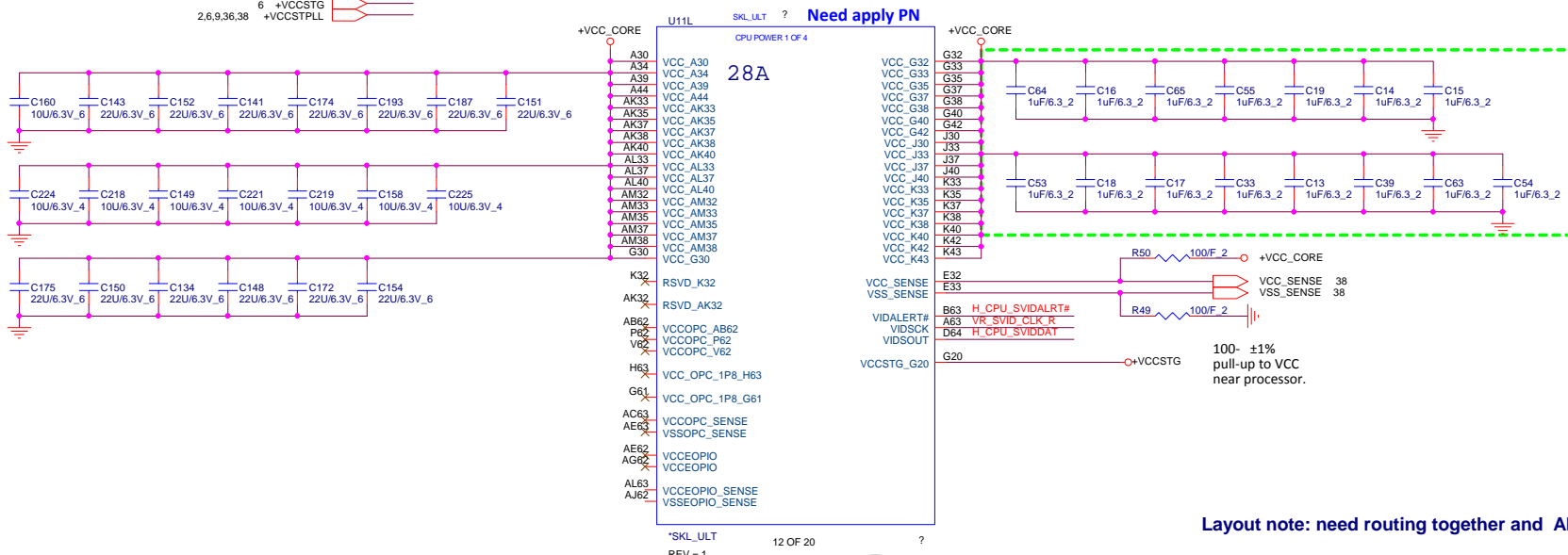
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PCH Pull-high/low(CLG)

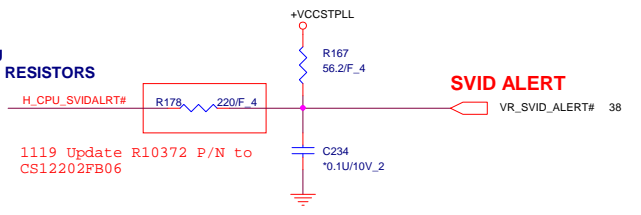


39 +VCC_CORE
2,4,6,30,36 +1.0V
8 +VCCSTG
2,6,9,36,38 +VCCSTPLL



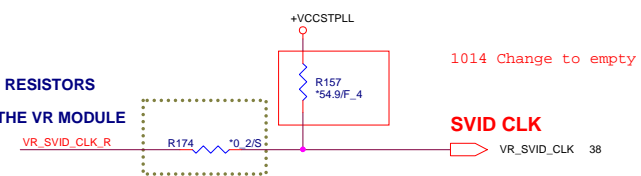
Layout note: need routing together and ALERT need between CLK and DATA.

CLOSE TO CPU
PLACE THE PU RESISTORS

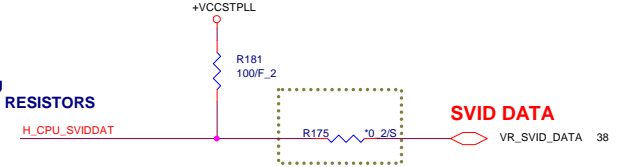


1119 Update R10372 P/N to CS12202FB06

PLACE THE PU RESISTORS
CLOSE TO VR
PULL UP IS IN THE VR MODULE



CLOSE TO CPU
PLACE THE PU RESISTORS

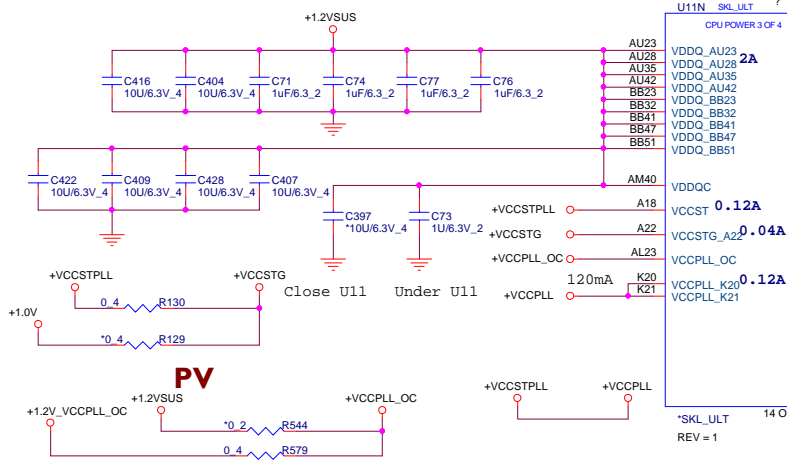


Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CCGT}	Processor Graphics Power Rails	SVID
V _{CCGTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V _{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CCIO}	IO Power Rail	Fixed
V _{CCST}	Sustain Power Rail	Fixed
V _{CCPLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCEOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

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- +VCCSTPLL 2.5,9,36,38
- +VCCSA 38,39
- +1.2VSUS 3,17,18,34,36
- +1.0V_DEEP_SUS 9,13,15,35,36
- +1.0V 2,4,30,36
- +3VPCU 13,15,27,28,30,31,32,33
- +1.2V_VCCPLL_OC 36

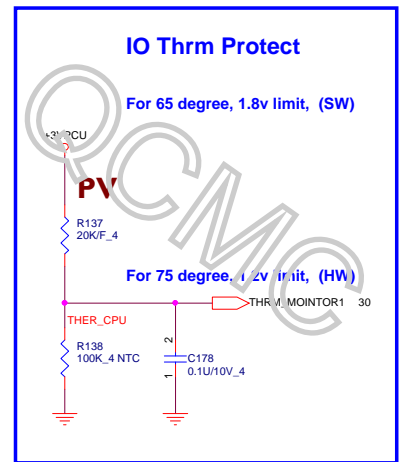
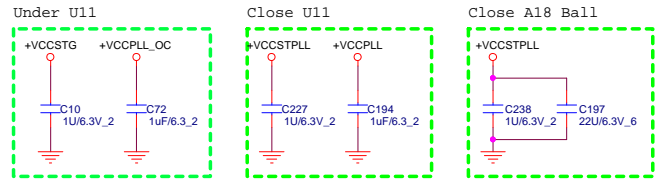
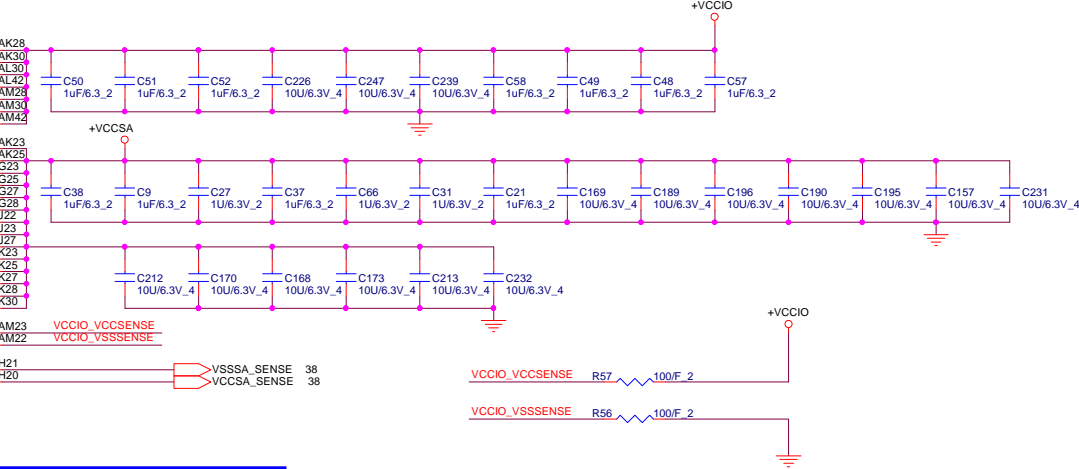


Need apply PN

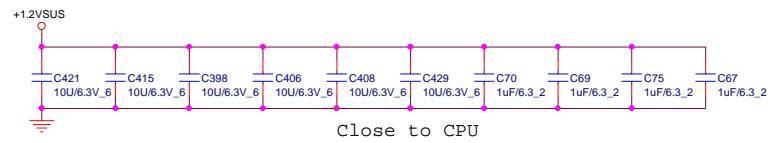
U11N SKL_U1T ?
CPU POWER 3 OF 4

3.1A	VCCIO	AK28
	VCCIO	AK30
	VCCIO	AL30
	VCCIO	AL42
	VCCIO	AM28
	VCCIO	AM30
	VCCIO	AM42
5A	VCCSA	AK23
	VCCSA	AK25
	VCCSA	G23
	VCCSA	G25
	VCCSA	G27
	VCCSA	G28
	VCCSA	J22
	VCCSA	J27
	VCCSA	K23
	VCCSA	K25
	VCCSA	K28
	VCCSA	K30
	VCCIO_SENSE	AM23
	VSSIO_SENSE	AM22
	VSSSA_SENSE	H21
	VCCSA_SENSE	H20

*SKL_U1T 14 OF 20
REV = 1



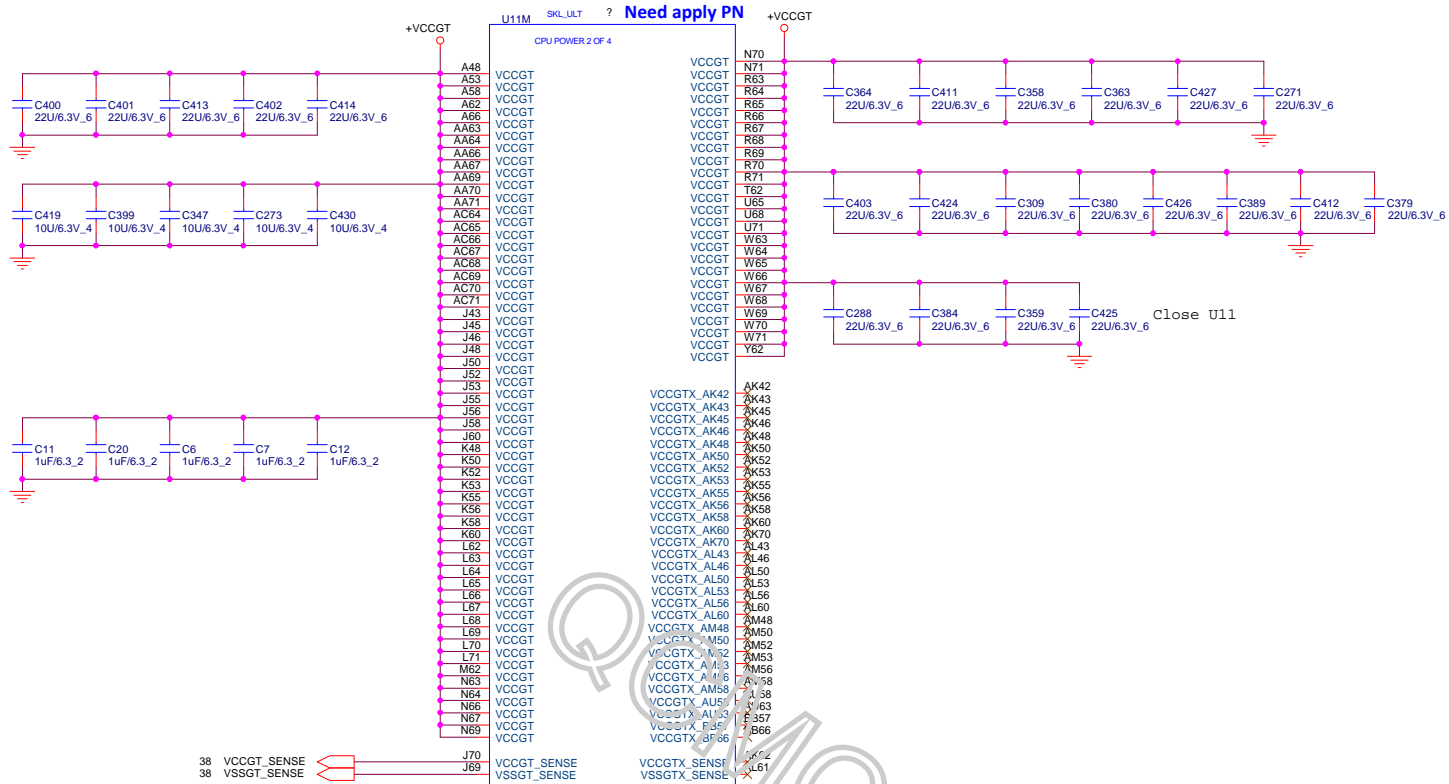
Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CCGT}	Processor Graphics Power Rails	SVID
V _{CCGTx}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V _{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CCIO}	IO Power Rail	Fixed
V _{CCST}	Sustain Power Rail	Fixed
V _{CCPLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCeOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed



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+VCCGT 38,40

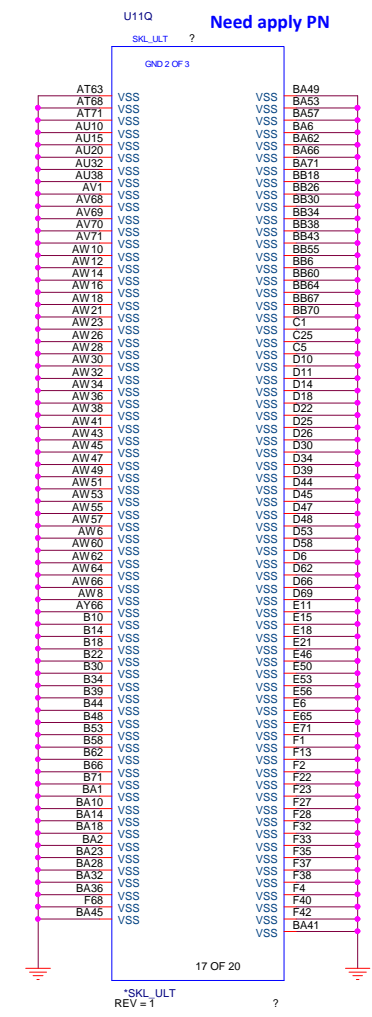
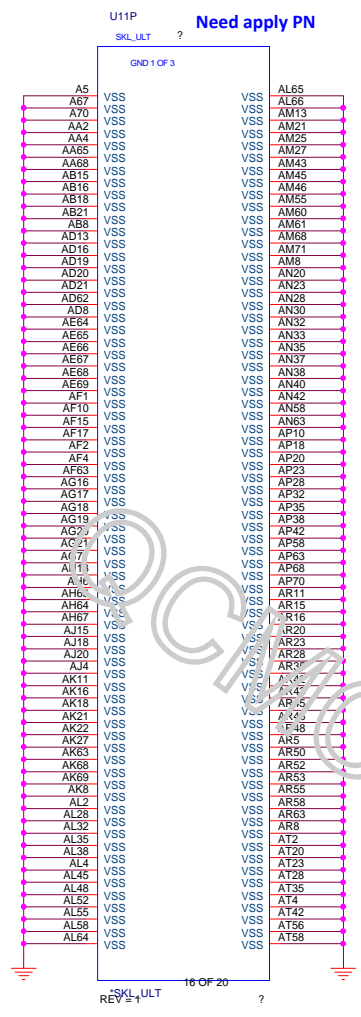
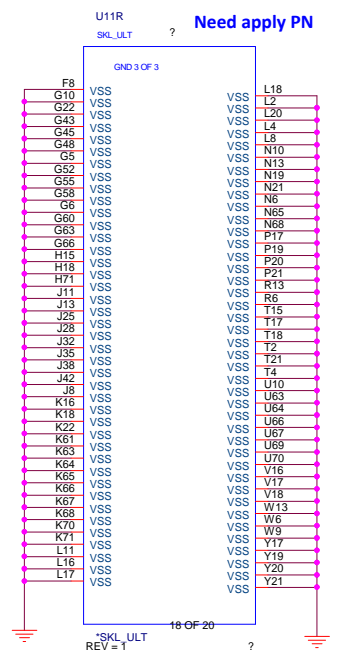


*SKL_ULT 13 OF 20
REV = 1

Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CCGT}	Processor Graphics Power Rails	SVID
V _{CCGTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V _{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CCIO}	IO Power Rail	Fixed
V _{CCST}	Sustain Power Rail	Fixed
V _{CCPLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCEOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

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Quanta Computer Inc.

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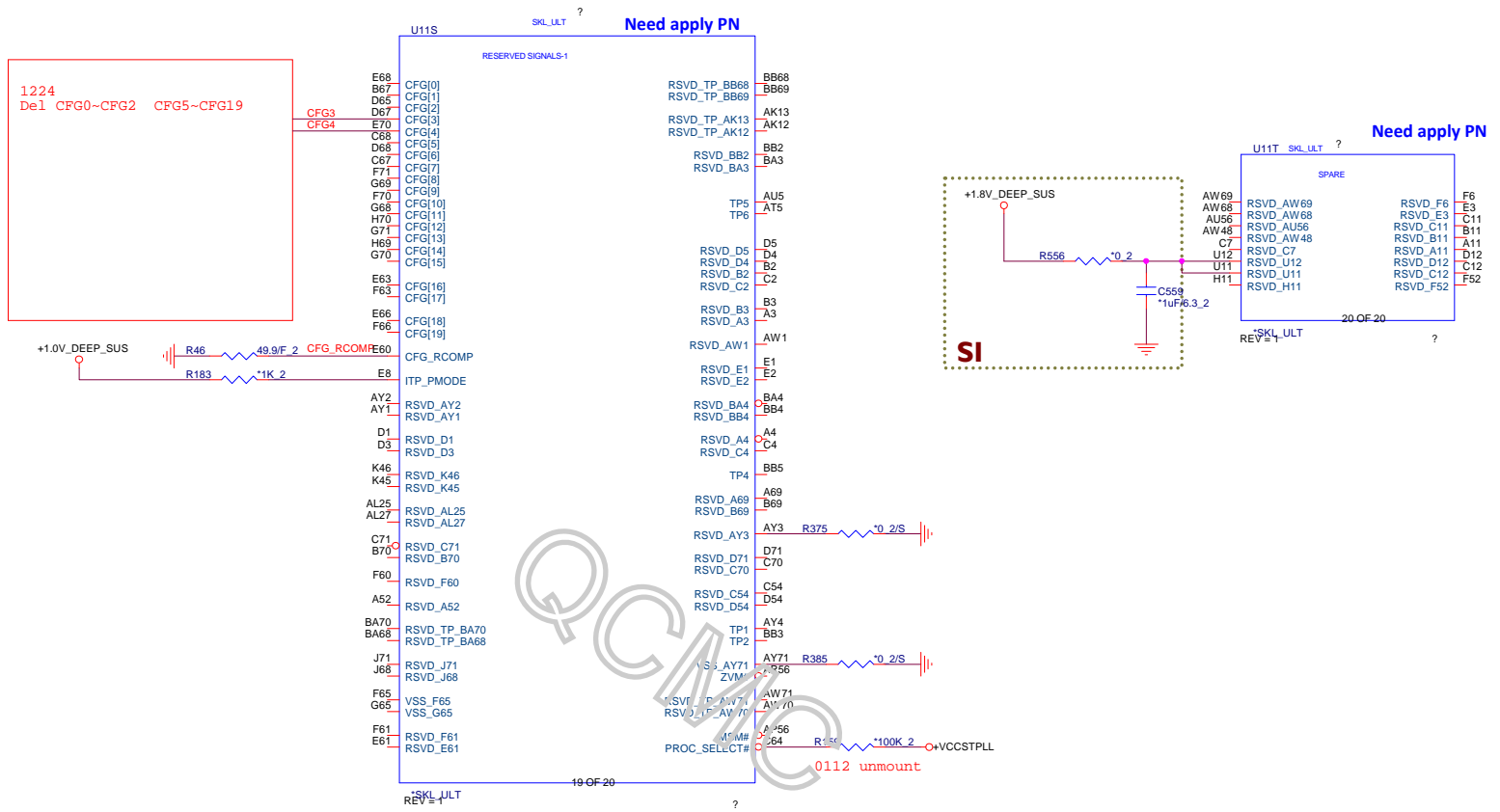


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NBS



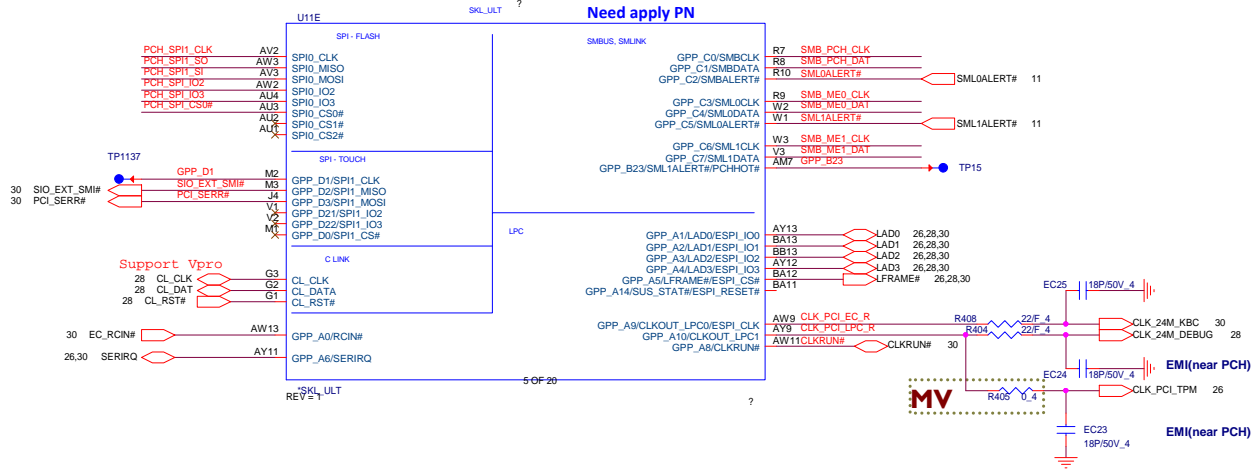
Processor Strapping The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physical Debug Enable) DFX Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	

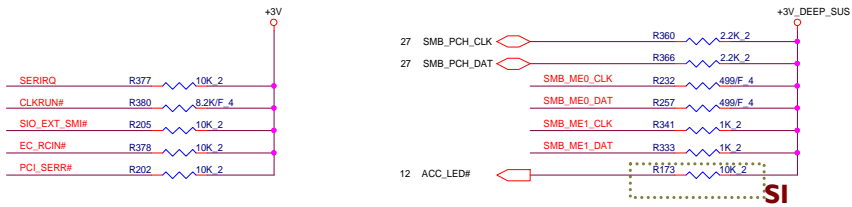
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- +3V_DEEP_SUS 4,11,12,14,15,27
- +3V 2,4,11,12,13,14,15,20,22,23,26,27,29,30,31,37,38
- +5V 22,23,24,27,37
- +1.0V 2,4,6,30,36
- +3VSS 4,15,22,28,30,31,33,35,36,37



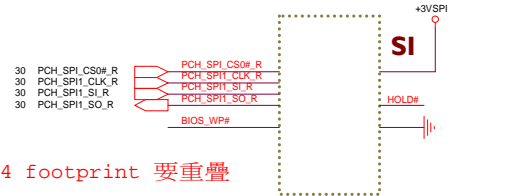
GPIO Pull UP



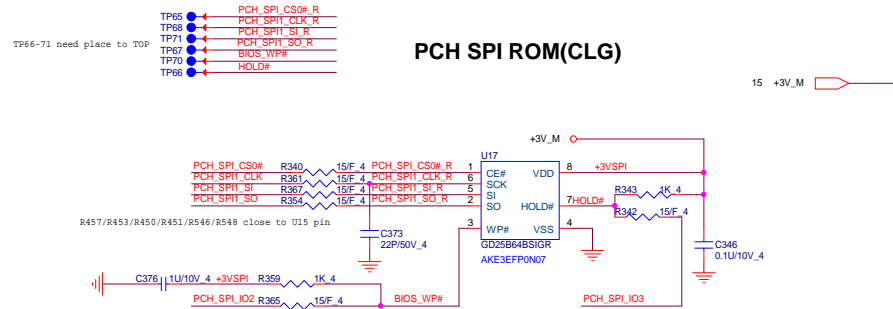
PCH SPI ROM(CLG)

Vendor	Size	P/N
EON	8MB	AKE3EZN0Q1 (EN25QH64-104HIP)
Winbond	8MB	AKE3EFPN07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q1 (GD25B64BSIGR)
Socket		DFN1008FS023

4M SPI ROM Socket



PCH SPI ROM(CLG)



SMBus/Pull-up(CLG)

1230
Change net name from SMB_RUN_CLK to SMB_PCH_CLK
Change net name from SMB_RUN_DAT to SMB_PCH_DAT

Touch Pad
XDP

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Functional Strap Definitions

DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET

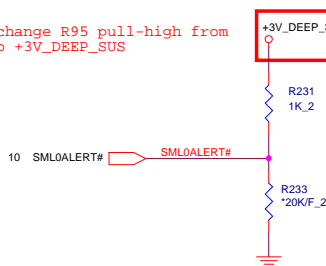


TOP SWAP OVERRIDE
HIGH - TOP SWAP ENABLE
LOW-DISABLED
HIGH: LPC SELECTED FOR SYSTEM FLASH
WEAK INTERNAL PD

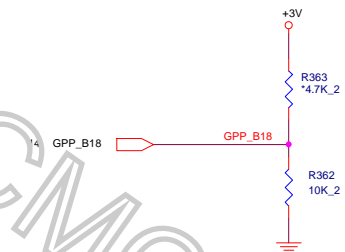


No Boot:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.

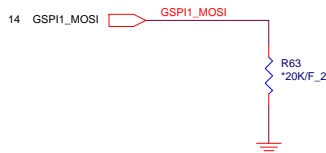
1212 change R95 pull-high from +3V to +3V_DEEP_SUS



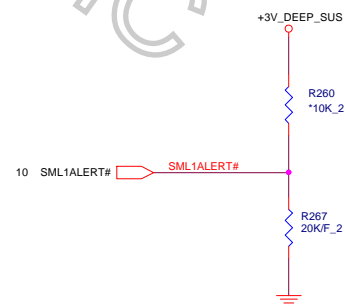
No Boot:
The signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.



No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

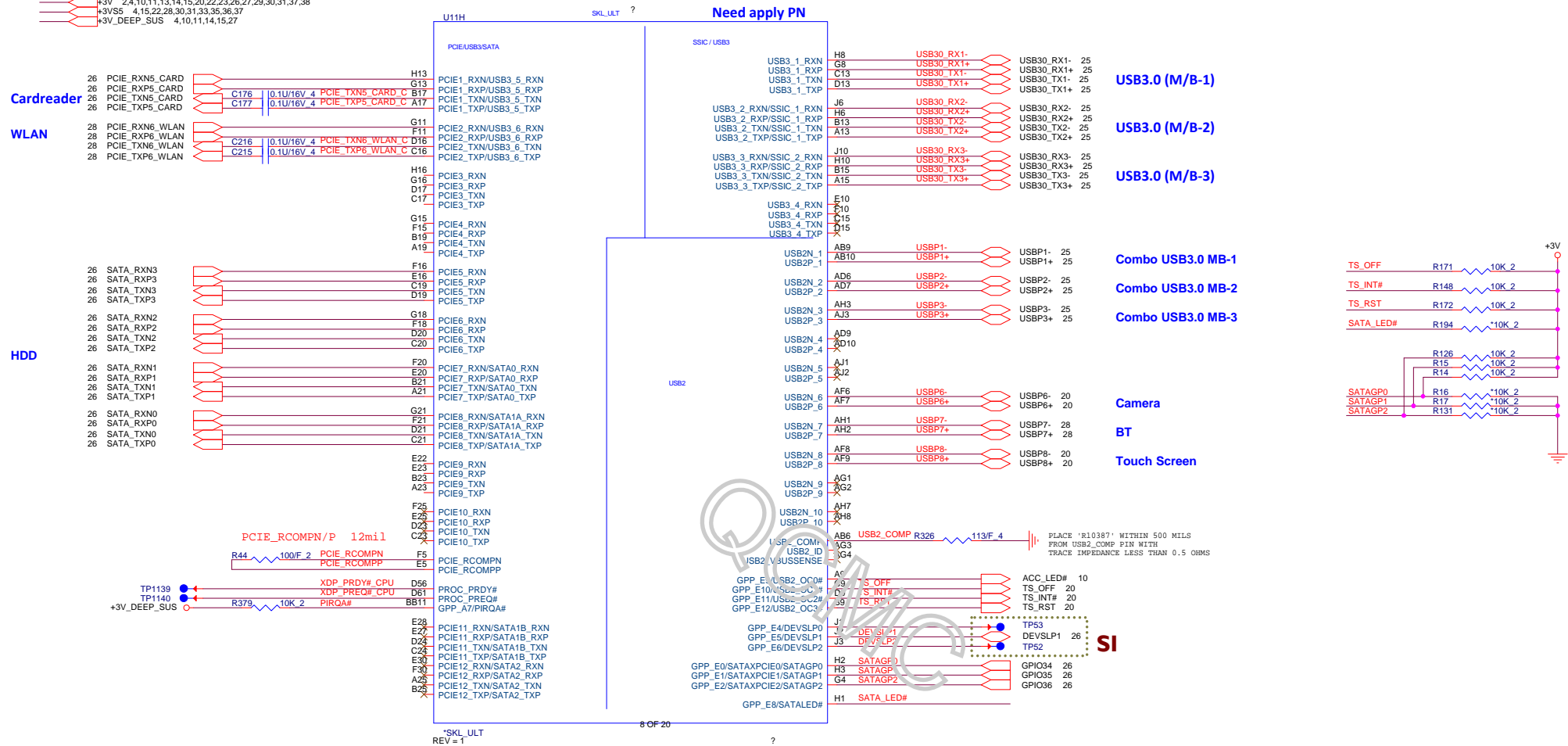


No Boot:
The signal has a weak internal pull-down.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.
Bit 10 Boot BIOS Destination
0 SPI
1 LPC



No Boot:
The signal has a weak internal pull-down.
0 = LPC is selected for EC.
1 = eSPI is selected for EC.

+3V 2,4,10,11,13,14,15,20,22,23,26,27,29,30,31,37,38
 +3VS5 4,15,22,28,30,31,33,35,36,37
 +3V_DEEP_SUS 4,10,11,14,15,27



PCI-E Port Mapping Table

PCI-E Port	Function	CLK RQ Port	Function
Port1	CardReader	Port0	Un-used
Port2	WLAN	Port1	CardReader
Port3	Un-used	Port2	WLAN
Port4	Un-used	Port3	Un-used
Port5	SSD	Port4	Un-used
Port6	SSD	Port5	SSD
Port7	SSD		
Port8	SSD		
Port9	Un-used		
Port10	Un-used		

USB3.0 Port Mapping Table

USB3.0	Function
PORT-1	USB3.0 MB-1
PORT-2	USB3.0 MB-2
PORT-3	USB3.0 MB-3
PORT-4	NC

USB2.0 Port Mapping Table

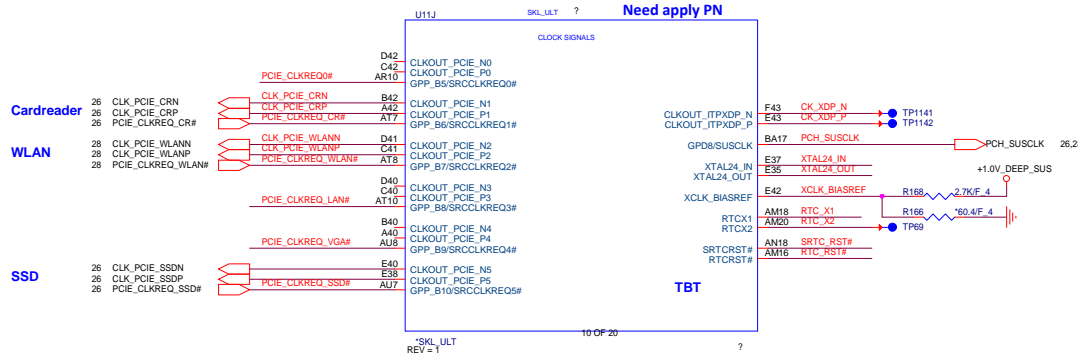
USB2.0	Function
PORT-1	USB3.0 MB-1
PORT-2	USB3.0 MB-2
PORT-3	USB3.0 MB-3
PORT-4	Sensor Hub
PORT-5	NC
PORT-6	Camera
PORT-7	WLAN
PORT-8	Touch Screen
PORT-9	NC
PORT-10	NC

PROJECT : YODD
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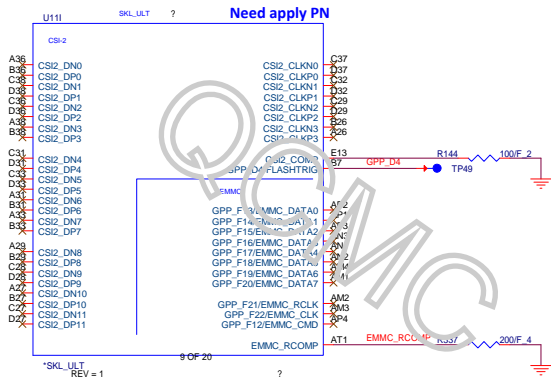
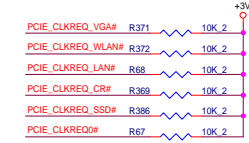
Size Custom Document Number **SKL U (11/14)** Rev 1A

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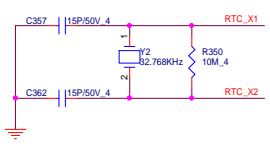
+1.0V_DEEP_SUS 9,15,36,37
 +3V 2,4,10,11,12,14,15,20,22,23,26,27,29,30,31,37,38



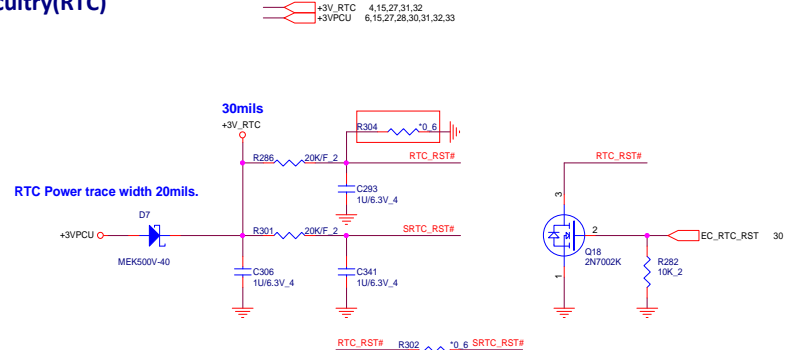
CLK_REQ/Strap Pin(CLG)



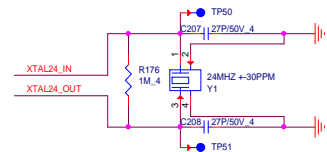
RTC Clock 32.768KHz



RTC Circuitry(RTC)



External Crystal



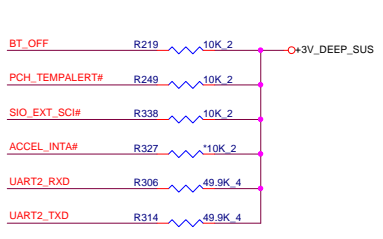
PROJECT : Y0DD
Quanta Computer Inc.

NB5

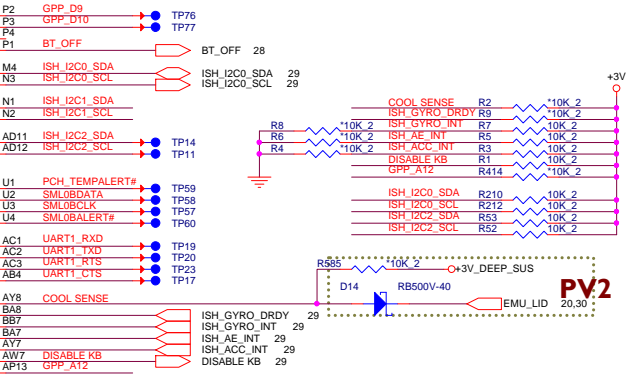
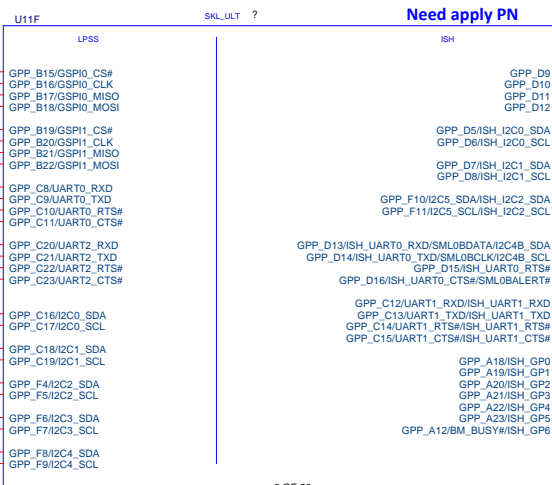
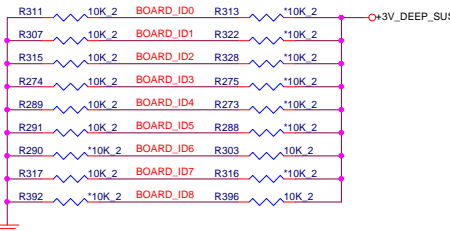
Size Custom	Document Number SKL U (12/14)	Rev 1A
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Skylake (GPIO)

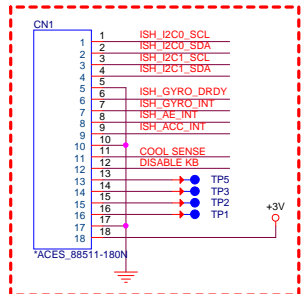
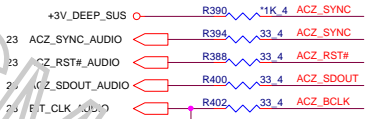
+3V 2,4,10,11,12,13,15,20,22,23,26,27,29,30,31,37,38
+3V_DEEP_SUS 4,10,11,12,15,27



1227 Add R306 and R314 for UART2 function reserved

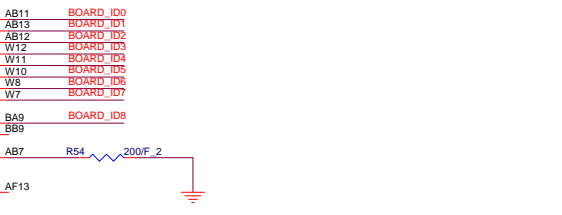
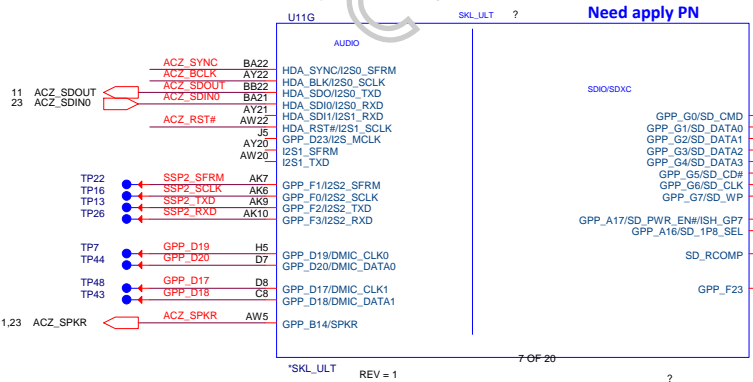


HDA Bus(CLG)



1207 Add Sensors Debug CONN
1209 Change CN5012 footprint from 88511-180n-18p-1 to fg-12x59-20-18p

Table with columns: Model, BOARD_ID8, BOARD_ID7, BOARD_ID6, Board ID [5], BOARD_ID[4:0]. Lists various memory and storage configurations for different models.

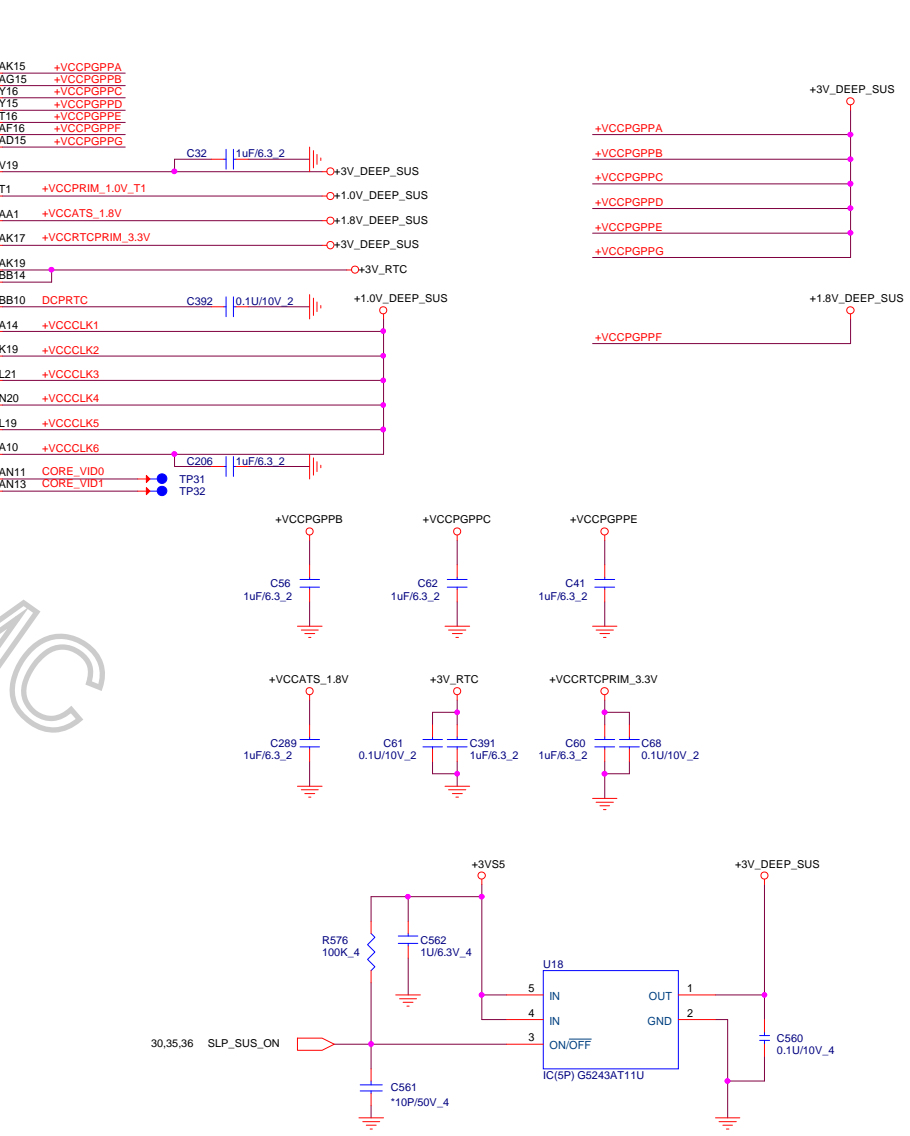
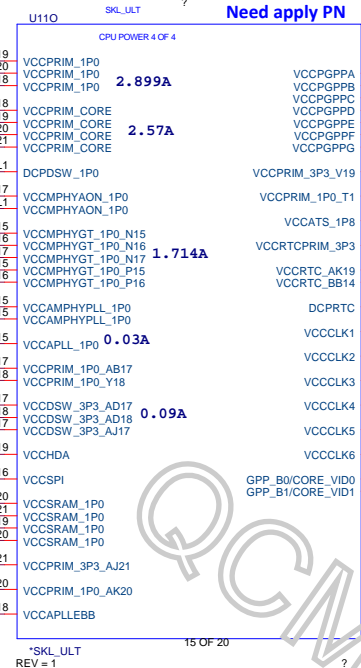
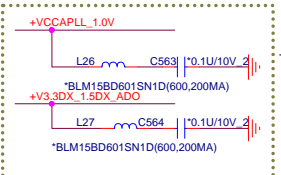


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NB5
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- 4,10,11,12,14,27 +3V_DEEP_SUS
- 9,13,35,36 +1.0V_DEEP_SUS
- 9,35,37 +1.8V_DEEP_SUS
- 4,13,27,31,32 +3V_RTC
- 4,22,28,30,31,33,35,36,37 +3VS5
- 10 +3V_M

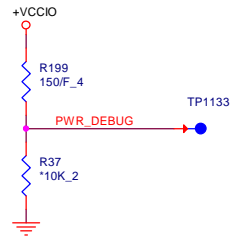
PCH Internal VRM
 C820 and C690 close to cpu less than 100 mils

PV



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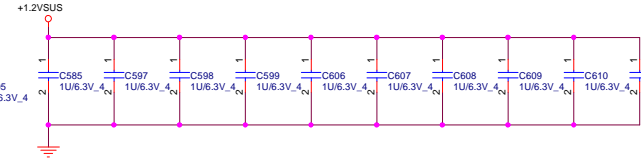
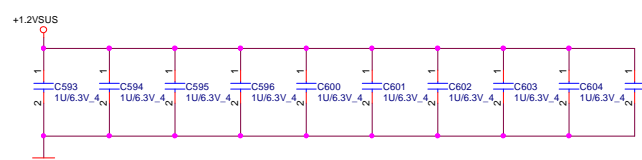
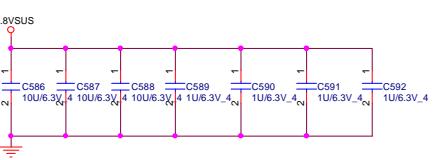
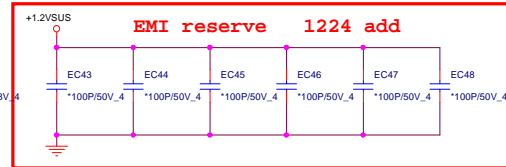
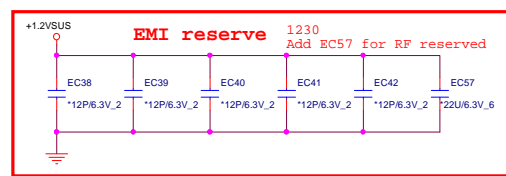
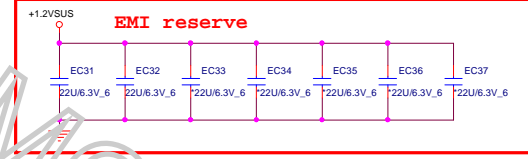
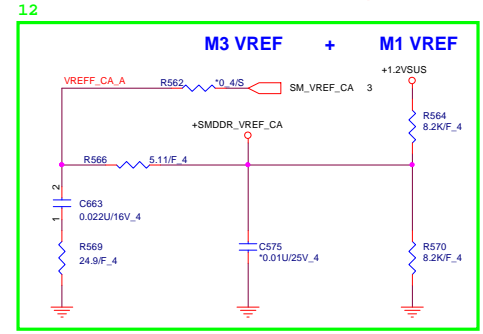
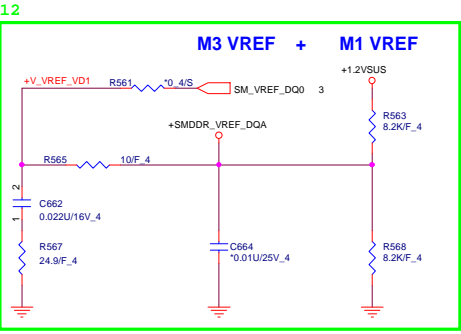
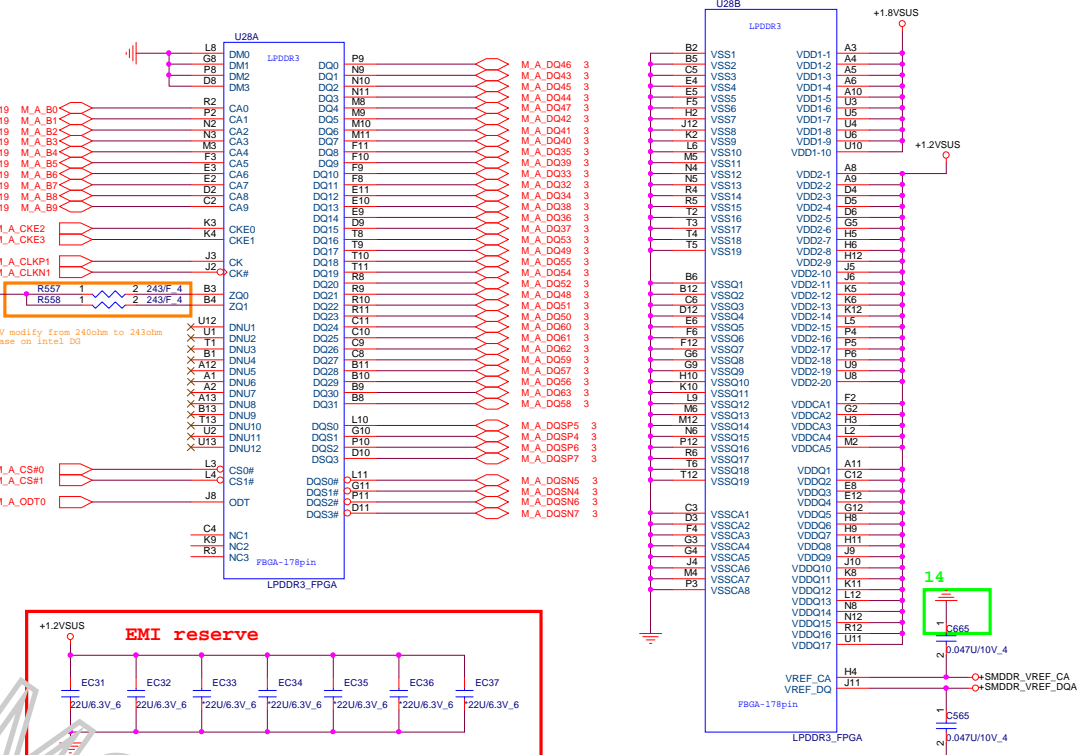
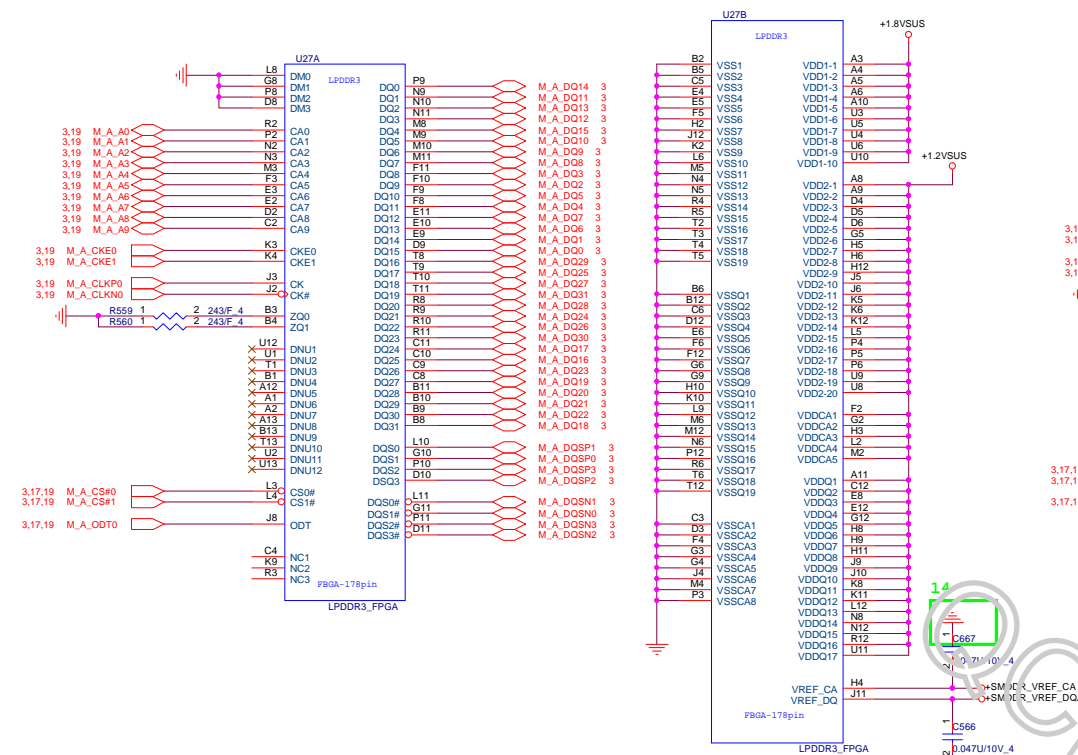
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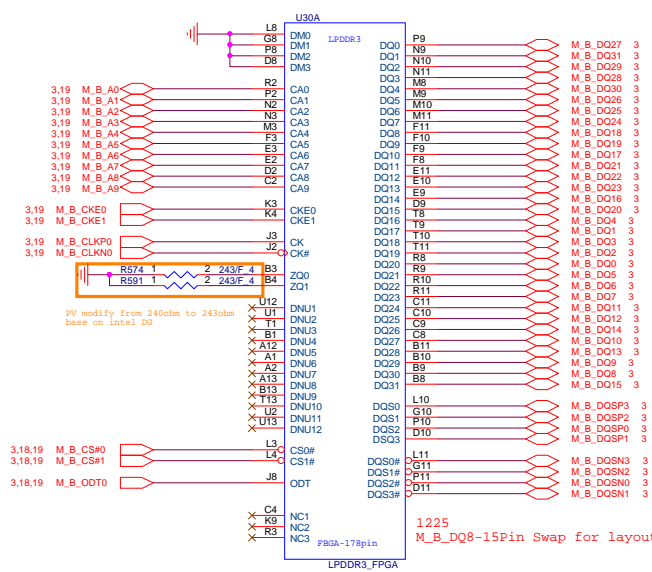
QCMC

bit:0-31

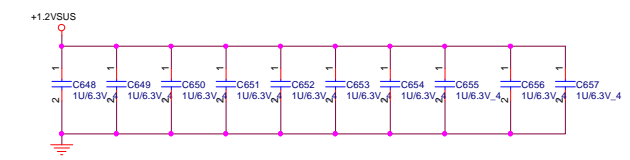
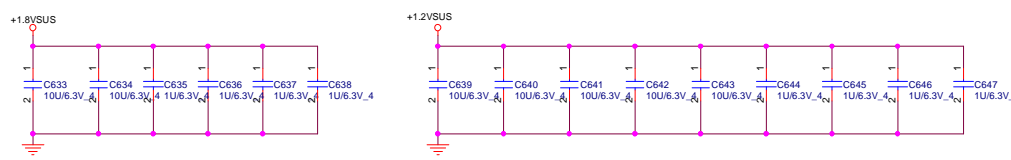
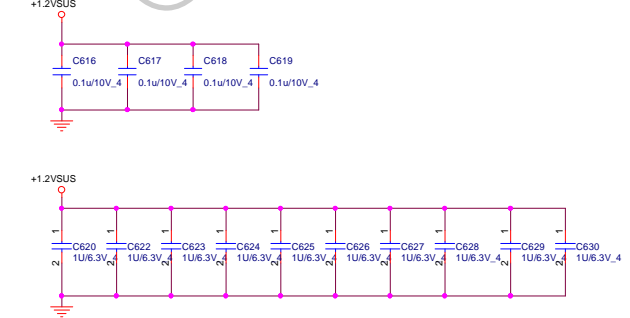
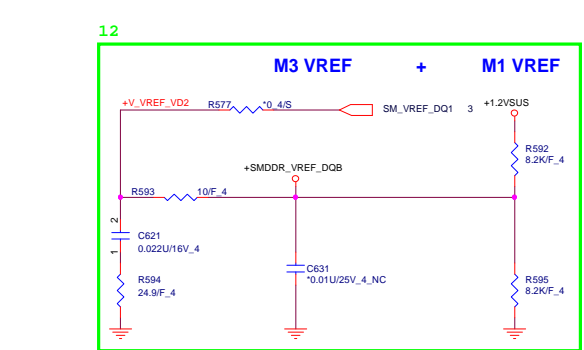
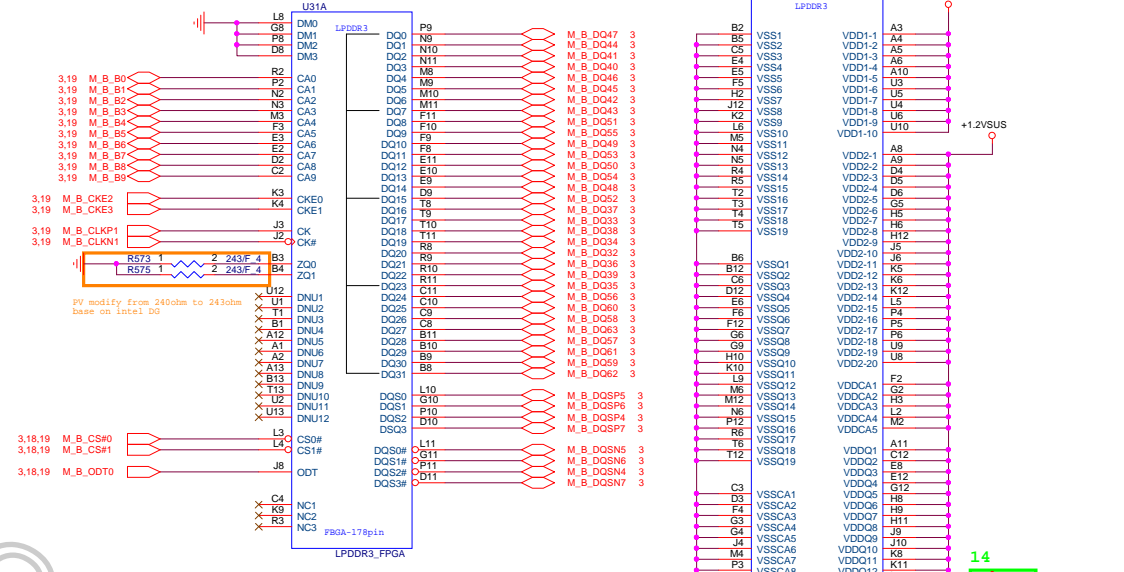
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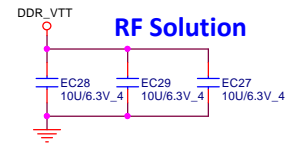
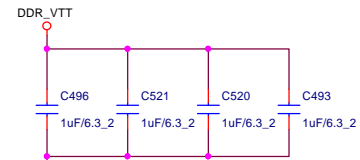
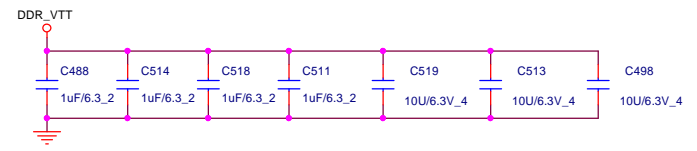
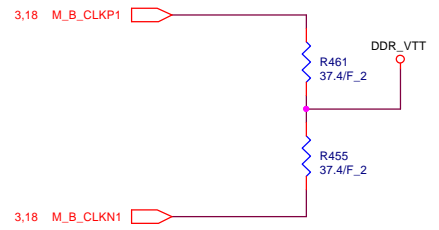
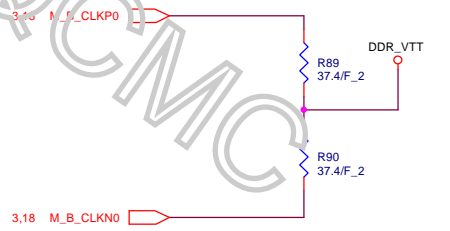
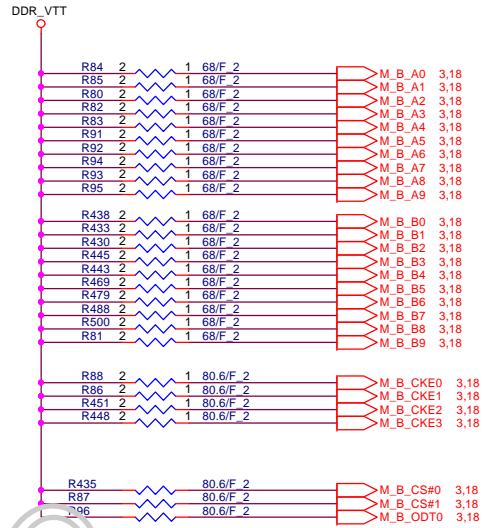
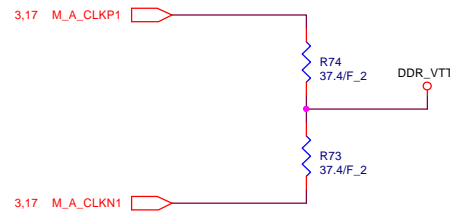
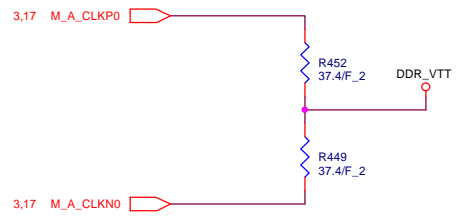
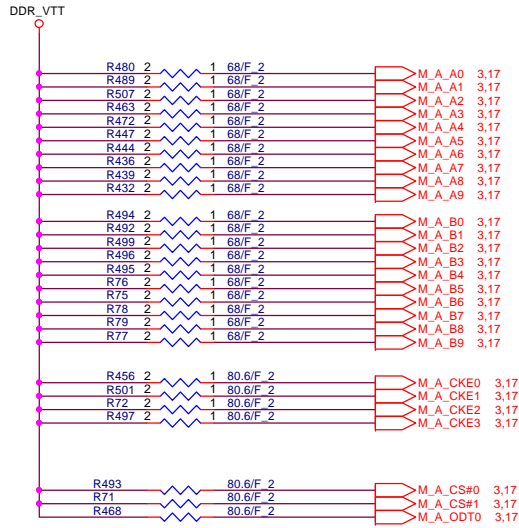


bit-0-31



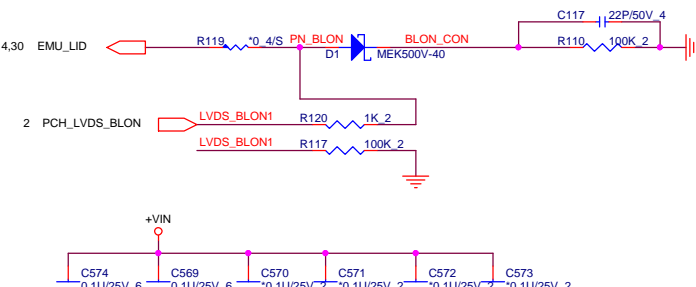
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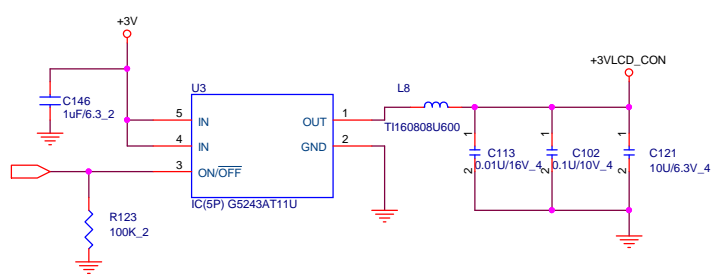
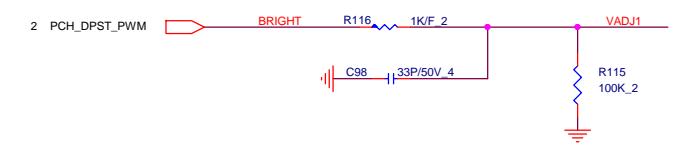
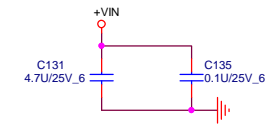
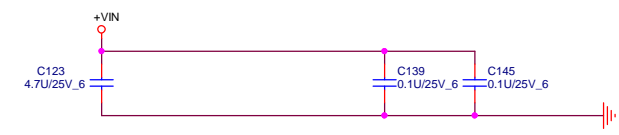
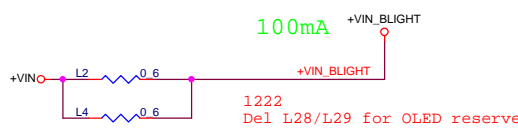
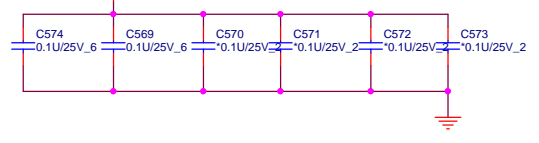
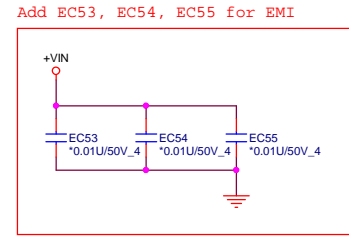


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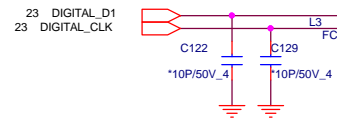
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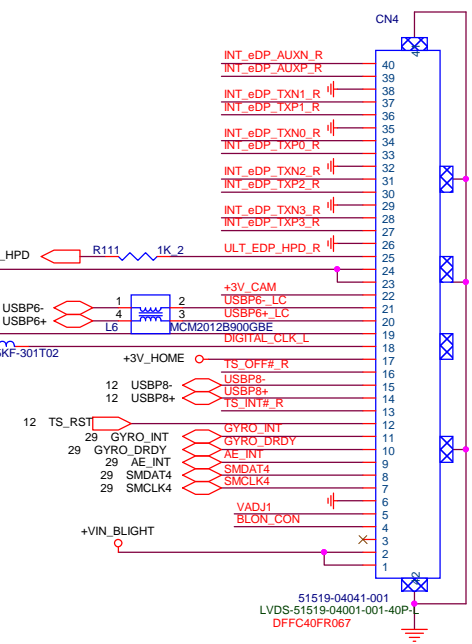
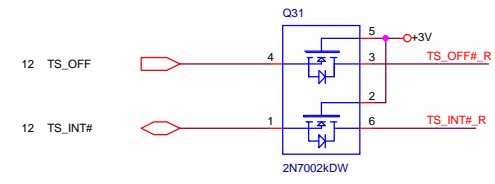
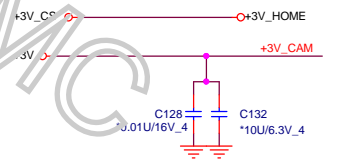
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2	INT_eDP_TXP2	C124	0.1U/10V_4	INT_eDP_TXP2_R
2	INT_eDP_TXN2	C125	0.1U/10V_4	INT_eDP_TXN2_R
2	INT_eDP_TXP1	C110	0.1U/10V_4	INT_eDP_TXP1_R
2	INT_eDP_TXN1	C111	0.1U/10V_4	INT_eDP_TXN1_R
2	INT_eDP_TXP0	C108	0.1U/10V_4	INT_eDP_TXP0_R
2	INT_eDP_TXN0	C109	0.1U/10V_4	INT_eDP_TXN0_R
2	INT_eDP_AUXP	C103	0.1U/10V_4	INT_eDP_AUXP_R
2	INT_eDP_AUXN	C104	0.1U/10V_4	INT_eDP_AUXN_R



1225 L6 Pin Swap for layout



1222 Del C112/C101 for EMI reserve



51519-04041-001
LVDS-51519-04001-001-40P-L
DFFC40FR067

SI modify R74 non-stuff

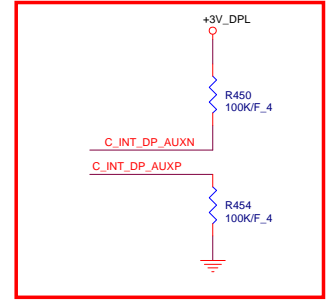
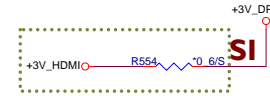
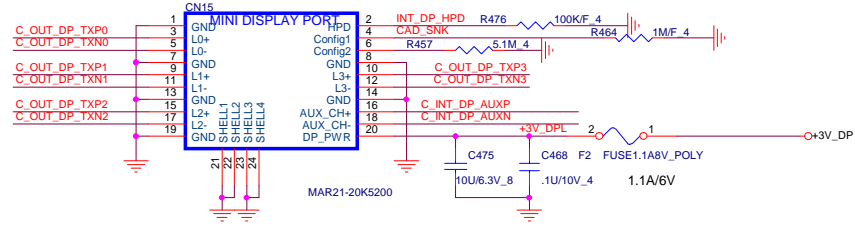
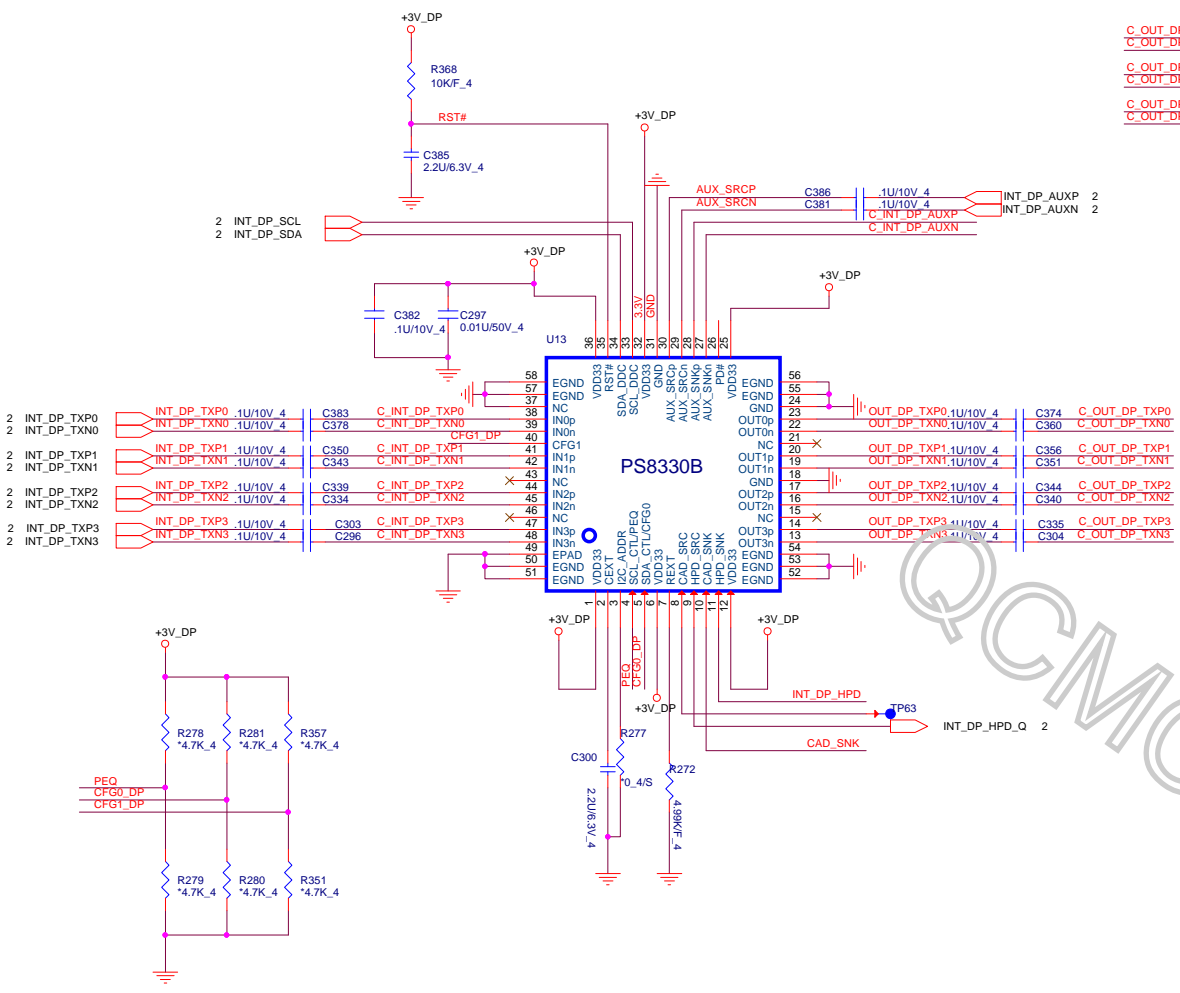
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6,13,15,27,28,30,31,32,33	+3VPCU
22,23,24,27,37	+5V
27,32,33,34,35,38,39,40	+VIN

PROJECT : YODD
Quanta Computer Inc.

Size Custom	Document Number LCD CONN/CAM/LID	Rev 1A
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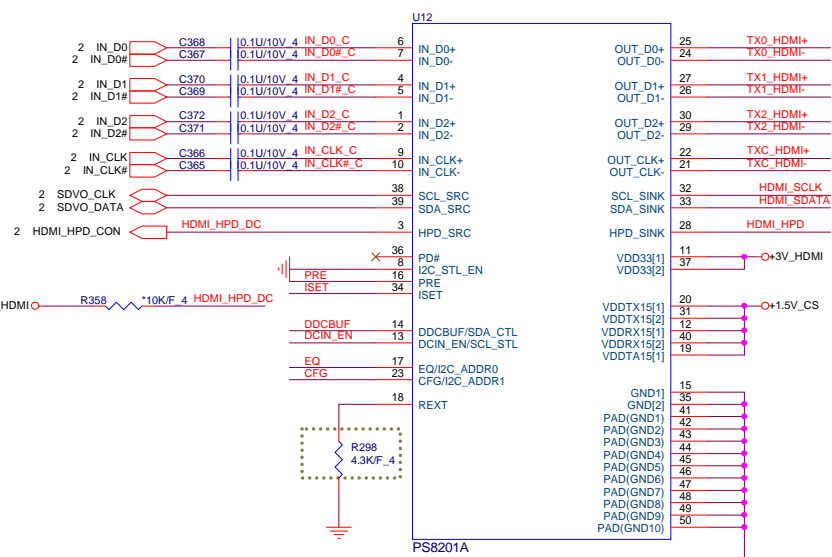
Mini Display

+5V 22,23,24,27,37
 +3V 2,4,10,11,12,13,14,15,20,22,23,26,27,29,30,31,37,38

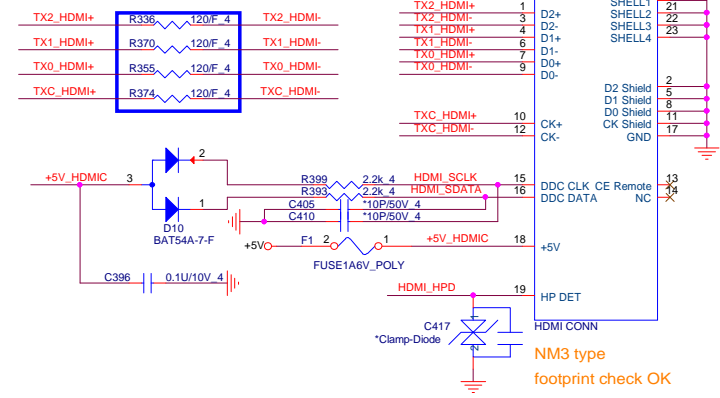


for intel recommend

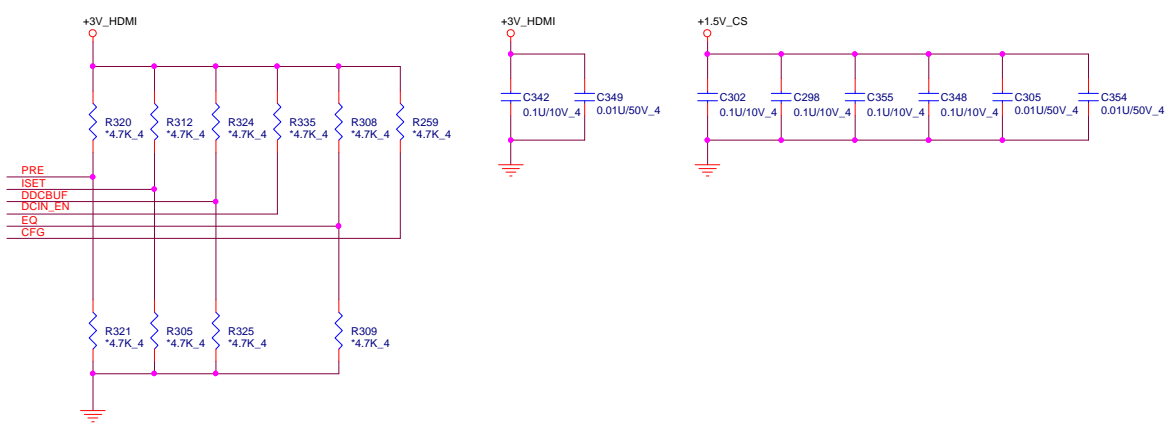
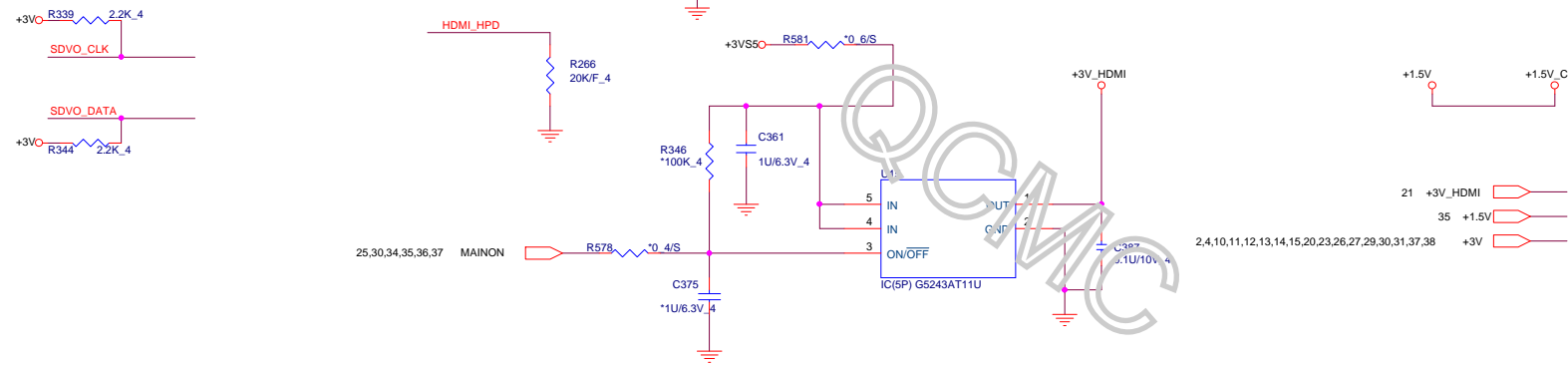
	PROJECT : YODD		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number Re-driver RS8330B	
Date: Wednesday, January 06, 2016 Sheet 21 of 41			



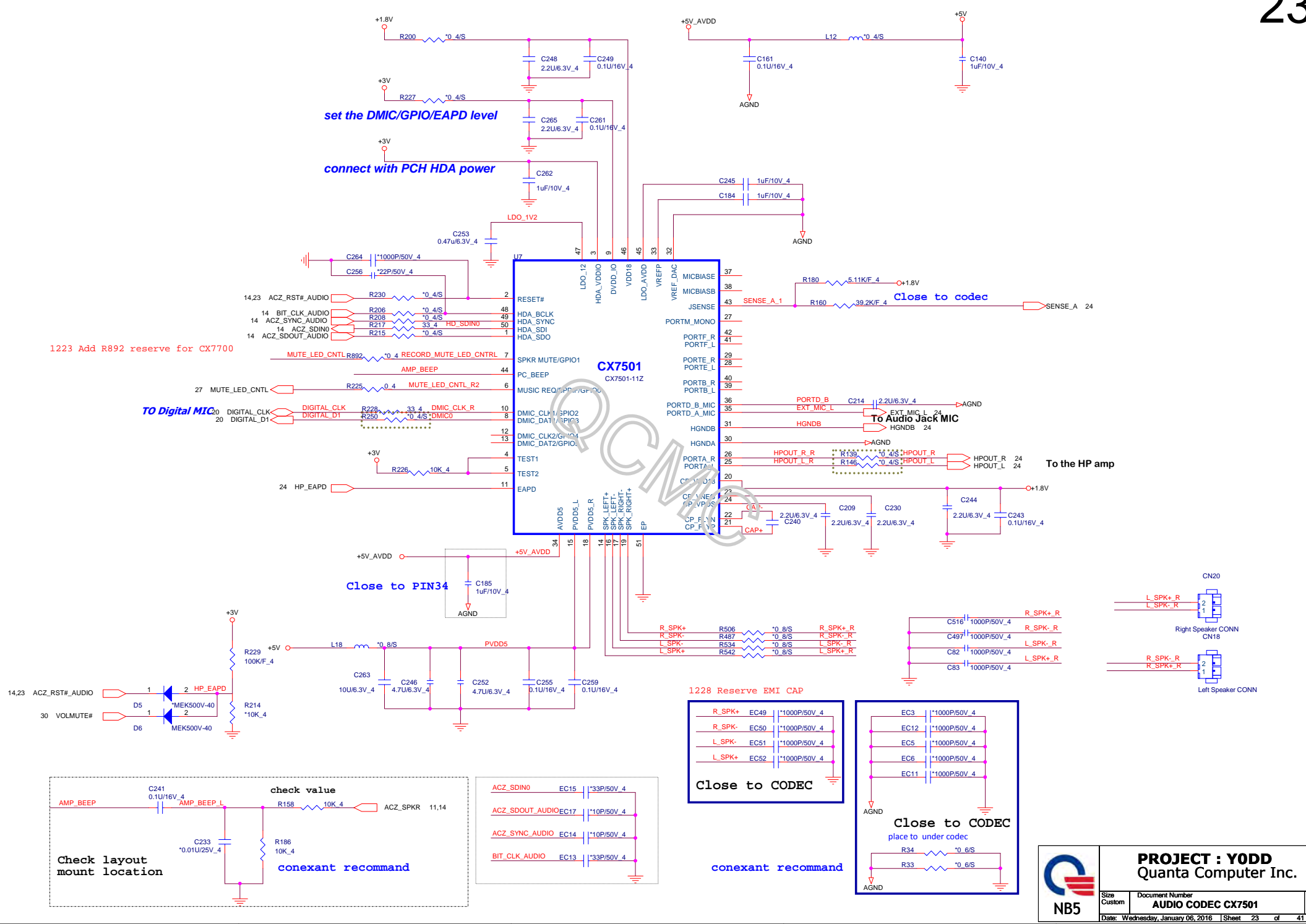
EMI Solution



1203 Update footprint from hdmi-hmrb1-ak520c-19p to hdmi-hmrb1-ak520c-19p-smt



	PROJECT : YODD		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number	
		HDMI	
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set the DMIC/GPIO/EAPD level

connect with PCH HDA power

1223 Add R892 reserve for CX7700

TO Digital MIC

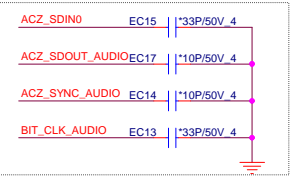
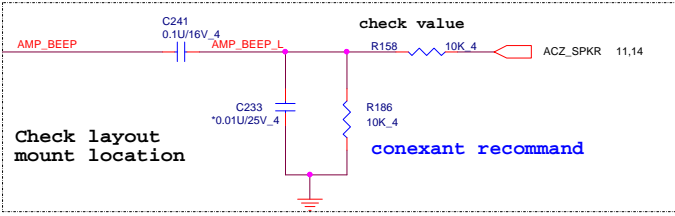
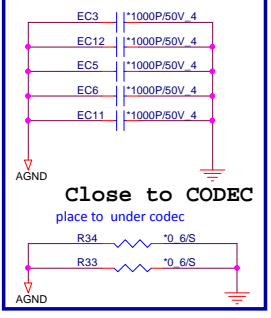
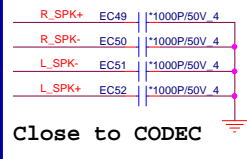
Close to codec

To Audio Jack MIC

To the HP amp

Close to PIN34

1228 Reserve EMI CAP

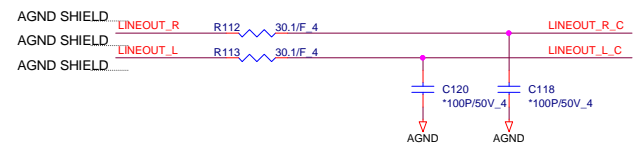
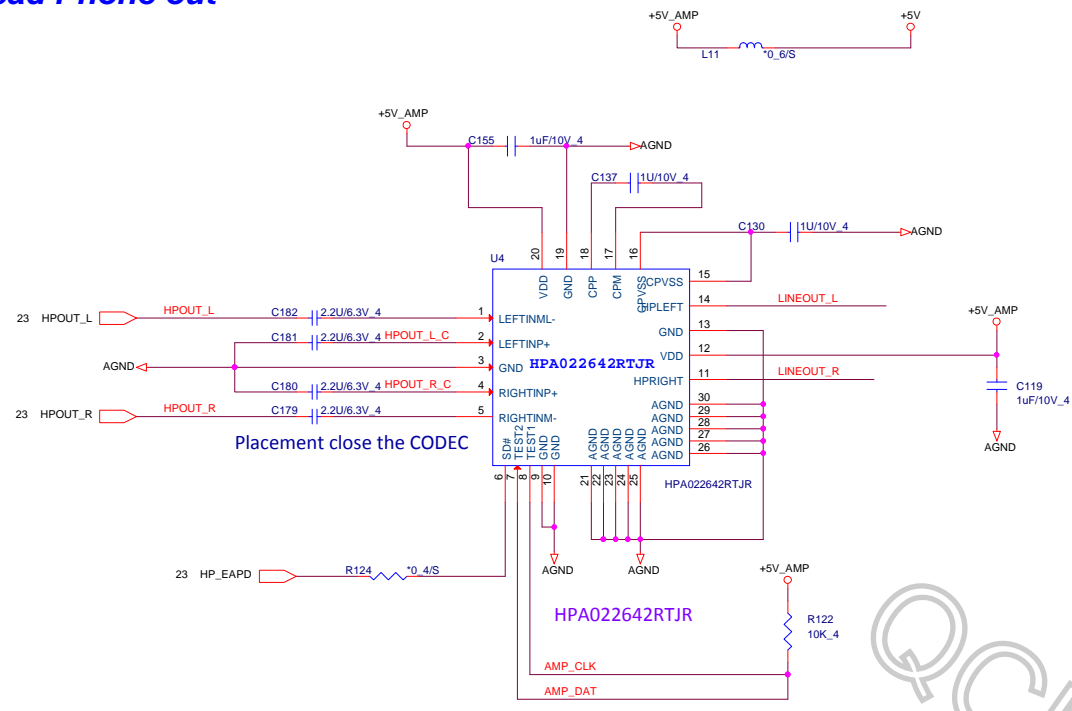


PROJECT : YODD
Quanta Computer Inc.

Size Custom Document Number **AUDIO CODEC CX7501** Rev 1A

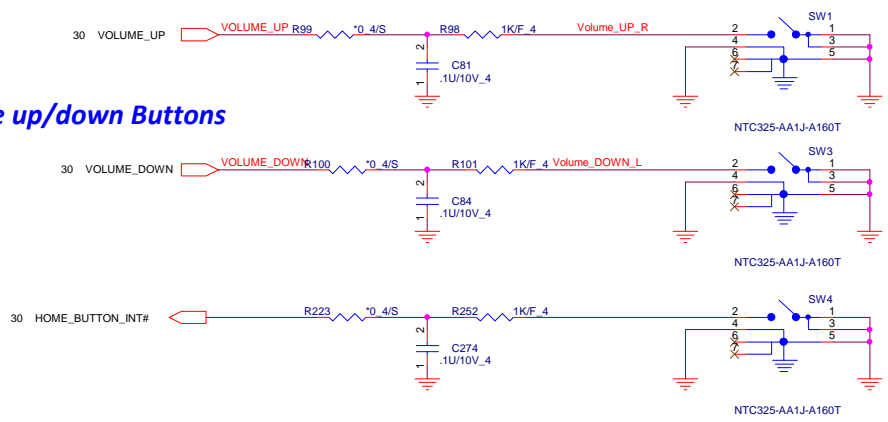
Date: Wednesday, January 06, 2016 | Sheet 23 of 41

Head Phone out

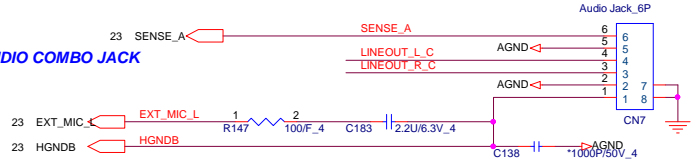


Audio combo JACK & Volume up/down Button

Volume up/down Buttons

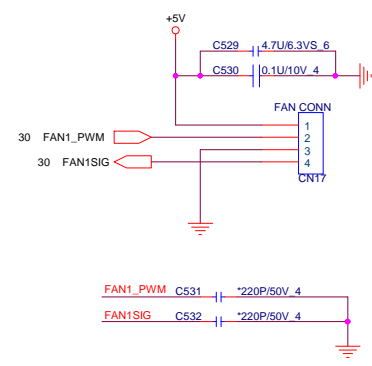


AUDIO COMBO JACK



FAN

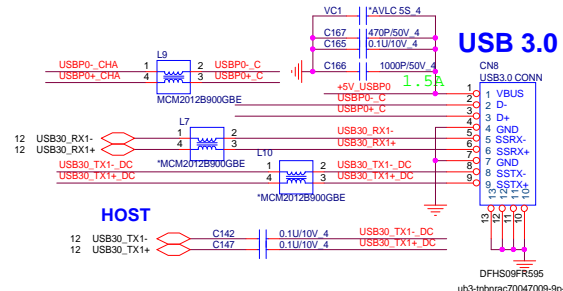
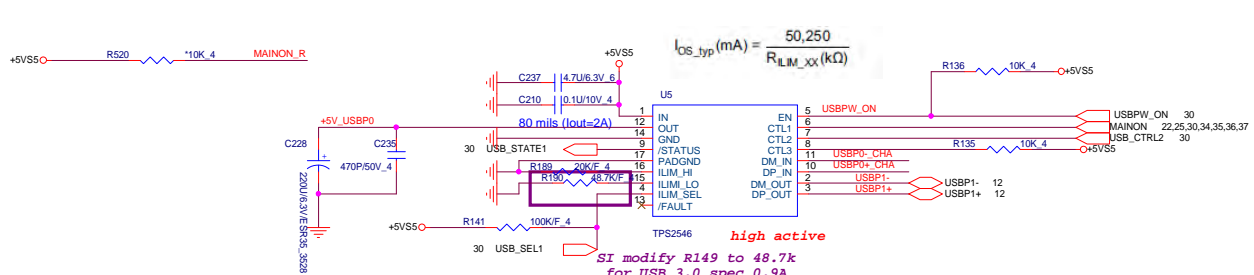
1203 Update footprint from 88266-0400-4p-1 to 88266-04x1-4p-1-smt



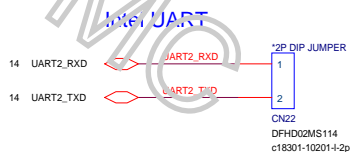
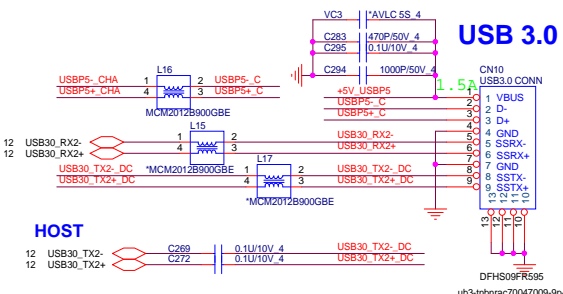
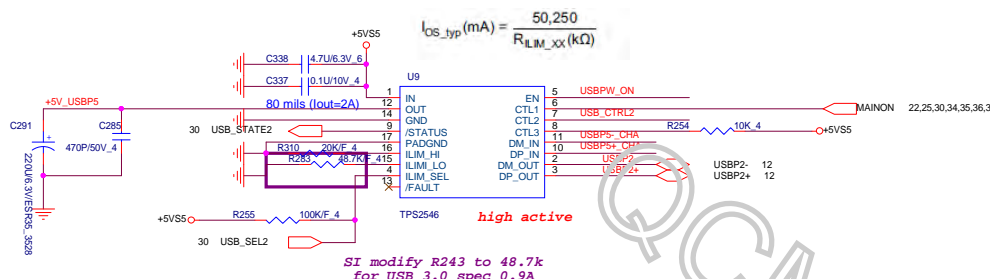
2,4,10,11,12,13,14,15,20,22,23,26,27,29,30,31,37,38 +3V
22,23,27,37 +5V
4,25,33,34,35,36,37,38,39,40 +5VSS

	PROJECT : YODD		
	Quanta Computer Inc.		
	Size Custom	Document Number AUDIO AMP	
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PV ADD R554/R555/R556 10k for USB 3.0 PU



1203 Update footprint from ub3-tbnbrac70047009-9p to ub3-tbnbrac70047009-9p-smt



Left side USB 2.0/3.0 Combo

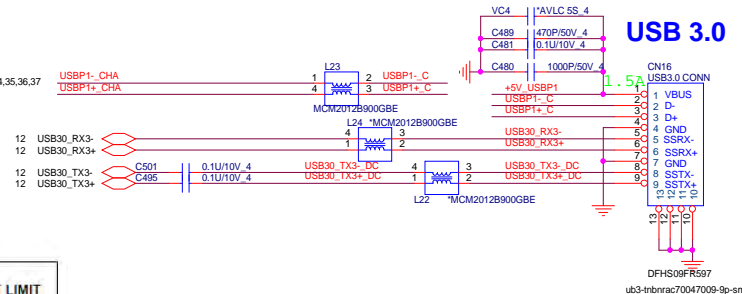
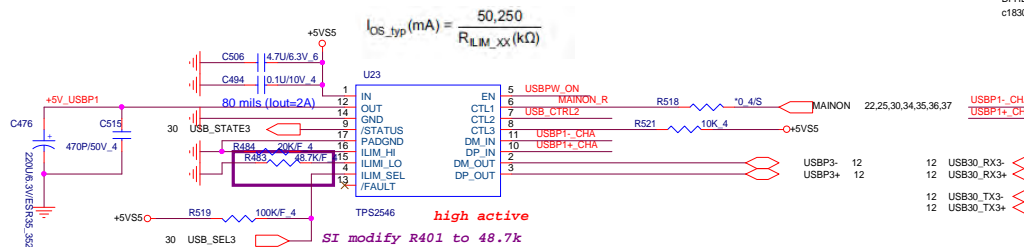
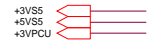


Table 3. Control Pin Settings Matched to System Power States

SYSTEM GLOBAL POWER STATE	TPS2546 CHARGING MODE	CTL1	CTL2	CTL3	ILIM_SEL	CURRENT LIMIT SETTING
S0	SDP1	1	1	0	1 or 0	ILIM_HI / ILIM_LO
S0	SDP2, no discharge to / from CDP	1	1	1	0	ILIM_LO
S0	CDP, load detection with ILIM_LO + 60mA thresholds or if a BC1.2 primary detection occurs	1	1	1	1	ILIM_HI
S4/S5	Auto mode, load detection with power wake thresholds	0	0	1	1	ILIM_HI
S3/S4/S5	Auto mode, no load detection	0	0	1	0	ILIM_HI
S3	Auto mode, keyboard/mouse wake up, load detection with ILIM_LO + 60 mA thresholds	0	1	1	1	ILIM_HI
S3	Auto mode, keyboard/mouse wake-up, no load detection	0	1	1	0	ILIM_HI
S3	SDP1, keyboard/mouse wake-up	0	1	0	1 or 0	ILIM_HI / ILIM_LO

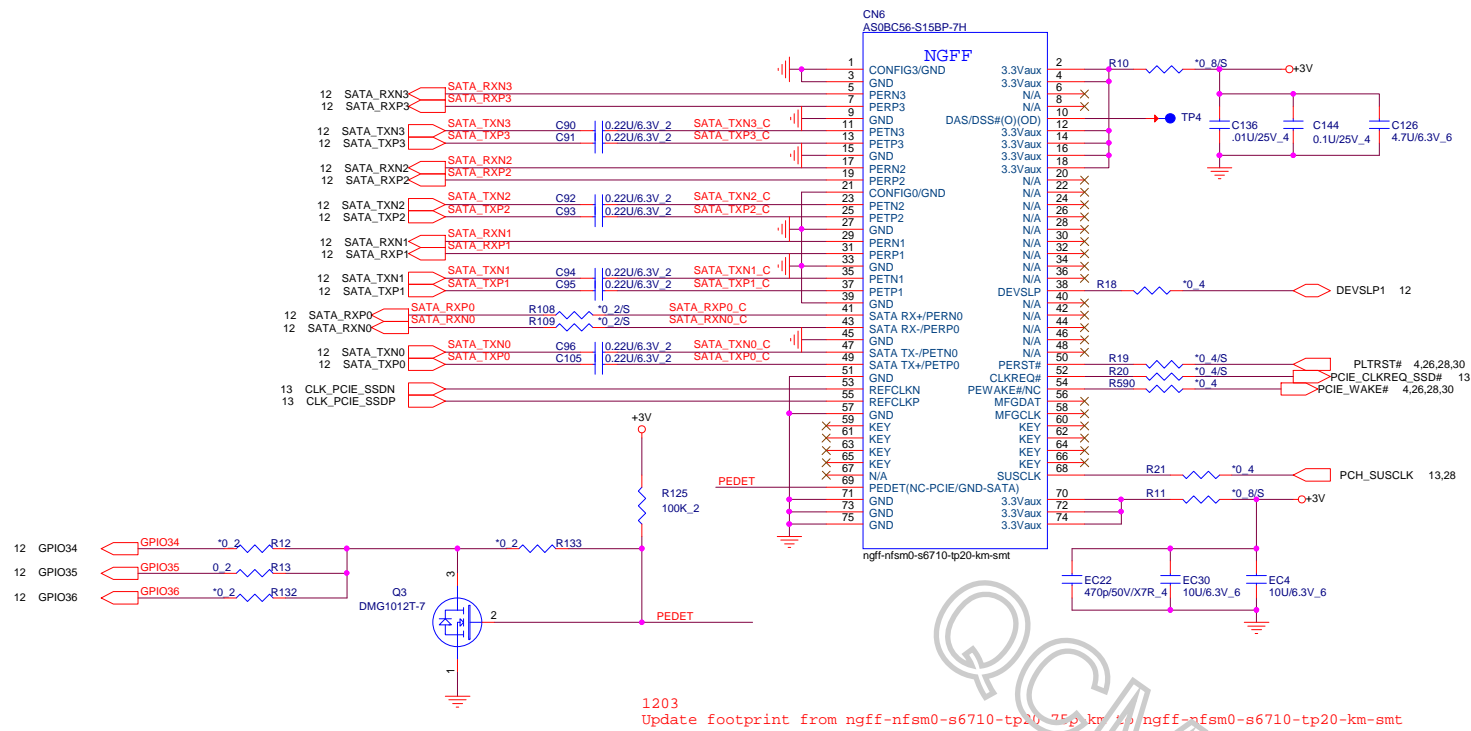
4,15,22,23,30,31,33,35,36,37
4,33,34,35,36,37,38,39,40
6,13,15,27,28,30,31,32,33



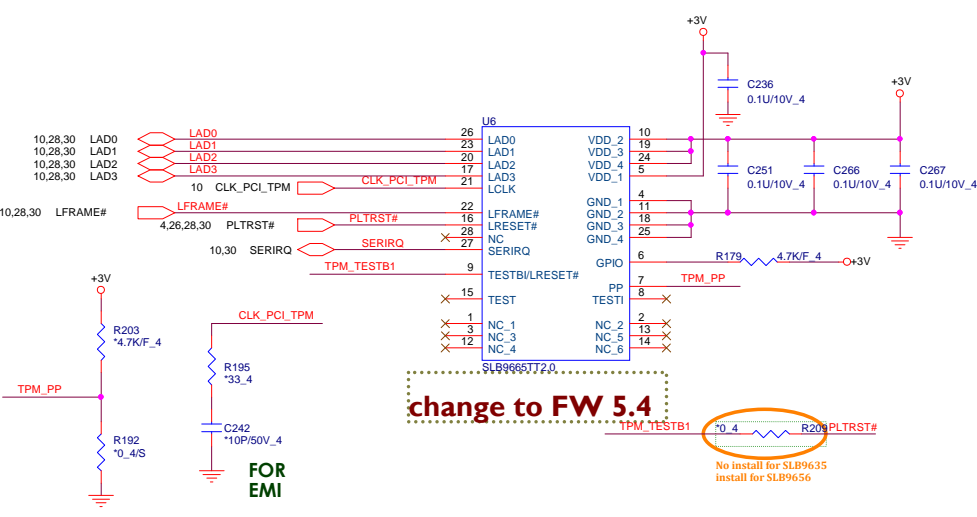
PROJECT : YODD
Quanta Computer Inc.

Size Custom Document Number **USB20/30** Rev 1A

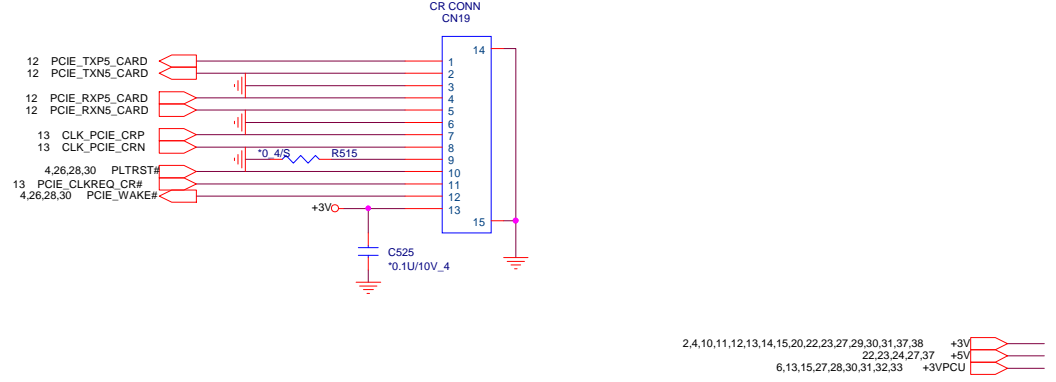
Date: Wednesday, January 06, 2016 | Sheet 25 of 41



TPM (2.0)

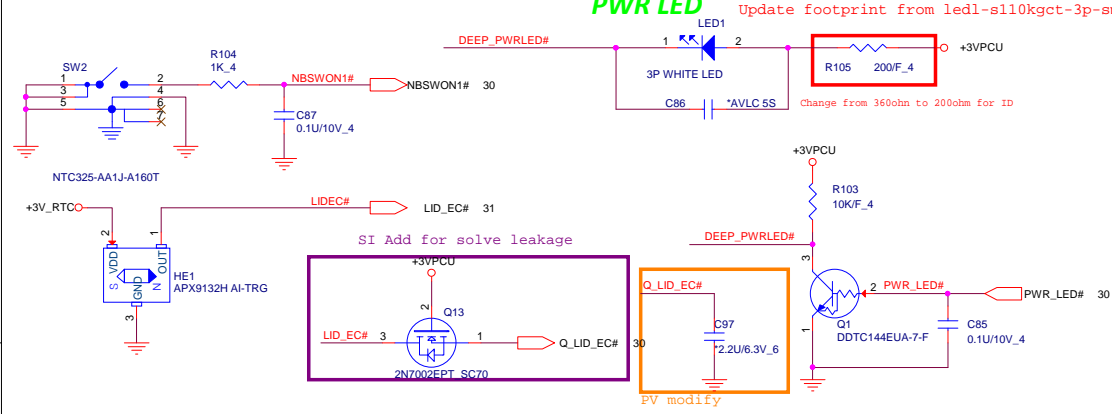


Card Reader CON

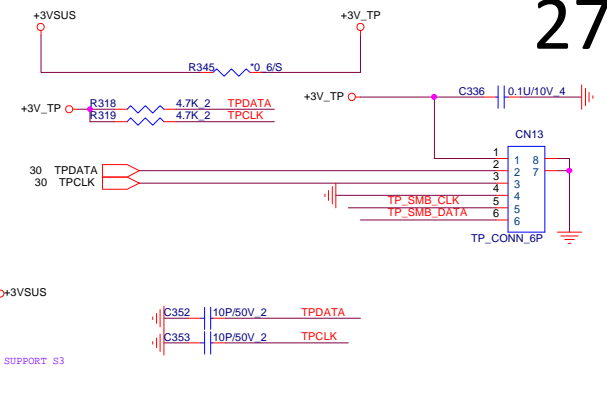
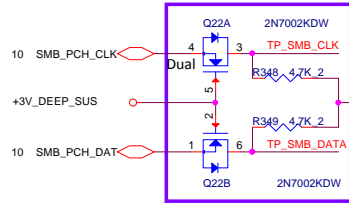


	PROJECT : YODD		+3V +5V +3VPCU
	Quanta Computer Inc.		
	Size Custom	Document Number NGFF HDD/TPM/CR	
Date: Wednesday, January 06, 2016 Sheet 26 of 41			

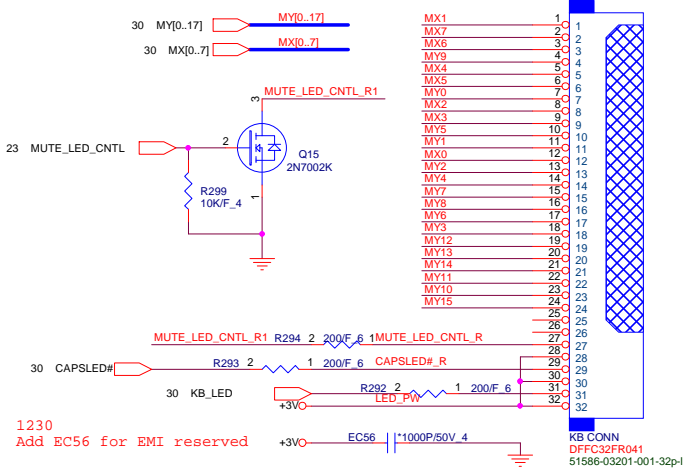
Power Button



1230
Change net name from SMB_RUN_CLK to SMB_PCH_CLK
Change net name from SMB_RUN_DAT to SMB_PCH_DAT



KEYBOARD Con.



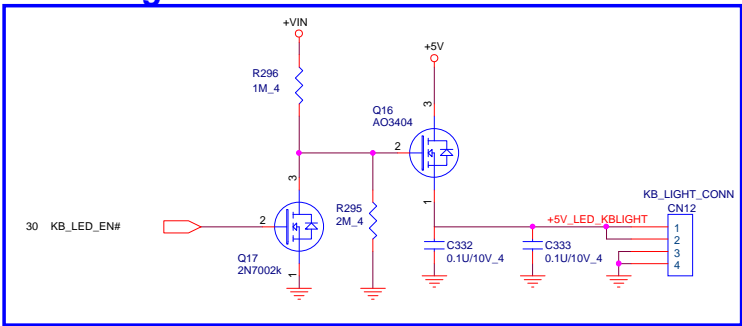
KEYBOARD PULL-UP

MY5	C321	220P/50V_4
MY6	C314	220P/50V_4
MY3	C331	220P/50V_4
MY7	C316	220P/50V_2
MY8	C315	220P/50V_2
MY9	C327	220P/50V_4
MY10	C311	220P/50V_4
MY11	C312	220P/50V_4
MY1	C320	220P/50V_2
MY2	C318	220P/50V_4
MY4	C317	220P/50V_2
MY0	C324	220P/50V_4
MX4	C326	220P/50V_4
MX6	C328	220P/50V_4
MX3	C322	220P/50V_4
MX2	C325	220P/50V_4
MX7	C307	220P/50V_4
MX5	C319	220P/50V_4
MX5	C325	220P/50V_4
MX1	C306	220P/50V_4
MY12	C330	220P/50V_4
MY13	C329	220P/50V_2
MY14	C313	220P/50V_4
MY15	C310	220P/50V_4

SI

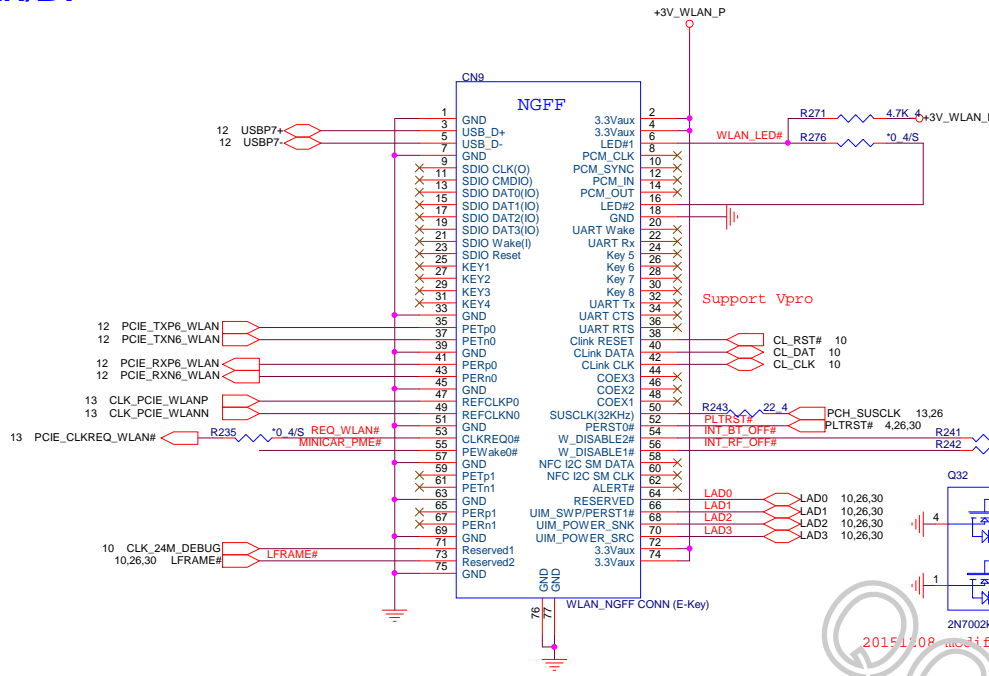
1203
Update footprint from 51586-03241-001-32p-1 to 51586-03201-001-32p-1

KB backlight

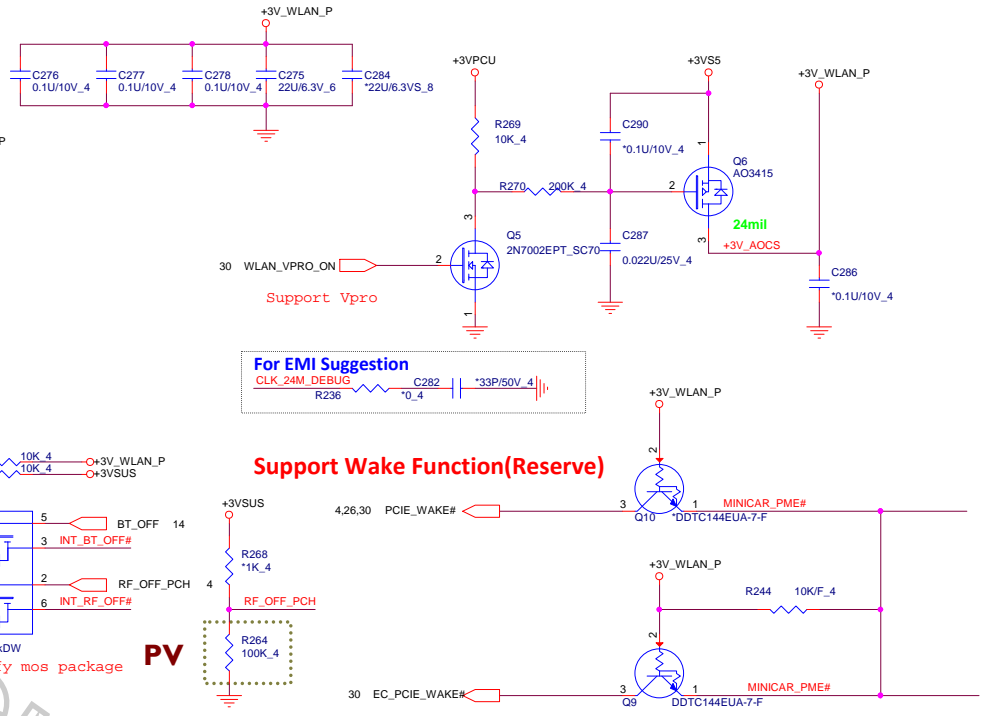


2,4,10,11,12,13,14,15,20,22,23,26,29,30,31,37,38 +3V
22,23,24,37 +5V
6,13,15,28,30,31,32,33 +3VPCU

	PROJECT : YODD		+3V +5V +3VPCU
	Quanta Computer Inc.		
	Size Custom	Document Number KB/PB/TP	
Date: Wednesday, January 06, 2016 Sheet 27 of 41			



1203 Update footprint from ngff-nfse0-s6710-tp20-75p-ke to ngff-nfse0-s6710-tp20-ke-smt

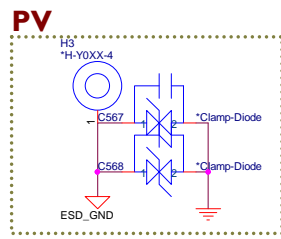
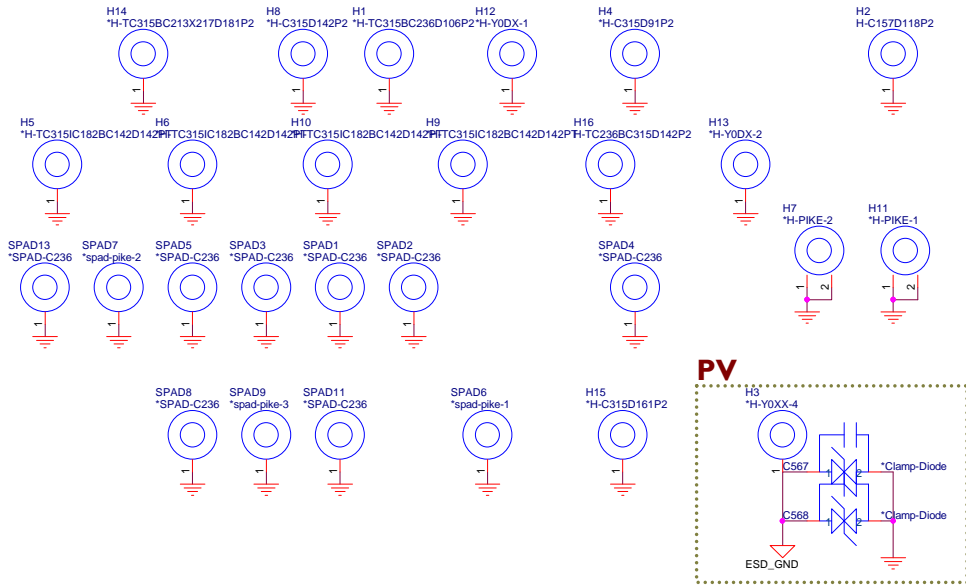


For EMI Suggestion
CLK_24M_DEBUG
R236 0.4 C282 *33P/50V_4

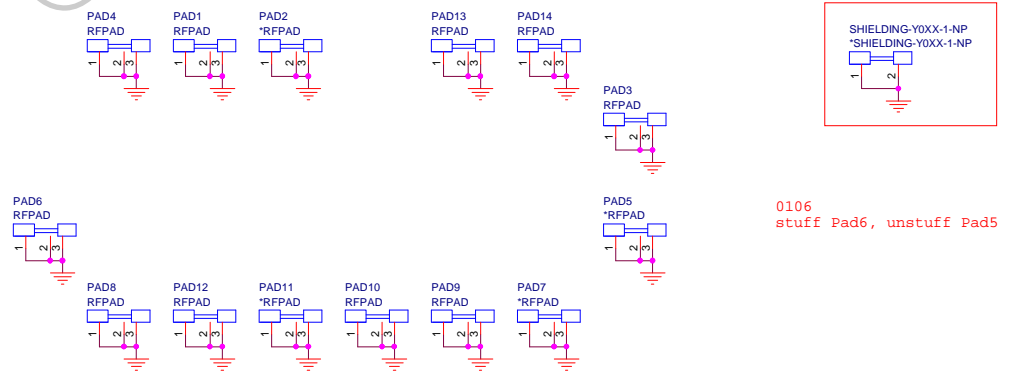
Support Wake Function(Reserve)

Hole

1229 Update H8 footprint from H-C315I142D142P2



GND GUARD



1229 Add PAD13 for EMI

1230 Add PAD14 for EMI

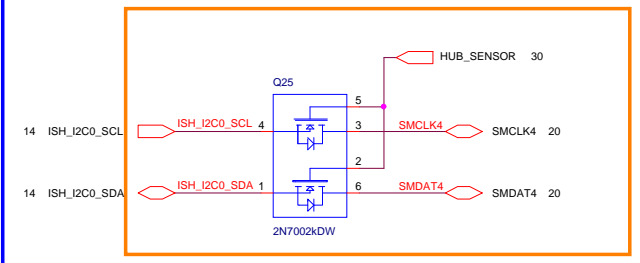
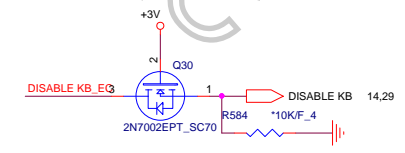
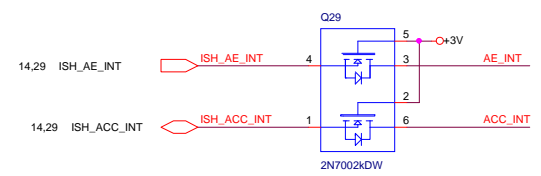
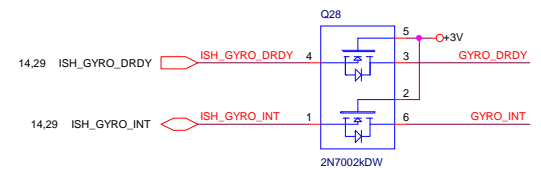
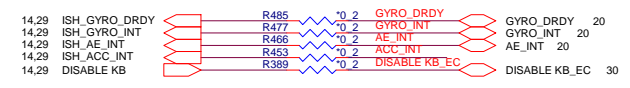
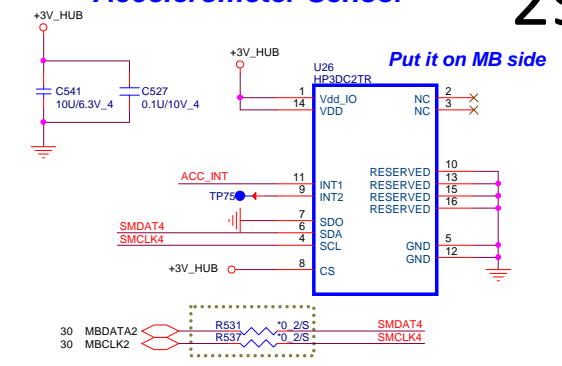
1231 Shielding for Y0XX

0106 stuff Pad6, unstuff Pad5

	PROJECT : Y0DD		Rev 1A
	Quanta Computer Inc.		
	Size Custom Document Number WLAN/HOLE		
Date: Wednesday, January 06, 2016		Sheet 28 of 41	

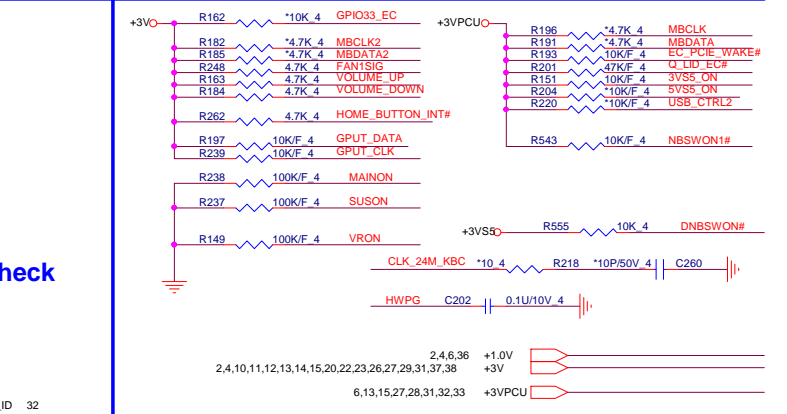
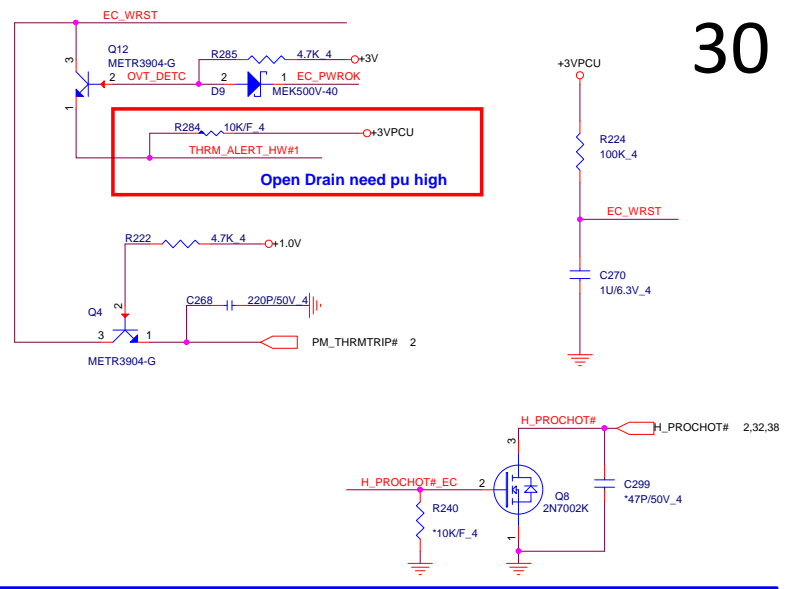
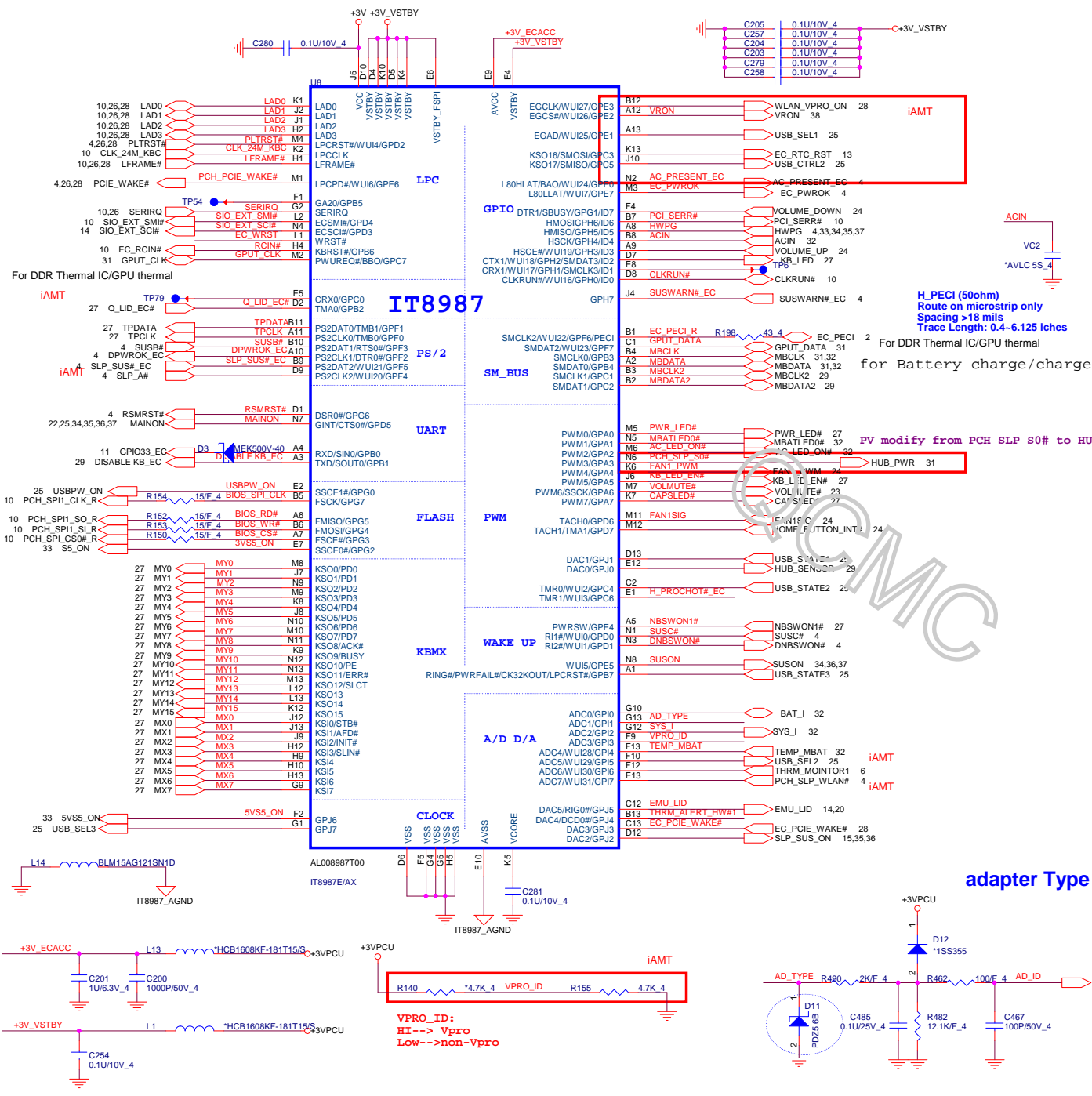
2,4,10,11,12,13,14,15,20,22,23,26,27,29,30,31,37,38 +3V
22,23,24,27,37 +5V
6,13,15,27,30,31,32,33 +3VPCU

Accelerometer Sensor



PV add for EC request

1222
Del Q26/ R587/ R588 for OLED reserve

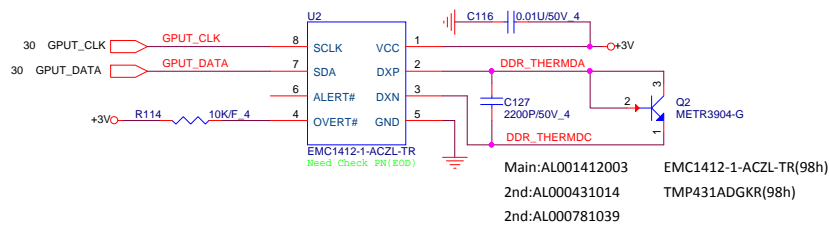
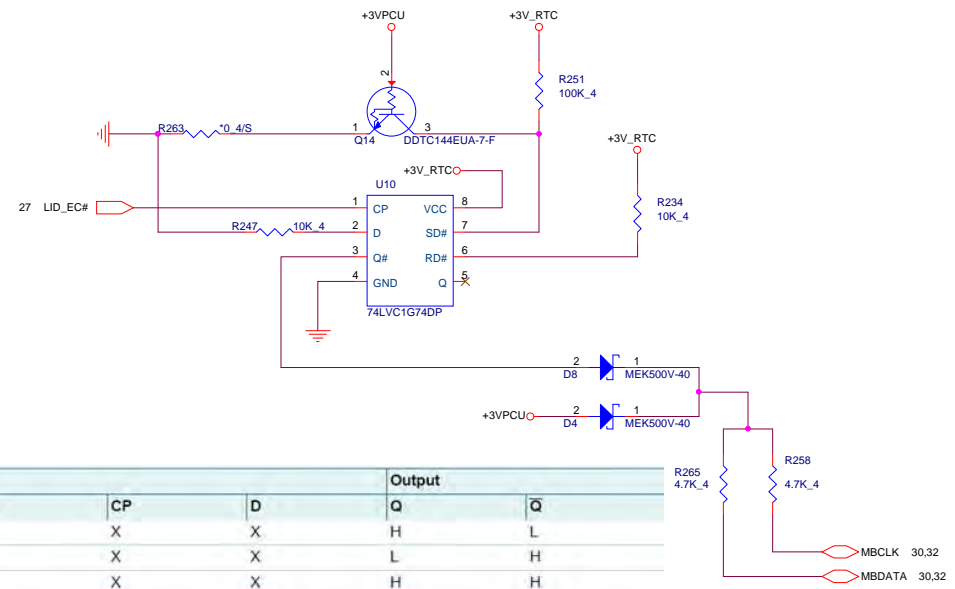
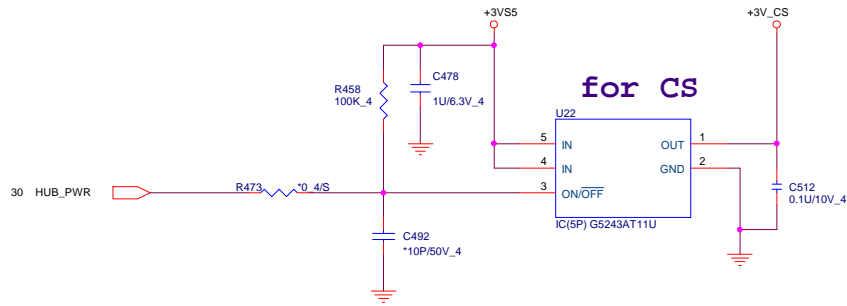


PROJECT : YODD
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	EC IT8987	1A

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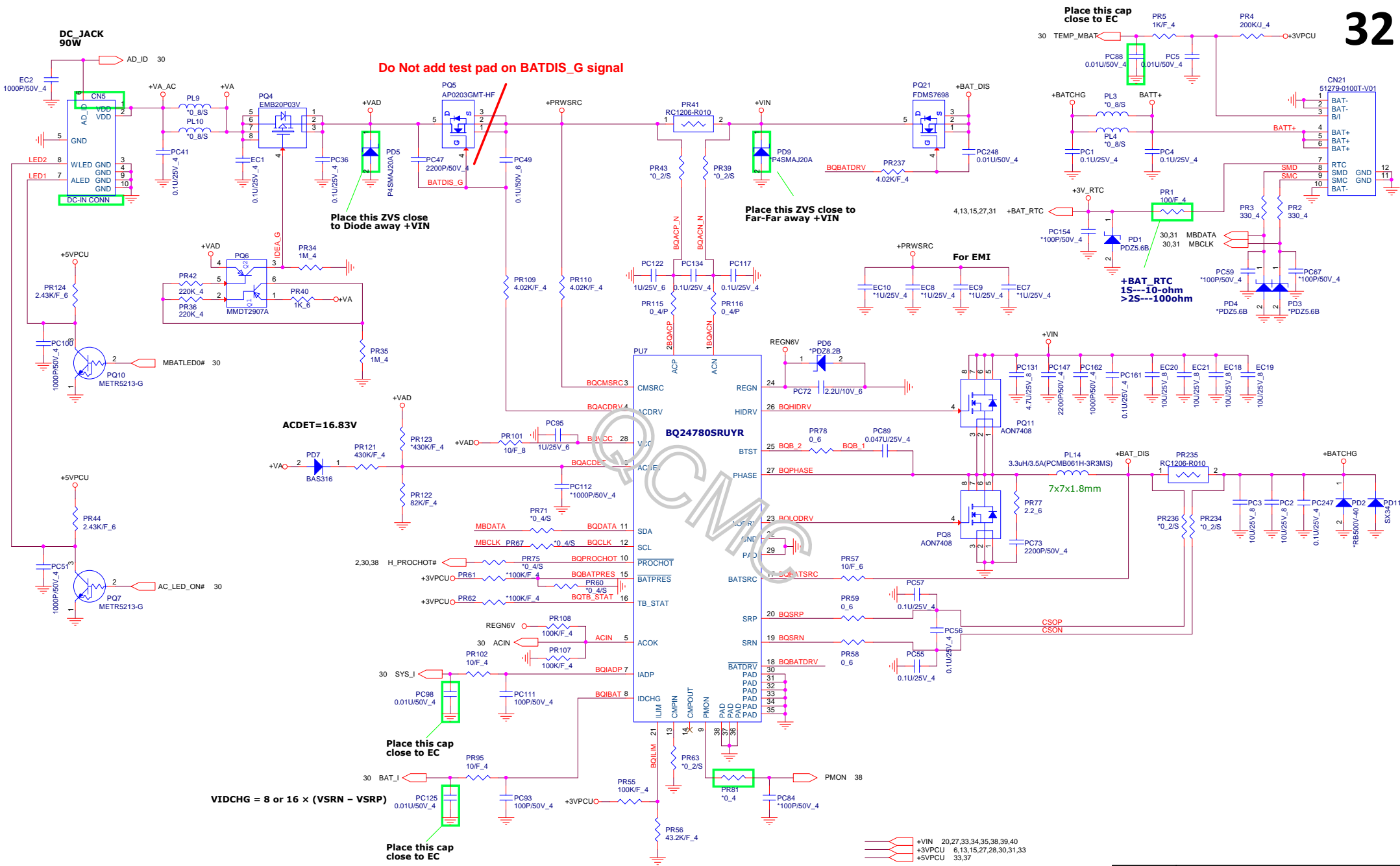


Input				Output	
SD	RD	CP	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

[1] H = HIGH voltage level;
 L = LOW voltage level;
 X = don't care.

Input				Output	
SD	RD	CP	D	Q _{n+1}	Q̄ _{n+1}
H	H	↑	L	L	H
H	H	↑	H	H	L

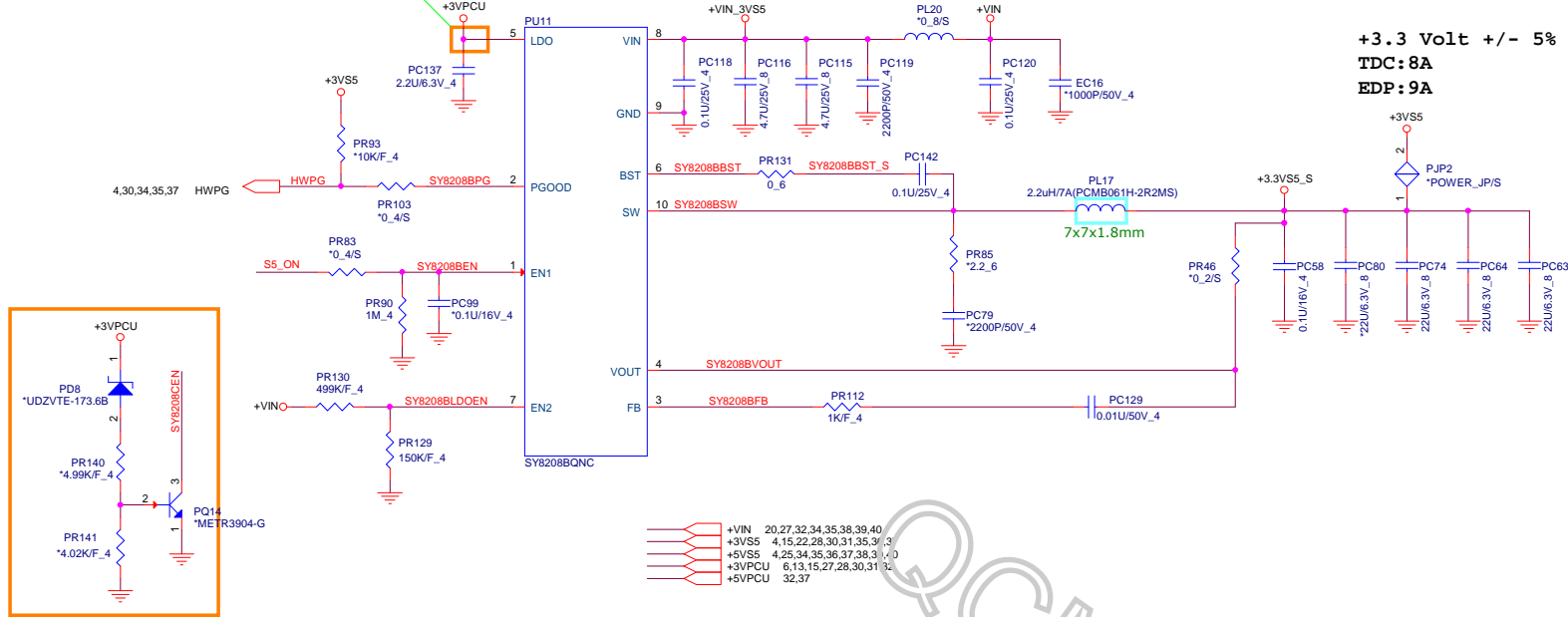
[1] H = HIGH voltage level;
 L = LOW voltage level;
 ↑ = LOW-to-HIGH CP transition;
 Q_{n+1} = state after the next LOW-to-HIGH CP transition.



		PROJECT : YODD	
		Quanta Computer Inc.	
Size Custom	Document Number Charger	Rev 1A	
Date: Wednesday, January 06, 2016		Sheet	32 of 41

DC/DC +3VS5/+5VS5

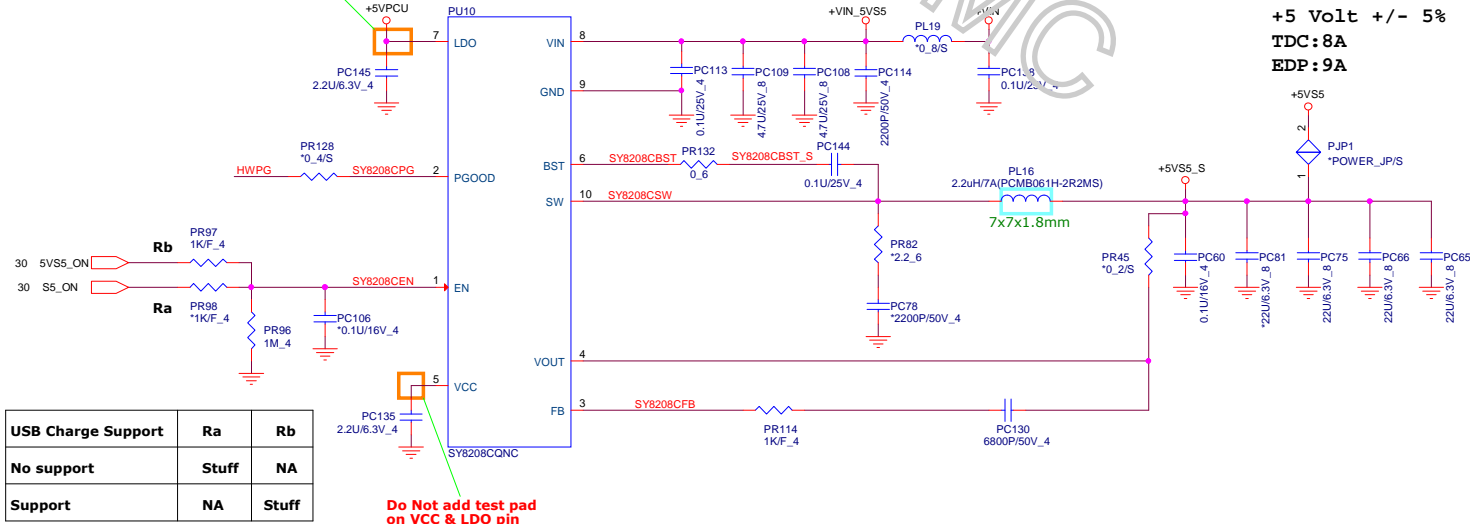
Do Not add test pad on VCC & LDO pin



+3.3 Volt +/- 5%
TDC:8A
EDP:9A

- +VIN 20,27,32,34,35,38,39,40
- +3VS5 4,15,22,28,30,31,35,37,38
- +5VS5 4,25,34,35,36,37,38,39,40
- +3VPCU 6,13,15,27,28,30,31,32
- +5VPCU 32,37

Do Not add test pad on VCC & LDO pin



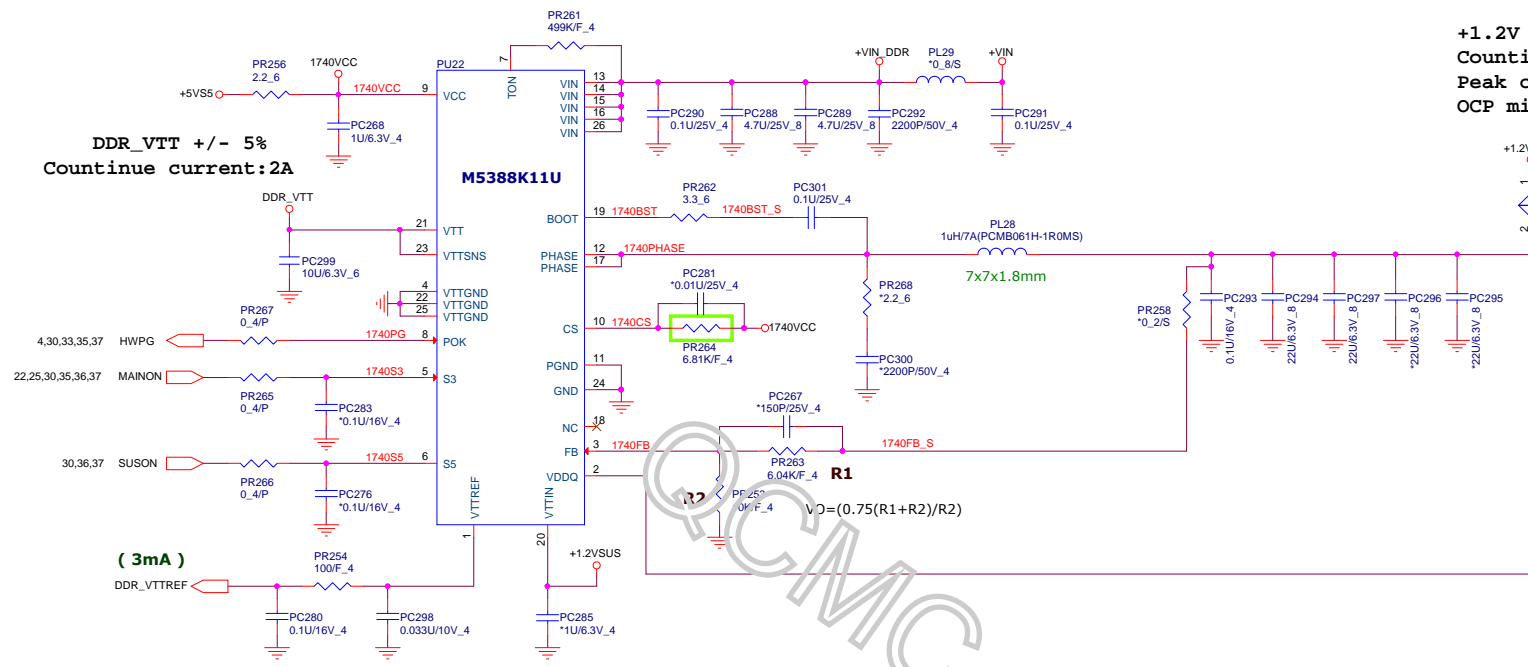
+5 Volt +/- 5%
TDC:8A
EDP:9A

USB Charge Support	Ra	Rb
No support	Stuff	NA
Support	NA	Stuff

Do Not add test pad on VCC & LDO pin

PROJECT : YODD
Quanta Computer Inc.

Size Custom	Document Number 3/555	Rev 1A
Date: Wednesday, January 06, 2016 Sheet 33 of 41		



+1.2V +/- 5%
Countinue current:6A
Peak current:8A
OCP minimum:12A

DDR_VTT +/- 5%
Countinue current:2A

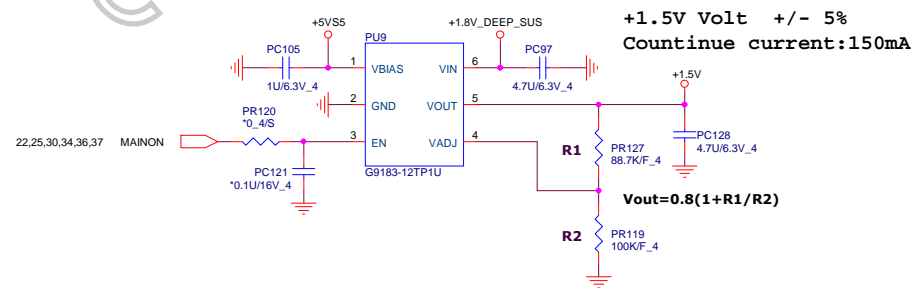
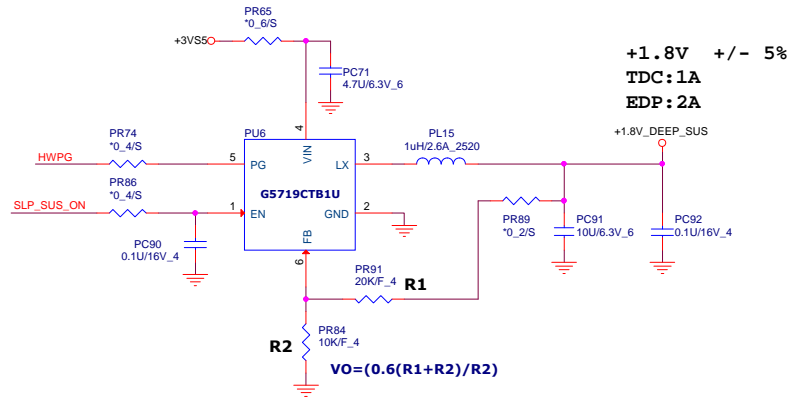
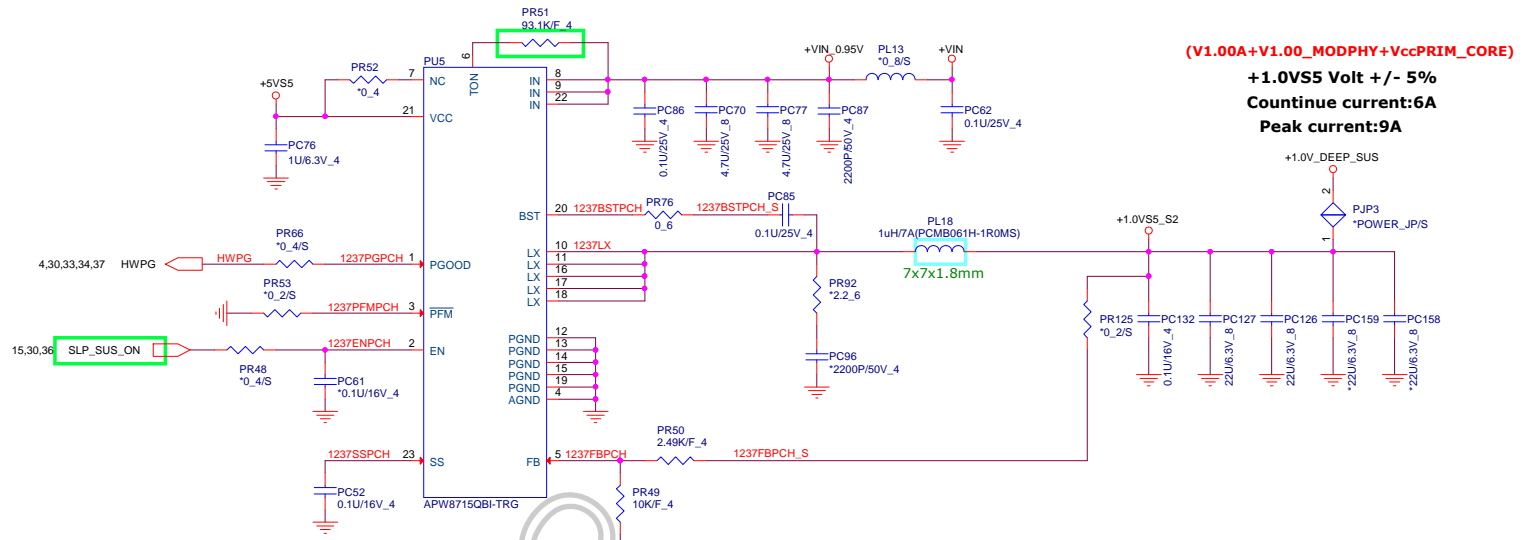
(3mA)

	S3	S5	+1.2VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

PROJECT : YODD
Quanta Computer Inc.

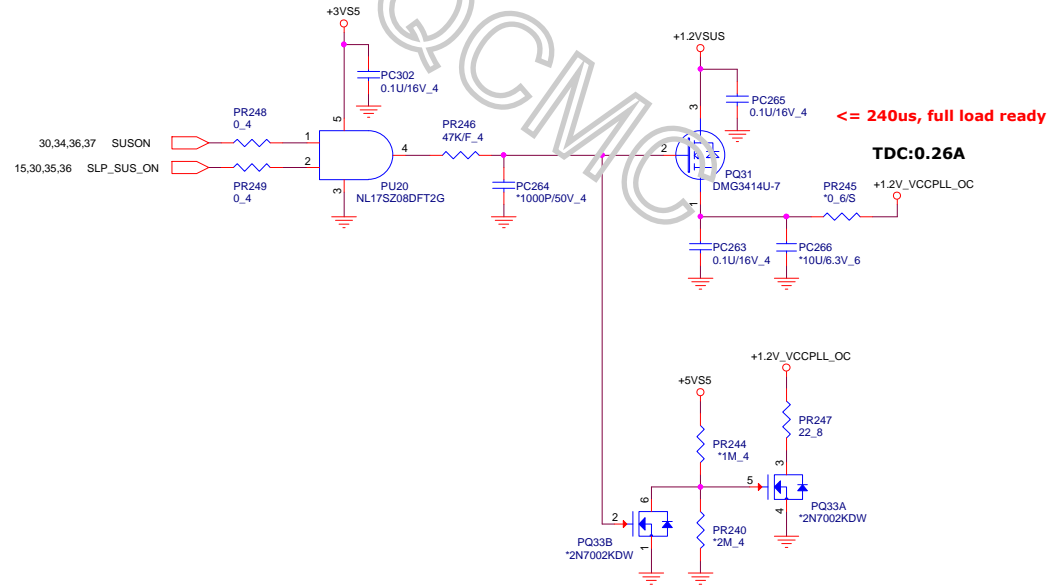
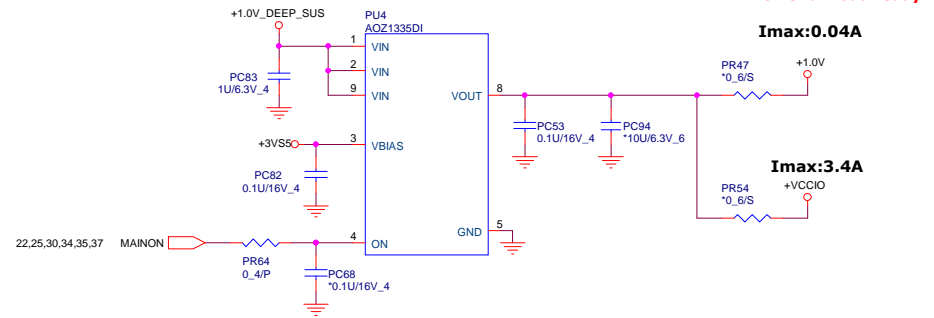
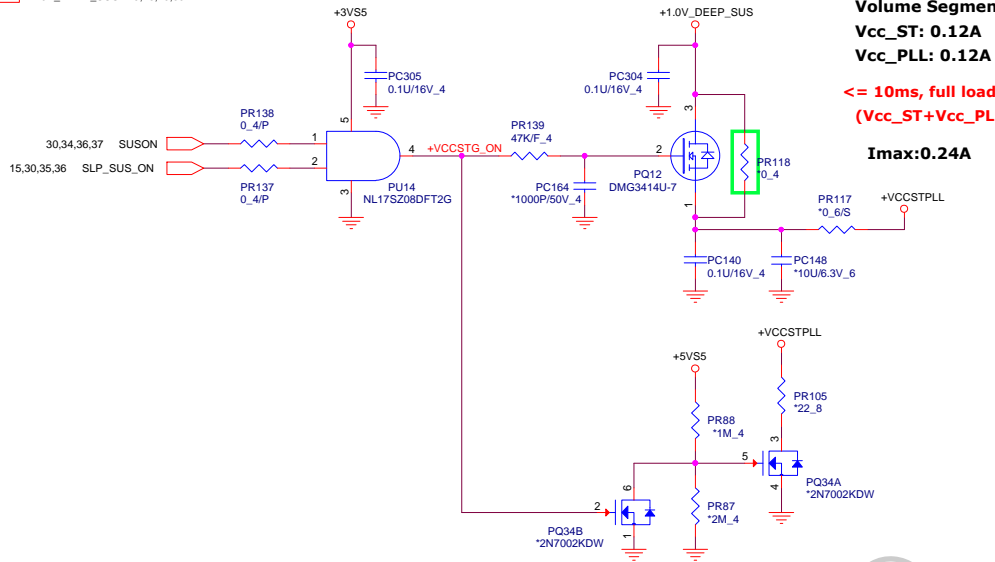
Size Custom	Document Number DDR	Rev 1A
Date: Wednesday, January 06, 2016 Sheet 34 of 41		


- +VIN 20,27,32,33,34,38,39,40
- +3VS5 4,15,22,28,30,31,33,36,37
- +5VS5 4,25,33,34,36,37,38,39,40
- +1.0V_DEEP_SUS 9,13,15,36
- +1.8V_DEEP_SUS 9,15,37



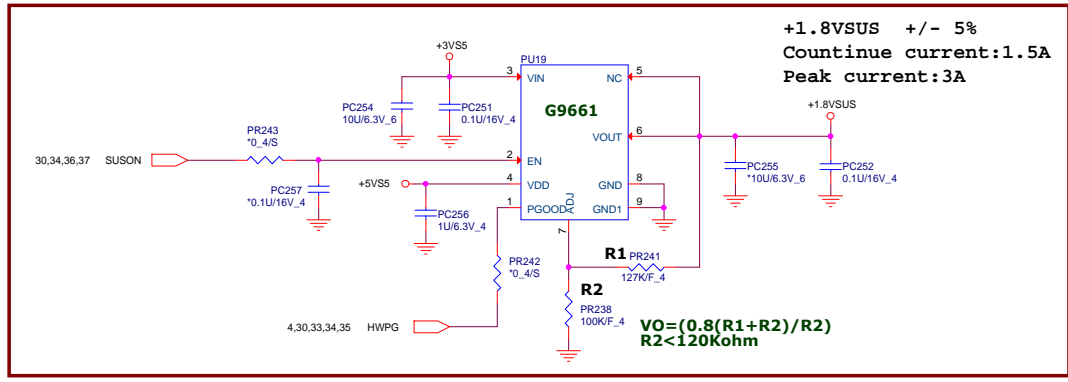
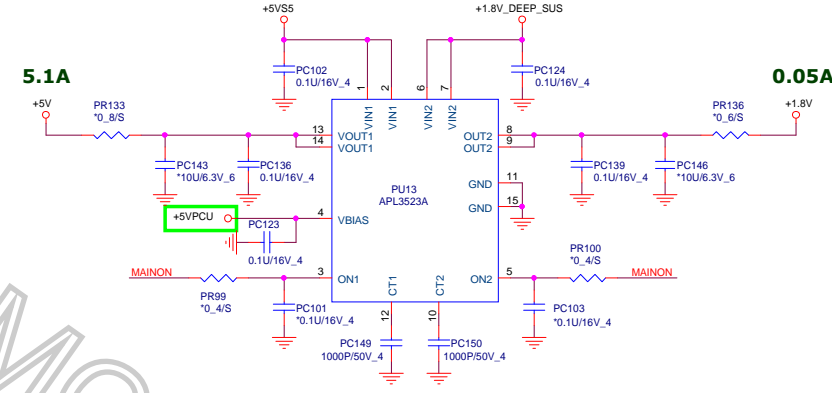
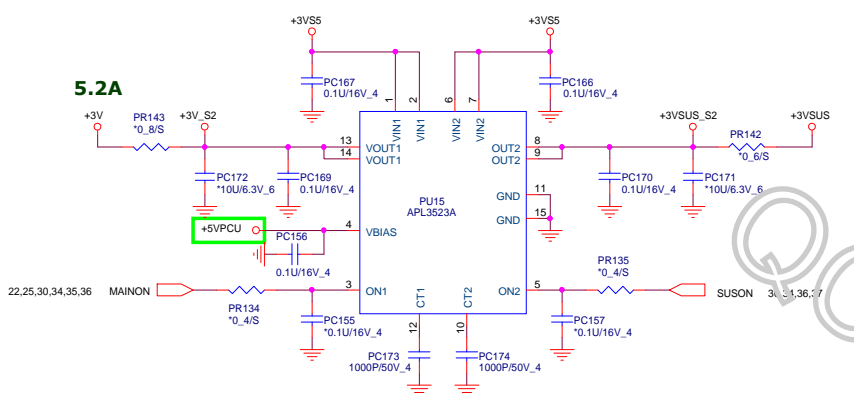
	PROJECT : YODD		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number +1.0V+1.5V+1.8V_DEEP_SUS	

- +1.0V 2,4,6,30
- +3V5S 4,15,22,28,30,31,33,35,37
- +5V5S 4,25,33,34,35,37,38,39,40
- +VCCIO 2,6,16
- +VCCSTPLL 2,5,6,9,38
- +1.0V_DEEP_SUS 9,13,15,35

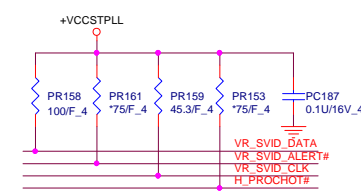
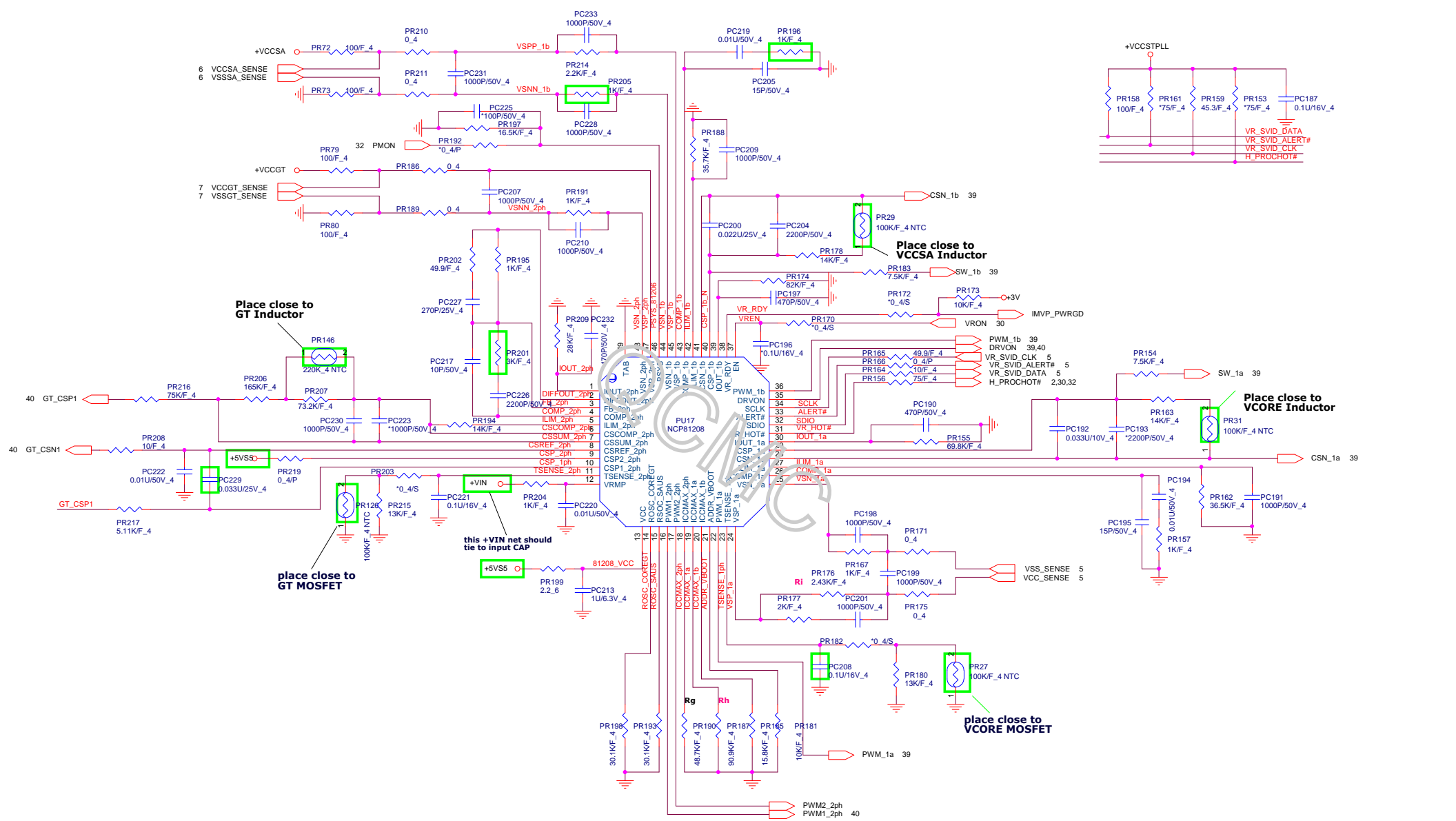


	PROJECT : YODD		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number +1.0V/+VCCSTPLL	
Date: Wednesday, January 06, 2016		Sheet 36 of 41	

- +3V 2,4,10,11,12,13,14,15,20,22,23,26,27,29,30,31,38
- +5V 22,23,24,27,37
- +3VS5 4,15,22,28,30,31,33,35,36
- +5VS5 4,25,33,34,35,36,38,39,40
- +3VSUS 27,28
- +1.8V_DEEP_SUS 9,15,35
- +1.8V 23
- +5V 22,23,24,27,37
- +VIN 20,27,32,33,34,35,38,39,40
- +1.8VSUS 17,18



- +VCCSA 6,39
- +VCCGT 7,40
- +5VPUC 32,33,37
- +5V 22,23,24,27,37



Place close to GT Inductor

Place close to VCCSA Inductor

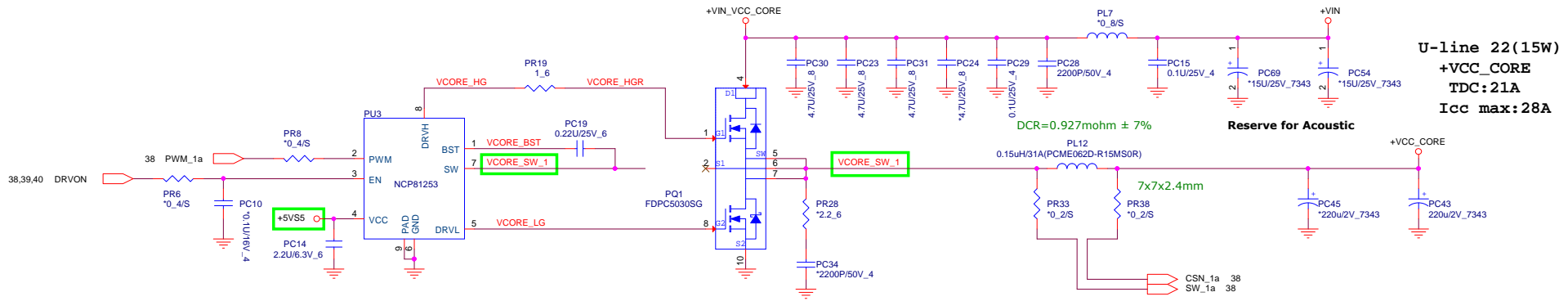
Place close to VCore Inductor

place close to GT MOSFET

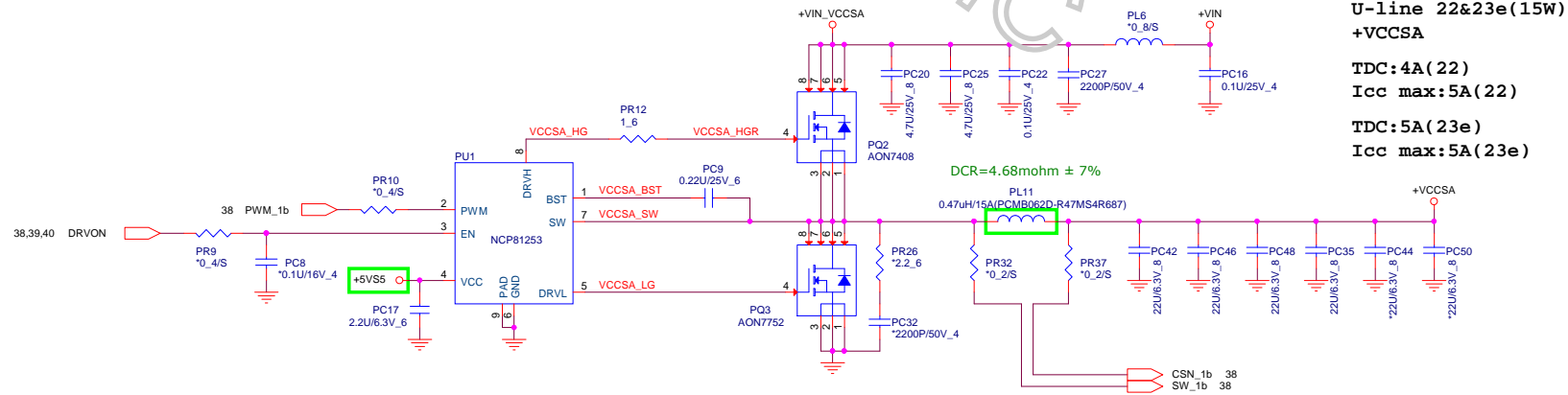
place close to VCore MOSFET

this +VIN net should tie to input CAP

	PROJECT : YODD		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number CPU VR IC (NCP81208)	
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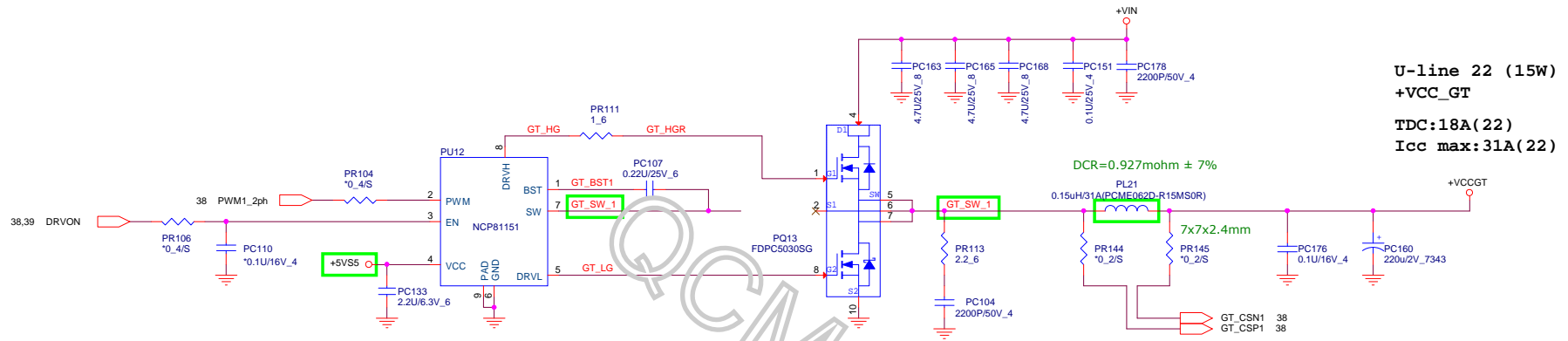


VCCSA



	PROJECT : YODD	
	Quanta Computer Inc.	
	Size Custom	Document Number +VCCORE/VCCSA (NCP81253)
Date: Wednesday, January 06, 2016 Sheet 39 of 41		

- +VIN 20,27,32,33,34,35,38,39
- +VCCGT 7,38
- +VIN_VCC_CORE
- +VPCU 32,33,37
- +5V 22,23,24,27,37



U-line 22 (15W)
 +VCC_GT
 TDC:18A(22)
 Icc max:31A(22)

	PROJECT : YODD		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number +VCCGT (NCP81151)	
Date: Wednesday, January 06, 2016		Sheet 40 of 41	