

MODEL NAME : Maple  
PCB NO : DA8000WL000 LA-B012PR01

# Dell / Compal Confidential

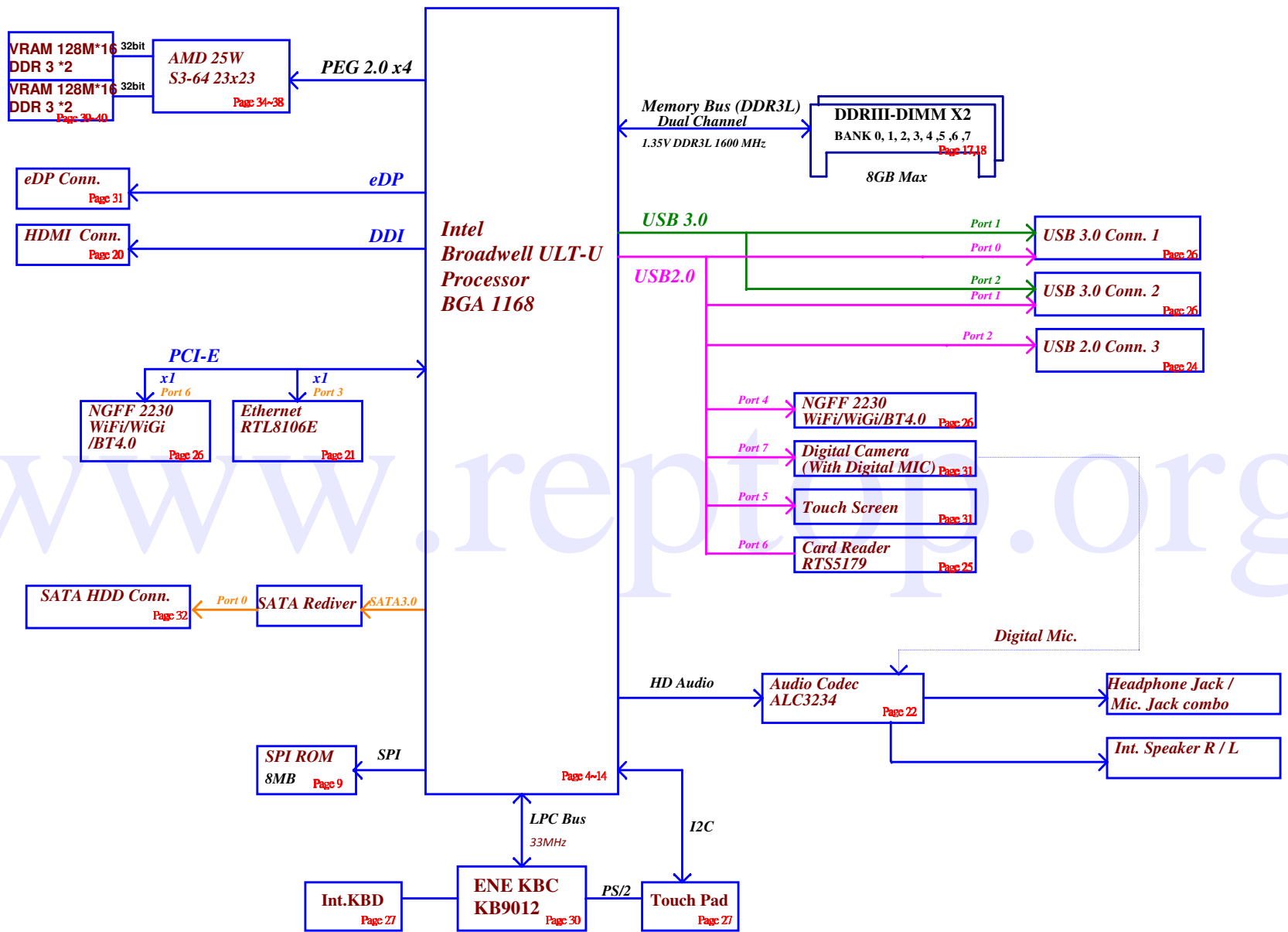
## Schematic Document

Intel Shark Bay ULT  
Maple 14"/15" Value  
UMA / DIS AMD 25W/S3+DDR3x4

2014-01-21

Rev: 1.0

|  |                    |                 |            |                          |                            |
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|  |                    |                 |            | Document Number          | LA-B012P                   |
| Date: Tuesday, August 05, 2014   |                    |                 |            | Sheet                    | 1 of 55                    |



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| Size   | 1.0                | Rev             | 1.0                      |   |



### Board ID Table for AD channel

| Vcc      | 3.3V +/- 1% |             |             |             |             |
|----------|-------------|-------------|-------------|-------------|-------------|
| Ra       | 100K +/- 1% |             |             |             |             |
| Board ID | Rb          | VAD_BID min | VAD_BID typ | VAD_BID max | EC AD3      |
| 0        | 0           | 0.000V      | 0.000V      | 0.300V      | 0x00 - 0x0B |
| 1        | 12K +/- 1%  | 0.347V      | 0.354V      | 0.360V      | 0x0C - 0x1C |
| 2        | 15K +/- 1%  | 0.423V      | 0.430V      | 0.438V      | 0x1D - 0x26 |
| 3        | 20K +/- 1%  | 0.541V      | 0.550V      | 0.559V      | 0x27 - 0x30 |
| 4        | 27K +/- 1%  | 0.691V      | 0.702V      | 0.713V      | 0x31 - 0x3B |
| 5        | 33K +/- 1%  | 0.807V      | 0.819V      | 0.831V      | 0x3C - 0x46 |
| 6        | 43K +/- 1%  | 0.978V      | 0.992V      | 1.006V      | 0x47 - 0x54 |
| 7        | 56K +/- 1%  | 1.169V      | 1.185V      | 1.200V      | 0x55 - 0x64 |
| 8        | 75K +/- 1%  | 1.398V      | 1.414V      | 1.430V      | 0x65 - 0x76 |
| 9        | 100K +/- 1% | 1.634V      | 1.650V      | 1.667V      | 0x77 - 0x87 |
| 10       | 130K +/- 1% | 1.849V      | 1.865V      | 1.881V      | 0x88 - 0x96 |
| 11       | 160K +/- 1% | 2.015V      | 2.031V      | 2.046V      | 0x97 - 0xA3 |
| 12       | 200K +/- 1% | 2.185V      | 2.200V      | 2.215V      | 0xA4 - 0xAD |
| 13       | 240K +/- 1% | 2.316V      | 2.329V      | 2.343V      | 0xAE - 0xB7 |
| 14       | 270K +/- 1% | 2.395V      | 2.408V      | 2.421V      | 0xB8 - 0xC0 |
| 15       | 330K +/- 1% | 2.521V      | 2.533V      | 2.544V      | 0xC1 - 0xC9 |
| 16       | 430K +/- 1% | 2.667V      | 2.677V      | 2.687V      | 0xCA - 0xD3 |
| 17       | 560K +/- 1% | 2.791V      | 2.800V      | 2.808V      | 0xD4 - 0xDC |
| 18       | 750K +/- 1% | 2.905V      | 2.912V      | 2.919V      | 0xDD - 0xE6 |
| 19       | NC          | 3.000V      | 3.300V      | 3.300V      | 0xE7 - 0xFF |

### HSW BOARD ID Table

| Board ID | UMA | DIS (JET) | DIS (Topaz) |
|----------|-----|-----------|-------------|
| 0        | SSI |           |             |
| 1        |     | SSI       |             |
| 2        |     |           | SSI         |
| 3        | PT  |           |             |
| 4        |     | PT        |             |
| 5        |     |           | PT          |
| 6        | ST  |           |             |
| 7        |     | ST        |             |
| 8        |     |           | ST          |
| 9        | 1.0 |           |             |
| 10       |     | 1.0       |             |
| 11       |     |           | 1.0         |

### BDW BOARD ID Table

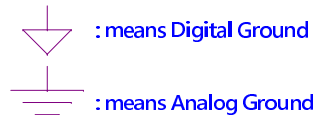
| Board ID | UMA     | DIS (JET) | DIS (Topaz) |
|----------|---------|-----------|-------------|
| 0        | Pre-SSI |           |             |
| 1        |         | Pre-SSI   |             |
| 2        |         |           | Pre-SSI     |
| 3        | SSI     |           |             |
| 4        |         | SSI       |             |
| 5        |         |           | SSI         |
| 6        | PT      |           |             |
| 7        |         | PT        |             |
| 8        |         |           | PT          |
| 9        | ST      |           |             |
| 10       |         | ST        |             |
| 11       |         |           | ST          |
| 12       | 1.0     |           |             |
| 13       |         | 1.0       |             |
| 14       |         |           | 1.0         |

### SMBUS Control Table

|                          | SOURCE | BATT | Charger | VGA | DIMM | XDP | Thermal Sensor | FFS |
|--------------------------|--------|------|---------|-----|------|-----|----------------|-----|
| EC_SMB_CK1<br>EC_SMB_DA1 | KB9012 | V    | V       |     |      |     |                |     |
| EC_SMB_CK2<br>EC_SMB_DA2 | KB9012 |      |         | V   |      |     | V              |     |
| SMBCLK<br>SMBDATA        | ULT    |      |         |     | V    | V   |                | V   |
| SML0CLK<br>SML0DATA      | ULT    |      |         |     |      |     |                |     |
| SML1CLK<br>SML1DATA      | ULT    |      |         |     |      |     |                |     |

Link

### Symbol Note :



### CLOCK SIGNAL

|              |                  |
|--------------|------------------|
| CLKOUT_PCIE0 |                  |
| CLKOUT_PCIE1 |                  |
| CLKOUT_PCIE2 | 10/100 LAN       |
| CLKOUT_PCIE3 | MINI Card (WLAN) |
| CLKOUT_PCIE4 | dGPU             |
| CLKOUT_PCIE5 |                  |

ULT

### USB3.0

Port1 USB connector 1

Port2 USB connector 2

Port3

Port4

### USB2.0

Port0 USB connector 1

Port1 USB connector 2

Port2 USB connector 3 (D/B)

Port3

Port4 MINI Card (WLAN)

Port5 Touch Screen Panel

Port6 Card Reader

Port7 Camera

### PCI EXPRESS

Lane 1

Lane 2

Lane 3 10/100 LAN

Lane 4 MINI Card (WLAN)

Lane 5 PEG (AMD JET/TOBAZ)

Lane 6

### SATA

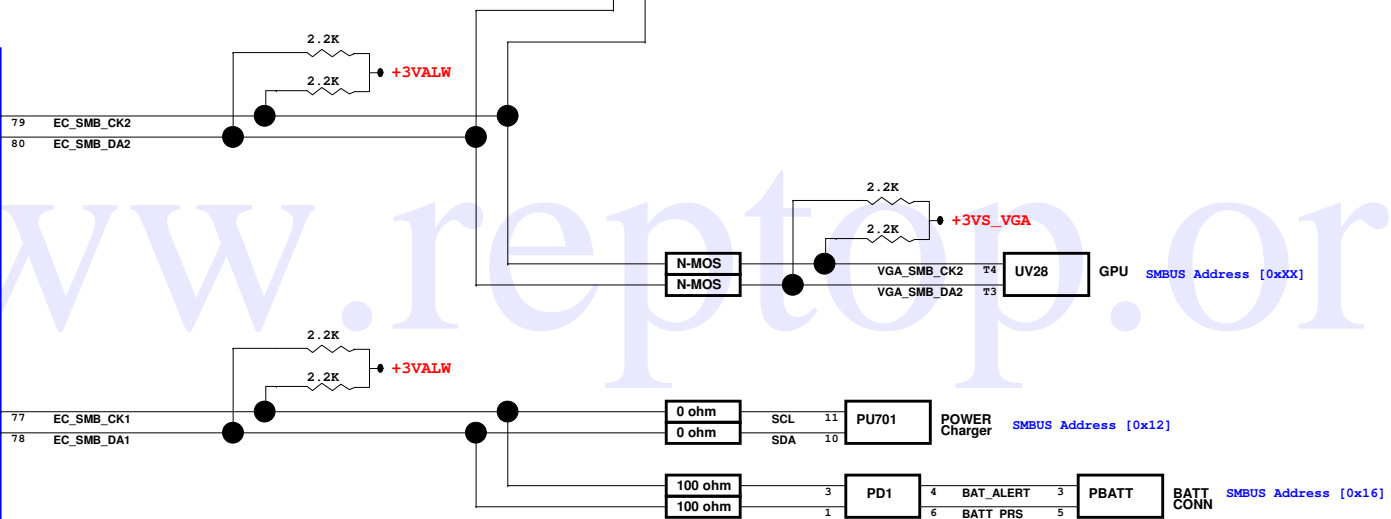
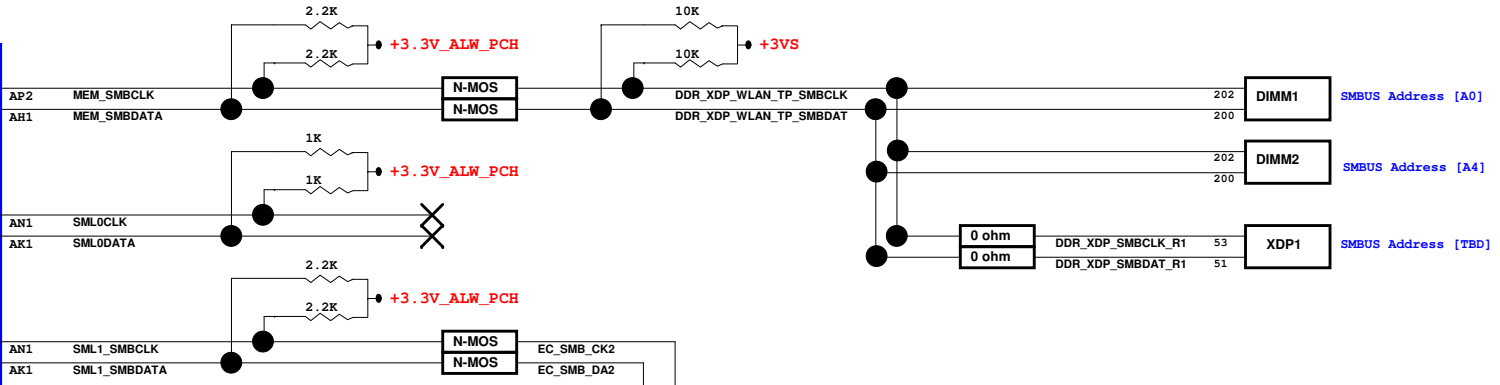
SATA0 HDD

SATA1

SATA2

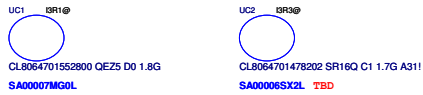
SATA3

SMBUS Address [0x9a]

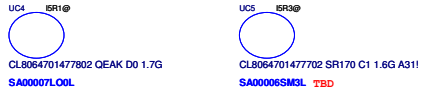


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|  |                    |                 |                          | 1.0                            |
|  |                    |                 |                          | Date: Tuesday, August 05, 2014 |
|  |                    |                 |                          | Sheet 5 of 55                  |

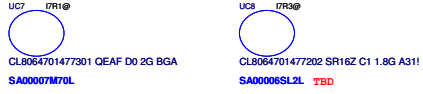
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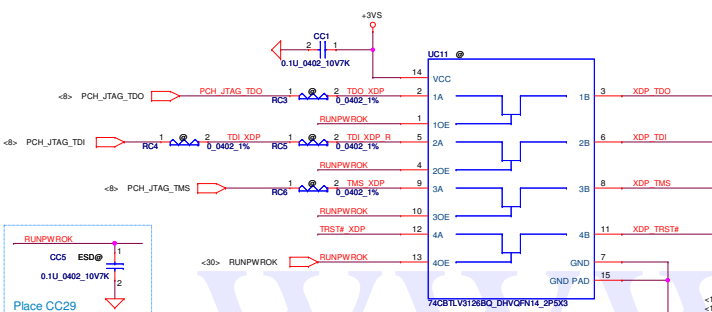
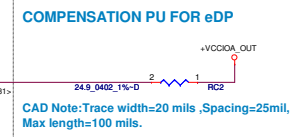
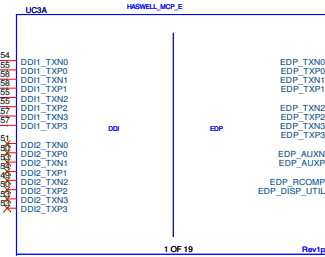
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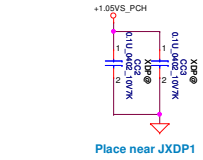
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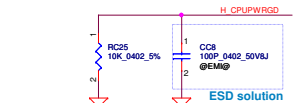
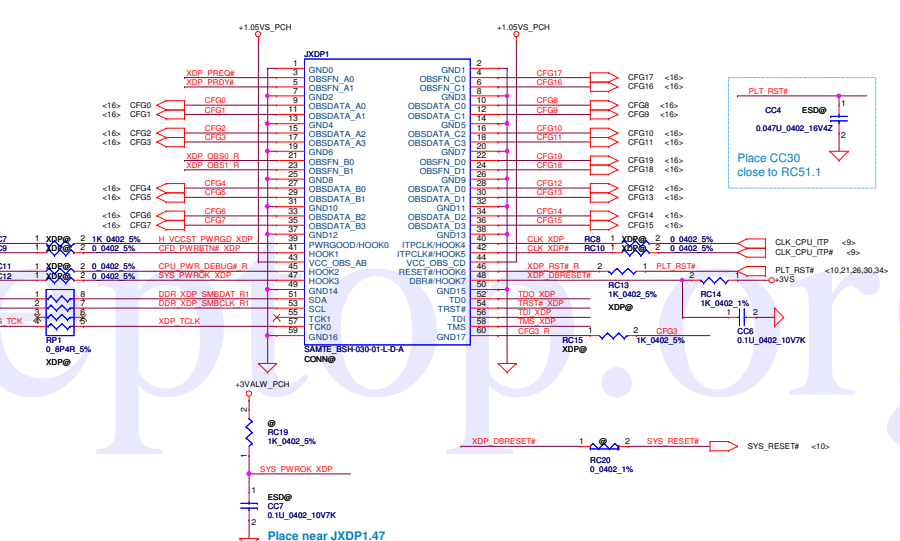
Broadwell



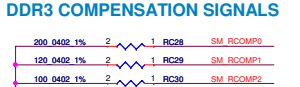
reference Shark Bay ULT Validation Customer Debug Port Implementation Requirement Rev 1.0



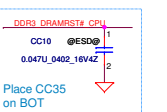
Place near JXD1



CAD Note: Avoid stubs in the PWRGD path while placing resistors RC115

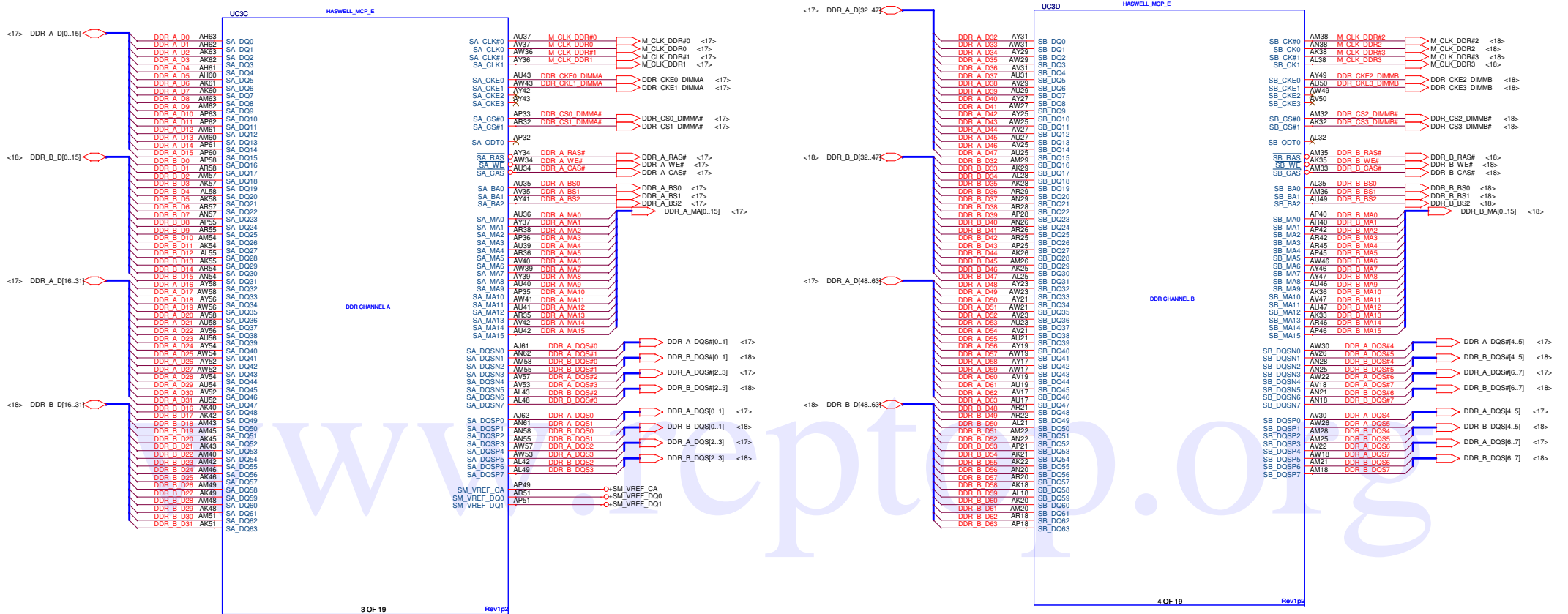


CAD Note: Trace width=12-15 mil, Spacing=20 mils, Max trace length=500 mil

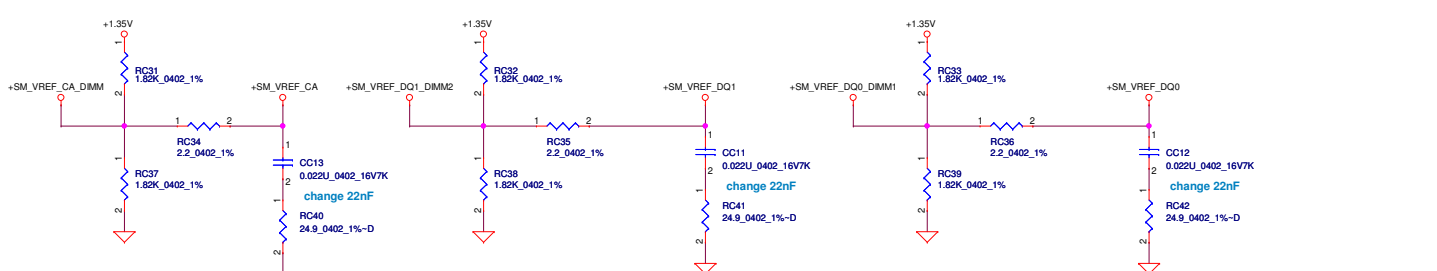


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# Interleaved Memory

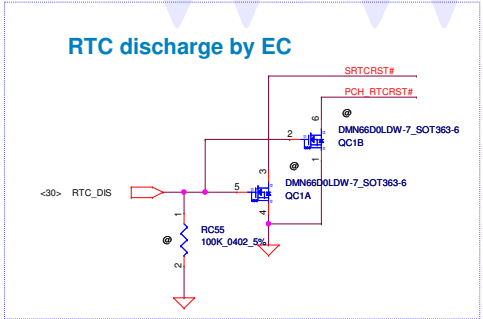
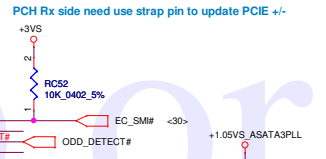
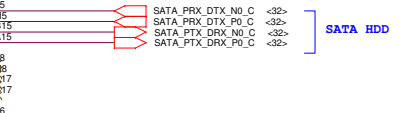
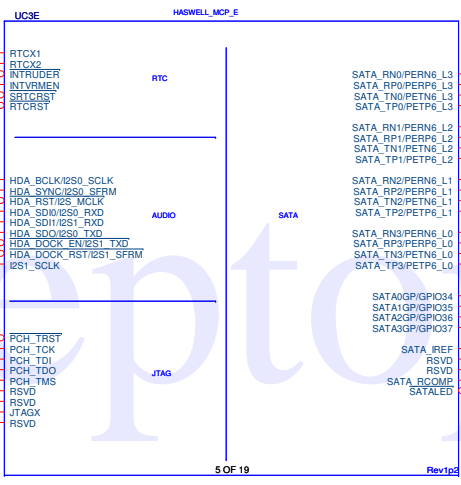
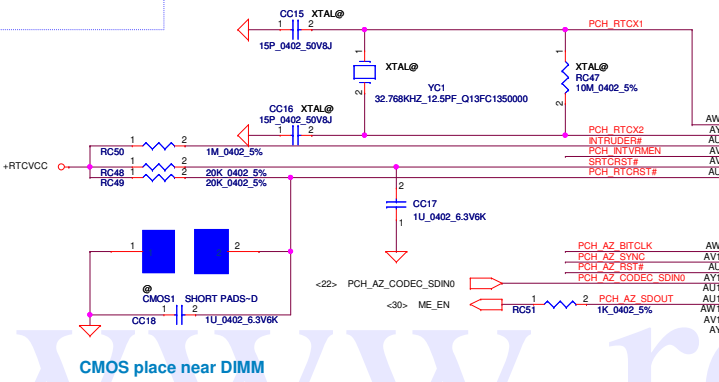
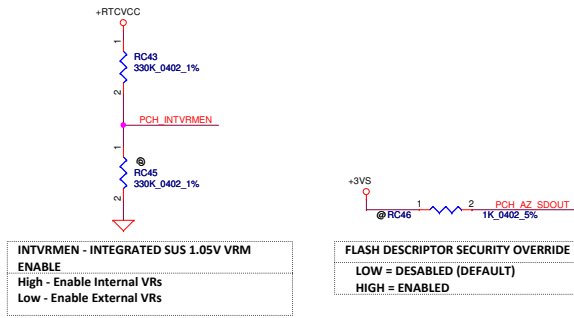
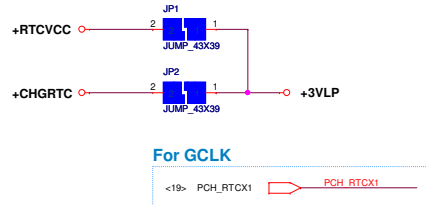
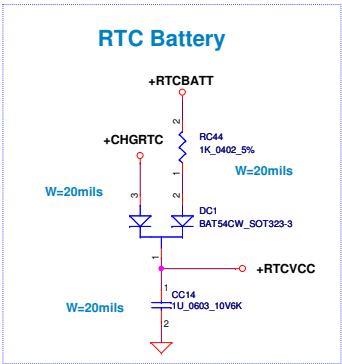


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confirm by intel request PDG P141

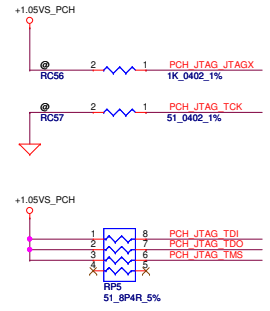
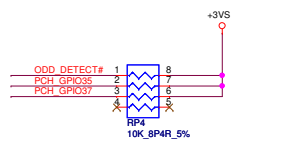
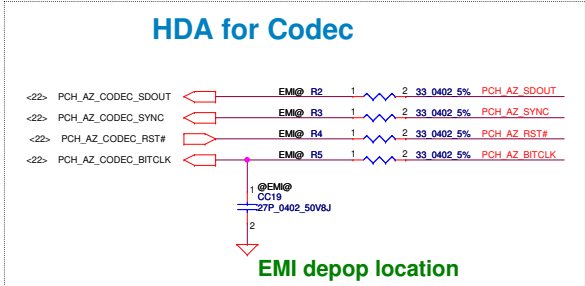
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| CMOS_CLR1 | CMOS setting |
|-----------|--------------|
| Shunt     | Clear CMOS   |
| Open      | Keep CMOS    |

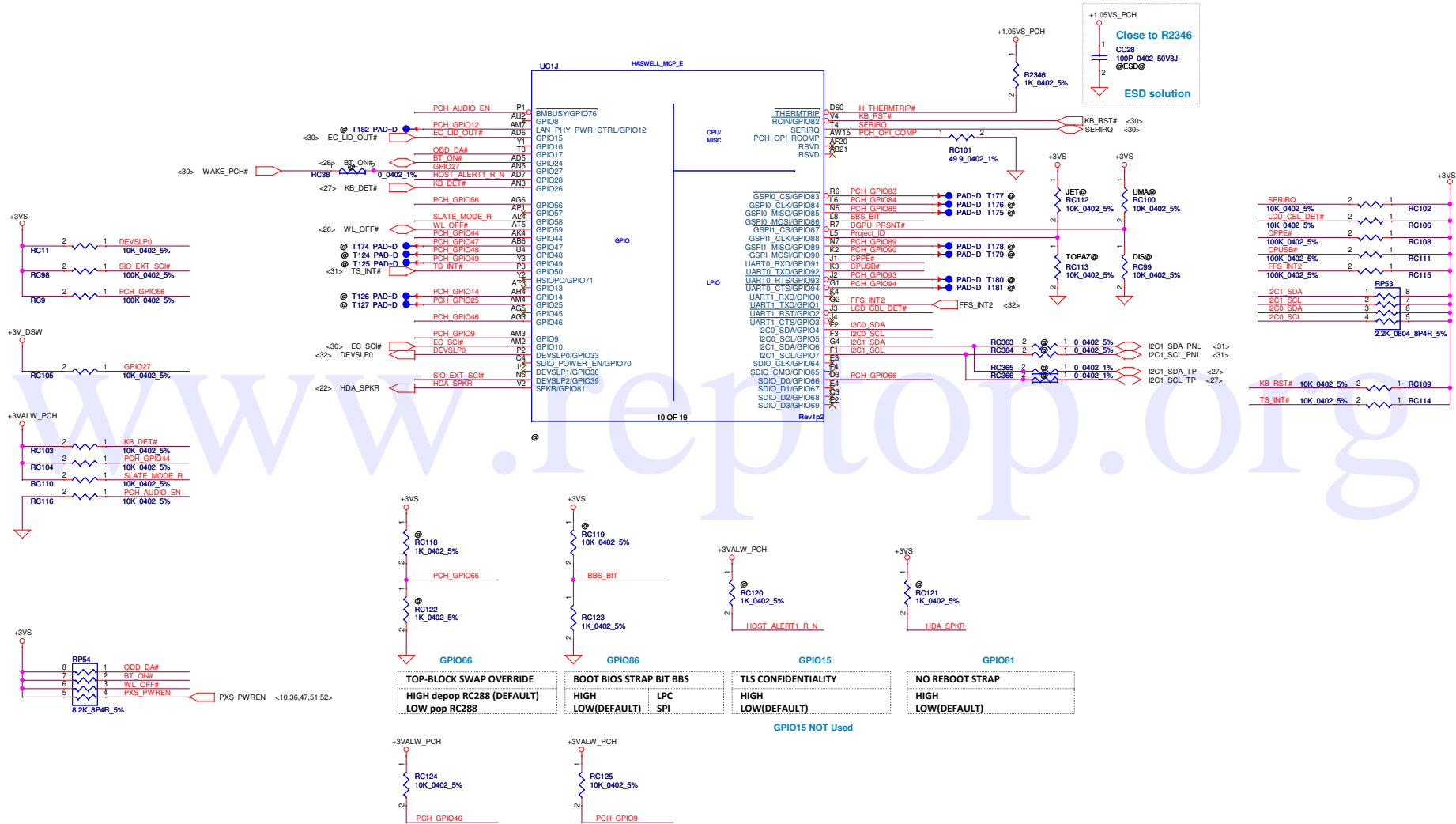
| ME_CLR1 | TPM setting            |
|---------|------------------------|
| Shunt   | Clear ME RTC Registers |
| Open    | Keep ME RTC Registers  |







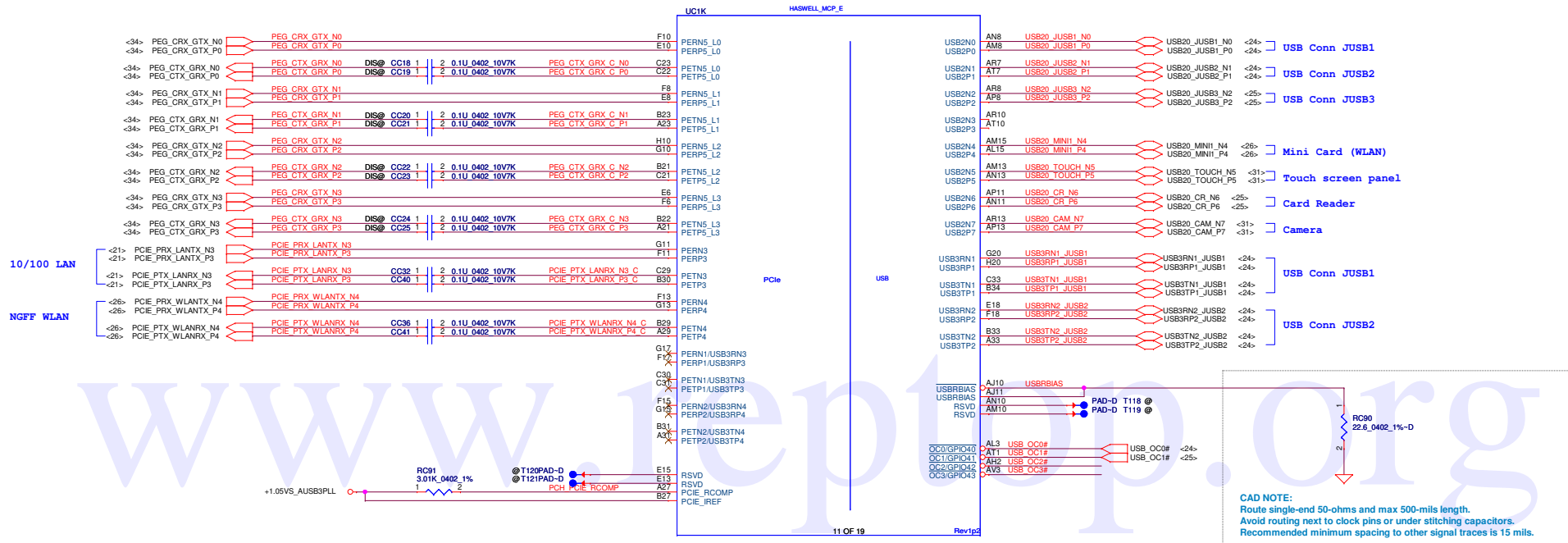




|   |  |   |   |
|---|--|---|---|
| <b>TOP-BLOCK SWAP OVERRIDE</b><br>HIGH depop RC288 (DEFAULT)<br>LOW pop RC288 | <b>BOOT BIOS STRAP BIT BBS</b><br>HIGH LOW(DEFAULT)<br>LPC SPI | <b>TLS CONFIDENTIALITY</b><br>HIGH LOW(DEFAULT) | <b>NO REBOOT STRAP</b><br>HIGH LOW(DEFAULT) |
|---|--|---|---|

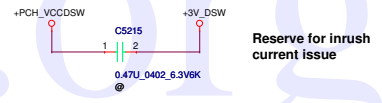
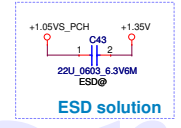
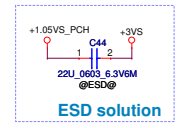
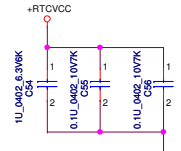
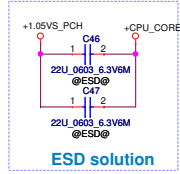
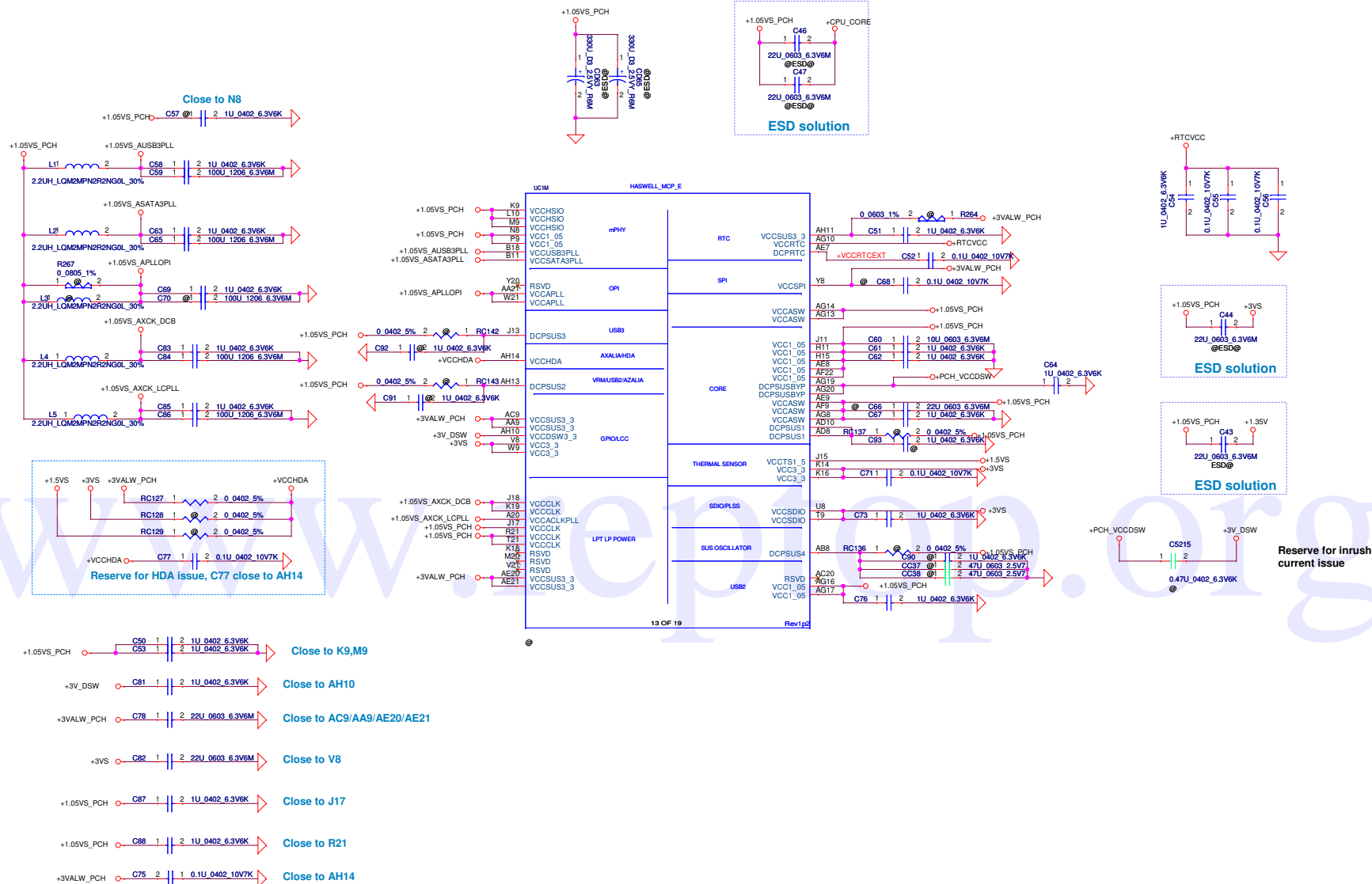
GPIO15 NOT USED



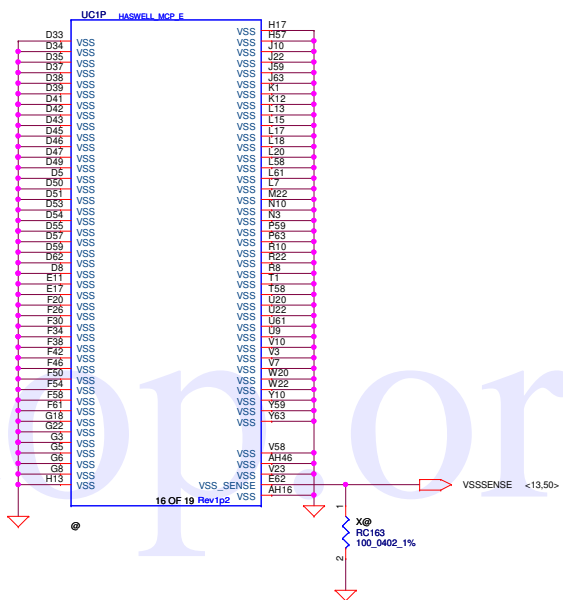
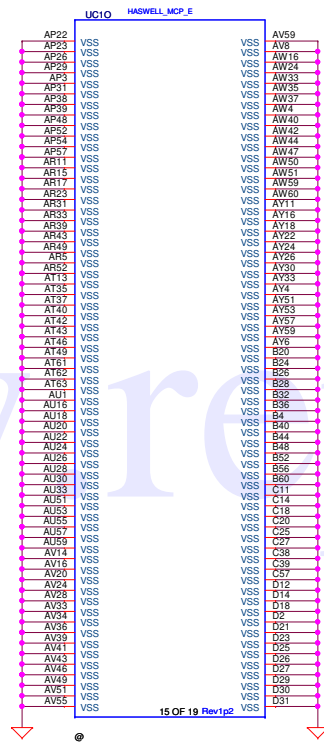
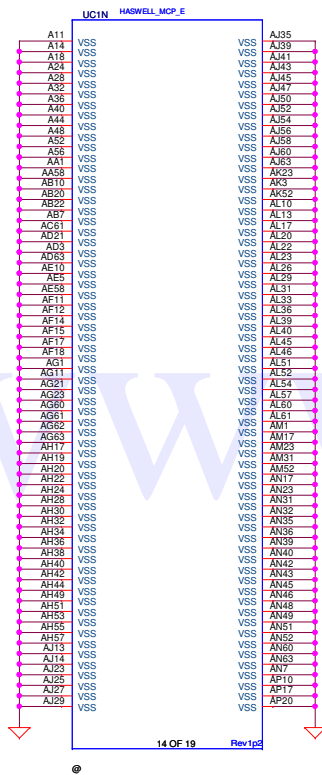


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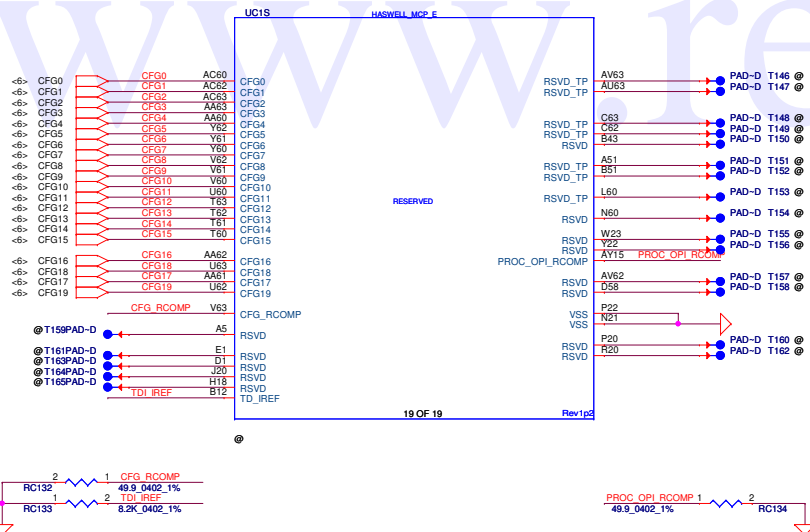
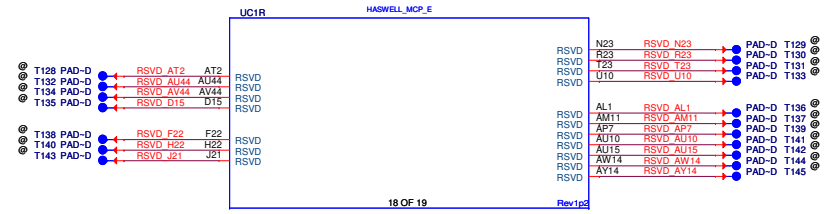
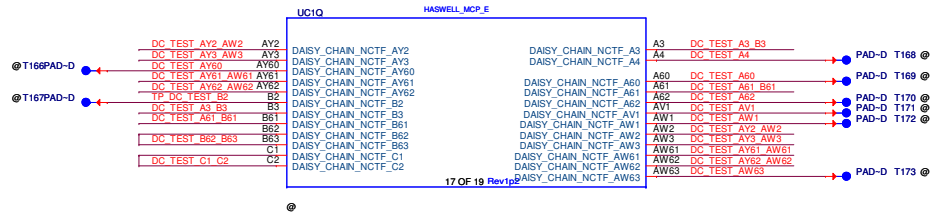


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|  |                    |                 |            | <b>MCP(13/19) Power</b>                         |
|  |                    |                 |            | LA-B012P  |
|  |                    |                 |            | Rev 1.0   |
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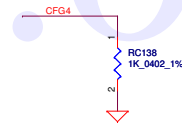


CAD Note: RC163 SHOULD BE PLACED CLOSE TO CPU

|  |                    |                 |            |  |
|--|--------------------|-----------------|------------|--|
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### CFG STRAPS for CPU



| Display Port Presence Strap |  |
|-----------------------------|--|
| CFG4                        | 1: Disabled; No Physical Display Port attached to Embedded Display Port<br>0: Enabled; An external Display Port device is connected to the Embedded Display Port |



H=4mm

Populate RD1, De-Populate RD7 for Intel DDR3 VREFDQ multiple methods M1  
Populate RD7, De-Populate RD1 for Intel DDR3 VREFDQ multiple methods M3

- <-> DDR\_A\_DQS[0..7]
- <-> DDR\_A\_D[0..63]
- <-> DDR\_A\_DQS[0..7]
- <-> DDR\_A\_MA[0..15]

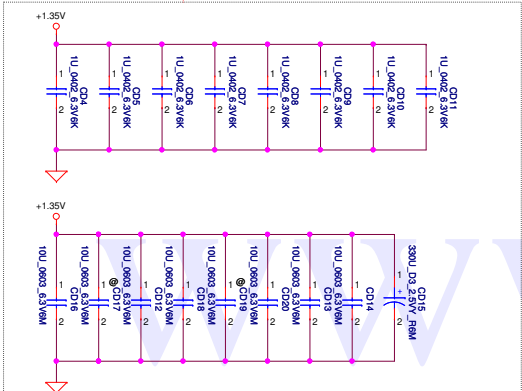
All VREF traces should have 10 mil trace width

Layout Note:  
Place near JDIMM1

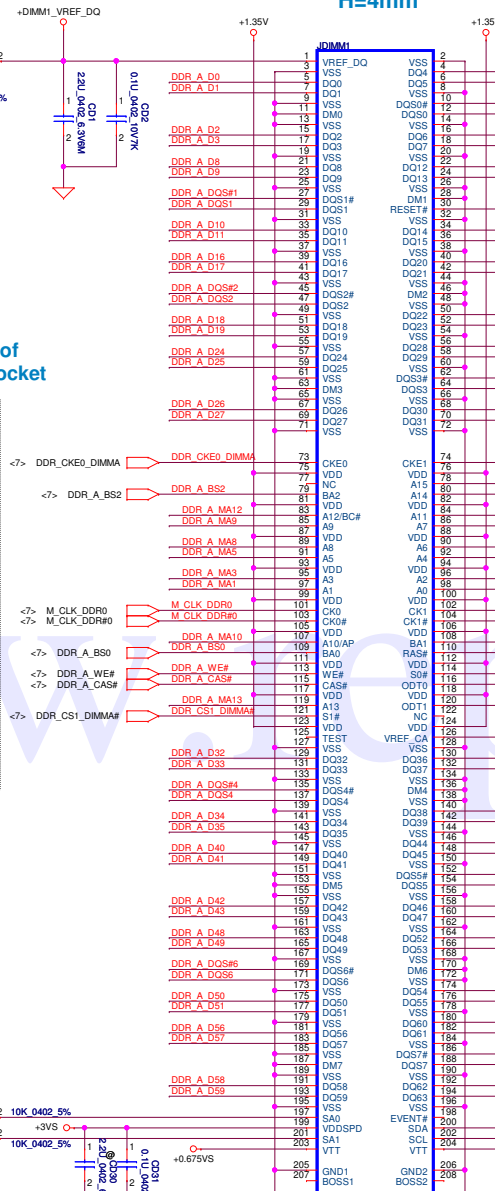
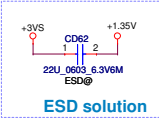
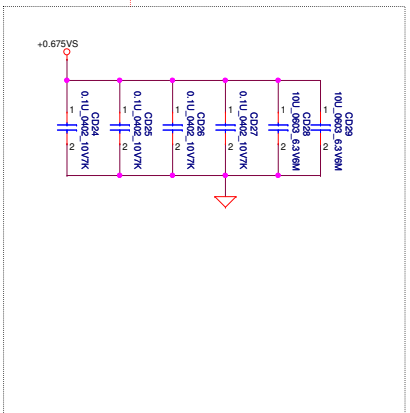
Note:  
Check voltage tolerance of VREF\_DQ at the DIMM socket

2-3A to 1 DIMMs/channel

CAD NOTE  
PLACE THE CAP NEAR TO DIMM RESET PIN



Layout Note:  
Place near JDIMM1. 203, 204



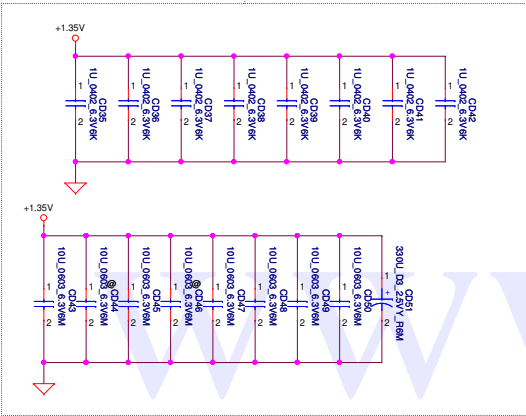
Populate RD4, De-Populate RD8 for Intel DDR3  
VREFDQ multiple methods M1  
Populate RD8, De-Populate RD4 for Intel DDR3  
VREFDQ multiple methods M3

- <-> DDR\_B\_DQS#(0..7)
- <-> DDR\_B\_D(0..63)
- <-> DDR\_B\_DQS(0..7)
- <-> DDR\_B\_MA(0..15)

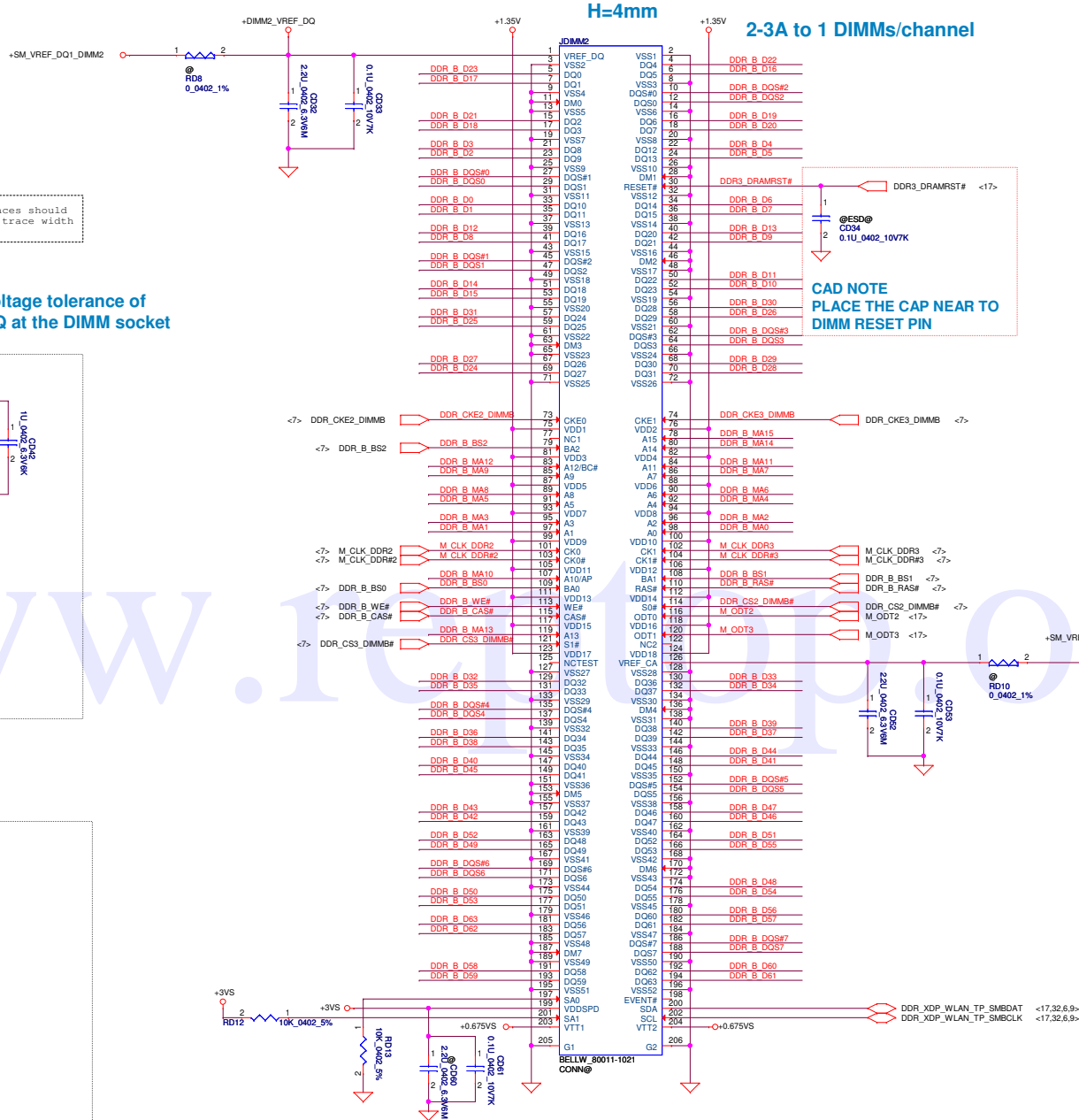
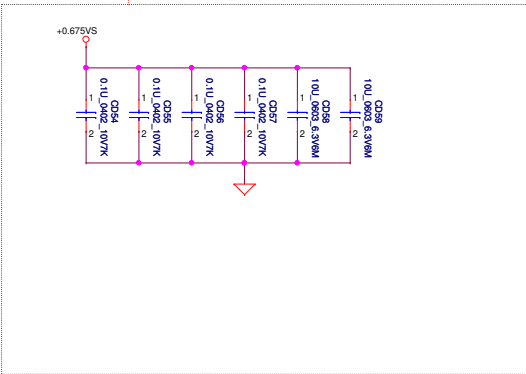
All VREF traces should have 10 mil trace width

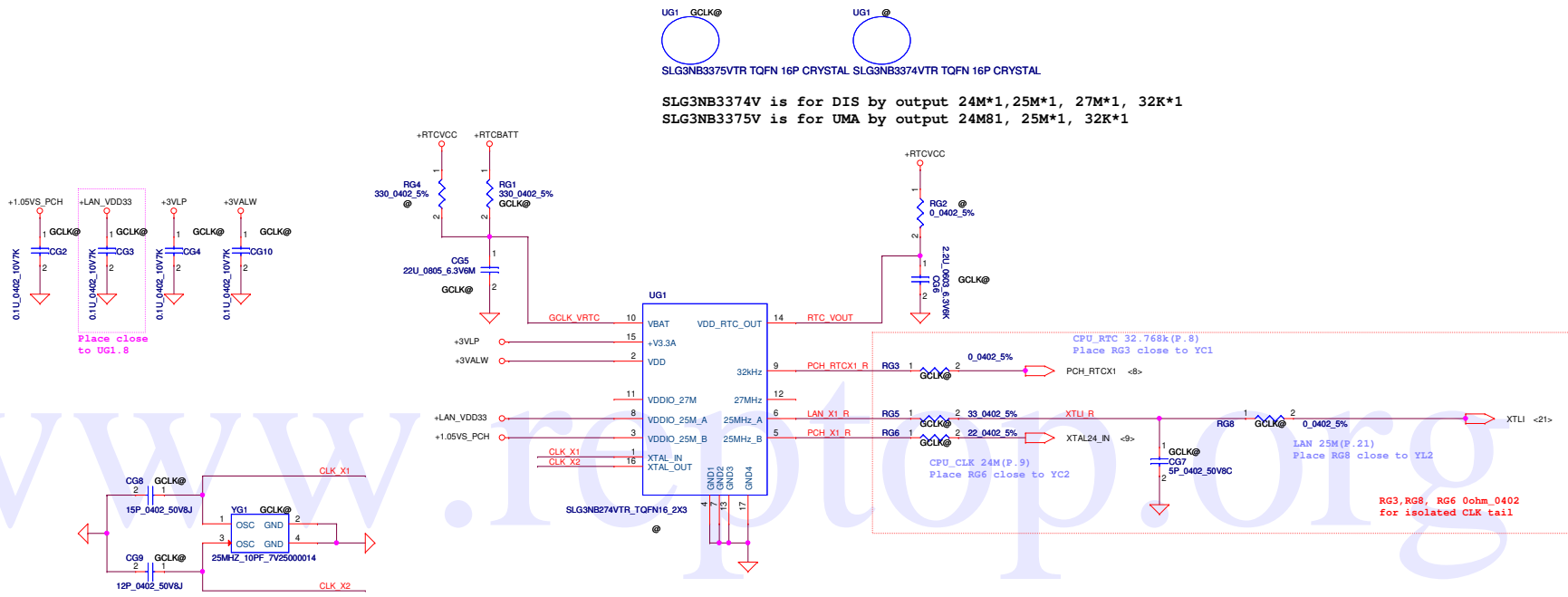
Layout Note:  
Place near JDIMM2

Note:  
Check voltage tolerance of VREF\_DQ at the DIMM socket



Layout Note:  
Place near JDIMM2.203,204



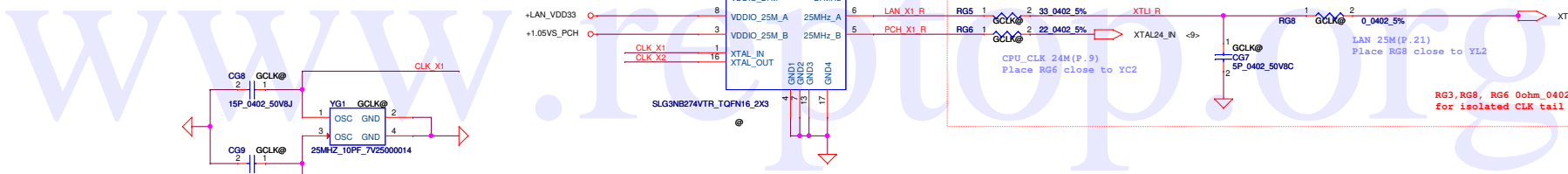


UG1 GCLK@

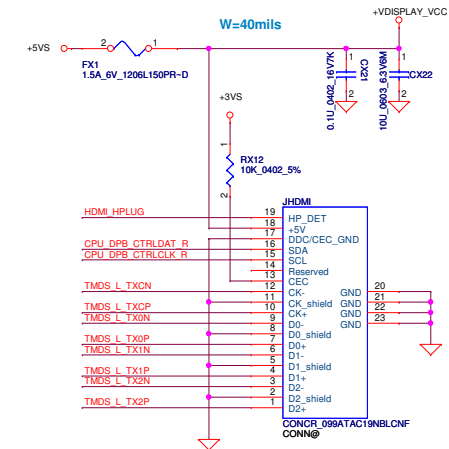
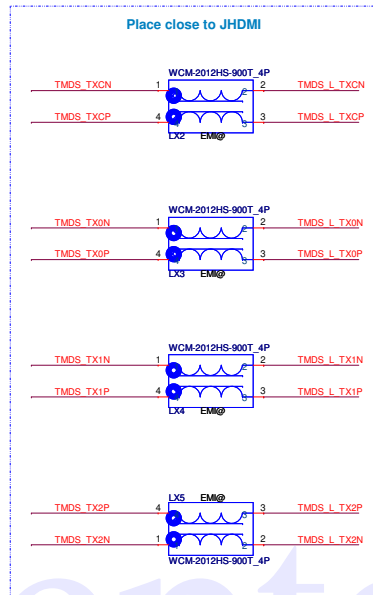
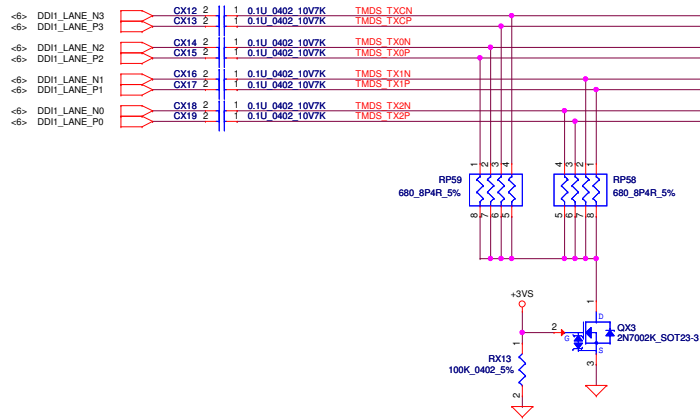
UG1 @

SLG3NB3375VTR TQFN 16P CRYSTAL SLG3NB3374VTR TQFN 16P CRYSTAL

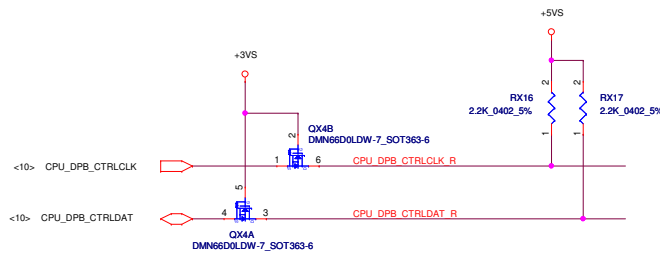
SLG3NB3374V is for DIS by output 24M\*1, 25M\*1, 27M\*1, 32K\*1  
 SLG3NB3375V is for UMA by output 24M81, 25M\*1, 32K\*1



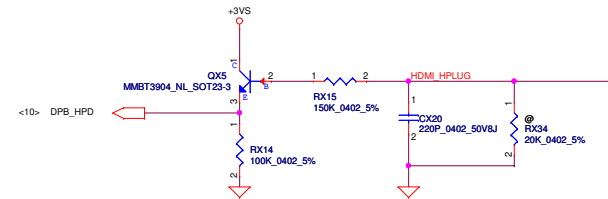
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| Date: Tuesday, August 05, 2014   |                    |                 |            | Rev<br>1.0                         |
| Sheet 19 of 55   |                    |                 |            |                                    |



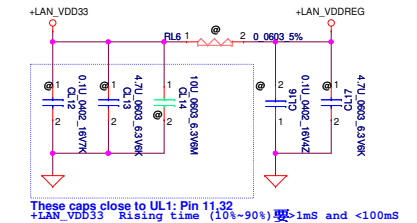
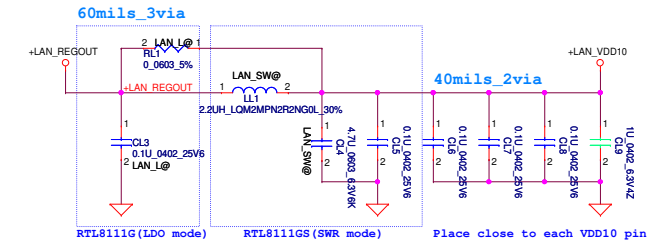
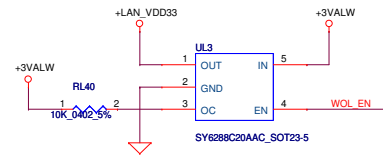
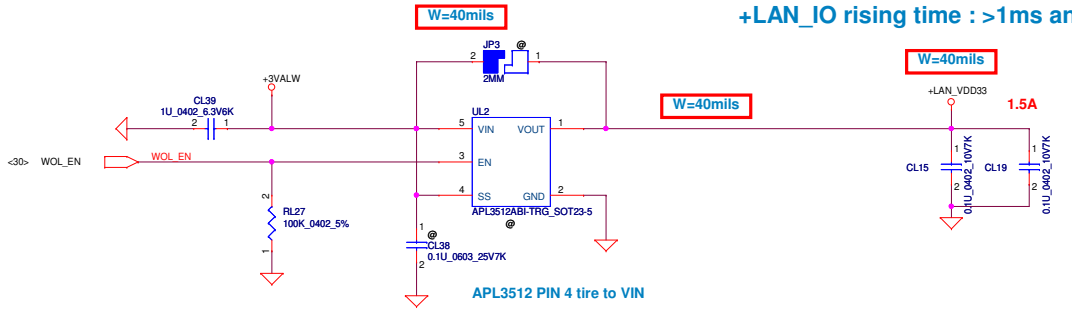
| 46@ ROYALTY HDMI W/LOGO |                         |
|-------------------------|-------------------------|
| Part Number             | Description             |
| R000000022HM            | HDMI W/Logo:R00000022HM |



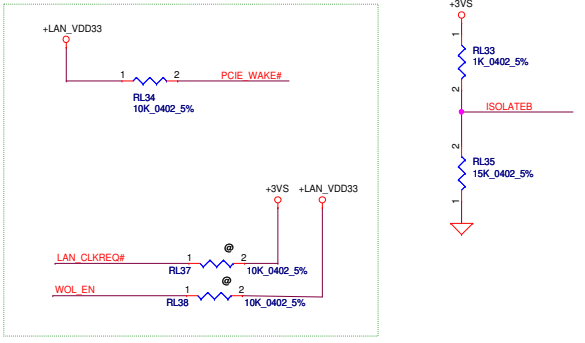
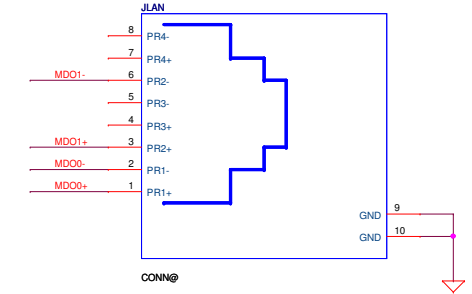
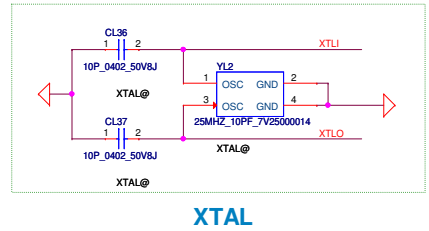
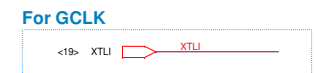
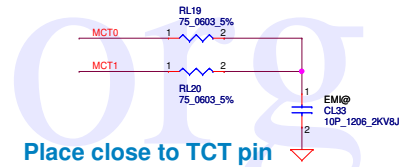
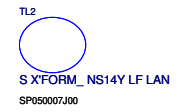
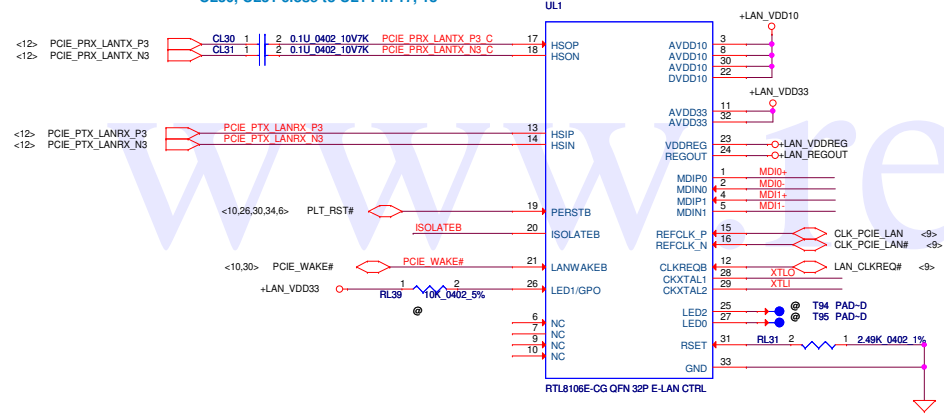
|             |      |      |   |   |                 |
|-------------|------|------|---|---|-----------------|
| TMD5_L_TXCN | @EM@ | CX23 | 1 | 2 | 3.3P_0402_50V8C |
| TMD5_L_TXCP | @EM@ | CX24 | 1 | 2 | 3.3P_0402_50V8C |
| TMD5_L_TXIN | @EM@ | CX25 | 1 | 2 | 3.3P_0402_50V8C |
| TMD5_L_TXOP | @EM@ | CX26 | 1 | 2 | 3.3P_0402_50V8C |
| TMD5_L_TXIN | @EM@ | CX27 | 1 | 2 | 3.3P_0402_50V8C |
| TMD5_L_TX1P | @EM@ | CX28 | 1 | 2 | 3.3P_0402_50V8C |
| TMD5_L_TX2N | @EM@ | CX29 | 1 | 2 | 3.3P_0402_50V8C |
| TMD5_L_TX2P | @EM@ | CX30 | 1 | 2 | 3.3P_0402_50V8C |



**+LAN\_IO rising time : >1ms and <100ms**



**CL30, CL31 close to UL1 Pin 17, 18**



**Reserve 10K pull LAN\_IO**

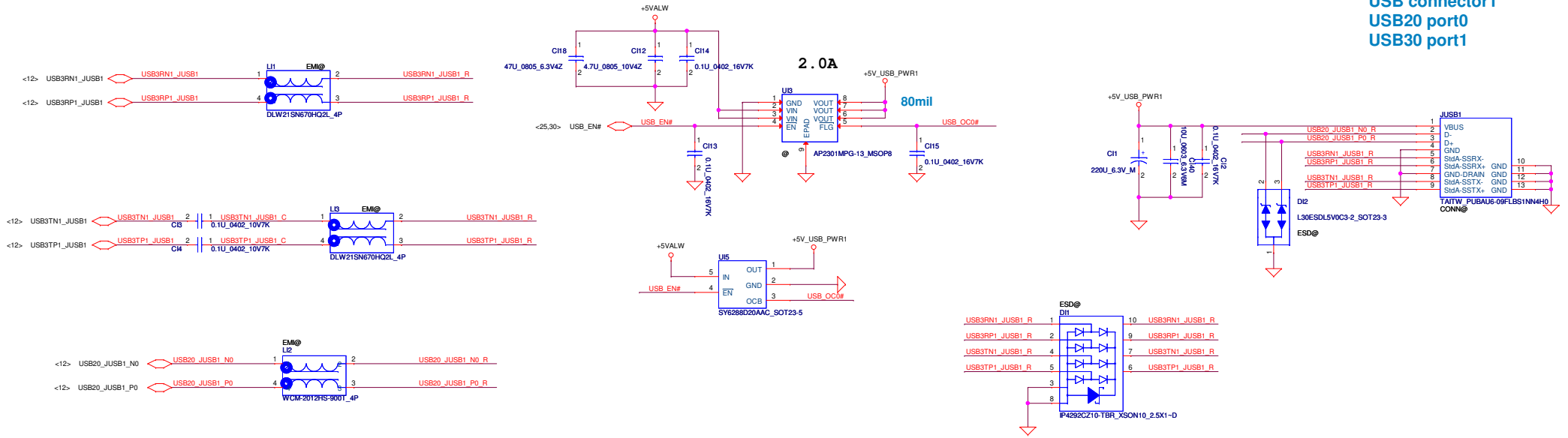
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| S220  | Custom                   | Document Number | LA-B012P   | Rev 1.0        |
| Date:   | Tuesday, August 05, 2014 | Sheet           | 21         | of 55          |



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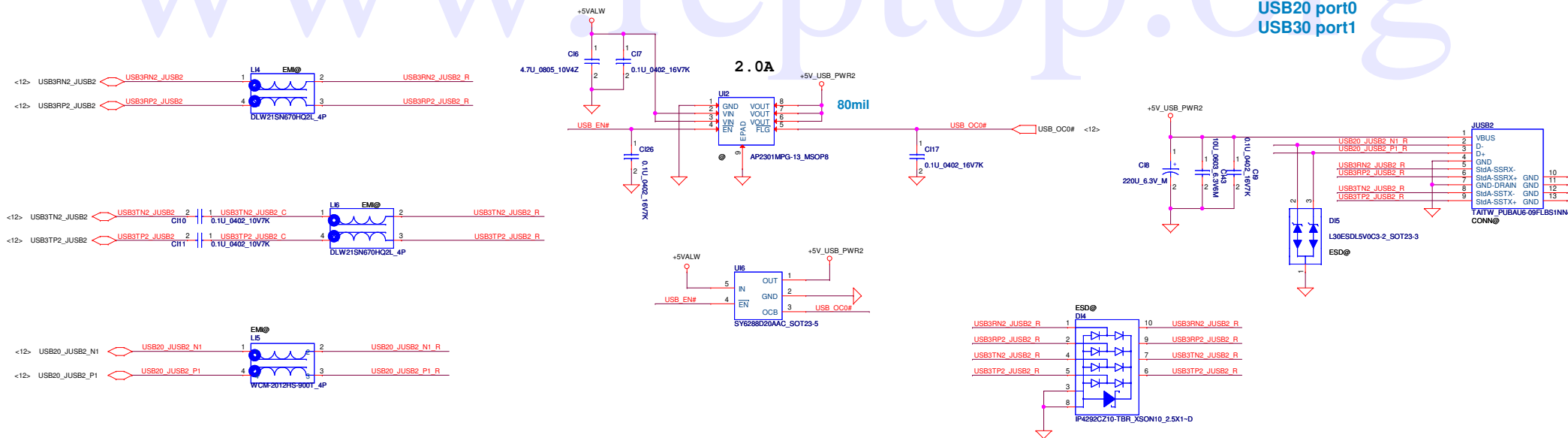
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|   |                    |                 | Date:           | Tuesday, August 05, 2014        | Sheet 23 of 55 |

USB connector1  
USB20 port0  
USB30 port1



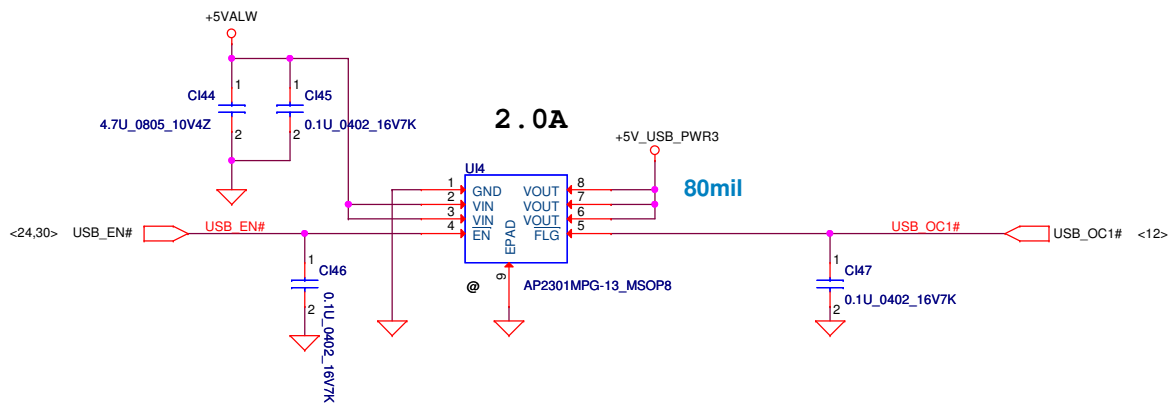
www.reptop.org

USB connector2  
USB20 port0  
USB30 port1

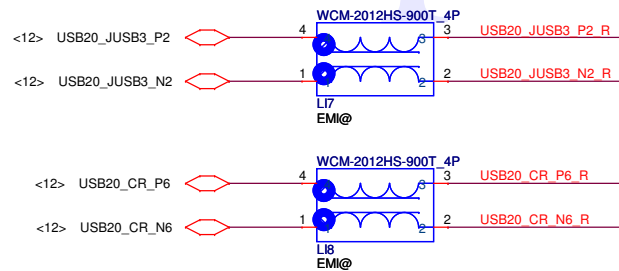
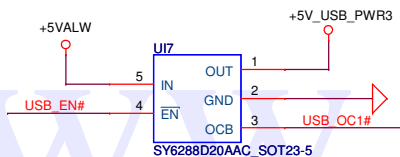
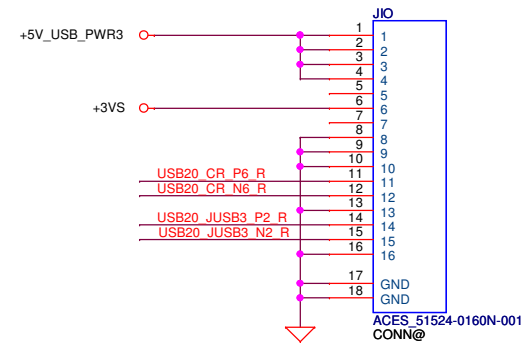


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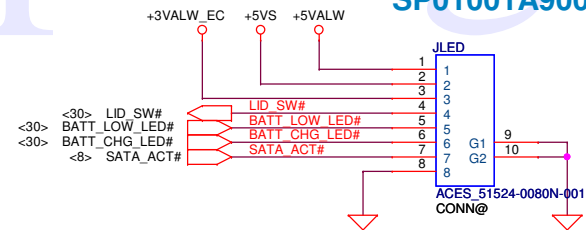




### IO to MB CONN Substitute:SP01001FS00



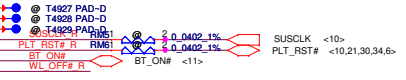
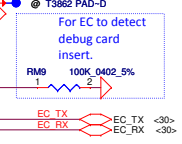
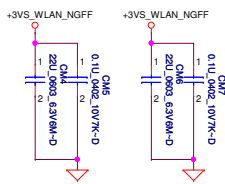
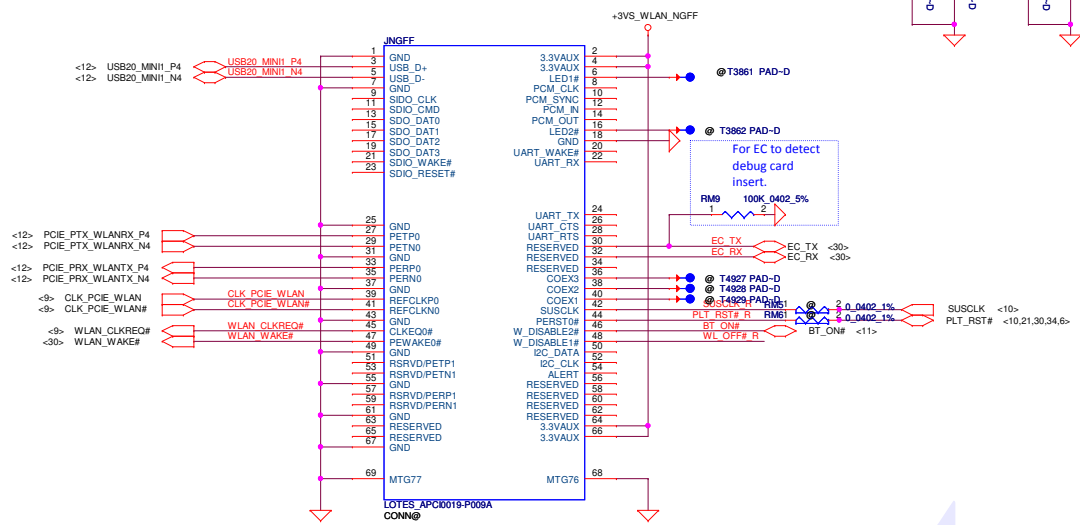
### LED/B TO M/B SP01001A900



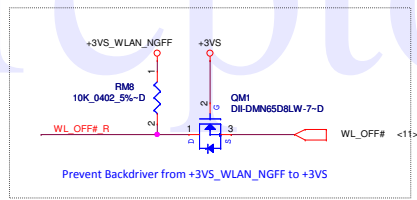
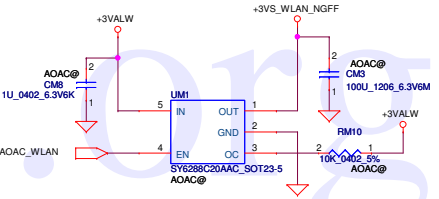
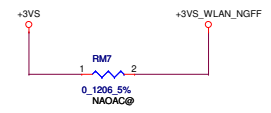
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| Security Classification   | Compal Secret Data |                 |            | Title           | <b>IO/B, LED/B</b>       |
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|   |                    |                 |            | Sheet           | 25 of 55                 |
|   |                    |                 |            | Rev             | 1.0                      |

# NGFF WL Con (E Key)

closed to pin 2, 4      closed to pin 64, 66



## +3VALW TO +3V\_WLAN\_NGFF

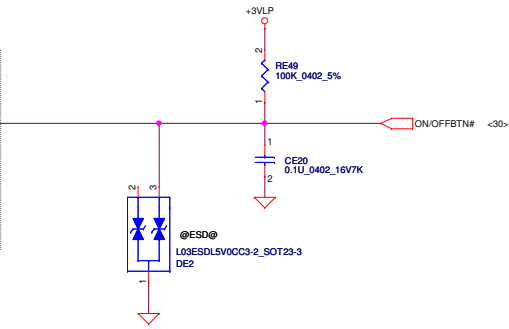
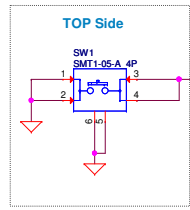


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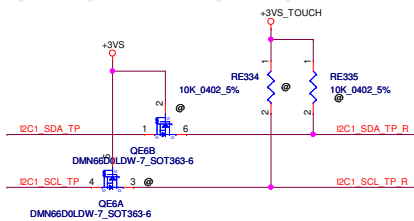
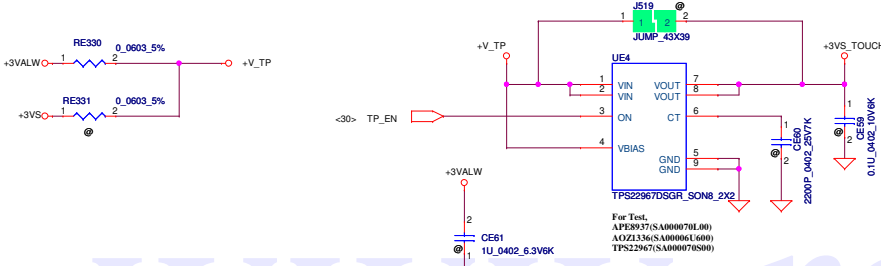
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| Date: Tuesday, August 05, 2014  |                    |                 |            | Rev<br>1.0                         |
| Sheet 26 of 55  |                    |                 |            |                                    |

# Power ON Circuit

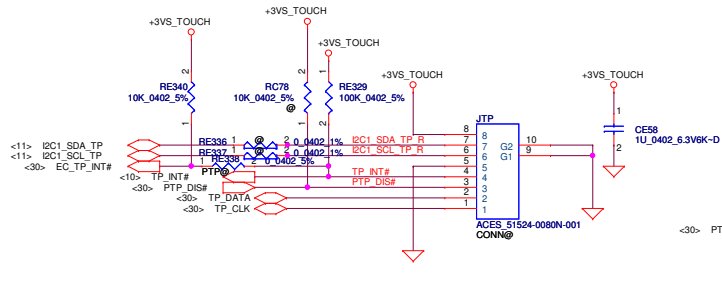
## ON/OFF switch



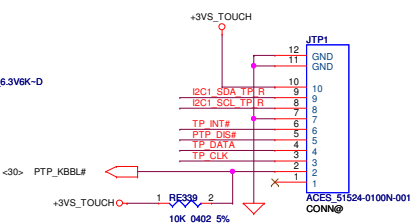
## J519 short



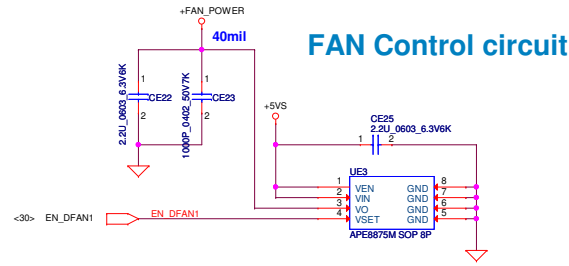
## Touch pad



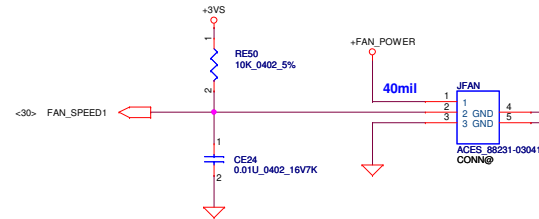
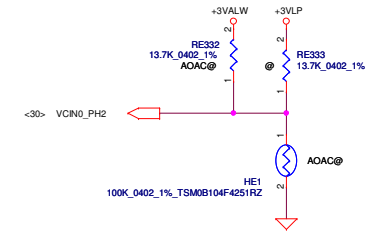
## PTP



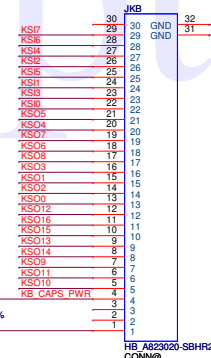
# FAN Control circuit



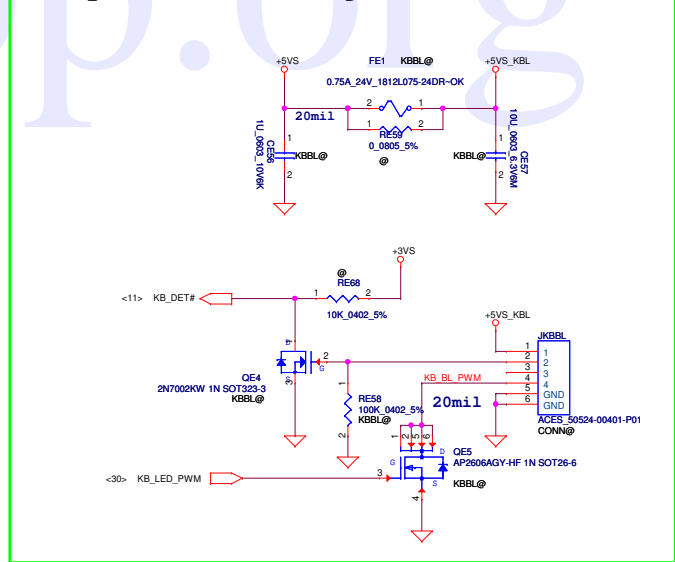
HE1 place around FAN area.



# INT\_KBD Connector

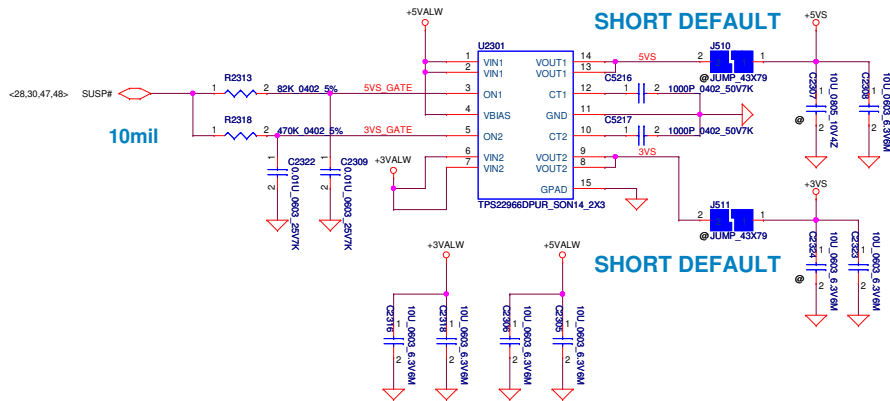


# \* Key Board Back Light

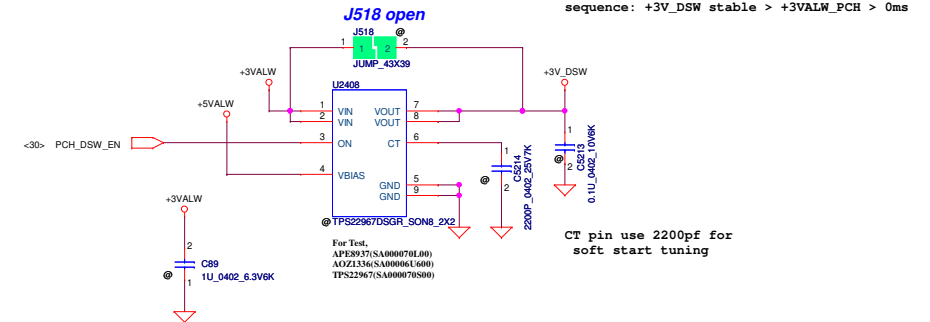


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|   |                    |                 |            | Date:                           | Sheet    |
|   |                    |                 |            | Tuesdays, August 05, 2014       | 27 of 55 |

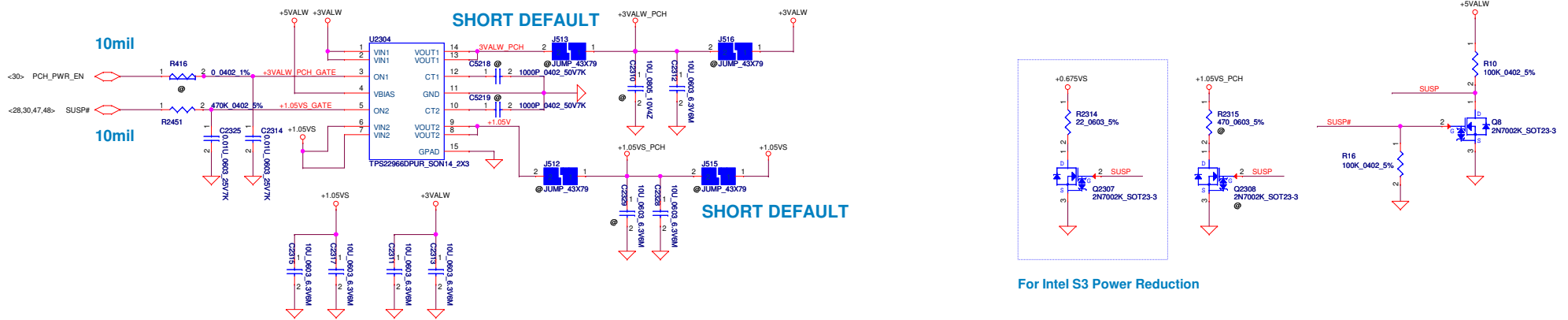
## +5VS and +3VS switch



## +3VALW TO +3V\_DSW



## +3VALW\_PCH switch

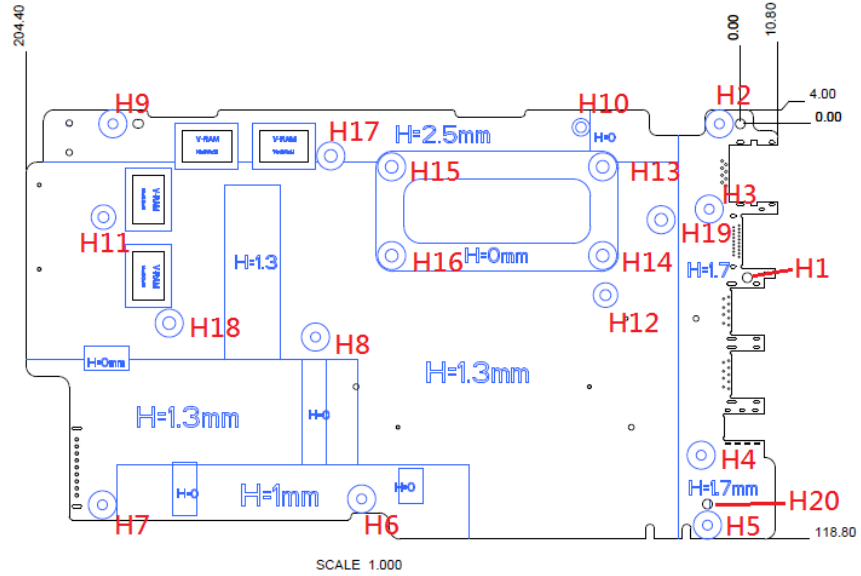
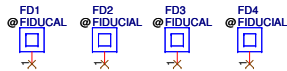
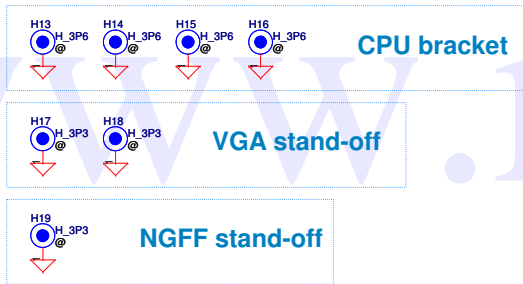
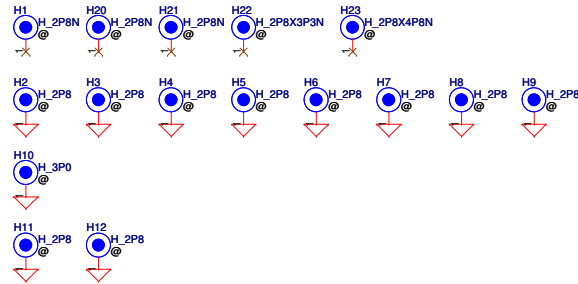


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|  |                    |                 |            |                 |
|--|--------------------|-----------------|------------|-----------------|
| Security Classification  | Compal Secret Data |                 | Title      |                 |
| Issued Date  | 2014/01/20         | Deciphered Date | 2015/01/19 | DC/DC Interface |
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| Date: Tuesday, August 05, 2014   |                    |                 |            | Sheet 28 of 55  |

# Screw Hole

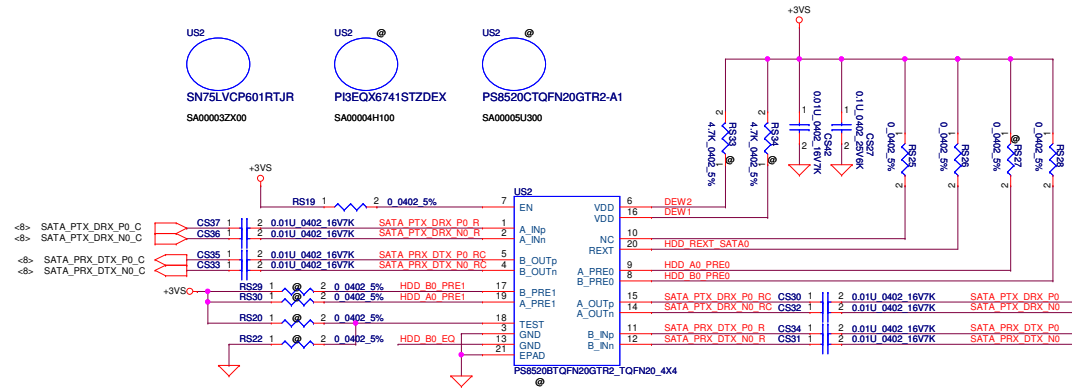
ZZZ  
 PCB 13P LA-B011P REV0 M/B  
 DA60013U000



|   |                    |                 |                                |                                 |          |
|---|--------------------|-----------------|--------------------------------|---------------------------------|----------|
| Security Classification   | Compal Secret Data |                 | Title                          | <b>Compal Electronics, Inc.</b> |          |
| Issued Date   | 2014/01/20         | Deciphered Date | 2015/01/19                     | Screw Hole                      |          |
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|   |                    |                 | Date: Tuesday, August 05, 2014 | Sheet                           | 29 of 55 |







Pin 20:  
PARADE PS8250B:  
Depop RS26

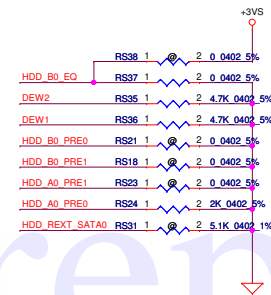
PERICOM PI3EQX6741ST:  
Pop RS26

ASMEDIA ASM1466:  
Pop RS26

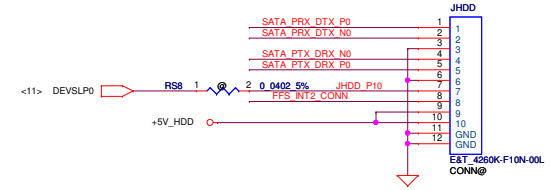
Pin 9:  
PARADE PS8250B:  
Depop RS24.

PERICOM PI3EQX6741ST:  
Depop RS24

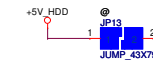
ASMEDIA ASM1466:  
Pop RS24 to pull down



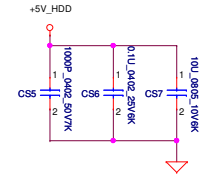
### SATA HDD Connector



### +5V\_HDD Source

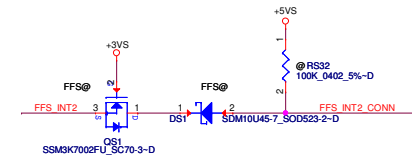
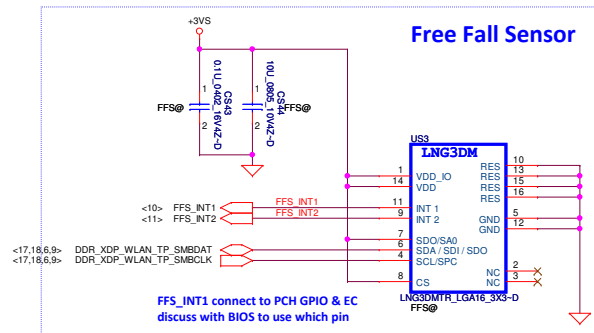


### SHORT DEFAULT



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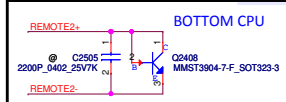
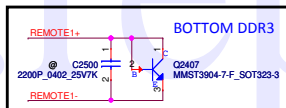
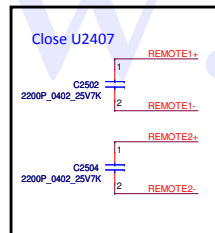
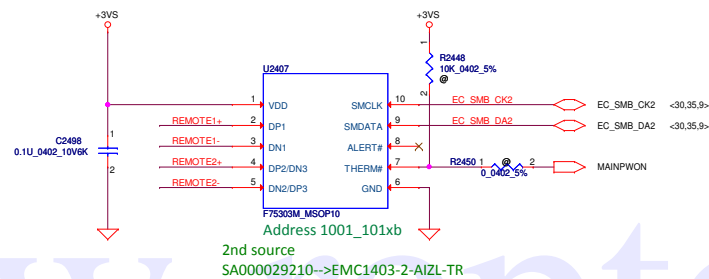
### Free Fall Sensor



|  |                    |                 |            |   |
|--|--------------------|-----------------|------------|---|
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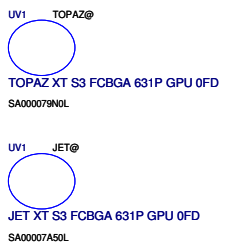
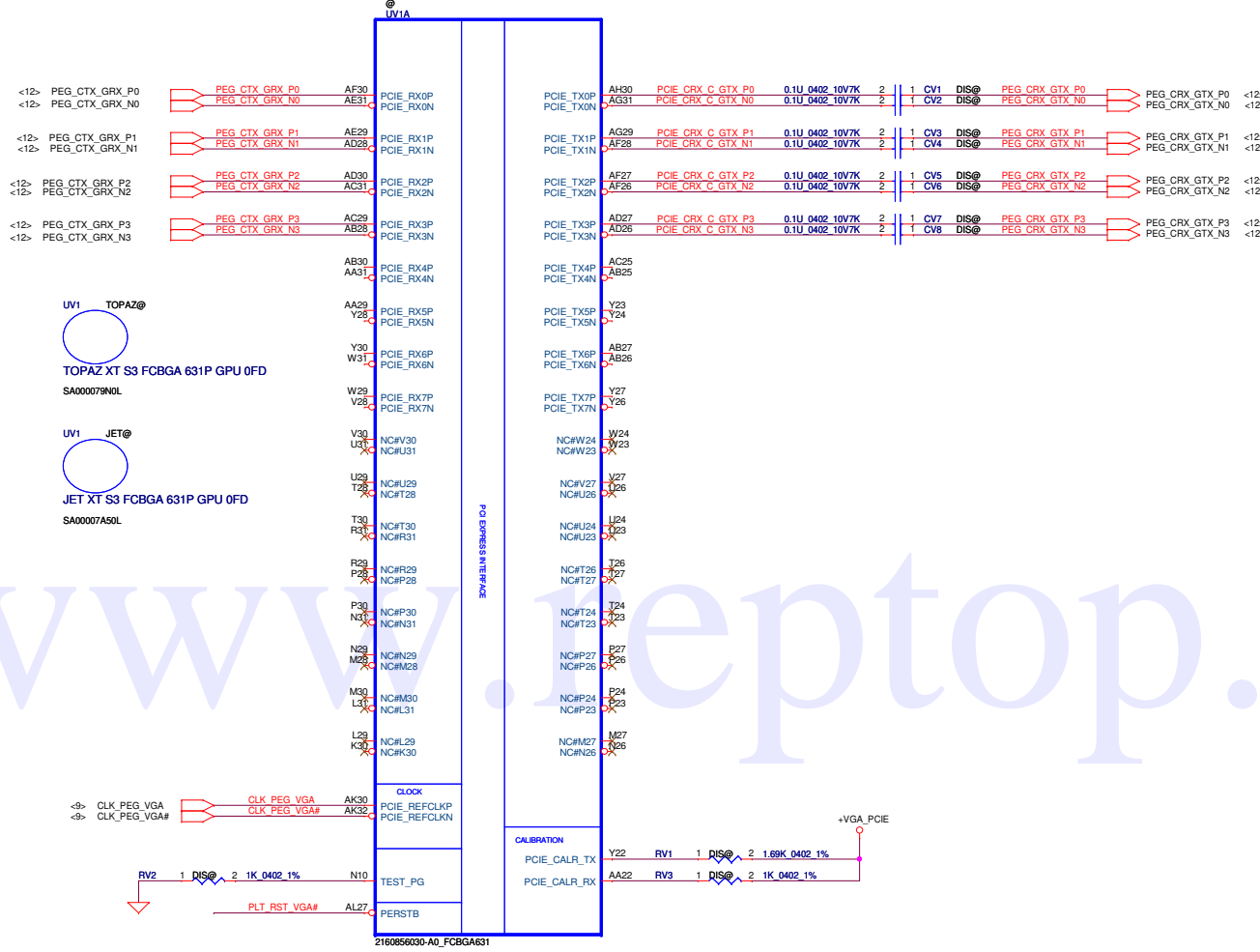


**Fintek thermal sensor  
placed near by TOP DDR3**

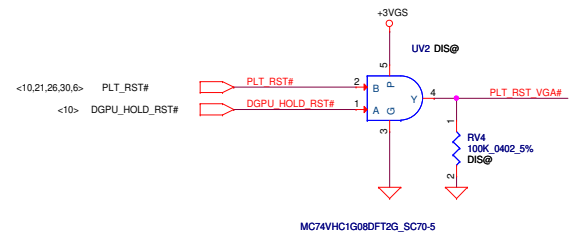
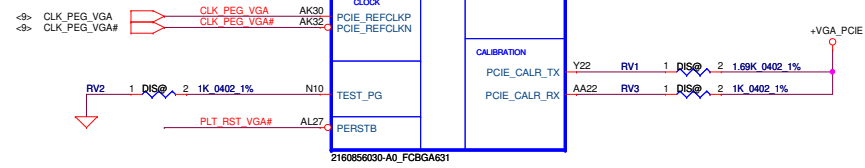
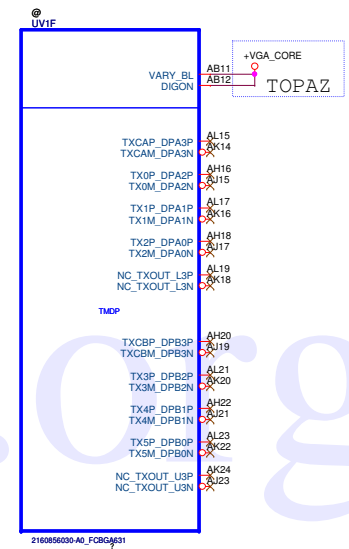


REMOTE1,2 (+/-) :  
Trace width/space:10/10 mil  
Trace length:<8"

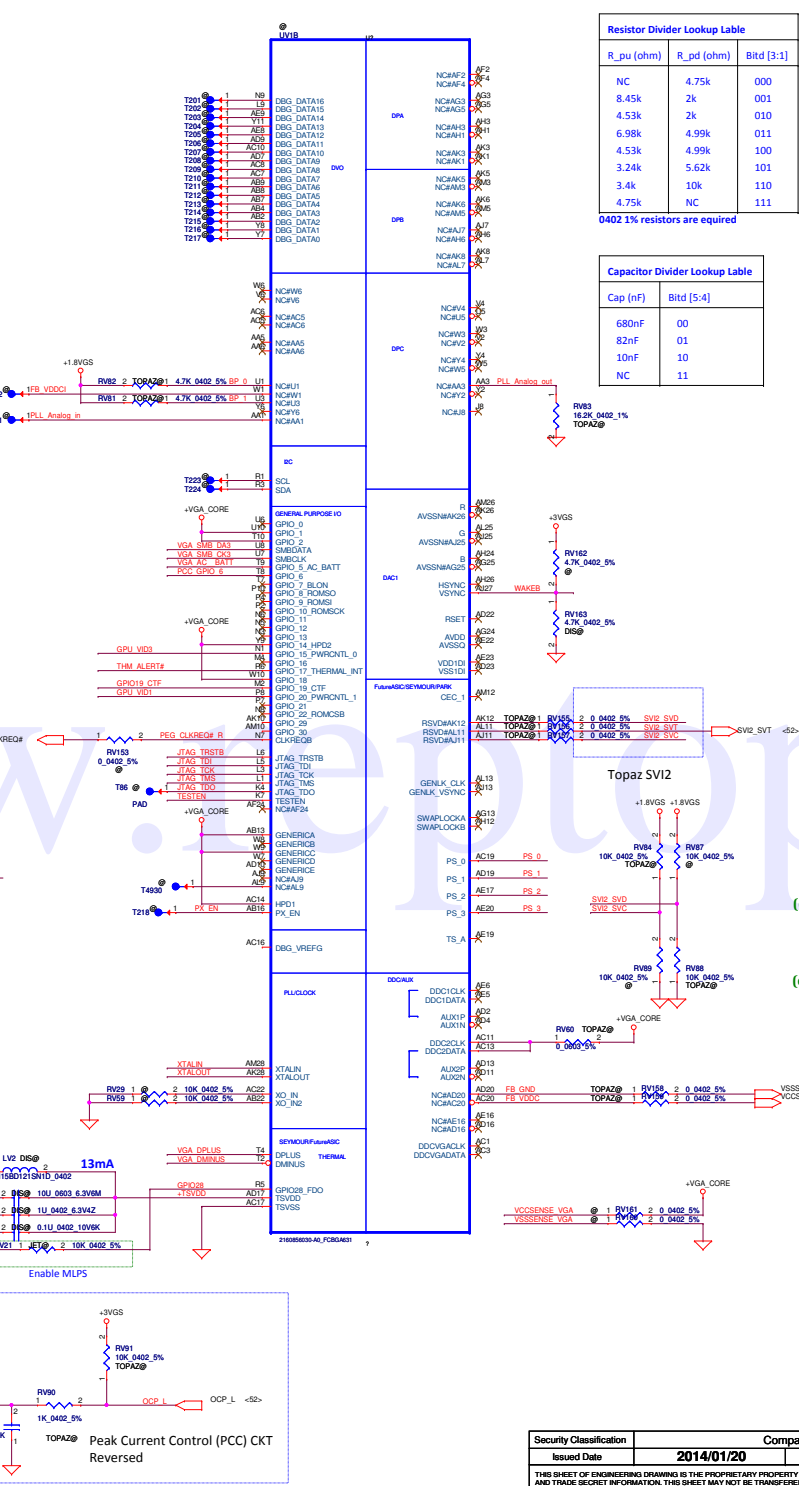
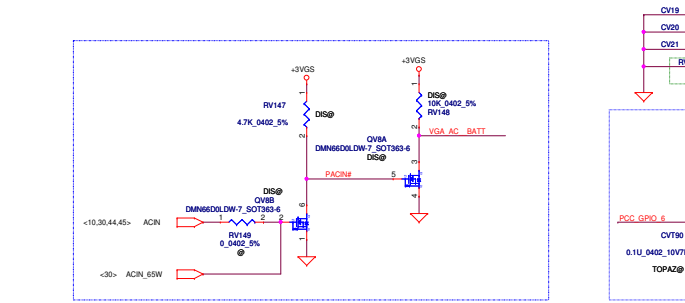
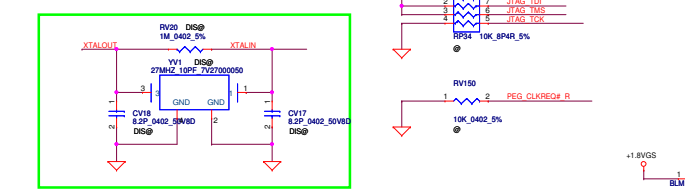
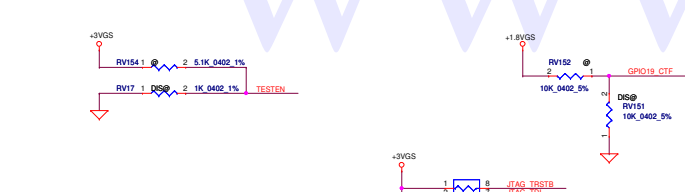
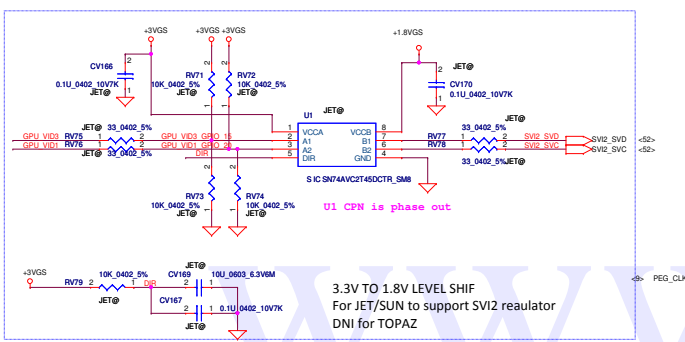
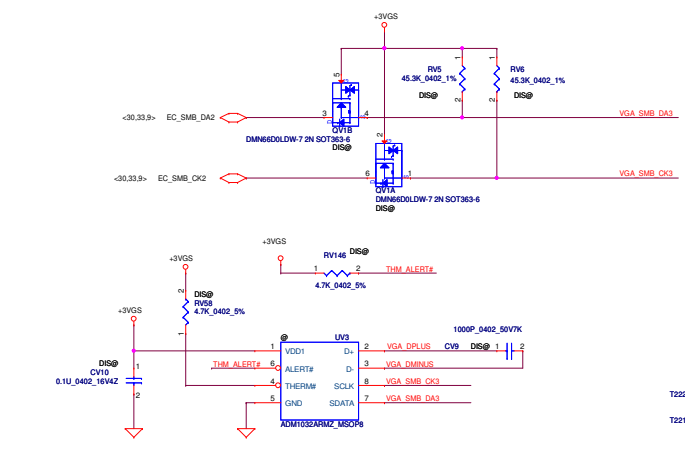
|  |                    |                 |                          |  |
|--|--------------------|-----------------|--------------------------|--|
| Security Classification  | Compal Secret Data |                 | Compal Electronics, Inc. |  |
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|  |                    |                 |                          | Rev<br>1.0<br>Sheet 33 of 55   |



No Use GPU Display Port output



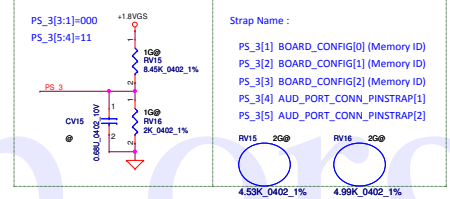
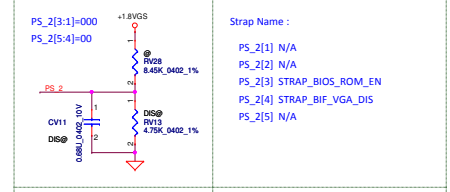
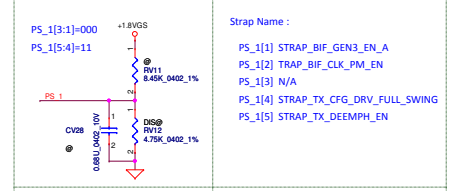
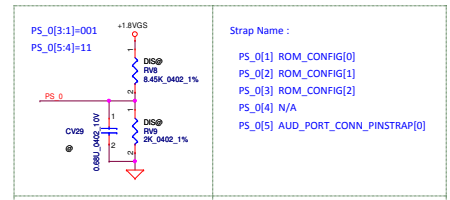
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|---|------------|--------------------|------------|-----------------|--|--------------------------|--|
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| Date: Tuesday, August 05, 2014  |            |                    |            | Sheet           |  | 34 of 55                 |  |



| R_pu (ohm) | R_pd (ohm) | Bitd [3:1] |
|------------|------------|------------|
| NC         | 4.75k      | 000        |
| 8.45k      | 2k         | 001        |
| 4.53k      | 2k         | 010        |
| 6.98k      | 4.99k      | 011        |
| 4.53k      | 4.99k      | 100        |
| 3.24k      | 5.62k      | 101        |
| 3.4k       | 10k        | 110        |
| 4.75k      | NC         | 111        |

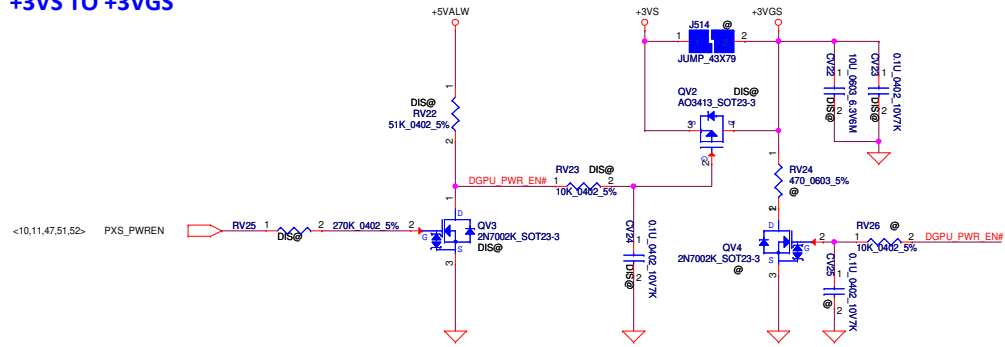
0402 1% resistors are required

| Cap (nF) | Bitd [5:4] |
|----------|------------|
| 680nF    | 00         |
| 82nF     | 01         |
| 10nF     | 10         |
| NC       | 11         |



| Memory ID     | P/N         | Vendor  | Configuration      | Size |
|---------------|-------------|---------|--------------------|------|
| (default) 000 | SA000068U0L | SAMSUNG | K4W2G1644G-BC1A    | 1GB  |
| 001           | SA00006H40L | HYNIX   | H5TC2G63FFR-11C    | 1GB  |
| 010           | SA00006750L | Micron  | MT41J128M16JT-093G | 1GB  |
| 011           | SA000076P0L | SAMSUNG | K4W4G1646B-HC11    | 2GB  |
| (default) 100 | SA00006E80L | HYNIX   | H5TC4G63AFR-11C    | 2GB  |
| 101           | SA000077K0L | Micron  | MT41J256M16HA-093G | 2GB  |

**+3VS TO +3VGS**

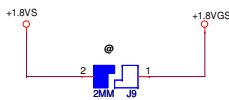


**+1.35VS\_VGA TO +1.35V\_MEM\_GFX**

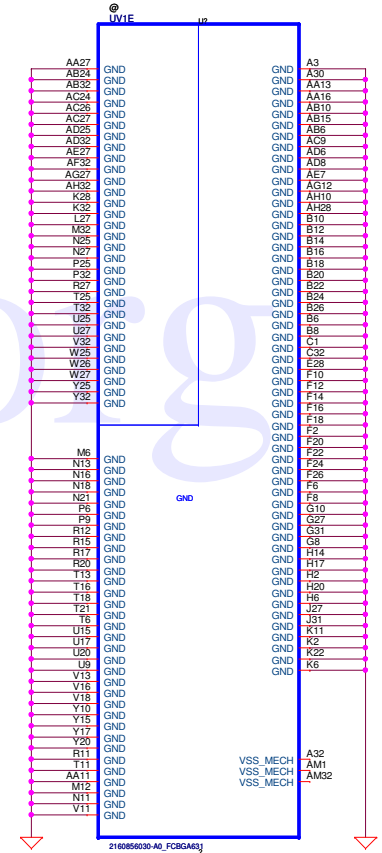
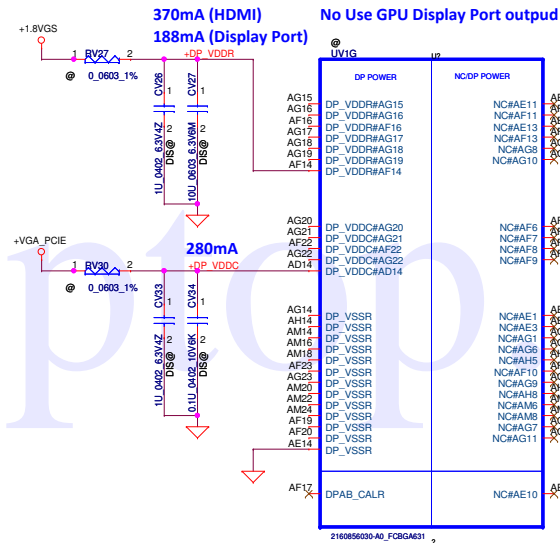


SHORT DEFAULT

**+1.8VS TO +1.8VGS**



SHORT DEFAULT



|   |                          |                 |            |                 |                          |          |
|---|--------------------------|-----------------|------------|-----------------|--------------------------|----------|
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| Date:   | Tuesday, August 05, 2014 | Sheet           | 36         | of              | 55                       |          |

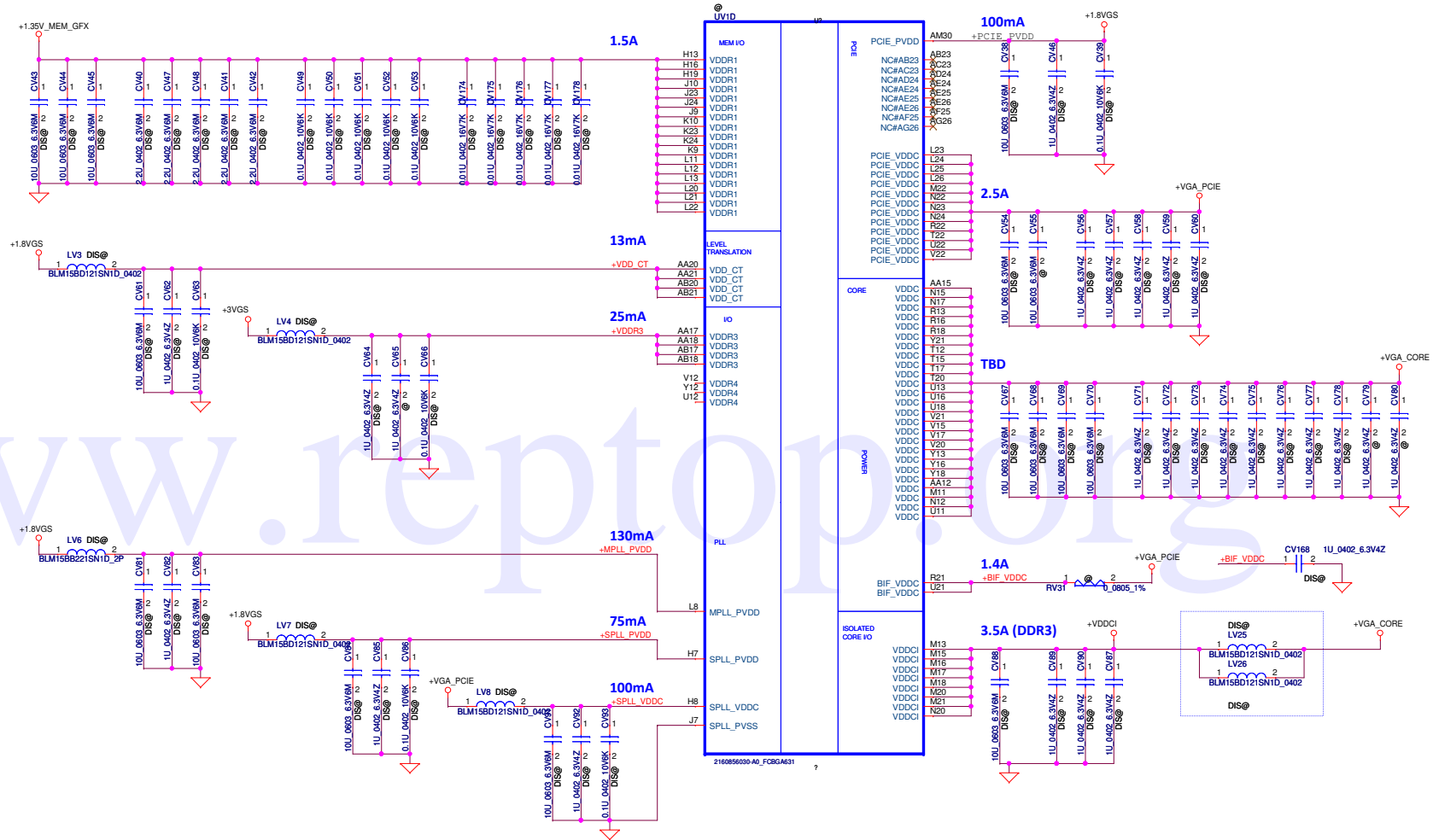
|                  |      |        |           |
|------------------|------|--------|-----------|
| <b>+VGA_CORE</b> | 10uF | 1uF    | 0.1uF     |
| VDDC             | TBD  | 5 (1@) | 10 (2@) 0 |
| VDDCI            | 3.5A | 1      | 3 0       |

|                  |       |        |          |
|------------------|-------|--------|----------|
| <b>+VGA_PCIE</b> | 10uF  | 1uF    | 0.1uF    |
| PCIE_VDDC        | 2.5A  | 2 (1@) | 5 (1@) 0 |
| BIF_VDDC         | 1.4A  | 0      | 1 0      |
| SPLL_VDDC        | 100mA | 1      | 1 1      |

|                       |      |       |       |        |
|-----------------------|------|-------|-------|--------|
| <b>+1.35V_MEM_GFX</b> | 10uF | 2.2uF | 0.1uF | 0.01uF |
| VDDR1 1.5A            | 3    | 5     | 5     | 5      |

|                |         |     |       |
|----------------|---------|-----|-------|
| <b>+1.8VGS</b> | 10uF    | 1uF | 0.1uF |
| PCIE_PVDD      | 100mA   | 1   | 1 1   |
| MPLL_PVDD      | 130mA   | 1   | 1 1   |
| SPLL_PVDD      | 75mA    | 1   | 1 1   |
| VDDR4          | (300mA) | 0   | 0 0   |
| VDD_CT         | 13mA    | 1   | 1 1   |
| +TSVDD         | 13mA    | 1   | 1 1   |
| +DP_VDDR       | 0       | 0   | 0 0   |
| +DP_VDDC       | 0       | 0   | 0 0   |

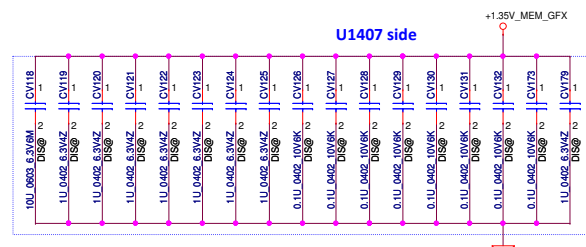
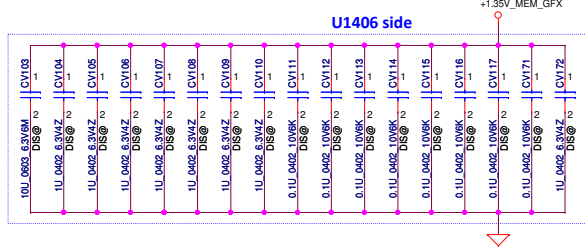
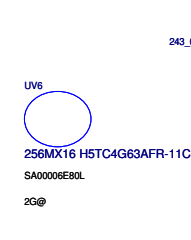
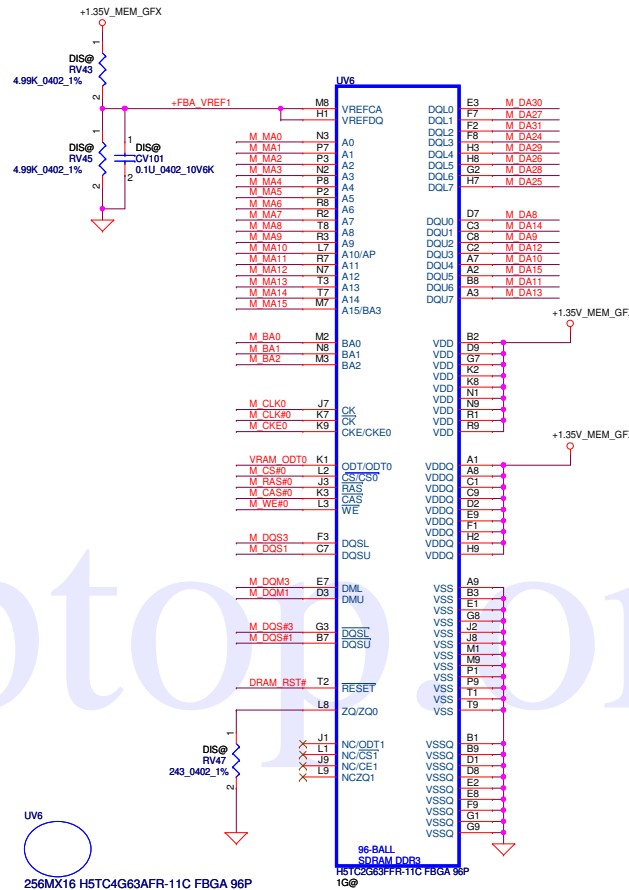
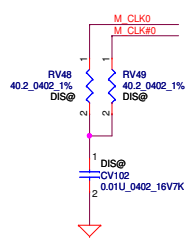
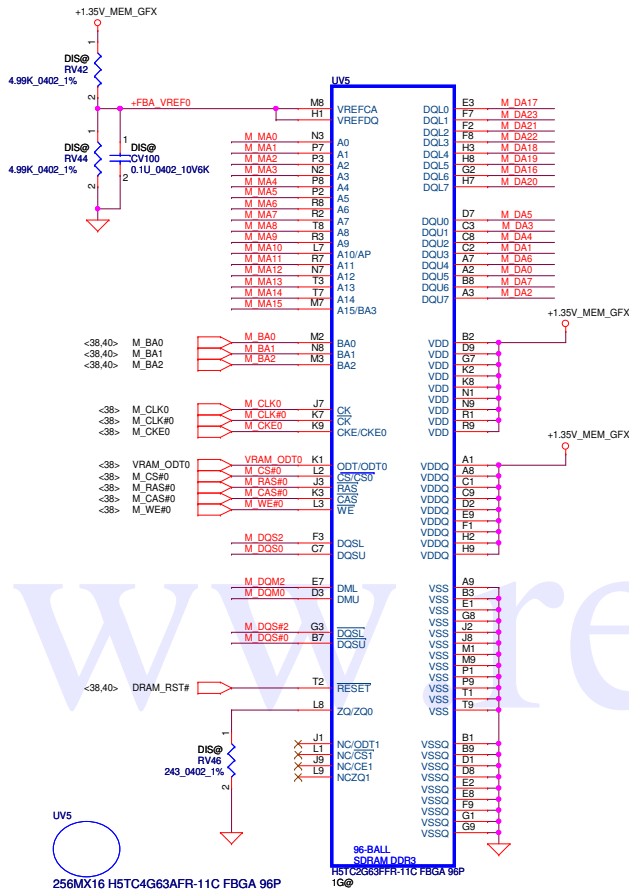
|              |      |     |          |
|--------------|------|-----|----------|
| <b>+3VGS</b> | 10uF | 1uF | 0.1uF    |
| VDDR3        | 25mA | 0   | 2 (1@) 1 |





# Memory Partition A - Lower 32 bits

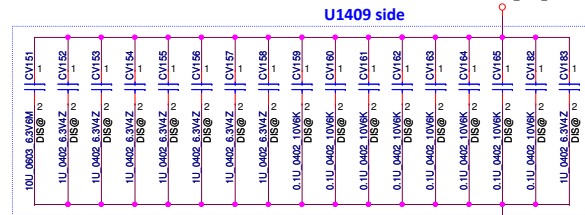
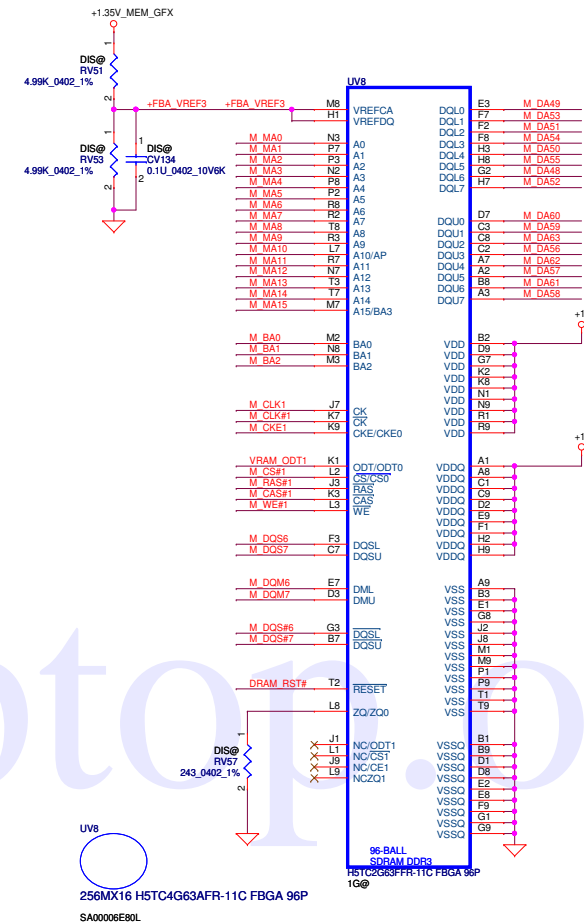
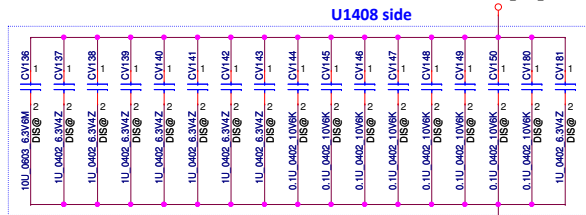
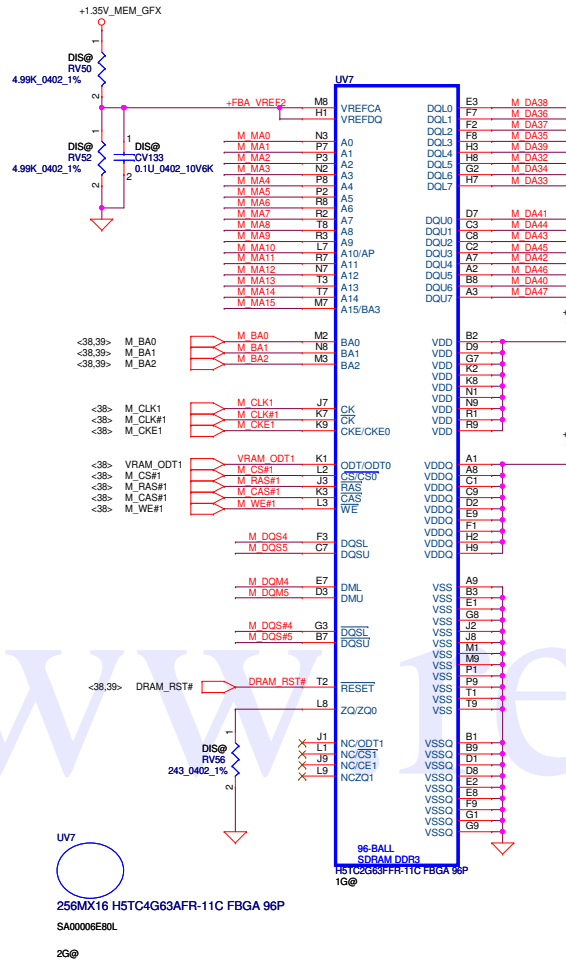
- <38,40> M\_DA[63..0] M\_DA[63..0]
- <38,40> M\_MA[15..0] M\_MA[15..0]
- <38,40> M\_DQM[7..0] M\_DQM[7..0]
- <38,40> M\_DQS[7..0] M\_DQS[7..0]
- <38,40> M\_DQS#[7..0] M\_DQS#[7..0]



|   |                          |                 |            |                    |
|---|--------------------------|-----------------|------------|--------------------|
| Security Classification   | Compal Secret Data       |                 | Title      |                    |
| Issued Date   | 2014/01/20               | Deciphered Date | 2015/01/19 | TOPAZ VRAM A Lower |
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| 320   | Document Number          | LA-B012P        |            | Rev 1.0            |
| Date:   | Tuesday, August 05, 2014 | Sheet           | 39         | of 55              |

# Memory Partition A - Upper 32 bits

- <38.39> M\_DA[63..0]  $\leftrightarrow$  M\_DA[63..0]
- <38.39> M\_MA[15..0]  $\leftrightarrow$  M\_MA15..0
- <38.39> M\_DQM[7..0]  $\leftrightarrow$  M\_DQM7..0
- <38.39> M\_DQS[7..0]  $\leftrightarrow$  M\_DQS7..0
- <38.39> M\_DQS# [7..0]  $\leftrightarrow$  M\_DQS#7..0



|   |            |                    |            |                                |                |
|---|------------|--------------------|------------|--------------------------------|----------------|
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|   |            |                    |            | SA00006E80L                    | 1.0            |
|   |            |                    |            | LA-B012P                       |                |
|   |            |                    |            | Date: Tuesday, August 05, 2014 | Sheet 40 of 55 |



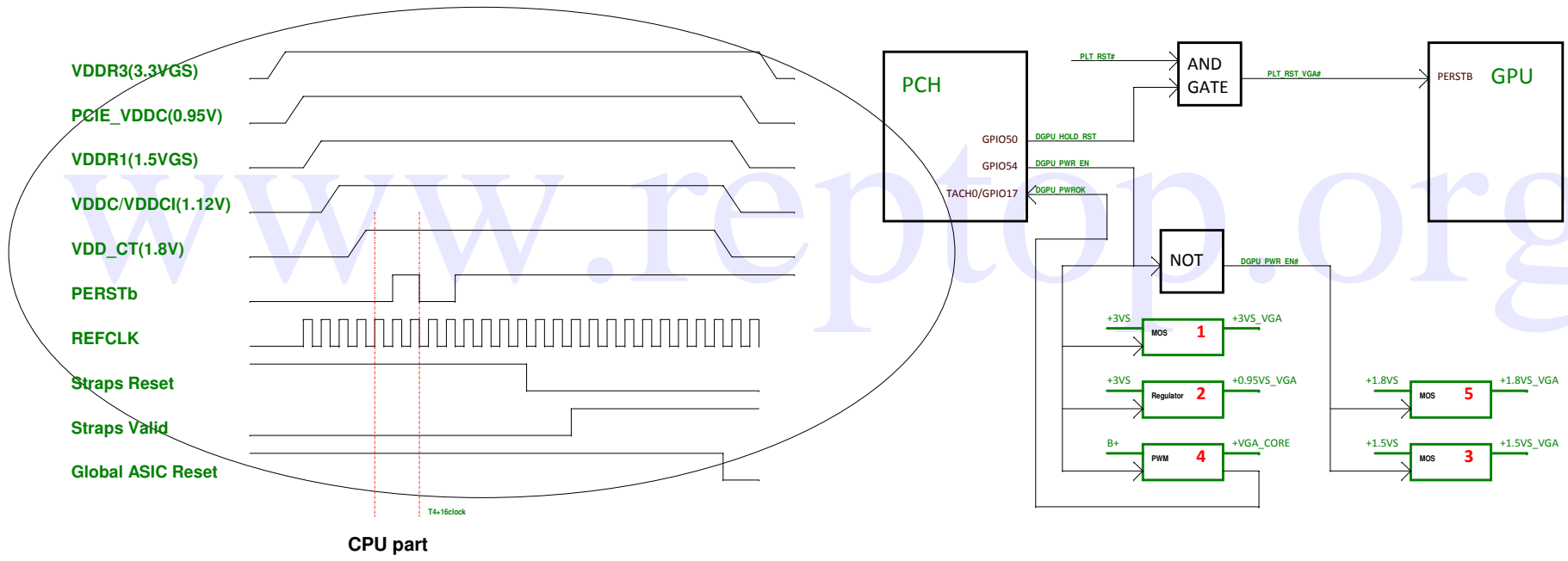
### Power-Up/Down Sequence

1. All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/ $\mu$ s.

2. The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD\_CT have ramped up.

3. VDDC and VDD\_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD\_CT starts to ramp up (or vice versa).

4. For power down, reversing the ramp-up sequence is recommended.



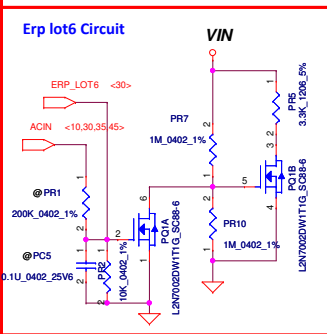
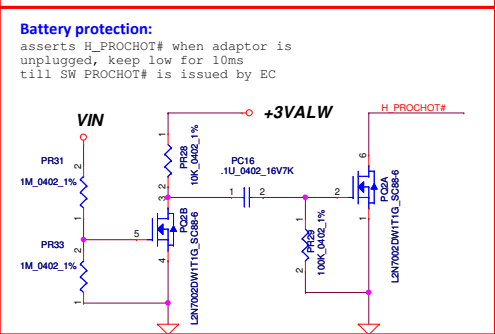
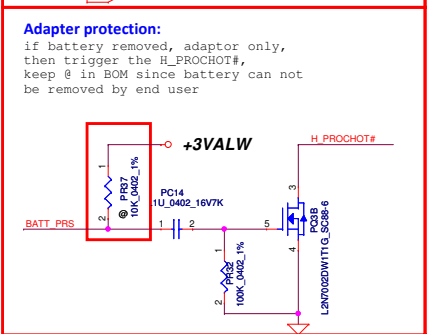
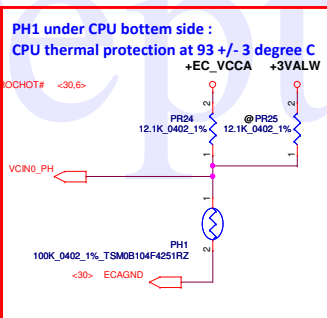
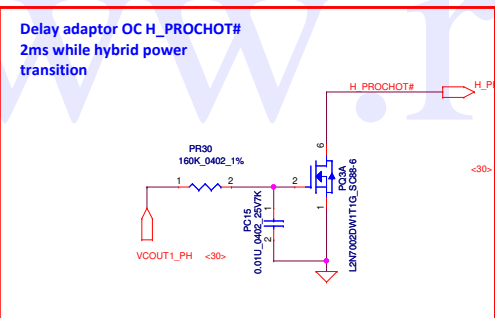
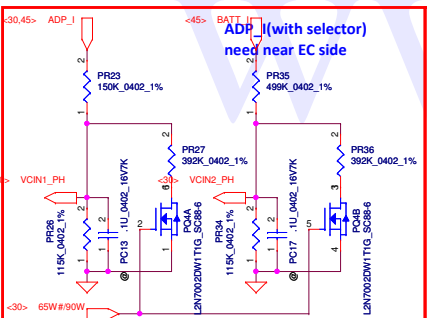
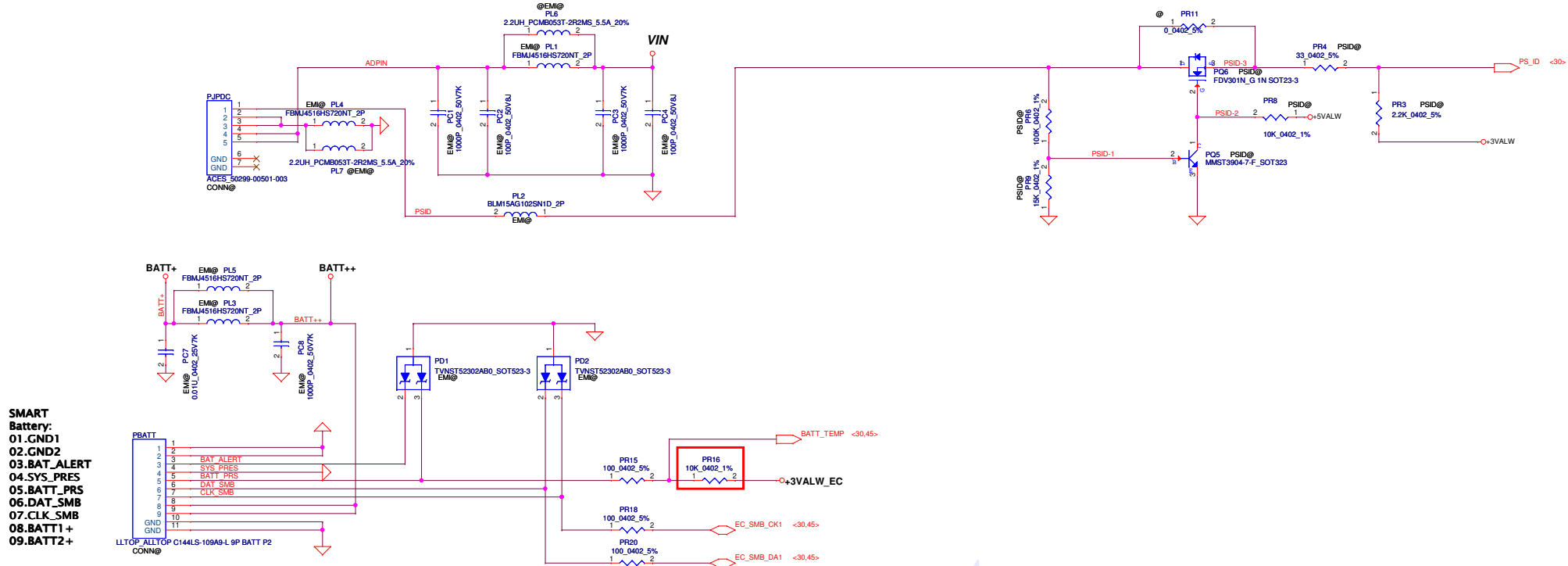
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| Size   | Sheet              | 41              | of                       | 55   |
| Rev  | 1.0                |                 |                          |  |

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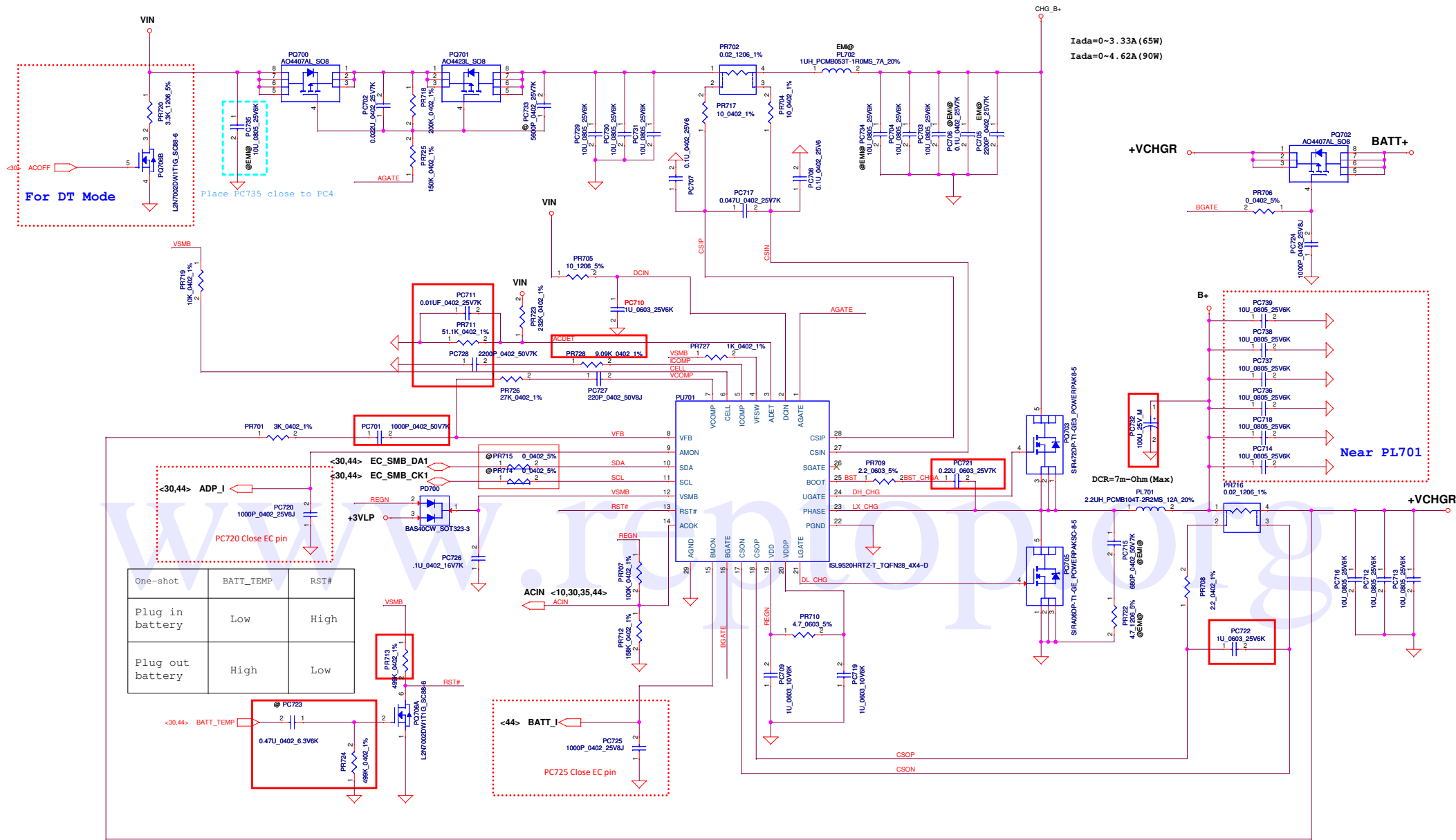
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|   |                    |                 |            | <b>LA-B012P</b>                 | 1.0                  |
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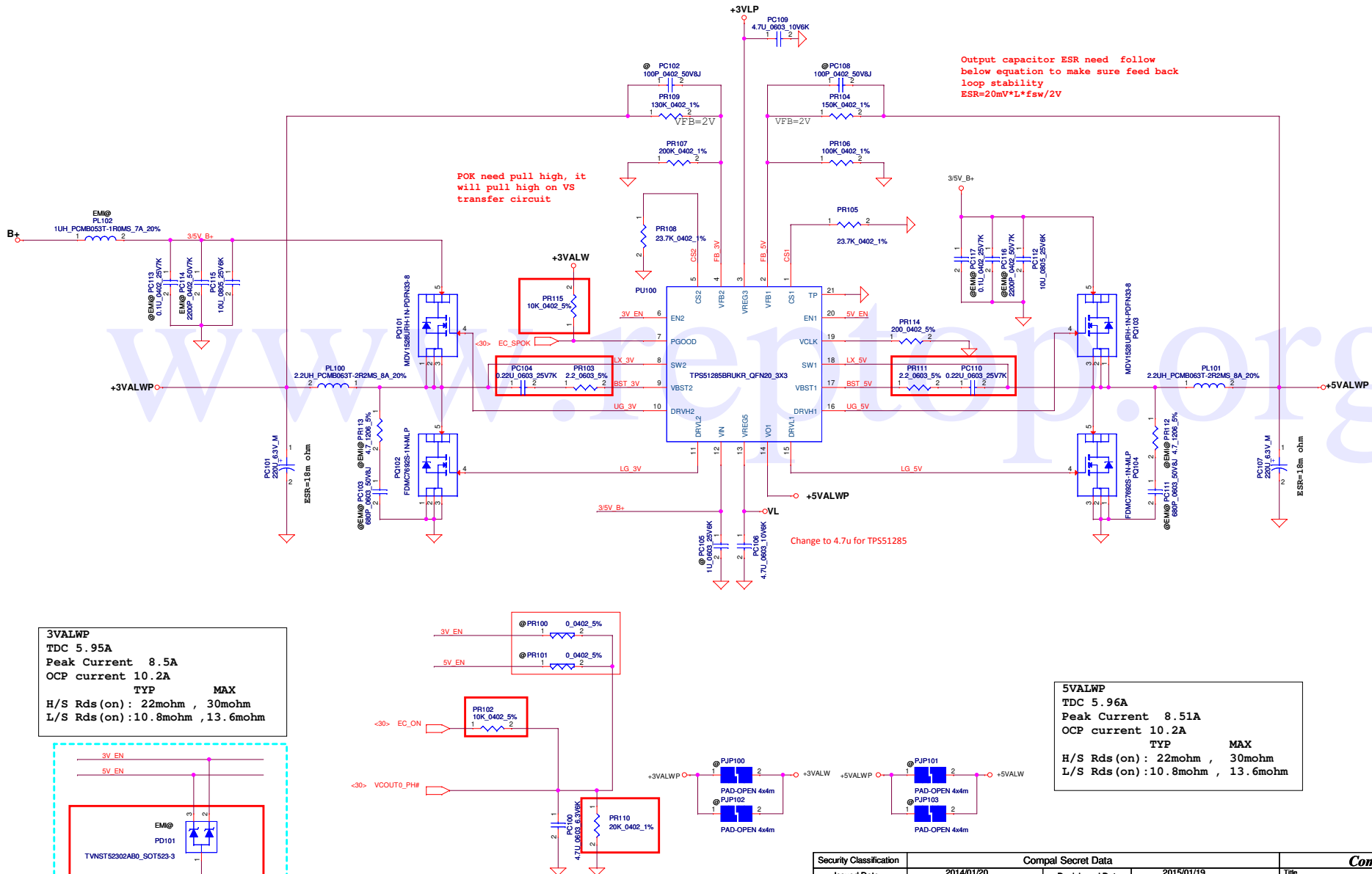
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|   |                    |                 |                                 | Document Number                | Rev            |
|   |                    |                 |                                 | <b>LA-B012P</b>                | 1.0            |
|   |                    |                 |                                 | Date: Tuesday, August 05, 2014 | Sheet 43 of 55 |



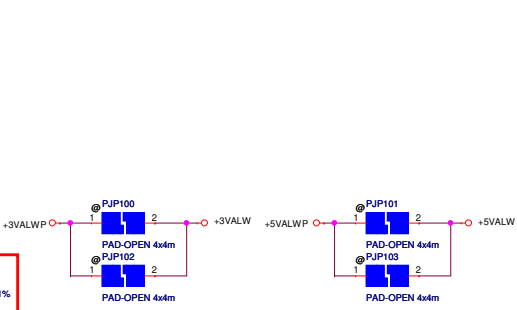
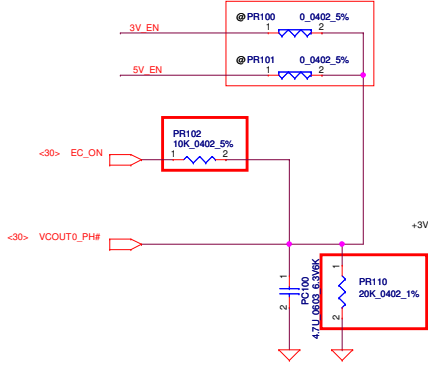
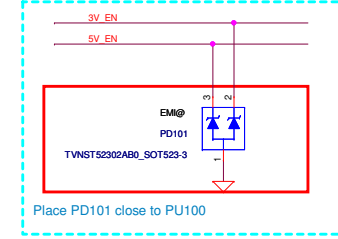
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| Date:  | Tuesday, August 05, 2014 | Sheet           | 44         | of                       | 55 |



2S2P : CV = 8.4V CC = 3.9A  
 3S1P : CV = 12.6V CC = 2A

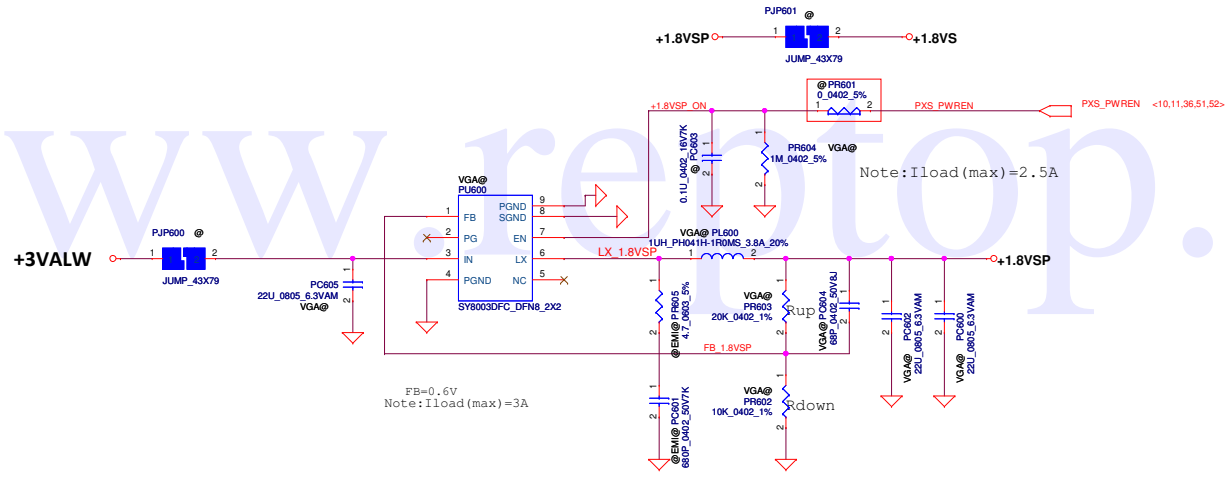
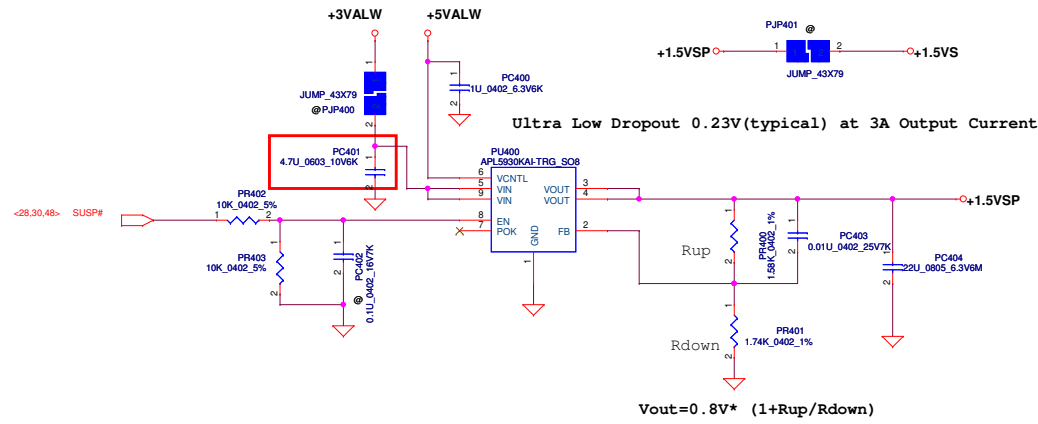


**3VALWP**  
 TDC 5.95A  
 Peak Current 8.5A  
 OCP current 10.2A  
 TYP MAX  
 H/S Rds (on) : 22mohm , 30mohm  
 L/S Rds (on) : 10.8mohm , 13.6mohm



**5VALWP**  
 TDC 5.96A  
 Peak Current 8.51A  
 OCP current 10.2A  
 TYP MAX  
 H/S Rds (on) : 22mohm , 30mohm  
 L/S Rds (on) : 10.8mohm , 13.6mohm

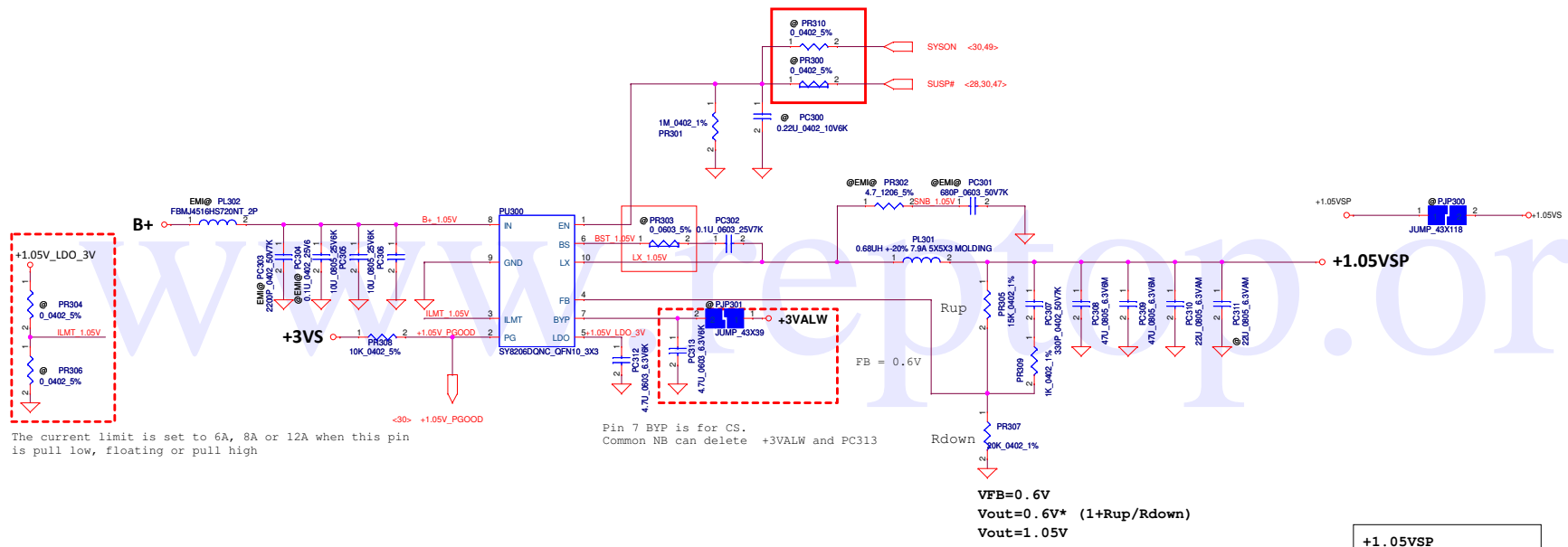
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|  |                    |                 |            | Date                     | Tuesday, August 05, 2014   |
|  |                    |                 |            | Sheet                    | 47 of 55                   |
|  |                    |                 |            | Rev                      | 1.0                        |

EN pin don't floating  
 If have pull down resistor at HW side, pls delete PR301



The current limit is set to 6A, 8A or 12A when this pin is pull low, floating or pull high

Pin 7 BYP is for CS.  
 Common NB can delete +3VALW and PC313

$$VFB=0.6V$$

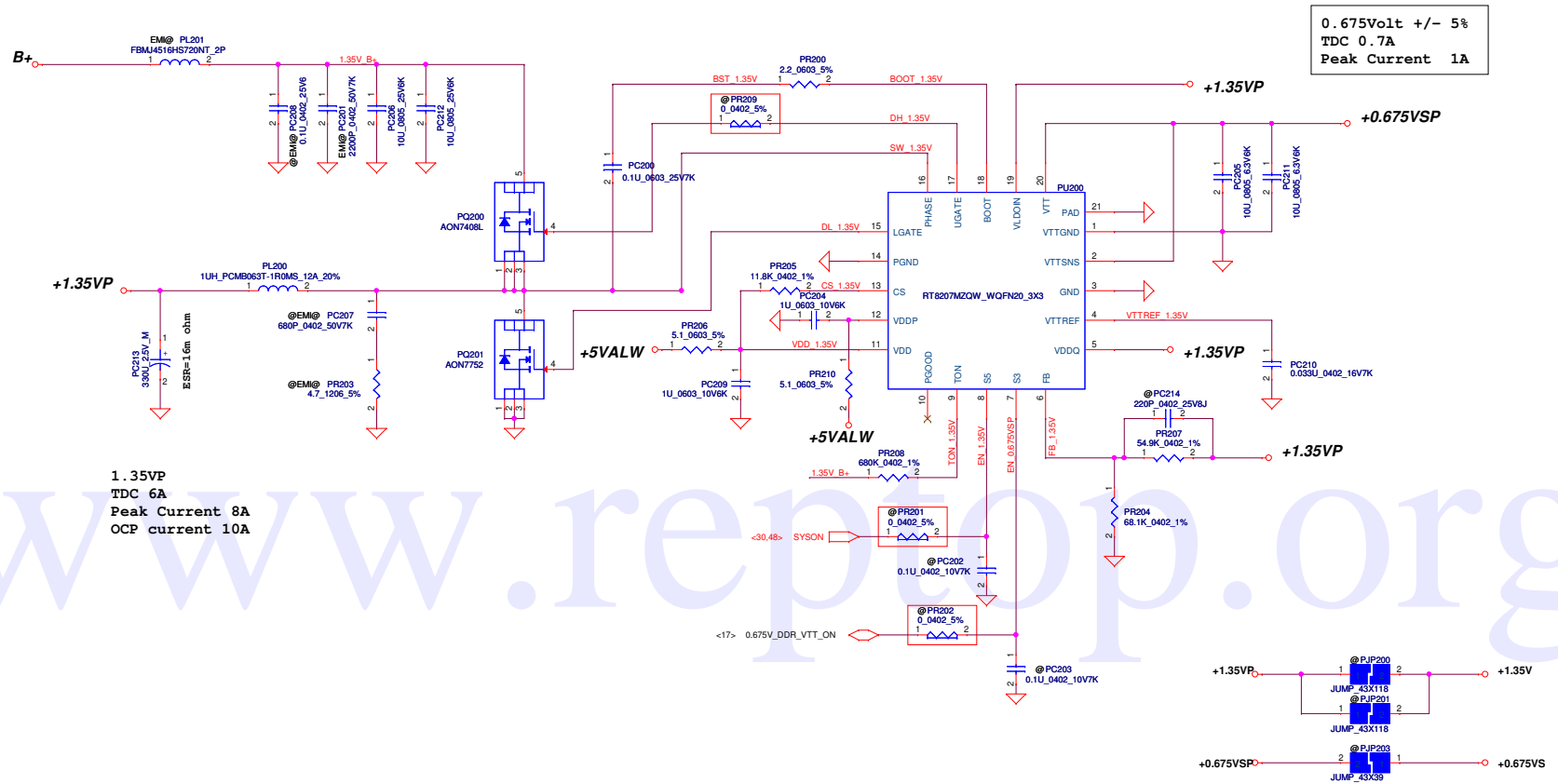
$$Vout=0.6V * (1+Rup/Rdown)$$

$$Vout=1.05V$$

+1.05VSP  
 TDC 5A  
 Peak Current 6.6A  
 OCP current 8A

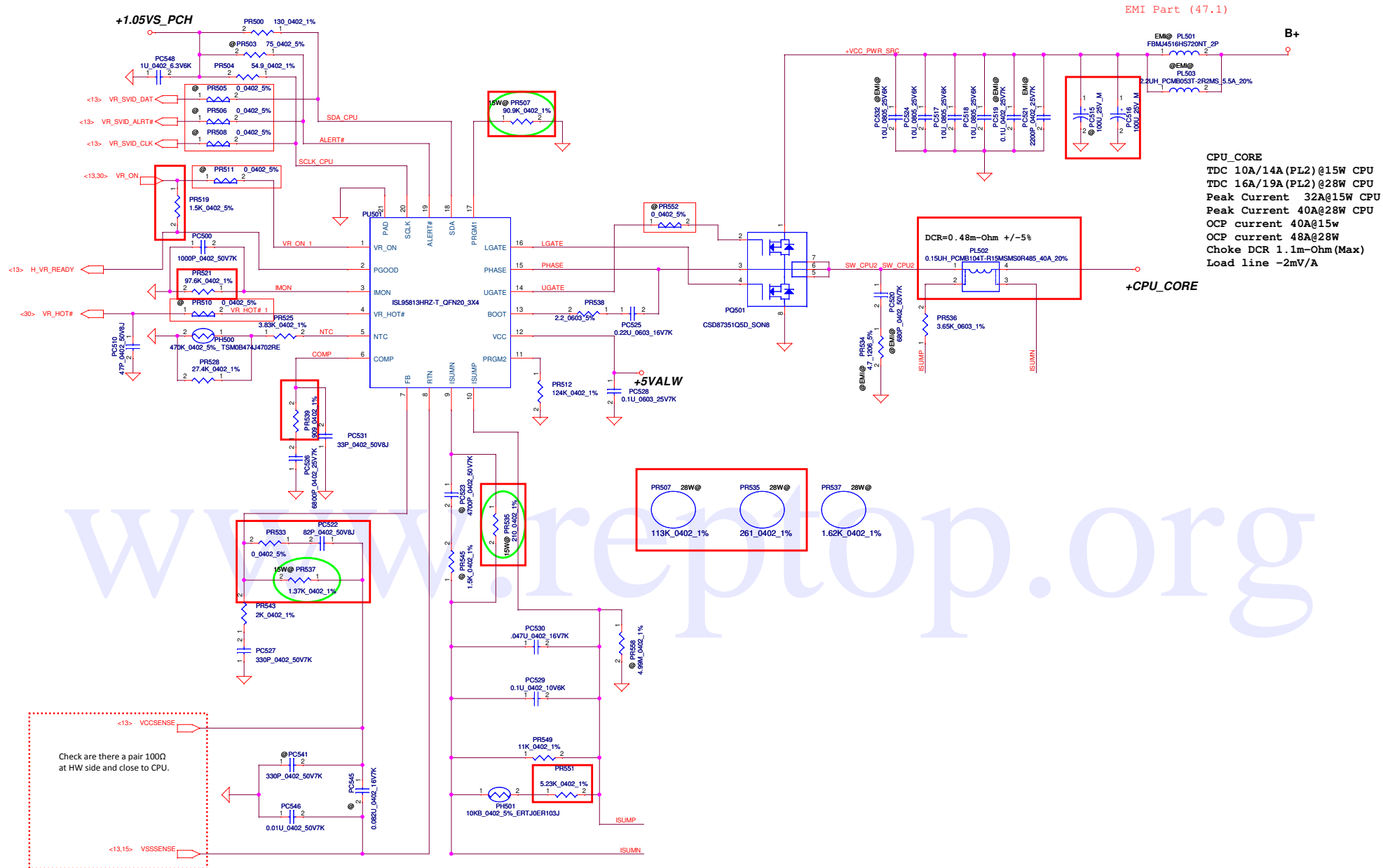
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EMI Part (47.1)

**CPU\_CORE**  
 TDC 10A/14A (PL2)@15W CPU  
 TDC 16A/19A (PL2)@28W CPU  
 Peak Current 32A@15W CPU  
 Peak Current 40A@28W CPU  
 OCP current 40A@15W  
 OCP current 48A@28W  
 Choke DCR 1.1m-Ohm(Max)  
 Load line -2mV/A

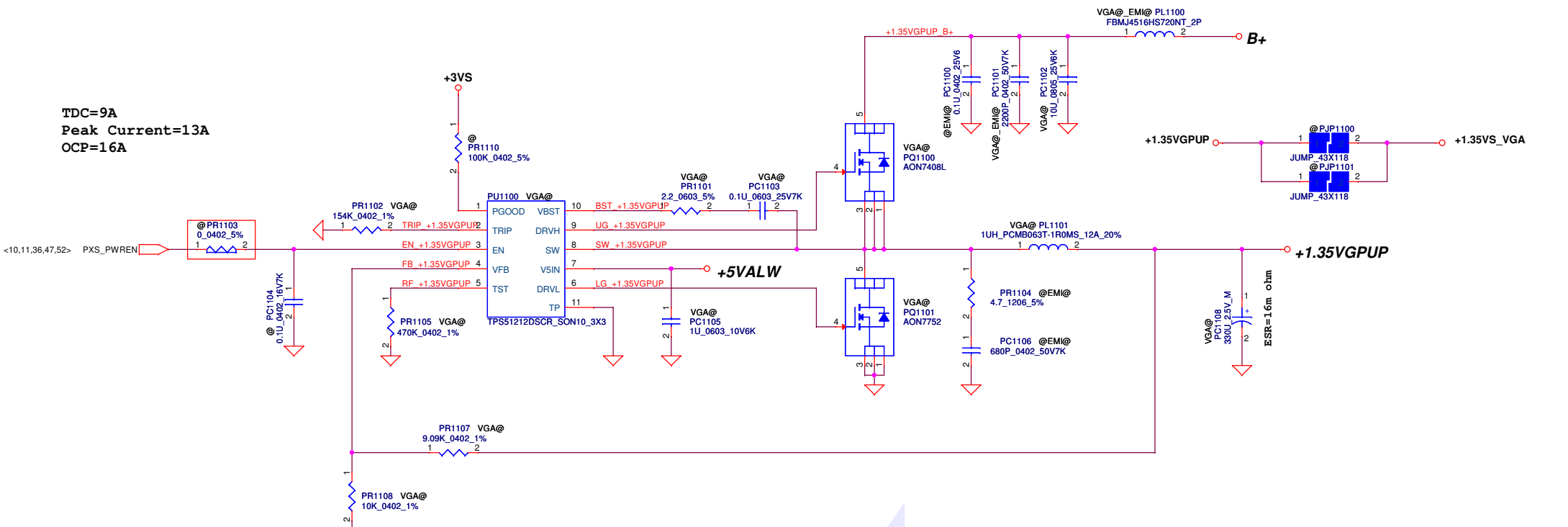
<13> VCCSENSE

Check are there a pair 100Ω at HW side and close to CPU.

<13,15> VSSSENSE

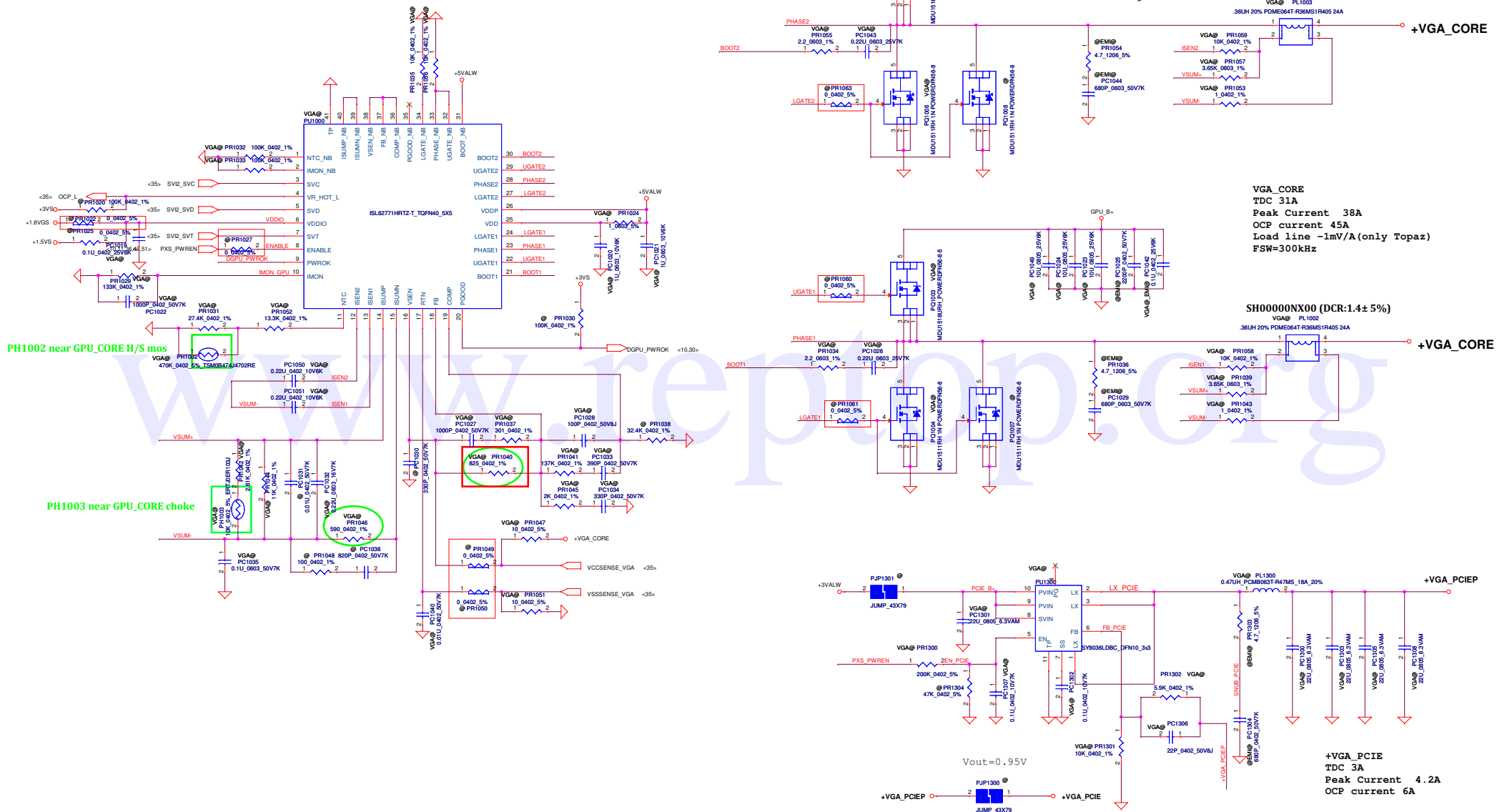
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| Security Classification  |            | Compal Secret Data |            | Title                    |          |
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| Date: Tuesday, August 05, 2014   |            |                    |            | Sheet                    | 50 of 55 |

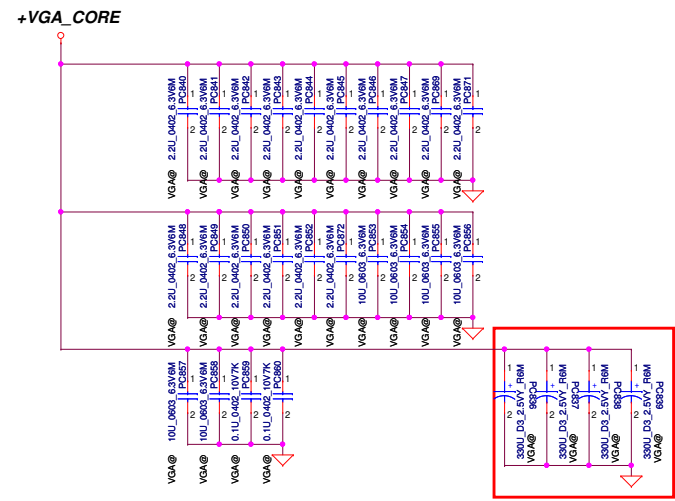
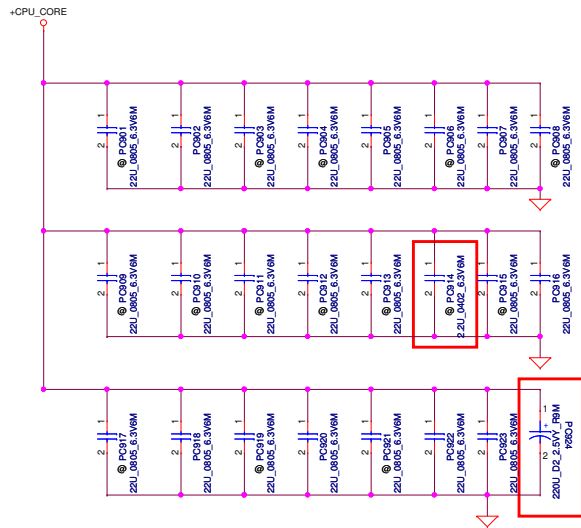
TDC=9A  
Peak Current=13A  
OCP=16A



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|  |            |                    |            |                          |                          |
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|  |            |                    |            | Sheet                    | 51 of 55                 |
|  |            |                    |            | Rev                      | 1.0                      |

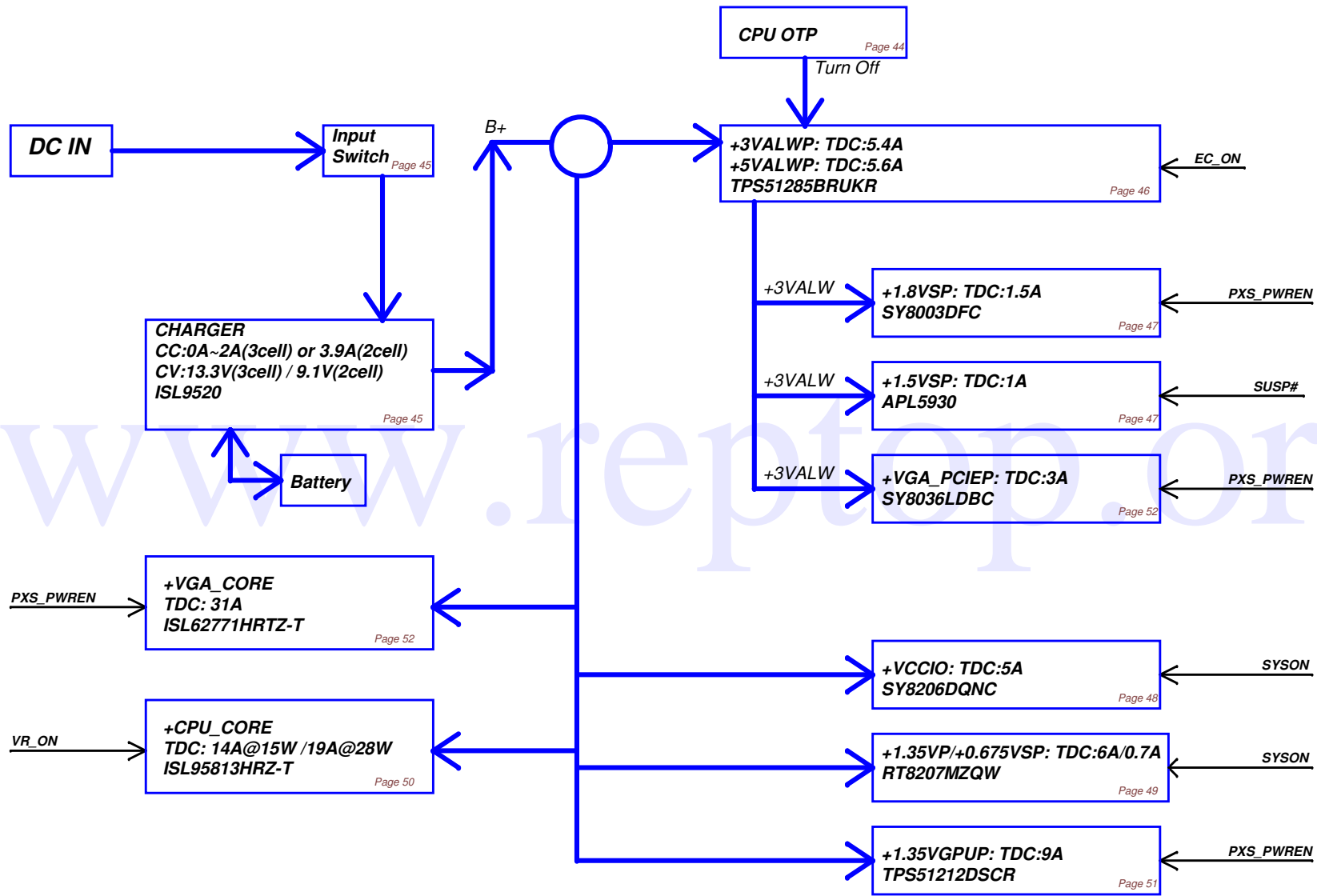




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# Power block



Version Change List (P. I. R. List)

| Item | Page# | Title                | Date     | Request Owner | Issue Description                                  | Solution Description   | Rev. |
|------|-------|----------------------|----------|---------------|--|--|------|
| 1    | 44    | DCIN/BATT CONN/OTP   | 13/10/24 | Morris        | design change                                      | change PR16 from 100K to 10K<br>add PR37 10K   | 0.2  |
| 2    | 45    | CHARGER              | 13/10/24 | Morris        | design change                                      | change PC711 from 1000pF to 0.01uF<br>change PR711 from 49.9K to 51.1K<br>change PR713 from 10K to 499K<br>change PR724 from 100K to 499K<br>change PC721 from 0.047u to 0.22u<br>change PC722 from 0.1u to 1u<br>add PC732 100u   | 0.2  |
| 3    | 46    | 3.3VALWP/5VALWP      | 13/10/24 | Morris        | design change for solve can't root issue           | change PC104 from 0.1u to 0.22u<br>change PC110 from 0.1u to 0.22u<br>change PR102 from 2.2K to 10K<br>add PR110 20K   | 0.2  |
| 4    | 50    | VCORE                | 13/10/24 | Morris        | adjust CPU parameter                               | change PR507(15W0) from 90.9K to 169K<br>change PR519 from 1.91K to 10K<br>change PR521 from 95.3K to 97.6K<br>change PR539 from 8.06K to 909<br>change PC515,PC516 from SF000005100 to SF000004M00<br>change PL502 from SH00000NM00 to SH00000PQ00<br>change PR535(15W0) from 340 to 210<br>change PR537 from 1.27K to 1.37K<br>change PR535(28W0) from 432 to 261<br>change PR507(28W0) from 113K to 205K<br>change PR551 from 2.61K to 5.23K<br>add PC522 82pF<br>add PR533 0-ohm | 0.2  |
| 6    | 52    | VGA_CORE/PCIE        | 13/10/24 | Morris        | design change from vendor change LL                | change PR1040 from 1.24K to 825  | 0.2  |
| 7    | 53    | PROCESSOR DECOUPLING | 13/10/24 | Morris        | adjust CPU parameter                               | change PC924 from SGA20331E10 to SGA00009800<br>remove PC901,PC903,PC904,PC906,PC908,PC909,PC910,PC911,PC912,PC913,PC914,PC915,PC917,PC919,PC921   | 0.2  |
| 8    | 45    | CHARGER              | 13/10/28 | Morris        | design change for plug out battery shut down issue | change PC723 from 0.01uF to 0.47uF<br>change PR728 from 0 to 9.09K<br>change PC728 from 4700pF to 2200pF<br>change PC701 from 220pF to 1000pF  | 0.2  |
| 9    | 46    | 3.3VALWP/5VALWP      | 13/12/12 | Morris        | design change from EE request                      | add PR115 10K-ohm  | 0.3  |
| 10   | 50    | VCORE                | 13/12/12 | Morris        | design change from Intel recommend                 | change PR519 from 10K to 1.5K  | 0.3  |
| 11   | 48    | +VCCIO               | 13/12/13 | Morris        | design change from EE request                      | delete PR310 and add PR300 0-ohm   | 0.3  |
| 12   | 50    | VCORE                | 14/01/20 | Morris        | adjust CPU parameter                               | change PR507(15W0) from 169K to 90.9K<br>change PR507(28W0) from 205K to 113K  | 1.0  |
| 13   | 53    | PROCESSOR DECOUPLING | 14/02/13 | Morris        | design change from thermal request                 | change PC836 PC837 PC838 PC839 from SGA20331E10 to SGA00006A00   | 1.0  |