


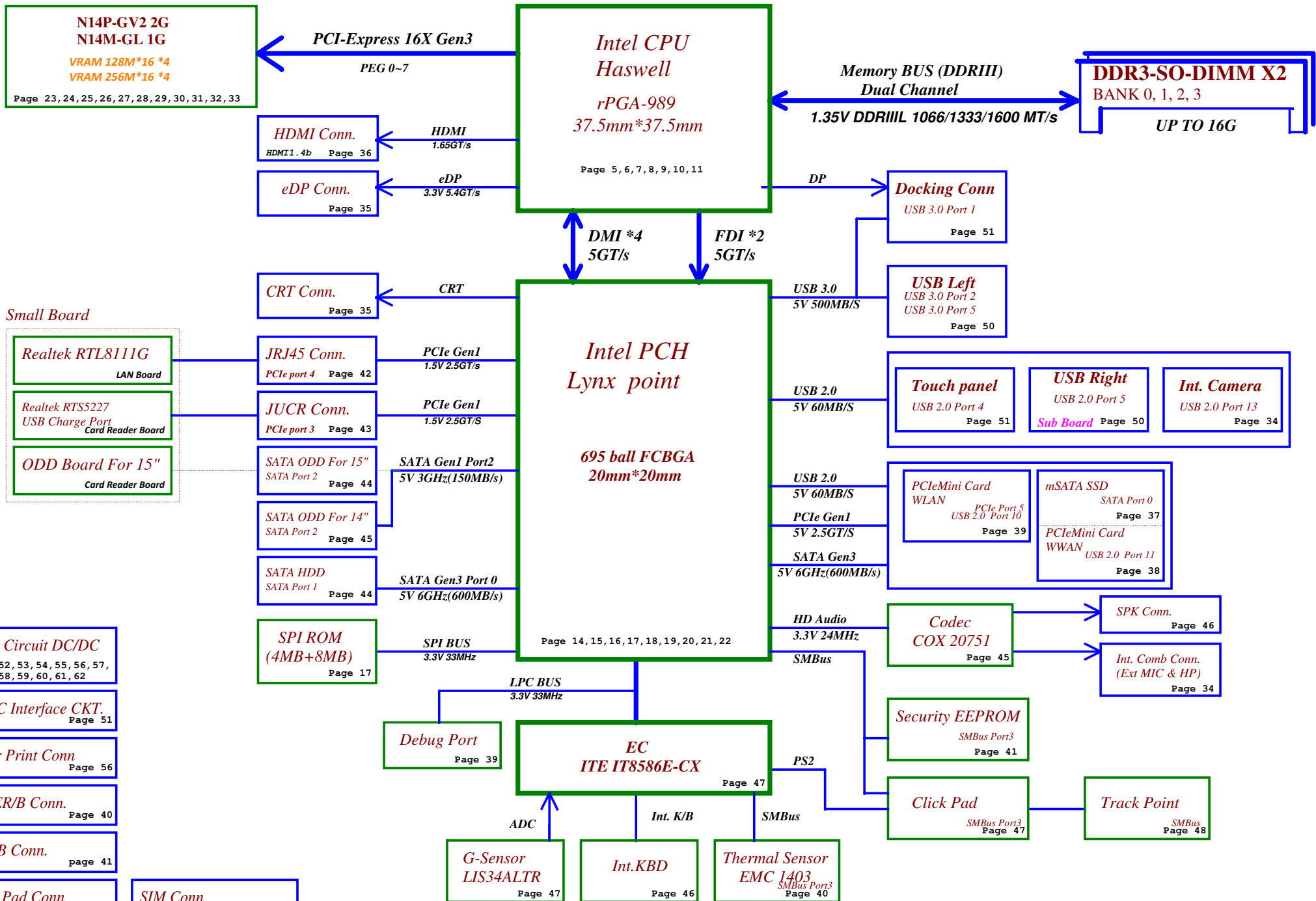
# ***E440***

## ***NM-A151 Rev1.0 Schematic***

***Intel Haswell Processor with DDRIII + Lynx point PCH  
nVIDIA N14P-GV2/ N14M-GL***

***2013-07-11 Rev 1.0***

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Date:					Thursday, July 11, 2013	Sheet 1 of 57
Document Number					<b><i>E440 NM-A151</i></b>	Rev 1.0



- Power Circuit DC/DC**  
Page 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62
- DC/DC Interface CKT.**  
Page 51
- Finger Print Conn.**  
Page 56
- POWER/B Conn.**  
Page 40
- ODD/B Conn.**  
page 41
- Touch Pad Conn**  
Page 56
- Click Pad Conn**  
Page 55
- SIM Conn**  
Page 54
- Track Point Conn.**  
Page 53

Security Classification	LC Future Center Secret Data		Title		
Issued Date	2012/12/05	Deciphered Date	2014/12/05		Block Diagram
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Date:	Thursday, July 11, 2013	Sheet	2	of	57

**Voltage Rails ( O --> Means ON , X --> Means OFF )**

Power Plane	State	B+	+3VALW	+5VALW	+1.5V	+5VS +3VS +1.5VS +VCCSA +V1.5S_VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +1.05VS +0.75VS +3.3VS_VGA +1.5VS_VGA +1.05VS_VGA
S0	O	O	O	O	O	
S3	O	O	O	O	X	
S5 S4/AC Only	O	O	O	X	X	
S5 S4 Battery only	O	X	X	X	X	
S5 S4 AC & Battery don't exist	X	X	X	X	X	

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

**USB Port Table**

USB 2.0	USB 3.0	Port	4 External USB Port
		0	Camera
	XHCCI	1	USB Port (Right Side)
		2	USB Port (Left Side)
		3	
		4	
	EHCI1	5	USB Port (Right Side)
		6	
		7	
		8	
		9	
		10	Mini Card(WLAN)
		11	
		12	
		13	Blue Tooth
	EHCI2		

**BOM Structure Table**

BOM Structure	BTO Item
HDMI@	HDMI part
CHG@	USB charger part
NOCHG@	No USB charger part
CMOS@	CMOS sensor support part
8171@	QCA8171 LAN part
8171S@	QCA8171 LAN surge part
SURGE@	QCA8171&8172 LAN surge part
X76@	X76 Level part for VRAM
GC6@	NV CG6 support part
NOGC6@	
AOAC@	AOAC support part
KBL@	K/B Light part
ME@	ME part
SLI@	For SLI function part
DS3@	Deep S3 support part
S3@	For S3 function part
GT@	NV chip part
@	Unpop
EDP@	Support EDP panel function
daul@	Support daul channel panel function

**SMBUS Control Table**

	SOURCE	Main VGA	2nd VGA	BATT	IT8580E	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	CP Module
EC_SMB_CK1 EC_SMB_DA1	IT8580E +3VALW	X	X	V +3VALW	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8580E +3VS	V +3VS	V +3VS	X	X	X	X	V +3VS	V +3V_PCH	X
PM_SMBCLK PM_SMBDATA	PCH +3V_PCH	X	X	X	X	V +3VS	V +3VS	X	V +3V_PCH	V +3VS

**PCIe PORT LIST**

Port	Device
1	LAN
2	WLAN
3	
4	Card Reader
5	
6	
7	
8	

**EC SM Bus1 address**

Device	Address
Smart Battery	0001 011X b

**EC SM Bus2 address**

Device	Address
Thermal Sensor EMC1403-2	1001_101xb
Master VGA	0x9E
Slave VGA	0x9C

**PCH SM Bus address**

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb



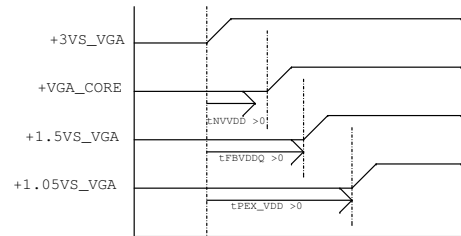
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Title	Notes List
Size Custom	Document Number <b>E440-NW-A151</b>
Date: Thursday, July 11, 2013	Rev 1.0
Sheet 3 of 57	

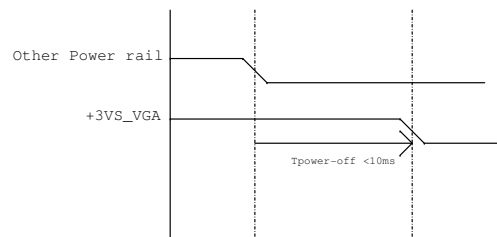


### VGA and GDDR5 Voltage Rails (N13Px GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU VID4
GPIO1	OUT	-	GPU VID3
GPIO2	OUT	-	VGA_BL_PWM
GPIO3	OUT	-	VGA_ENVDD
GPIO4	OUT	-	VGA_ENBKL
GPIO5	OUT	-	GPU VID1
GPIO6	OUT	-	GPU VID2
GPIO7	OUT	-	DPRSLPVR_VGA
GPIO8	I/O	-	Thermal Catastrophic Over Temperature
GPIO9	OUT	-	GPIO9
GPIO10	OUT	-	Memory VREF Control
GPIO11	OUT	-	GPU VID0
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	GPU VID5
GPIO14	OUT	-	FB_CLAMP_TOGGLE_REQ#
GPIO15	IN	N/A	(100K pull low)
GPIO16	OUT	-	FRMLCK#
GPIO17	IN	N/A	
GPIO18	IN	-	dGPU_HDMI_HP
GPIO19	IN	-	HPD_IRQ



1. all power rail ramp up time should be larger than 40us



1. all GPU power rails should be turned off within 10ms  
2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ

### Performance Mode P0 TDP at Tj = 102 C\* (GDDR5)

Products	GPU (4)	Mem (1,5)	NVCLK /MCLK	NVVDD			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		PCI Express (1.05V) (6)		I/O and PLLVDD (1.8V)		I/O and PLLVDD (1.05V)		Other (3.3V)	
	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N13X 128bit 1GB GDDR5	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

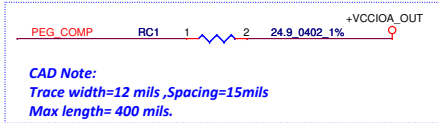
Device ID	setting	I2C Slave address ID
N13P-GT (28nm)	0x0FDB	
	SMB_ALT_ADDR (ROM_SO Bit 1)	0 0x9E
		1 0x9C

GPU	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4	
N13P-GT1 28nm	PU 10K	PU 25K	PU 45K	PD 35K	PD 10K	PU 5K	PD 10K	Master
	PU 20K	PU 25K	PU 45K	PD 35K	PD 10K	PD 5K	PD 10K	Slave

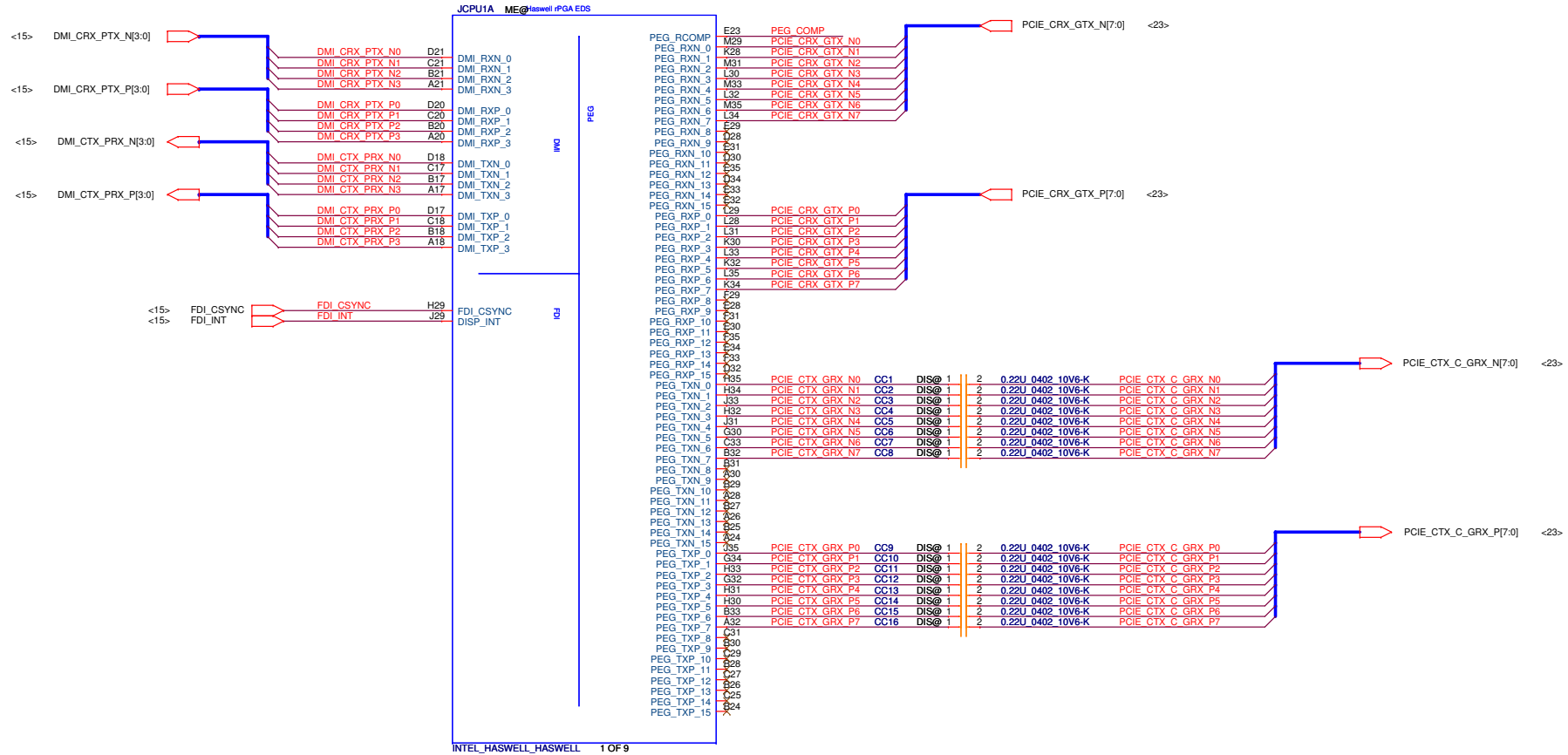
GPU	N13P-GT		
FB Memory (GDDR5)	ROM_SI		
Samsung 2500MHz	K4G10325FG-HC04		
	32Mx32	PD 45K	
Hynix 2500MHz	H5GQ1H24BFR-T2C		
	32Mx32	PD 35K	
Samsung 2500MHz	K4G20325FD-FC04		
	64Mx32	PD 30K	
Hynix 2500MHz	H5GQ2H24MFR-T2C		
	64Mx32	PD 25K	

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			Document Number
			<b>E440-NM-A151</b>
			Rev 1.0
			Date: Thursday, July 11, 2013
			Sheet 4 of 57





**CAD Note:**  
Trace width=12 mils, Spacing=15mils  
Max length= 400 mils.



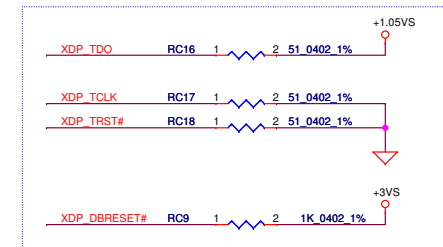
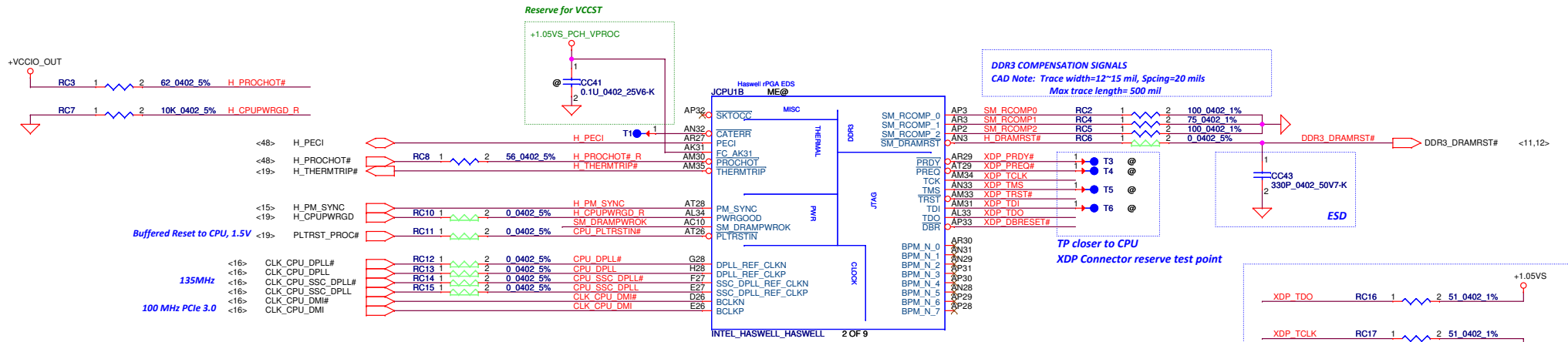
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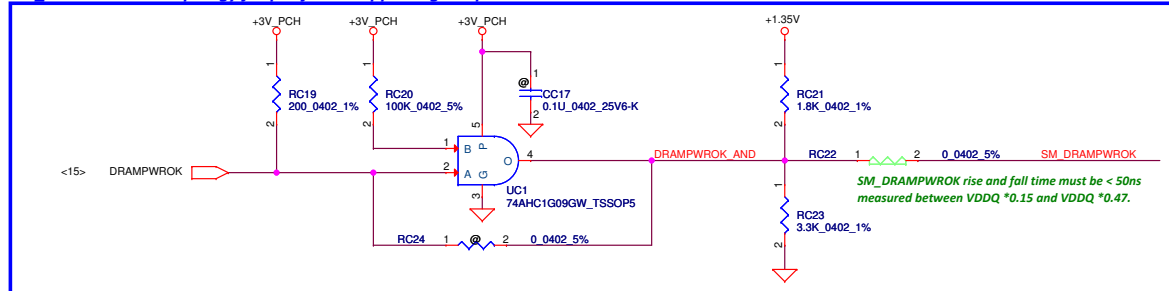
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Title		Rev	
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Size	Document Number	E440 NM-A151	
Custom			
Date:	Thursday, July 11, 2013	Sheet	5 of 57

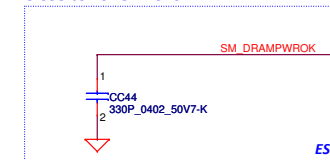




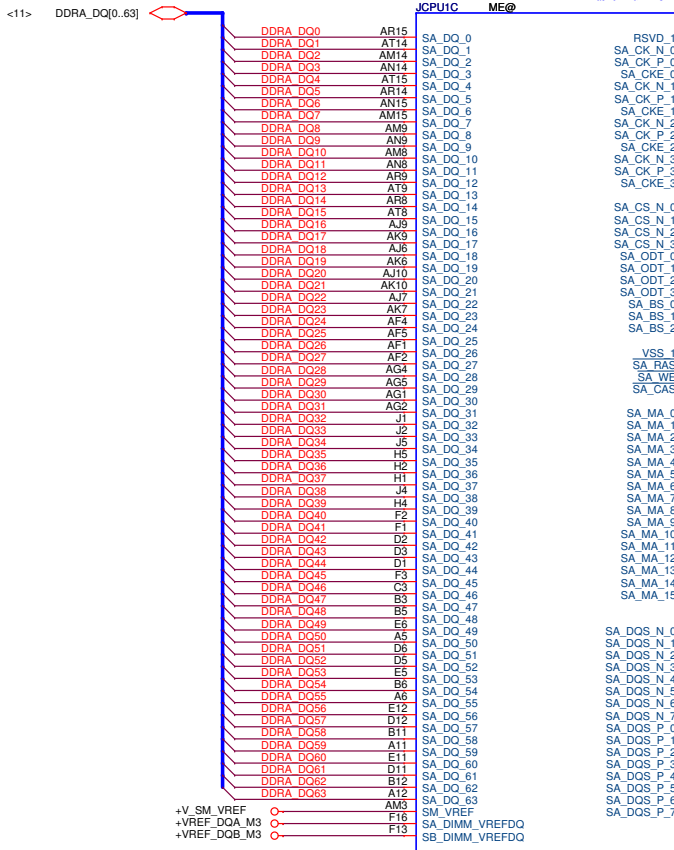
**SM\_DRAMPWROK Topology for platforms supporting Deep S3**



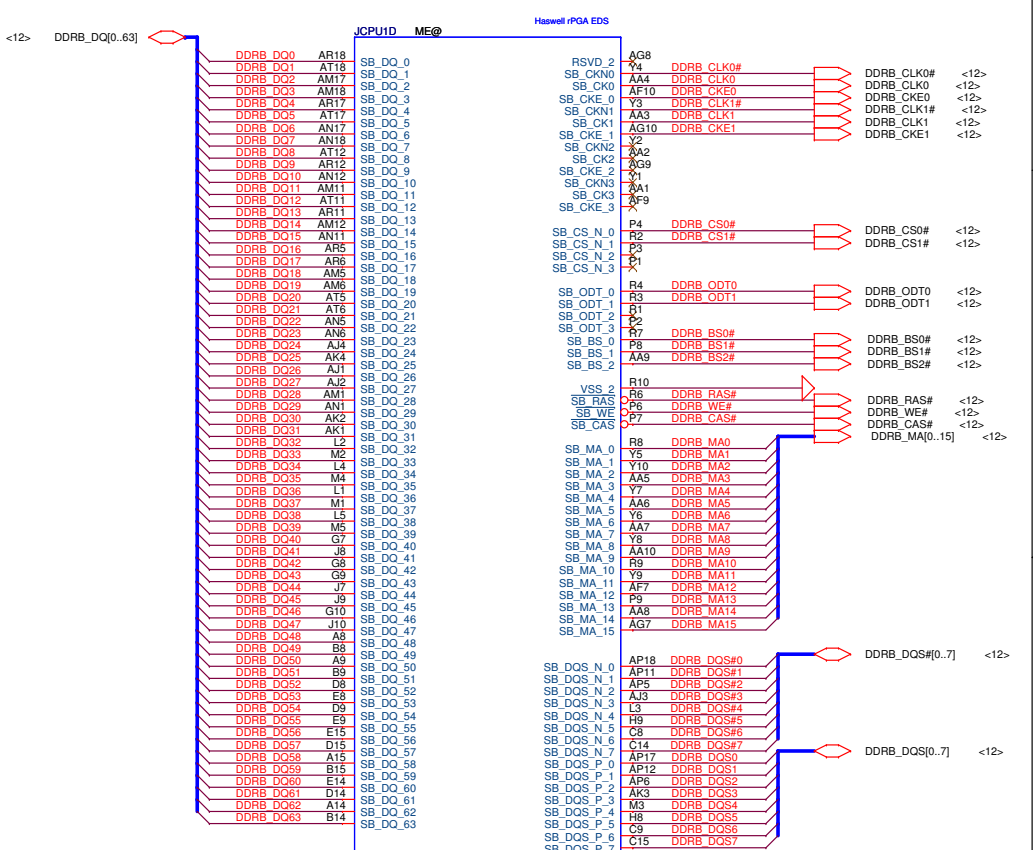
**Close to JCPU. AC10**



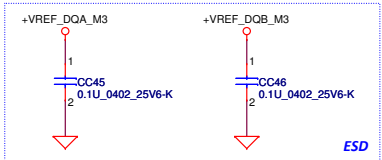
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Size	Document Number	Date	Thursday, July 11, 2013	Rev 1.0
Custom	<b>E440 NM-A151</b>	Sheet	6	of 57



INTEL\_HASWELL\_HASWELL 3 OF 9



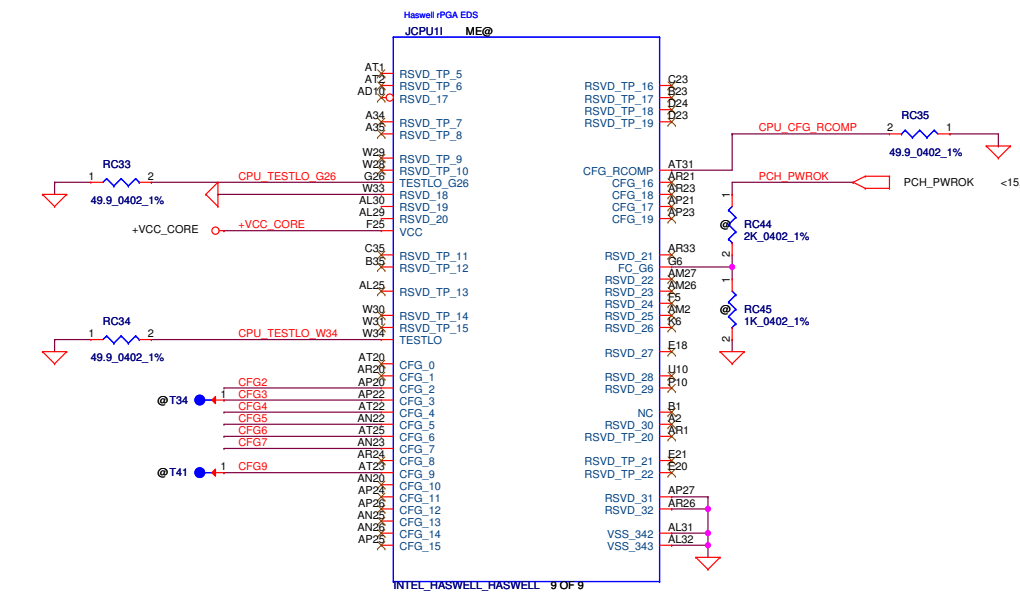
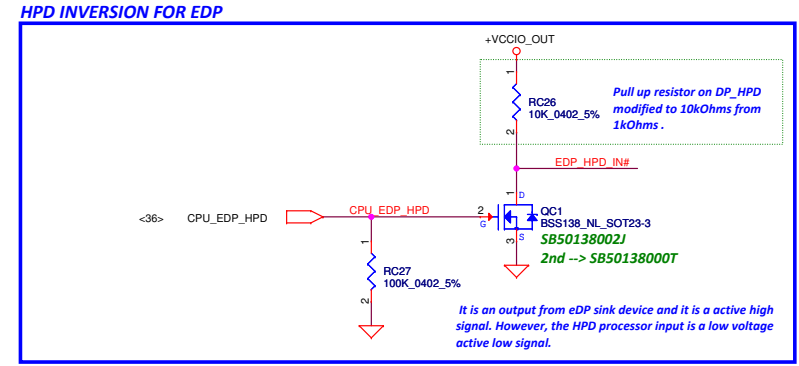
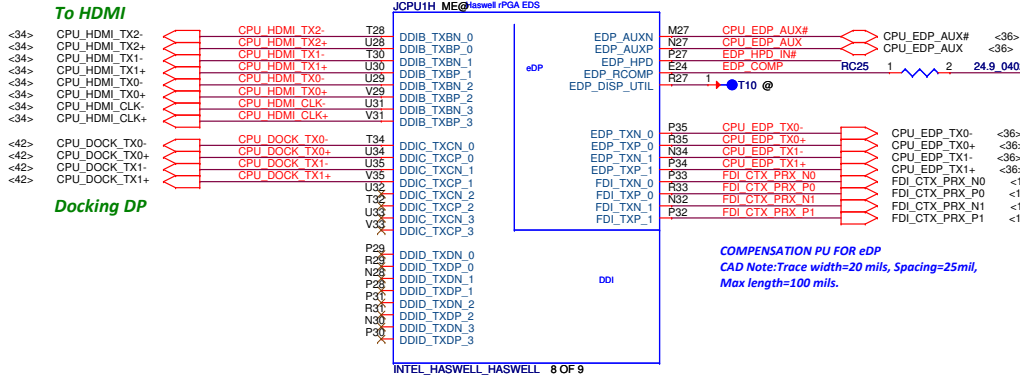
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ESD

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Size	Document Number	Date	Sheet
Custom	E440 NM-A151	Thursday, July 11, 2013	7 of 57

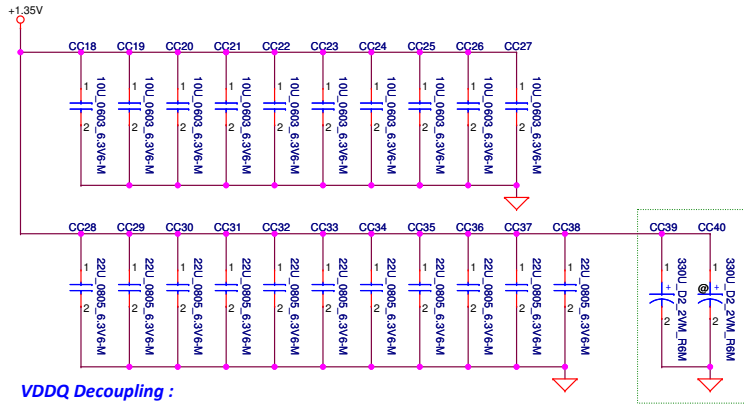


**CFG STRAPS For CPU**  
 (CFG[17:0] internal pull high 5 ~15K to VCCIO)

<b>PEG Static Lane Reversal - CFG2 is for the 16x</b>		CFG2 RC28 1 @ 2 1K_0402_1%
CFG2	* 1: (Default) Normal Operation; Lane# definition matches socket pin map definition 0: Lane Reversed	
<b>Display Port Presence Strap</b>		CFG4 RC29 1 @ 2 1K_0402_1%
CFG4	1: Disabled No Physical Display Port attached to Embedded Display Port * 0: Enabled; An external Display Port device is connected to the Embedded Display Port	
<b>PCIe Port Bifurcation Straps</b>		CFG5 RC30 1 @ 2 1K_0402_1% CFG6 RC31 1 @ 2 1K_0402_1%
CFG[6:5]	11: Func 1 Disabled, Func 2 Disabled (x16,---,---) * 10: Func 1 Enabled, Func 2 Disabled (x8,x8,---) 01: Func 1 Disabled, Func 2 Enabled 00: Func 1 Enabled, Func 2 Enabled (x8,x4,x4)	
<b>PEG DEFER TRAINING</b>		CFG7 RC32 1 @ 2 1K_0402_1%
CFG7	* 1: (Default) PEG Train Immediately Following XXRESETB Deassertion 0: PEG Wait for BIOS for Training	



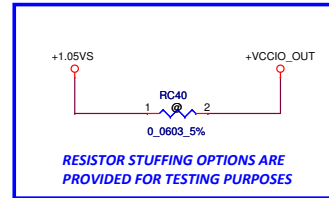
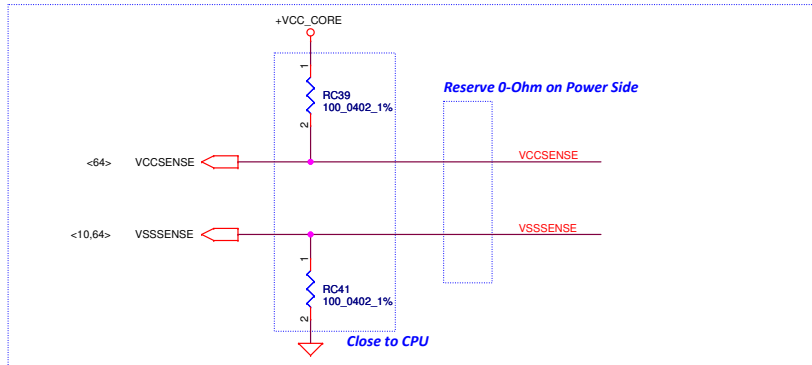
### CPU VDDQ DECOUPLING



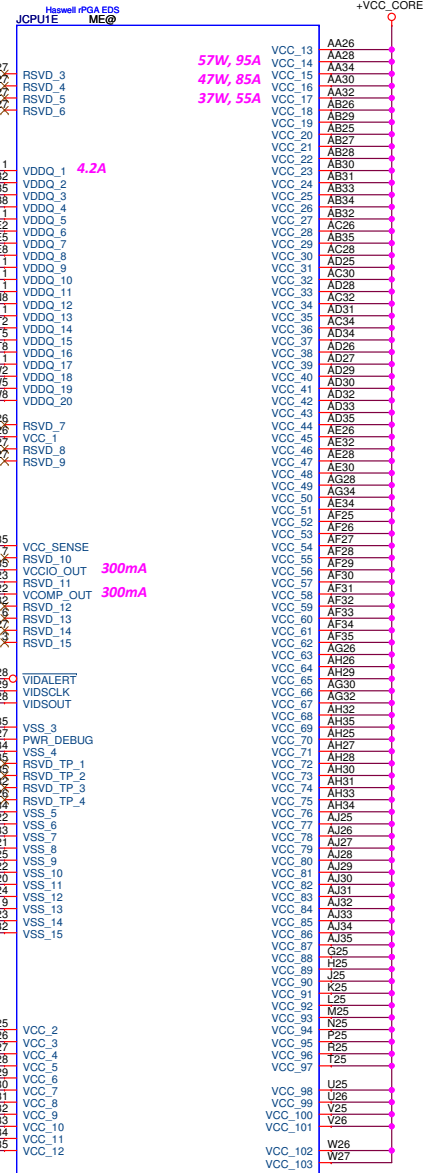
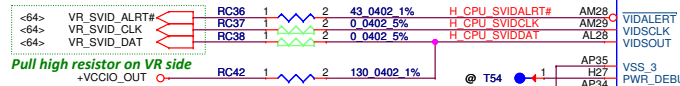
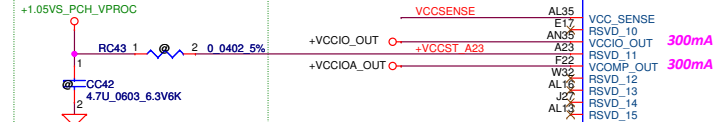
#### VDDQ Decoupling :

1. MB Bottom Socket Edge --> 2\* 330uf, 6mΩ
2. 6x MB Bottom Socket Cavity --> 11\* 22 µF (0805), 3mΩ  
5x MB Top Socket Cavity
3. 5x MB Bottom Socket Cavity --> 10 x 10 µF (0805), 3mΩ  
5x MB Top Socket Cavity

### VCC/VSS SENSE



#### Reserve for VCCST.

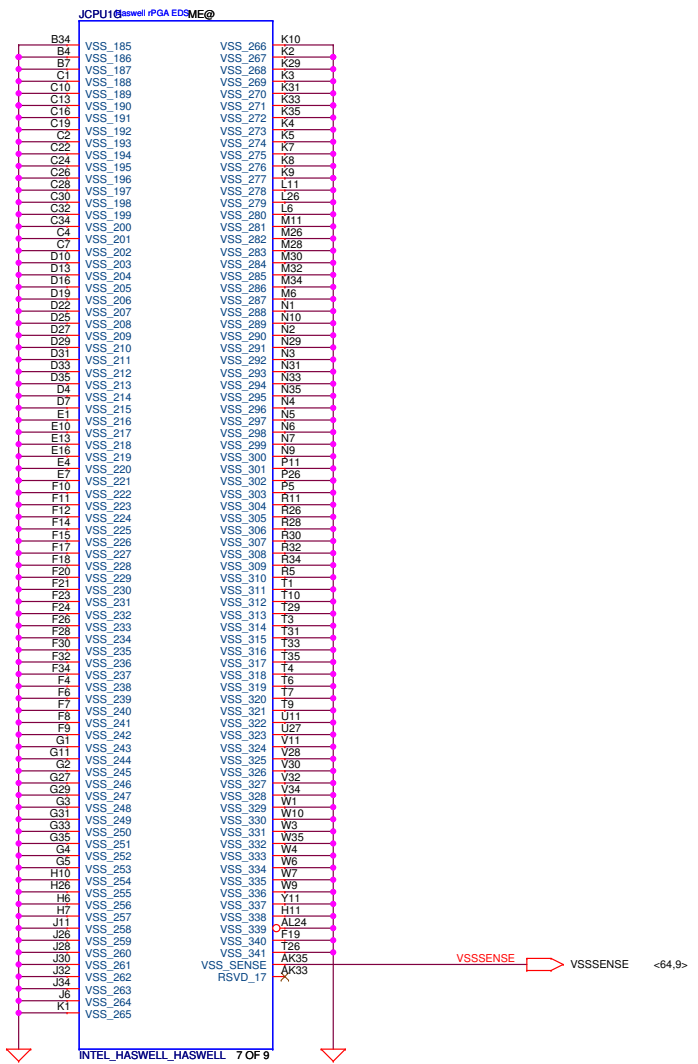
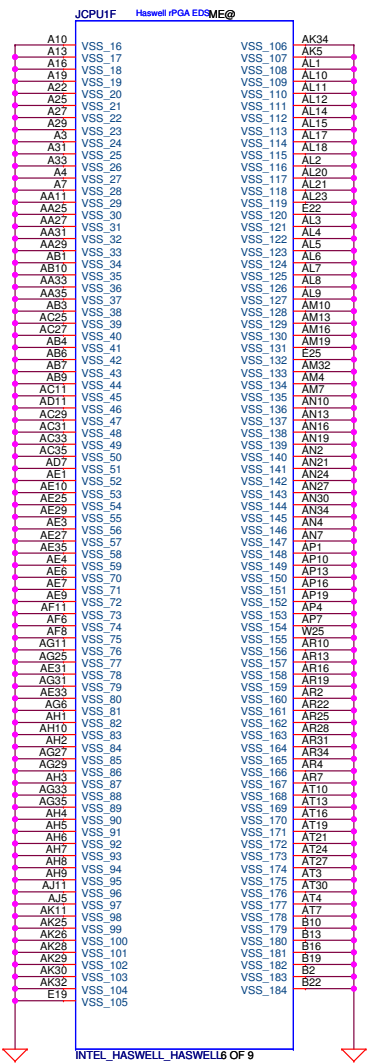


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Date: Thursday, July 11, 2013 Sheet 9 of 57

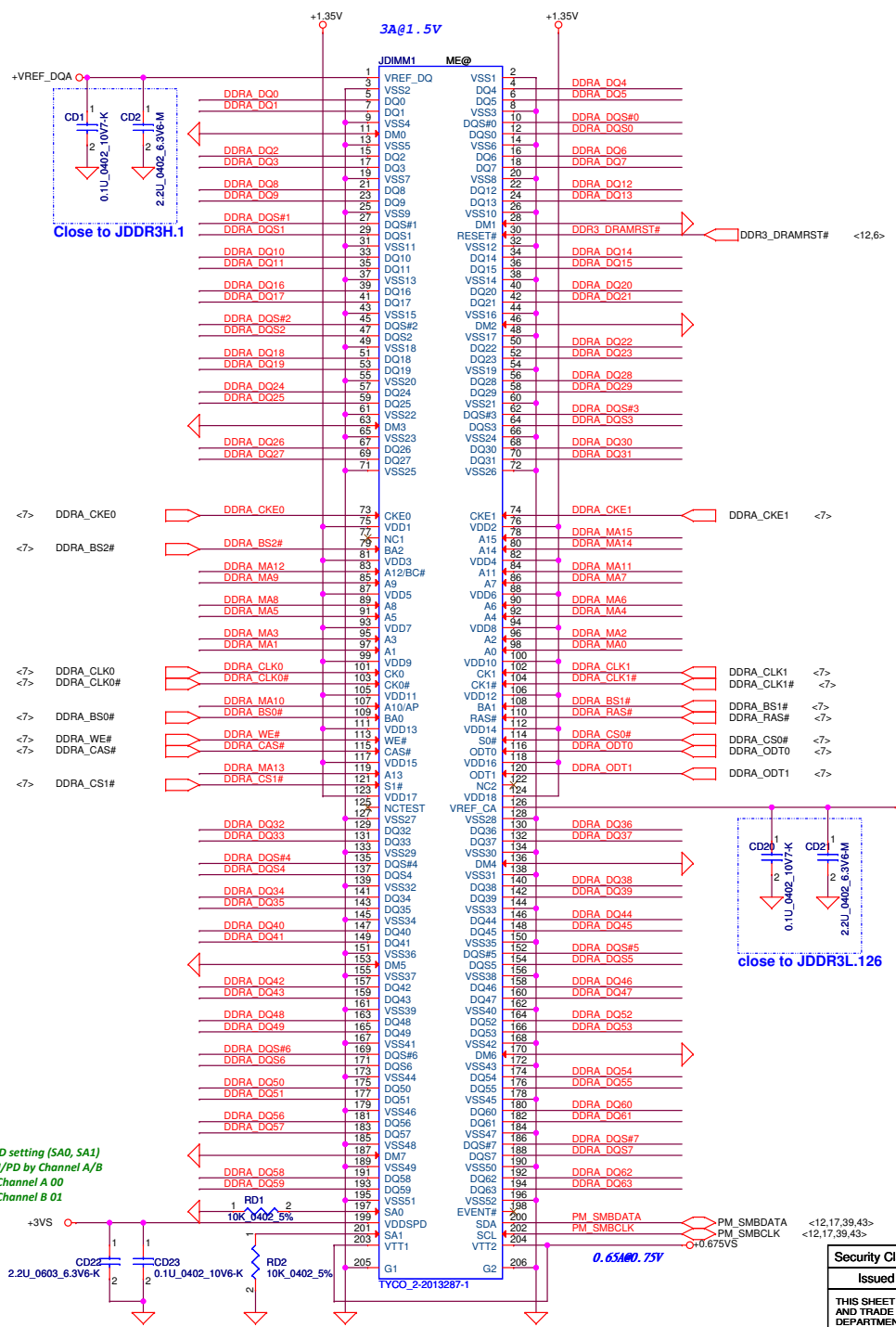


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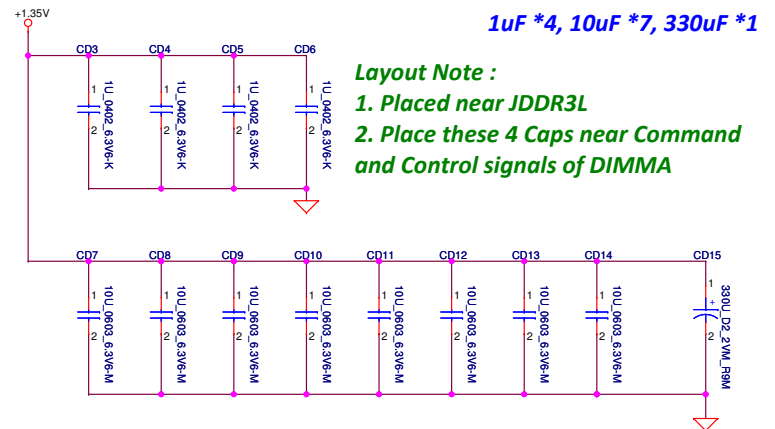
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CPU_GND		
Size Custom	Document Number	<b>E440 NM-A151</b>
Date: Thursday, July 11, 2013	Sheet 10 of 57	
Rev 1.0		

# DDR3 SO-DIMM A

- DDR4\_DQ[0..63] <-7>
- DDR4\_DQS[0..7] <-7>
- DDR4\_DQS# [0..7] <-7>
- DDR4\_MA[0..15] <-7>



## DDR Decoupling

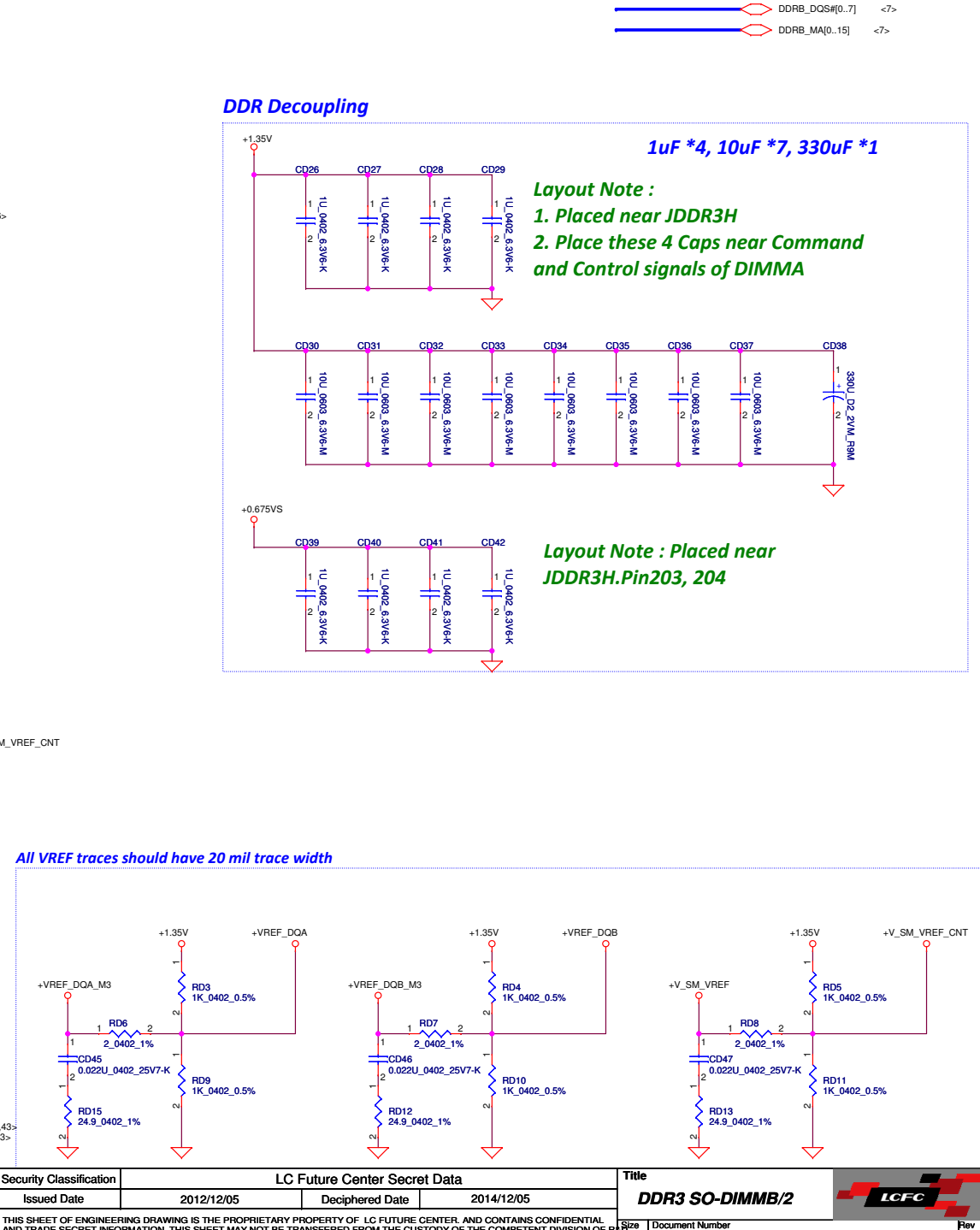
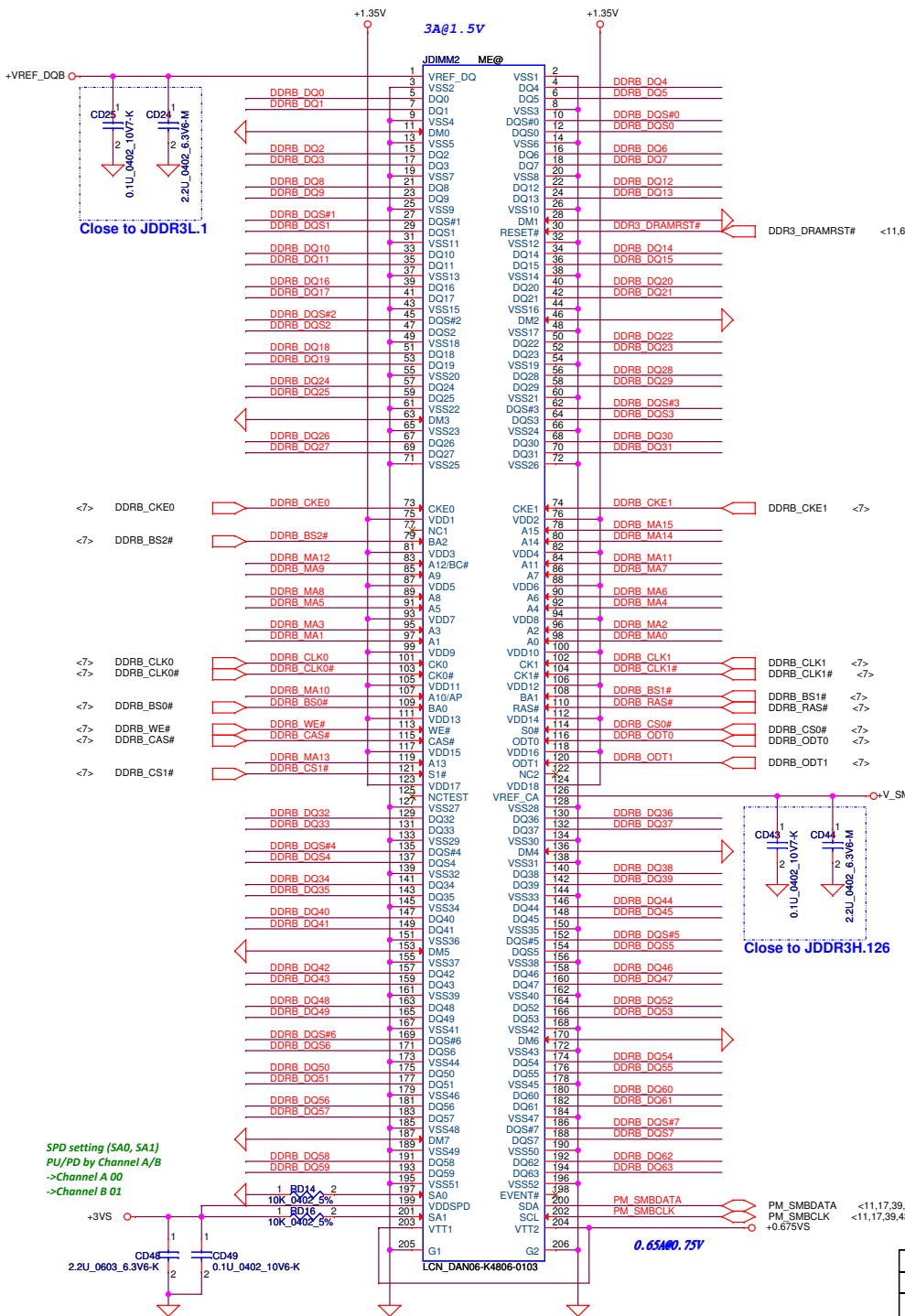
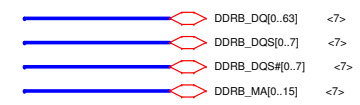


**Layout Note : Placed near JDDR3L1.Pin203, 204**

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DDR3 SO-DIMMA/1			
Size	Document Number	Rev	
Custom	<b>E440 NM-A151</b>	1.0	
Date:	Thursday, July 11, 2013	Sheet	11 of 57

# DDR3 SO-DIMM B



**Layout Note :**  
 1. Placed near JDDR3H  
 2. Place these 4 Caps near Command and Control signals of DIMMA

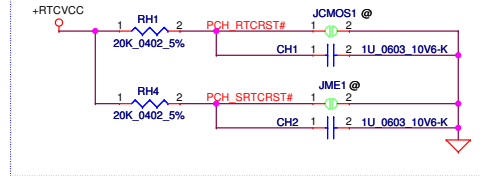
**Layout Note :** Placed near JDDR3H.Pin203, 204

All VREF traces should have 20 mil trace width

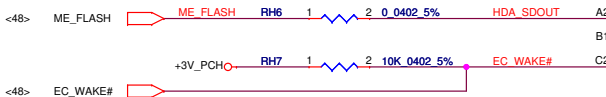
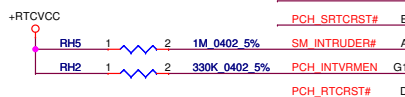
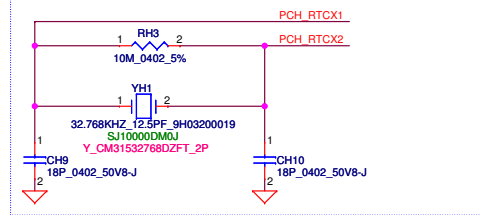
SPD setting (SA0, SA1)  
 PU/PD by Channel A/B  
 ->Channel A 00  
 ->Channel B 01

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Size	Document Number	Date:		Thursday, July 11, 2013		Rev 1.0	
Custom	E440 NM-A151	Sheet		12		of 57	

JCMOS, JME Setting, Need Under DDR Door

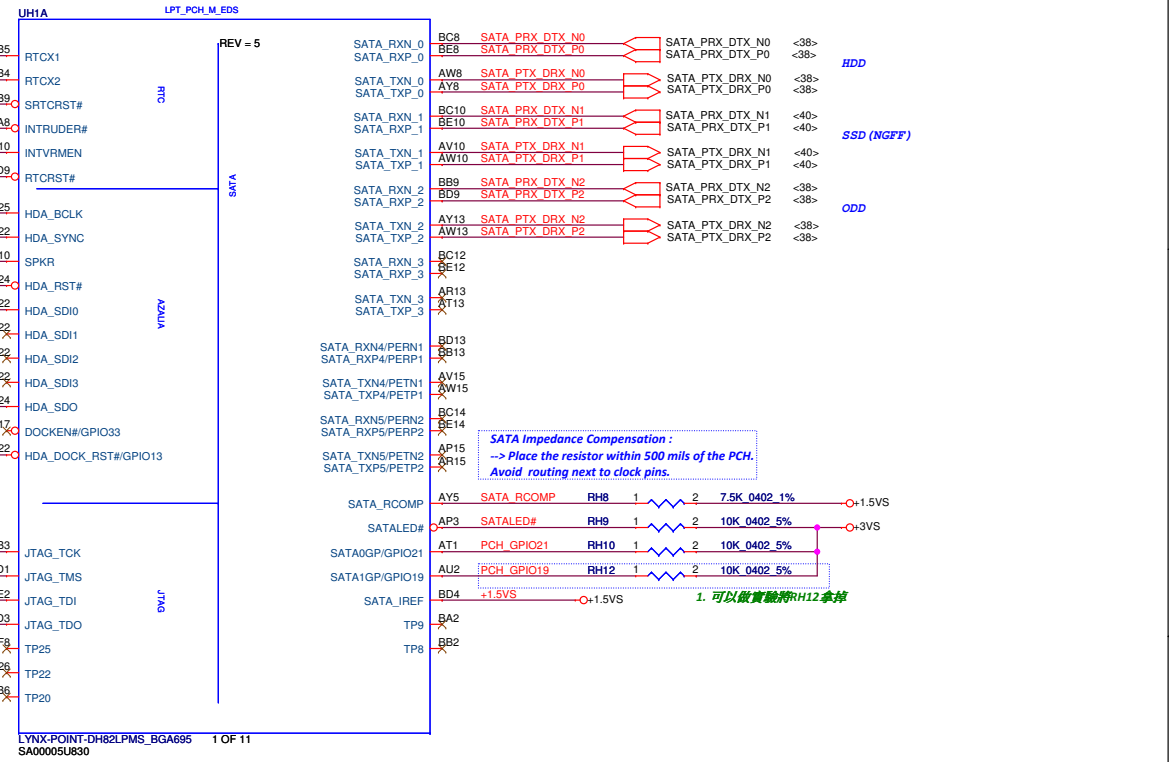


1. INTVRMEN, should always be pull high  
 \* H : Integrated VRM enable (Default)  
 L : Integrated VRM disable
2. Internal Voltage Regulator Enable:  
 This signal enables the internal 1.05 V regulators.



During Reset", Immediately after Reset and S3/S4/S5  
 1. JTAG\_TDI, JTAG\_TMS --> Int. PU 20K  
 2. JTAG\_TCK --> Int. PD 20K  
 3. JTAG\_TDO --> High-Z

- @T64 1 PCH\_JTAG\_TCK AB3
- @T65 1 PCH\_JTAG\_TMS AD1
- @T66 1 PCH\_JTAG\_TDI AE2
- @T67 1 PCH\_JTAG\_TDO AD3

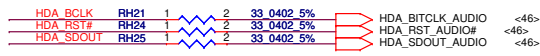


SATA Impedance Compensation :  
 --> Place the resistor within 500 mils of the PCH.  
 Avoid routing next to clock pins.

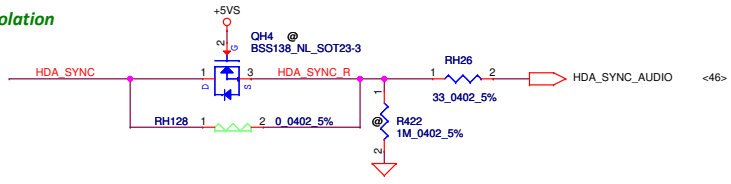
1. 可以做實驗將RH12拿掉

HDA AUDIO SIGNAL

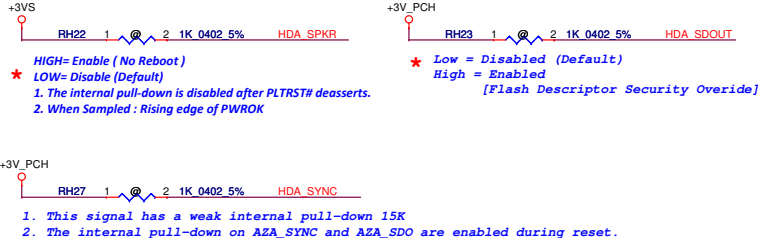
HDA AUDIO For Codec



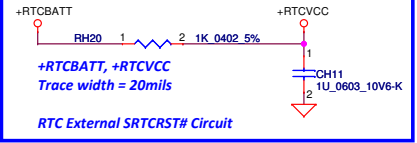
Isolation



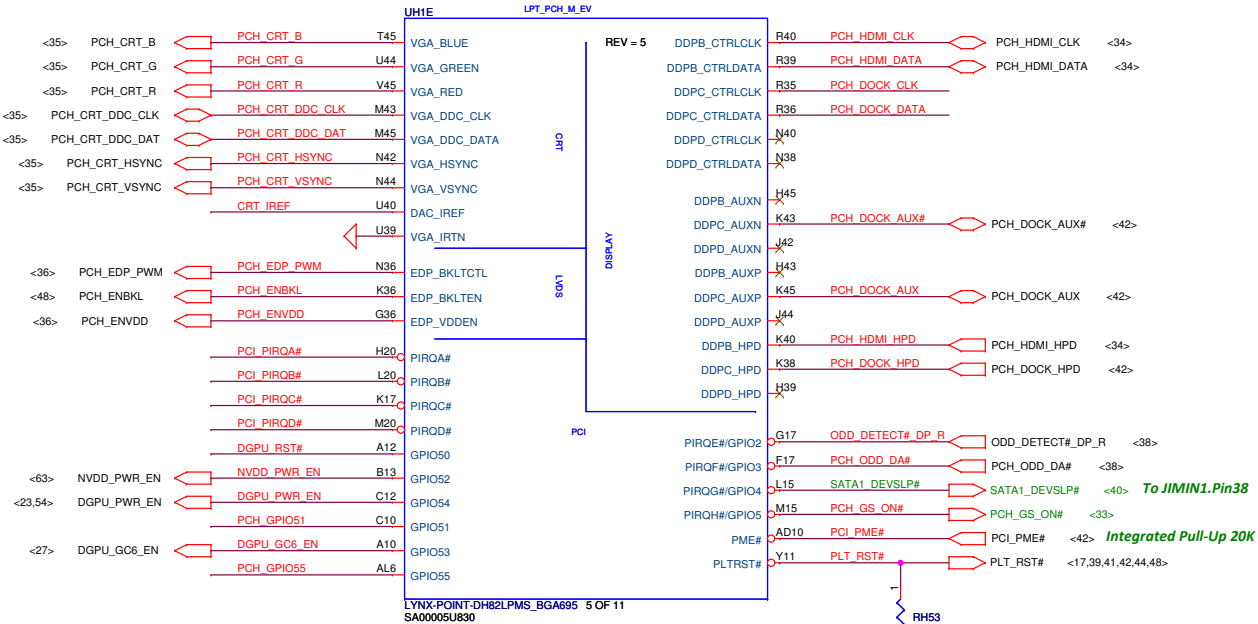
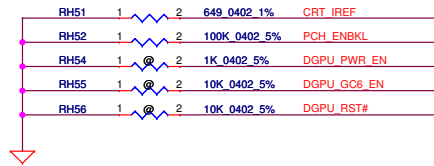
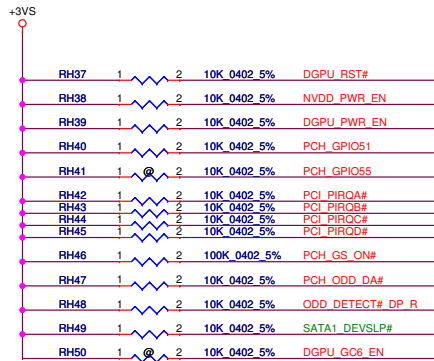
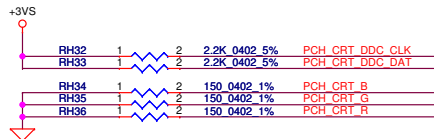
HDA STRAP



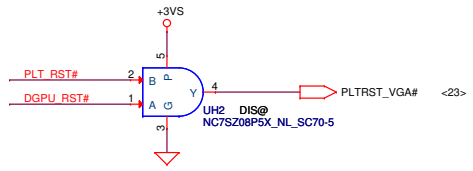
RTCVCV Circuit



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Custom	E440	NW-A151	
Date:	Thursday, July 11, 2013	Sheet	13 of 57



+VGA\_CORE  
+3VS\_VGA



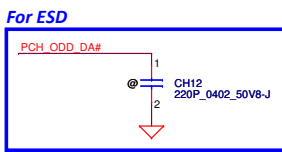
A16 swap override Strap/Top-Block Swap Override jumper

PCI_GNT3#	Low = A16 swap override/Top-Block Swap Override enabled * **High=Default
-----------	---

1. The signal has a weak internal pull-up, which is disabled after PLTRST# deasserts.  
2. When sampled : Rising edge of PWROK

**Boot BIOS Straps (BBS)**

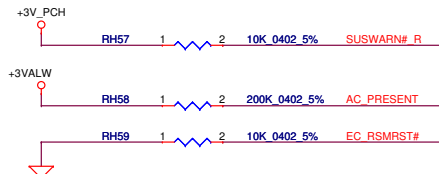
BBS_BIT1 (GPIO51)	BBS_BIT0 (GPIO19)	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI *



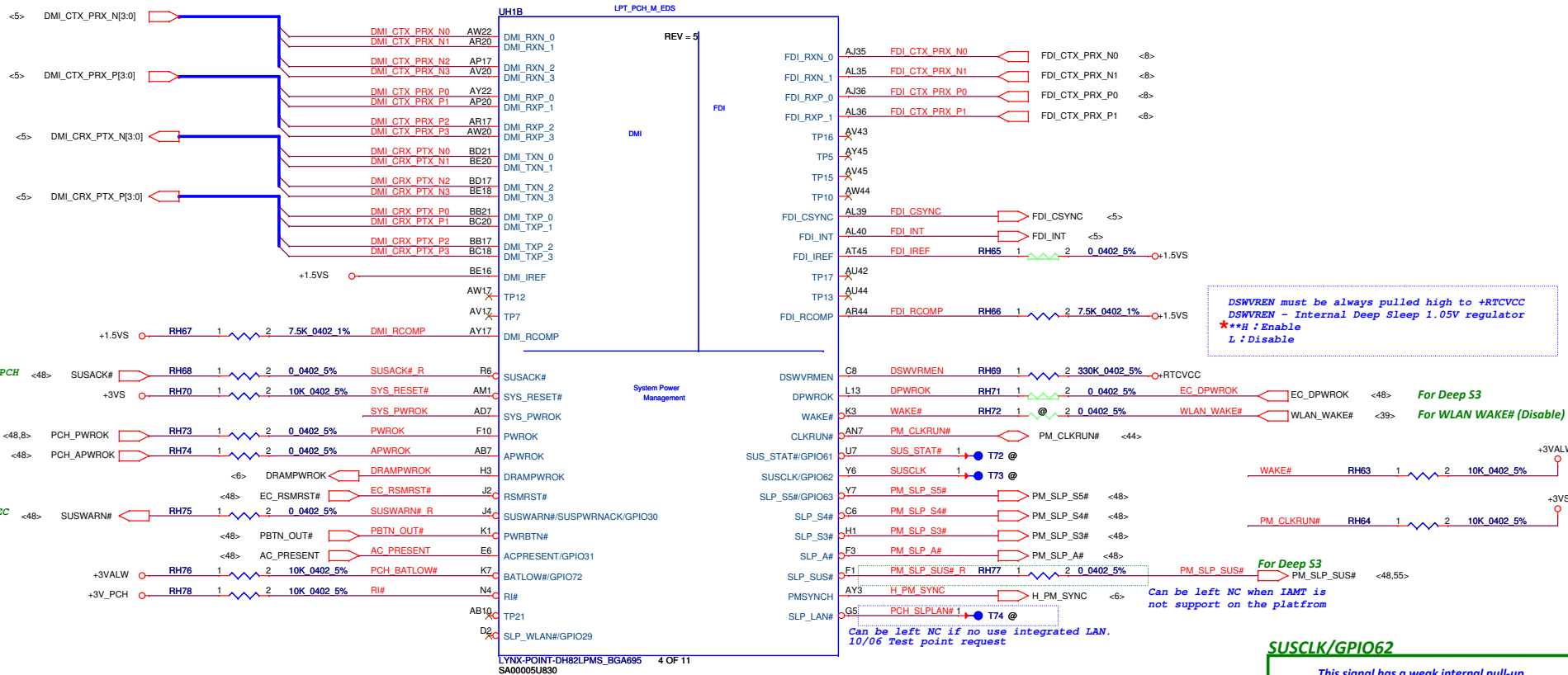
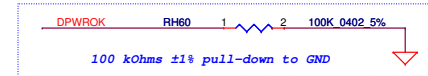
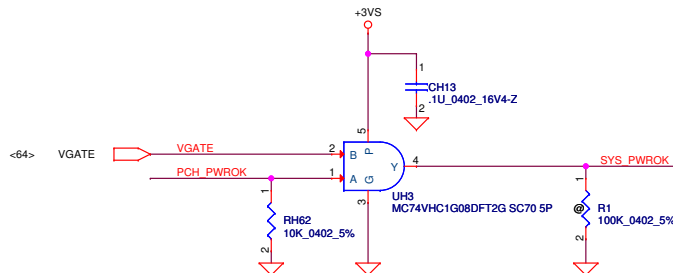
- GPIO51/19 has weak internal pull-up via 20kohm
- The internal pull-up is disabled after PLTRST# deasserts.
- GPIO51 (bit 11) at the rising edge of PWROK SATA1GP/GPIO19 (bit 10) at the rising edge of PWROK.

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Size	Document Number	Rev
Custom	<b>E440 NM-A151</b>	1.0
Date:	Thursday, July 11, 2013	Sheet 14 of 57



SUSACK# R RH61 1 @ 2 0.0402 5% SUSWARN# R  
 Stuff RH289 if EC does not want to involve in the handshake mechanism for the DeepSX state entry and exit



APWROK may come up earlier than PWROK but no later

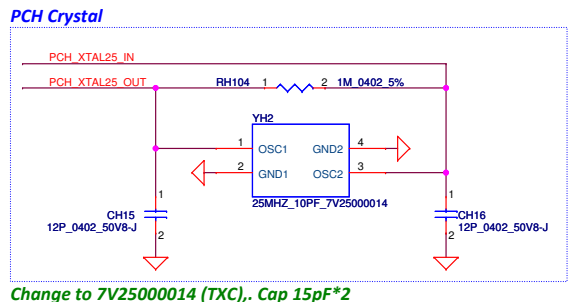
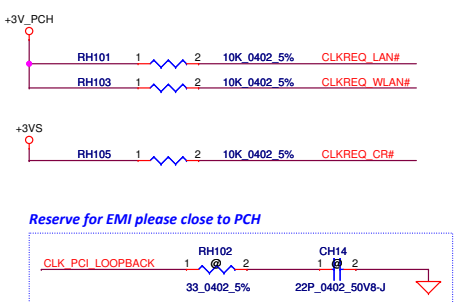
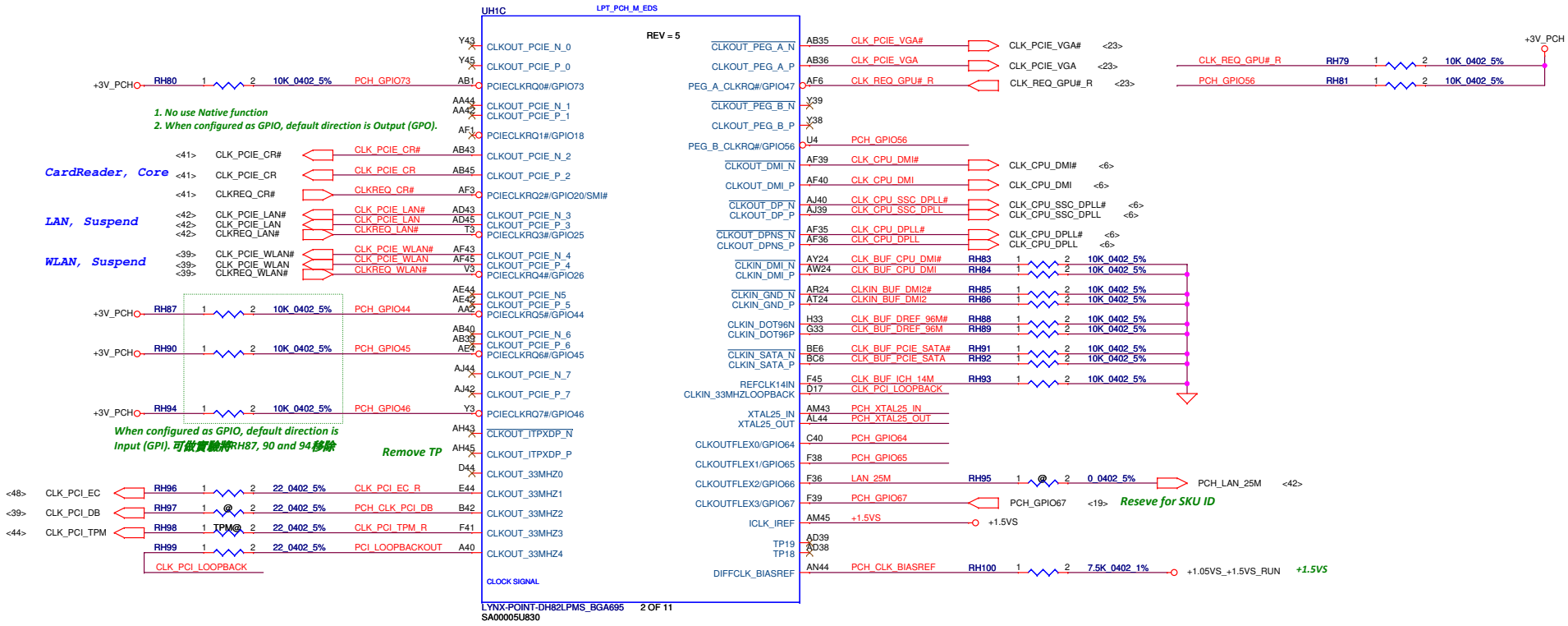
APWROK only for A phase



**SUSCLK#/GPIO62**  
 This signal has a weak internal pull-up.  
 0 = Disable PLL On-Die voltage regulator.  
 \* 1 = Enable PLL On-Die voltage regulator.  
 NOTES:  
 1. The internal pull-up is disabled after RSMRST# deasserts.  
 2. This signal is in the Suspend well.

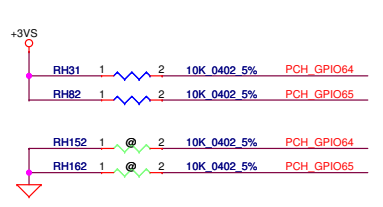
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Title		LCFC	
PCH_DMI/FDI/PM		E440 NM-A151	
Size Custom	Document Number	Date: Thursday, July 11, 2013	Rev 1.0
		Sheet 15	of 57



**Project Phase ID**

Project Phase	PCH_GPIO64	PCH_GPIO65
SDV, FVT	0	0
SIT2 (R 0.5)	0	1
SIT (R 0.4)	1	0
* SVT	1	1



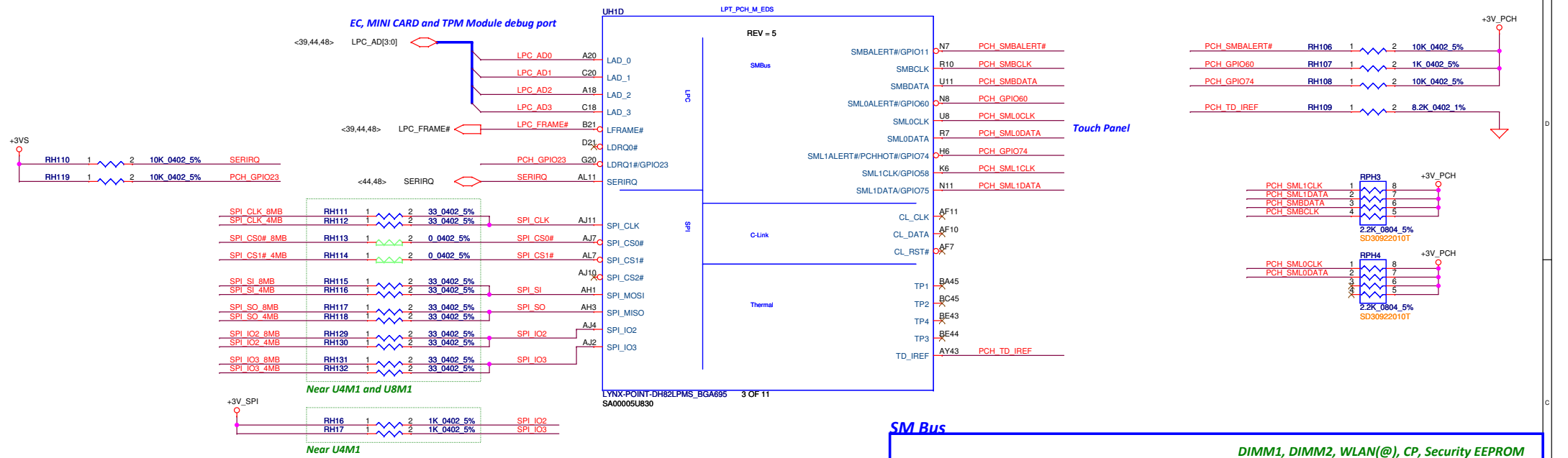
Security Classification	LC Future Center Secret Data	
Issued Date	2012/12/05	Deciphered Date 2014/12/05

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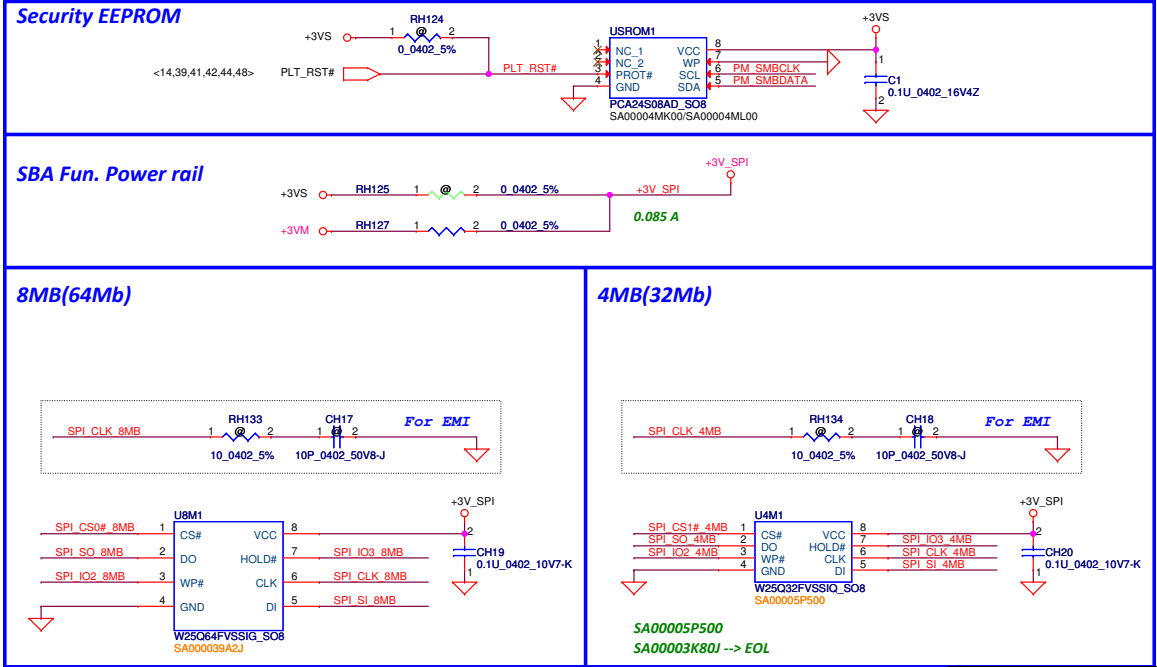
**Title**  
PCH\_PCIE/CLK

**Size** Custom  
**Document Number** E440 NM-A151  
**Date** Thursday, July 11, 2013  
**Sheet** 16 of 57  
**Rev** 1.0

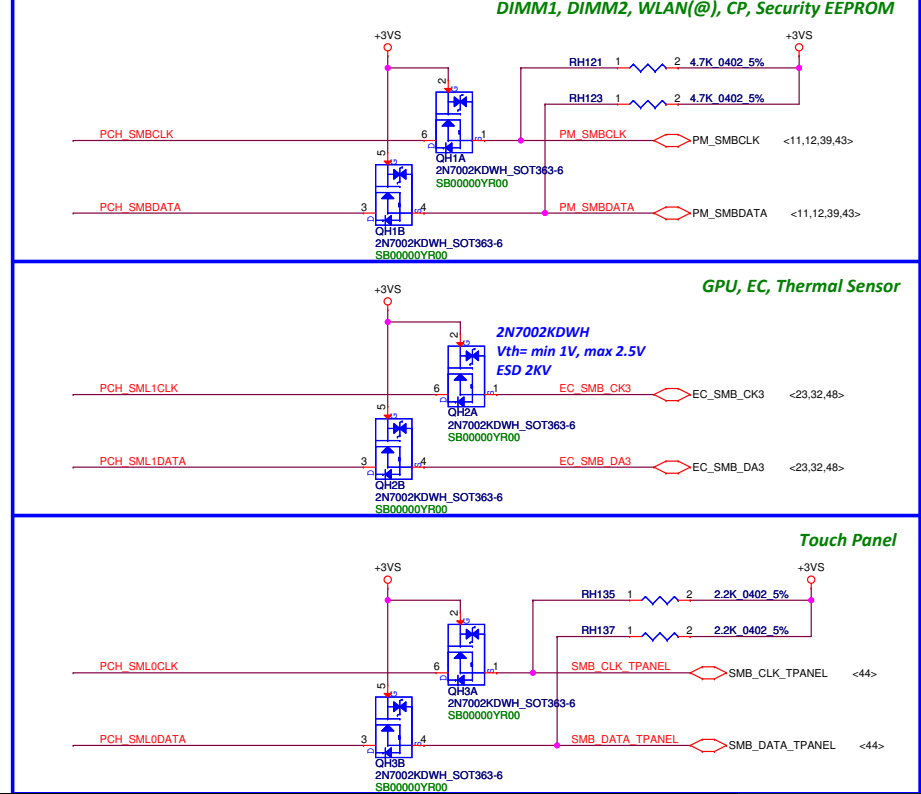




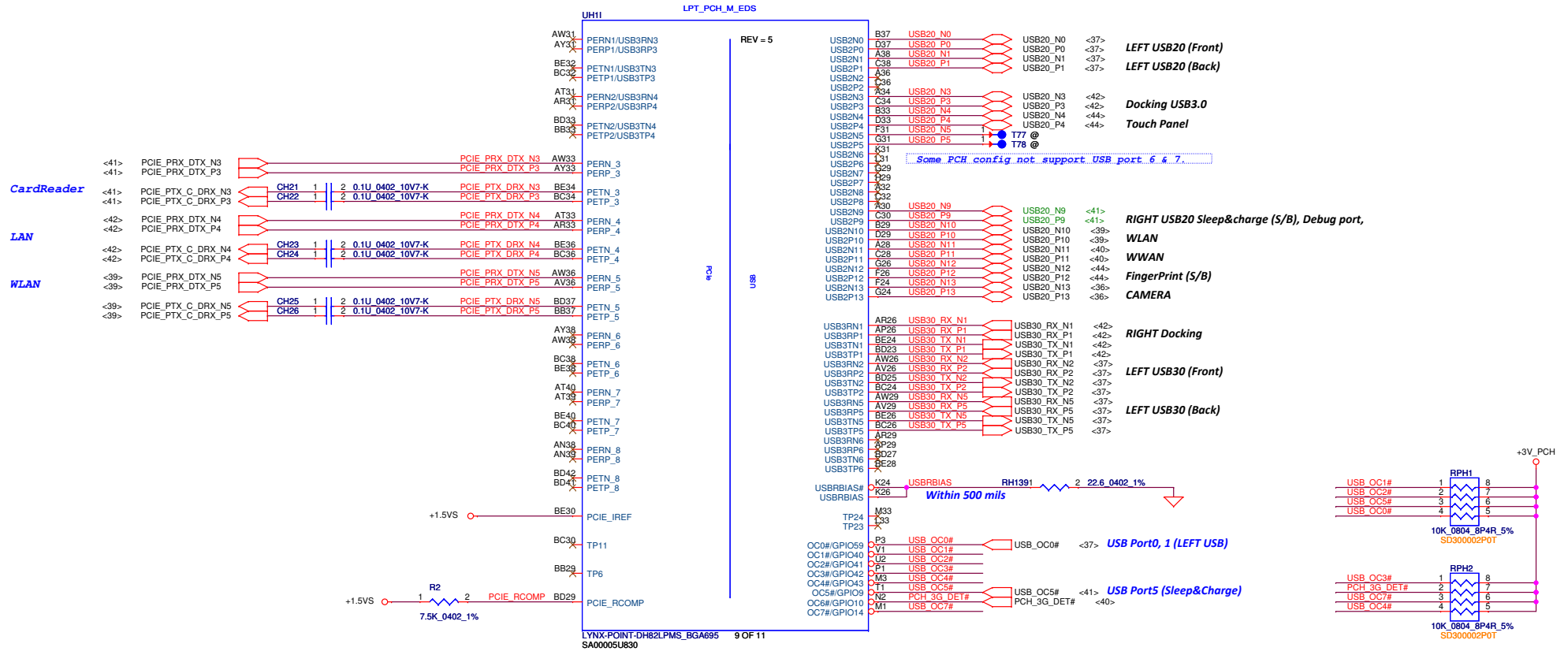
**8MB + 4MB SPI ROM, 5MB ME(SBA), Security EEPROM**



**SM Bus**



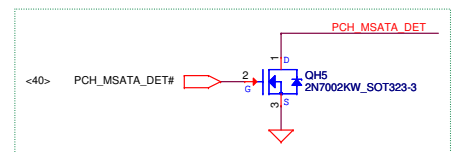
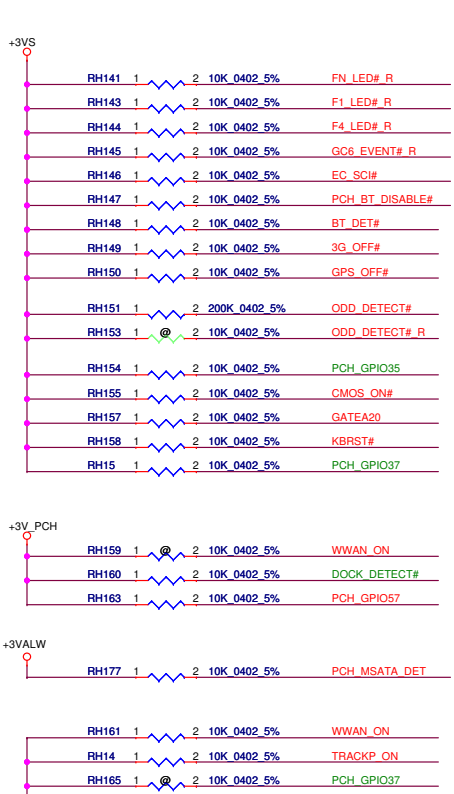
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Size	Document Number	Rev	
Custom	E440	NW-A151	
Date:	Thursday, July 11, 2013	Sheet	17 of 57



**USB2.0 :**  
**OC#0-3 --> Port 0-7**  
**OC#4-7 --> Port 8-13**

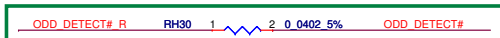
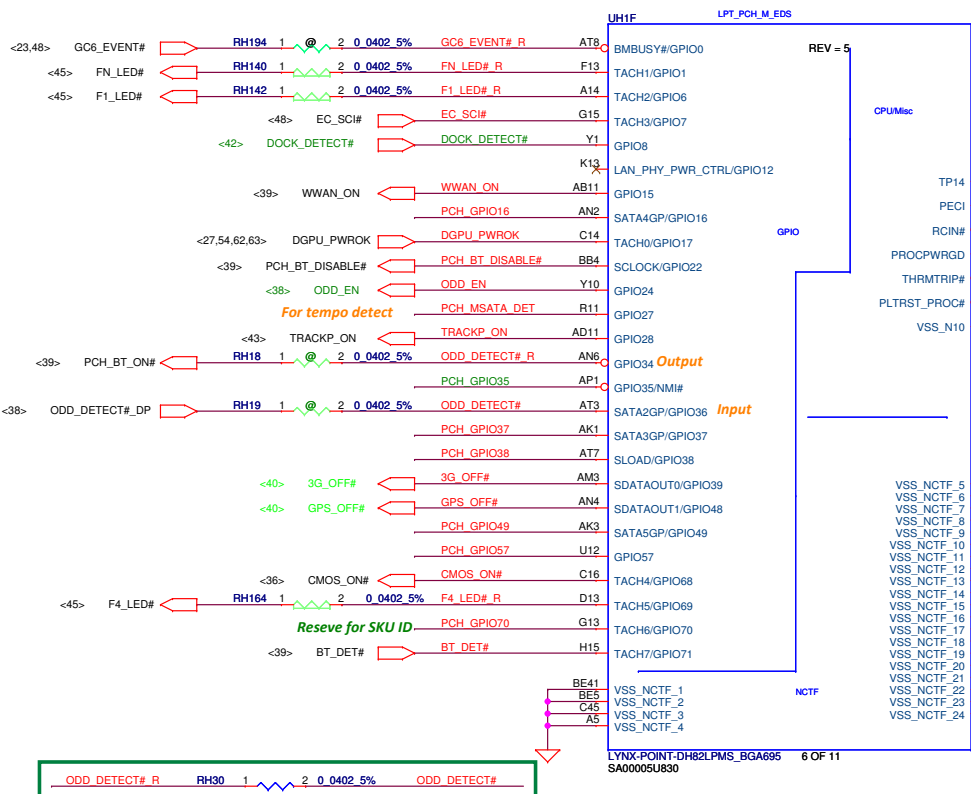
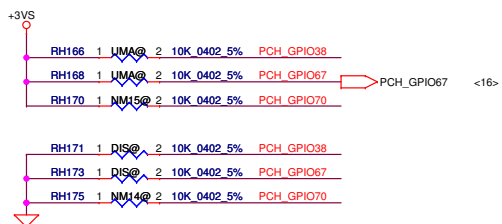
**OC[3:0]# should be connected with USB 2.0 ports 0 - 7 and any 4 of USB 3.0 ports 1 - 6.**

USB3.0	USB2.0	OC#	Note
Port1	Port3	X	Docking (Right)
Port2	Port0	OC0#	LEFT USB (Front)
Port5	Port1	OC0#	LEFT USB (Back)
X	Port9	OC5#	Sleep&Charge (Right)

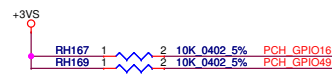


**SKU ID**

Function	PCH_GPIO38	PCH_GPIO67	PCH_GPIO70
* Optimus	0	0	
Reserve	0	1	
DIS	1	0	
* UMA	1	1	
* 14"			0
* 15"			1



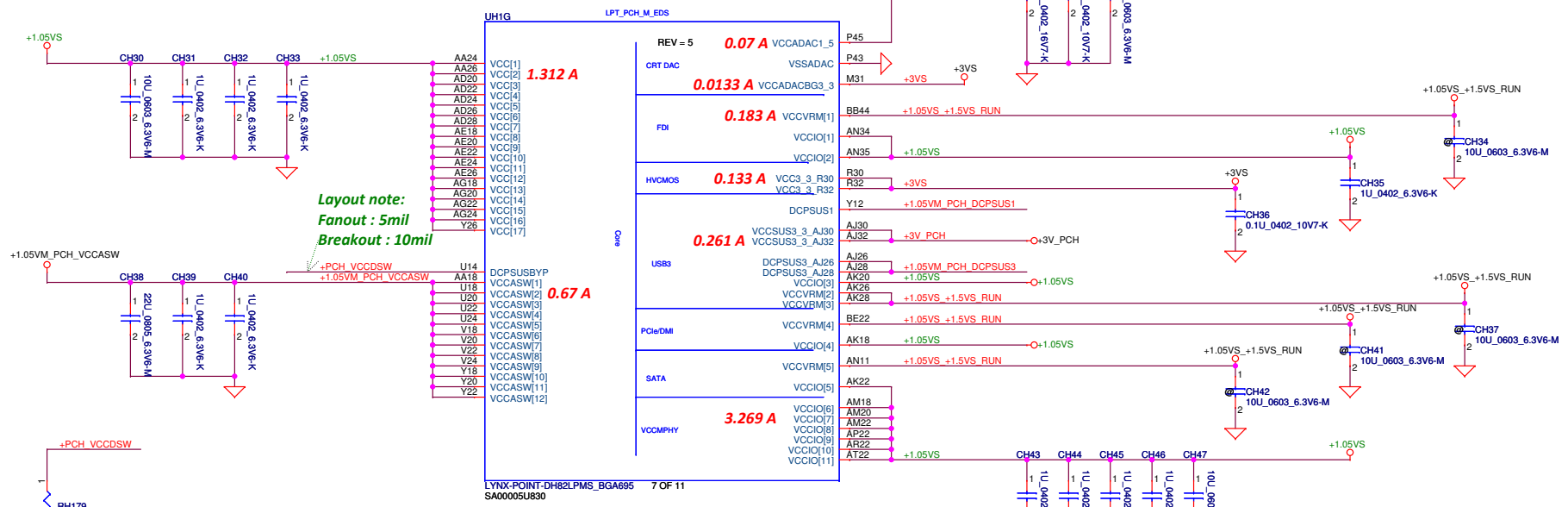
CONFIG	GPIO16, 49
* USB X4,PCIEX8,SATAx6	11
USB X6,PCIEX8,SATAx4	01



No use Flexible I/O pin, delete RH172, RH174

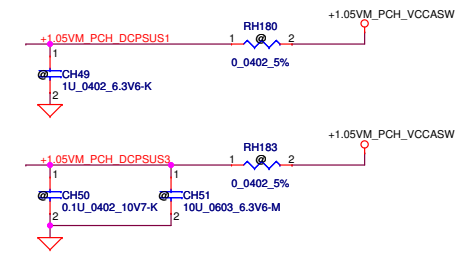
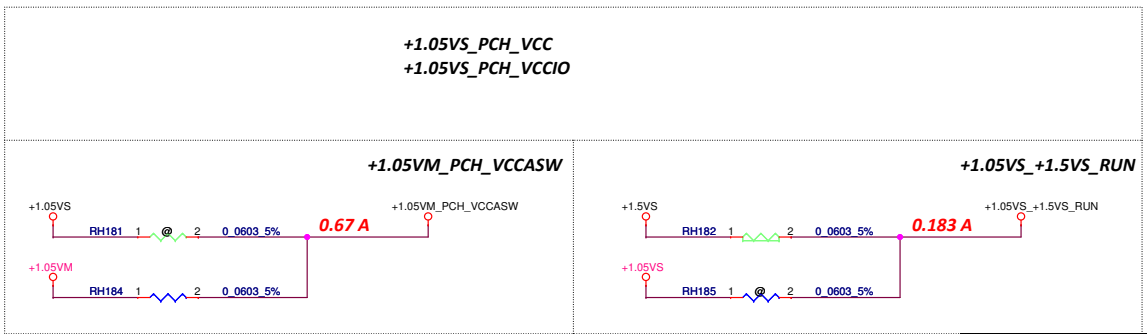
Fixed Signals				Muxed Signals		Fixed Signals								Muxed Signals		Fixed Signals				
USB3 1	USB3 2	USB3 5	USB3 6	PCIE 1	PCIE 2	PCIE 3	PCIE 4	PCIE 5	PCIE 6	PCIE 7	PCIE 8	PCIE 9	PCIE 10	SATA 4	SATA 5	SATA 0	SATA 1	SATA 2	SATA 3	
				(00)	(00)									(00)	(00)					
				USB3 3	USB3 4									PCIE 1	PCIE 2					
				(01)	(01)									(01)	(01)					

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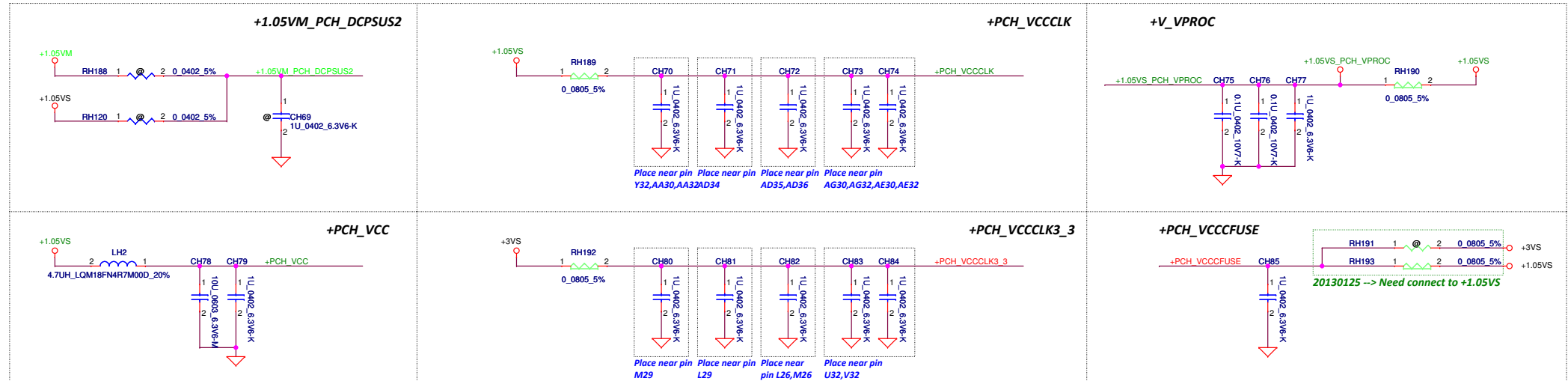
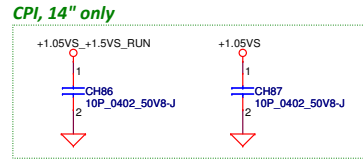
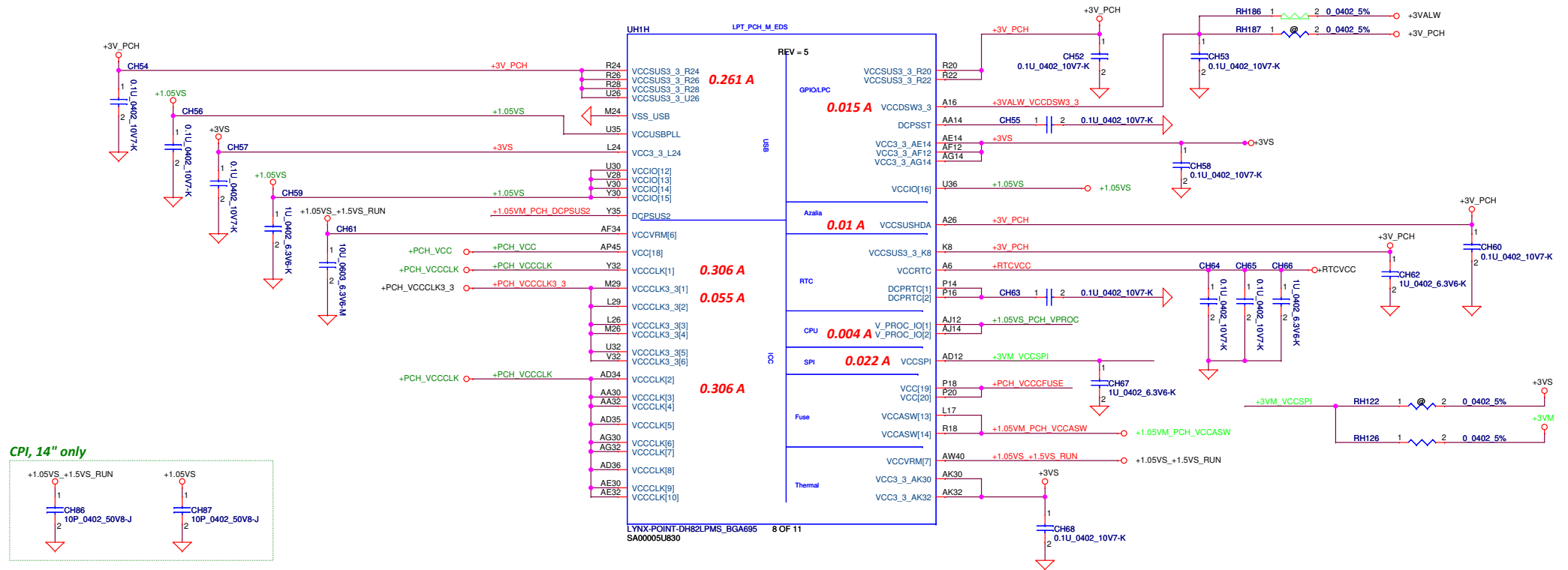
Layout note:  
Fanout : 5mil  
Breakout : 10mil

PCH Power Rail Table (EDS Rev1.0)		
Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	1.05V	1.312 A
VCCIO	1.05V	3.629 A
VCCADAC1_5	1.5V	0.07 A
VCCADAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.183 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A

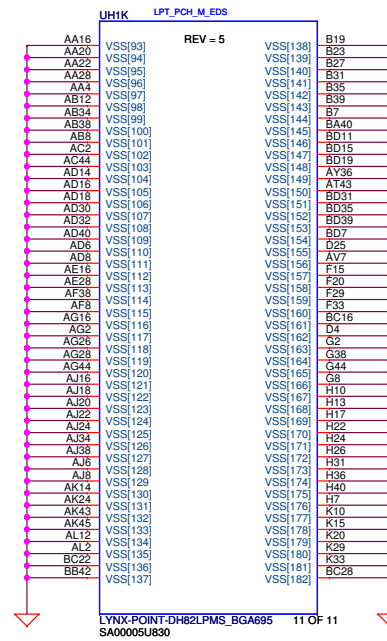
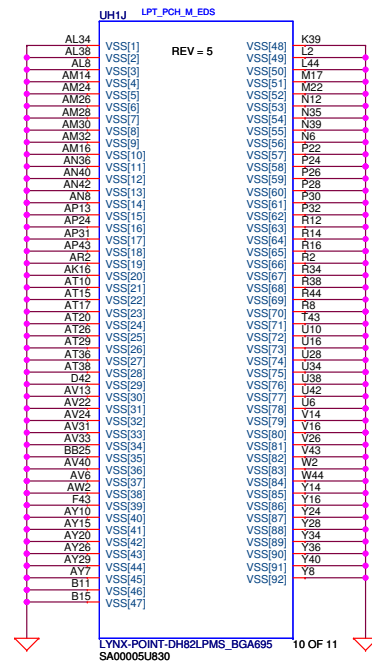


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Date:	Thursday, July 11, 2013	Sheet 20 of 57

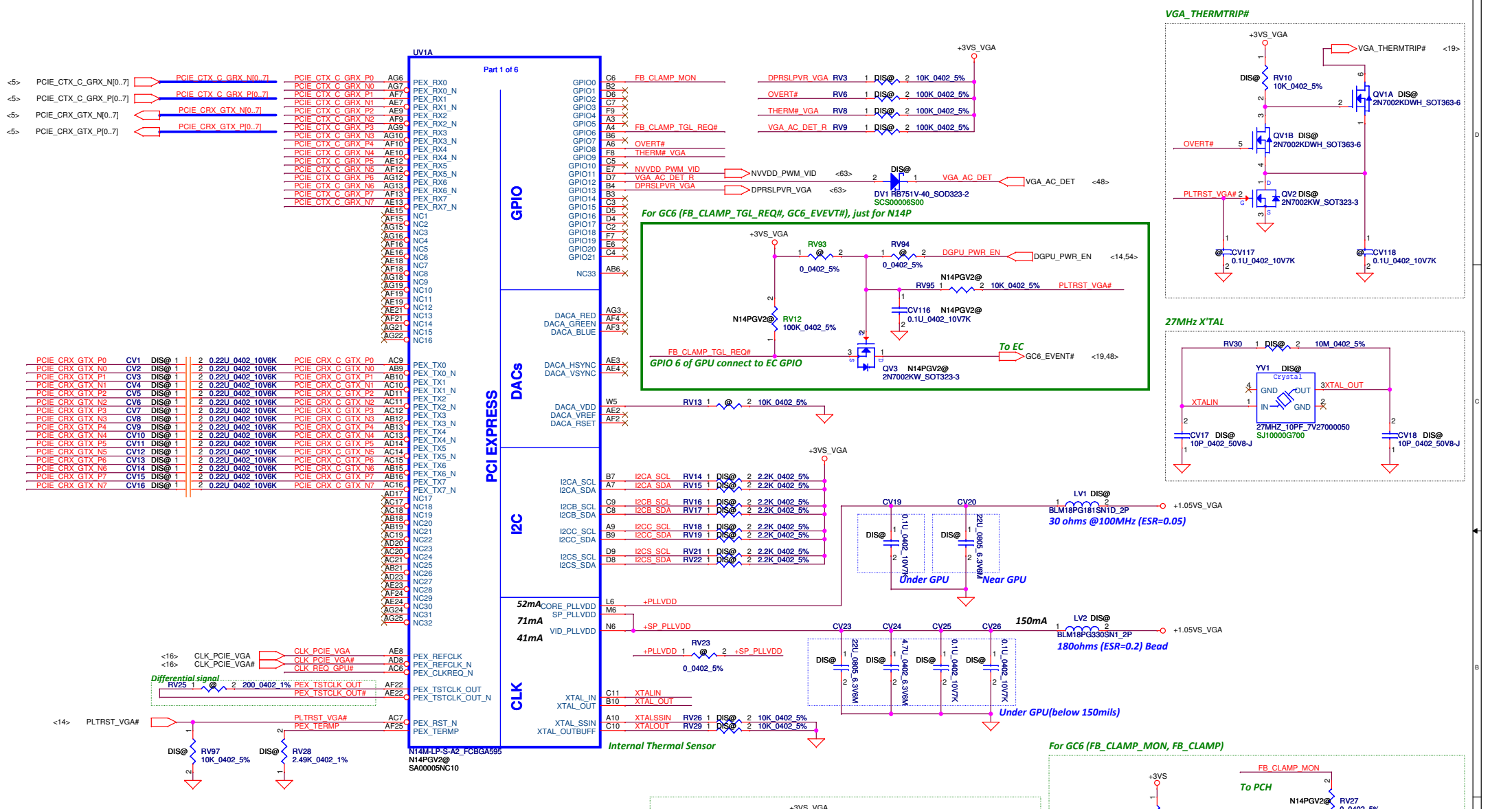


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Size	Document Number	Rev	
Custom	<b>E440 NM-A151</b>	1.0	
Date:	Thursday, July 11, 2013	Sheet	21 of 57

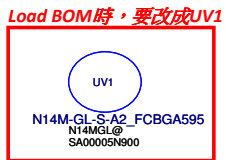


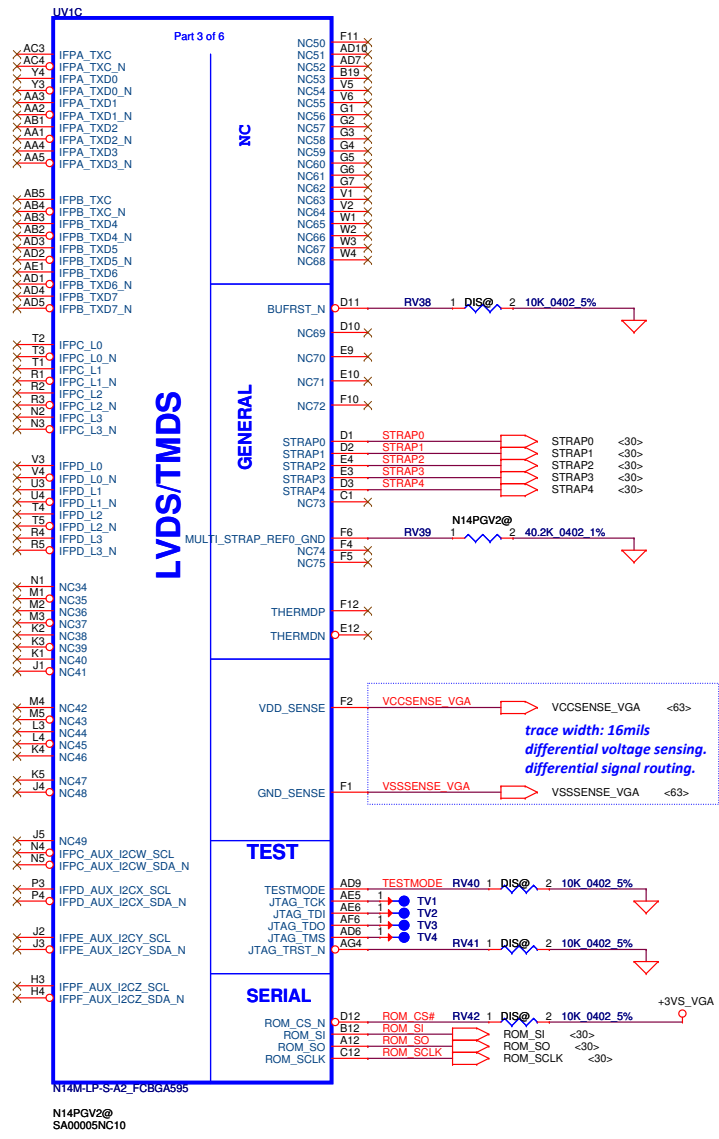
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Issued Date	2012/12/05	Deciphered Date	2014/12/05
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			Rev 1.0





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Size	Custom	Document Number	E440 NM-A151
Date:	Thursday, July 11, 2013	Sheet	23 of 57

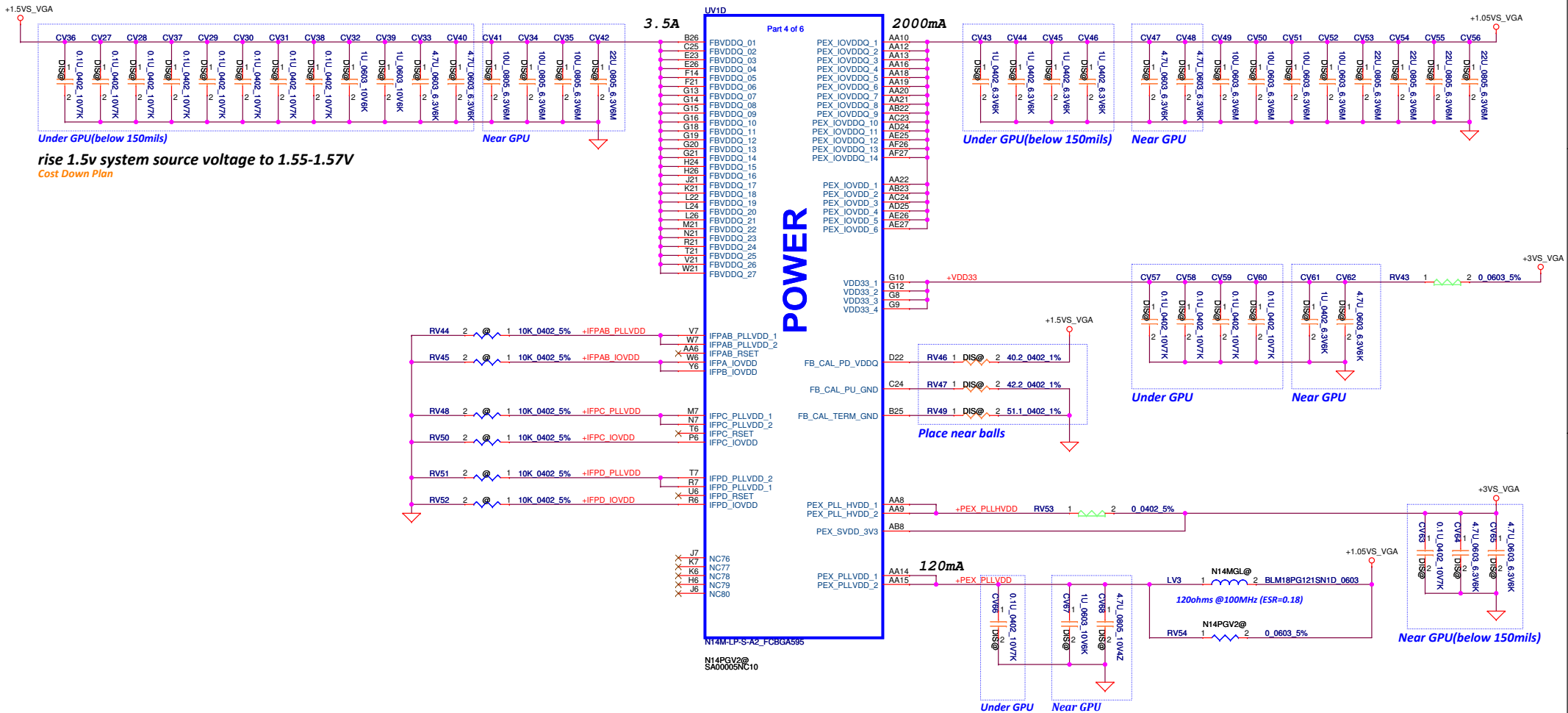




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Title		
N14P_SPI ROM/SENSE		
Size	Document Number	<b>E440 NM-A151</b>
Custom		
Date:	Thursday, July 11, 2013	Sheet 24 of 57
Rev	1.0	



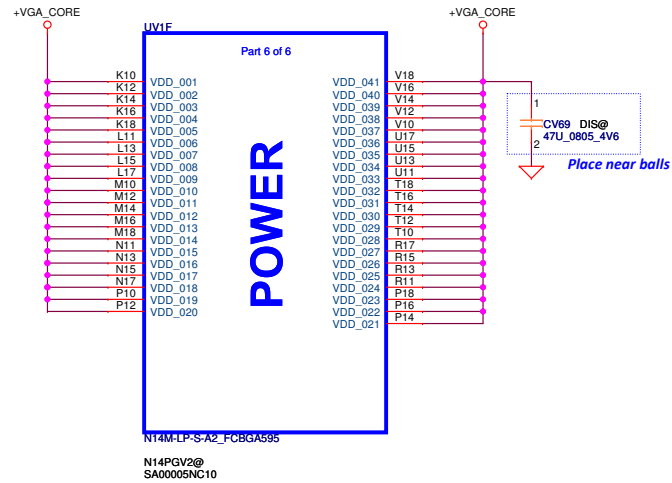
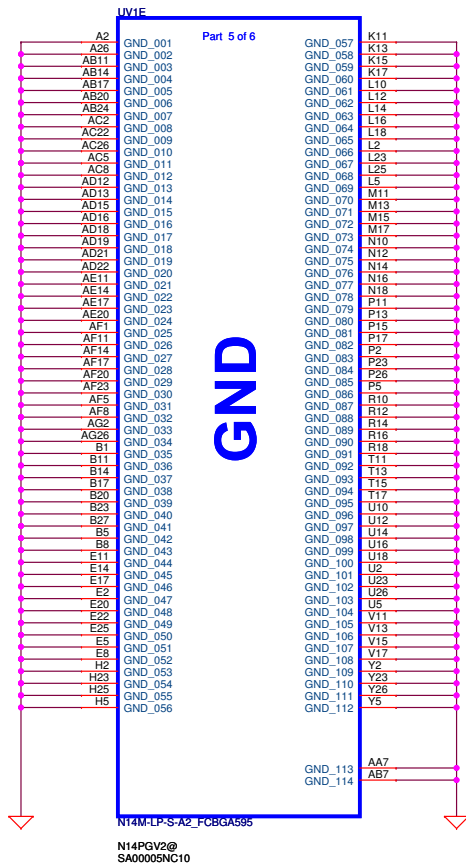


Under GPU (below 150mils)  
 rise 1.5v system source voltage to 1.55-1.57V  
 Cost Down Plan

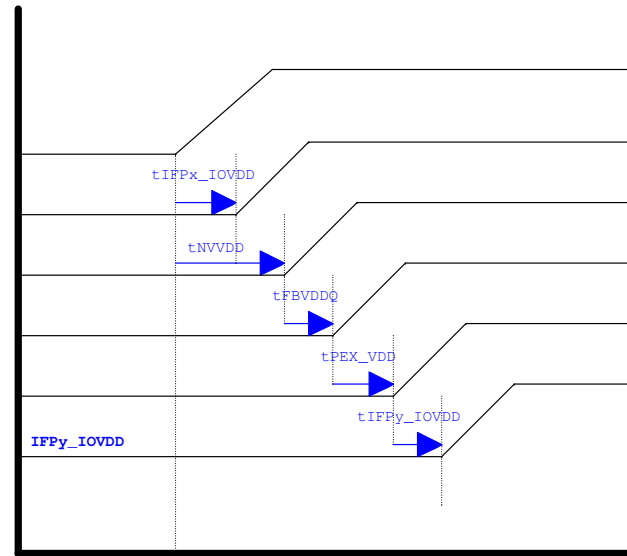
CALIBRATION PIN	DDR3
FB_CAL_x_PD_VDDQ	40.2Ohm
FB_CAL_x_PU_GND	42.2Ohm
FB_CAL_xTERM_GND	51.10Ohm

Security Classification	LC Future Center Secret Data	
Issued Date	2012/12/05	Deciphered Date 2014/12/05
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Title	N14P_POWER	
Size	Document Number	Rev
Custom	E440 NM-A151	1.0
Date:	Thursday, July 11, 2013	Sheet 25 of 57



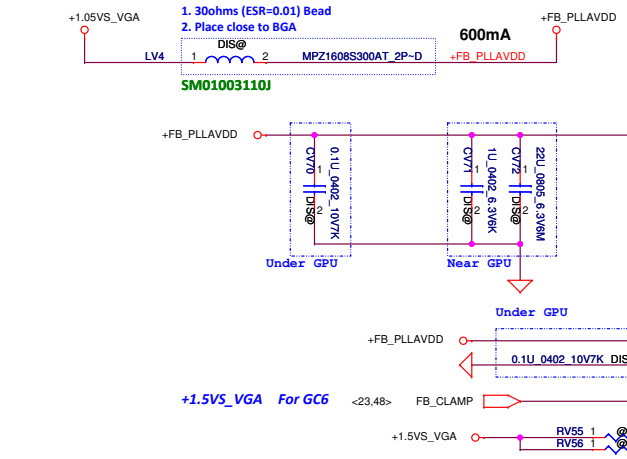
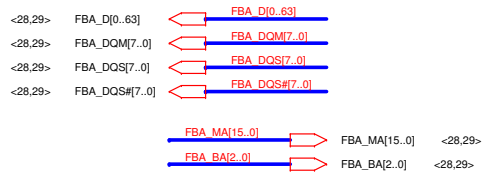
VDD33 (+3VS\_VGA)  
 IFPx\_IOVDD  
 NVVDD (+VGA\_CORE)  
 FBVDDQ (+1.5VS\_VGA)  
 PEX\_VDD (+1.05VS\_VGA)



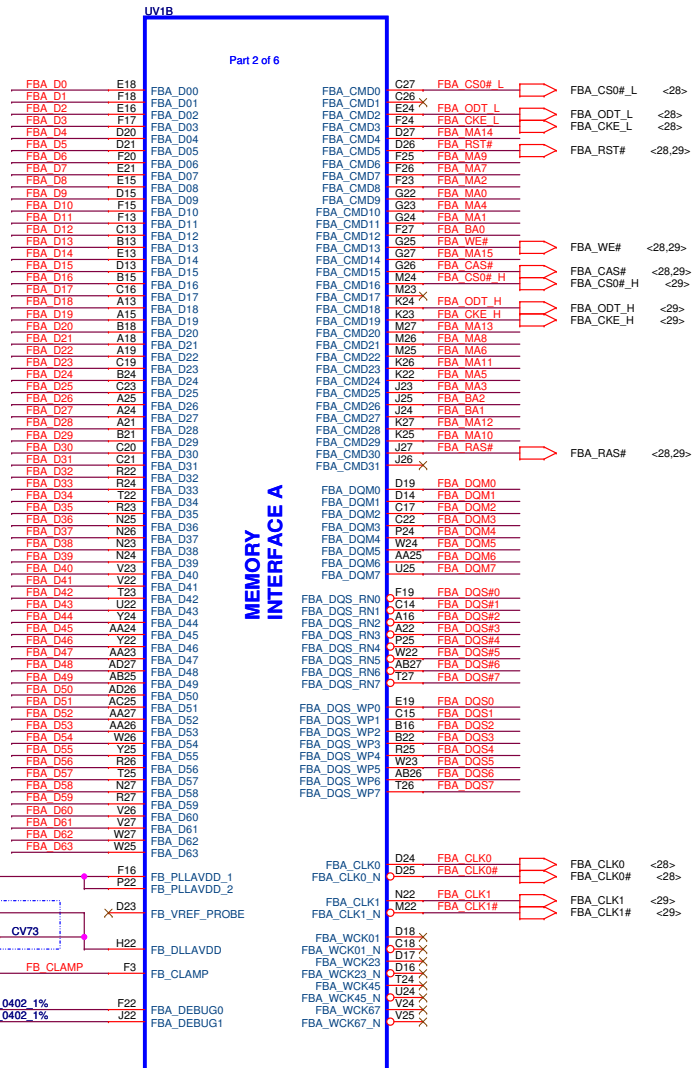
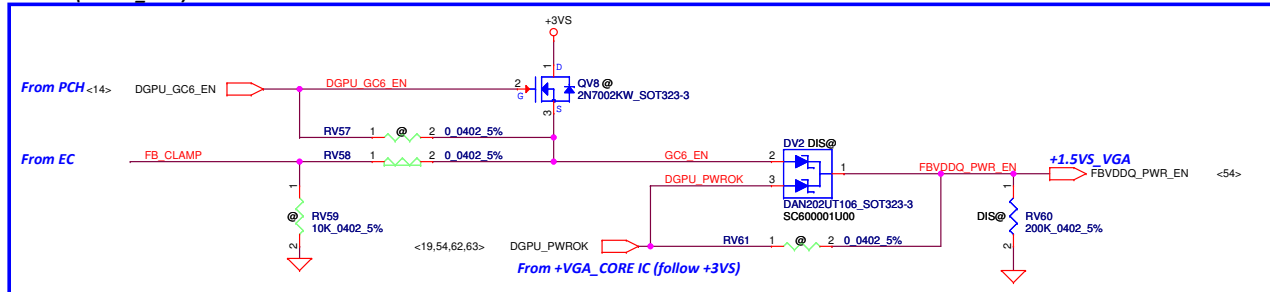
### NV Recommended Power On Sequencing Order

X=A and B  
 Y=C, D, E and F

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				Custom		
				Date:	Thursday, July 11, 2013	Sheet 26 of 57



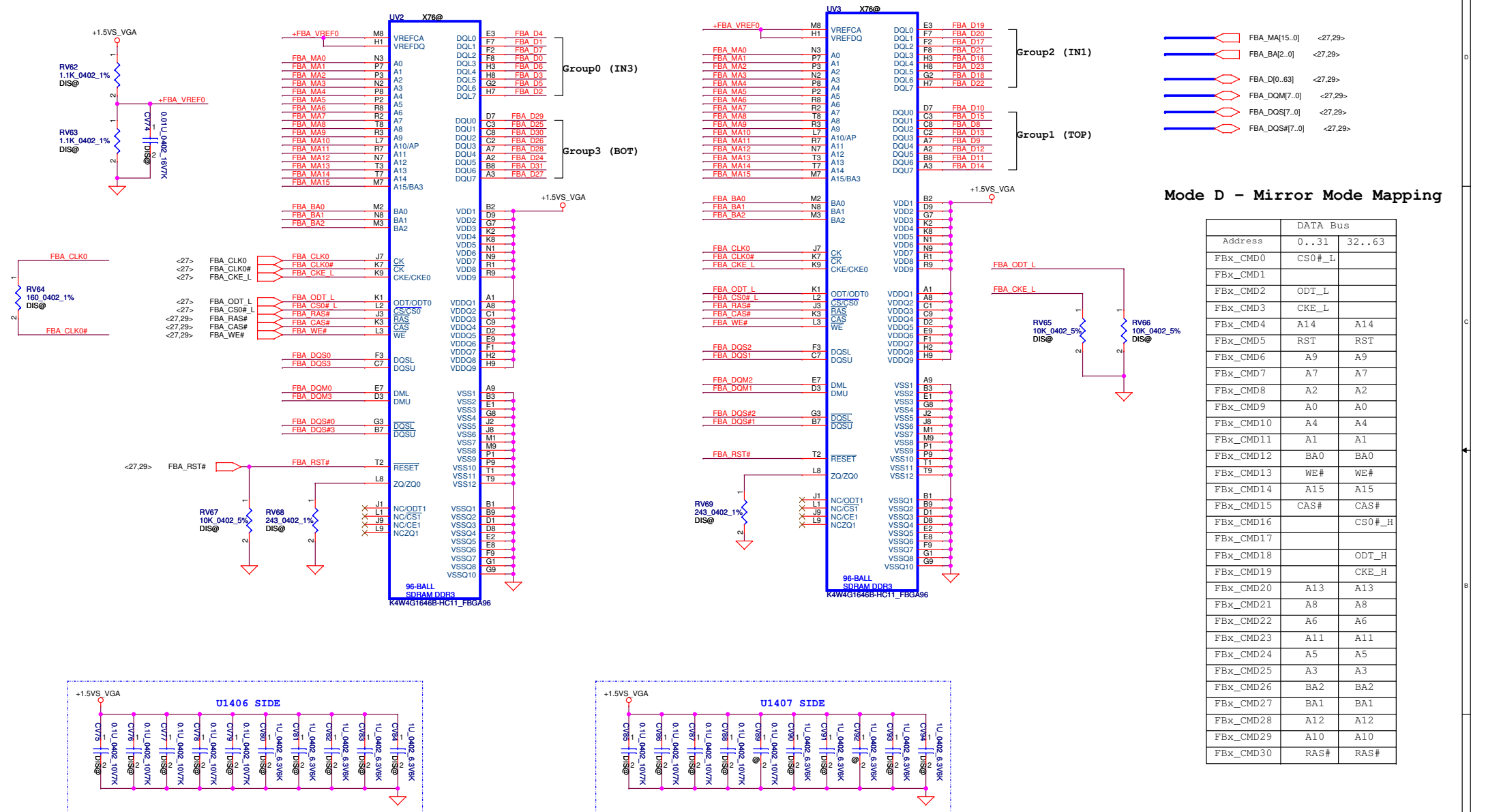
For GC6 (+1.5V\_VGA)



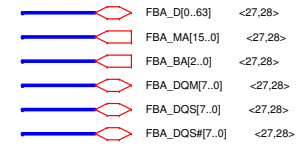
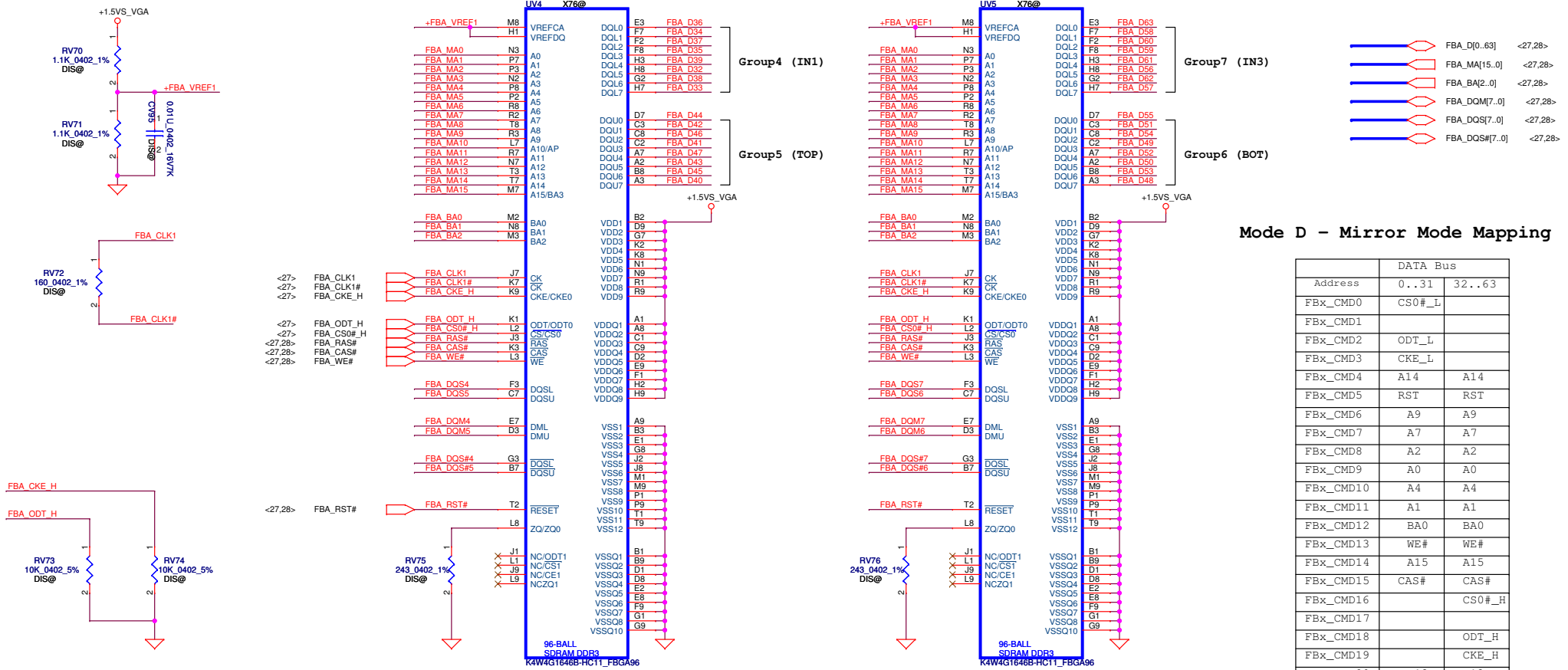
Mode D - Mirror Mode Mapping

Address	DATA Bus	
FBx_CMD0	0..31	32..63
FBx_CMD1	CS0#_L	
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

# Memory Partition A - Lower 32 bits

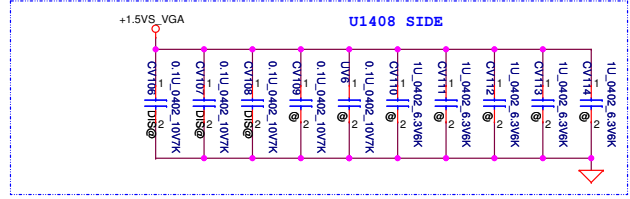
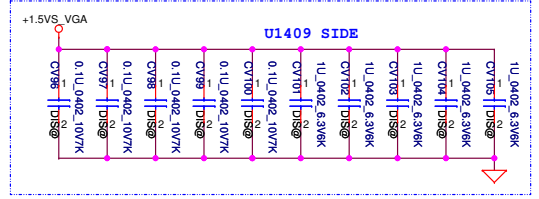


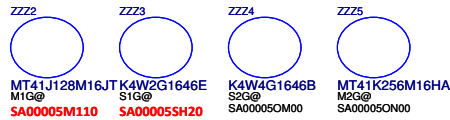
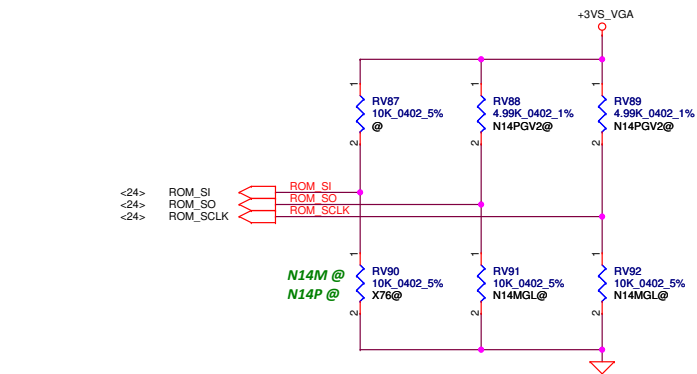
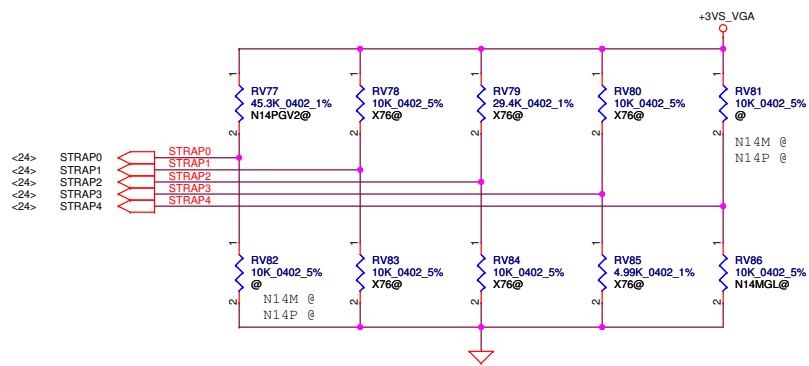
# Memory Partition A - Upper 32 bits



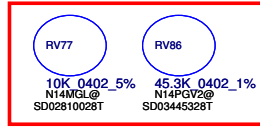
## Mode D - Mirror Mode Mapping

Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

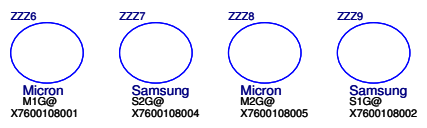




For N14P-GV2 QS Sample  
 ROM\_SO change from PU 10K to PU 5K  
 ROM\_SCLK change from PD 15K to PU 5K  
 STRAP1 change from PD 5K to PD 45K  
 STRAP2 change from PU 30K to PD 15K  
 STRAP4 change from PD 5K to PD 45K



Load BOM時，要改成RV86, RV77



Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

3GIO_PADCFG[3:0]	
0110	Gen1/Gen2 support only
0000	Gen3 support

FB[1:0]	
0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

PCIE_MAX_SPEED	
0	Limit booting to PCIe Gen1
1	Allow booting to PCIe Gen 2/3

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

USER Straps	
User [3:0]	
1000-1100	Customer defined

PCIE_SPEED_CHANGE_GEN3	
0	Disable PCIe Gen3 operation
1	Enable PCIe Gen3 operation

DP_PLL_VDD33V	
0	Reserved
1	Default

				X76		PU, RV78 PU, RV79		PU, RV80		
				RV90	RV77	PD, RV83	PD, RV84	PD, RV85	PD, RV86	
GPU	FB Memory GDDR3		ROM_SO	ROM_SCLK	ROM_SI	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
S2G, X76~04 SA00005OM00	N14P-GV2	* Samsung 1000MHz	K4W2G1646E-BC1A	PU 5K	PD 45K	PU 45.3K	PD 45.3K	PD 15K	PD 5K	PD 45.3K
			128Mx16							
	Micron 1000MHz	MT41J128M16JT-093G	PD 30K							
		128Mx16								
	* Samsung 900MHz	K4W4G1646B-HC11	PD 20K							
		256Mx16								
M2G, X76~05 SA00005ON00		* Micron 900MHz	MT41K256M16HA-107G	PD 10K						
			256Mx16							

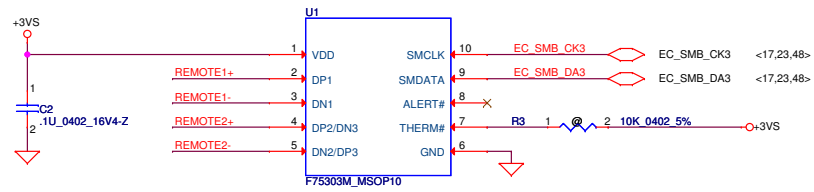
				PU, RV78 PU, RV79		PU, RV80				
				RV77	PD, RV83	PD, RV84	PD, RV85	PD, RV86		
GPU	FB Memory GDDR3		ROM_SO	ROM_SCLK	ROM_SI	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
S1G, X76~02 SA00005SH20	N14M-GL	* Samsung 1000MHz	K4W2G1646E-BC1A	PD 10K	PU 10K	PU 10K	PU 10K	PU 10K	PD 10K	
			128Mx16		PD 10K	PU 10K	PU 10K	PD 10K		
M1G, X76~01 SA00005M110		Hynix 1000MHz	H5TQ2G63DFR-N0C							
			128Mx16							
	* Micron 1000MHz	MT41J128M16JT-093G	PU 10K		PD 10K	PD 10K	PD 10K			
		128Mx16								
	Samsung 900MHz	K4W4G1646B-HC11	PU 10K	PU 10K	PU 10K	PU 10K				
		256Mx16								
	Hynix 900MHz	H5TQ4G63MFR-11C	PU 10K	PU 10K	PD 10K	PD 10K				
		256Mx16								
	Micron 900MHz	MT41K256M16HA-107G	PD 10K	PD 10K	PU 10K	PU 10K				
		256Mx16								

Security Classification	LC Future Center Secret Data		
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Title	N14P_MISC(2/2)		
Size	Document Number	Rev	
Custom	E440 NW-A151	1.0	
Date:	Thursday, July 11, 2013	Sheet	31 of 57

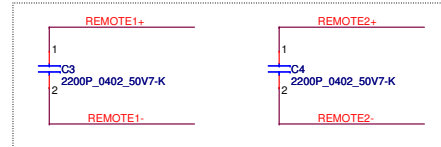
# Thermal Sensor

**Thermal Sensor  
placed near by VRAM**

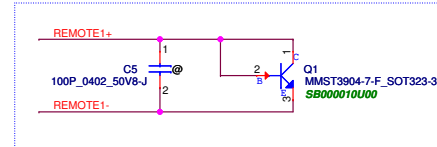


**Address 1001\_101xb**  
**Internal pull up 1.2K to 1.5V**  
**R for initial thermal shutdown temp**

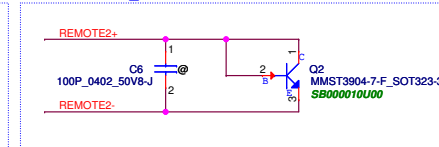
**Close to U2**



**Close to BOTTOM DDR3**



**Close to +CPU\_CORE**



**REMOTE2+/-:**  
**Trace width/space:10/10 mil**  
**Trace length:<8"**

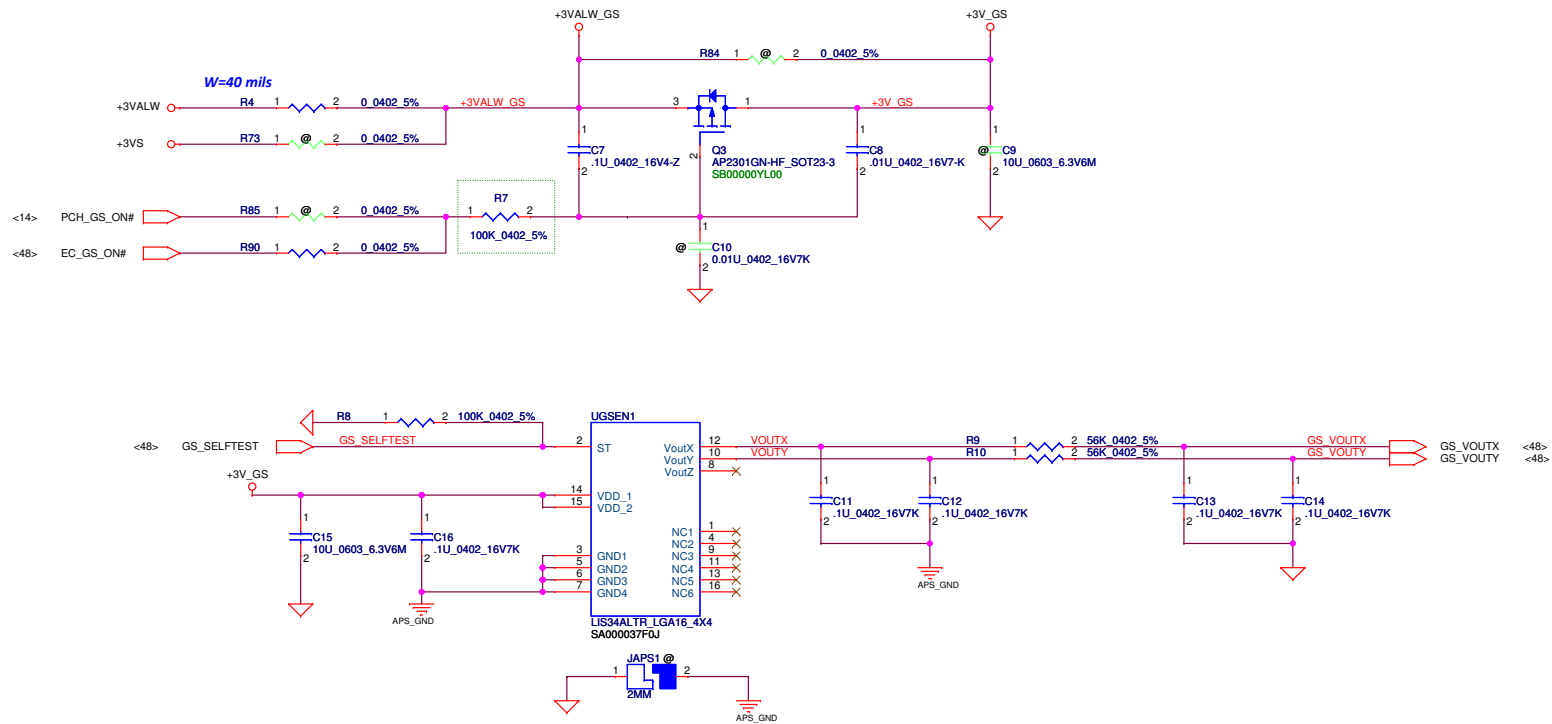
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Issued Date	2012/12/05	Deciphered Date 2014/12/05
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Title	THERMAL SENSOR	
Size	Document Number	Rev
Custom	E440 NW-A151	1.0
Date:	Thursday, July 11, 2013	Sheet 32 of 57



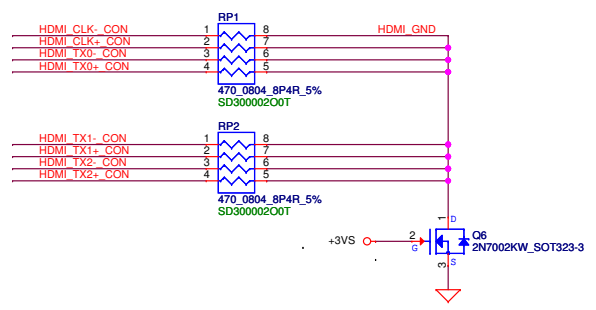
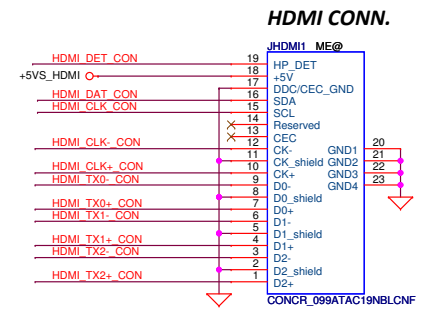
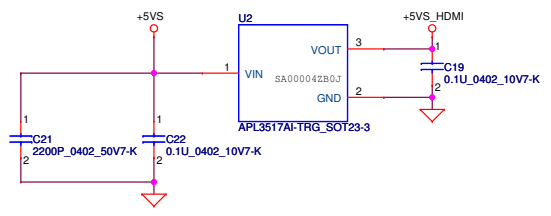
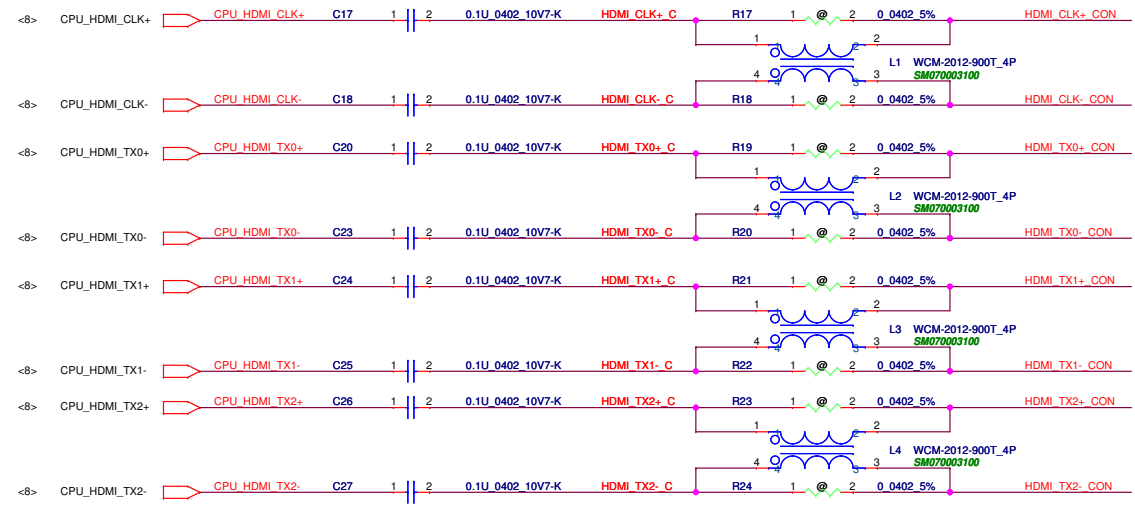
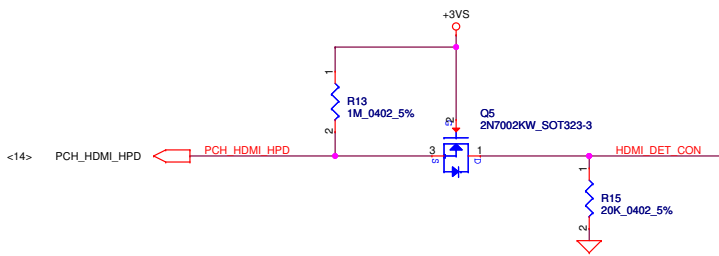
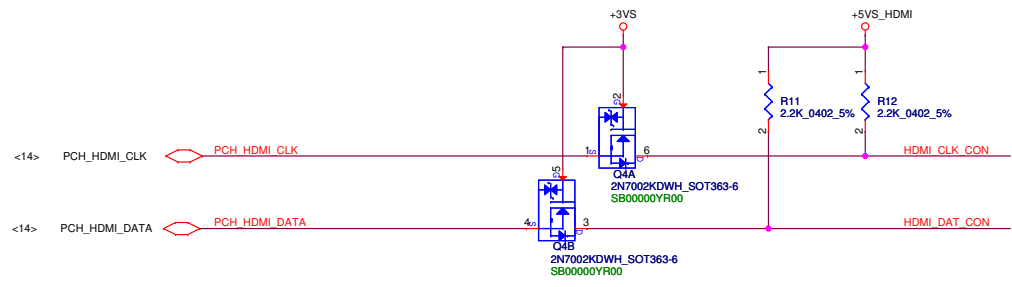


# APS G-Sensor

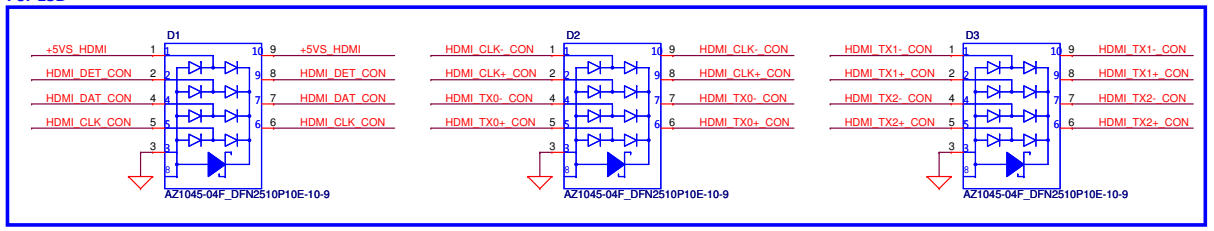


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Title	APS G-SENSOR		
Size	Custom	Document Number	
Date:	Thursday, July 11, 2013	Sheet	33 of 57
Rev	1.0	<b>E440 NW-A151</b>	



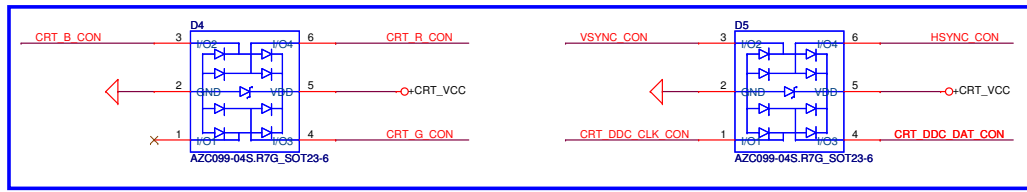
For ESD



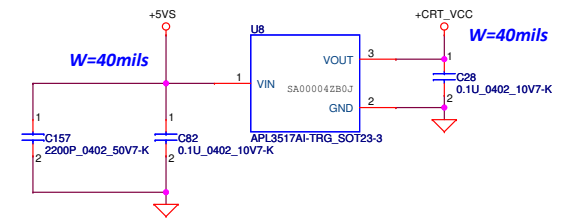
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Issued Date	2012/12/05	Deciphered Date	2014/12/05
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Size	Document Number	Rev
Custom	<b>E440 NM-A151</b>	1.0
Date:	Thursday, July 11, 2013	Sheet 34 of 57

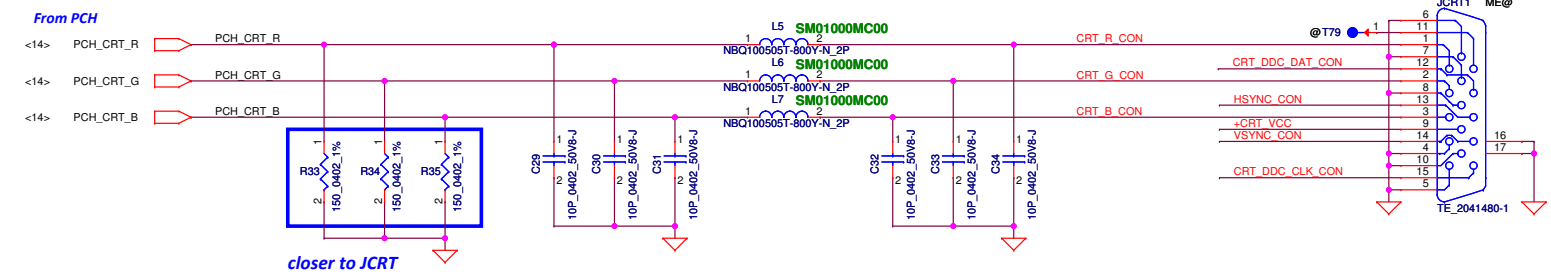




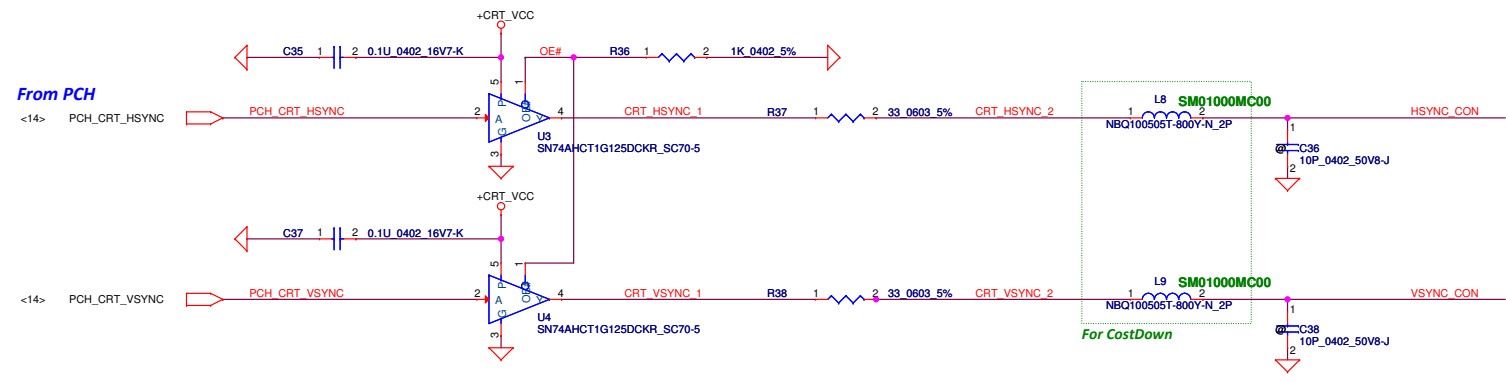
closer to JCRT



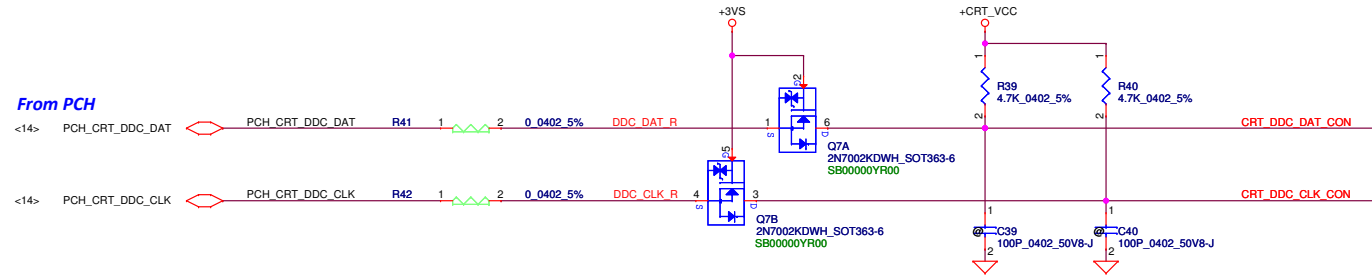
### CRT Connector



closer to JCRT

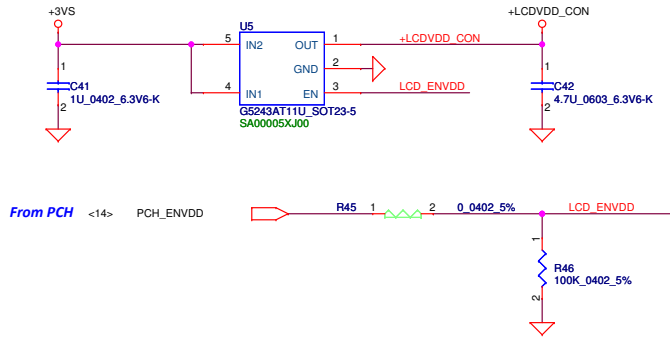


For CostDown

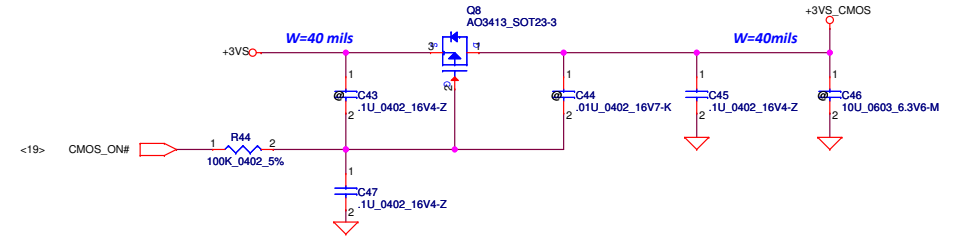


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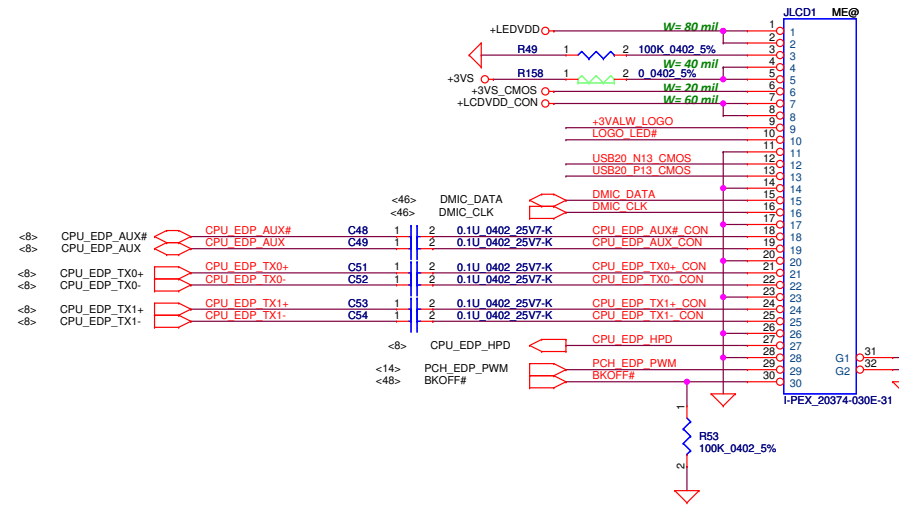
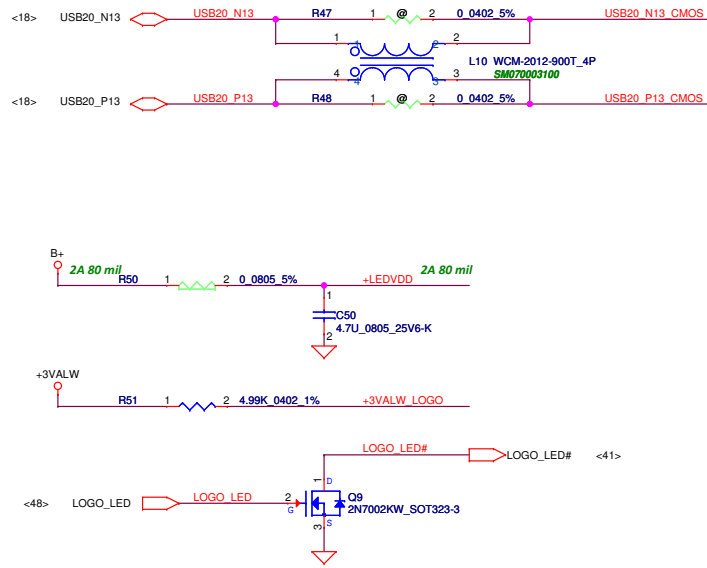
### LCDVDD Circuit



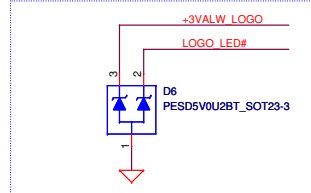
### CMOS Camera



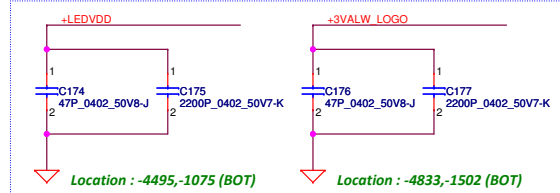
### CMOS USB Port10



### ESD request

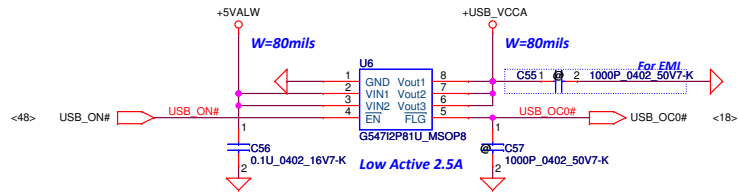


### EMI

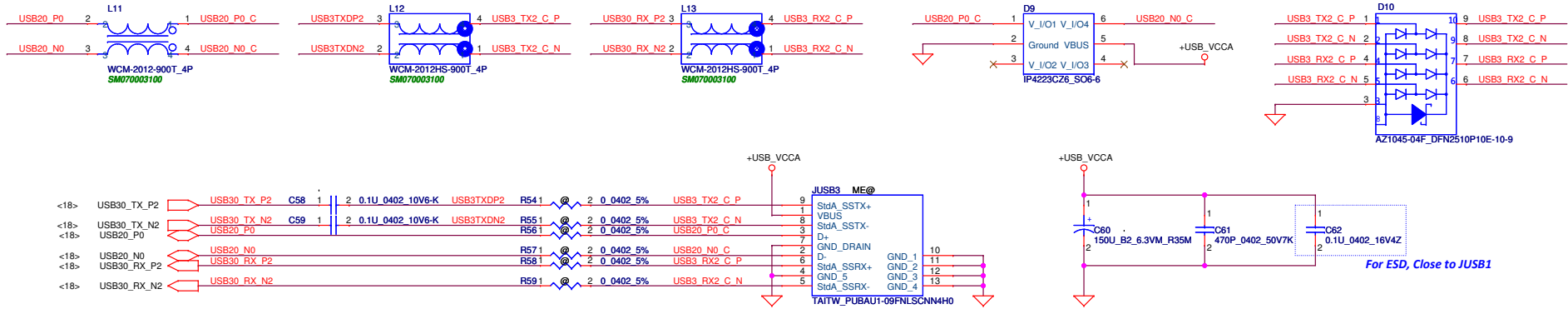


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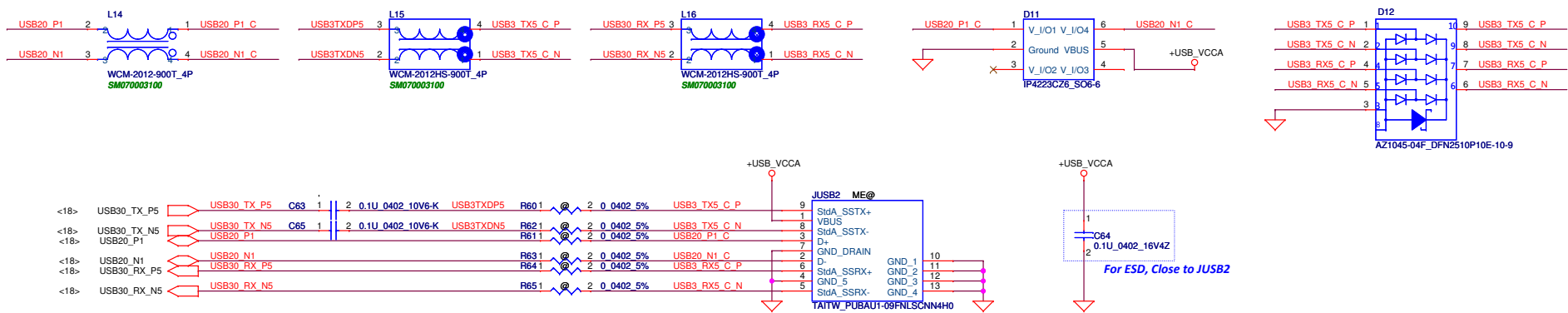
Title	LCFC
LCD/CMOS CONN.	
Size	Document Number
Custom	E440 NM-A151
Date:	Thursday, July 11, 2013
Sheet	36 of 57
Rev	1.0



### USB30 Front



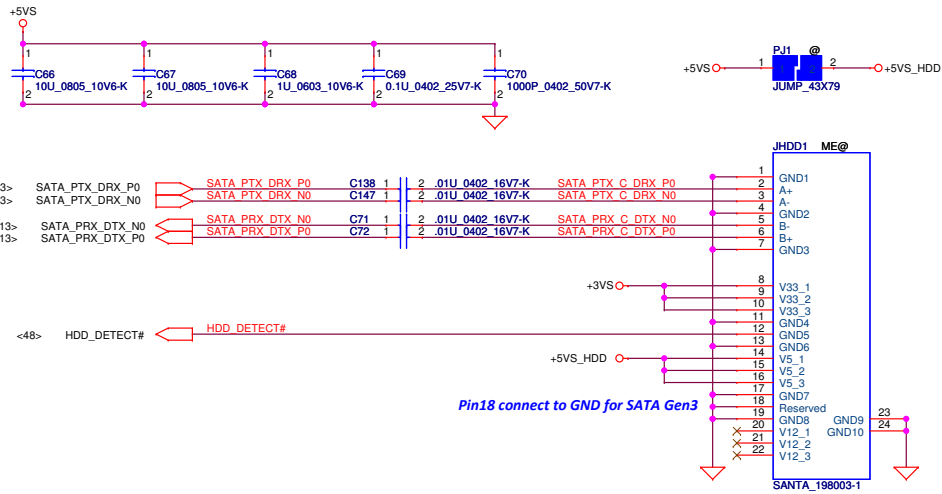
### USB30 Back



Security Classification	LC Future Center Secret Data		Title
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Size	Document Number	Rev	
Custom	E440 NM-A151	1.0	
Date:	Thursday, July 11, 2013	Sheet	37 of 57

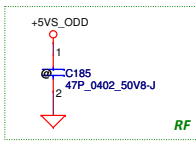
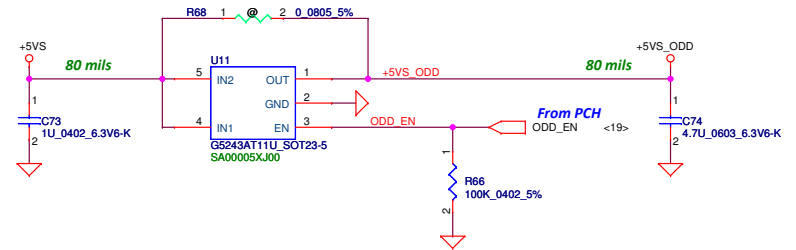
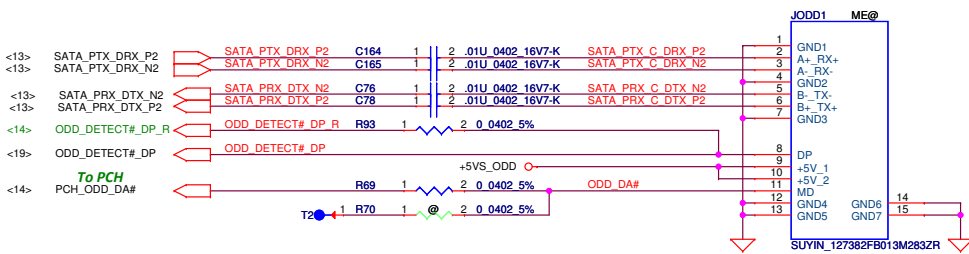



### SATA HDD CONN.



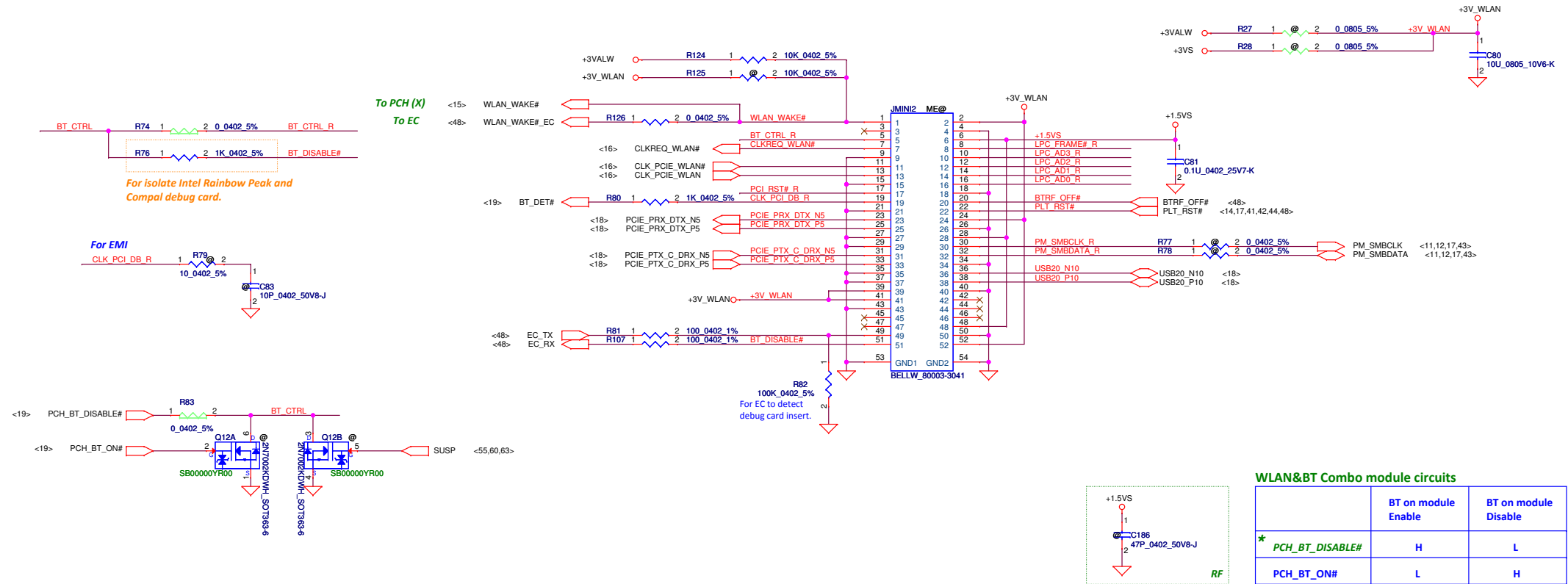
### SATA ODD CONN & ODD Power Control

### +5VS TO +5VS\_ODD



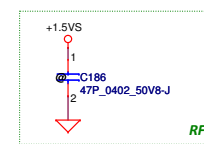
Security Classification	LC Future Center Secret Data		Title	SATA HDD/ODD CONN.	
Issued Date	2012/12/05	Deciphered Date	2014/12/05		
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Size	Document Number	Date		Thursday, July 11, 2013	Sheet 38 of 57
Custom	E440 NW-A151	Rev		1.0	

# Mini-Express Card(WLAN/WiMAX)



**WLAN&BT Combo module circuits**

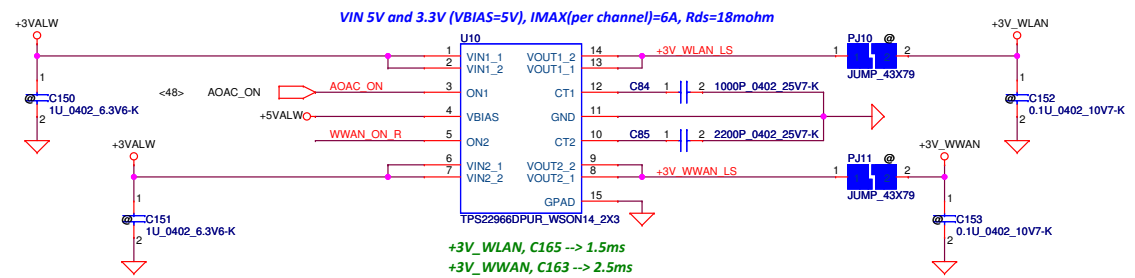
	BT on module Enable	BT on module Disable
* PCH_BT_DISABLE#	H	L
PCH_BT_ON#	L	H



## Load Switch

**+3VALW To +3V\_WLAN**  
**+3VALW To +3V\_WWAN**

1. softstart (RC) will check on EVT PCB
2. if AOAC enable +3V\_WLAN always ON  
if AOAC disable +3V\_WLAN is same as +3VS

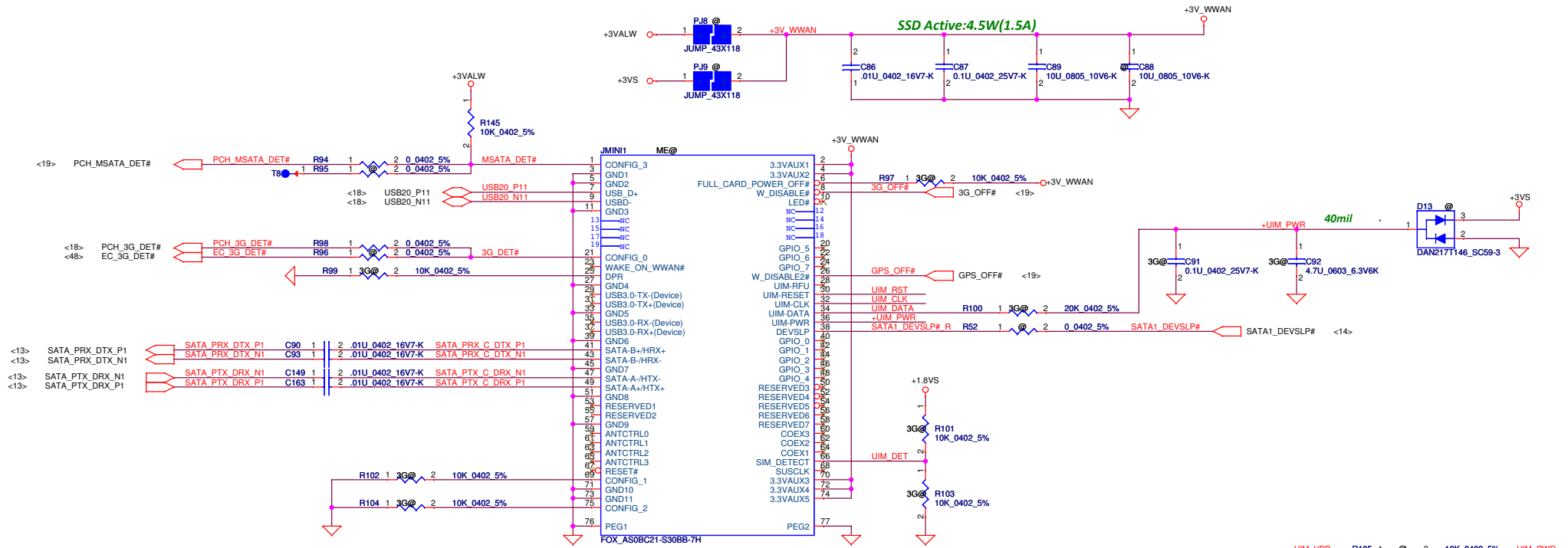


Reserve for SW mini-pcie debug card.  
Series resistors closed to KBC side.

LPC_FRAME# R	R86	1	@	2	0.0402_5%	LPC_FRAME#	LPC_FRAME#	<17,44,48>
LPC_AD3 R	R87	1	@	2	0.0402_5%	LPC_AD3	LPC_AD3	<17,44,48>
LPC_AD2 R	R88	1	@	2	0.0402_5%	LPC_AD2	LPC_AD2	<17,44,48>
LPC_AD1 R	R89	1	@	2	0.0402_5%	LPC_AD1	LPC_AD1	<17,44,48>
LPC_AD0 R	R91	1	@	2	0.0402_5%	LPC_AD0	LPC_AD0	<17,44,48>
PCI_RST# R	R92	1	@	2	0.0402_5%	PLT_RST#	PLT_RST#	<17,44,48>
CLK_PCIE_DB R	R106	1	@	2	0.0402_5%	CLK_PCIE_DB	CLK_PCIE_DB	<16>

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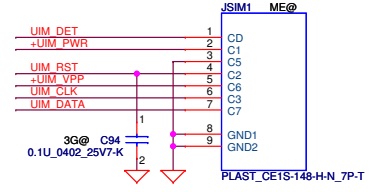
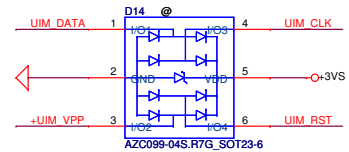
# NGFF(SSD) & SIM CARD CONN.



Only for 15"

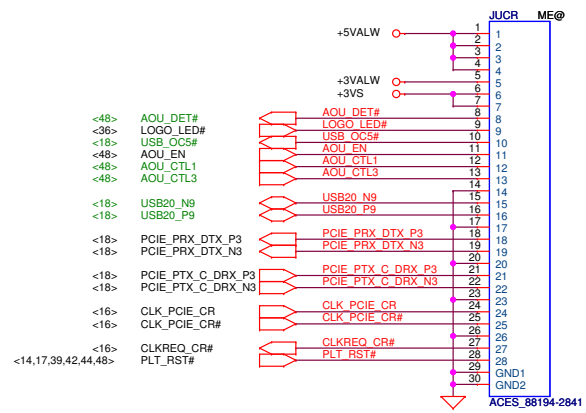
1. PCH\_MSATA\_DET# --> +3V\_PCH  
EC\_MSATA\_DET# --> +3VL
2. PCH\_3G\_DET# --> +3VS  
EC\_3G\_DET# --> +3VL  
需小心EC漏電到PCH
3. EC don't have GPIO pin for DET# pin as below
  - a. PCH\_3G\_DET#
  - b. PCH\_MSATA\_DET#

NGFF Detect Desc.		
	MSATA_DET#	3G_DET#
No Card	1	1
WWAN CARD	1	0
SSD CARD	0	0






### USB2.0, CR & LOGO Board

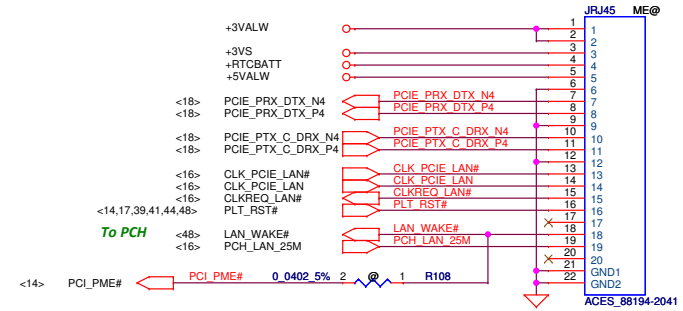


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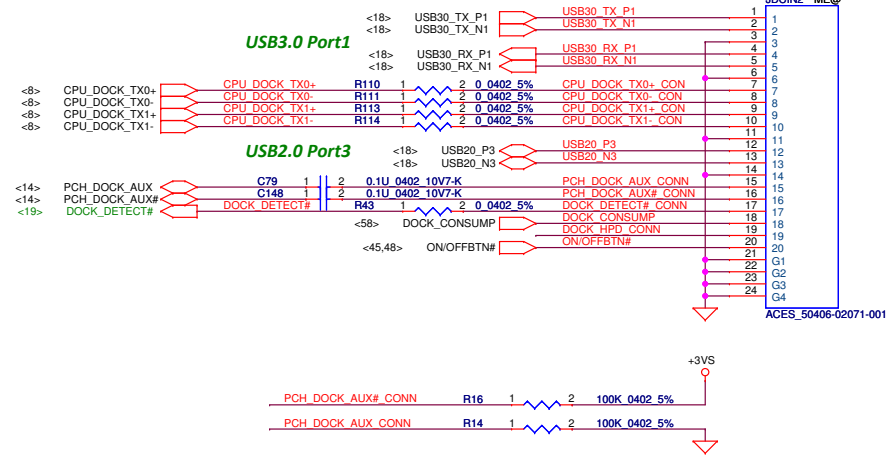
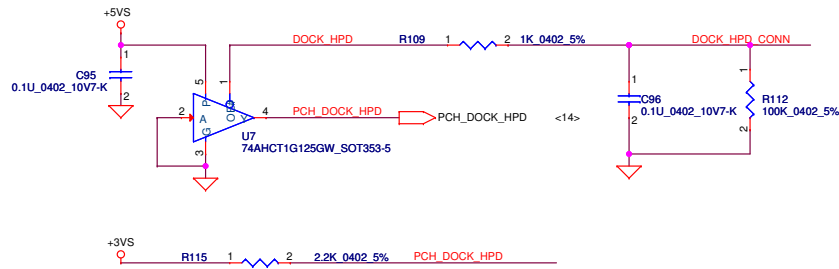
Title	PCie-CR/USB-Charge CONN. 	
Size	Document Number	Rev
Custom	<b>E440 NM-A151</b>	1.0
Date:	Thursday, July 11, 2013	Sheet 41 of 57

**LAN (Port4)  
USB3.0/2.0 (Port1/3)  
DP(DDIC)**

**LAN CONN. (FFC)**

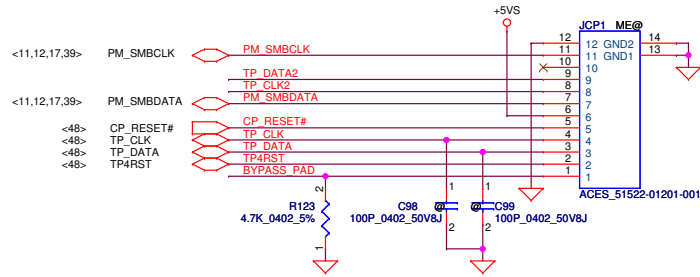


**DCIN CONN. (Coaxial)**

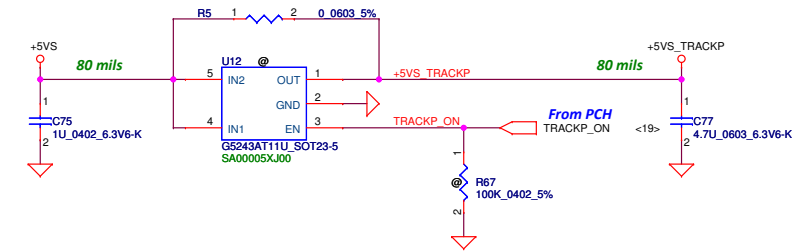
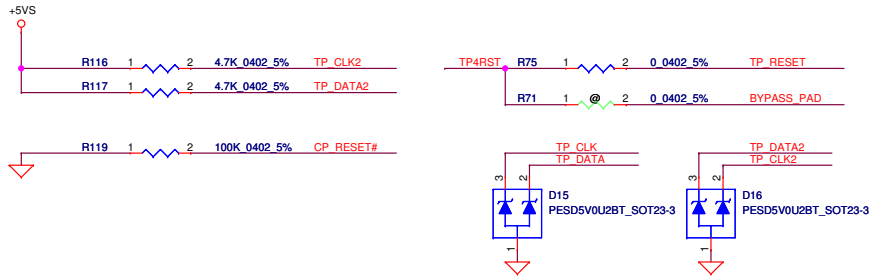
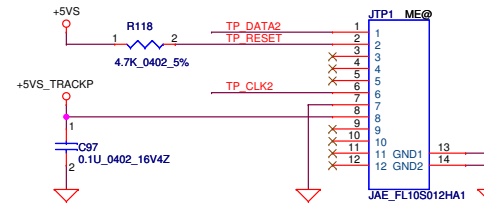


Security Classification				LC Future Center Secret Data				Title					
Issued Date		2012/12/05		Deciphered Date		2014/12/05		PCIE-RJ45/RTC/Docking CON					
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								Custom		E440 NM-A151		1.0	
								Date:		Thursday, July 11, 2013		Sheet 42 of 57	

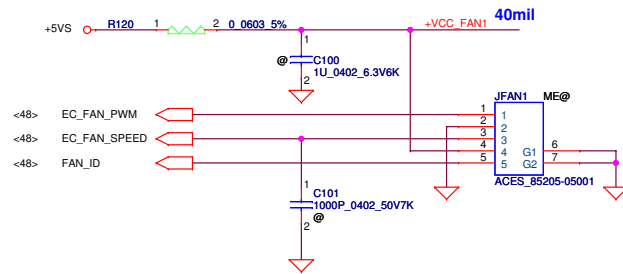
### Click Pad



### Track point



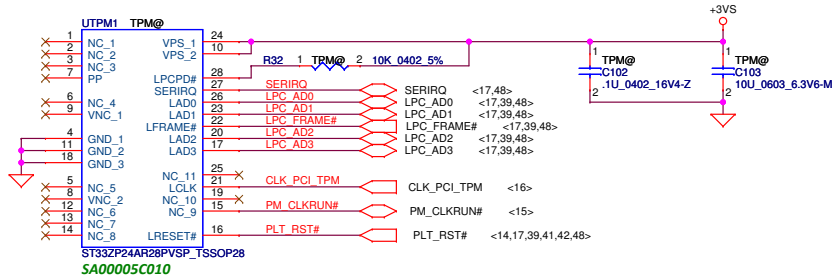
### FAN CONN.



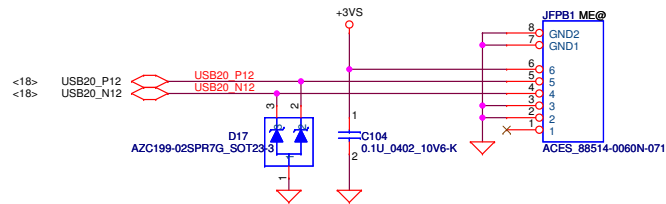
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Document Number	E440 NM-A151	
Date	Thursday, July 11, 2013	Sheet 43 of 57

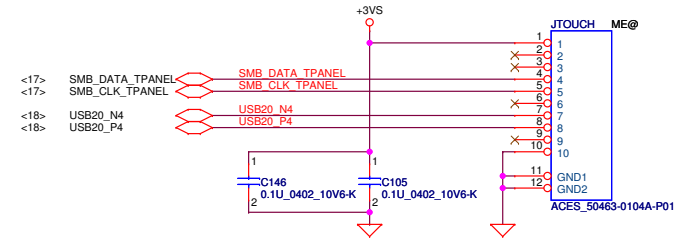
### TPM IC




### FingerPrint CONN.



### Touch Panel CONN.

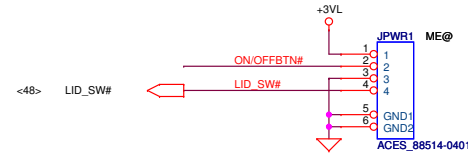
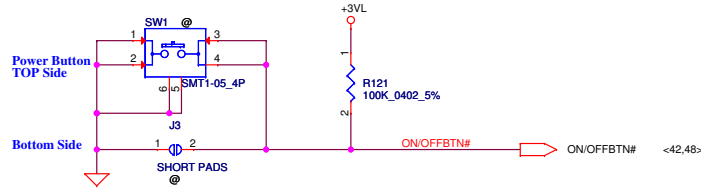


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				Rev: 1.0

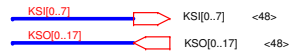
# PWR BTN/LID SW CONN.

1. Power Button/B link to Function/B Conn. 10pin
2. Lid Switch

ON/OFF switch



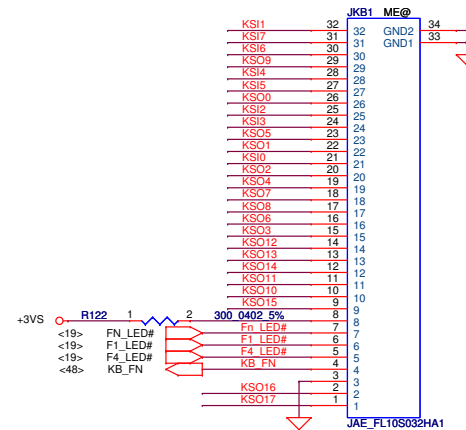
# KeyBoard CONN.(14")



KSI0	C108	1	2	100P_0402_50V8J
KSI1	C110	1	2	100P_0402_50V8J
KSI2	C106	1	2	100P_0402_50V8J
KSI3	C107	1	2	100P_0402_50V8J
KSI4	C114	1	2	100P_0402_50V8J
KSI5	C116	1	2	100P_0402_50V8J
KSI6	C118	1	2	100P_0402_50V8J
KSI7	C120	1	2	100P_0402_50V8J
Fn_LED#	C124	1	2	100P_0402_50V8J
F1_LED#	C126	1	2	100P_0402_50V8J
F4_LED#	C128	1	2	100P_0402_50V8J
KB_FN	C130	1	2	100P_0402_50V8J

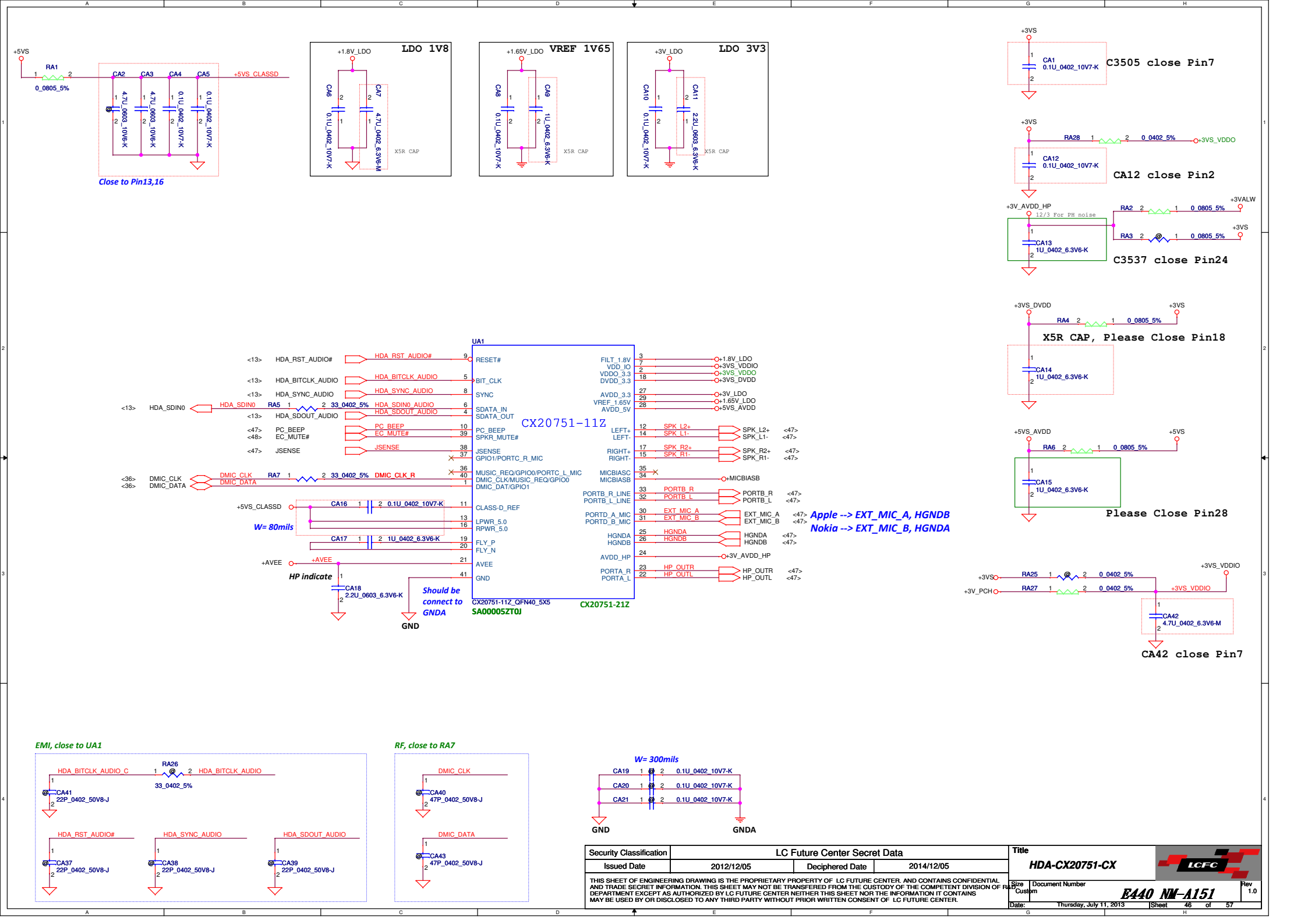
CONN PIN define need double check

KSO0	C109	1	2	100P_0402_50V8J
KSO1	C111	1	2	100P_0402_50V8J
KSO2	C112	1	2	100P_0402_50V8J
KSO3	C113	1	2	100P_0402_50V8J
KSO4	C115	1	2	100P_0402_50V8J
KSO5	C117	1	2	100P_0402_50V8J
KSO6	C119	1	2	100P_0402_50V8J
KSO7	C121	1	2	100P_0402_50V8J
KSO8	C122	1	2	100P_0402_50V8J
KSO9	C123	1	2	100P_0402_50V8J
KSO10	C125	1	2	100P_0402_50V8J
KSO11	C127	1	2	100P_0402_50V8J
KSO12	C129	1	2	100P_0402_50V8J
KSO13	C131	1	2	100P_0402_50V8J
KSO14	C132	1	2	100P_0402_50V8J
KSO15	C133	1	2	100P_0402_50V8J
KSO16	C134	1	2	100P_0402_50V8J
KSO17	C135	1	2	100P_0402_50V8J



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Custom	E440 NM-A151	Thursday, July 11, 2013	1.0





Close to Pin13,16

CX20751-11Z

CX20751-21Z

Apple --> EXT\_MIC\_A, HGND B  
 Nokia --> EXT\_MIC\_B, HGND A

EMI, close to UA1

RF, close to RA7

W= 300mils

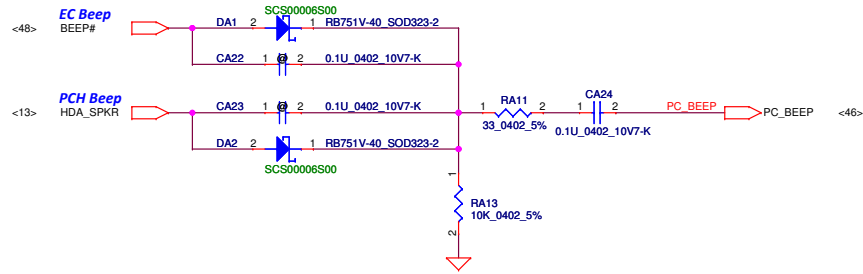
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Issued Date	2012/12/05	Deciphered Date	2014/12/05

Title		LCFC
HDA-CX20751-CX		

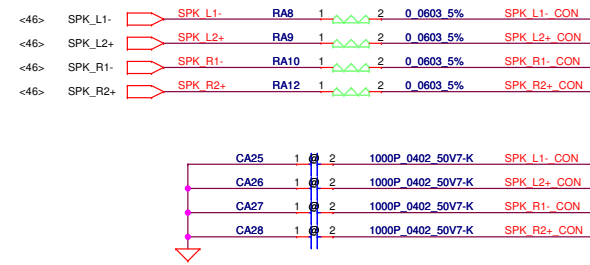
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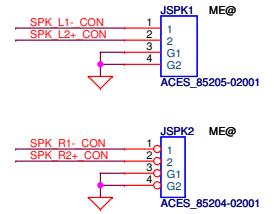
### PC BEEP



### Speaker OUT

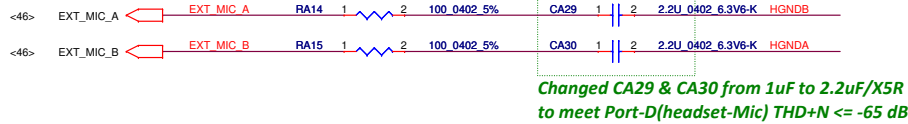


### SPK CONN.



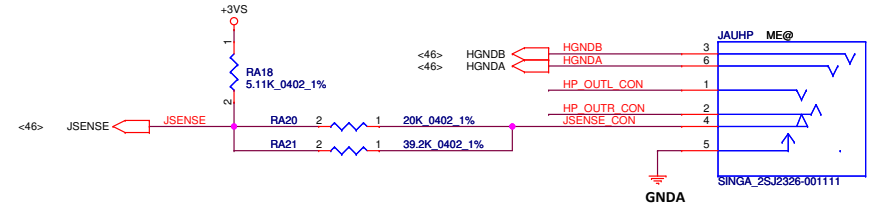
### EXT. MIC/LINE IN

Apple --> EXT\_MIC\_A, HGNCB  
Nokia --> EXT\_MIC\_B, HGNCB

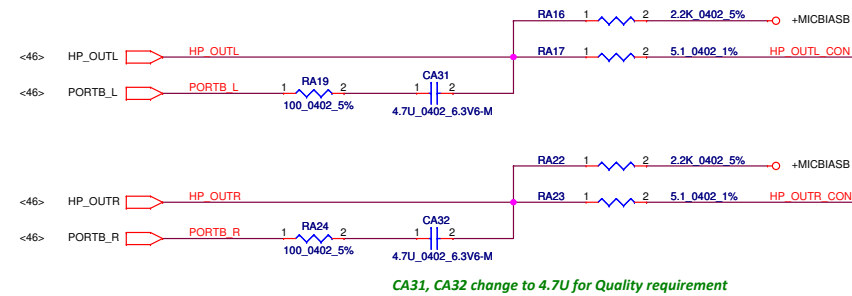


Changed CA29 & CA30 from 1uF to 2.2uF/X5R to meet Port-D(headset-Mic) THD+N <= -65 dB

### Audio Jack

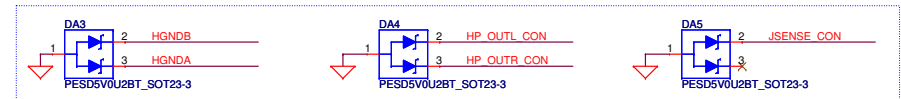


### HeadPhone/LINE OUT

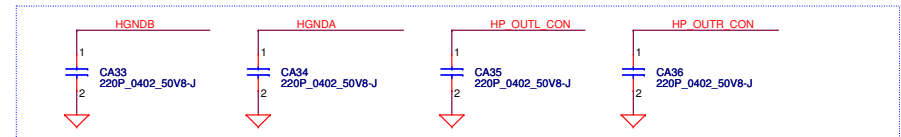


CA31, CA32 change to 4.7uF for Quality requirement

#### ESD Diode, close to JAUHP



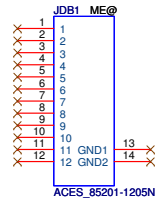
#### EMI, close to JAUHP




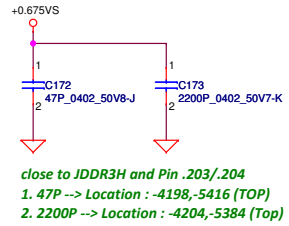
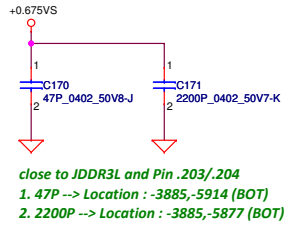
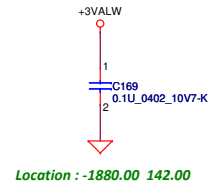
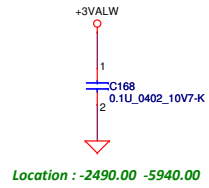
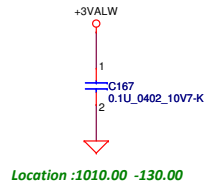
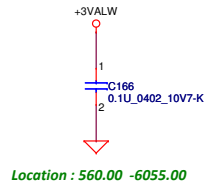
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Date:	Thursday, July 11, 2013	Sheet	47	of 57	




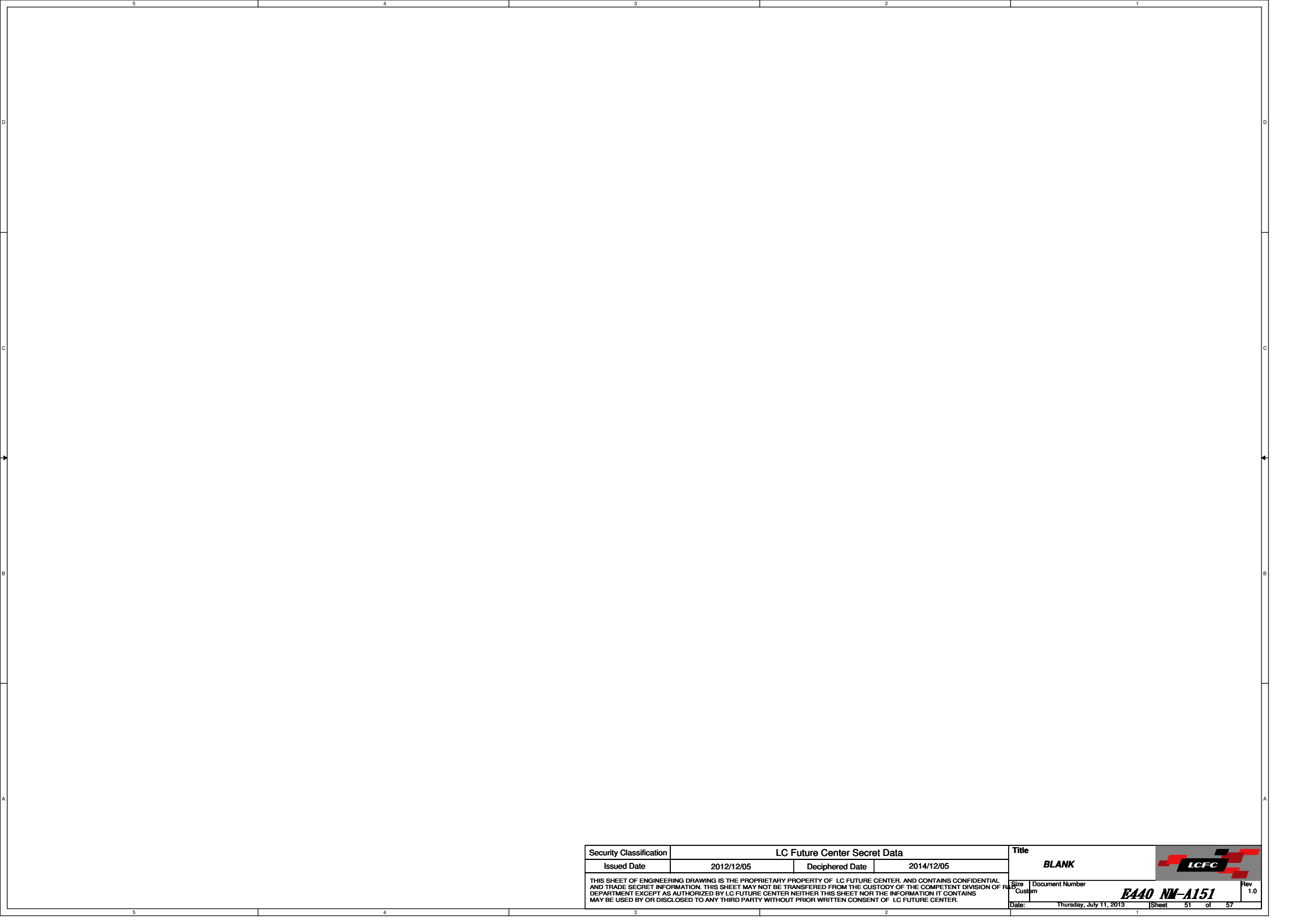




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				Date: Thursday, July 11, 2013	Rev 1.0
				Sheet 50 of 57	



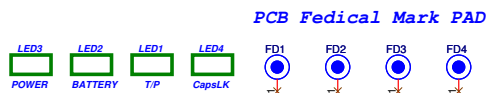
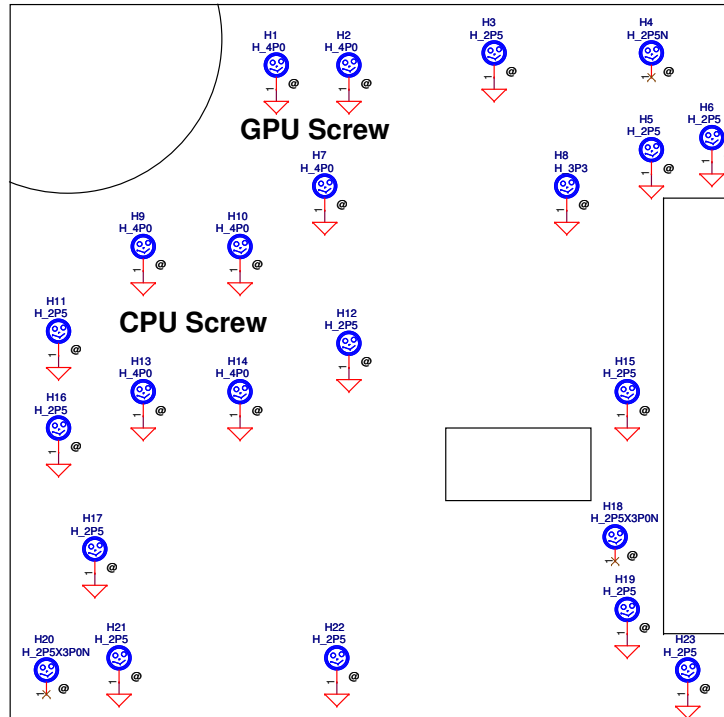
Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05
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Title	<b>BLANK</b>
Date:	Thursday, July 11, 2013



Size	Document Number	Rev
Custom	<b>E440 NM-A151</b>	1.0
Sheet 51 of 57		

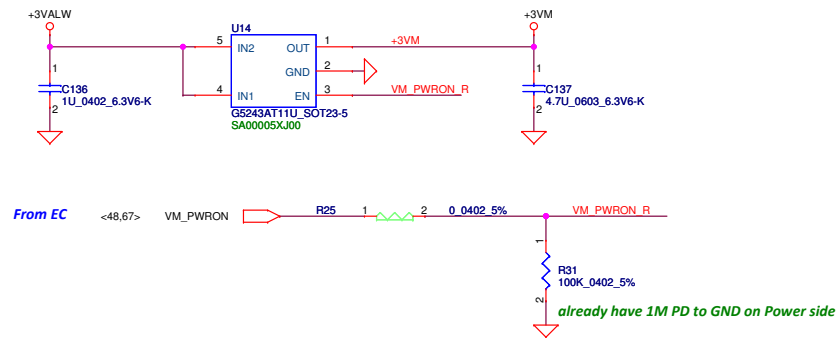
# Screw Hole




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Issued Date	2012/12/05	Deciphered Date	2014/12/05	LED	
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Date:	Thursday, July 11, 2013	Sheet	52	of	57

## +3VALW to +3VM

FOR SBA Function POWER(always mount)

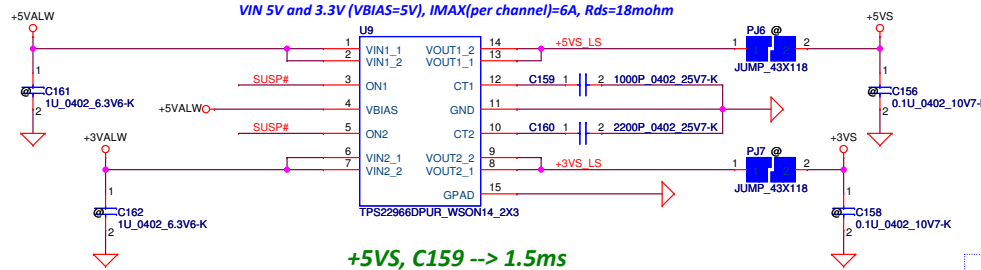
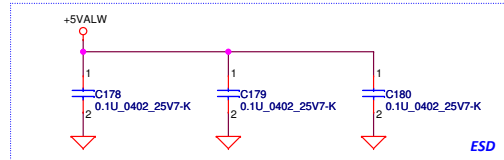
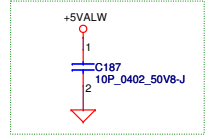


Security Classification	LC Future Center Secret Data		Title	
Issued Date	2012/12/05	Deciphered Date	2014/12/05	
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Size	Document Number	Date	Rev	
Custom	JITR1_LA-4141 E540 NM-A161	Thursday, July 11, 2013	1.0	
Date:			Sheet	53 of 57

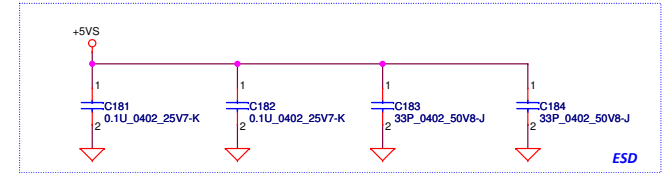


**Load Switch**  
**+5VALW To +5VS**  
**+3VALW To +3VS**

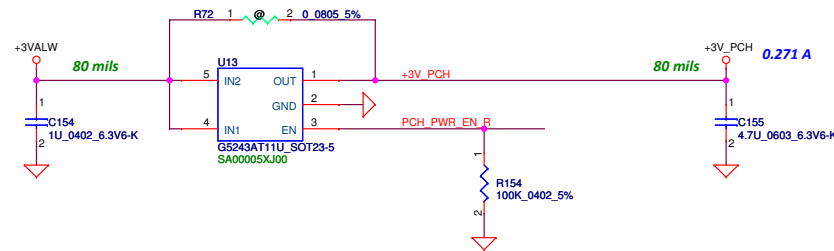
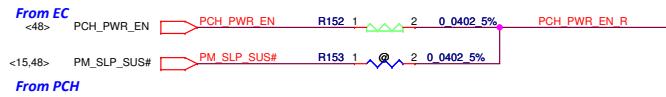
CPI, 14" only



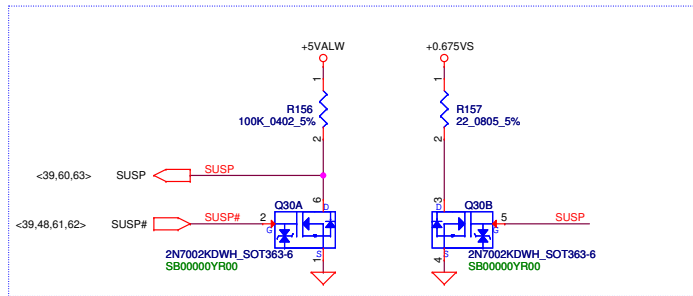
**+5VS, C159 --> 1.5ms**  
**+3VS, C160 --> 2.5ms**



**+3VALW To +3V\_PCH**

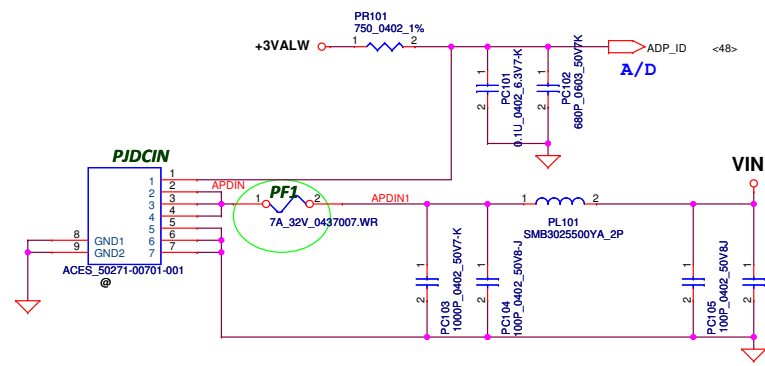


**For DisCharge**

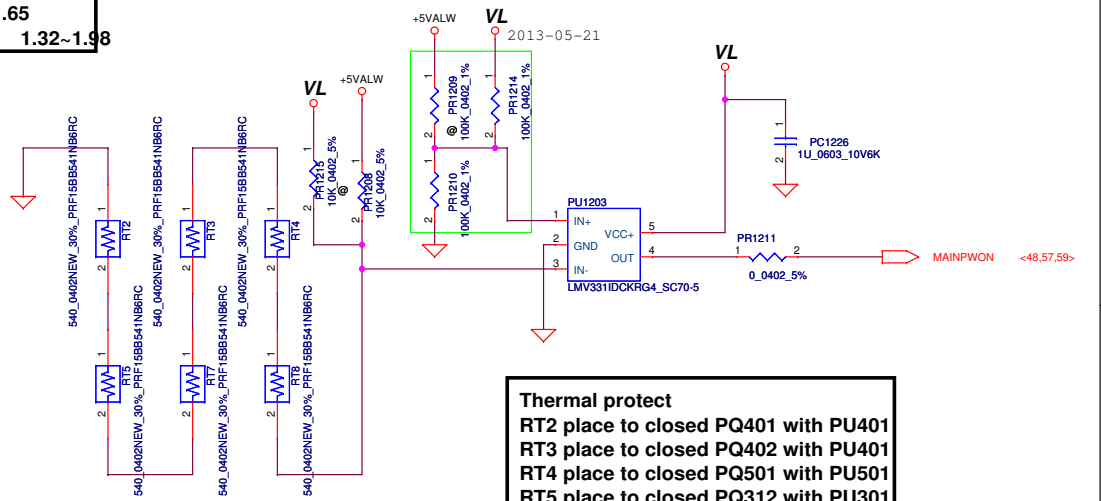


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Issued Date	2012/12/05	Deciphered Date 2014/12/05
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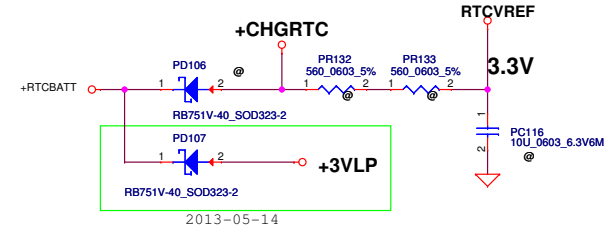
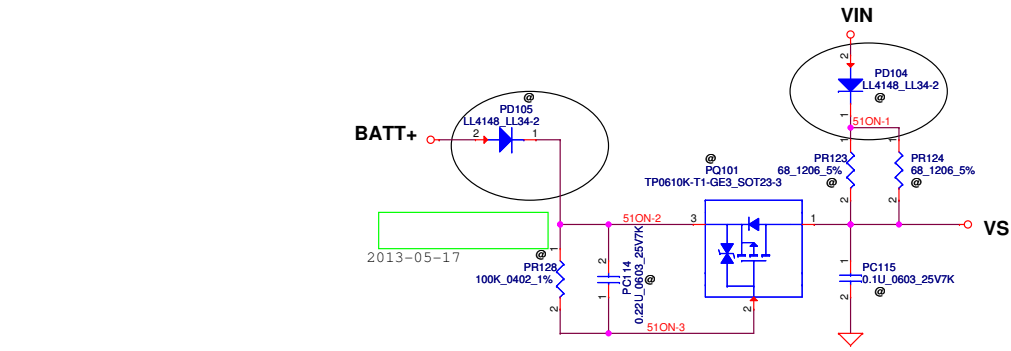
Title	DC V TO V/V5 INTERFACE	
Document Number	E440 NM-A151	
Date	Thursday, July 11, 2013	Rev 1.0
Sheet	35 of 57	



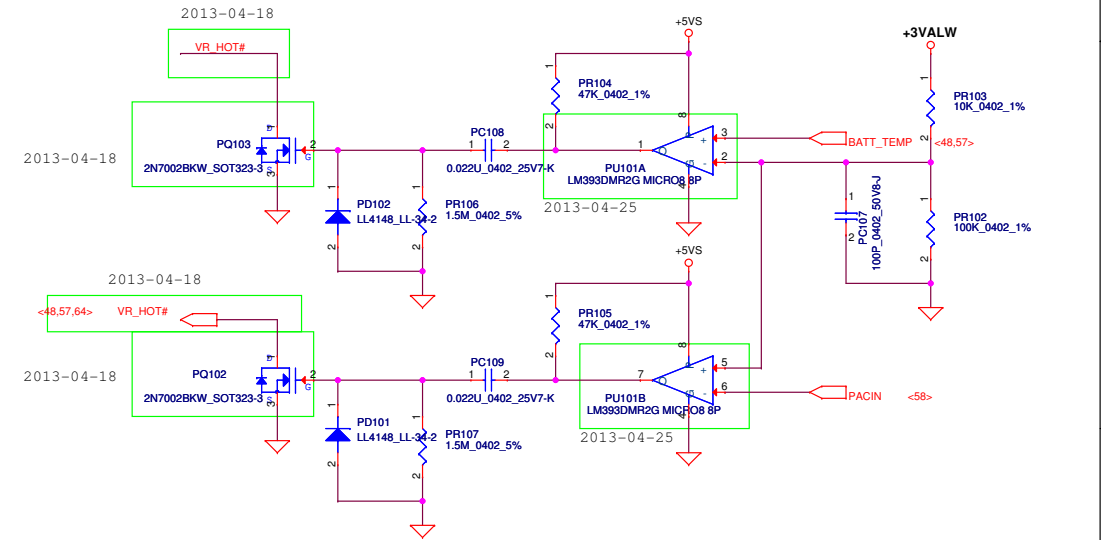
ADP_ID		
AC Adapter	90W	65W
R(K ohm)	open	10
ADP_ID(V)	3.3	1.65
Detection voltage	>2.64	1.32~1.98



**Thermal protect**  
 RT2 place to closed PQ401 with PU401  
 RT3 place to closed PQ402 with PU401  
 RT4 place to closed PQ501 with PU501  
 RT5 place to closed PQ312 with PU301  
 RT7 place to closed PQ804 with PU801  
 RT8 place to closed PQ1001 with PU901



**RTC Battery**



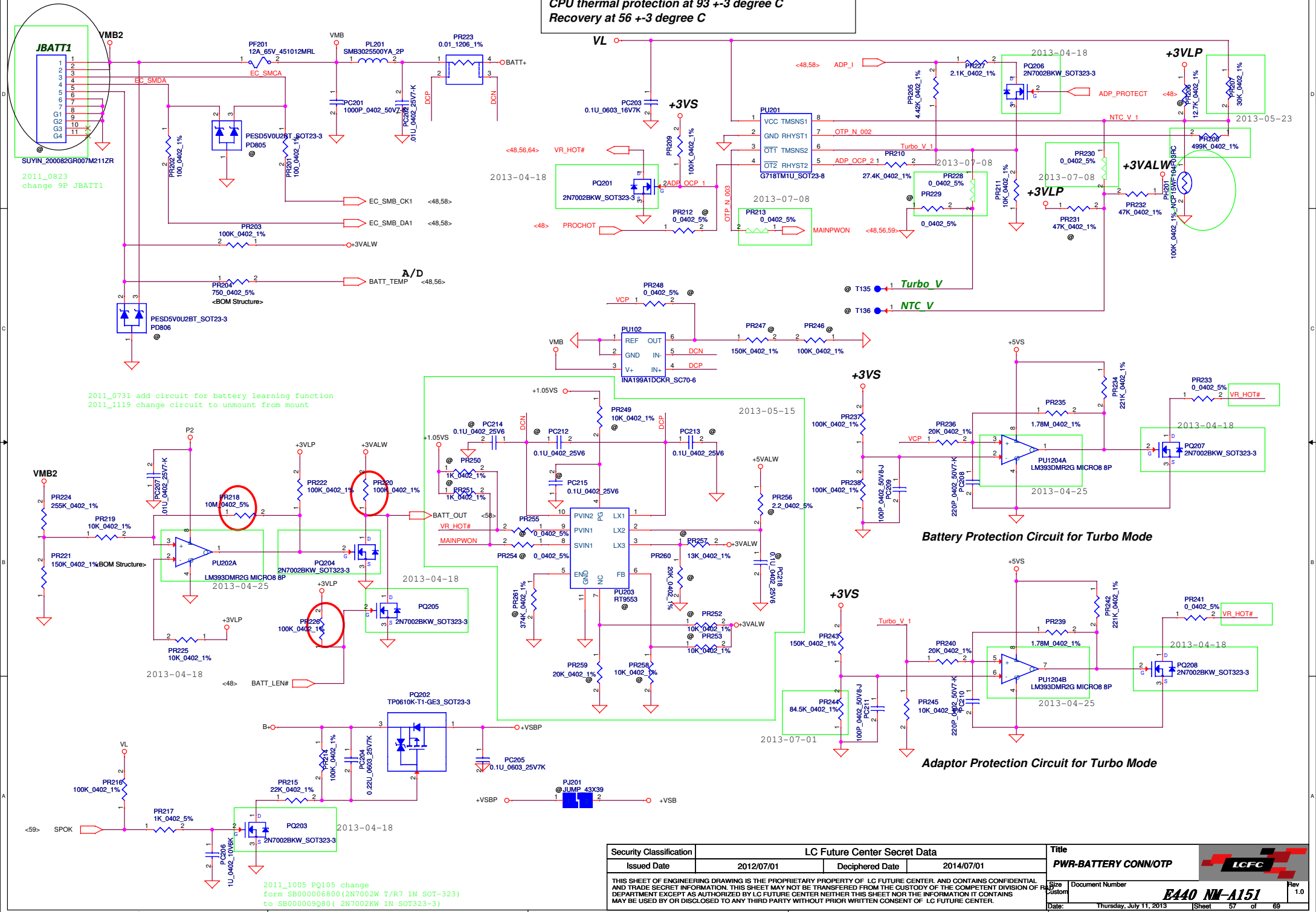
Security Classification			
LC Future Center Secret Data			
Issued Date	2012/07/01	Deciphered Date	2014/07/01
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Title	
PWR-DCIN / Vin Detector	
Size	Document Number
Custom	E440 NM-A151
Date:	Thursday, July 11, 2013
Sheet	36 of 69
Rev	1.0





PH1 under CPU bottom side :  
 CPU thermal protection at 93 +/-3 degree C  
 Recovery at 56 +/-3 degree C



2011\_0823  
 change 9P JBATT1

2011\_0731 add circuit for battery learning function  
 2011\_1119 change circuit to unmount from mount

Battery Protection Circuit for Turbo Mode

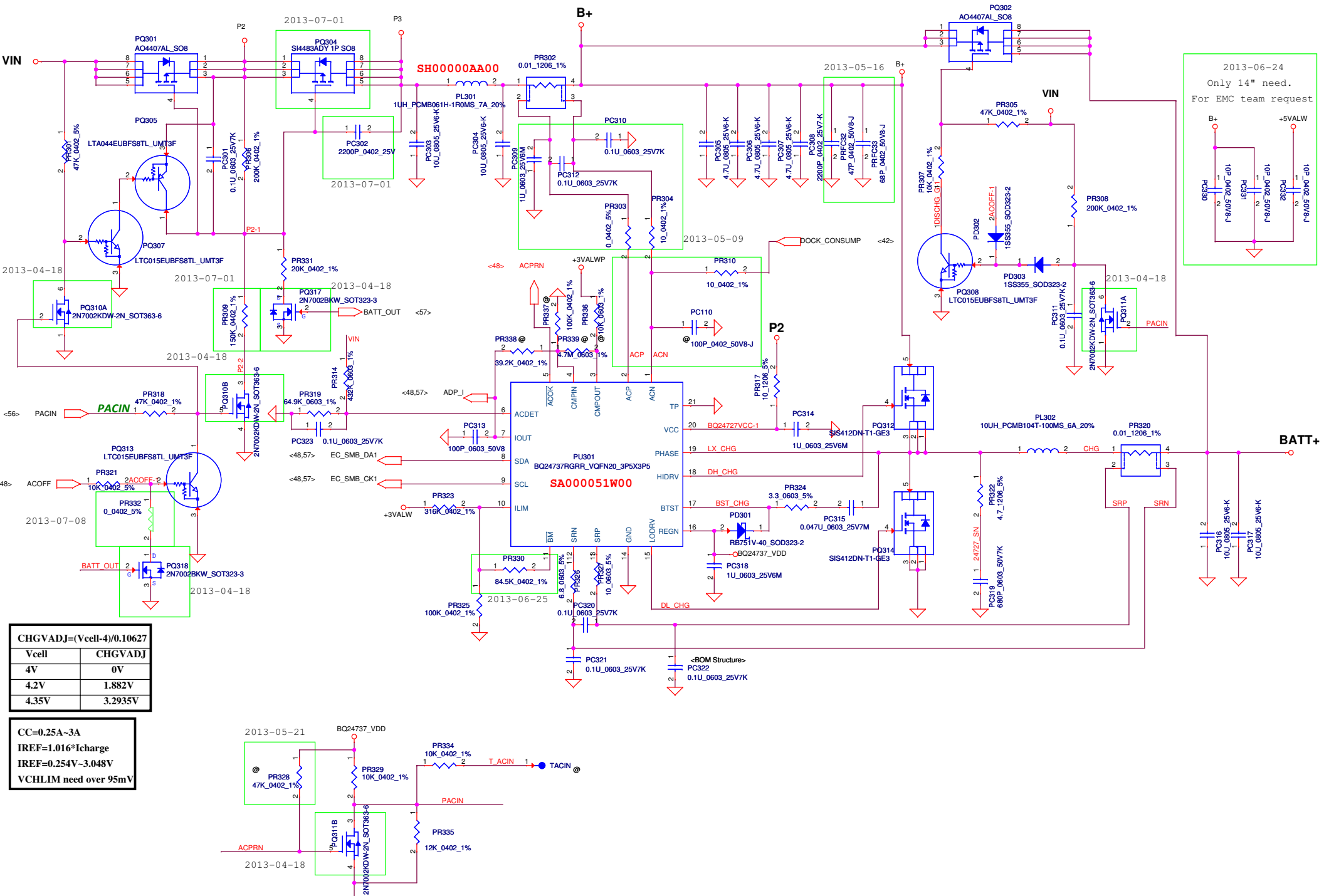
Adaptor Protection Circuit for Turbo Mode

2011\_1005 PQ105 change  
 form SB000006800 (2N7002W T/R7 1N SOT-323)  
 to SB000009080 (2N7002KW 1N SOT323-3)

Security Classification			
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Issued Date	2012/07/01	Deciphered Date	2014/07/01
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Title	
PWR-BATTERY CONN/OTP	
Size	Document Number
Custom	<b>E440 NM-A151</b>
Date:	Thursday, July 11, 2013
Sheet	37 of 69
Rev	1.0

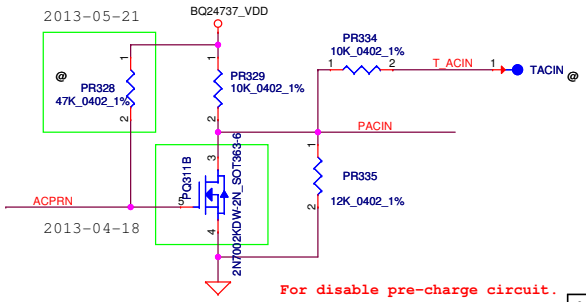




CHGVADJ=(Vcell-4)/0.10627

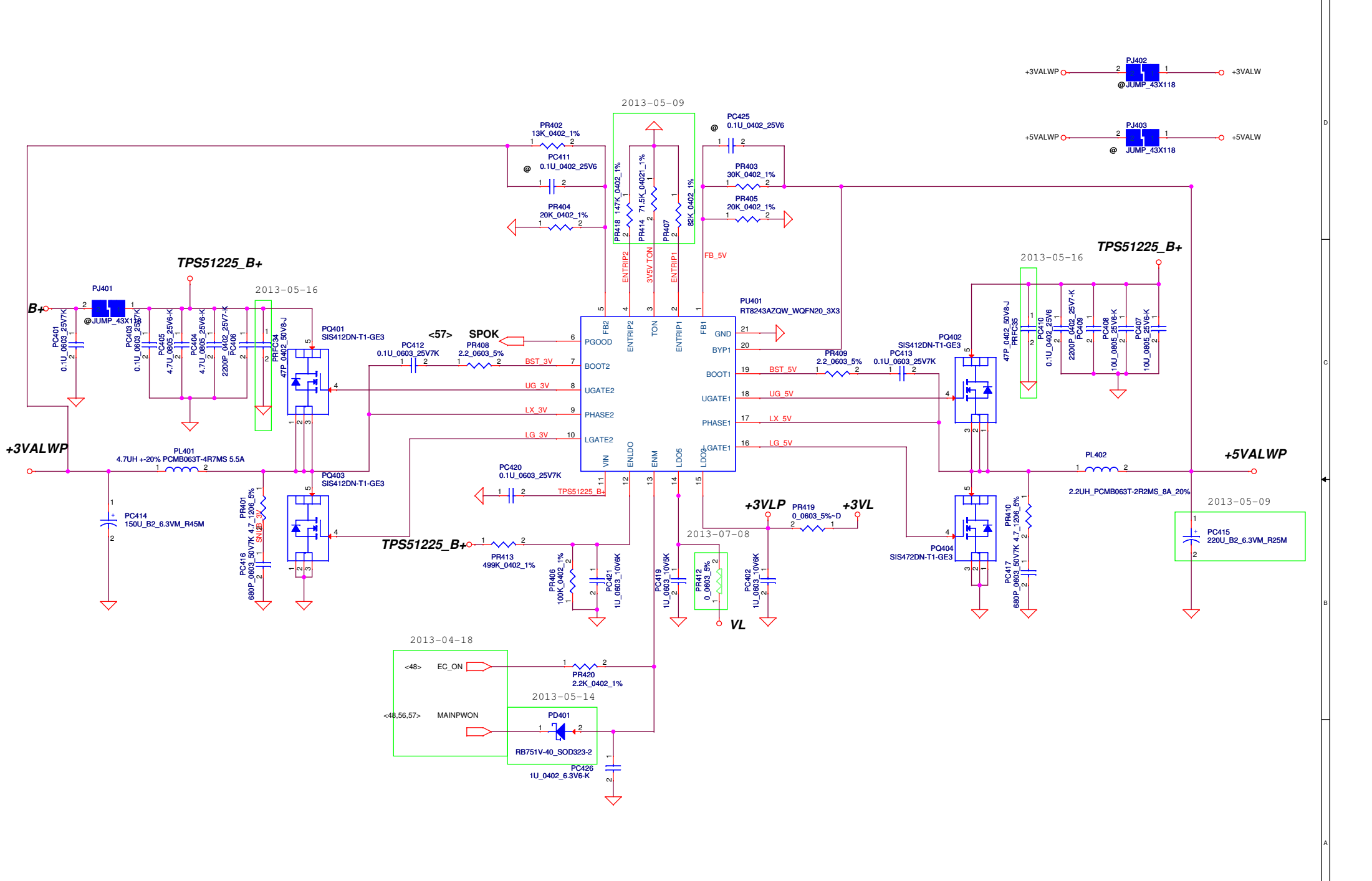
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A~3A  
 IREF=1.016\*Icharge  
 IREF=0.254V~3.048V  
 VCHLIM need over 95mV




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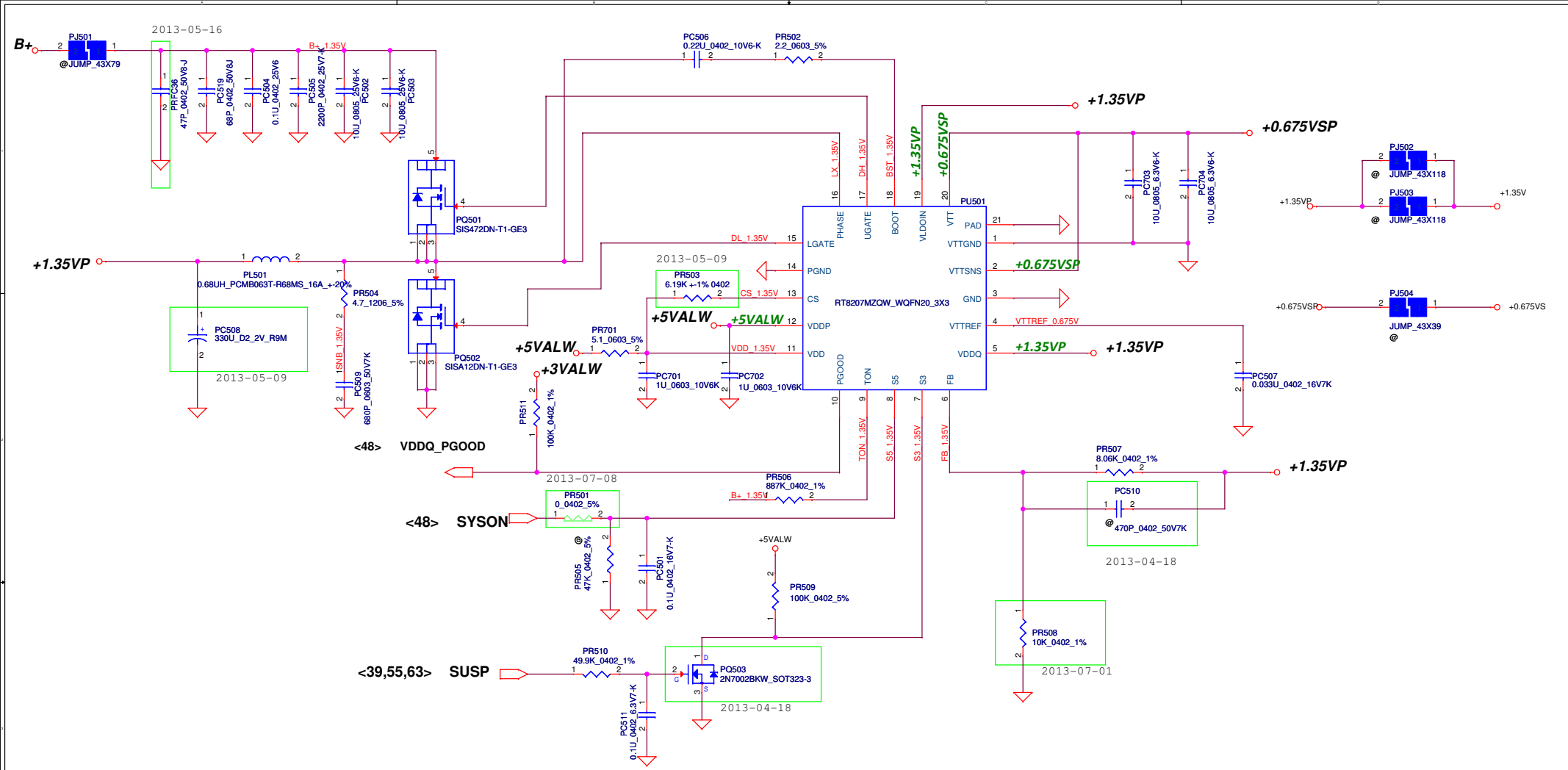
Title		
PWR-CHARGER-BQ24737		
Size	Document Number	<b>E440 NM-A151</b>
Custom		
Date:	Thursday, July 11, 2013	Sheet 58 of 69



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Issued Date	2012/07/01	Deciphered Date	2014/07/01
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Title		
PWR-3VALWP/5VALWP		
Size	Document Number	<b>E440 NM-A151</b>
Custom		
Date:	Thursday, July 11, 2013	Sheet 59 of 69

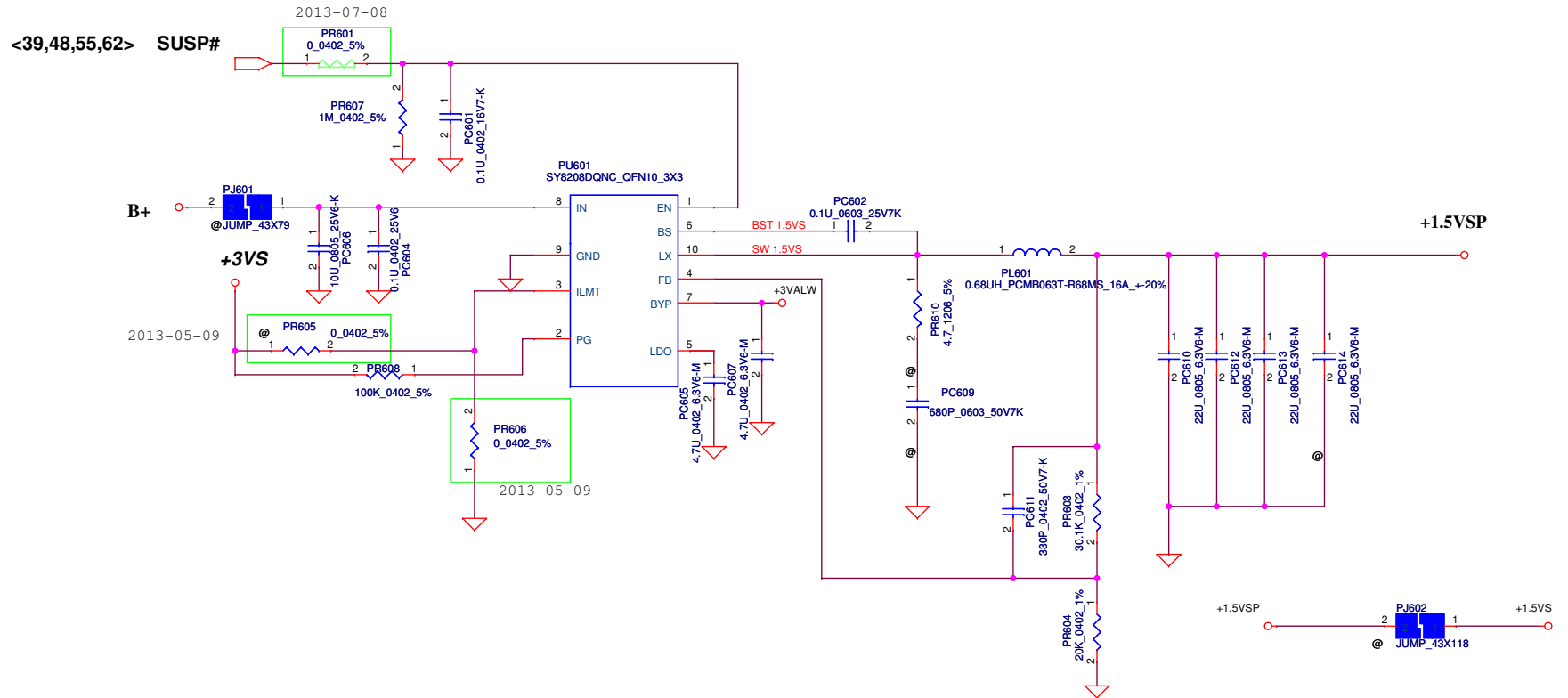
Rev 1.0




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Title	PWR-+1.35VP/+0.675VSP	
Size	Document Number	Rev
630	E440 NM-A151	1.0
Date:	Thursday, July 11, 2013	Sheet 60 of 69





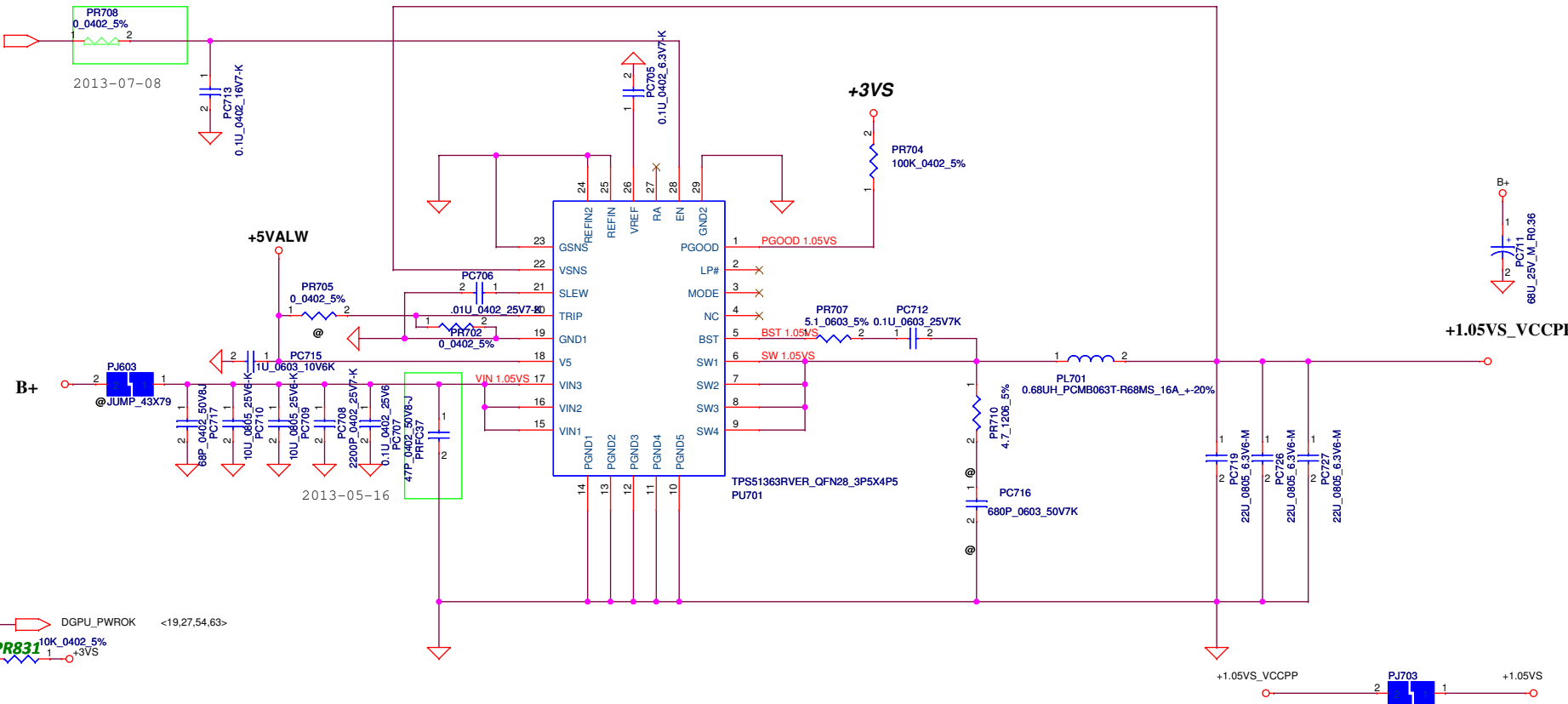
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Size	Custom	Document Number			
Date:	Thursday, July 11, 2013	Sheet		61	of 69

**E440 NM-A151** Rev 1.0

<39,48,55,61> SUSP#

PR708  
0.0402\_5%

2013-07-08



B+

+5VALW

+3VS

+1.05VS\_VCCPP

DGPU\_PWROK <19,27,54,63>  
PR831 10K\_0402\_5%  
+3VS

+1.05VS\_VCCPP  
PJ703  
JUMP\_43X118  
+1.05VS

+5VALW

SUSP#  
PR703  
0.0402\_5%

2013-07-08

PU702

SY8032ABC\_SOT23-6

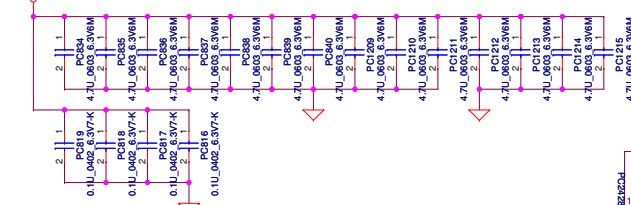
PL702  
1UH\_PH041H-1R0MS\_3.8A\_20%

+1.8VSP

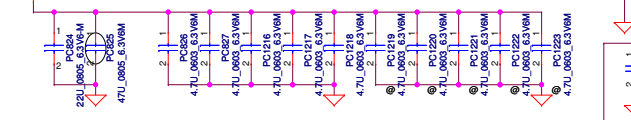
+1.8VSP  
PJ704  
JUMP\_43X39  
+1.8VS

Security Classification		LC Future Center Secret Data		Title	
Issued Date	2012/07/01	Deciphered Date	2014/07/01	PWR-+1.05VS_VCCPP/+1.8VSP	
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Size	Document Number	E440 NM-A151		Rev	1.0
Date:	Thursday, July 11, 2013	Sheet	62	of	69

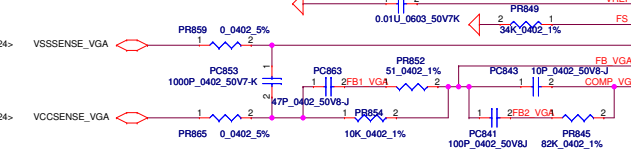
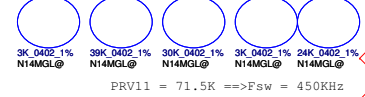
**+VGA\_CORE Under VGA Core GB4-128 package**



**+VGA\_CORE Near VGA Core**



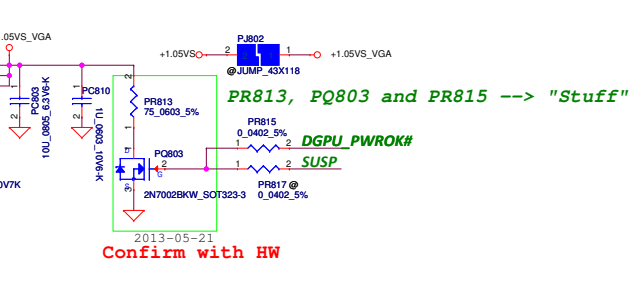
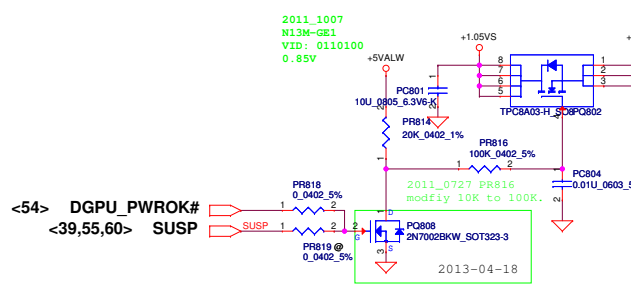
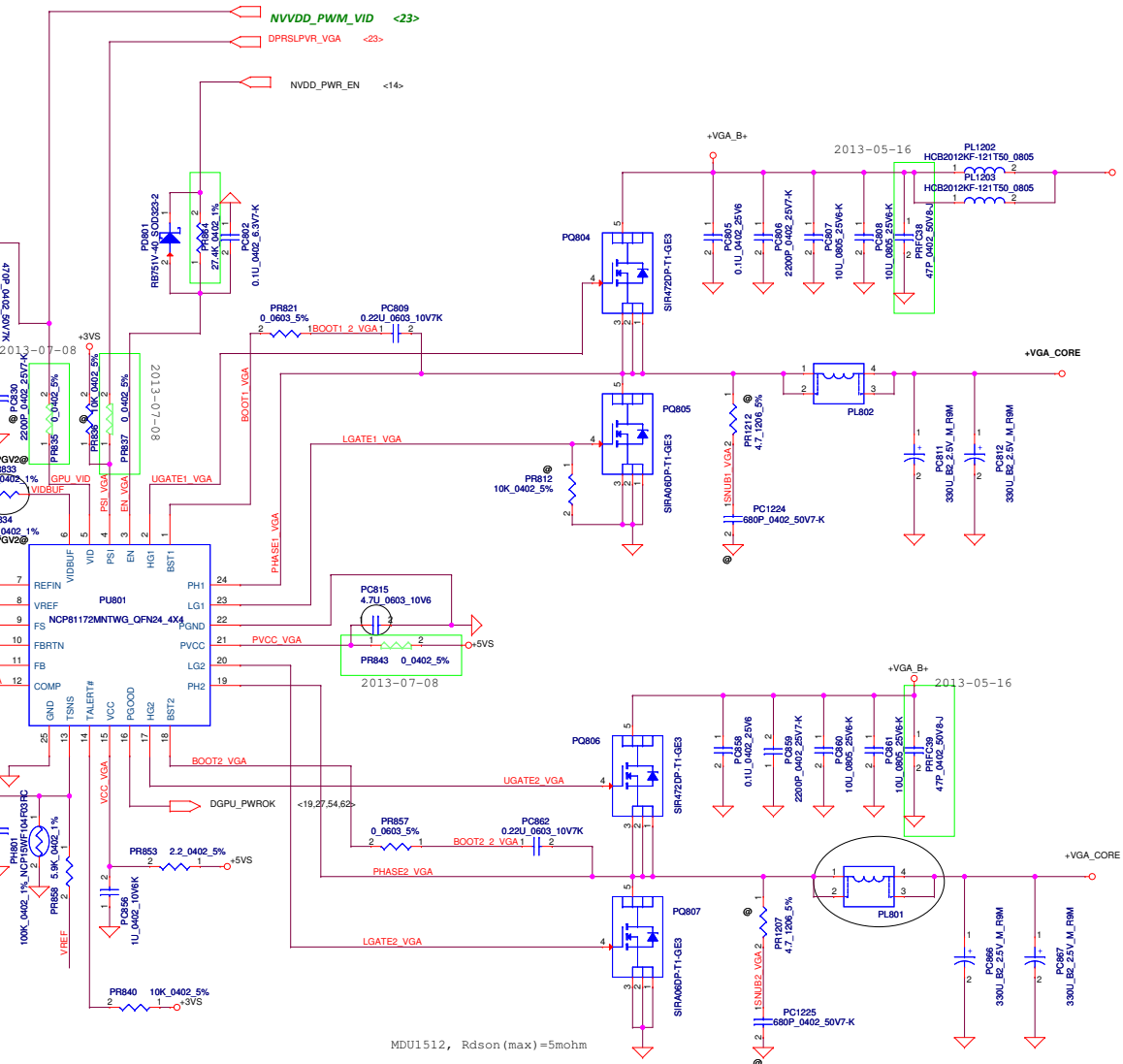
**PR834 PR833 PR844 PR846**



Thermistor near MOSFET trigger point 97 degree C.

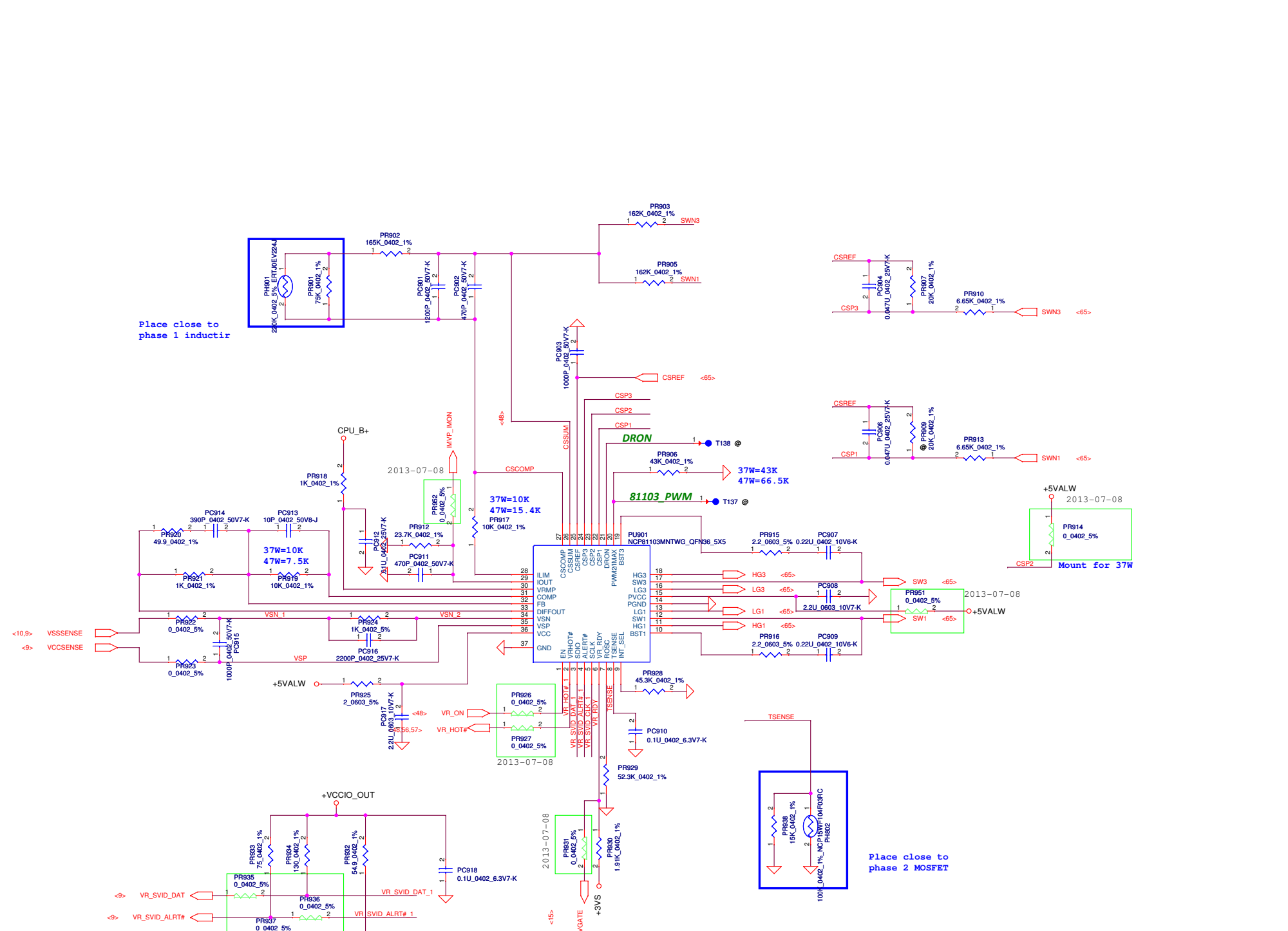
N14P-GT 35W Ipeak=50A Imax=35A Iocp=64.8A Fsw=450KHz bulk cap 330uF 9m \*4

N14P-GS 25W Ipeak=36A Imax=25A Iocp=64.8A Fsw=450KHz bulk cap 330uF 9m \*3



<54> DGPU\_PWROK# <39,55,60> SUSP

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			<b>E440 NM-A151</b>
			Rev 1.0
			Date: Thursday, July 11, 2013 (Sheet 63 of 69)




Place close to phase 1 inductor

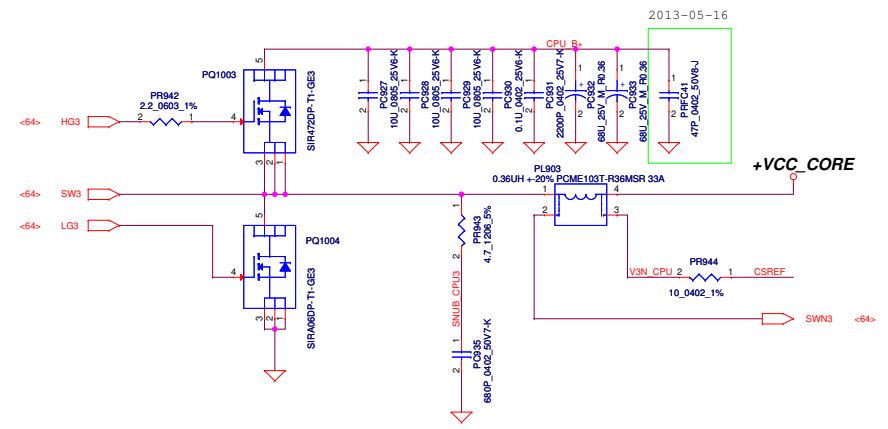
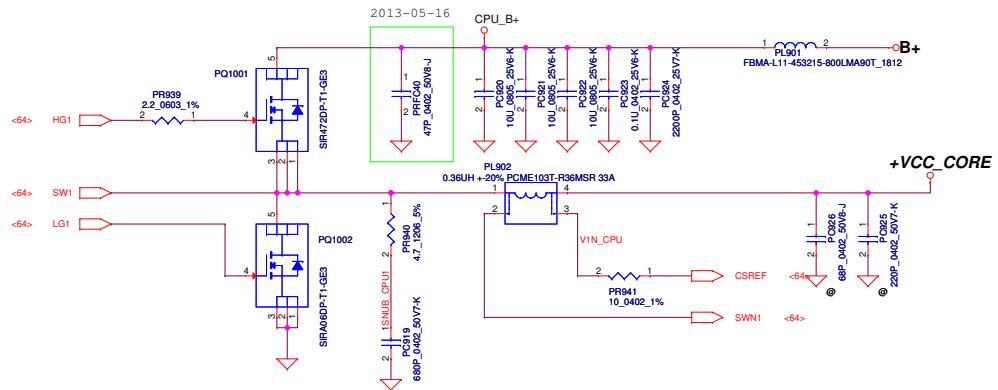
Place close to phase 2 MOSFET


Mount for 37W

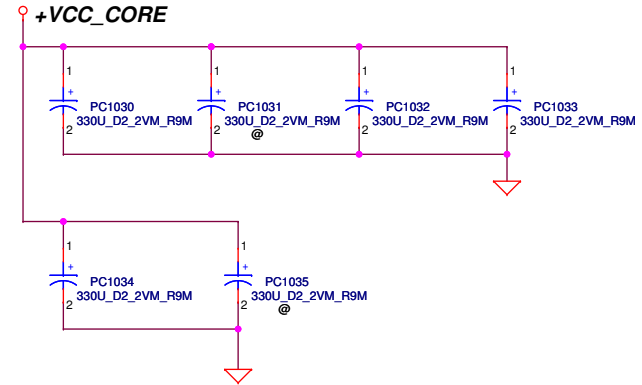
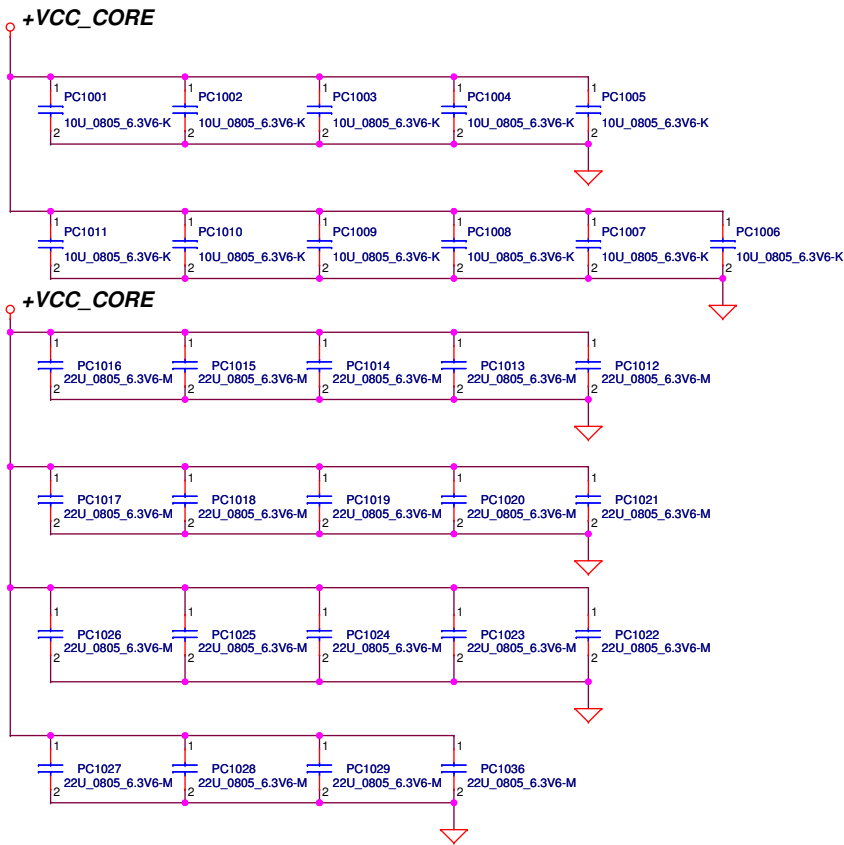
Security Classification	LC Future Center Secret Data	
Issued Date	2012/12/05	Deciphered Date
		2014/12/05
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Title		
CPU_CORE		
Size	Document Number	<b>E440 NW-A151</b>
Rev	1.0	
Date:	Thursday, July 11, 2013	Sheet 64 of 69



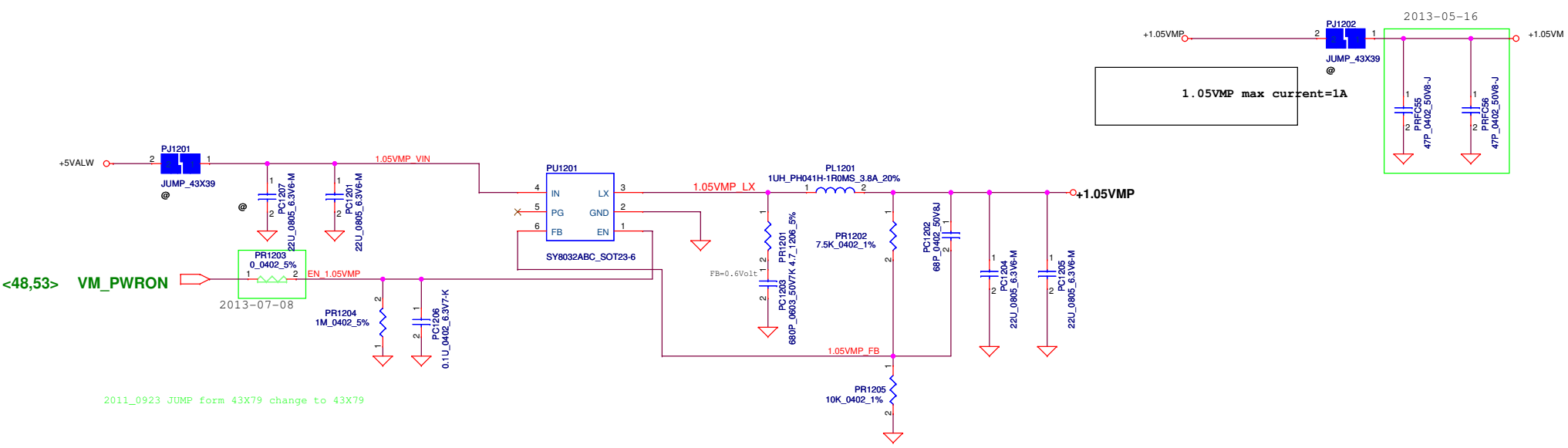


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			Document Number	Rev 1.0
			Date: Thursday, July 11, 2013	Sheet 66 of 69

**E440 NM-A151**



<48,53> VM\_PWRON

2013-07-08

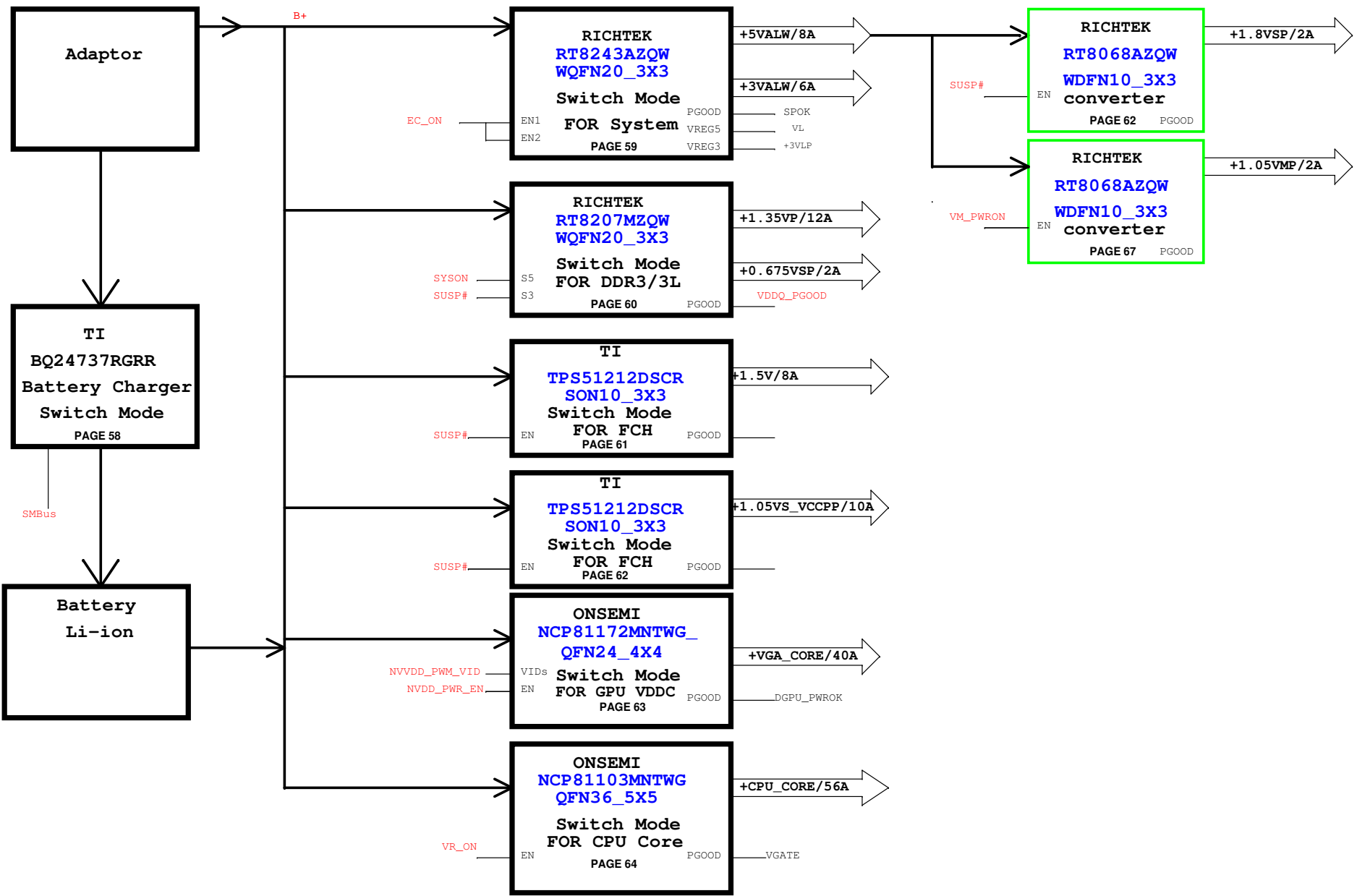
2011\_0923 JUMP Form 43X79 change to 43X79

Security Classification		LC Future Center Secret Data		Title	
Issued Date	2012/07/01	Deciphered Date	2014/07/01	PWR-+1.05VMP	
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				Date: Thursday, July 11, 2013	Rev 1.0
				Sheet 67	of 69

# POWER PIR (Product Improve Record)

AILE1 NM-A151 SCHEMATIC CHANGE LIST  
 REVISION CHANGE: 0.1  
 GERBER-OUT DATE: 2013/01/16

NO DATE PAGE MODIFICATION LIST PURPOSE



Security Classification	LC Future Center Secret Data		Title	
Issued Date	2012/12/05	Deciphered Date	2014/12/05	
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				Document Number <b>E440 NM-A151</b>
				Rev 1.0
				Date: Thursday, July 11, 2013 Sheet 68 of 69

# HW PIR (Product Improve Record)

AILE1 NM-A151 SCHEMATIC CHANGE LIST  
 REVISION CHANGE: 0.1  
 GERBER-OUT DATE: 2013/01/16

NO	DATE	PAGE		MODIFICATION LIST	PURPOSE
01)	03/14	10	R64	Change R64 BOM structure from "@" to "DS3@"	For Deep S3 Function

Security Classification	Compal Secret Data			Title	
Issued Date	2012/12/05	Deciphered Date	2014/12/05	PIR (PWR)	
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				Y490-LA8691P	1.0
Date: Thursday, July 11, 2013				Sheet	69 of 69