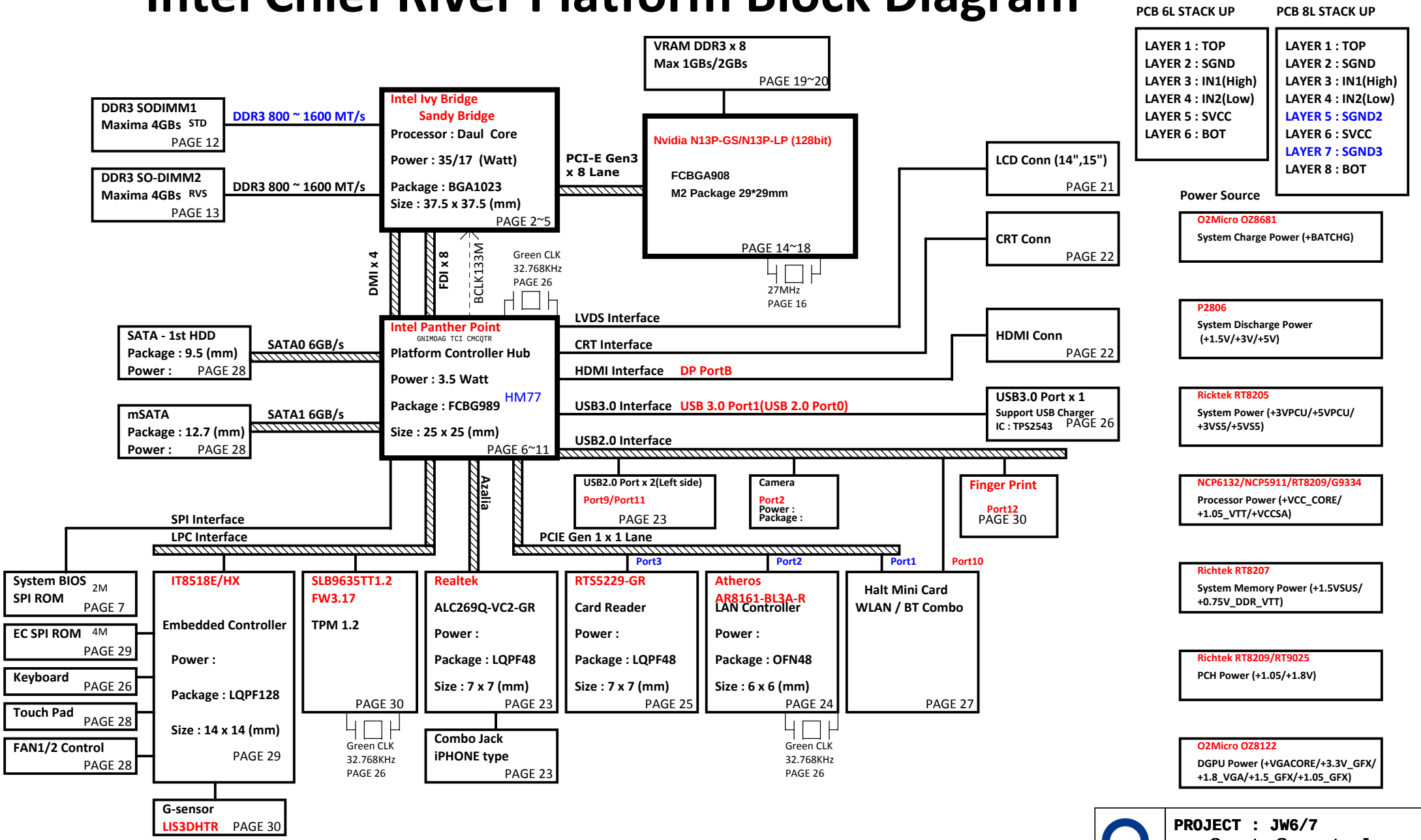
JW6/7 DIS/UMA (14",15") Ultra
Intel Chief River Platform Block Diagram

01



PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT

PCB 8L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SGND2
LAYER 6 : SVCC
LAYER 7 : SGND3
LAYER 8 : BOT

Power Source

O2Micro OZ8681
System Charge Power (+BATCHG)

P2806
System Discharge Power
(+1.5V/+3V/+5V)

Ricktek RT8205
System Power (+3VPCU/+5VPCU/
+3VS5/+5VS5)

NCP6132/NCP5911/RT8209/G9334
Processor Power (+VCC_CORE/
+1.05_VTT/+VCCSA)

Richtek RT8207
System Memory Power (+1.5VSUS/
+0.75V_DDR_VTT)

Richtek RT8209/RT9025
PCH Power (+1.05/+1.8V)

O2Micro OZ8122
DGPU Power (+VGACORE/+3.3V_GFX/
+1.8_VGA/+1.5_GFX/+1.05_GFX)

NB5

PROJECT : JW6/7
Quanta Computer Inc.

Size	Document Number	Rev
A3	Block Diagram	B

Date: Thursday, May 17, 2012 | Sheet 1 of 42

Ivy Bridge Processor (DMI,PEG,FDI)

02

PEG_COMP connect to PIN G3&G4 W:4mils/S:15mils/L: 500mils.
PEG_COMP connect to PIN G1 W:12mils/S:15mils/L: 500mils.

U14A

DMI
Intel(R) FDI
PCI EXPRESS -- GRAPHICS
eDP

IC,IVB_2CBGA,0P7

U14B

MISC
THERMAL
PWR MANAGEMENT
CLOCKS
DDR3 MISC
JTAG & BPM

IC,IVB_2CBGA,0P7

Place C626 Close to R394

Placement close to EC.

20120411,MV

CPU XDP

SM_RCOMP[0] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[1] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[2] W:15mils/S:20mils/L: 500mils,

PEG x8

CPU RESET#

20110816 modify:
REGULATOR DEL FOR SHORT

Intel DG request

DDR3 DRAM RESET

20110816 modify:
REGULATOR DEL FOR SHORT

SM_DRAMPWROK
Processor Input.

Processor pull-up (CPU)

eDP_COMPIO and ICOMPO signals should be shorted
near balls and routed with typical impedance <25 mohms

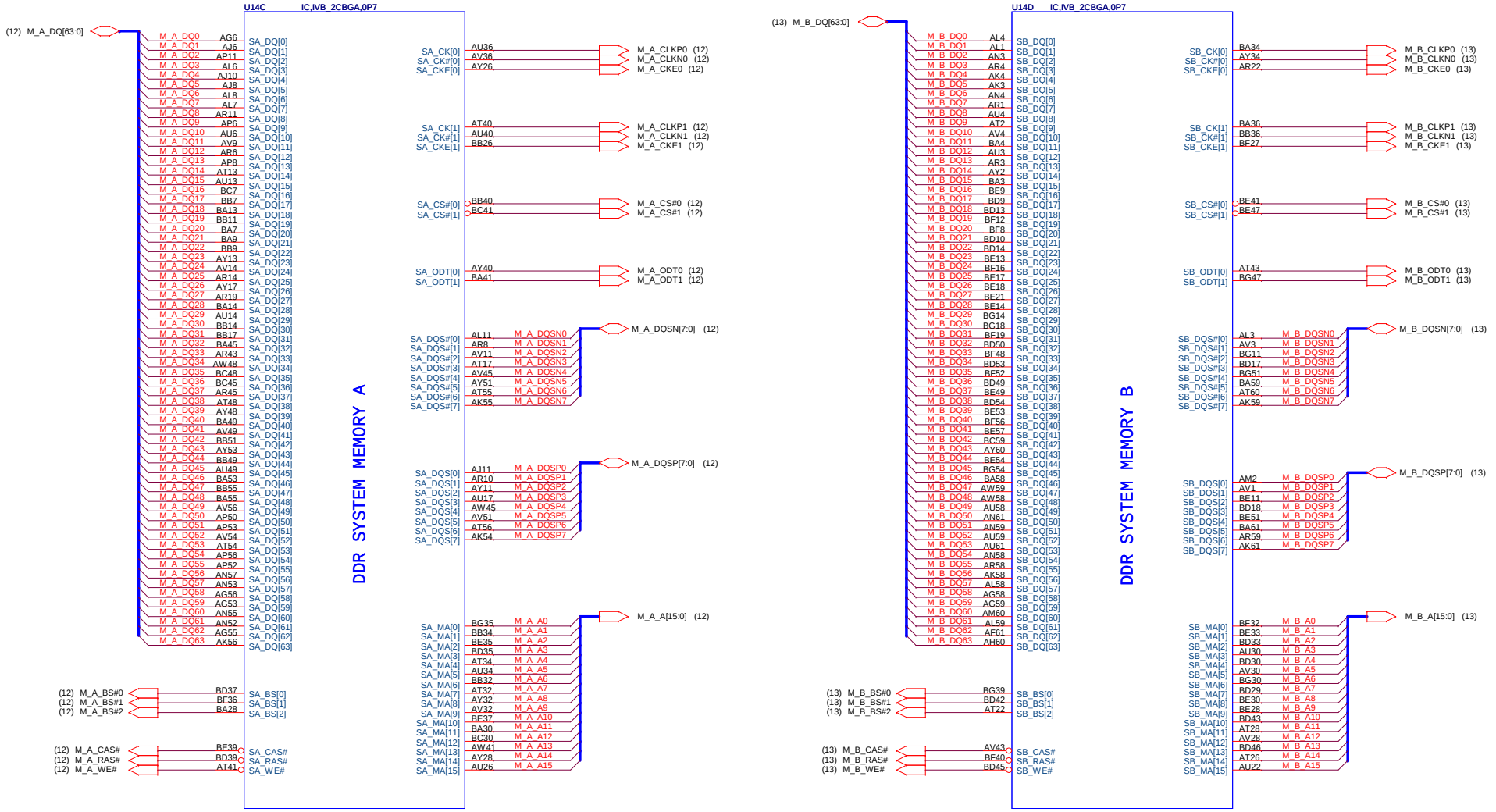
For iFDIM
Trigger Point

Connect a Test Point on BPM# 6 signal, very close to processor.

Connect a Test Point on BPM# 7 signal, very close to processor.

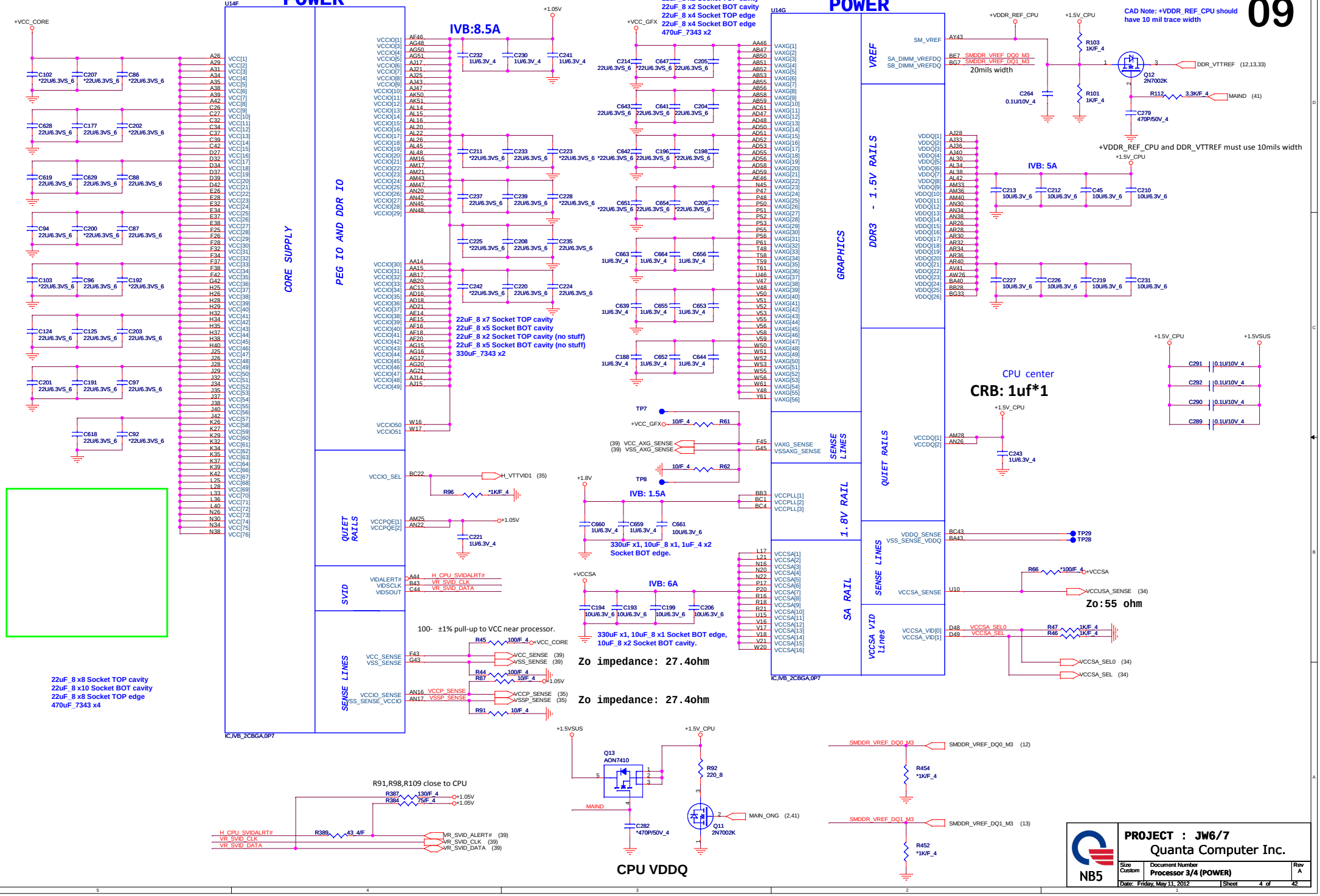
PROJECT :	JW6/7
	Quanta Computer Inc.
NB5	Size: Custom; Document Number: Processor 1/4 (Host/GPU); Rev: A
	Date: Friday, May 11, 2012; Sheet 2 of 42

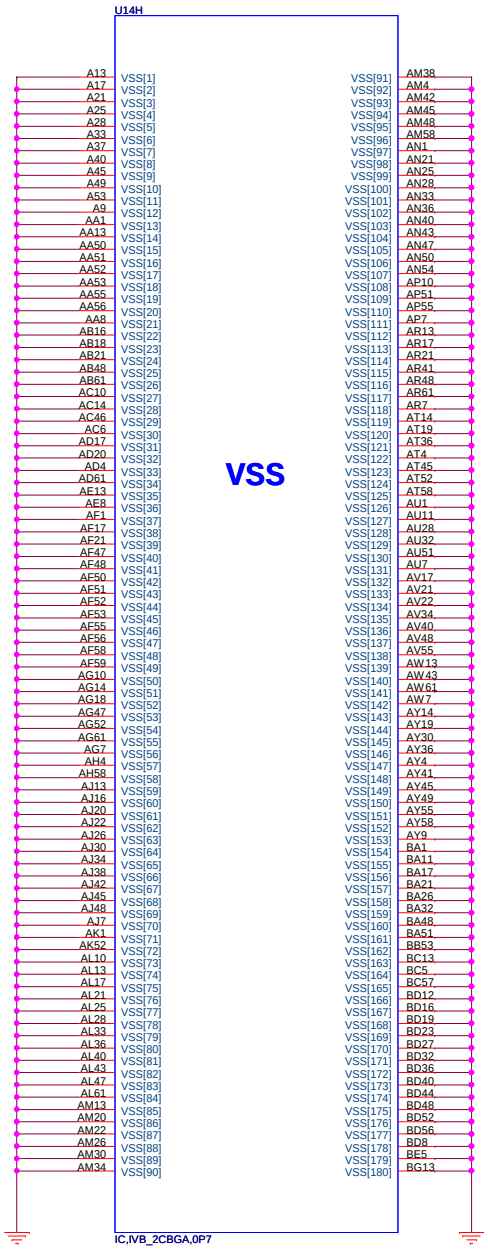
Ivy Bridge Processor (DDR3)

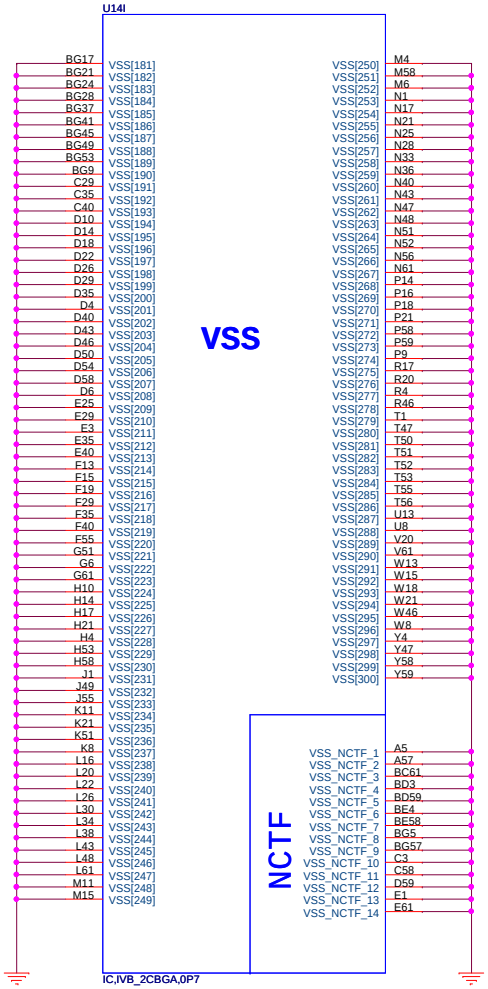


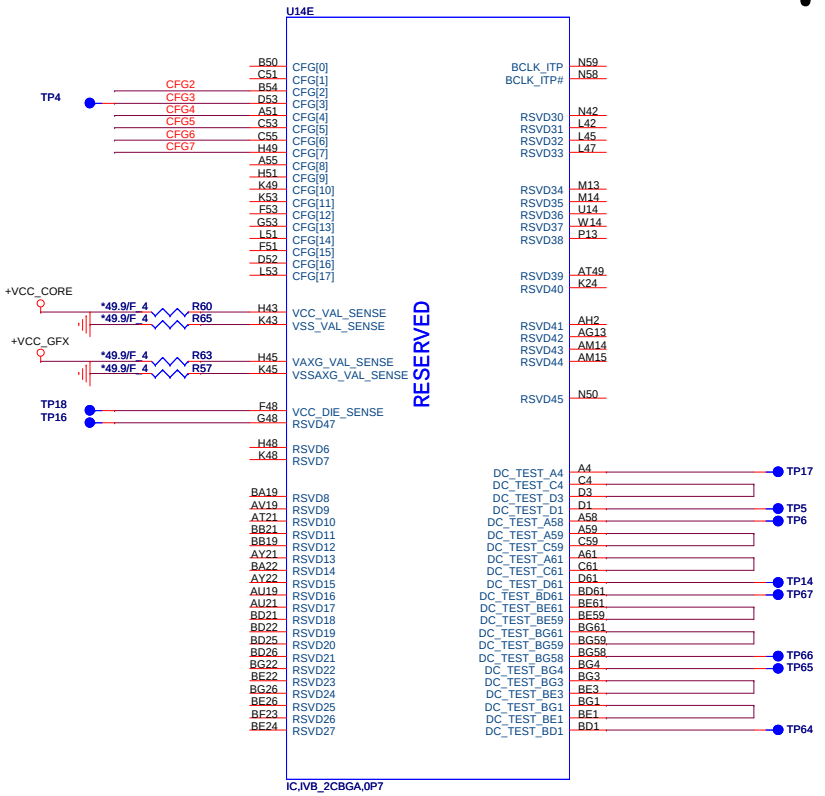
NB5	PROJECT : JW6/7 Quanta Computer Inc.	
Size: Custom	Document Number: Processor 2/5 (DDR3 I/F)	Rev: A
Date: Friday, May 11, 2012	Sheet 3 of 42	

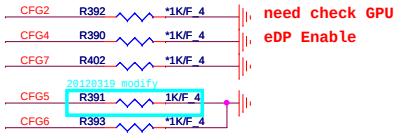
POWER











CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

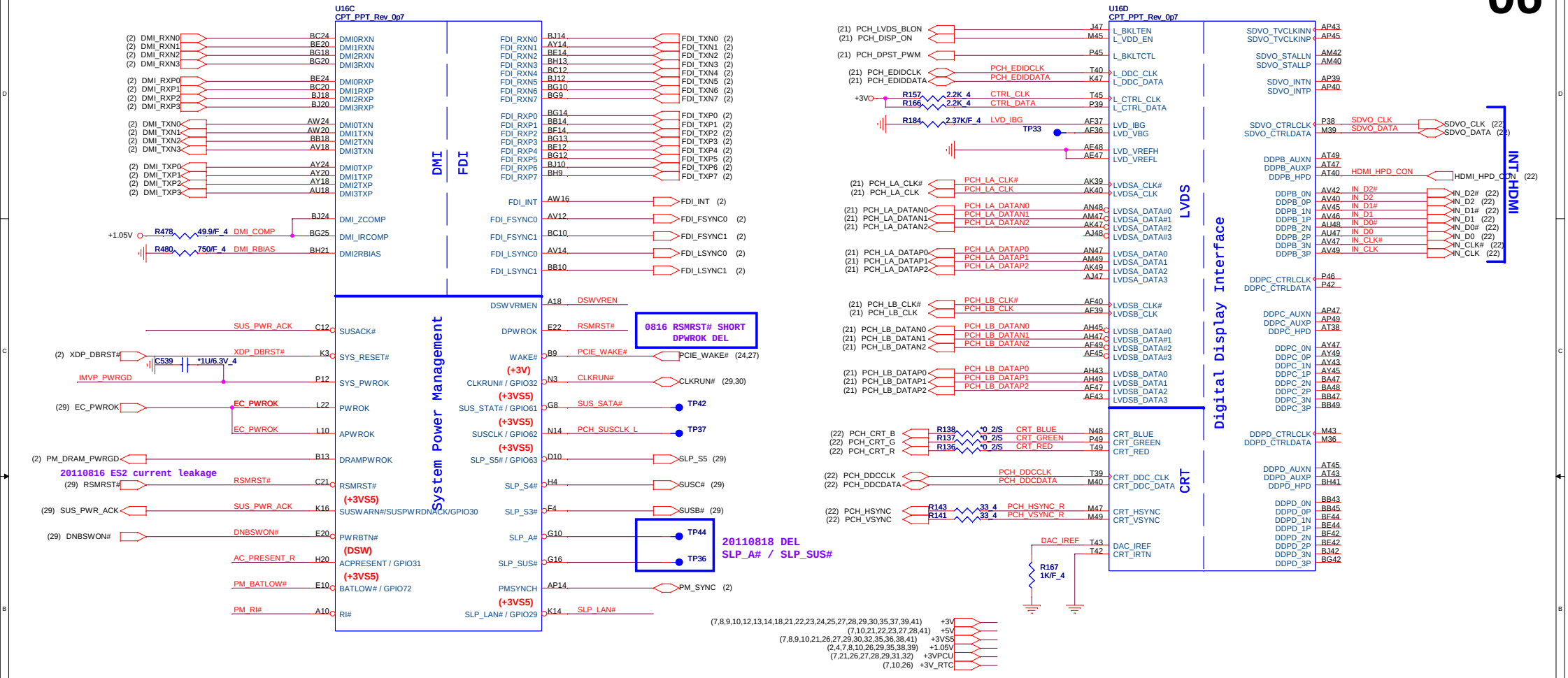
	1	0
CFG2 (PCIe Static x16 Lane Numbering Reversal.)	Normal Operation(Default)	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP

NB5	PROJECT : JW6/7 Quanta Computer Inc.	
	Size: Custom Document Number: Processor 4/4 (RSV,Ground)	Rev: A
	Date: Friday, May 11, 2012	Sheet 5 of 42

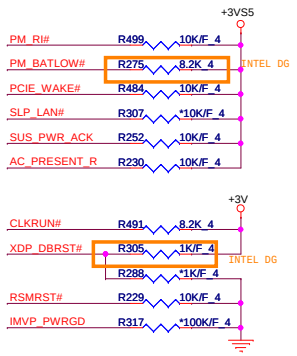
Cougar Point/Panther Point (DMI,FDI,PM)

Cougar Point/Panther Point (LVDS,DDI)

06

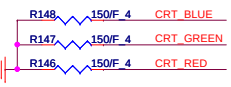


PCH Pull-high/low(CLG)

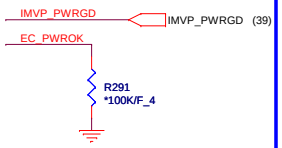


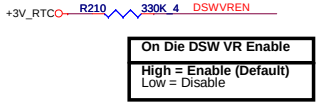
PD Res place close to PCH

PCH to Res routeing 50 ohm Impedance.
Res to connector filter routeing 37.5ohm Impedance.



System PWR_OK(CLG)



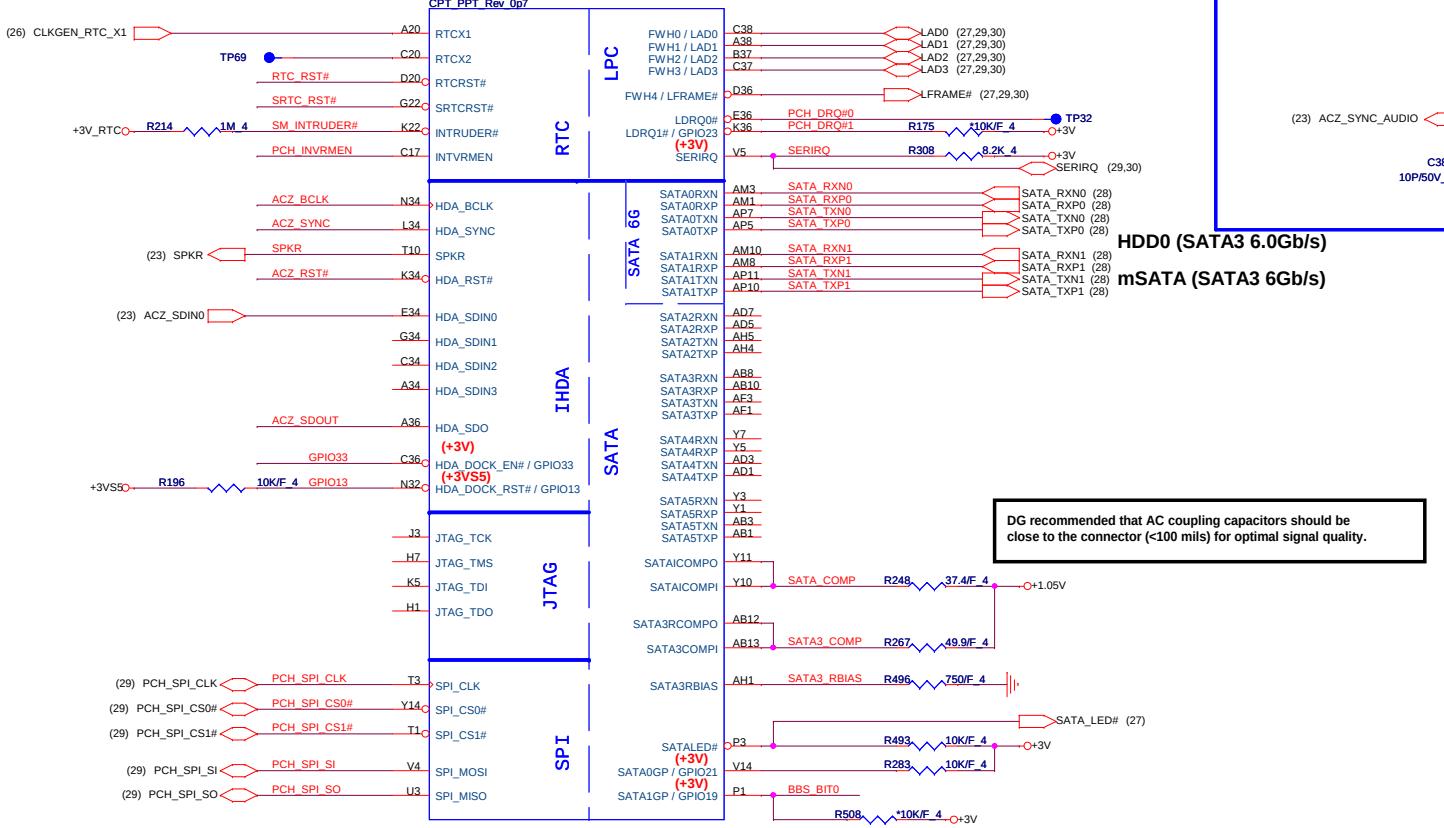


PROJECT : JW6/7
Quanta Computer Inc.

NB5

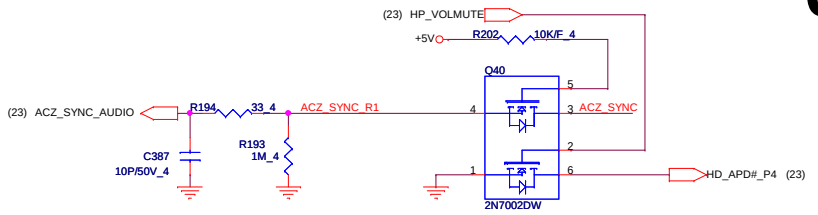
Size	Document Number	Rev
Custom	PCH 1/6 (Host/Display)	A
Date: Monday, May 14, 2012	Sheet 6 of 42	

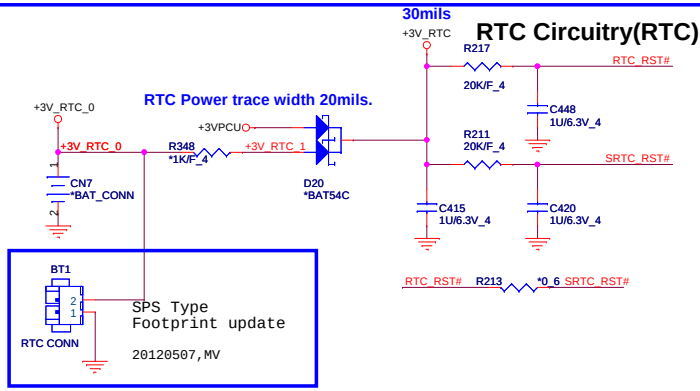
Cougar Point/Panther Point (HDA,JTAG,SATA)

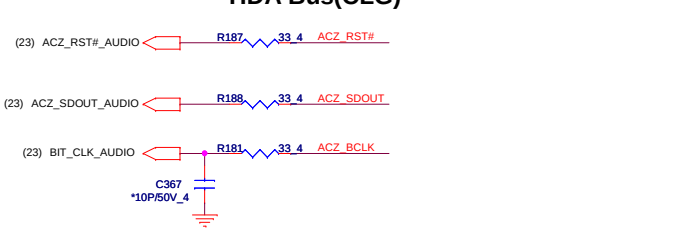


07

20120201,B





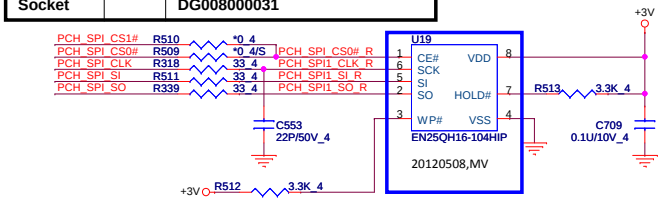


PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# 1 0 / GNT0# 1 0 / Boot Location SPI LPC	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#
GPIO19	Different from Calpella Boot BIOS Selection 0 [bit-0]	PWROK		
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	
DF_TVS	DMI and FDI Tx/Rx Termination Voltage	PWROK	weak pull-down 20kohm	
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	Rising edge of PWROK	1 = Override 0 = Default (weak pull-down 20K)	

Vender	Size	P/N
EON	2MB	AKE38ZN0Q00 (EN25QH16-104HIP)
AMIC	2MB	AKE38ZN0802 (A25LQ16M-F/Q)
Socket		DG008000031

PCH SPI ROM(CLG)



+3V (6,8,9,10,12,13,14,18,21,22,23,24,25,27,28,29,30,35,37,39,41)
+5V (10,21,22,23,27,28,41)
+1.8V (4,10,36)
+1.05V (2,4,6,8,10,26,29,35,38,39)
+3VS5 (6,8,9,10,21,26,27,29,30,32,35,36,38,41)
+3VPCU (21,26,27,28,29,31,32)
+3V_RTC (6,10,26)

PROJECT : JW6/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 2/6 (HDA/RTC/SATA/SPI)	A
Date: Friday, May 11, 2012	Sheet 7 of 42	

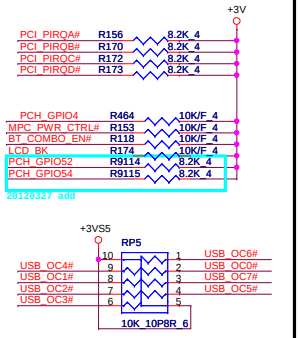
NB5

Cougar Point-M/Panther Point (PCI,USB,NVRAM)

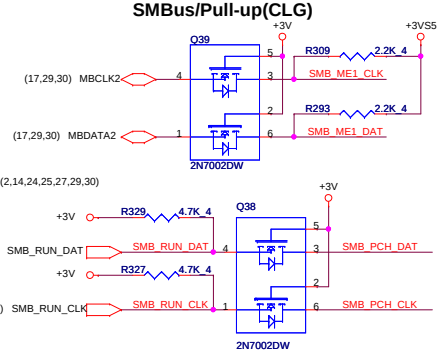
Cougar Point-M/Panther Point (PCI-E,SMBUS,CLK)

08

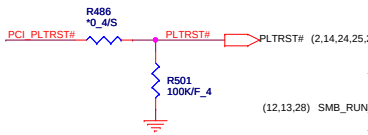
PCI/USBOC# Pull-up(CLG)



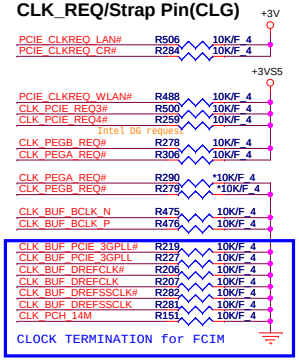
SMBus/Pull-up(CLG)



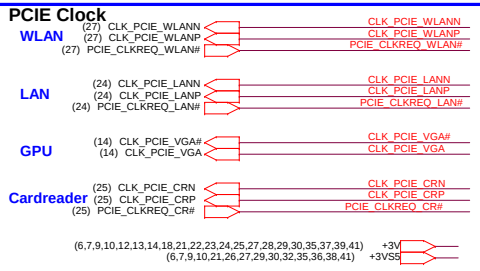
PLTRST#(CLG)



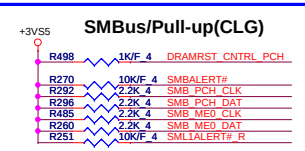
CLK_REQ/Strap Pin(CLG)



PCIE Clock



SMBus/Pull-up(CLG)



MPC Switch Control

MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)

MPC_PWR_CTRL# R154 *1K/F_4

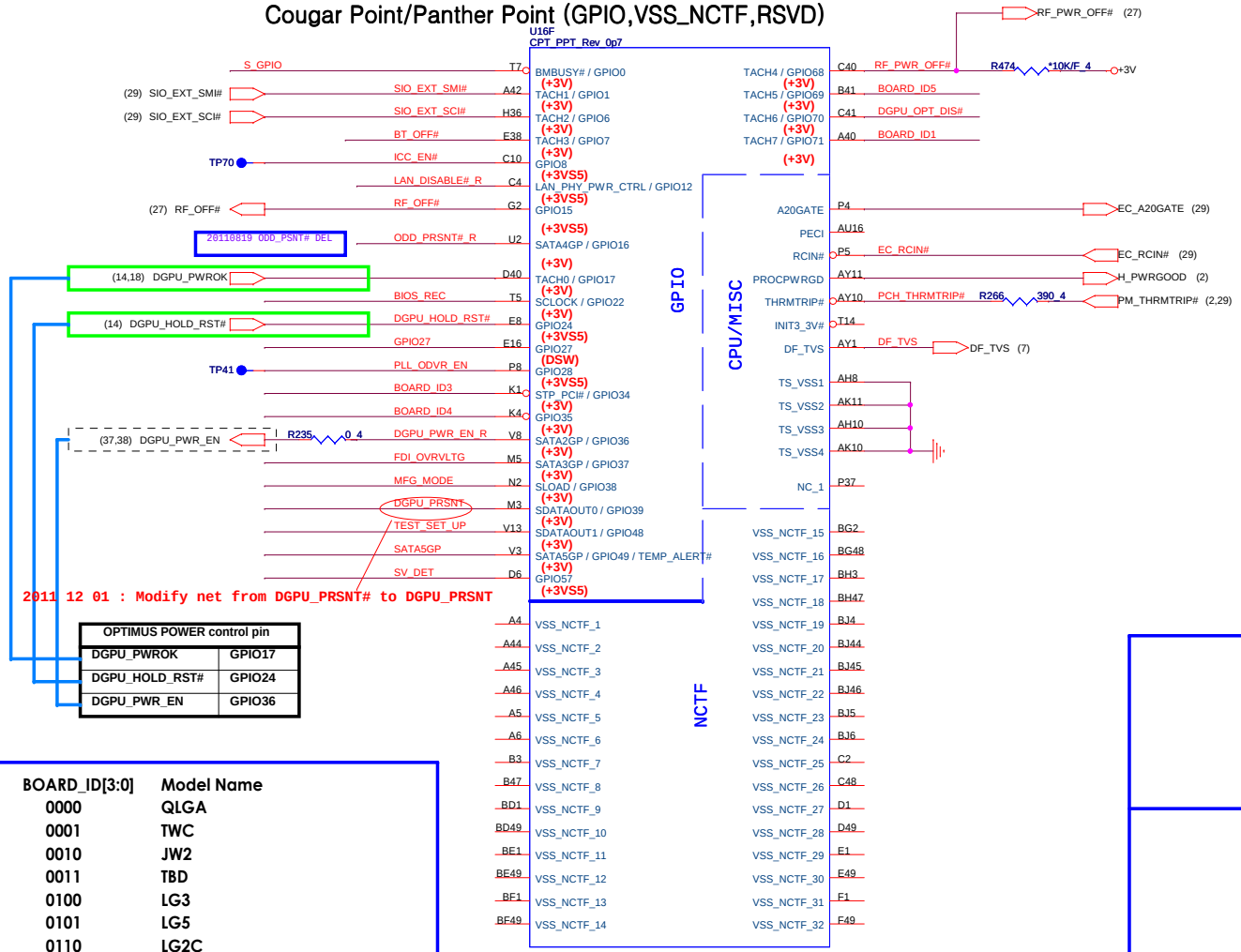
20111130 Modify USB3.0 for HM70

EMI(near PCH)

Size: Custom	Document Number: PCH 3/6 (Clock/PCI/PCIE/USB)		Rev: A
Date: Friday, May 11, 2012	Sheet: 8 of 42		

PROJECT : JW6/7
Quanta Computer Inc.
NB5

Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)



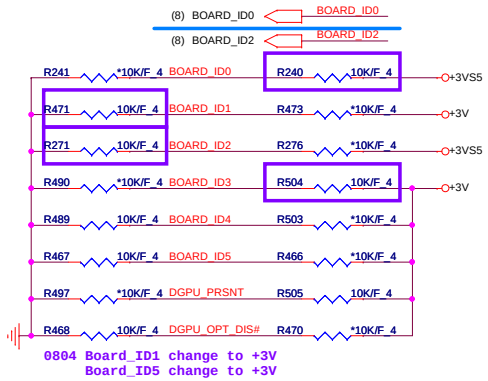
OPTIMUS POWER control pin	
DGPU_PWROK	GPIO17
DGPU_HOLD_RST#	GPIO24
DGPU_PWR_EN	GPIO36

BOARD_ID[3:0]	Model Name
0000	QLGA
0001	TWC
0010	JW2
0011	TBD
0100	LG3
0101	LG5
0110	LG2C
0111	LG4C
1000	TBD
1001	JW6/JW7
1010	JW3
1011	JW6H/JW6L
1100	JW3H

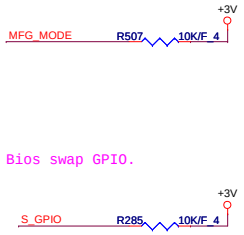
Chief River BOARD ID SETTING

BOARD_ID0	GPIO44	MODEL BIT0
BOARD_ID1	GPIO71	MODEL BIT1
BOARD_ID2	GPIO46	MODEL BIT2
BOARD_ID3	GPIO34	MODEL BIT3
BOARD_ID4	GPIO35	Reserve and pull low
BOARD_ID5	GPIO69	HM77=0,HM70=1
DGPU_PRSNT	GPIO39	Optimus=1, UMA=0
DGPU_OPT_DIS#	GPIO70	Optimus=0, Dis only=1

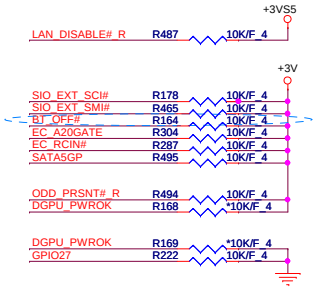
20110816 Define BRD_ID[3:0]

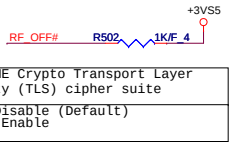


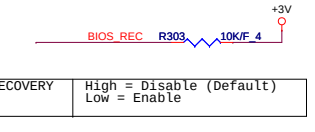
MFG-TEST

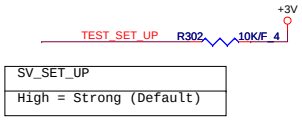


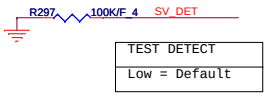
GPIO Pull-up/Pull-down(CLG)











SATA2GP/GPIO36	Reserved only

(6,7,8,10,12,13,14,18,21,22,23,24,25,27,28,29,30,35,37,39,41) +3V
(6,7,8,10,21,26,27,29,30,32,35,36,38,41) +3VS5

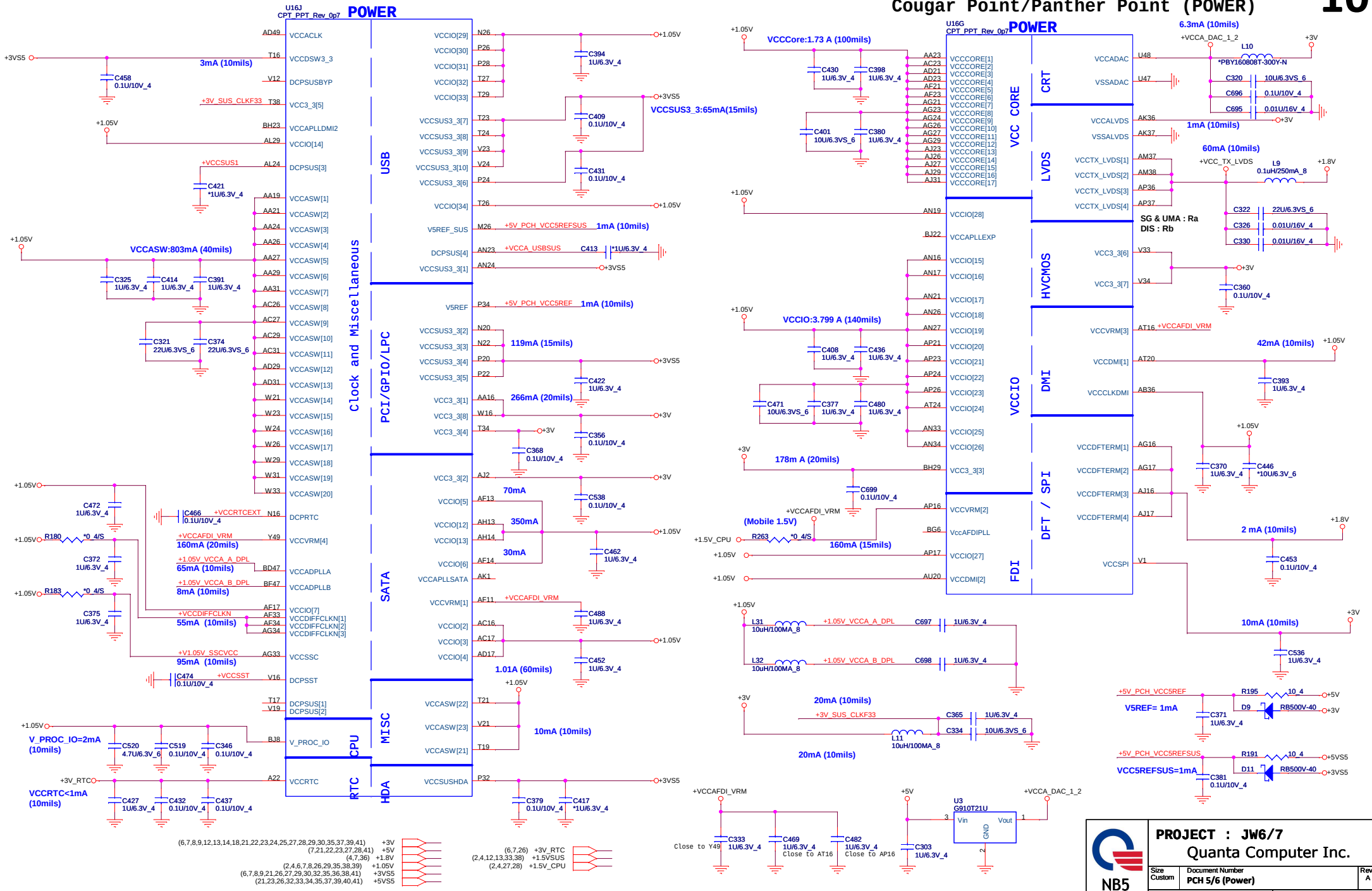
PROJECT : JW6/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 4/6 (GPIO)	A
Date: Tuesday, May 15, 2012	Sheet 9 of 42	

NB5

Cougar Point/Panther Point (POWER)

Cougar Point/Panther Point (POWER)

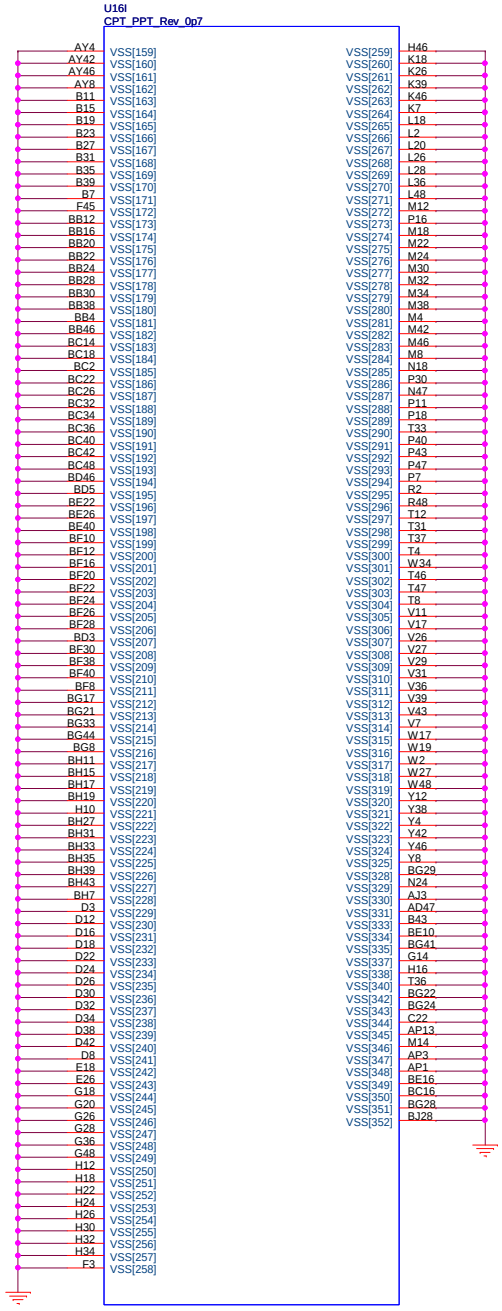


(6,7,8,9,12,13,14,18,21,22,23,24,25,27,28,29,30,35,37,39,41) +3V
(7,21,22,23,27,28,41) +5V
(4,7,36) +1.8V
(2,4,6,7,8,26,29,35,38,39) +1.05V
(6,7,8,9,21,26,27,29,30,32,35,36,38,41) +3VS5
(21,23,26,32,33,34,35,37,39,40,41) +5VS5

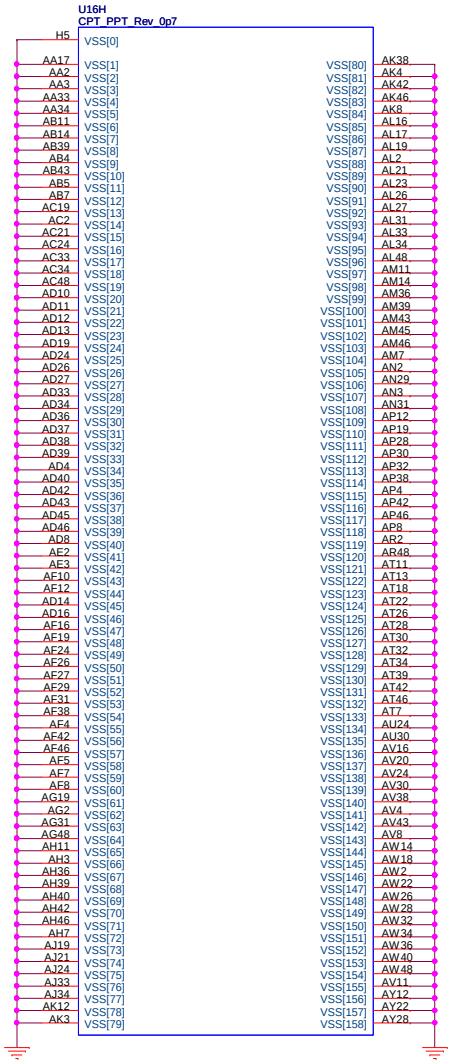
(6,7,26) +3V_RTC
(2,4,12,13,33,38) +1.5VSUS
(2,4,27,28) +1.5V_CPU

Quanta Computer Inc.	PROJECT : JW6/7		
NB5	Size: Custom	Document Number: PCH 5/6 (Power)	Rev: A
	Date: Friday, May 11, 2012	Sheet: 10of	42

Cougar Point/Panther Point (GND)



Cougar Point/Panther Point (GND)



PROJECT : JW6/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 6/6 (Ground)	A

NB5

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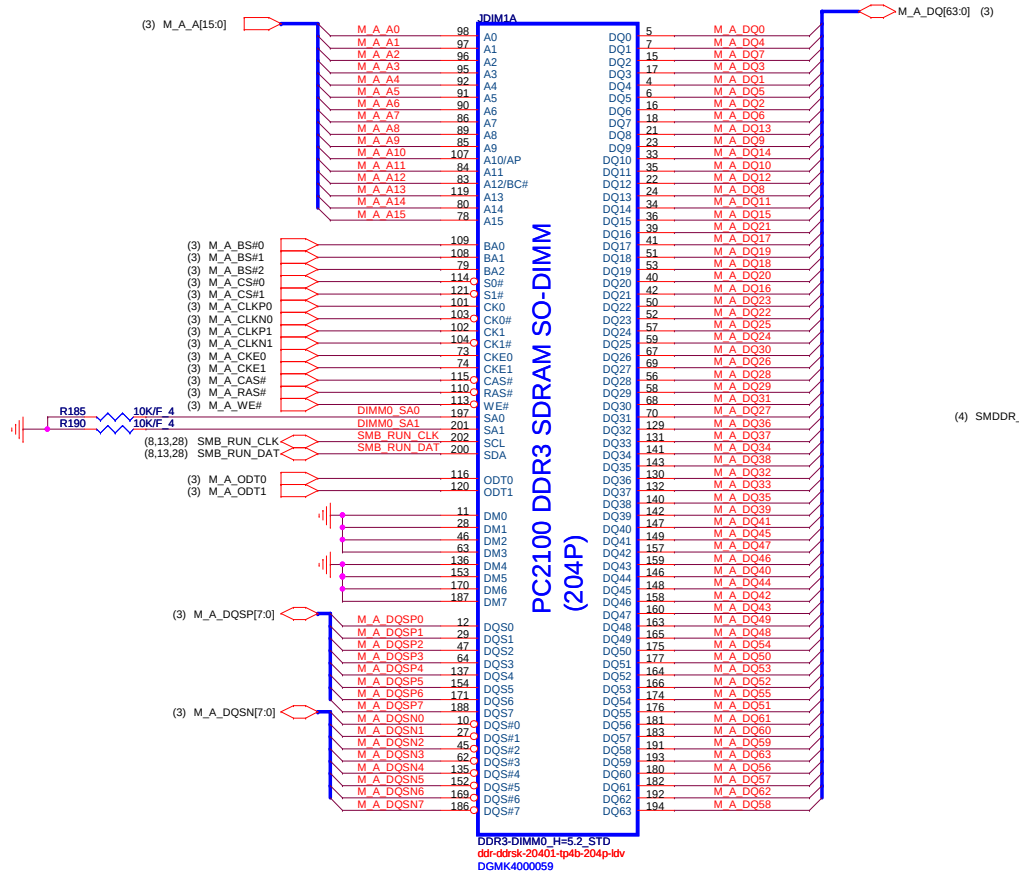
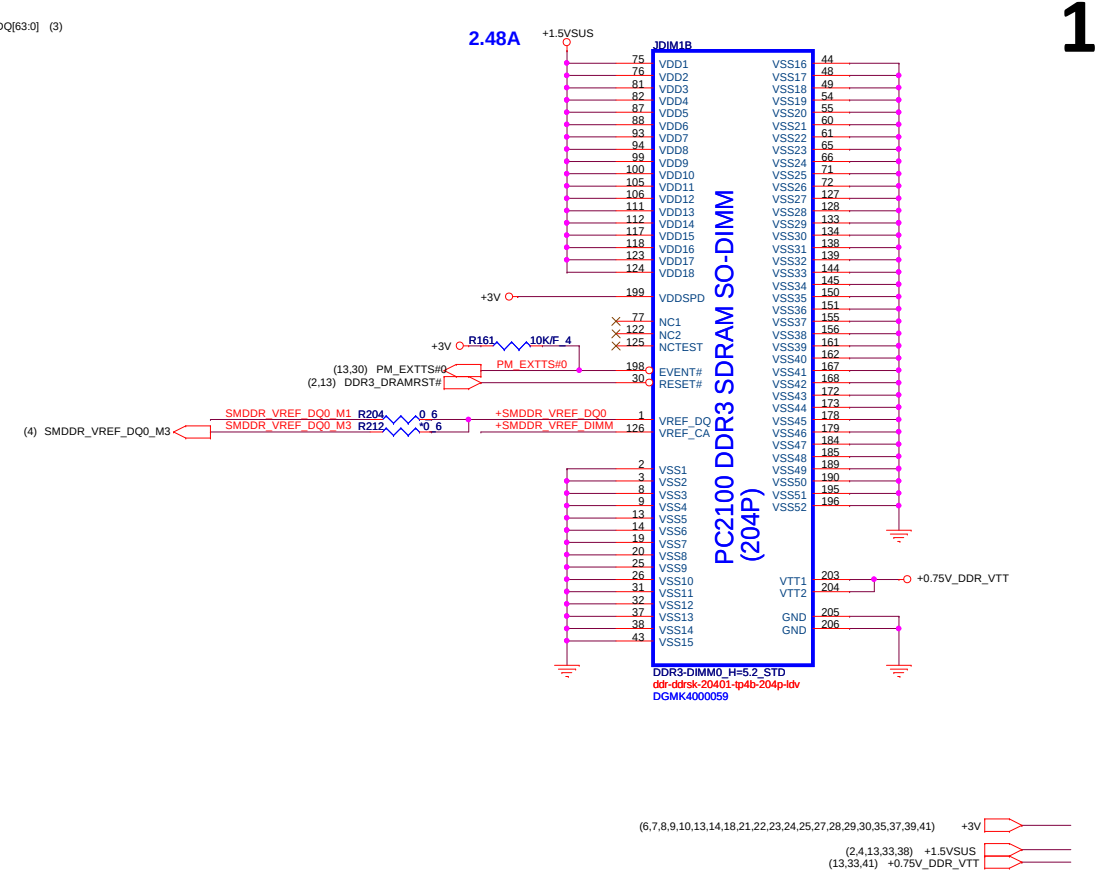
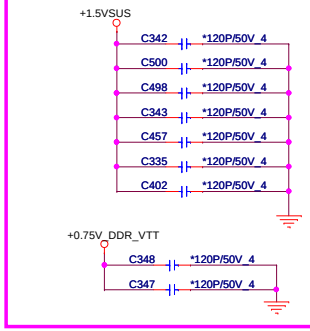
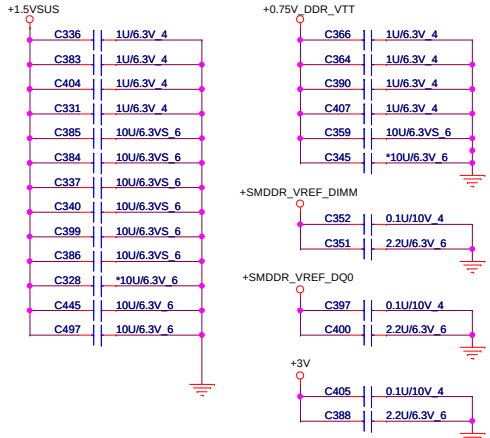




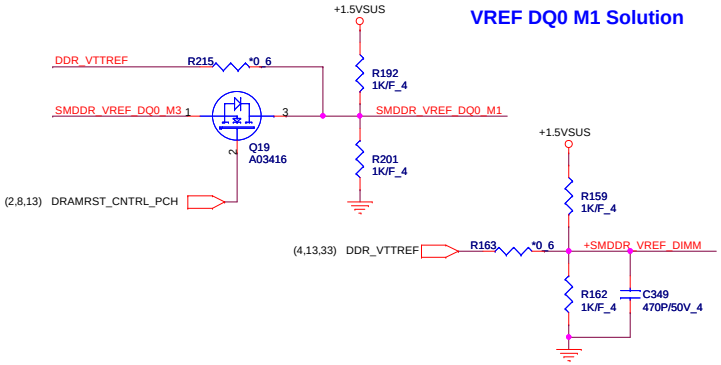
For EMI RESERVE 8/30



Place these Caps near So-Dimm0.



VREF DQ0 M1 Solution



NB5	PROJECT : JW6/7 Quanta Computer Inc.	
Size: Custom	Document Number: System Memory 1/2 (5.2H)	Rev: A
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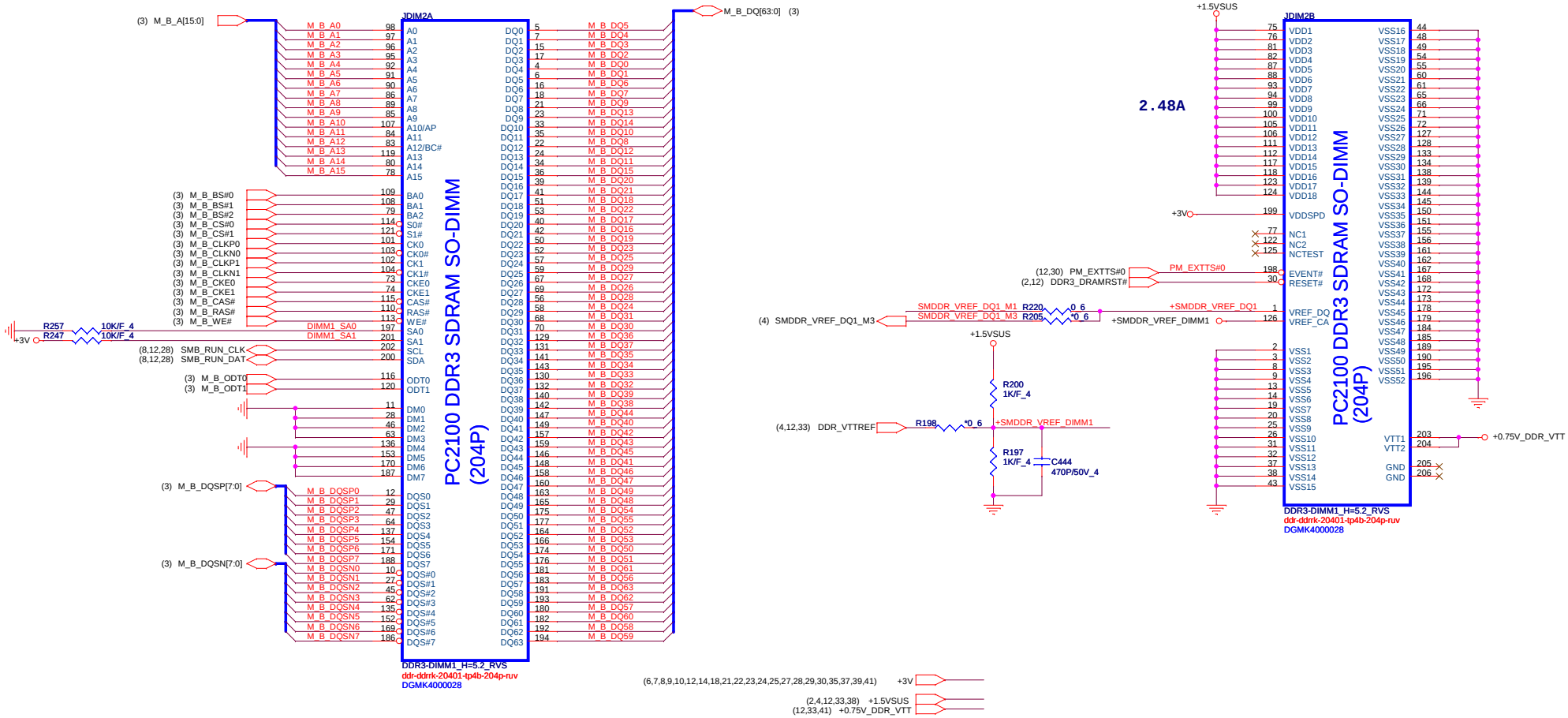
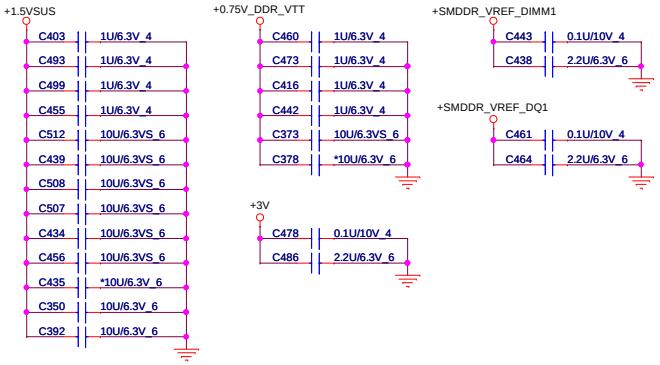
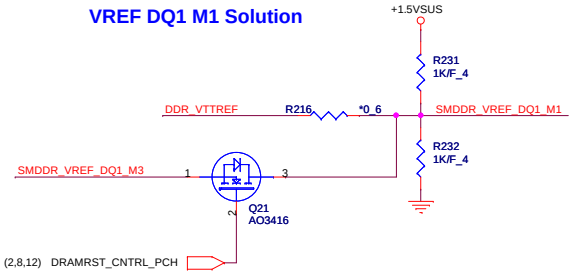


Place these Caps near So-Dimm1.



VREF DQ1 M1 Solution



NB5	PROJECT : JW6/7 Quanta Computer Inc.	
Size: Custom	Document Number: System Memory 2/2 (9.2H)	Rev: A
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+1.05V_GFX

To be placed no further from the GPU than bewteen the PS and GPU

C63 22U/6.3VS_6
C64 22U/6.3VS_6
C112 10U/6.3VS_6
C114 10U/6.3VS_6
PLACE UNDER BGA
C113 4.7U/6.3V_6
C106 1U/6.3V_4
PLACE NEAR BALLS
C117 1U/6.3V_4

+1.05V_GFX

To be placed no further from the GPU than bewteen the PS and GPU

C57 22U/6.3VS_6
C56 22U/6.3VS_6
C69 10U/6.3VS_6
C68 10U/6.3VS_6
PLACE UNDER BGA
C115 4.7U/6.3V_6
C107 1U/6.3V_4
PLACE NEAR BALLS
C108 1U/6.3V_4

0727 PEX_IOVDD/Q
TOTAL 3500mA

U13A

[PEG Interface]
0.088mA

2500mA

AG19 PEX_IOVDD_1
AG21 PEX_IOVDD_2
AG22 PEX_IOVDD_3
AG24 PEX_IOVDD_4
AH21 PEX_IOVDD_5
AH25 PEX_IOVDD_6

AG13 PEX_IOVDDQ_1
AG15 PEX_IOVDDQ_2
AG16 PEX_IOVDDQ_3
AG18 PEX_IOVDDQ_4
AG25 PEX_IOVDDQ_5
AH15 PEX_IOVDDQ_6
AH18 PEX_IOVDDQ_7
AH26 PEX_IOVDDQ_8
AH27 PEX_IOVDDQ_9
AJ27 PEX_IOVDDQ_10
AK27 PEX_IOVDDQ_11
AL27 PEX_IOVDDQ_12
AM28 PEX_IOVDDQ_13
AN28 PEX_IOVDDQ_14

PEX_RX0 AN12 PEG_TX0 — PEG_TX0 (2)
PEX_RX0_N AM12 PEG_TX#0 — PEG_TX#0 (2)
PEX_RX1 AN14 PEG_TX1 — PEG_TX1 (2)
PEX_RX1_N AM14 PEG_TX#1 — PEG_TX#1 (2)
PEX_RX2 AP14 PEG_TX2 — PEG_TX2 (2)
PEX_RX2_N AP15 PEG_TX#2 — PEG_TX#2 (2)
PEX_RX3 AN15 PEG_TX3 — PEG_TX3 (2)
PEX_RX3_N AM15 PEG_TX#3 — PEG_TX#3 (2)
PEX_RX4 AN17 PEG_TX4 — PEG_TX4 (2)
PEX_RX4_N AM17 PEG_TX#4 — PEG_TX#4 (2)
PEX_RX5 AP17 PEG_TX5 — PEG_TX5 (2)
PEX_RX5_N AP18 PEG_TX#5 — PEG_TX#5 (2)
PEX_RX6 AN18 PEG_TX6 — PEG_TX6 (2)
PEX_RX6_N AM18 PEG_TX#6 — PEG_TX#6 (2)
PEX_RX7 AN20 PEG_TX7 — PEG_TX7 (2)
PEX_RX7_N AM20 PEG_TX#7 — PEG_TX#7 (2)
PEX_RX8 AP20
PEX_RX8_N AP21
PEX_RX9 AN21
PEX_RX9_N AM21
PEX_RX10 AN23
PEX_RX10_N AM23
PEX_RX11 AP23
PEX_RX11_N AP24
PEX_RX12 AN24
PEX_RX12_N AM24
PEX_RX13 AN26
PEX_RX13_N AM26
PEX_RX14 AP26
PEX_RX14_N AP27
PEX_RX15 AN27
PEX_RX15_N AM27

PEX_TX0 AK14 C_PEG_RX0 C66 0.22U/10V_4 — PEG_RX0 (2)
PEX_TX0_N AJ14 C_PEG_RX#0 C65 0.22U/10V_4 — PEG_RX#0 (2)
PEX_TX1 AH14 C_PEG_RX1 C76 0.22U/10V_4 — PEG_RX1 (2)
PEX_TX1_N AG14 C_PEG_RX#1 C77 0.22U/10V_4 — PEG_RX#1 (2)
PEX_TX2 AK15 C_PEG_RX2 C71 0.22U/10V_4 — PEG_RX2 (2)
PEX_TX2_N AJ15 C_PEG_RX#2 C70 0.22U/10V_4 — PEG_RX#2 (2)
PEX_TX3 AL16 C_PEG_RX3 C72 0.22U/10V_4 — PEG_RX3 (2)
PEX_TX3_N AK16 C_PEG_RX#3 C73 0.22U/10V_4 — PEG_RX#3 (2)
PEX_TX4 AK17 C_PEG_RX4 C79 0.22U/10V_4 — PEG_RX4 (2)
PEX_TX4_N AJ17 C_PEG_RX#4 C78 0.22U/10V_4 — PEG_RX#4 (2)
PEX_TX5 AH17 C_PEG_RX5 C80 0.22U/10V_4 — PEG_RX5 (2)
PEX_TX5_N AG17 C_PEG_RX#5 C81 0.22U/10V_4 — PEG_RX#5 (2)
PEX_TX6 AK18 C_PEG_RX6 C84 0.22U/10V_4 — PEG_RX6 (2)
PEX_TX6_N AJ18 C_PEG_RX#6 C85 0.22U/10V_4 — PEG_RX#6 (2)
PEX_TX7 AL19 C_PEG_RX7 C82 0.22U/10V_4 — PEG_RX7 (2)
PEX_TX7_N AK19 C_PEG_RX#7 C83 0.22U/10V_4 — PEG_RX#7 (2)
PEX_TX8 AK20
PEX_TX8_N AJ20
PEX_TX9 AH20
PEX_TX9_N AG20
PEX_TX10 AK21
PEX_TX10_N AJ21
PEX_TX11 AL22
PEX_TX11_N AK22
PEX_TX12 AK23
PEX_TX12_N AJ23
PEX_TX13 AH23
PEX_TX13_N AG23
PEX_TX14 AK24
PEX_TX14_N AJ24
PEX_TX15 AL25
PEX_TX15_N AK25

AC6 NC_1
AJ28 NC_2
AJ4 NC_3
AJ5 NC_4
AL11 NC_5
C15 NC_6
D19 NC_7
D20 NC_8
D23 NC_9
D26 NC_10
H31 NC_11
T8 NC_12
V32 NC_13

PEX_REFCLK AL13 CLK_PCIE_VGA — CLK_PCIE_VGA (8)
PEX_REFCLK_N AK13 CLK_PCIE_VGA# — CLK_PCIE_VGA# (8)

PEX_TSTCLK_OUT AJ26 PEX_TSTCLK R373 *200/F_4
PEX_TSTCLK_OUT_N AK26 PEX_TSTCLK#

PEX_WAKE AJ11
PEX_RST_N AJ12 VGA_RST# R372 *0_4/S PEGX_RST#

PEX_CLKREQ_N AK12 PEX_CLKREQ# R444 10K/F_4 +3V_GFX

PEX_TERMP AP29 PEX_TERMP R366 2.49K/F_4

TESTMODE AK11 TESTMODE R370 10K/F_4

+3V_GFX J8 K8 VDD33_1 VDD33_2 0.085mA
+3V_GFX L8 M8 VDD33_3 VDD33_4

0.130mA
0.022mA
0.167mA

PEX_PLLVDD AG26 PEX_PLLVDD — L2 PBY160808T-300Y-N +1.05V_GFX
C67 4.7U/6.3V_6 PLACE NEAR BGA CLOSE TO CAPS
C75 1U/6.3V_4
C74 0.1U/10V_4 PLACE UNDER BGA
PLACE NEAR BALLS

PEX_PLL_HVDD AH12
PEX_SVDD_3V3 AG12

3.3V_AUX_NC P8

VDD_SENSE L4

GND_SENSE L5

PLACE NEAR BGA
0.1U/10V_4 C109
4.7U/6.3V_6 C608
4.7U/6.3V_6 C60
+3V_GFX
12~16 mils width

VGPU_CORE_SENSE (37)
VSS_GPU_SENSE (37)

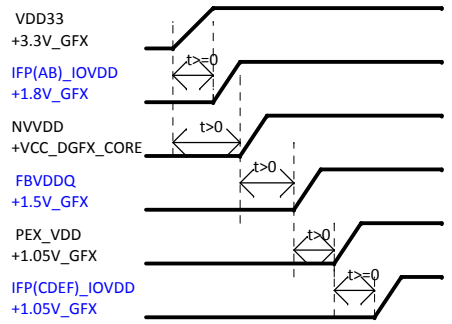
N13x
N13P

+3V_GFX
PLACE CLOSE TO BGA
C638 4.7U/6.3V_6
C657 1U/10V_6
C184 0.1U/10V_4
C174 0.1U/10V_4
C167 0.1U/10V_4
C176 0.1U/10V_4
PLACE CLOSE TO GPU BALLS

+3V_GFX
R445 4.7K_4
(9,18) DGPU_PWROK
20120508,MV
R446 *0_4/S
Q35 DTC144EUA
CLK_PEGA_REQ# (8)
PEX_CLKREQ# Q36 *DTC144EUA

+3V
U17 MC74VHC1G08DFT2G
C475 0.1U/10V_4
(2,8,24,25,27,29,30) PLTRST#
(9) DGPU_HOLD_RST#
DGPU_HOLD_RST#
PEGX_RST#
PEGX_RST# (17)
20120508,MV
R322 100K/F_4
R311 *330/F_4

Power up sequence



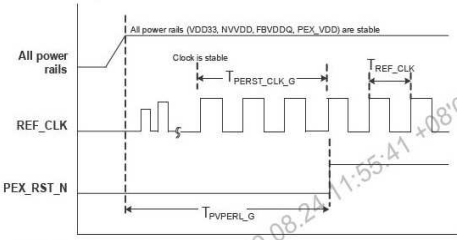
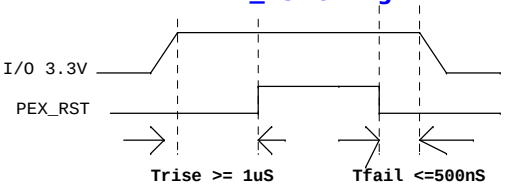


Figure 3-18. PEX_RST_N Timing for GPU

Table 3-8. N11x Reset Requirements for PCI Express 2.0

Constraint Parameter	Requirement	Notes
T_{PVPERL_G}	$T_{PVPERL\_G} \geq 1us$	
$T_{PERST\_CLK\_G}$	$T_{PERST\_CLK\_G} \geq 1T_{REF\_CLK}$	

PEX_RST timing



(15,16,18,38) +1.05V_GFX
(16,17,18,37,38) +3V_GFX

NB5

PROJECT : JW6/7
Quanta Computer Inc.

Size	Document Number	Rev
A3	DGPU 1/5 (PEG)	A

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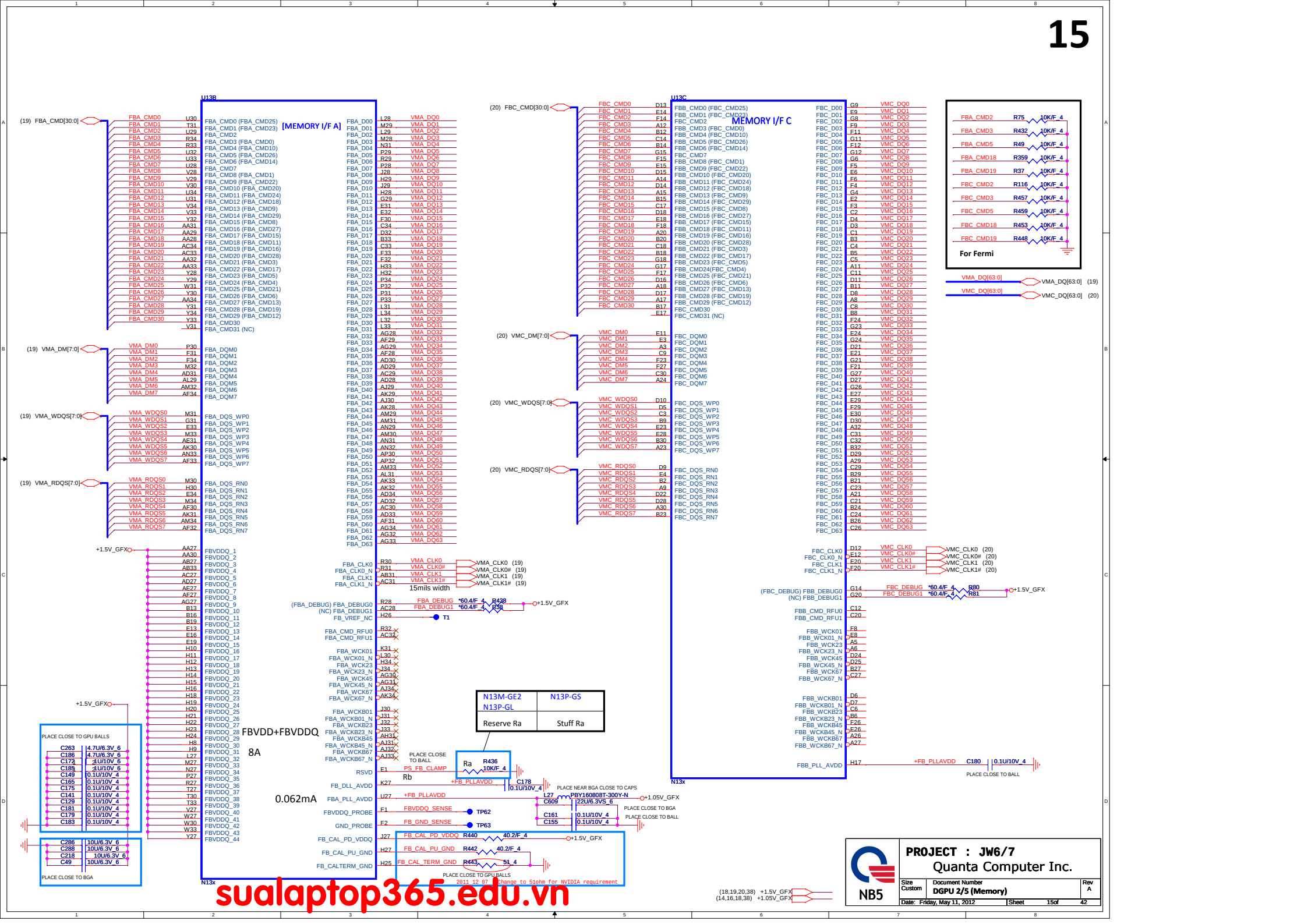

PROJECT :	JW6/7
Quanta Computer Inc.	
NB5	Size: Custom; Document Number: DGPU 2/5 (Memory); Rev: A
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(14,15,18,38) +1.05V_GFX
(14,17,18,37,38) +3V_GFX

U13D

R364 10K/F_4 IFPAB_PLLVDD — AH8 IFPAB_PLLVDD
IFPAB_IOVDD — AG8 IFPA_IOVDD
R362 10K/F_4 — AG9 IFPB_IOVDD
R363 *1K/F_4 — AJ8 IFPAB_RSET

[IFPA/B_LVDS]
IFPA_TXC AM6
IFPA_TXC_N AN6
IFPA_TXD0 AP3
IFPA_TXD0_N AN3
IFPA_TXD1 AN5
IFPA_TXD1_N AM5
IFPA_TXD2 AL6
IFPA_TXD2_N AK6
IFPA_TXD3 AJ6
IFPA_TXD3_N AH6
IFPB_TXC AJ9
IFPB_TXC_N AH9
IFPB_TXD4 AP6
IFPB_TXD4_N AP5
IFPB_TXD5 AM7
IFPB_TXD5_N AL7
IFPB_TXD6 AN8
IFPB_TXD6_N AM8
IFPB_TXD7 AK8
IFPB_TXD7_N AL8

0824 Update Symbol

AF7 IFPC_PLLVDD
R378 10K/F_4 IFPCD_PLLVDD — AG7 IFPD_PLLVDD
AF6 IFPC_IOVDD
R377 10K/F_4 IFPCD_IOVDD — AG6 IFPD_IOVDD
R365 *1K/F_4 — AF8 IFPC_RSET
AN2 IFPD_RSET

[IFPC/D_TMDS]
IFPC_AUX_I2CW_SCL AG3
IFPC_AUX_I2CW_SDA_N AG2
IFPC_L0 AK1
IFPC_L0_N AJ1
IFPC_L1 AJ3
IFPC_L1_N AJ2
IFPC_L2 AH3
IFPC_L2_N AH4
IFPC_L3 AG5
IFPC_L3_N AG4
IFPD_AUX_I2CX_SCL AK3
IFPD_AUX_I2CX_SDA_N AK2
IFPD_L0 AM1
IFPD_L0_N AM2
IFPD_L1 AM3
IFPD_L1_N AM4
IFPD_L2 AL3
IFPD_L2_N AL4
IFPD_L3 AK4
IFPD_L3_N AK5

R381 10K/F_4 IFPEF_PLLVDD — AB8 IFPEF_PLLVDD
AC7 IFPE_IOVDD
R379 10K/F_4 IFPEF_IOVDD — AC8 IFPF_IOVDD
AD6 IFPEF_RSET

[IFPE/F_DP]
IFPE_AUX_I2CY_SCL AB3
IFPE_AUX_I2CY_SDA_N AB4
IFPE_L0 AD2
IFPE_L0_N AD3
IFPE_L1 AD1
IFPE_L1_N AC1
IFPE_L2 AC2
IFPE_L2_N AC3
IFPE_L3 AC4
IFPE_L3_N AC5
IFPF_AUX_I2CZ_SCL AF3
IFPF_AUX_I2CZ_SDA_N AF2
IFPF_L0 AE3
IFPF_L0_N AF4
IFPF_L1 AF4
IFPF_L1_N AF5
IFPF_L2 AD4
IFPF_L2_N AD5
IFPF_L3 AG1
IFPF_L3_N AF1

R361 10K/F_4 DACA_VDD — AG10 DACA_VDD
T3 — AP9 DACA_VREF
T2 — AP8 DACA_RSET

[DACA/B_CRT]
DACA_RED AK9
DACA_GREEN AL10
DACA_BLUE AL9
DACA_HSYNC AM9
DACA_VSYNC AN9

I2CA_SCL
I2CA_SDA
R4 I2CA_SCL R59 2.2K_4
R5 I2CA_SDA R64 2.2K_4
+3V_GFX

+1.05V_GFX L28 PBY160808T-300Y-N — NV_PLLVDD AD8 PLLVDD 0.052mA
C625 22U/6.3VS_6
C624 0.1U/10V_4

AE8 SP_PLLVDD 0.067mA

PLACE CLOSE TO GPU

AD7 VID_PLLVDD 0.041mA
C150
C135
C130 22U/6.3VS_6
4.7U/6.3V_6
0.1U/10V_4

[XTAL IN]
XTAL_IN H3
XTAL_OUT H2
XTAL_OUTBUFF J4
XTAL_SSIN H1
CLK_27M_XTAL_IN
CLK_27M_XTAL_OUT
R67 10K/F_4
R427 10K/F_4

Y2 27MHZ +-10PPM
C197 12P/50V_4
C190 12P/50V_4

20120328,Change to 12pf

N13x

NB5

PROJECT : JW6/7
Quanta Computer Inc.
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Net name	N13M-GE2	N13P-GS(QS)
ROM_SI		
ROM_SO	PD 10K	PU 10K
ROM_SCLK	PD 15K	PU 5K
STRAP0	PU 45K	PU 45K
STRAP1	PD 45K	PD 5K
STRAP2	PU 15K	PD 15K
STRAP3	UN-STUFF	PD 5K
STRAP4	UN-STUFF	PD 45K

Net name	N13P-GL
ROM_SI	
ROM_SO	PD 10K
ROM_SCLK	PD 15K
STRAP0	PU 45K
STRAP1	PD 5K
STRAP2	PU 10K
STRAP3	UN-STUFF
STRAP4	UN-STUFF

For N13M-GE2
ROM_SO PD 10K
ROM_SCLK PD 15K

For N13P-GS
ROM_SO PU 10K
ROM_SCLK PU 5K

N13M-GE2-A1 ID:0X0DEA
N13P-GS ID:0X0FD2
N13P-GL-A1 ID:0X0DE9

17

Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

Default: Hynix VRAM

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	1001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	0011
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	0111
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	XXXX
STRAP4	RESERVED	PCI SPEED CHANGE GEN3	PCI_MAX SPEED	DP_PLL_VDD33	XXXX

VID 0 0 0 0 1 1 0 ---> 0.9V N13P-GS-A2
VID 0 0 1 1 0 1 0 ---> 0.95V N13P-GL-A1

	N13M-GE2	N13P-GS
Ra	Un-Stuff	Stuff
Qa	Stuff	Un-Stuff

For N13M-GE2, N13M-GS (QS)
Defult : 2G Samsung

VRAM Configuration Table
ROM_SI
1G Hynix 64Mx16 -->15K PD
1G Samsung 64Mx16 -->20K PD
2G Hynix 128Mx16 -->35K PD
2G Samsung 128Mx16 -->45K PD

GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	OUT	GPU_VID4	GPU CORE_VDD VID4
1	OUT	GPU_VID3	GPU CORE_VDD VID3
2	OUT	LCD_BL_PWM	LCD BACKLIGHT PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	GPU_VID1	GPU CORE_VDD VID1
6	OUT	GPU_VID2	GPU CORE_VDD VID2
7	OUT	3D VISION	3D VISION LEFT/RIGHT VISION
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM VREF	MEMMORY VREF CONTROL
11	OUT	GPU_VID0	GPU CORE_VDD VID0
12	IN	PWR_LEVEL	Power Detect ,HIGH=AC, LOW=DC
13	OUT	GPU_VID5	GPU CORE_VDD VID5
14	IN	HPD_AB	HOT PLUG DETECT FOR IFPAB
15	IN	HPD_C	HOT PLUG DETECT FOR IFPC
16	OUT	MEM VDD	MEMMORY VDD CONTROL
17	IN	HPD_D	HOT PLUG DETECT FOR IFPD
18	IN	HPD_E	HOT PLUG DETECT FOR IFPE
19	IN	HPD_F	HOT PLUG DETECT FOR IFPF
20/21		RESERVE	

GFx SMBus Isolation

2011 12 01 : Add off-page connector

N13M-GE2 N13P-GL	N13P-GS
Stuff Rc	Un-stuff Rc

PROJECT : JW6/7
Quanta Computer Inc.
NB5
Size Custom | Document Number DGPU 4/5 (MIO/GPIO) | Rev A
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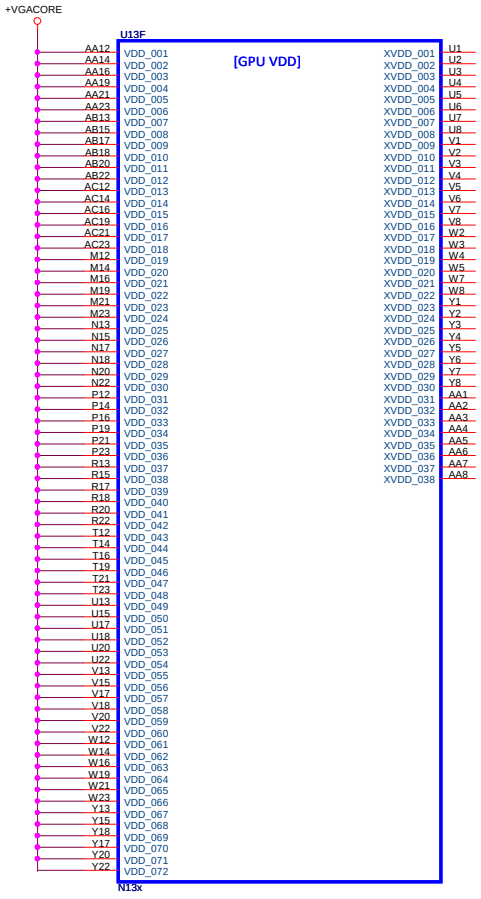
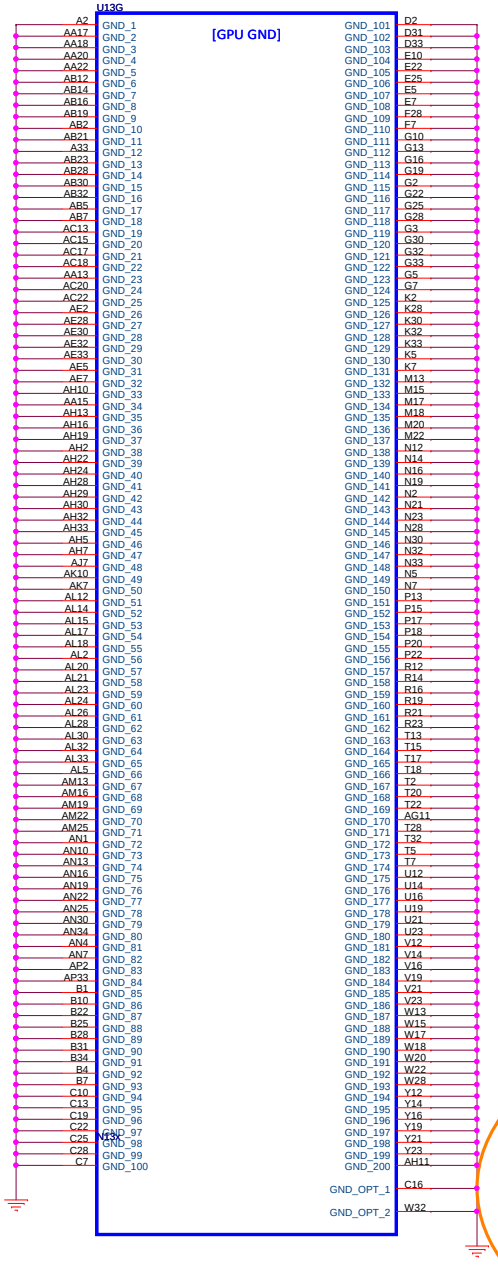
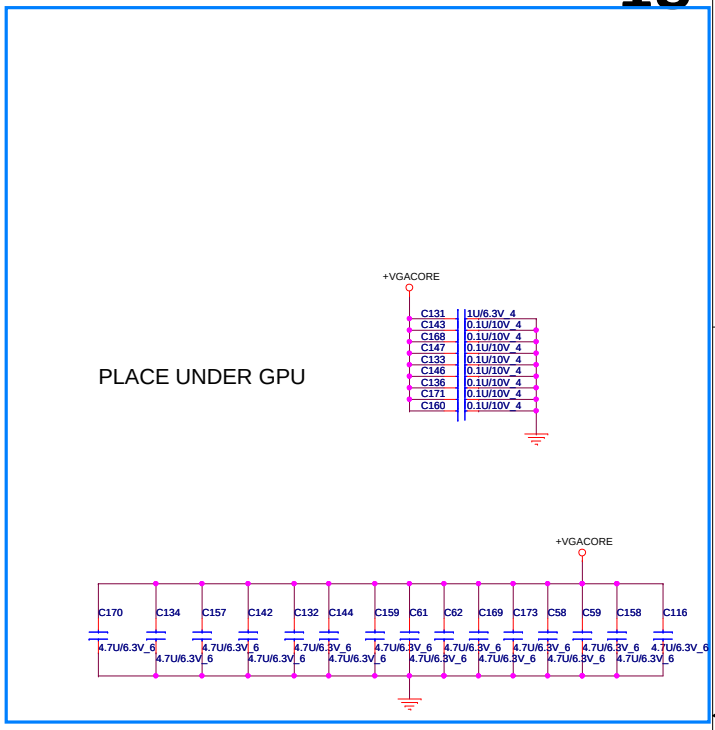
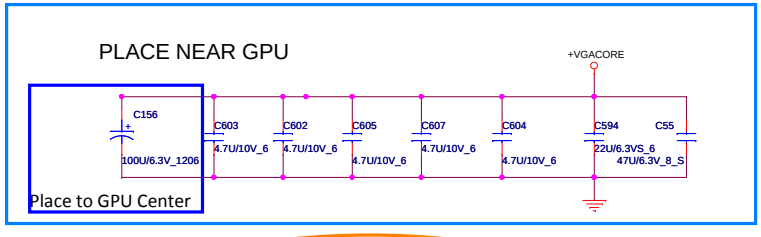
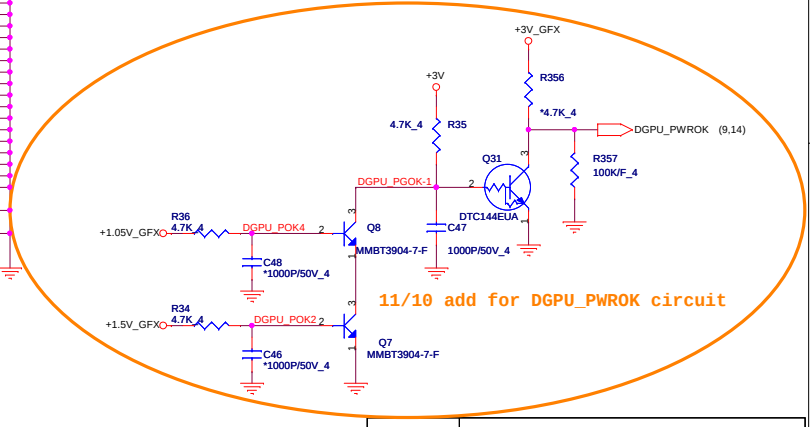


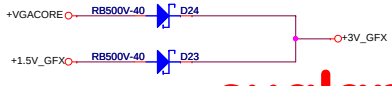








for meet Power down sequence for +3V_GFX



(37) +VGACORE
(14,15,16,38) +1.05V_GFX
(15,19,20,38) +1.5V_GFX
(14,16,17,37,38) +3V_GFX
(6,7,8,9,10,12,13,14,21,22,23,24,25,27,28,29,30,35,37,39,41) +3V

NB5

PROJECT : JW6/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DGPU 5/5 (Power/Ground)	A
Date: Friday, May 11, 2012	Sheet 18of 42	

900MHz VRAM size:
Samsung 64Mx16, P/N = AKD5EGGT500
Samsung 128Mx16, P/N = AKD5MGWT500
Hynix 64Mx16, P/N = AKD5LZWTW02
Hynix 128Mx16, P/N = AKD5MGWTW00

CHANNEL A: 256MB/512MB DDR3

(15) VMA_DQ[63..0]
(15) VMA_DM[7..0]
(15) VMA_WDQS[7..0]
(15) VMA_RDQS[7..0]

VRAM2 / VRAM6 / VRAM1 / VRAM5
96-BALL SDRAM DDR3
VRAM _DDR3_SAMSUNG_64MX16

Should be 240 Ohms +-1%
R50 243/F_4
R431 243/F_4
R39 243/F_4
R376 243/F_4

+1.5V_GFX

(15) FBA_CMD9 (15) FBA_CMD11 (15) FBA_CMD8 (15) FBA_CMD25 (15) FBA_CMD10 (15) FBA_CMD24 (15) FBA_CMD22 (15) FBA_CMD7 (15) FBA_CMD21 (15) FBA_CMD6 (15) FBA_CMD29 (15) FBA_CMD23 (15) FBA_CMD28 (15) FBA_CMD20 (15) FBA_CMD4 (15) FBA_CMD14
(15) FBA_CMD12 (15) FBA_CMD27 (15) FBA_CMD26
(15) VMA_CLK0 (15) VMA_CLK0# (15) FBA_CMD3
(15) FBA_CMD2 (15) FBA_CMD0 (15) FBA_CMD30 (15) FBA_CMD15 (15) FBA_CMD13
(15) FBA_CMD5
(15) VMA_CLK1 (15) VMA_CLK1# (15) FBA_CMD19
(15) FBA_CMD18 (15) FBA_CMD16

VREFC_VMA1 / VREFD_VMA1
VMA_WDQS0 / VMA_RDQS0
VMA_ZQ1
VMA_DM1 / VMA_DM0

VREFC_VMA3 / VREFD_VMA3
VMA_WDQS4 / VMA_RDQS4
VMA_ZQ3
VMA_DM5 / VMA_DM4

VREFC_VMA1 / VREFD_VMA1
VMA_WDQS3 / VMA_RDQS3
VMA_ZQ2
VMA_DM3 / VMA_DM2

VREFC_VMA3 / VREFD_VMA3
VMA_WDQS5 / VMA_RDQS5
VMA_ZQ4
VMA_DM7 / VMA_DM6

VMA_DQ0 … VMA_DQ63

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

VMA_CLK0 — R428 162/F_4 — VMA_CLK0#

+1.5V_GFX — R385 1.33K/F_4 — VREFC_VMA1 — R386 1.33K/F_4 — C617 0.1U/10V_4
+1.5V_GFX — R435 1.33K/F_4 — VREFD_VMA1 — R430 1.33K/F_4 — C648 0.1U/10V_4

(15) FBA_CMD17 — FBA_CMD17 — TP2
(15) FBA_CMD1 — FBA_CMD1 — TP9

VMA_CLK1 — R40 162/F_4 — VMA_CLK1#

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

+1.5V_GFX — R375 1.33K/F_4 — VREFC_VMA3 — R374 1.33K/F_4 — C613 0.1U/10V_4
+1.5V_GFX — R358 1.33K/F_4 — VREFD_VMA3 — R360 1.33K/F_4 — C597 0.1U/10V_4

+1.5V_GFX
C137 C612 C614 C621 — 1U/6.3V_4

+1.5V_GFX
C616 C601 C599 C622 C596 C53 — 10U/6.3V_6 / 1U/6.3V_4

+1.5V_GFX
C128 — 10U/6.3V_6
C600 C215 C623 — 1U/6.3V_4
C645 C138 C216 C620 — 1U/6.3V_4

+1.5V_GFX
C650 — 10U/6.3V_6
C89 — 10U/6.3V_6
C51 C139 C93 — 0.1U/10V_4
C140 C52 — 0.1U/10V_4

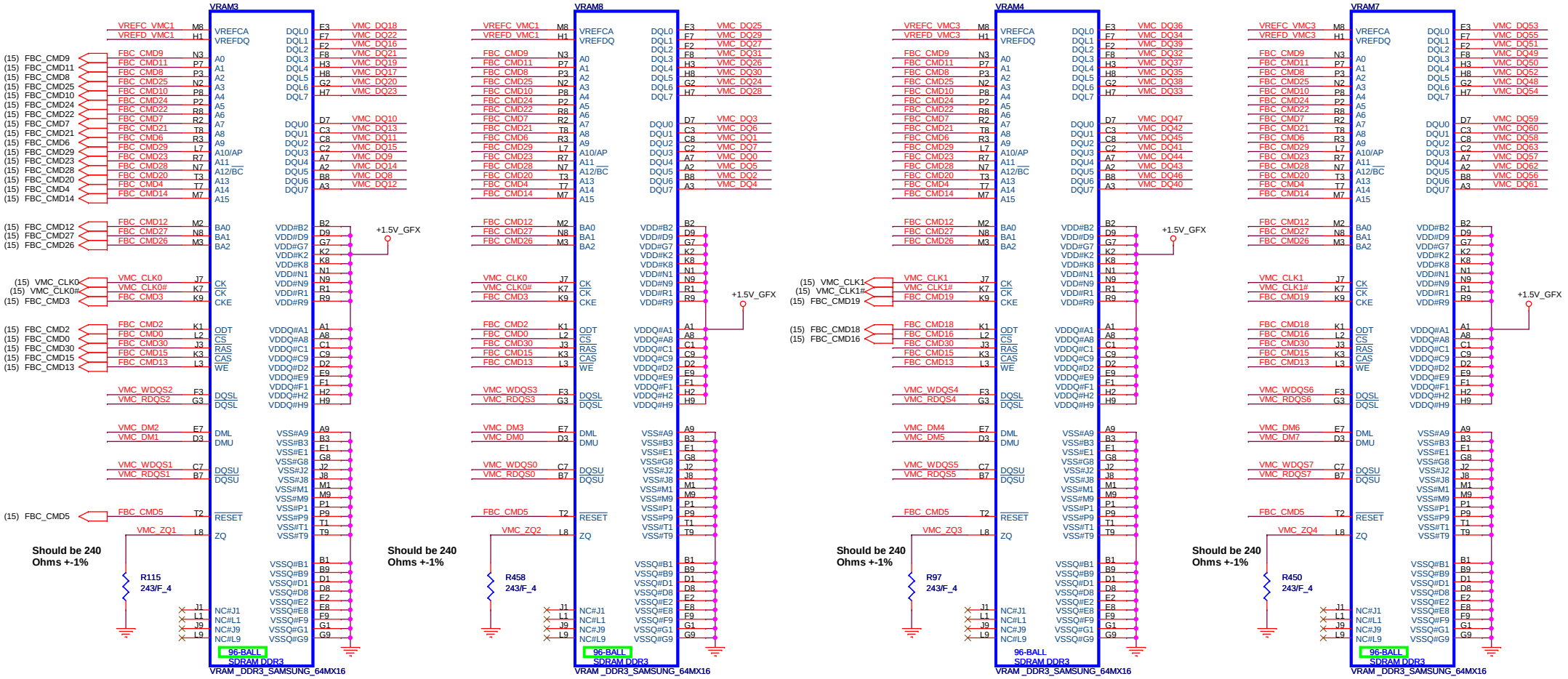
+1.5V_GFX
C649 — 10U/6.3V_6
C50 — 10U/6.3V_6
C217 C595 C598 — 0.1U/10V_4

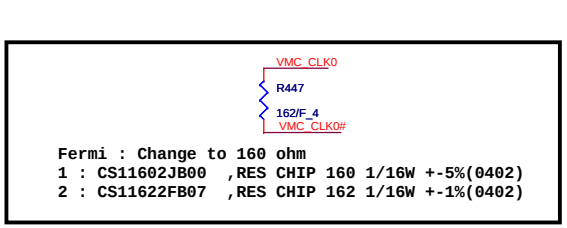
(15,18,20,38) +1.5V_GFX

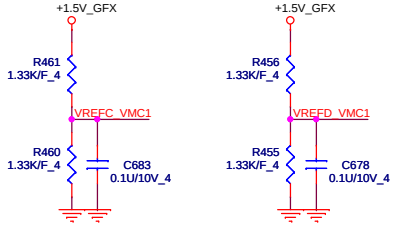
PROJECT : JW6/7
Quanta Computer Inc.
NB5
Size: Custom | Document Number: DGPU Memory 1/2 (DDR3) | Rev: 1A
Date: Friday, May 11, 2012 | Sheet 19 of 42

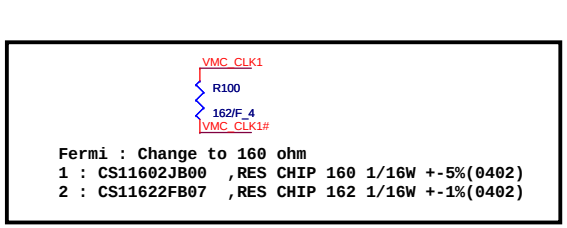
CHANNEL B: 256MB/512MB DDR3

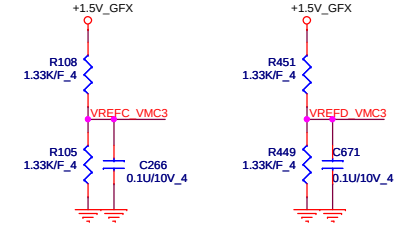
(15) VMC_DQ[63..0]
(15) VMC_DM[7..0]
(15) VMC_WDQS[7..0]
(15) VMC_RDQS[7..0]

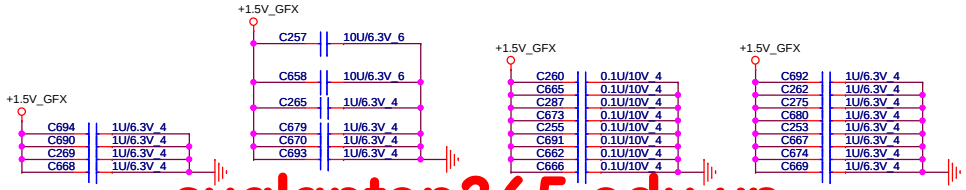












(15) FBC_CMD17 — FBC_CMD17 — TP26
(15) FBC_CMD1 — FBC_CMD1 — TP27

900MHz VRAM size:
Samsung 64Mx16, P/N = AKD5EGGT500
Samsung 128Mx16, P/N = AKD5MGWT500
Hynix 64Mx16, P/N = AKD5LZWTW02
Hynix 128Mx16, P/N = AKD5MGWTW00

(15,18,19,38) +1.5V_GFX

NB5

PROJECT : JW6/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DGPU Memory 2/2 (DDR3)	1A

Date: Friday, May 11, 2012 | Sheet 20 of 42

USB Camera Connector

MIC

(23) DIGITAL_D1 — L26 — FCM1608KF-301T02 — DIGITAL_D1_R
(23) DIGITAL_CLK — L25 — FCM1608KF-301T02 — DIGITAL_CLK_R

C582 100P/50V_4
C581 100P/50V_4
EMI request

(8) USBP2-
(8) USBP2+
CAMERA
L1 *WCM2012-90
USBP2-
USBP2+

C33 *10P/50V_4 USBP2-
C40 *10P/50V_4 USBP2+
C589 33P/50V_4 DIGITAL_D1
C588 33P/50V_4 DIGITAL_CLK

Change from +5V to +3V
+3V — C38 0.01U/16V_4
C587 *4.7U/6.3V_6

+3V — R24 2.2K_4 — R23 2.2K_4
(6) PCH_EDIDCLK — PCH_EDIDCLK
(6) PCH_EDIDDATA — PCH_EDIDDATA

H=2.0
CN1
+3VLCD_CON — C37 1000P/50V_4
+3V
PCH_EDIDCLK
PCH_EDIDDATA
(6) PCH_LA_DATAN0 — PCH_LA_DATAN0
(6) PCH_LA_DATAP0 — PCH_LA_DATAP0
(6) PCH_LA_DATAN1 — PCH_LA_DATAN1
(6) PCH_LA_DATAP1 — PCH_LA_DATAP1
(6) PCH_LA_DATAN2 — PCH_LA_DATAN2
(6) PCH_LA_DATAP2 — PCH_LA_DATAP2
(6) PCH_LA_CLK# — PCH_LA_CLK#
(6) PCH_LA_CLK — PCH_LA_CLK
(6) PCH_LB_DATAN0 — PCH_LB_DATAN0
(6) PCH_LB_DATAP0 — PCH_LB_DATAP0
(6) PCH_LB_DATAN1 — PCH_LB_DATAN1
(6) PCH_LB_DATAP1 — PCH_LB_DATAP1
(6) PCH_LB_DATAN2 — PCH_LB_DATAN2
(6) PCH_LB_DATAP2 — PCH_LB_DATAP2
(6) PCH_LB_CLK# — PCH_LB_CLK#
(6) PCH_LB_CLK — PCH_LB_CLK
DIGITAL_D1_R
DIGITAL_CLK_R
Change from +5V to +3V
+3V
USBP2-
USBP2+
(6) PCH_DPST_PWM — R353 1K/F_4 — PCH_DPST_PWM_R
C584 22P/50V_4 — BLON_CON
+VIN_BLIGHT
GS12407-11141-9F

+3V — C586 1U/6.3V_4 — U10
IN IN ON/OFF OUT GND
(6) PCH_DISP_ON — PCH_DISP_ON
R351 100K/F_4
IC(5P) G5243AT11U
+LCDVCC — L22 *0_6/S (20120314 modify)
+3VLCD_CON
C39 *10U/6.3V_6
C36 *0.01U/16V_4
C35 0.1U/10V_4

(29) LID_CONTROL — LID_CONTROL — D21 RB500V-40 — R352 100K/F_4 — C583 22P/50V_4 — BLON_CON
(6) PCH_LVDS_BLON — PCH_LVDS_BLON — R354 1K/F_4 — D22 *RB500V-40 — R350 47K/F_4 — +3VPCU
LID_EC# (28,29)
R355 100K/F_4
(8) LCD_BK — Q30 *DTC144EUA

+VIN_BLIGHT
+VIN — L24 *TI160808U600 — L23 *0_6/S (20120314 modify) — +VIN_BLIGHT
C580 0.1U/50V_6
C585 *4.7U/25V_8
C590 0.1U/50V_6
C591 0.01U/25V_4

+5V: C148 C54 C449 C267 C576 C566 — 0.1U/10V_4
+3VS5: C551 C358 C548 C529 C537 C540 — 0.1U/10V_4
+3V: C195 C339 C249 C309 C522 C513 — 0.1U/10V_4
+5V: C570 C261 C406 C567 C569 C189 — 0.1U/10V_4
+3VS5: C560 C554 C357 C562 C563 C703 — 0.1U/10V_4
+5VS5

EMI/ESD

Stitching Cap(each 1" place one cap)

(6,7,8,9,10,12,13,14,18,22,23,24,25,27,28,29,30,35,37,39,41) +3V
(7,26,27,28,29,31,32) +3VPCU
(7,10,22,23,27,28,41) +5V
(31,32,33,35,37,38,40,41) +VIN
(38,41) +12VALW
(10,23,26,32,33,34,35,37,39,40,41) +5VS5

NB5

PROJECT : JW6/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD Connector (LVDS)	A
Date: Friday, May 11, 2012	Sheet 21of 42	

40 MIL

40 mils F1 FUSE1A6V_POLY +5V +5VCRT +5VCRT
C145 0.1U/10V_4
SSM14 spec is 40V 1A

CRT PORT

20120505,MV
L5 SBK160808T-680Y-N
L4 SBK160808T-680Y-N
L3 SBK160808T-680Y-N

(6) PCH_CRT_R
(6) PCH_CRT_G
(6) PCH_CRT_B

CRT_R_CON
CRT_G_CON
CRT_B_CON

R58 150/F_4
R53 150/F_4
R48 150/F_4

C182 6.8P/50V_4
C164 6.8P/50V_4
C127 6.8P/50V_4
C126 6.8P/50V_4
C166 6.8P/50V_4
C187 6.8P/50V_4
EMI

+5VCRT

CRT CONN
CN12

C611 .1U/10V_4

(6) PCH_VSYNC PCH_VSYNC
U11
M74VHC1GT125DF2G

(6) PCH_HSYNC PCH_HSYNC
U12
M74VHC1GT125DF2G

CRTVSYNC1 R380 *0_4/S CRTVSYNC2
CRTHSYNC1 R396 *0_4/S CRTHSYNC2
R43 *0_4/S DDCCLK3
R405 *0_4/S DDCDAT3

C90 *470P/50V_4
C615 *47P/50V_6
C630 *470P/50V_4
C631 *47P/50V_6

+3V R42 10K/F_4
(6) PCH_DDCCLK
+3V R415 10K/F_4
(6) PCH_DDCDATA
Q42
2N7002DW
DDCCLK2
DDCDATA2
20120201,B

R41 2.2K_4
R397 2.2K_4

D25 RB500V-40
+5VCRT +5V_CRT2

PCH_CRT_R PCH_CRT_G PCH_CRT_B DDCCLK3 DDCDAT3 CRTHSYNC2 CRTVSYNC2

D5 *BAV99W
D4 *BAV99W
D3 *BAV99W
D2 *BAV99W
D28 *BAV99W
D27 *BAV99W
D26 *BAV99W
+3V +5V

inputs		function
/E	SET	
L	L	Y - port 0
L	H	Y - port 1
H	X	Disconnect

HDMI SMBus Isolation

+3V R171 2.2K_4 Q17
(6) SDVO_CLK HDMI_SCL_R HDMI_SCLK
(6) SDVO_DATA HDMI_SDA_R HDMI_SDATA
+3V R189 2.2K_4
2N7002DW

Close to HDMI connector

EMI Solution

C_TX2_HDMI+ R150 100/F_4 C_TX2_HDMI-
C_TX1_HDMI+ R133 100/F_4 C_TX1_HDMI-
C_TX0_HDMI+ R139 100/F_4 C_TX0_HDMI-
C_IN_CLK R125 100/F_4 C_IN_CLK#

C_IN_CLK# R122 *0_4/S C_TXC_HDMI-
C_IN_CLK R127 *0_4/S C_TXC_HDMI+
20120508,MV

HDMI PORT

CN16
SHELL3 SHELL1
D2+ D2 Shield D2- D1+ D1 Shield D1- D0+ D0 Shield D0- CK+ CK Shield CK- CE Remote NC DDC CLK DDC DATA GND +5V HP DET
SHELL2 SHELL4

(6) IN_D2 C341 0.1U/10V_4 C_TX2_HDMI+
(6) IN_D2# C332 0.1U/10V_4 C_TX2_HDMI-
(6) IN_D1 C323 0.1U/10V_4 C_TX1_HDMI+
(6) IN_D1# C319 0.1U/10V_4 C_TX1_HDMI-
(6) IN_D0 C327 0.1U/10V_4 C_TX0_HDMI+
(6) IN_D0# C324 0.1U/10V_4 C_TX0_HDMI-
(6) IN_CLK C315 0.1U/10V_4 C_IN_CLK C_TXC_HDMI+
(6) IN_CLK# C310 0.1U/10V_4 C_IN_CLK# C_TXC_HDMI-

RB500V-40
+5V D8 D7 RB500V-40
5V_HSMBCK R131 2.2K_4
5V_HSMBDT R130 2.2K_4
HDMI_SCLK
HDMI_SDATA
C311 *10P/50V_4
C312 *10P/50V_4
+5VCRT

HDMI_HPD R117 *0_4/S HDMI_DET_C
C302 220P/50V_4
HDMI CONN_4 pin GND
add for EMI

D6 *BAV99W
+5V 20120423,MV
R124 110K/F_4
B-stage change

+3V DGPU_CL_HDMIP
R152 510/F_4 C_TX2_HDMI+
R144 510/F_4 C_TX2_HDMI-
R134 510/F_4 C_TX1_HDMI+
R132 510/F_4 C_TX1_HDMI-
R142 510/F_4 C_TX0_HDMI+
R135 510/F_4 C_TX0_HDMI-
R128 510/F_4 C_IN_CLK
R123 510/F_4 C_IN_CLK#
R179 100K/F_4
Q16 2N7002K
C354 0.1U/10V_4
Close to Q24

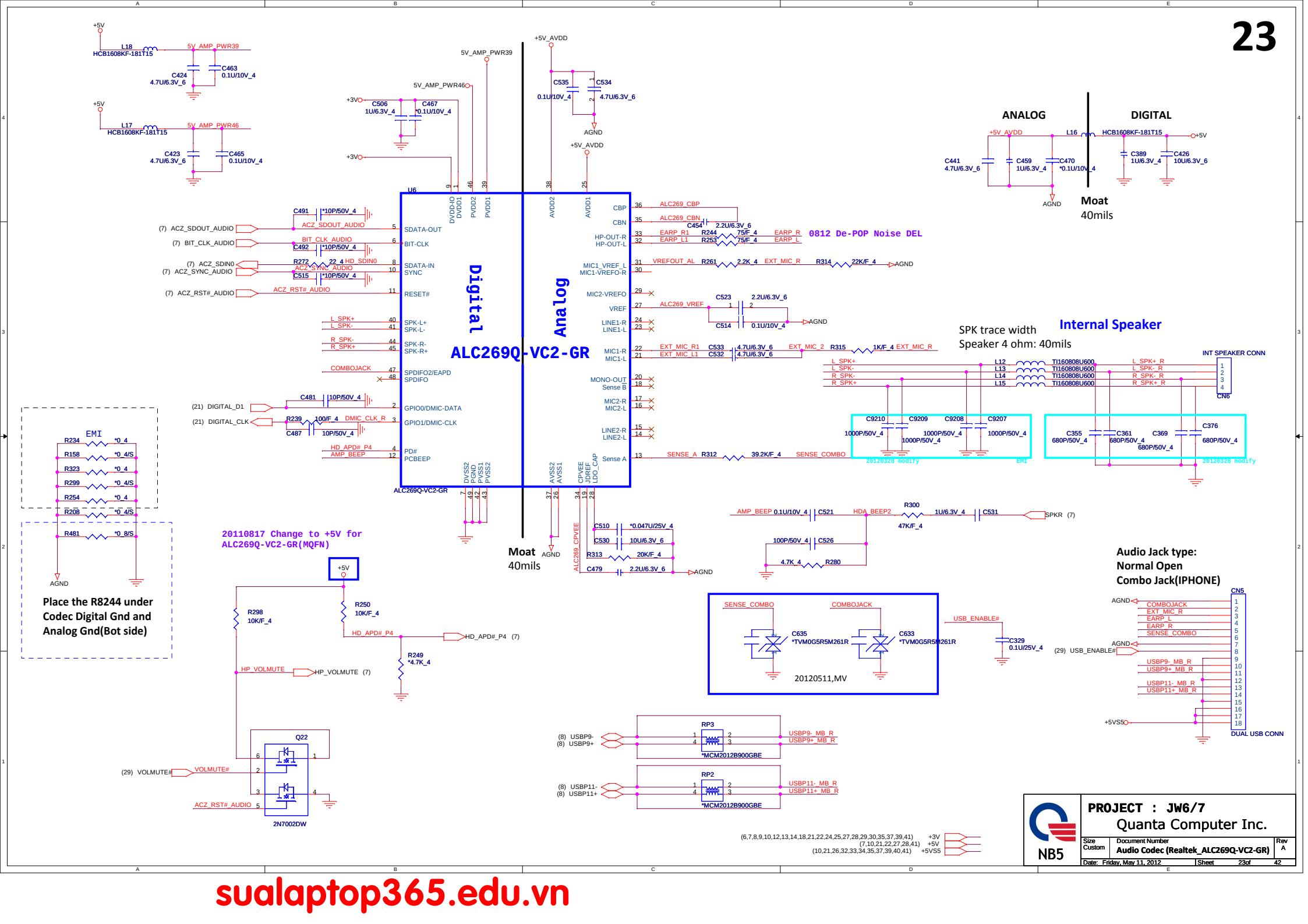
+3V
Q14 MMBT3904-7-F
HDMI_DET_P
R120 150K/F_4
HDMI_HPD
(6) HDMI_HPD_CON HDMI_HPD_CON
R129 10K/F_4

+5VCRT
C276 *0.01U/16V_4
for EMI request

NB5

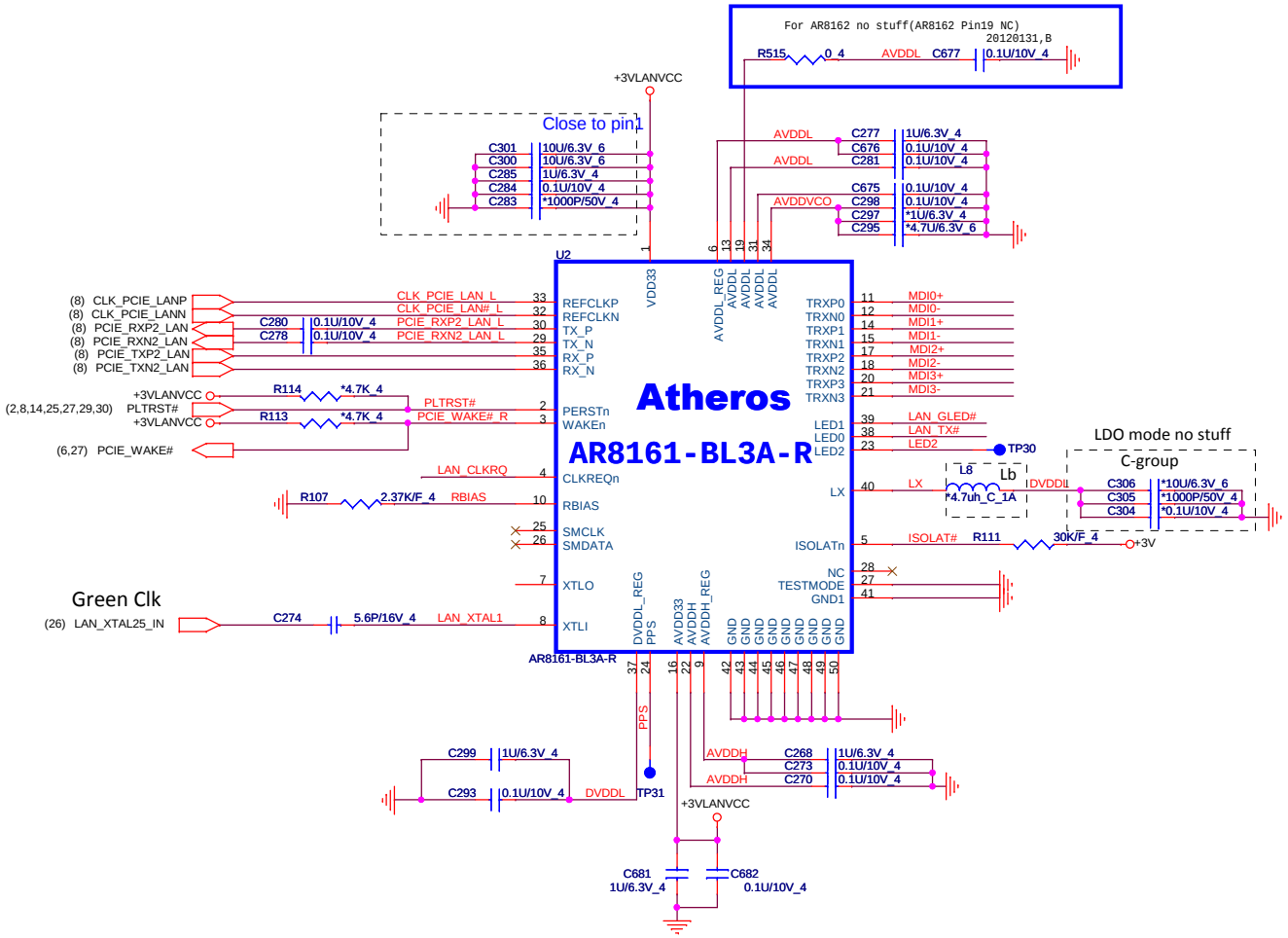
PROJECT : JW6/7
Quanta Computer Inc.

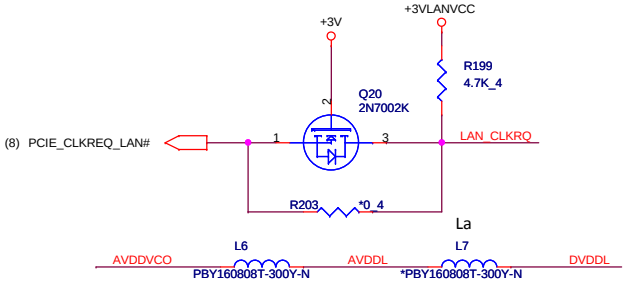
Size	Document Number	Rev
Custom	CRT/HDMI Connector	A
Date: Friday, May 11, 2012	Sheet 22of 42	



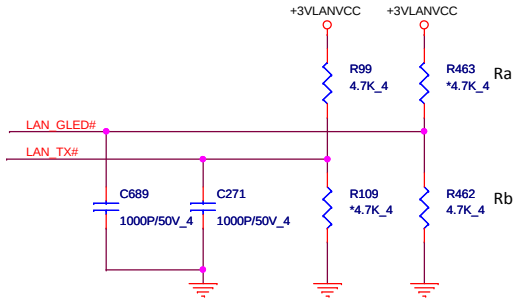
PROJECT :	JW6/7
	Quanta Computer Inc.
Size: Custom	Document Number: Audio Codec (Realtek_ALC269Q-VC2-GR)
Rev: A	
Date: Friday, May 11, 2012	Sheet 23of 42

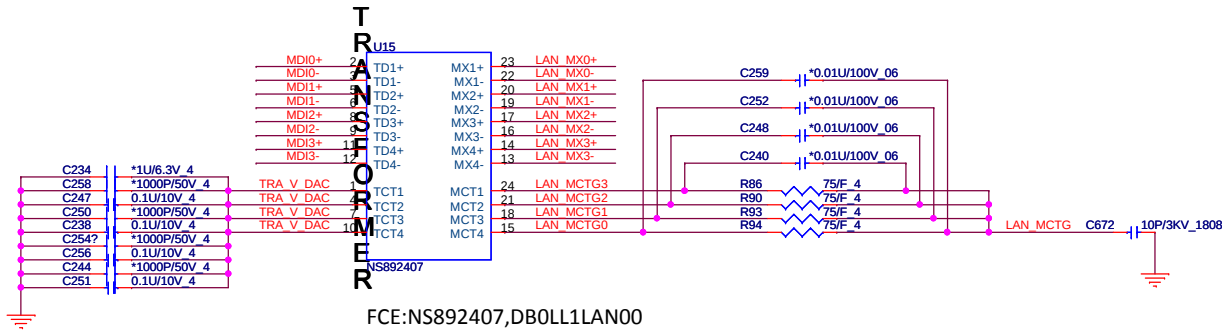
NB5

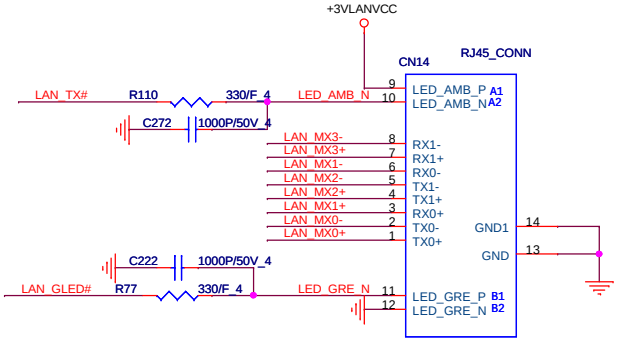




LDO mode:	
Rb	**Stuff**
La	No stuff
Lb	No stuff
C-group	No stuff
Ra	No stuff







FCE:NS892407,DB0LL1LAN00

BOT:GST5009B LF,DB0Z06LAN00

NB5

PROJECT : JW6/7

Quanta Computer Inc.

Size	Document Number	Rev
Custom	LAN Controller (Atheros_AR8161)	A

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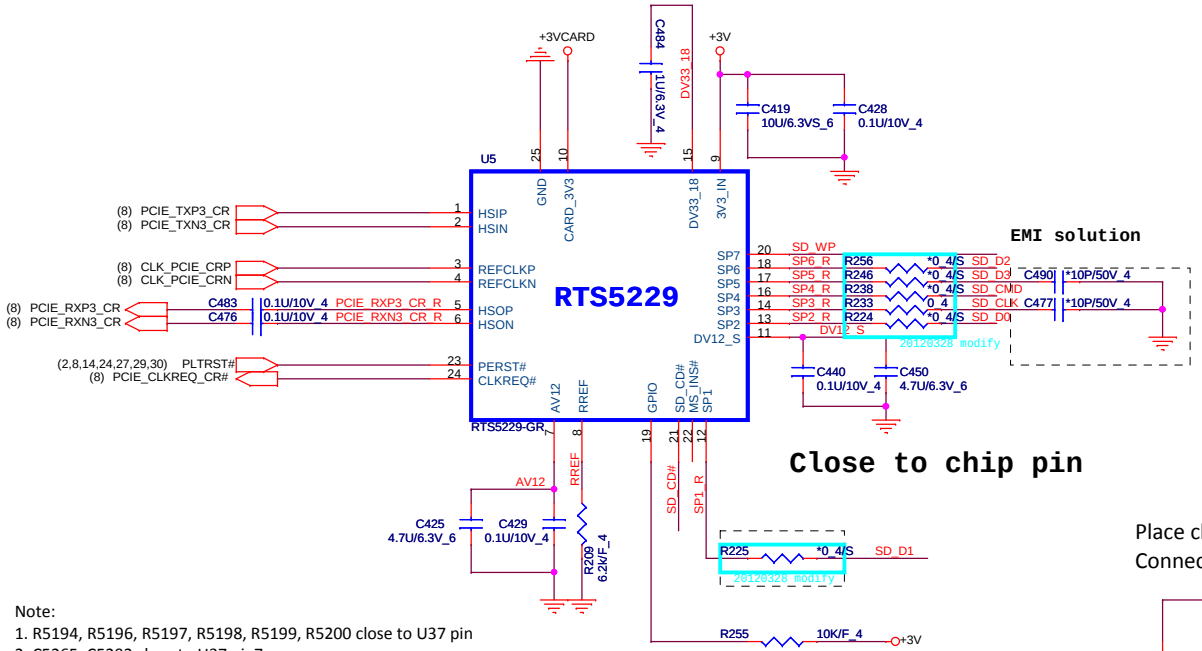
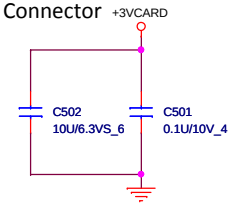
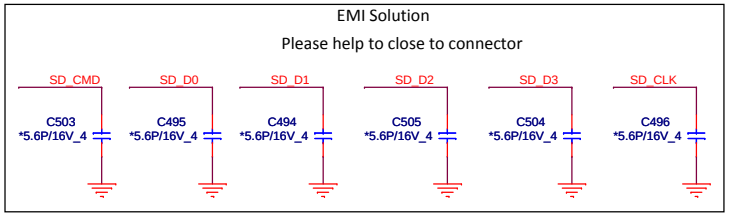


Note:
1. R5194, R5196, R5197, R5198, R5199, R5200 close to U37 pin
2. C5265, C5202 close to U37 pin7
3. C1021, C1022 close to U37 pin11
4. C1089, C1090 close to U37 pin9
5. C1019 close to U37 pin15
6. C1026, C1027 close to CN27 pin11
7. C1025 close to CN27 pin4

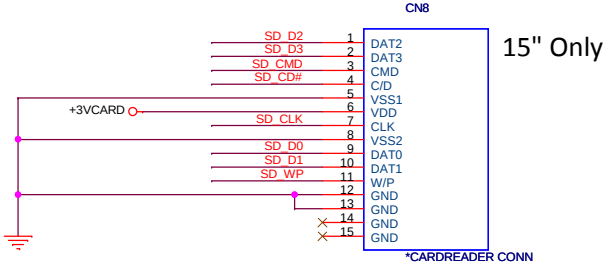
Place close to Connector



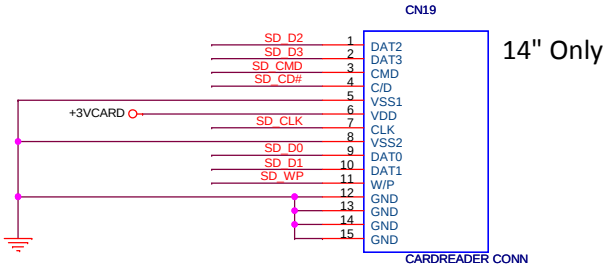
Share Pin



SD / MMC CARD READER

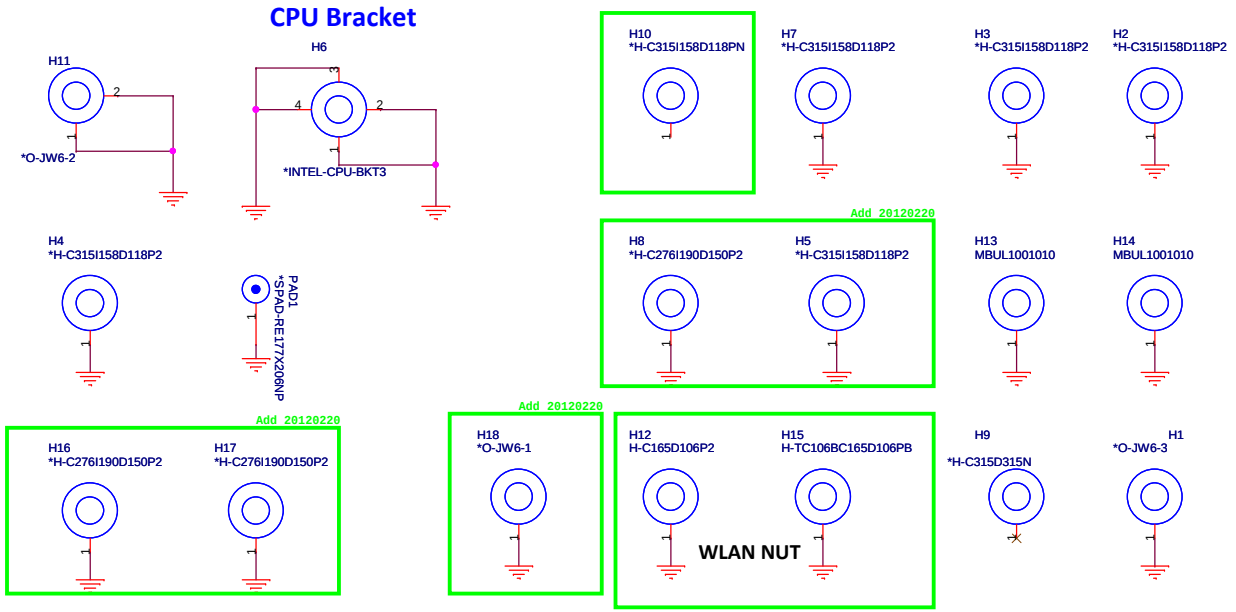


15" Only



14" Only

CPU Bracket

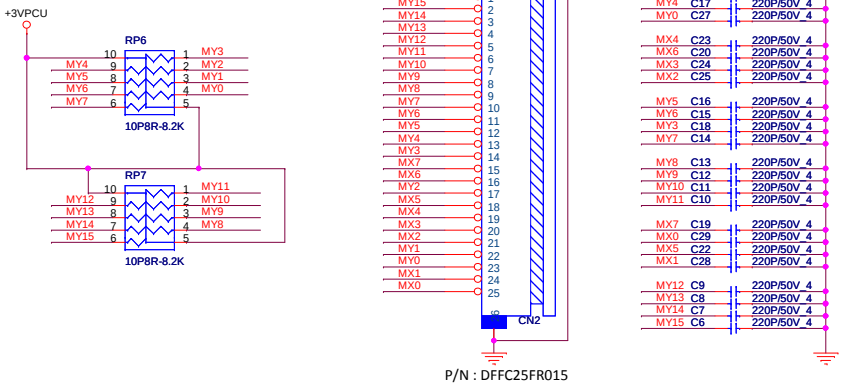


NB5

PROJECT : JW6/7
Quanta Computer Inc.

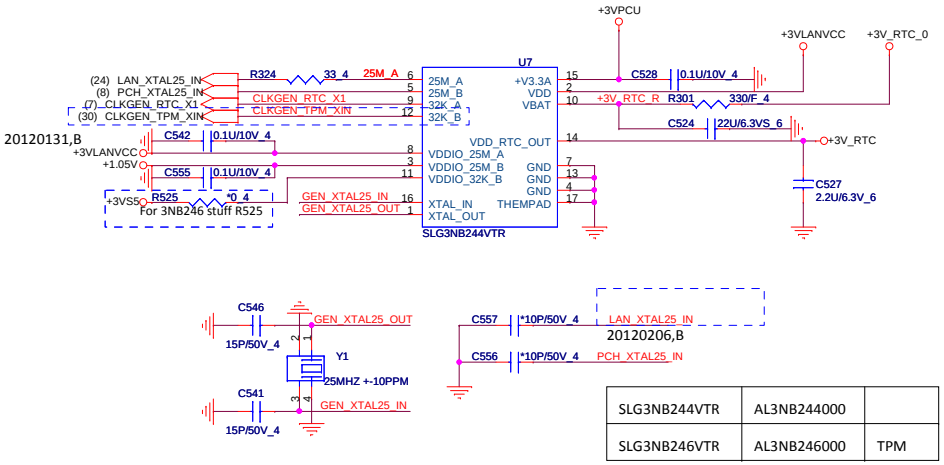
Size	Document Number	Rev
Custom	Card Reader control (RTS5229-GR)	A
Date: Tuesday, May 15, 2012	Sheet 25of 42	

Keyboard Connector



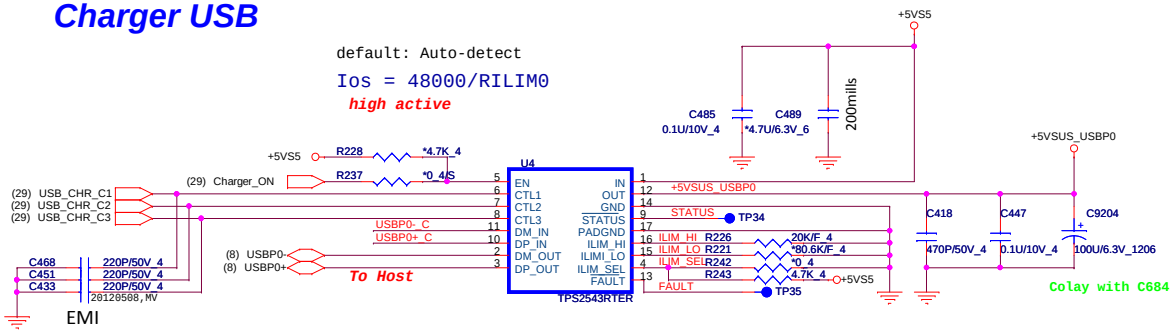
Green CLK Circuitry

+3V_RTC_0,+3V_RTC_R,+3V_RTC..
20mils width(min)



SLG3NB244VTR	AL3NB244000	
SLG3NB246VTR	AL3NB246000	TPM

Charger USB



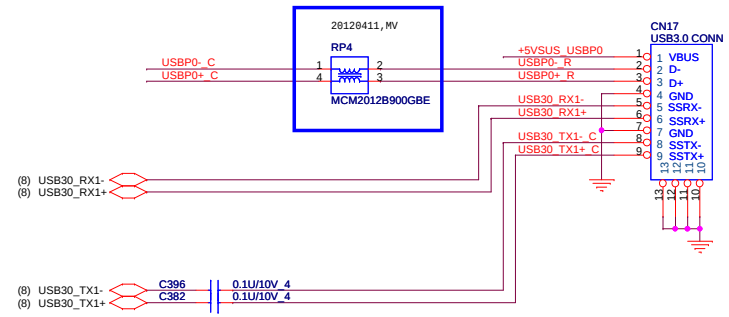
TPS2543/45 Control Truth Table

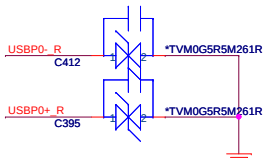
CTL1	CTL2	CTL3	ILIM_SEL	Charging Mode	Current Limit Setting	TPS2543 STATUS Output (active low)
0	0	0	1	Discharge	NA	off
0	0	1	1	DCP/auto	IOS_PW & ILIM_HI (1)	DCP load present
0	1	0	1	SDP	ILIM_HI	off
0	1	1	1	DCP/auto	ILIM_HI	DCP load present
1	1	0	1	SDP	ILIM_HI	off
1	1	1	1	CDP	ILIM_HI	CDP load present

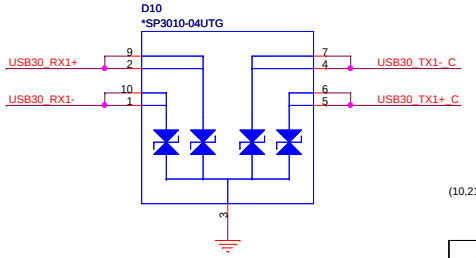
(1) ILIM_HI: 20K(R5233), 2.4A

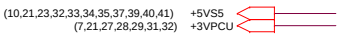
USB3.0 X 1/USB2.0 COMBO

USB 3.0





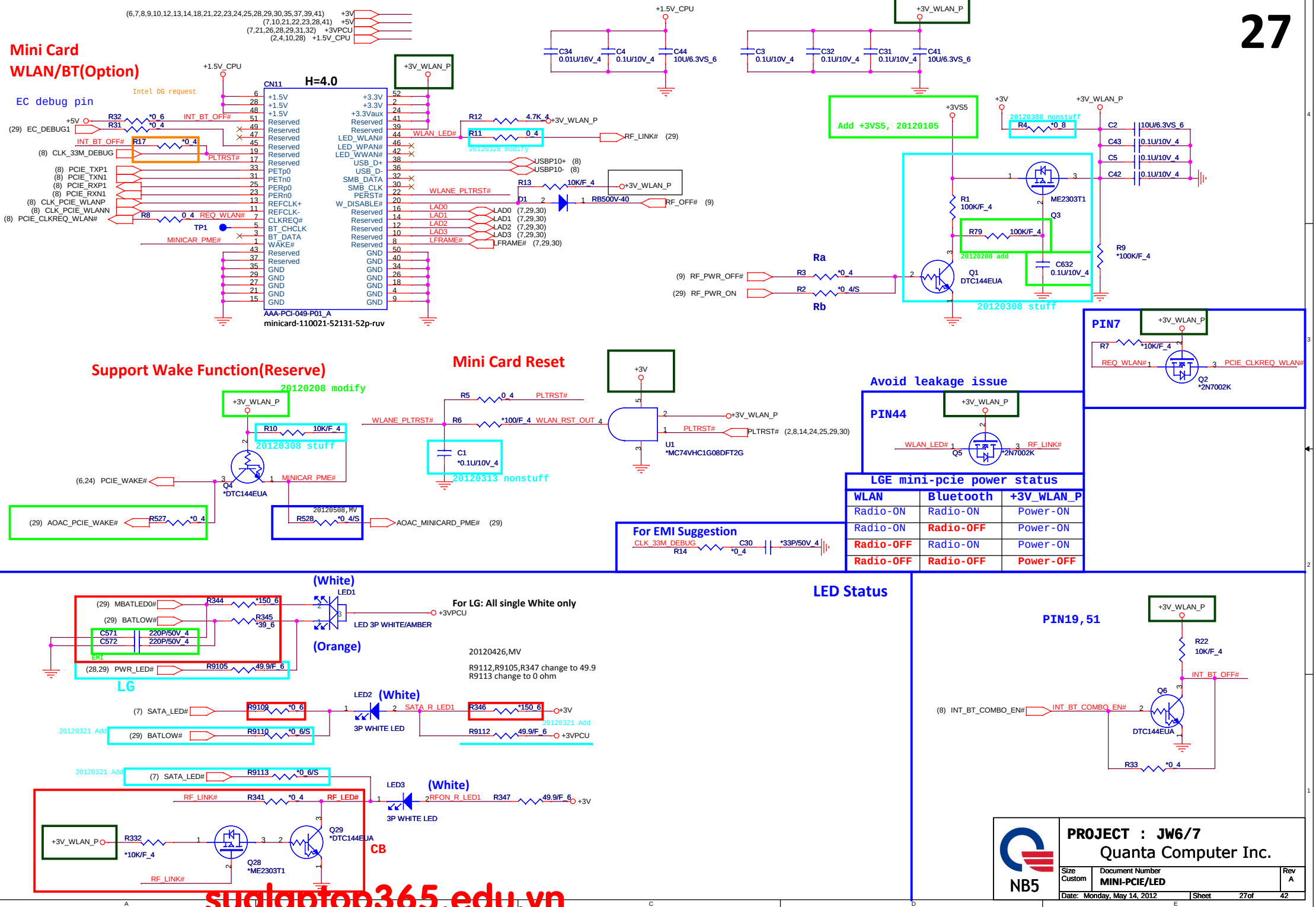




PROJECT :	JW6/7
Quanta Computer Inc.	
Size: Custom	Document Number: USB 3.0/KB/Green CLK
Rev: A	
Date: Friday, May 11, 2012	Sheet: 26of 42

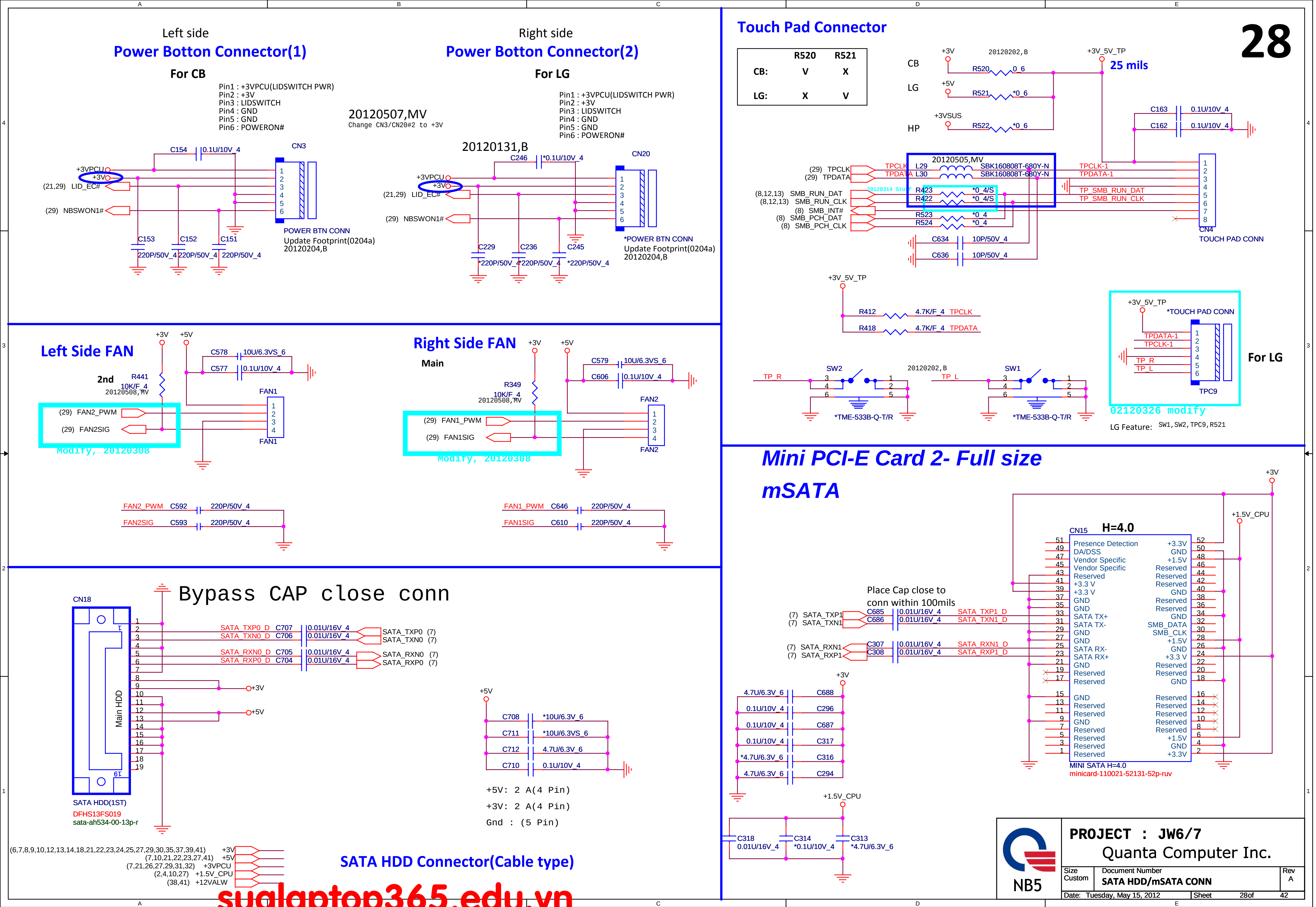
NB5

Mini Card
WLAN/BT(Option)



PROJECT :	JW6/7
Quanta Computer Inc.	
Size: Custom	Document Number: MINI-PCIE/LED
Rev: A	
Date: Monday, May 14, 2012	Sheet: 27 of 42

NB5



IT8518E/HX

Select Pin

	Vpro Select
Vpro	Ra
Non-Vpro	Rb

Select Pin

	CB/LG Select
LG	Ra
CB	Rb

Layout Note:
Place all capacitors close to IT8502N.

Platform	ADC
JW6/7	0V
Reserve	0.75V
Reserve	1.5V
Reserve	2.25V
JW3	3V

Vender	Size	P/N
EON	4MB	AKE39ZN0Q02 (EN25Q32B-104HIP)
AMIC	4MB	AKE39F-0800 (A25LQ32AM-F/Q)
Socket		DFHS08FS023

Socket: DFHS08FS023

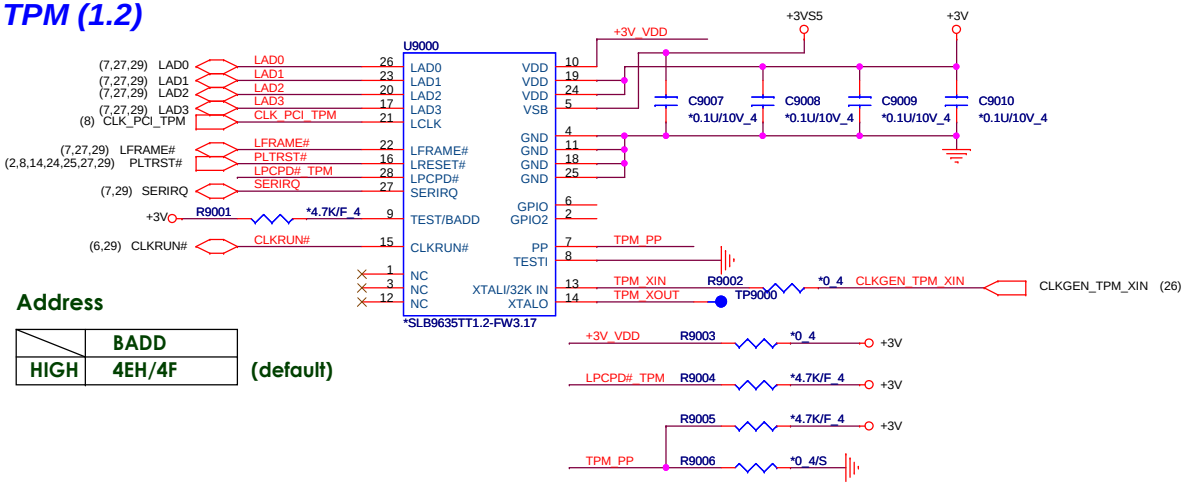
For Battery charge/Therm2

For PCH SMB/DDR Thermal IC/VGA and Cap board

thermal shutdown circuit

PROJECT	JW6/7
Quanta Computer Inc.	
NB5	
Size: Custom	Document Number: Embedded Controller (ITE_IT8518)
Rev	A
Date: Friday, May 11, 2012	Sheet 29 of 42

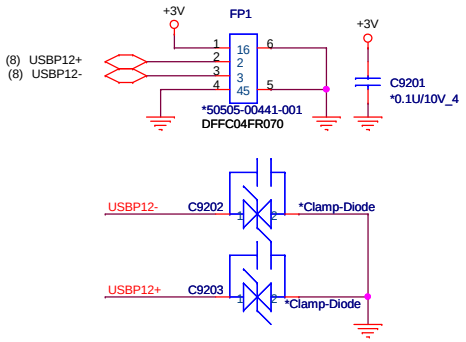
TPM (1.2)



Address

	BADD
HIGH	4EH/4F (default)

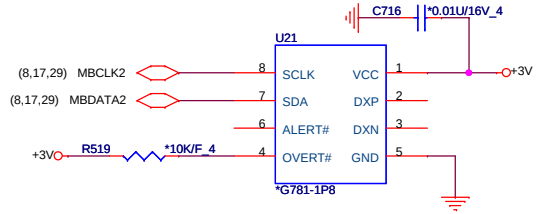
Finger Printer



Local Thermal Sensor

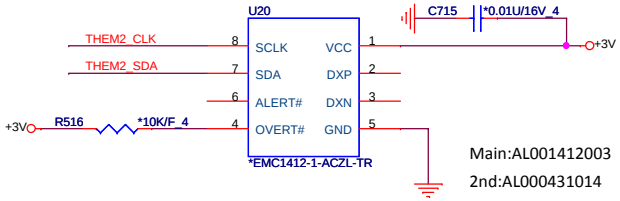
20120131,B

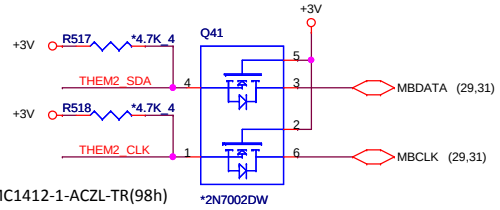
Thermal Solution(Close to GPU)



Main:AL000781039 G781-1P8(9Ah)
2nd:AL001412005 EMC1412-2-ACZL-TR(9Ah)

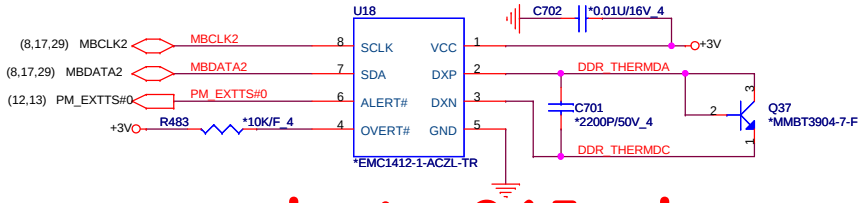
Thermal Solution(Close to CRT)



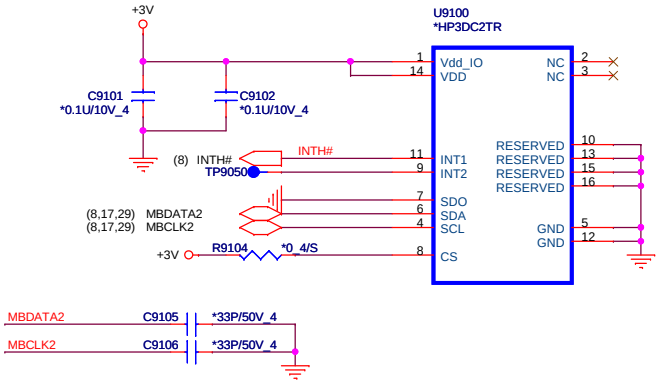


Main:AL001412003 EMC1412-1-ACZL-TR(98h)
2nd:AL000431014 TMP431ADGKR(98h)

DDR3 Thermal Sensor



Accelerometer Sensor



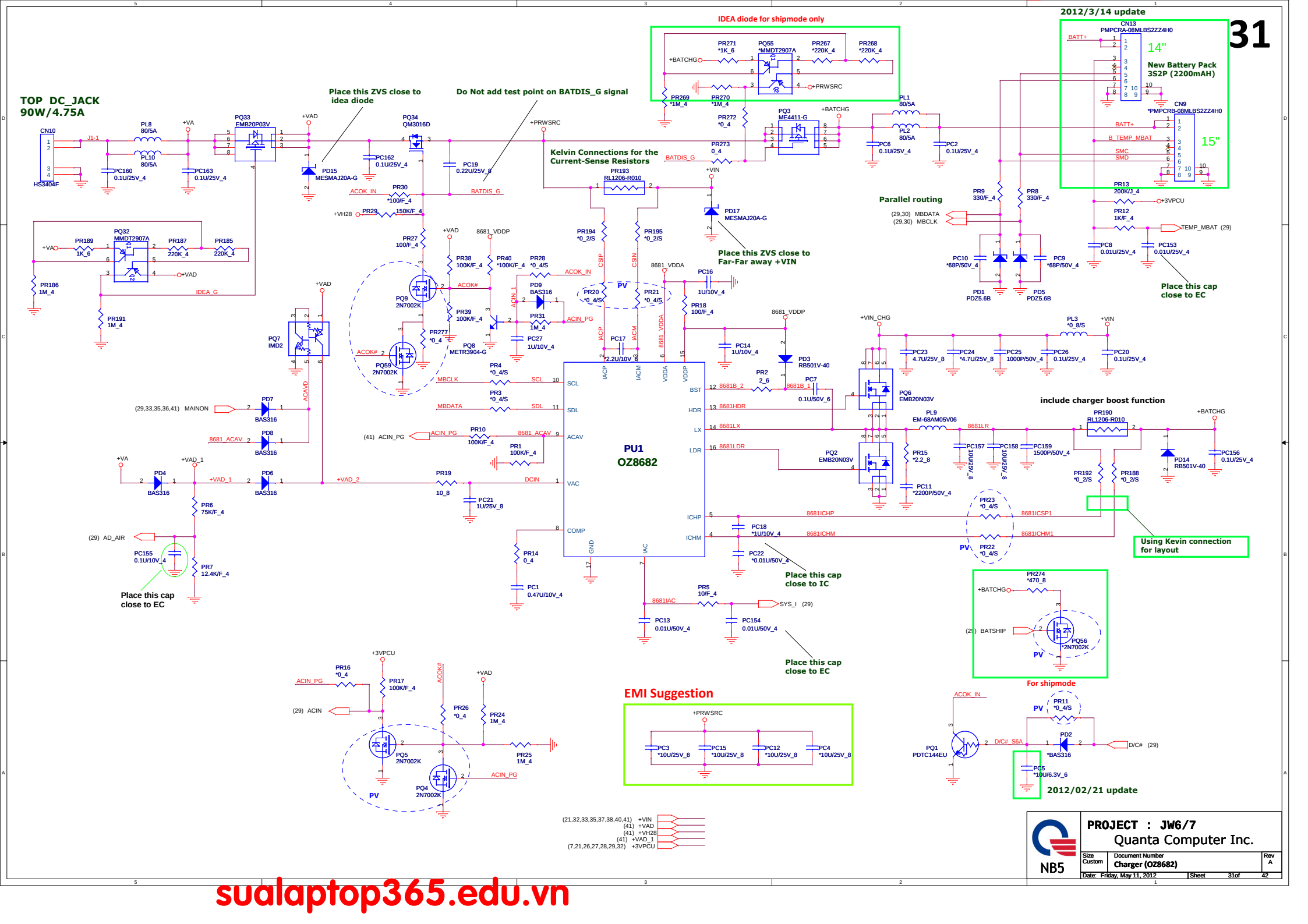
SGT-LIS302DLTR interrupt pin default is low / active Hi , BIOS need to programming 22h to change status from active Hi to low

I2C (ST HP3DC2) SDO,Pin7	
0x50	Gnd **Default**
0x52	VDD

NB5

PROJECT : JW6/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	G-sensor/FP/TPM/THEM	A
Date: Friday, May 11, 2012	Sheet 30 of 42	


31
2012/3/14 update
IDEA diode for shipmode only
TOP DC_JACK
90W/4.75A
Place this ZVS close to idea diode
Do Not add test point on BATDIS_G signal
Kelvin Connections for the Current-Sense Resistors
Parallel routing
14"
New Battery Pack
3S2P (2200mAH)
15"
Place this ZVS close to Far-Far away +VIN
Place this cap close to EC
include charger boost function
Using Kevin connection for layout
Place this cap close to IC
Place this cap close to EC
Place this cap close to EC
PU1
OZ8682
EMI Suggestion
For shipmode
2012/02/21 update
PROJECT : JW6/7
Quanta Computer Inc.
NB5
Charger (OZ8682)
Date: Friday, May 11, 2012
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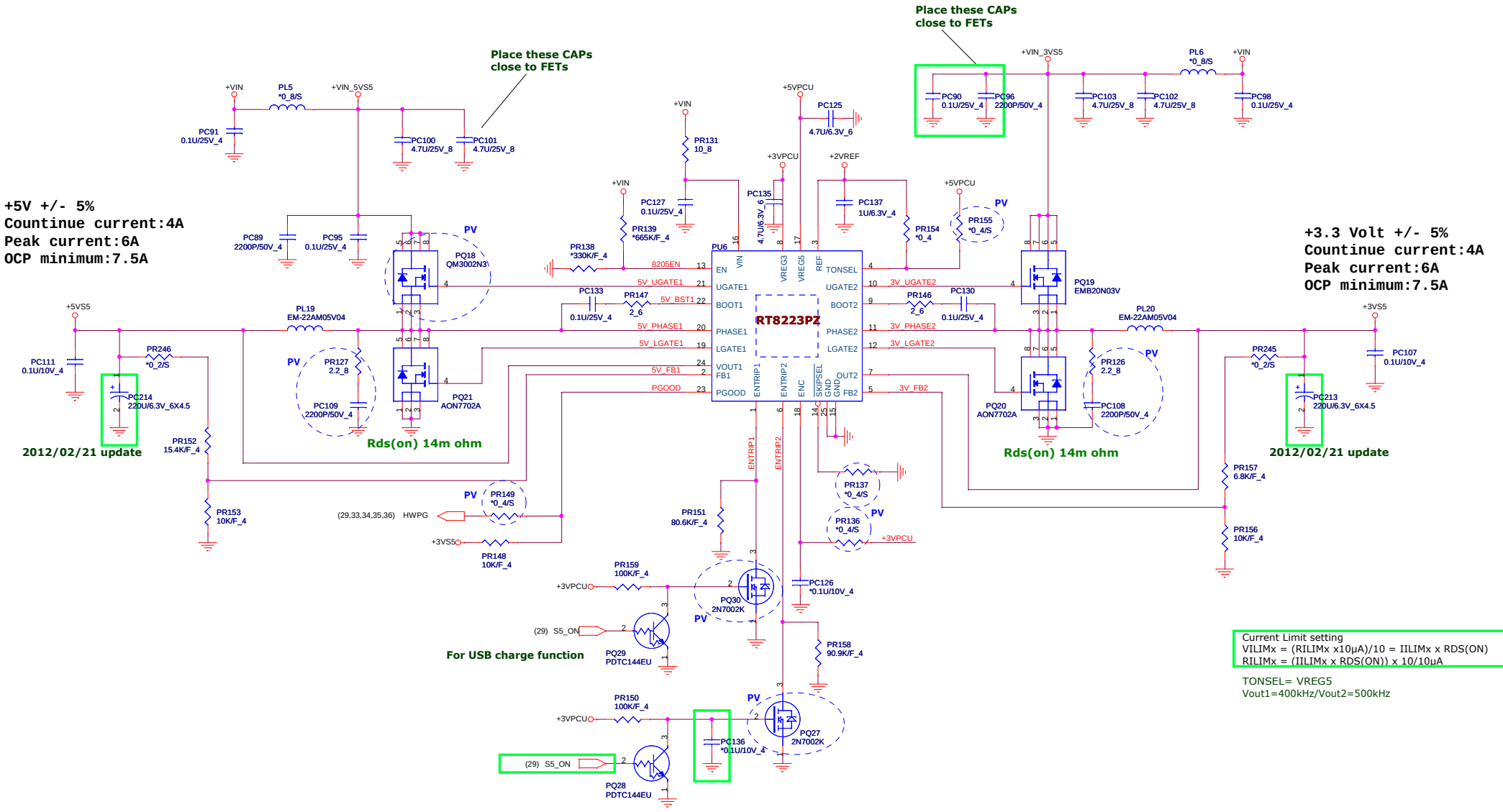
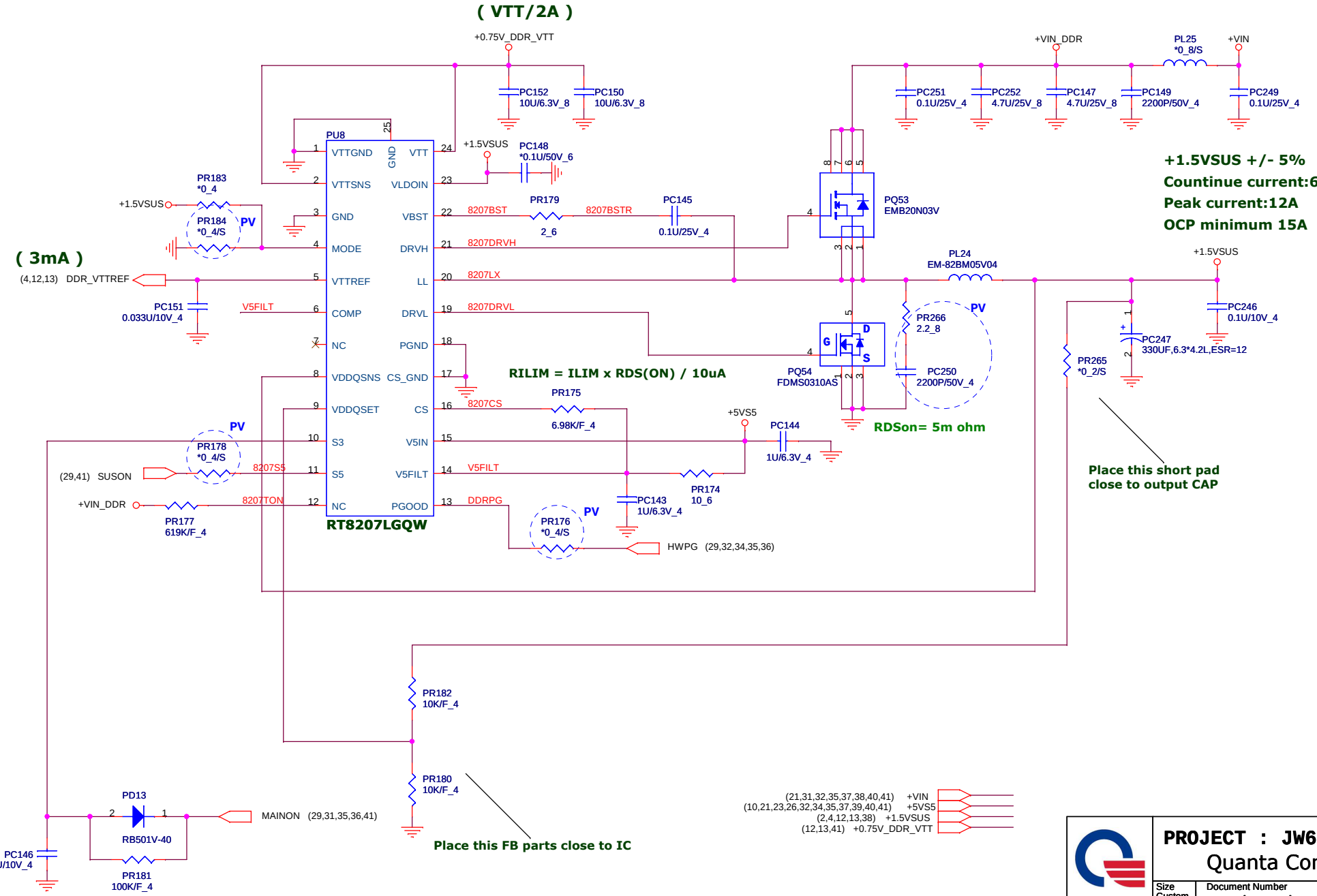
sualaptop365.edu.vn

DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW



PROJECT :	JW6/7
Quanta Computer Inc.	
NB5	Size: Custom; Document Number: 3/5VS5 (RT8223P); Rev: A
Date: Friday, May 11, 2012	Sheet 32 of 42



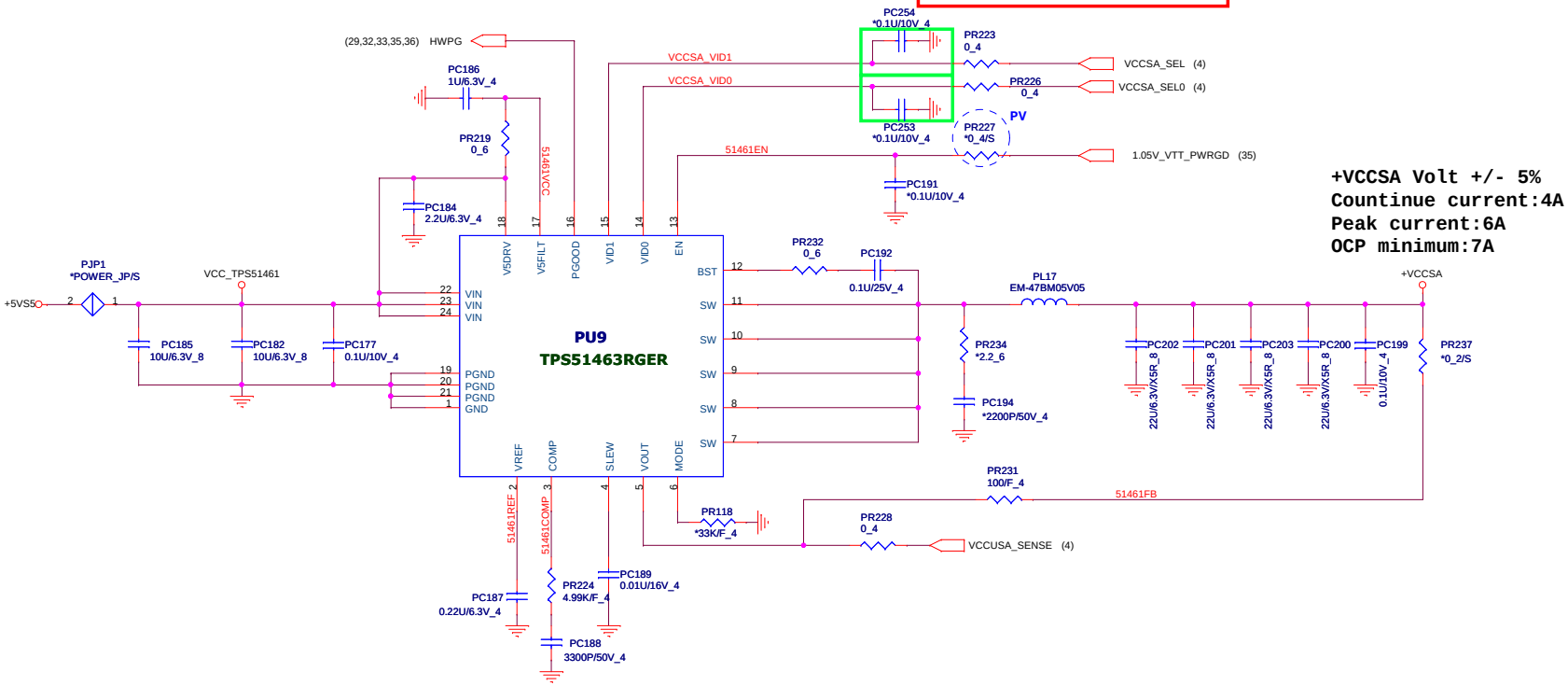
NB5	PROJECT : JW6/7 Quanta Computer Inc.	
Size: Custom	Document Number: DDR3 (RT8207)	Rev: A
Date: Friday, May 11, 2012	Sheet: 33of	42

ULV
17W

CPU system agent voltage slew rate of 0.5 -10 mV/µs

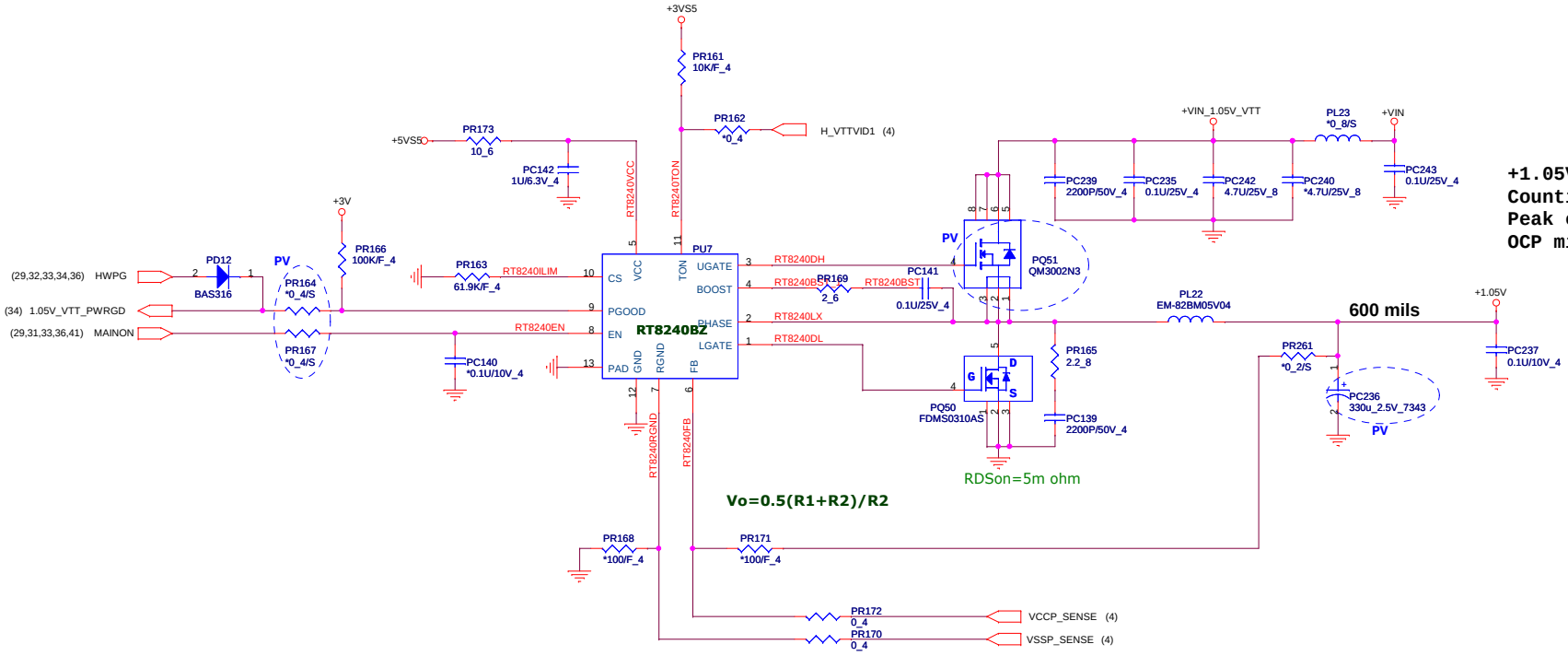
SEL0	SEL1	+VCCSA
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

VCCSA	PU9
35W	TPS51462RGER
ULV 17W	TPS51463RGER



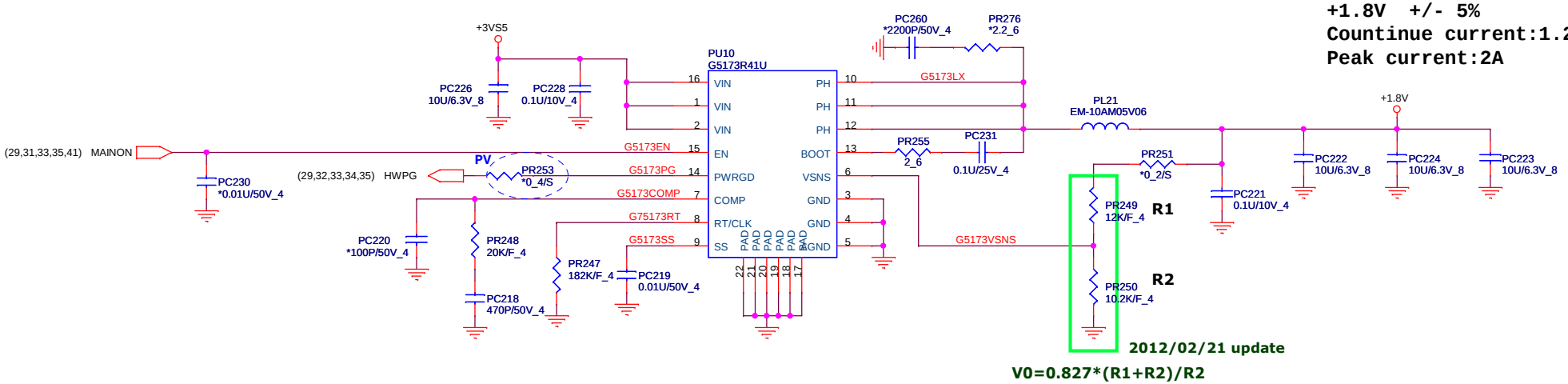
+VCCSA Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7A

NB5	PROJECT : JW6/7 Quanta Computer Inc.	
Size: Custom	Document Number: +VCCSA (TPS51462RGER)	Rev: A
Date: Friday, May 11, 2012	Sheet: 34of 42	

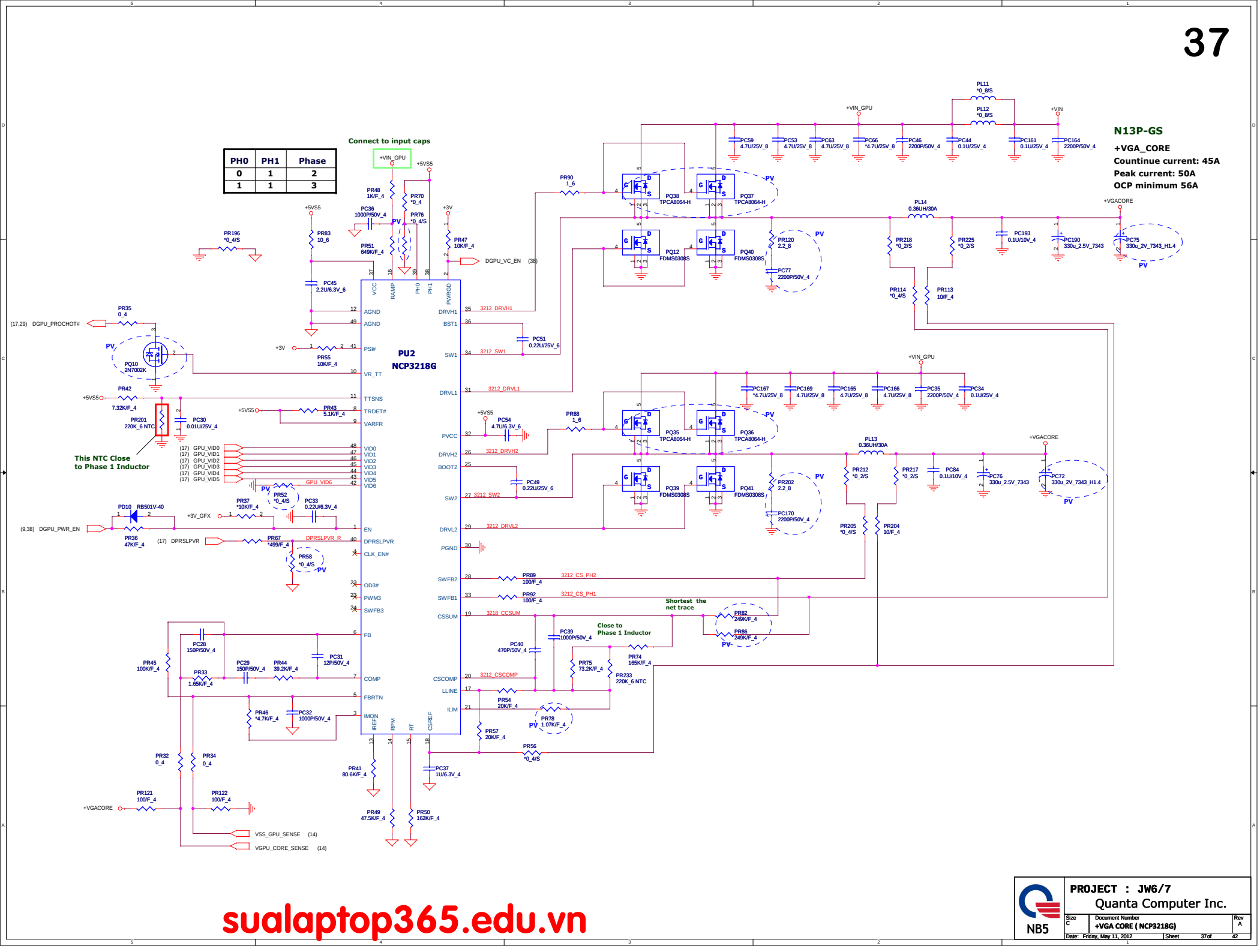


+1.05V_VTT +/- 5%
Countinue current:10A
Peak current: 12A
OCP minimum: 14.5A

NB5	**PROJECT : JW6/7** Quanta Computer Inc.	
Size: Custom	Document Number: **+1.05V (RT8240B)**	Rev: A
Date: Friday, May 11, 2012	Sheet: 35of 42	



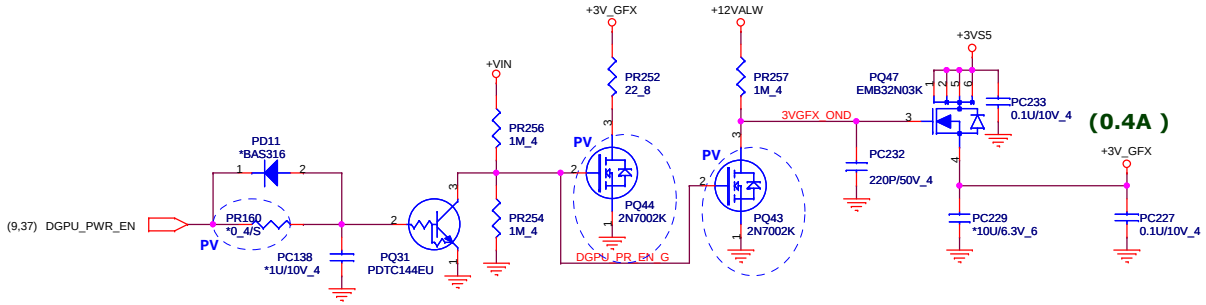
NB5	PROJECT : JW6/7 Quanta Computer Inc.	
Size B	Document Number +1.8V (G9661)	Rev A
Date: Friday, May 11, 2012	Sheet 36of 42	

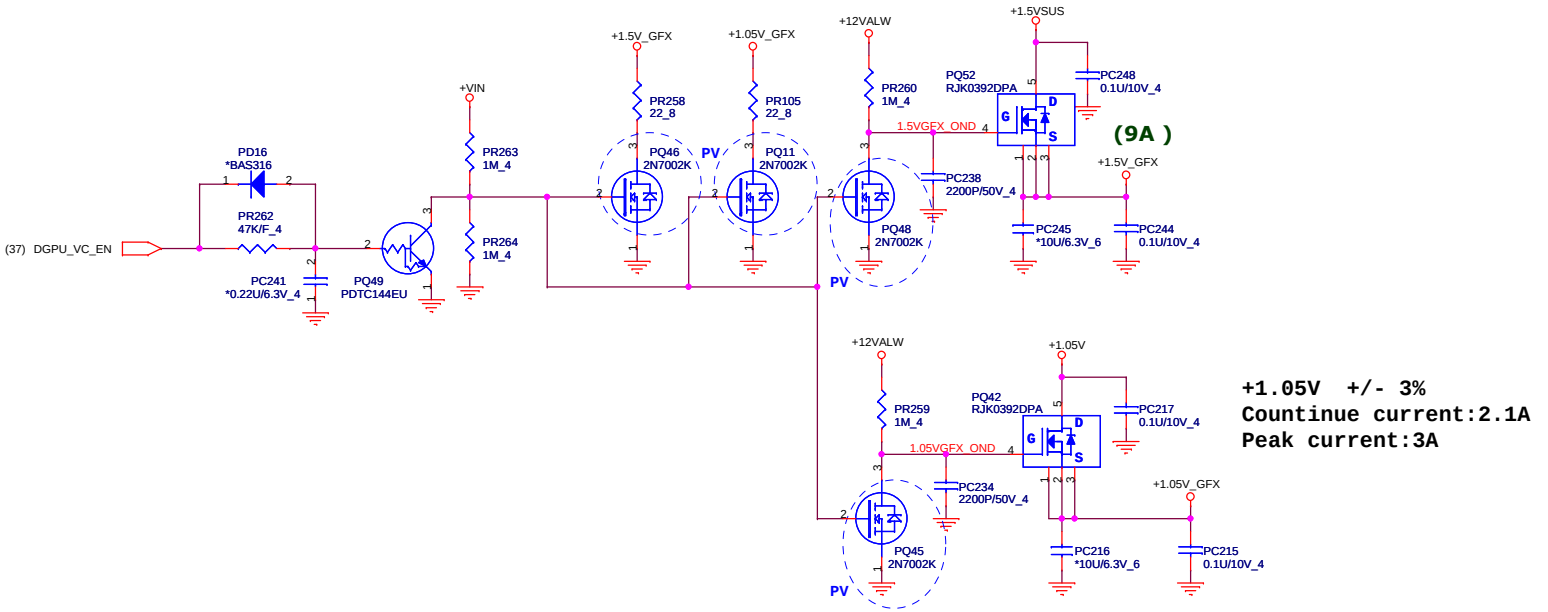


PROJECT : JW6/7		
Quanta Computer Inc.		
NB5	Size C	Document Number +VGA CORE (NCP3218G) Rev A
	Date: Friday, May 11, 2012	Sheet 37of 42

VGA

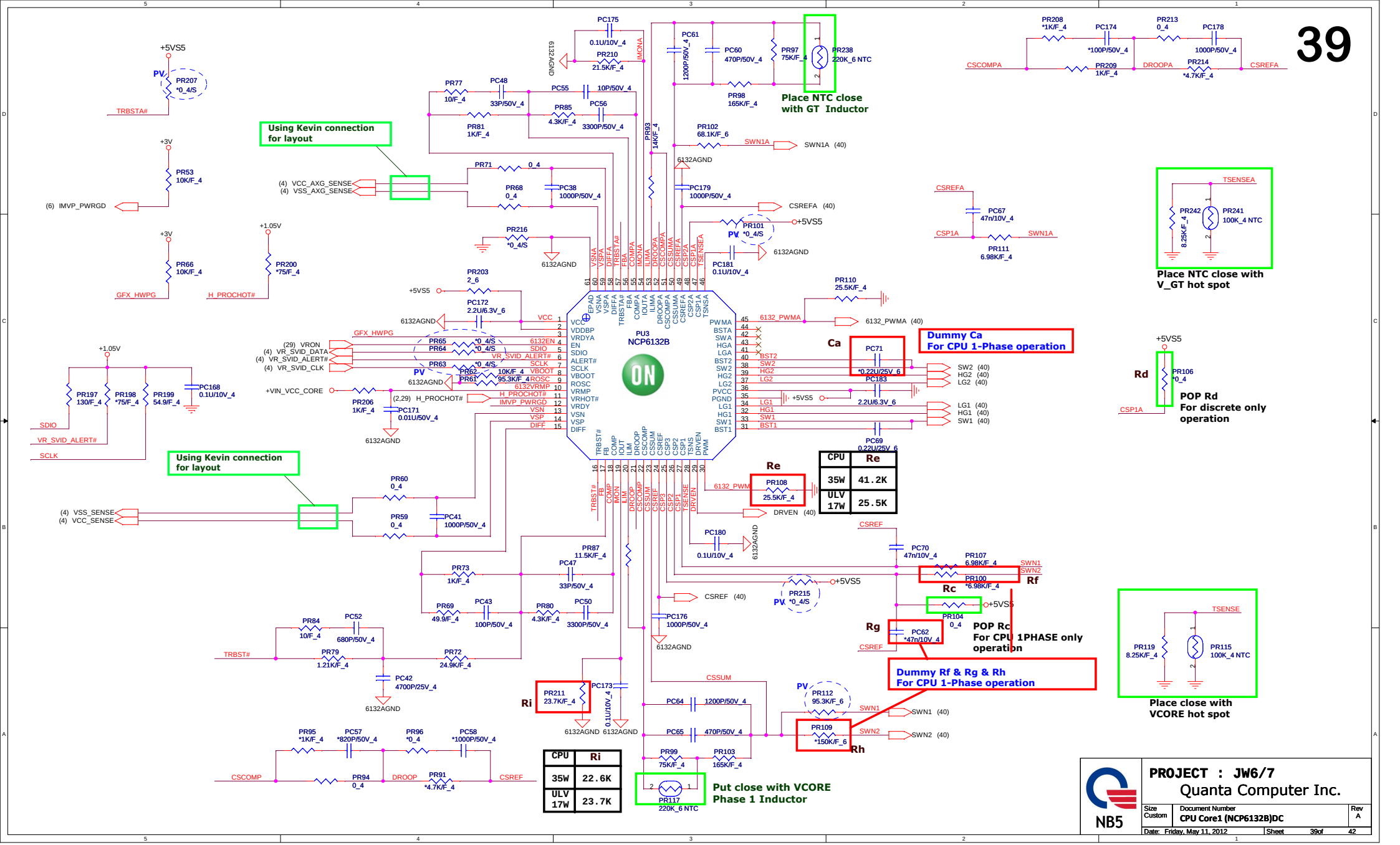
(2,4,12,13,33) +1.5VSUS
(3,9,10,21,26,27,29,30,32,35,36,41) +3VS5
(14,16,17,18,37) +3V_GFX
(15,18,19,20) +1.5V_GFX
(14,15,16,18) +1.05V_GFX
(41) +12VALW
(2,4,6,7,8,10,26,29,35,39) +1.05V

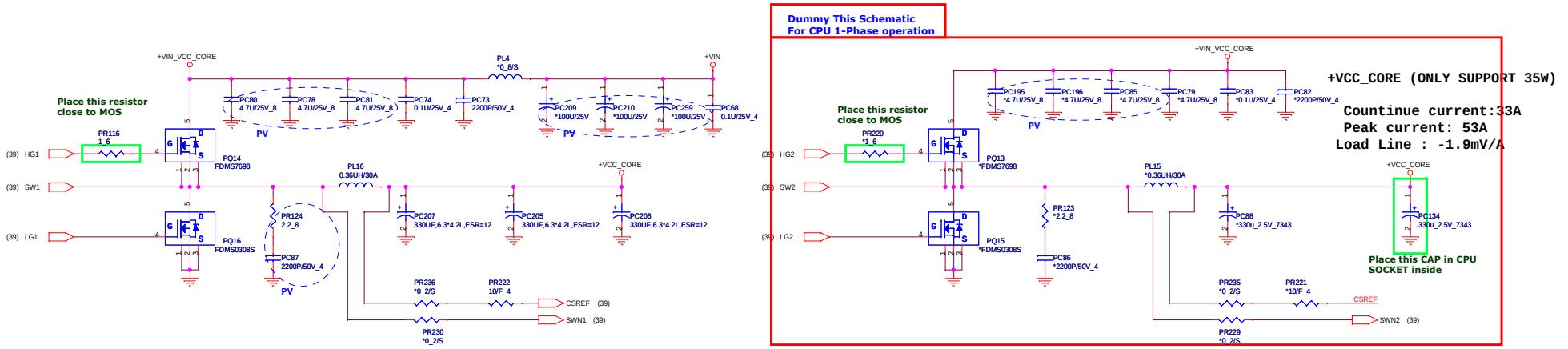




+1.05V +/- 3%
Countinue current:2.1A
Peak current:3A

NB5	PROJECT : JW6/7 Quanta Computer Inc.	
Size: Custom	Document Number: +VGA POWER	Rev: A
Date: Friday, May 11, 2012	Sheet: 38of 42	



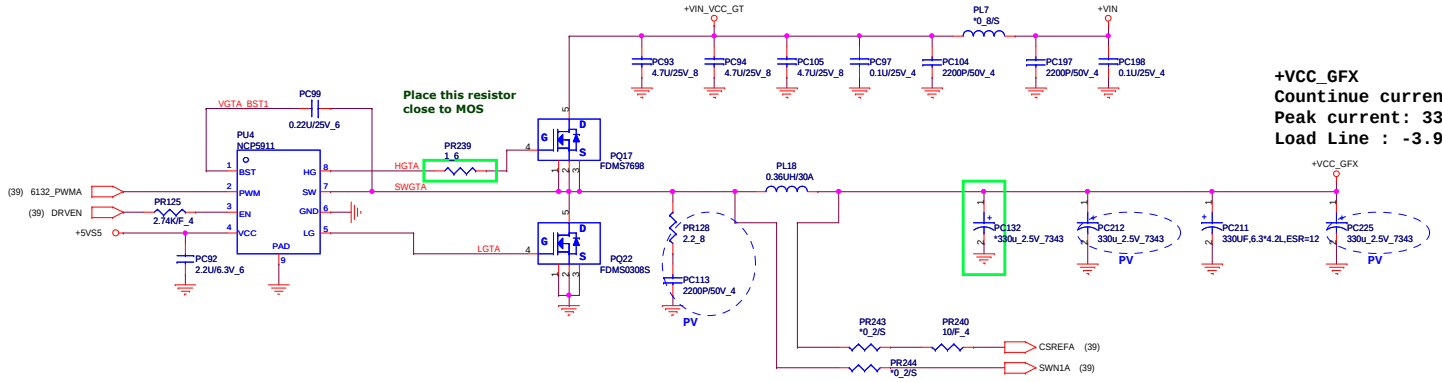


+VCC_CORE (ONLY SUPPORT 35W)

Countinue current:33A
Peak current: 53A
Load Line : -1.9mV/A

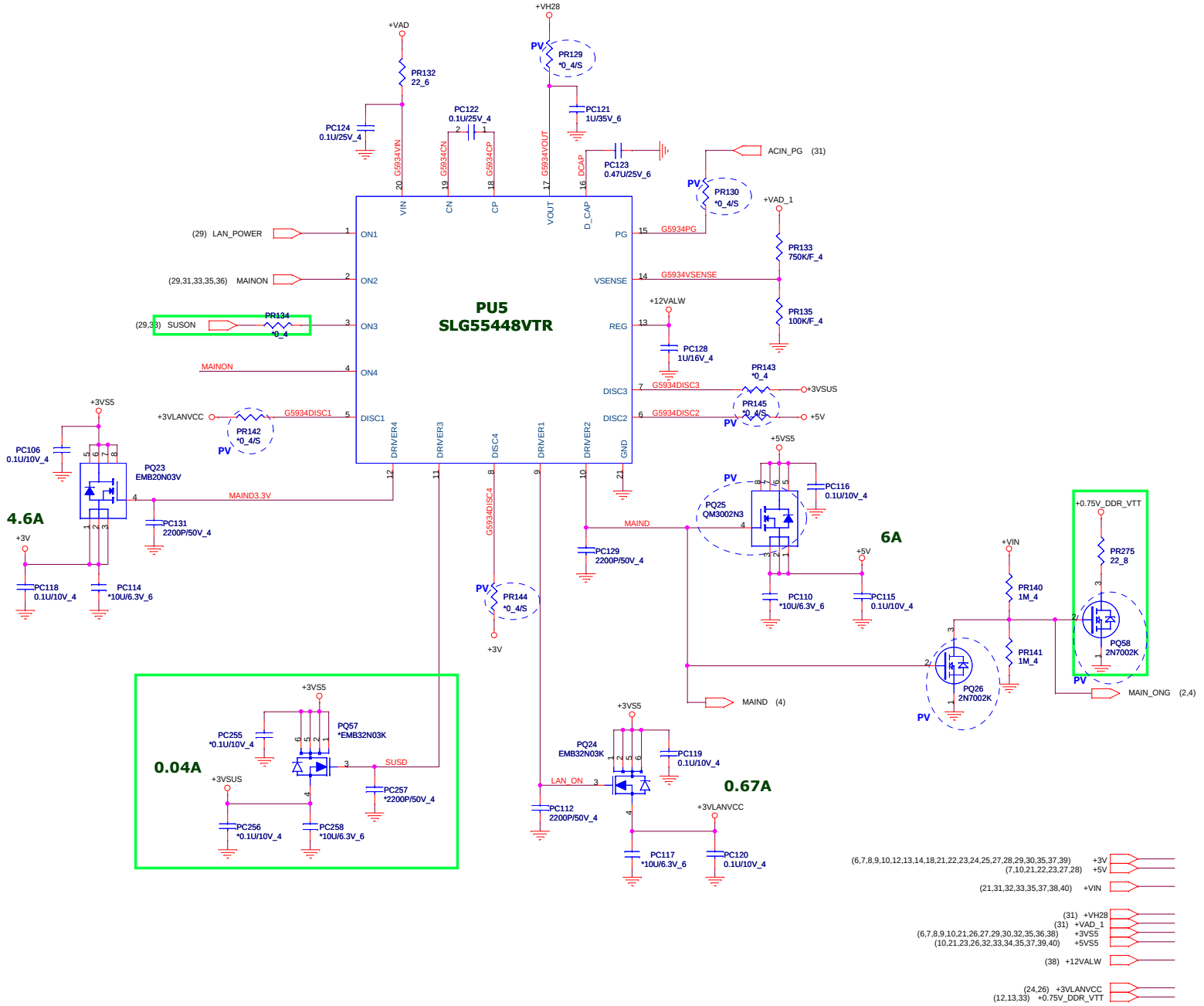
+VCC_CORE (ULV 17W)

TDC : 25A
Peak current: 33A
Load Line : -2.9mV/A



+VCC_GFX
Countinue current:21.5A
Peak current: 33A
Load Line : -3.9mV/A

NB5	PROJECT : JW6/7 Quanta Computer Inc.	
Size C	Document Number CPU Core2 (NCP5911)DC	Rev A
Date: Friday, May 11, 2012	Sheet 40of 42	



NB5

PROJECT : JW6/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Dis-charge IC (SLG55448V)	A

Date: Friday, May 11, 2012 | Sheet 41 of 42

NB5

PROJECT : JW6/7

Quanta Computer Inc.

Size	Document Number	Rev
C	History	A

Date: Friday, May 11, 2012 | Sheet 42of 42