MODEL NAME : VAW00
PROJECT CODE : ANRVAW0000
PCB NO : LA-9104P (Thames XT)

DA60000VV00 LA-9104P M/B
DA40001FO00 LS-9101P POWER BUTTON/B
DA40001FP00 LS-9102P USB/B
DA40001FQ00 LS-9103P TP BUTTON/B

ZZZ R1@
PCB VAW00 LA-9104P LS-9101P/9102P/9103P
DAZ0SZ00200

ZZZ GCER3@
PCB VAW00 LA-9104P LS-9101P/9102P/9103P GOLD A31 !
DAZ0SZ00201

ZZZ TRIR3@
PCB VAW00 LA-9104P LS-9101P/9102P/9103P TRIPOD A31 !
DAZ0SZ00202

ZZZ HANNR3@
PCB VAW00 LA-9104P LS-9101P/9102P/9103P HANNSTARB A31 !
DAZ0SZ00203

ZZZ ZDTR3@
PCB VAW00 LA-9104P LS-9101P/9102P/9103P ZDT A31 !
DAZ0SZ00204

Dell / Compal Confidential

Schematic Document

Intel Chief River
Ivy Bridge(BGA) + Panther Point
OAK 15" UMA/DIS AMD Thames XT

2012-08-22

Rev: 1.0

46@ : for 46 level
@ : Nopop Component
CONN@ : Connector Component
KB9012@ : ENE KB9012 Implemented
UMA@ : Only for UMA
EMC@ : EMI/ESD parts

GCLK@ : Green CLK implemented
GCLKUMA@ : Green CLK for UMA
GCLKDIS@ : Green CLK for DIS
XTAL@ : X'tal implemented
XTALDIS@ : X'tal with DIS implemented

R1@ : R1 P/N
R3@ : R3 P/N

i3R1@ : CPU i3-3217 1.8G
i3VOSR1@ : CPU i3-2365 1.4G
i5R1@ : CPU i5-3317 1.7G
i7R1@ : CPU i7-3517 1.9G
CELR1@ : CPU Celeron 887 1.5G
PENR1@ : CPU Pentium 997 1.6G

DIS@ : Only for Discrete
TH@/THR1@ : Thames-XT
MS@/MSR1@ : Mars Pro
X76@ :
SPI-ROM & VRAM Group

Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

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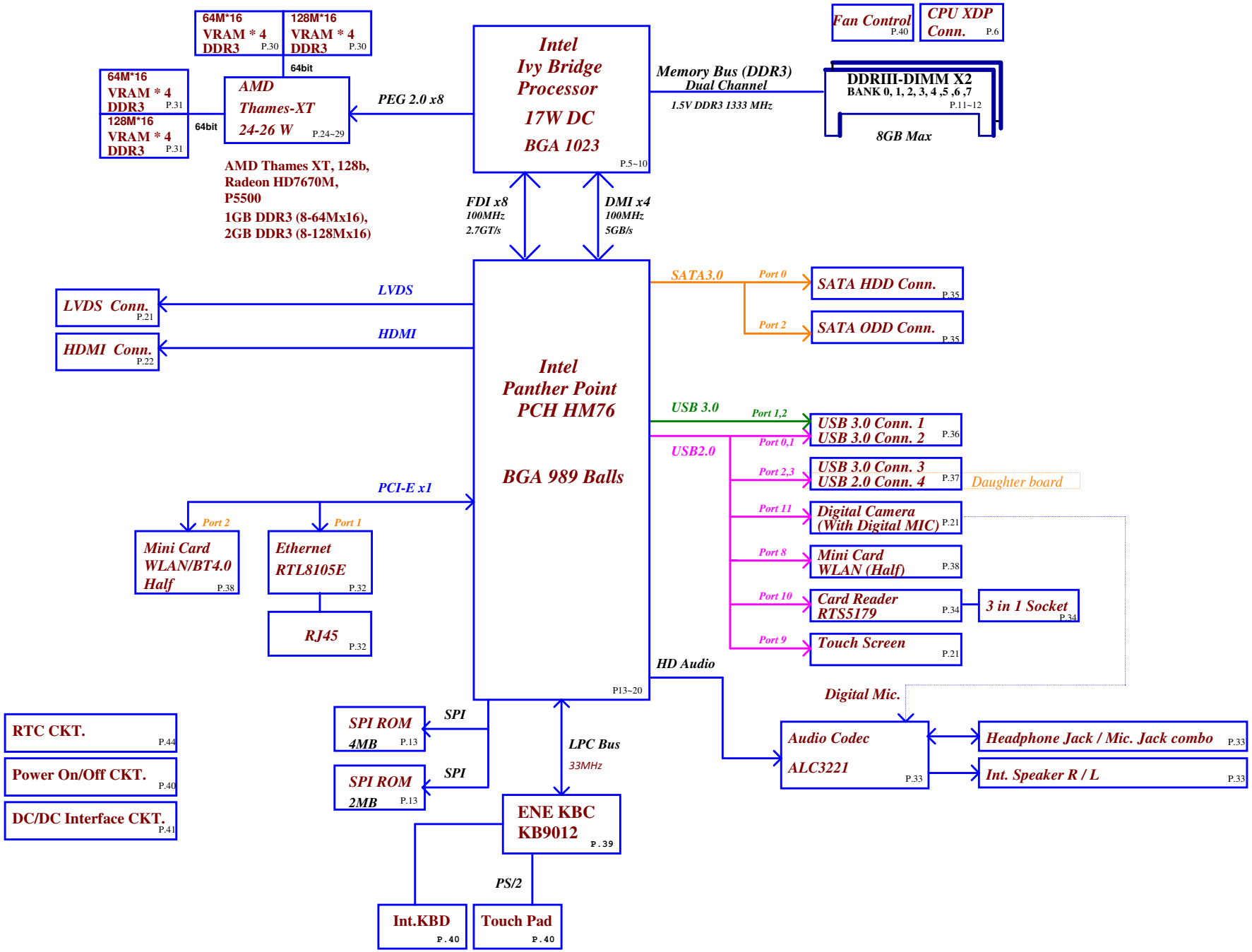
Compal Electronics, Inc.

Title: Cover Page

Size: Custom | Document Number: LA-9104P | Rev: 1.0

Date: Wednesday, August 29, 2012 | Sheet 1 of 57



Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

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Compal Electronics, Inc.

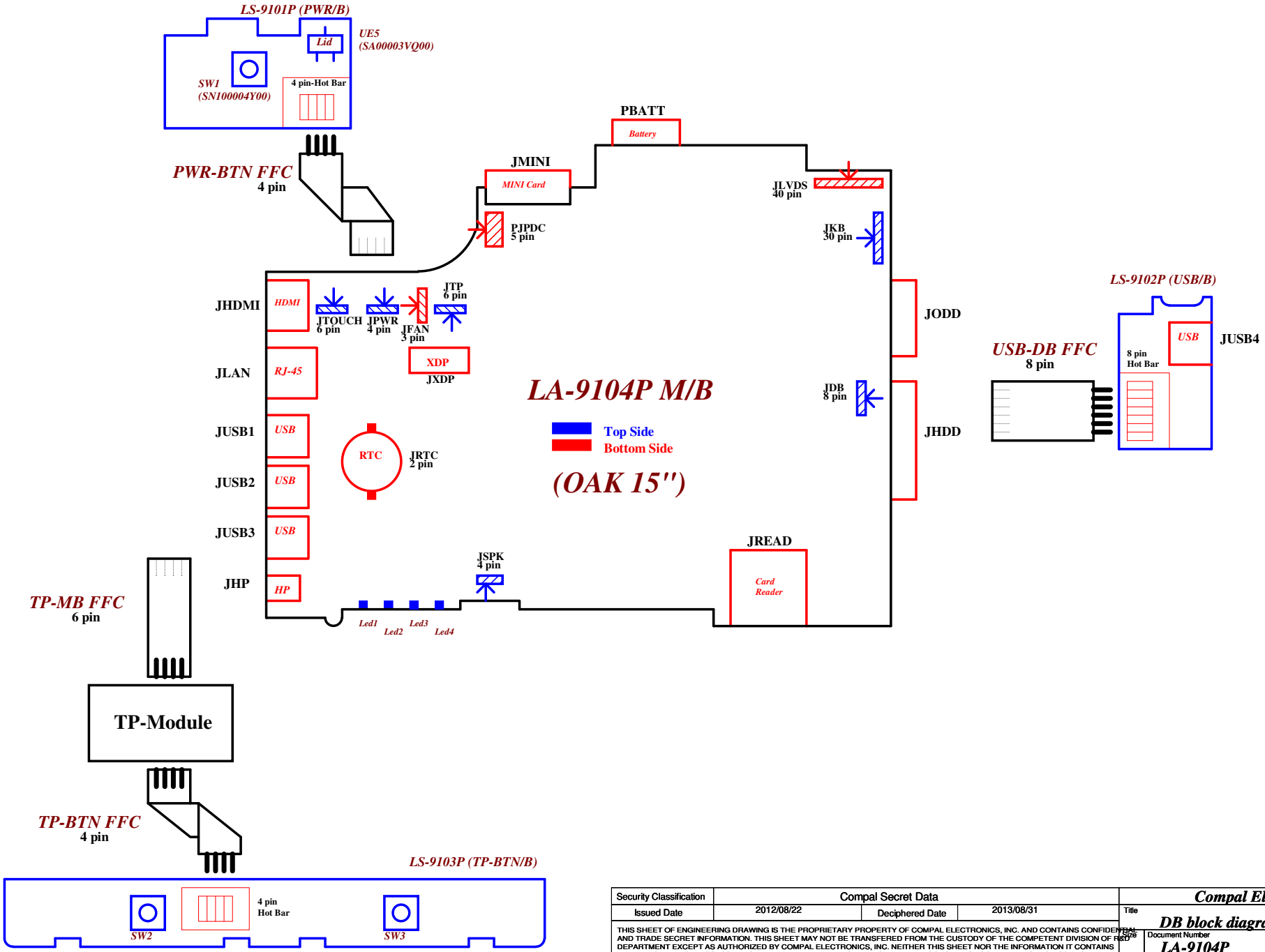
Title: **Block diagram**

Size | Document Number: **LA-9104P** | Rev: 1.0

Date: Wednesday, August 29, 2012 | Sheet 2 of 57

Compal Confidential

Project Code : VAW00
File Name : LA-9104P



Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

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Compal Electronics, Inc.

Title: **DB block diagram**

Size | Document Number: **LA-9104P** | Rev 1.0

Date: Wednesday, August 29, 2012 | Sheet 3 of 57

Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

ID	PCB Revision		
0	0.1		
1		0.1	0.1
2	0.2		
3		0.2	0.2
4	0.3		
5		0.3	0.3
6	1.0		
7		1.0	1.0
	UMA	THM	MARS

Project ID Table

ID	Project Revision
0	
1	
2	
3	
4	
5	UMA
6	DIS THAMES
7	DIS MARS PRO

	USB PORT#	DESTINATION
PCH	0	USB conn.2
	1	USB conn.1
	2	USB conn.3
	3	USB conn.4 (DB)
	4	NC
	5	NC
	6	NC
	7	NC
	8	MINI CARD (WLAN)
	9	Touch Screen
	10	Card Reader
	11	Camera
	12	NC
	13	NC

SMBUS Control Table

	SOURCE	MINI1	MINI2	BATT	SODIMM	Express Card	Thermal Sensor	FFS	VGA Thermal Sensor	VGA	XDP	Charger
EC_SMB_CK1 EC_SMB_DA1	KB9012			V								V
EC_SMB_CK2 EC_SMB_DA2	KB9012								V	V		
PCH_SML0CLK PCH_SML0DATA	PCH											
PCH_SML1CLK PCH_SML1DATA	PCH											
MEM_SMBCLK MEM_SMBDATA	PCH	V	V		V	V		V			V	

Link

	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
CLK	CLKOUT_PCIE0	10/100 LAN	CLKOUTFLEX0	None
	CLKOUT_PCIE1	MINI CARD WLAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	None
	CLKOUT_PCIE3	None	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC LPC
PCI2	None
PCI3	None
PCI4	None

SATA	DESTINATION
SATA0	HDD
SATA1	None
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

PCI EXPRESS	DESTINATION
Lane 1	10/100 LAN
Lane 2	MINI CARD (WLAN)
Lane 3	None
Lane 4	None
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

Symbol Note :

: means Digital Ground

: means Analog Ground

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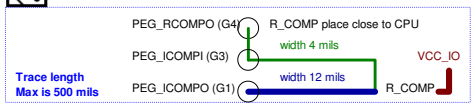
UC1 i3R1@ SA00005L52L AV80638010584 01-SR0N9-L1-1.8G_BGA1023~D
UC1 i3R3@ SA00005L53L AV80638010584 01-SR0N9-L1-1.8G_BGA1023~D
UC1 i3VOSR1@ SA00005UH1L AV8062701313000-SR0U3-J1-1.4G_BGA1023~D
UC1 i3VOSR3@ SA00005UH2L AV8062701313000-SR0U3-J1-1.4G_BGA1023~D
UC1 i5R3@ SA00005K62L AV8063801058002-SR0N8-L1-1.7G_BGA1023~D
UC1 i7R1@ SA00005K53L AV8063801057605-SR0N6-L1-1.9G_BGA1023~D
UC1 i7R3@ SA00005K52L AV8063801057605-SR0N6-L1-1.9G_BGA1023~D
UC1 CELR1@ SA00006021L AV8062701085401-SR0VA-Q0-1.5G_BGA1023~D
UC1 CELR3@ SA00006022L AV8062701085401-SR0VA-Q0-1.5G_BGA1023~D
UC1 PENR1@ SA00005ZZ1L AV8062701084801-SR0V5-Q0-1.6G_BGA1023~D
UC1 PENR3@ SA00005ZZ2L AV8062701084801-SR0V5-Q0-1.6G_BGA1023~D

(1)PEG_RCOMPO (G4) use 4mil connect to PEG_ICOMPI, then use 4mil connect to RC1.
(2)PEG_ICOMPO use 12mil connect to RC1



+VCCP
RC2 24.9_0402_1%

SA00005K63L

UC1A i5R1@

PEG_ICOMPI G3 — PEG_COMP
PEG_ICOMPO G1
PEG_RCOMPO G4

PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

DMI
<15> DMI_CRX_PTX_N0 — DMI_RX#[0] M2
<15> DMI_CRX_PTX_N1 — DMI_RX#[1] P6
<15> DMI_CRX_PTX_N2 — DMI_RX#[2] P1
<15> DMI_CRX_PTX_N3 — DMI_RX#[3] P10
<15> DMI_CRX_PTX_P0 — DMI_RX[0] N3
<15> DMI_CRX_PTX_P1 — DMI_RX[1] P7
<15> DMI_CRX_PTX_P2 — DMI_RX[2] P9
<15> DMI_CRX_PTX_P3 — DMI_RX[3] P11
<15> DMI_CTX_PRX_N0 — DMI_TX#[0] K1
<15> DMI_CTX_PRX_N1 — DMI_TX#[1] M8
<15> DMI_CTX_PRX_N2 — DMI_TX#[2] N4
<15> DMI_CTX_PRX_N3 — DMI_TX#[3] R2
<15> DMI_CTX_PRX_P0 — DMI_TX[0] K3
<15> DMI_CTX_PRX_P1 — DMI_TX[1] M7
<15> DMI_CTX_PRX_P2 — DMI_TX[2] P4
<15> DMI_CTX_PRX_P3 — DMI_TX[3] T3

FDI
<15> FDI_CTX_PRX_N0 — FDI_CTX_PRX_N0 U7 — FDI0_TX#[0] W11
<15> FDI_CTX_PRX_N1 — FDI_CTX_PRX_N1 W1 — FDI0_TX#[1]
<15> FDI_CTX_PRX_N2 — FDI_CTX_PRX_N2 AA6 — FDI0_TX#[2]
<15> FDI_CTX_PRX_N3 — FDI_CTX_PRX_N3 W6 — FDI0_TX#[3]
<15> FDI_CTX_PRX_N4 — FDI_CTX_PRX_N4 N4 — FDI1_TX#[0]
<15> FDI_CTX_PRX_N5 — FDI_CTX_PRX_N5 Y2 — FDI1_TX#[1]
<15> FDI_CTX_PRX_N6 — FDI_CTX_PRX_N6 AC9 — FDI1_TX#[2]
<15> FDI_CTX_PRX_N7 — FDI1_TX#[3]
<15> FDI_CTX_PRX_P0 — FDI_CTX_PRX_P0 U6 — FDI0_TX[0] W10
<15> FDI_CTX_PRX_P1 — FDI_CTX_PRX_P1 W3 — FDI0_TX[1]
<15> FDI_CTX_PRX_P2 — FDI_CTX_PRX_P2 AA7 — FDI0_TX[2]
<15> FDI_CTX_PRX_P3 — FDI_CTX_PRX_P3 W7 — FDI0_TX[3]
<15> FDI_CTX_PRX_P4 — FDI_CTX_PRX_P4 T4 — FDI1_TX[0]
<15> FDI_CTX_PRX_P5 — FDI_CTX_PRX_P5 AA3 — FDI1_TX[1]
<15> FDI_CTX_PRX_P6 — FDI_CTX_PRX_P6 AC8 — FDI1_TX[2]
<15> FDI_CTX_PRX_P7 — FDI_CTX_PRX_P7 — FDI1_TX[3]
<15> FDI_FSYNC0 — FDI_FSYNC0 AA11 — FDI0_FSYNC
<15> FDI_FSYNC1 — FDI_FSYNC1 AC12 — FDI1_FSYNC
<15> FDI_INT — FDI_INT U11 — FDI_INT
<15> FDI_LSYNC0 — FDI_LSYNC0 AA10 — FDI0_LSYNC
<15> FDI_LSYNC1 — FDI_LSYNC1 AG8 — FDI1_LSYNC

PCI EXPRESS - GRAPHICS

PEG_RX#[0] J21 — PEG_GTX_C_HRX_N7 — PEG_GTX_C_HRX_N7 <24>
PEG_RX#[1] B22 — PEG_GTX_C_HRX_N6 — PEG_GTX_C_HRX_N6 <24>
PEG_RX#[2] D21 — PEG_GTX_C_HRX_N5 — PEG_GTX_C_HRX_N5 <24>
PEG_RX#[3] A19 — PEG_GTX_C_HRX_N4 — PEG_GTX_C_HRX_N4 <24>
PEG_RX#[4] D17 — PEG_GTX_C_HRX_N3 — PEG_GTX_C_HRX_N3 <24>
PEG_RX#[5] B14 — PEG_GTX_C_HRX_N2 — PEG_GTX_C_HRX_N2 <24>
PEG_RX#[6] D13 — PEG_GTX_C_HRX_N1 — PEG_GTX_C_HRX_N1 <24>
PEG_RX#[7] A11 — PEG_GTX_C_HRX_N0 — PEG_GTX_C_HRX_N0 <24>
PEG_RX#[8] B10
PEG_RX#[9] G8
PEG_RX#[10] A8
PEG_RX#[11] B6
PEG_RX#[12] H8
PEG_RX#[13] E5
PEG_RX#[14] K7
PEG_RX#[15]

PEG_RX[0] K22 — PEG_GTX_C_HRX_P7 — PEG_GTX_C_HRX_P7 <24>
PEG_RX[1] K19 — PEG_GTX_C_HRX_P6 — PEG_GTX_C_HRX_P6 <24>
PEG_RX[2] C21 — PEG_GTX_C_HRX_P5 — PEG_GTX_C_HRX_P5 <24>
PEG_RX[3] D19 — PEG_GTX_C_HRX_P4 — PEG_GTX_C_HRX_P4 <24>
PEG_RX[4] C19 — PEG_GTX_C_HRX_P3 — PEG_GTX_C_HRX_P3 <24>
PEG_RX[5] D16 — PEG_GTX_C_HRX_P2 — PEG_GTX_C_HRX_P2 <24>
PEG_RX[6] C13 — PEG_GTX_C_HRX_P1 — PEG_GTX_C_HRX_P1 <24>
PEG_RX[7] D12 — PEG_GTX_C_HRX_P0 — PEG_GTX_C_HRX_P0 <24>
PEG_RX[8] C11
PEG_RX[9] C9
PEG_RX[10] F8
PEG_RX[11] C8
PEG_RX[12] C5
PEG_RX[13] H6
PEG_RX[14] F6
PEG_RX[15] K6

PEG_TX#[0] G22 — PEG_HTX_GRX_N7 CC9 1 — 2 DIS@ 220nF 0402 16V7K — PEG_HTX_C_GRX_N7 <24>
PEG_TX#[1] C23 — PEG_HTX_GRX_N6 CC10 1 — 2 DIS@ 220nF 0402 16V7K — PEG_HTX_C_GRX_N6 <24>
PEG_TX#[2] D23 — PEG_HTX_GRX_N5 CC11 1 — 2 DIS@ 220nF 0402 16V7K — PEG_HTX_C_GRX_N5 <24>
PEG_TX#[3] F21 — PEG_HTX_GRX_N4 CC12 1 — 2 DIS@ 220nF 0402 16V7K — PEG_HTX_C_GRX_N4 <24>
PEG_TX#[4] H19 — PEG_HTX_GRX_N3 CC13 1 — 2 DIS@ 220nF 0402 16V7K — PEG_HTX_C_GRX_N3 <24>
PEG_TX#[5] C17 — PEG_HTX_GRX_N2 CC14 1 — 2 DIS@ 220nF 0402 16V7K — PEG_HTX_C_GRX_N2 <24>
PEG_TX#[6] K15 — PEG_HTX_GRX_N1 CC15 1 — 2 DIS@ 220nF 0402 16V7K — PEG_HTX_C_GRX_N1 <24>
PEG_TX#[7] F17 — PEG_HTX_GRX_N0 CC16 1 — 2 DIS@ 220nF 0402 16V7K — PEG_HTX_C_GRX_N0 <24>
PEG_TX#[8] F14
PEG_TX#[9] A15
PEG_TX#[10] J14
PEG_TX#[11] H13
PEG_TX#[12] M10
PEG_TX#[13] F10
PEG_TX#[14] D9
PEG_TX#[15] J4

PEG_TX[0] F22 — PEG_HTX_GRX_P7 CC25 1 — 2 DIS@ 220nF 0402 16V7K — PEG_HTX_C_GRX_P7 <24>
PEG_TX[1] A23 — PEG_HTX_GRX_P6 CC26 1 — 2 DIS@ 220nF 0402 16V7K — PEG_HTX_C_GRX_P6 <24>
PEG_TX[2] D24 — PEG_HTX_GRX_P5 CC27 1 — 2 DIS@ 220nF 0402 16V7K — PEG_HTX_C_GRX_P5 <24>
PEG_TX[3] E21 — PEG_HTX_GRX_P4 CC28 1 — 2 DIS@ 220nF 0402 16V7K — PEG_HTX_C_GRX_P4 <24>
PEG_TX[4] G19 — PEG_HTX_GRX_P3 CC29 1 — 2 DIS@ 220nF 0402 16V7K — PEG_HTX_C_GRX_P3 <24>
PEG_TX[5] B18 — PEG_HTX_GRX_P2 CC30 1 — 2 DIS@ 220nF 0402 16V7K — PEG_HTX_C_GRX_P2 <24>
PEG_TX[6] K17 — PEG_HTX_GRX_P1 CC31 1 — 2 DIS@ 220nF 0402 16V7K — PEG_HTX_C_GRX_P1 <24>
PEG_TX[7] G17 — PEG_HTX_GRX_P0 CC32 1 — 2 DIS@ 220nF 0402 16V7K — PEG_HTX_C_GRX_P0 <24>
PEG_TX[8] E14
PEG_TX[9] C15
PEG_TX[10] K13
PEG_TX[11] G13
PEG_TX[12] K10
PEG_TX[13] G10
PEG_TX[14] D8
PEG_TX[15] K4

eDP
eDP_COMPIO AF3
eDP_ICOMPO AD2
eDP_HPD# AG11
eDP_AUX# AG4
eDP_AUX AF4
eDP_TX#[0] AC3
eDP_TX#[1] AC4
eDP_TX#[2] AE11
eDP_TX#[3] AE7
eDP_TX[0] AC1
eDP_TX[1] AA4
eDP_TX[2] AE10
eDP_TX[3] AE6

+VCCP
RC36 24.9_0402_1% — +EDP_COM
RC158 10K_0402_5% @

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

AV8063801058002-SR0N8-L1-1.7G_BGA1023~D

UC1I i5R1@

VSS
BG17 VSS[181] — VSS[250] M4
BG21 VSS[182] — VSS[251] M58
BG24 VSS[183] — VSS[252] M6
BG28 VSS[184] — VSS[253] N1
BG37 VSS[185] — VSS[254] N17
BG41 VSS[186] — VSS[255] N21
BG45 VSS[187] — VSS[256] N25
BG49 VSS[188] — VSS[257] N28
BG53 VSS[189] — VSS[258] N33
BG9 VSS[190] — VSS[259] N36
C29 VSS[191] — VSS[260] N40
C35 VSS[192] — VSS[261] N43
C40 VSS[193] — VSS[262] N47
D10 VSS[194] — VSS[263] N48
D14 VSS[195] — VSS[264] N51
D18 VSS[196] — VSS[265] N52
D22 VSS[197] — VSS[266] N56
D26 VSS[198] — VSS[267] N61
D29 VSS[199] — VSS[268] P14
D35 VSS[200] — VSS[269] P16
D4 VSS[201] — VSS[270] P18
D40 VSS[202] — VSS[271] P21
D43 VSS[203] — VSS[272] P58
D46 VSS[204] — VSS[273] P59
D50 VSS[205] — VSS[274] P9
D54 VSS[206] — VSS[275] R17
D58 VSS[207] — VSS[276] R20
D6 VSS[208] — VSS[277] R4
E25 VSS[209] — VSS[278] R46
E29 VSS[210] — VSS[279] T1
E3 VSS[211] — VSS[280] T47
E35 VSS[212] — VSS[281] T50
E40 VSS[213] — VSS[282] T51
F13 VSS[214] — VSS[283] T52
F15 VSS[215] — VSS[284] T53
F19 VSS[216] — VSS[285] T55
F29 VSS[217] — VSS[286] T56
F35 VSS[218] — VSS[287] U13
F40 VSS[219] — VSS[288] U8
F55 VSS[220] — VSS[289] V20
G51 VSS[221] — VSS[290] V61
G6 VSS[222] — VSS[291] W13
G61 VSS[223] — VSS[292] W15
H10 VSS[224] — VSS[293] W18
H14 VSS[225] — VSS[294] W21
H17 VSS[226] — VSS[295] W46
H21 VSS[227] — VSS[296] W8
H4 VSS[228] — VSS[297] Y4
H53 VSS[229] — VSS[298] Y47
H58 VSS[230] — VSS[299] Y58
J1 VSS[231] — VSS[300] Y59
J49 VSS[232] — VSS[301] G48
J55 VSS[233]
K11 VSS[234]
K21 VSS[235]
K51 VSS[236]
K8 VSS[237]
L16 VSS[238]
L20 VSS[239]
L22 VSS[240]
L26 VSS[241]
L30 VSS[242]
L34 VSS[243]
L38 VSS[244]
L43 VSS[245]
L48 VSS[246]
L61 VSS[247]
M11 VSS[248]
M15 VSS[249]

@ RC20 1K_0402_5%

NCTF
VSS_NCTF_1 A5
VSS_NCTF_2 A57
VSS_NCTF_3 BC61
VSS_NCTF_4 BD3
VSS_NCTF_5 BD59
VSS_NCTF_6 BE4
VSS_NCTF_7 BE58
VSS_NCTF_8 BG5
VSS_NCTF_9 BG57
VSS_NCTF_10 C3
VSS_NCTF_11 C58
VSS_NCTF_12 D59
VSS_NCTF_13 E1
VSS_NCTF_14 E61

AV8063801058002-SR0N8-L1-1.7G_BGA1023~D

Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

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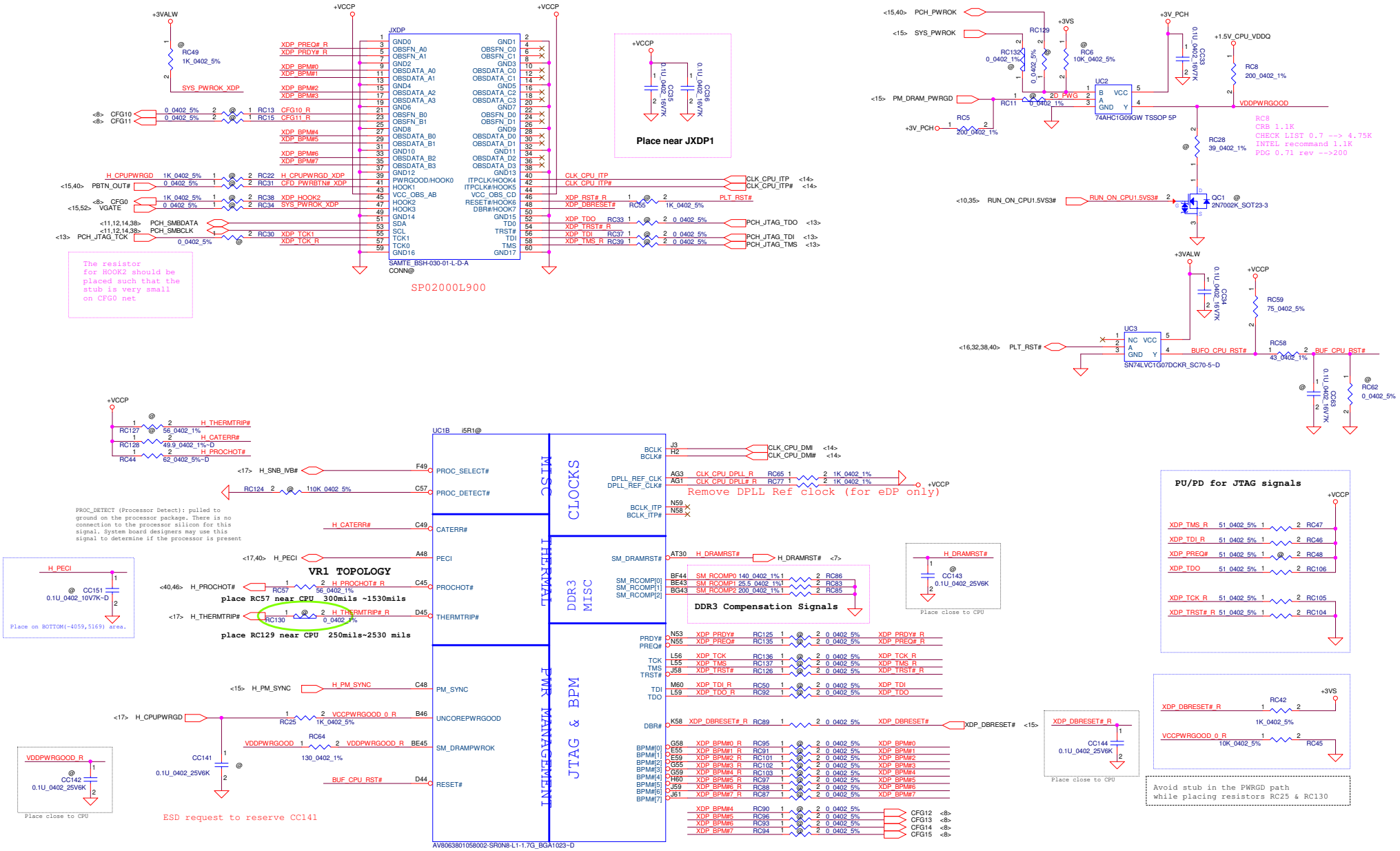
Compal Electronics, Inc.

Title: PROCESSOR(1/6) DMI,FDI,PEG

Size | Document Number: LA-9104P | Rev 1.0

Date: Wednesday, August 29, 2012 | Sheet 5 of 57



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Issued Date	2012/08/22	Deciphered Date	2013/08/31

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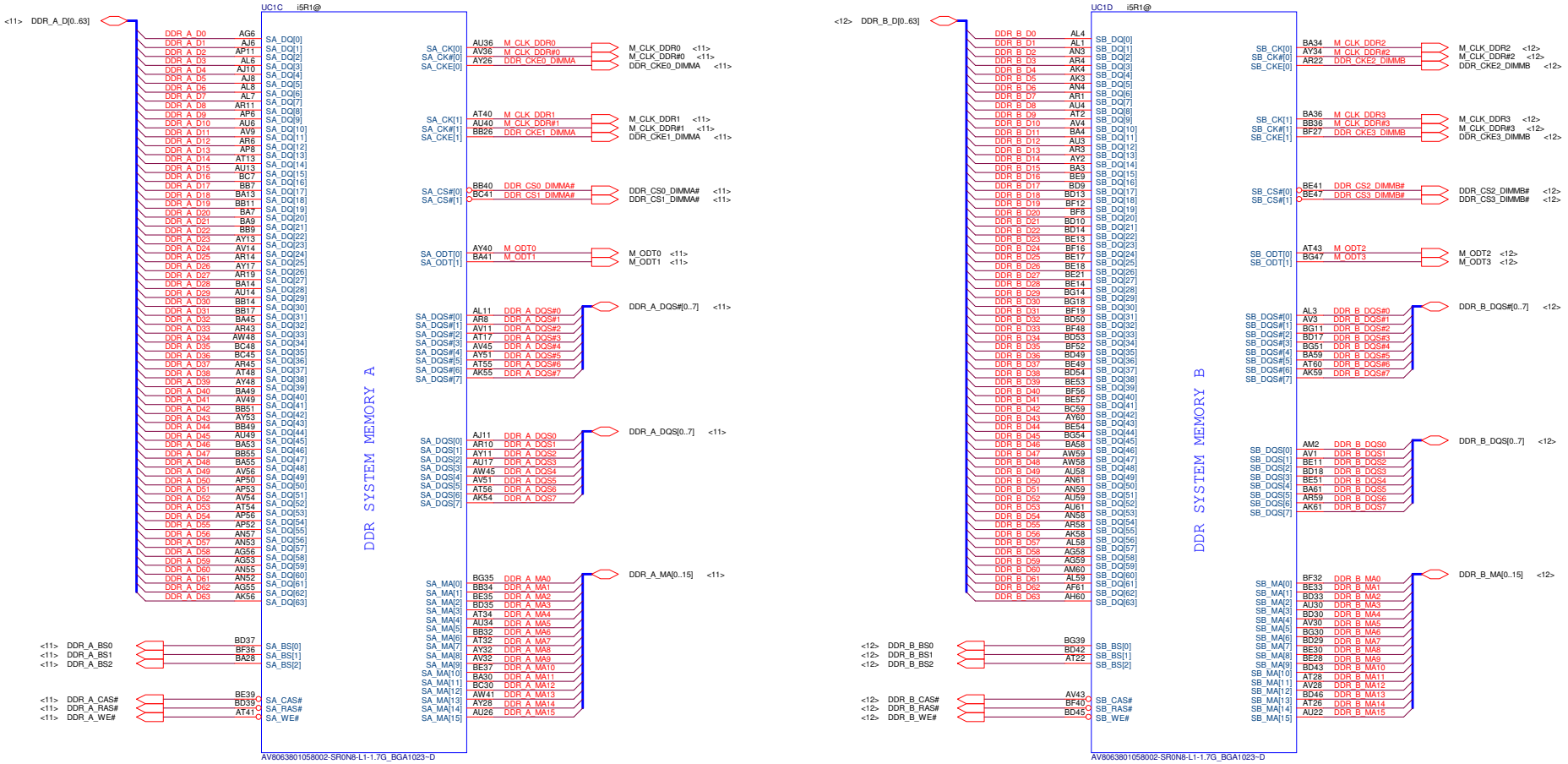
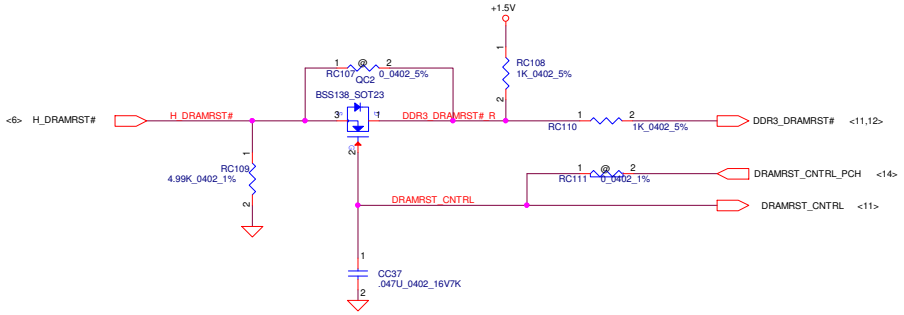
Compal Electronics, Inc.

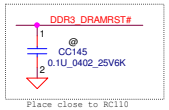
Title: **PROCESSOR(2/6) PM,XDP,CLK**

Size: | Document Number: **LA-9104P** | Rev: 1.0

Date: Wednesday, August 29, 2012 | Sheet 6 of 57







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Issued Date	2012/08/22	Deciphered Date	2013/08/31

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Compal Electronics, Inc.

Title: **PROCESSOR(3/6) DDRIII**

Size | Document Number: **LA-9104P** | Rev: 1.0

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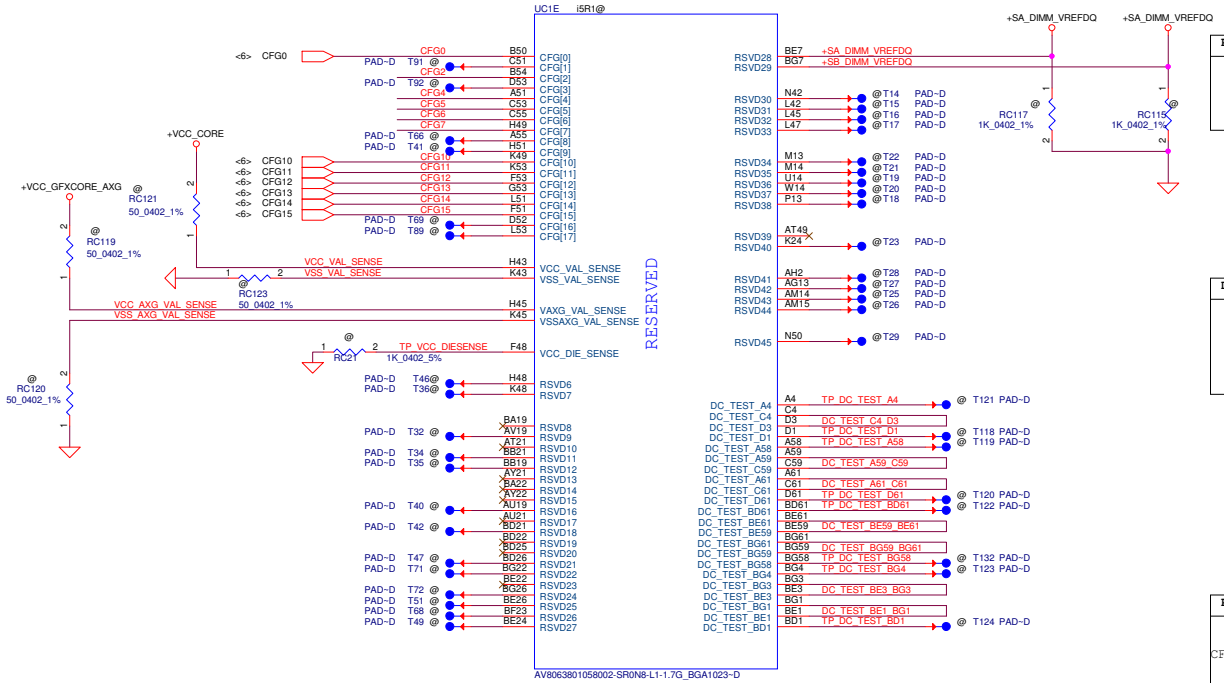
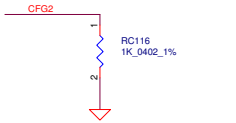
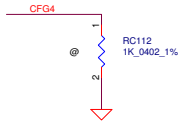
CFG Straps for Processor

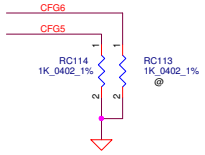




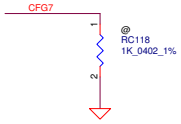
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition ★0:Lane Reversed



Display Port Presence Strap	
CFG4	★ 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled ★10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	★1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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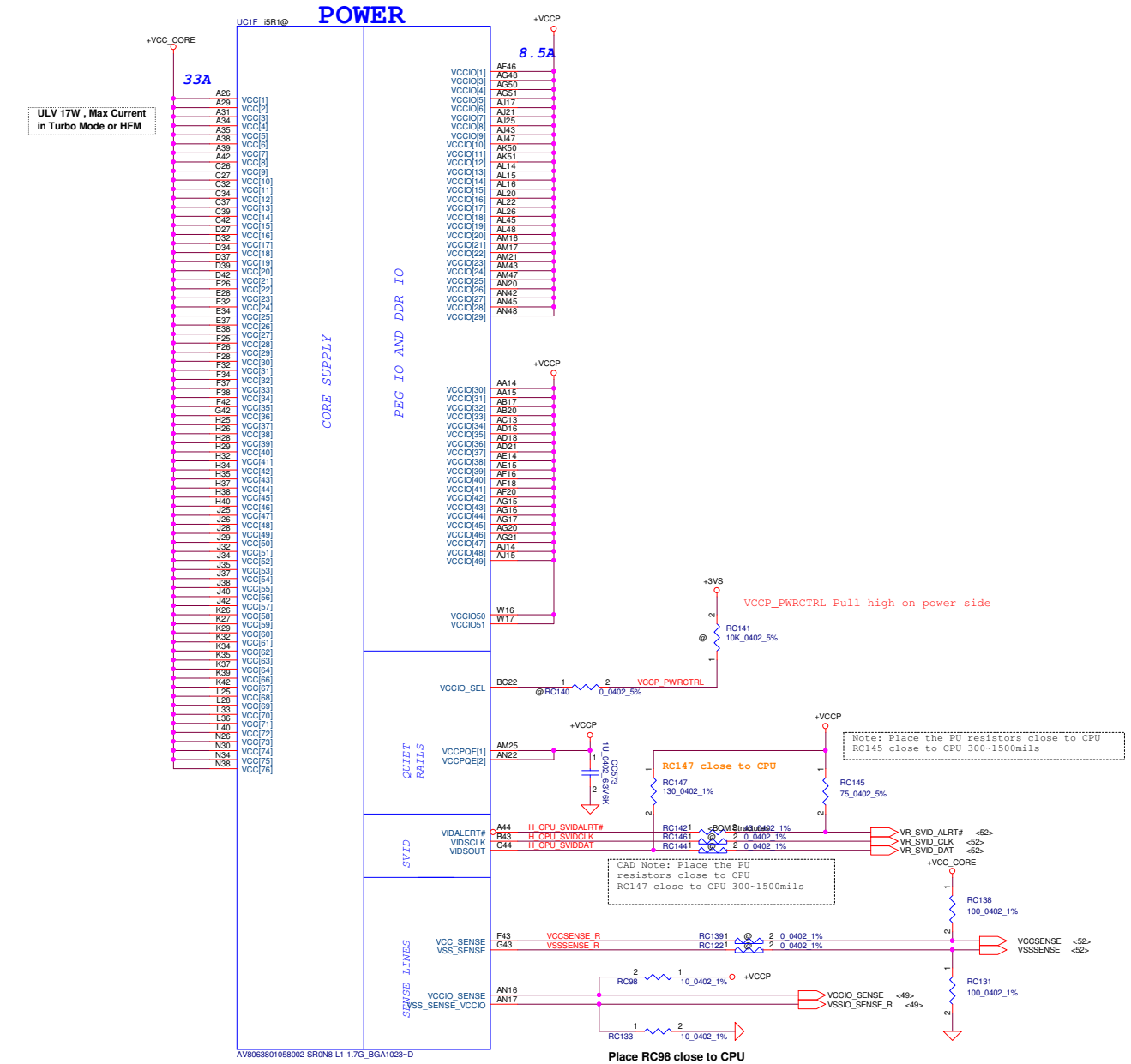
Compal Electronics, Inc.

Title: **PROCESSOR(4/6) RSVD,CFG**

Size | Document Number: **LA-9104P** | Rev: 1.0

Date: Wednesday, August 29, 2012 | Sheet 8 of 57



Place RC98 close to CPU

Iccmax current changed for PDDG Rev0.7

CPU Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	0.65-1.3	53
VCCIO	1.05/1	8.5
VAXG	0.0-1.1	33
VCCPLL	1.8	1.2
VDDQ	1.5	5
VCCSA	0.65-0.9	6
+1.5V_MEM	1.5	12-16 ★

★ Description

5A to Mem controller(+1.5V_CPU_VDDQ)
5-6A to 2 DIMMs/channel
2-5A to +1.5V_RUN & +0.75V_DDR_VTT

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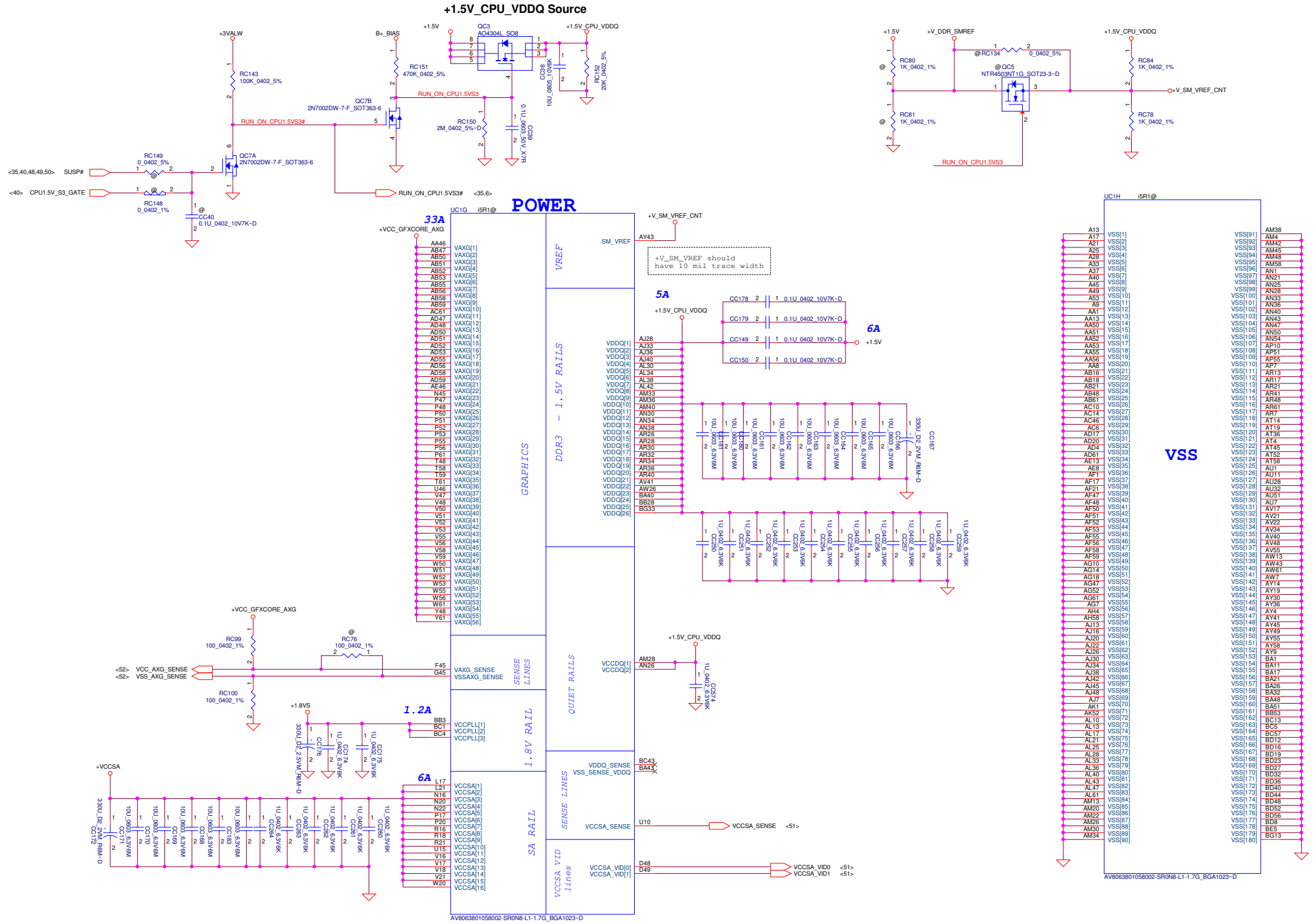
Compal Electronics, Inc.

Title: PROCESSOR(5/6) PWR,BYPASS

Size | Document Number: LA-9104P | Rev 1.0

Date: Wednesday, August 29, 2012 | Sheet 9 of 57



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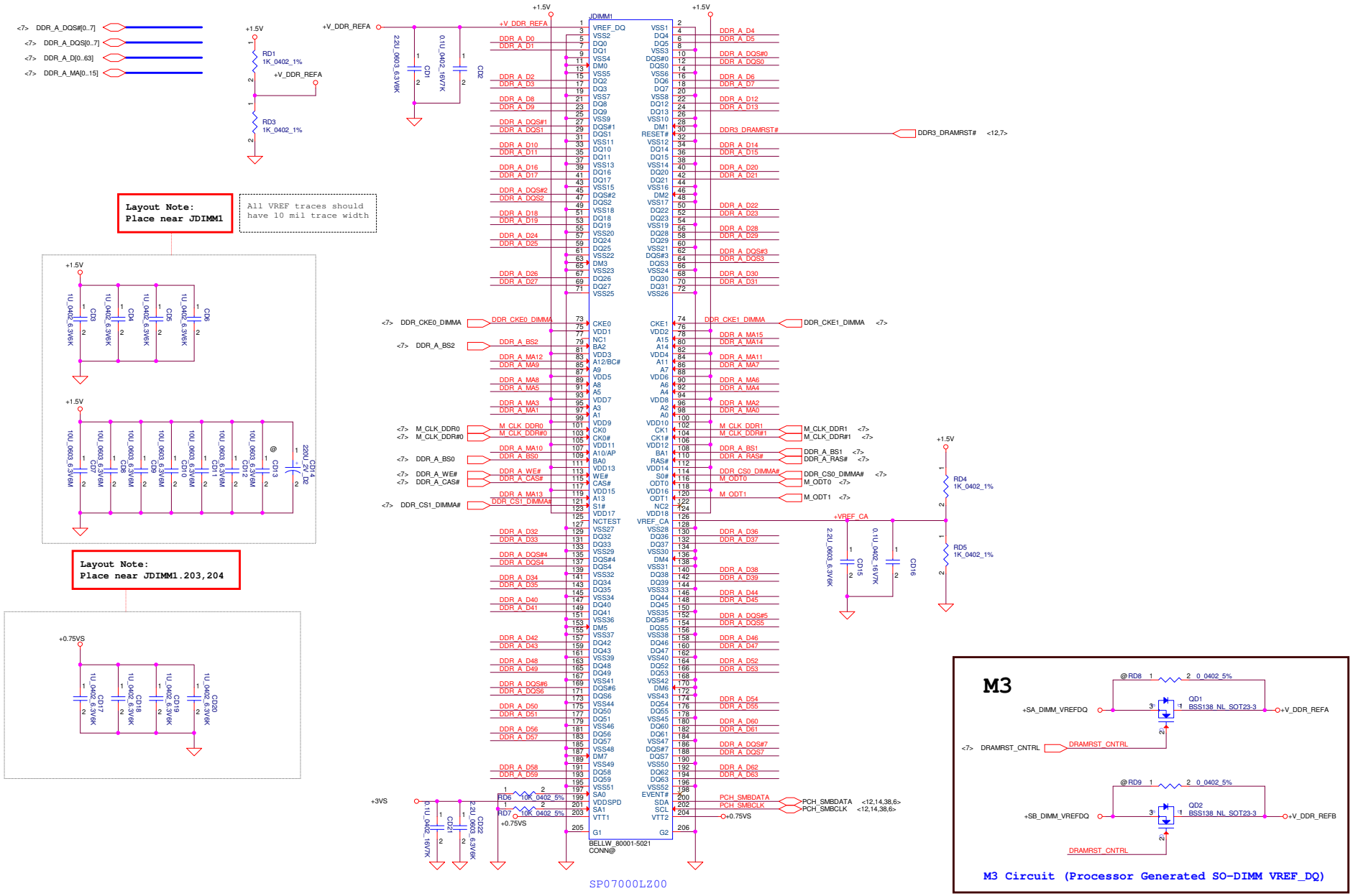
Compal Electronics, Inc.

Title: PROCESSOR(6/6) PWR,VSS

Size | Document Number: LA-9104P | Rev: 1.0

Date: Wednesday, August 29, 2012 | Sheet 10 of 57



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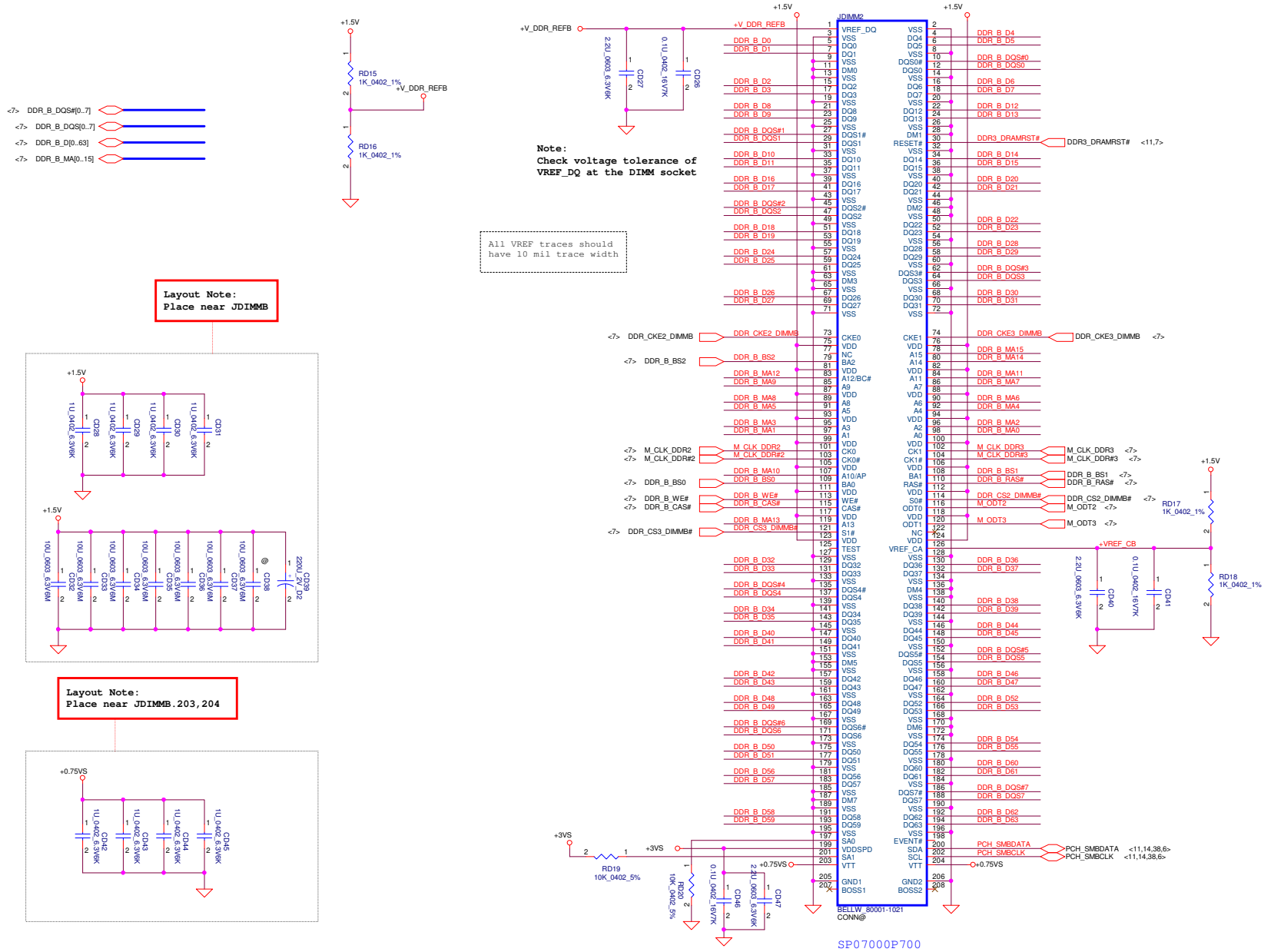
Compal Electronics, Inc.

Title: **DDRIII DIMMA**

Size: | Document Number: **LA-9104P** | Rev: 1.0

Date: Wednesday, August 29, 2012 | Sheet 11 of 57



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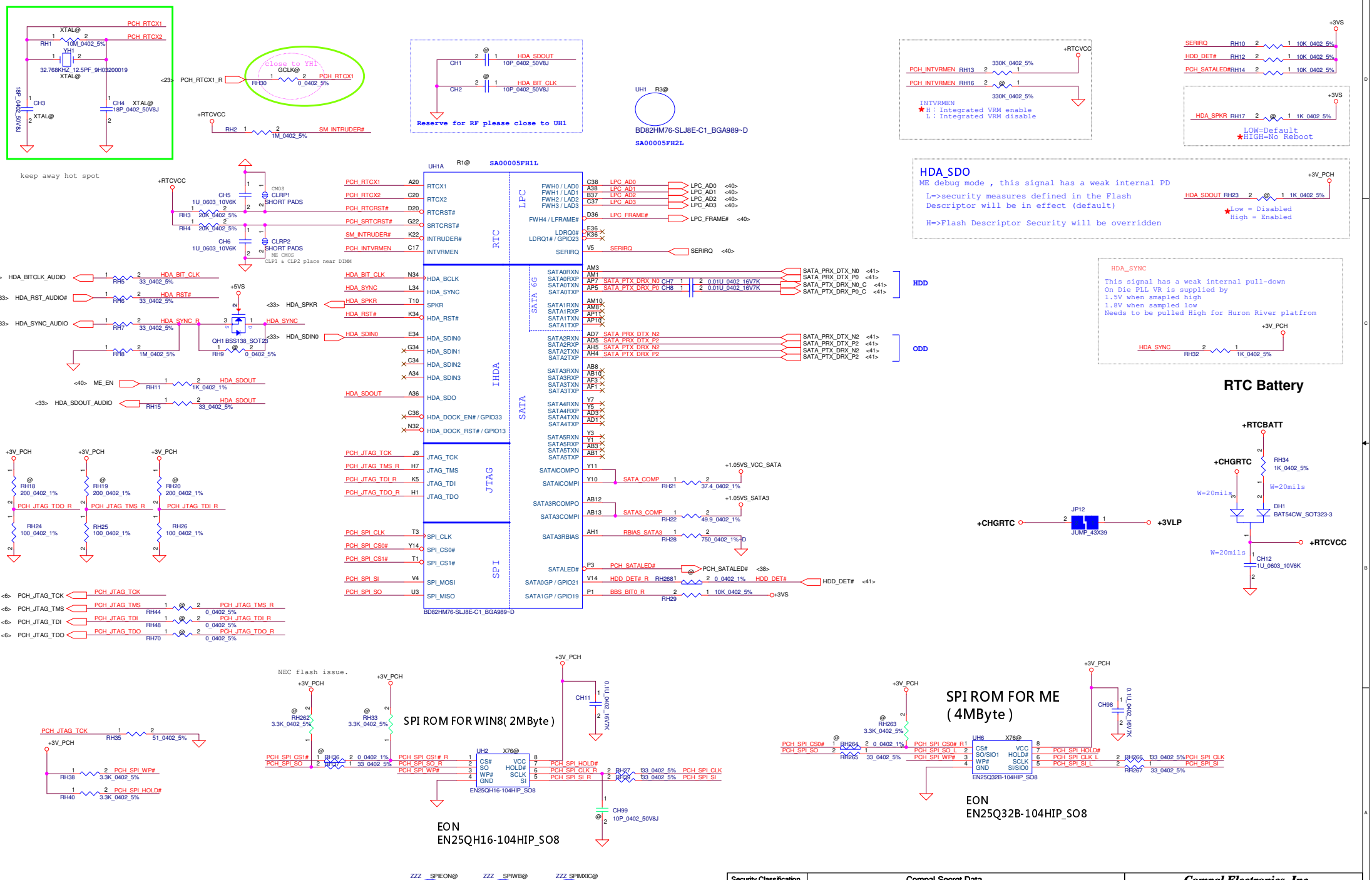
Compal Electronics, Inc.

Title: **DDRIII DIMMB**

Size: | Document Number: **LA-9104P** | Rev: 1.0

Date: Wednesday, August 29, 2012 | Sheet 12 of 57



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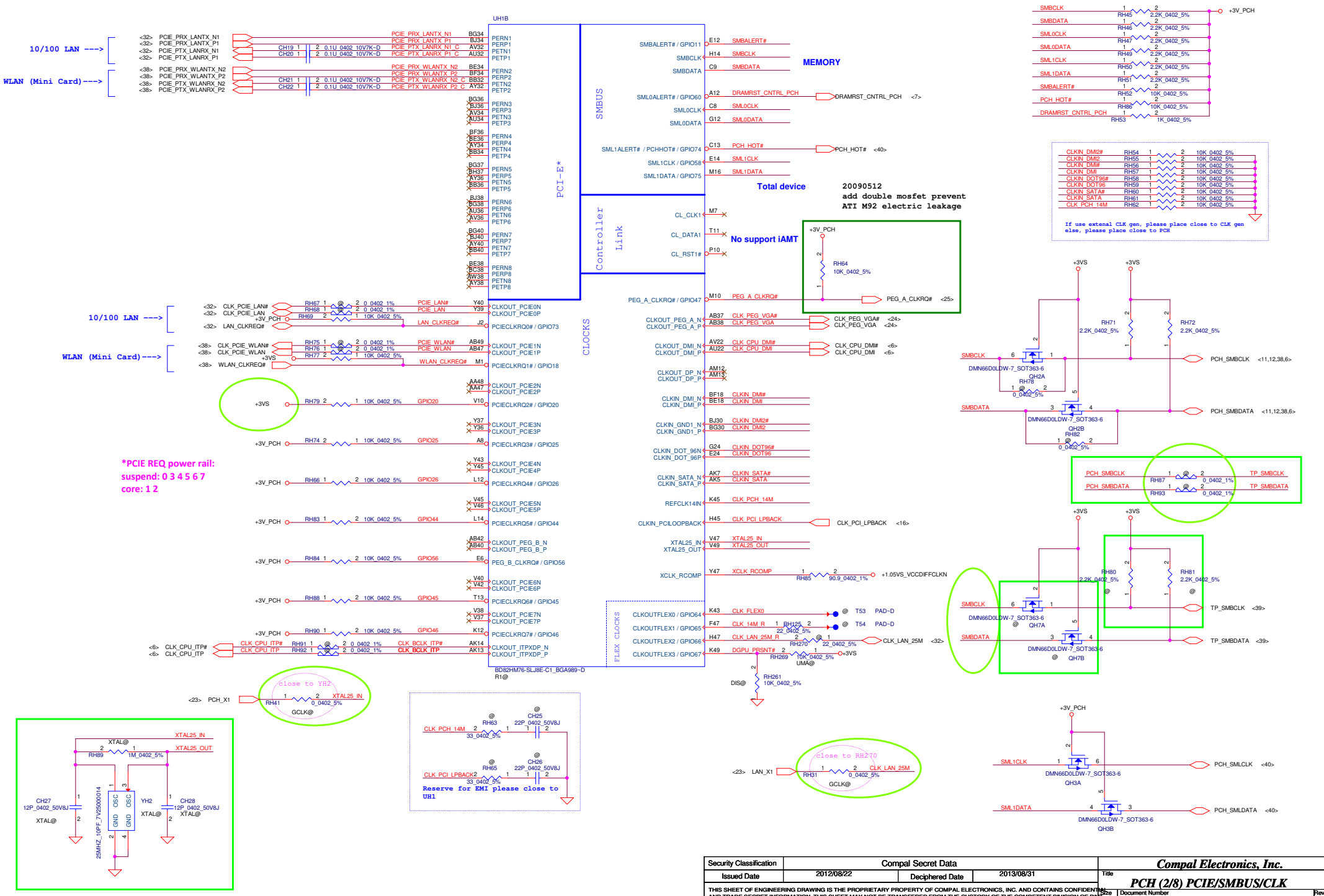
Compal Electronics, Inc.

Title: **PCH (1/8) SATA/HDA/SPI/LPC**

Size: | Document Number: **LA-9104P** | Rev: 1.0

Date: Wednesday, August 29, 2012 | Sheet 13 of 57



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Compal Electronics, Inc.

Title: **PCH (2/8) PCIE/SMBUS/CLK**

Size | Document Number: **LA-9104P** | Rev: 1.0

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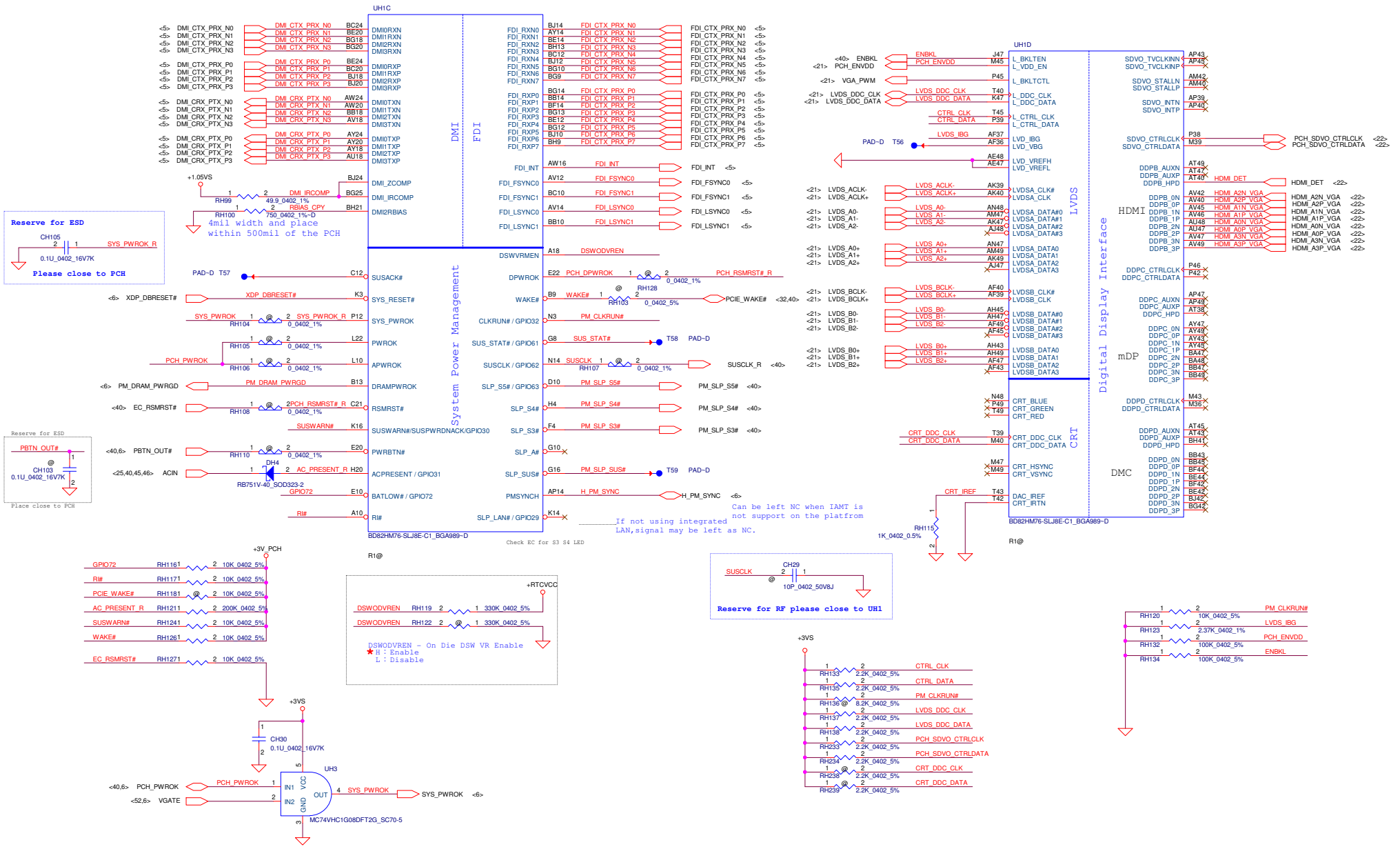

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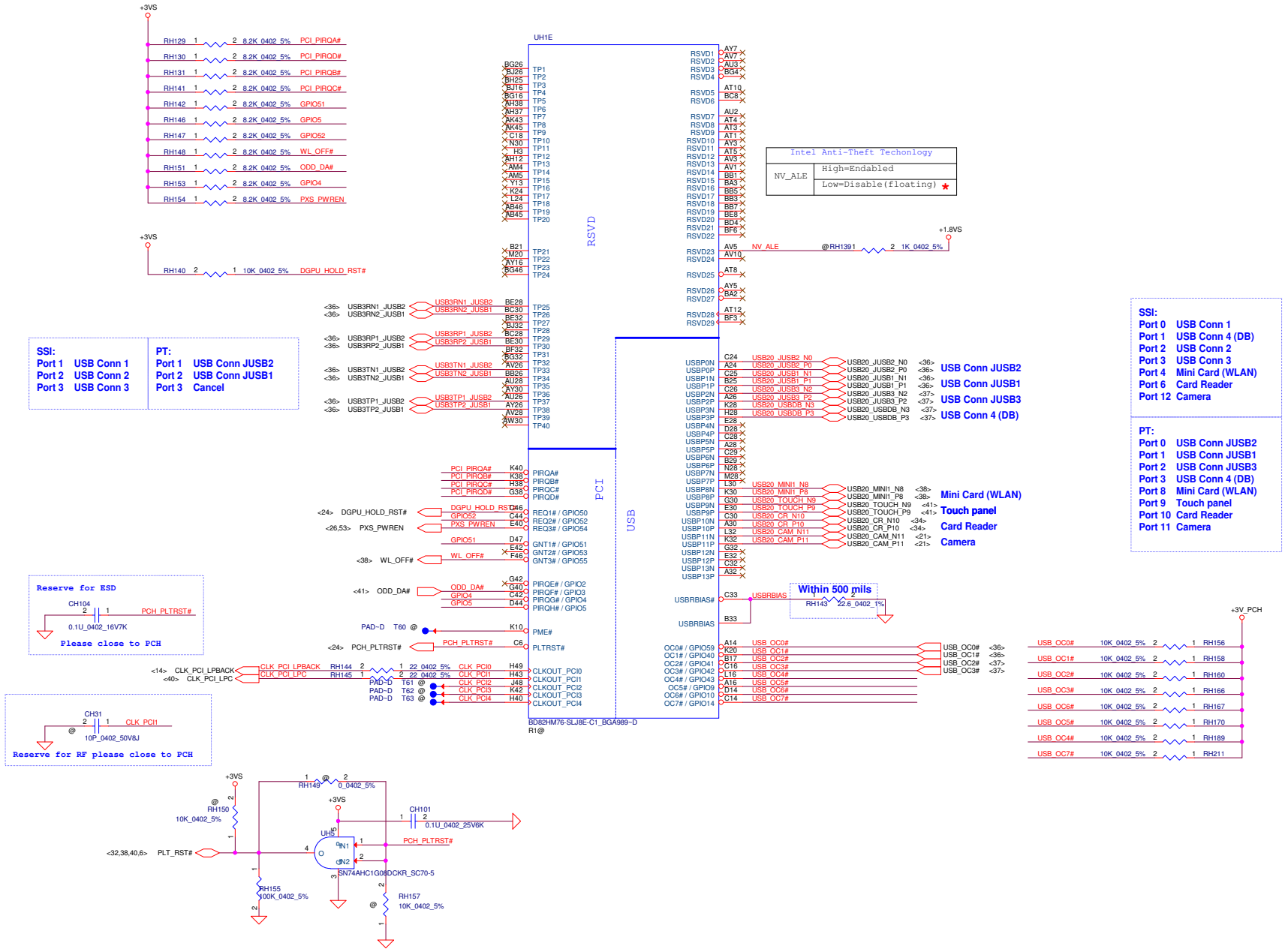
Compal Electronics, Inc.

Title: **PCH (3/8) DMI/FDI/PM/GFX/DP**

Size | Document Number: **LA-9104P** | Rev: 1.0

Date: Wednesday, August 29, 2012 | Sheet 15 of 57



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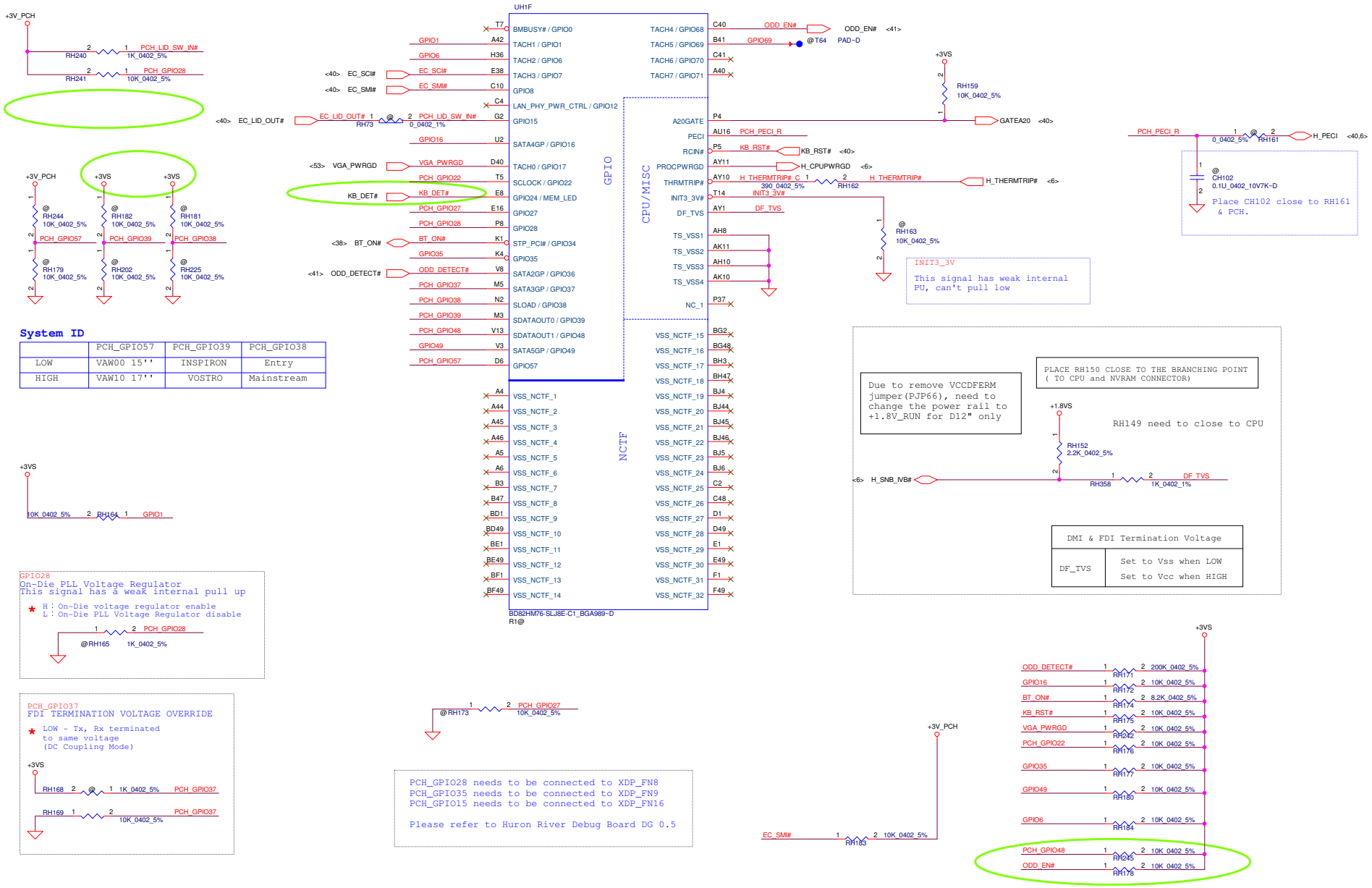
Compal Electronics, Inc.

Title: **PCH (4/8) PCI/USB/NVRAM**

Size | Document Number: **LA-9104P** | Rev: 1.0

Date: Wednesday, August 29, 2012 | Sheet 16 of 57



System ID

	PCH_GPIO57	PCH_GPIO39	PCH_GPIO38
LOW	VAW00 15''	INSPIRON	Entry
HIGH	VAW10 17''	VOSTRO	Mainstream

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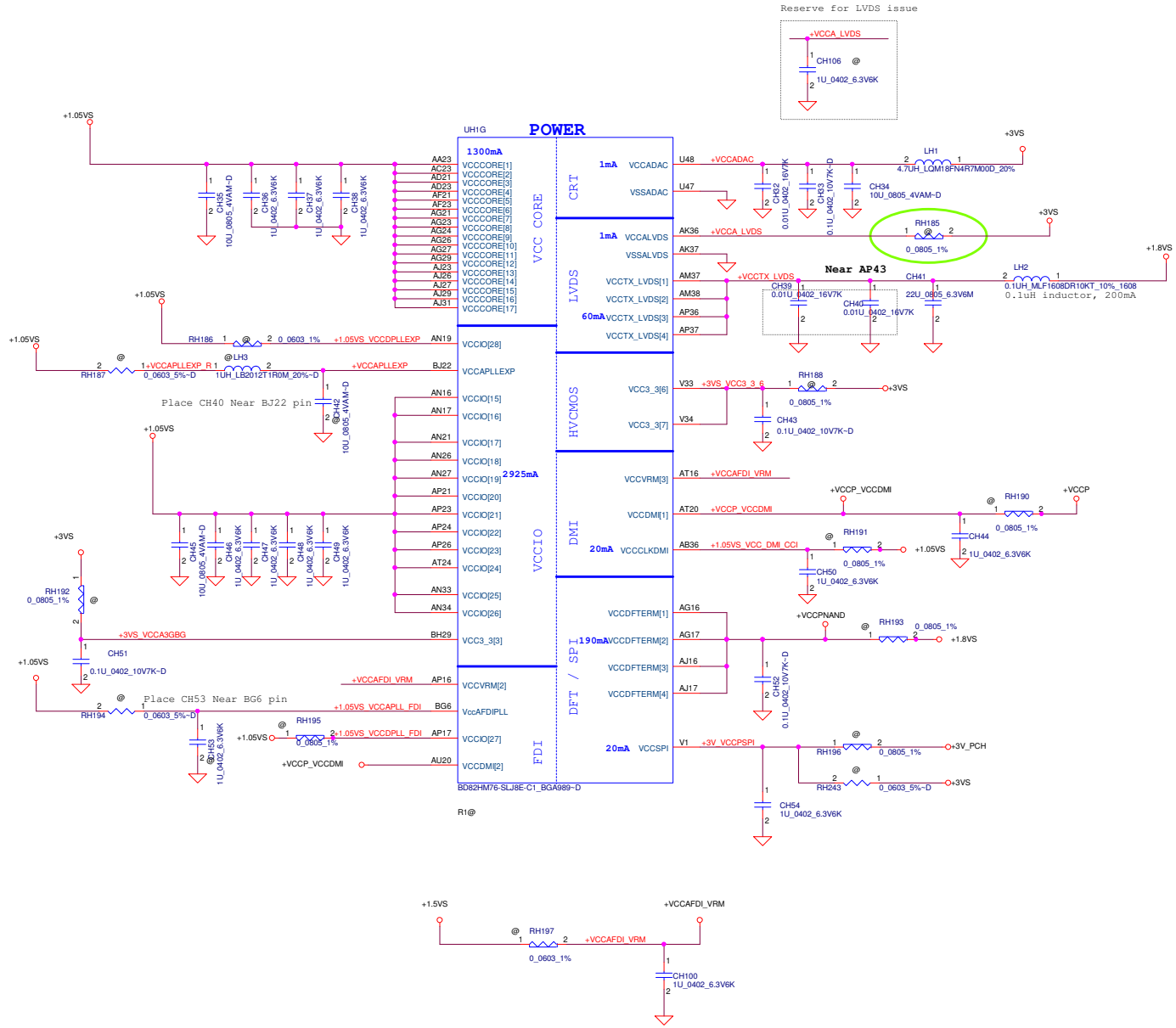
Compal Electronics, Inc.

Title: **PCH (5/8) GPIO/CPU/MISC**

Size | Document Number: **LA-9104P** | Rev: 1.0

Date: Wednesday, August 29, 2012 | Sheet 17 of 57



PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

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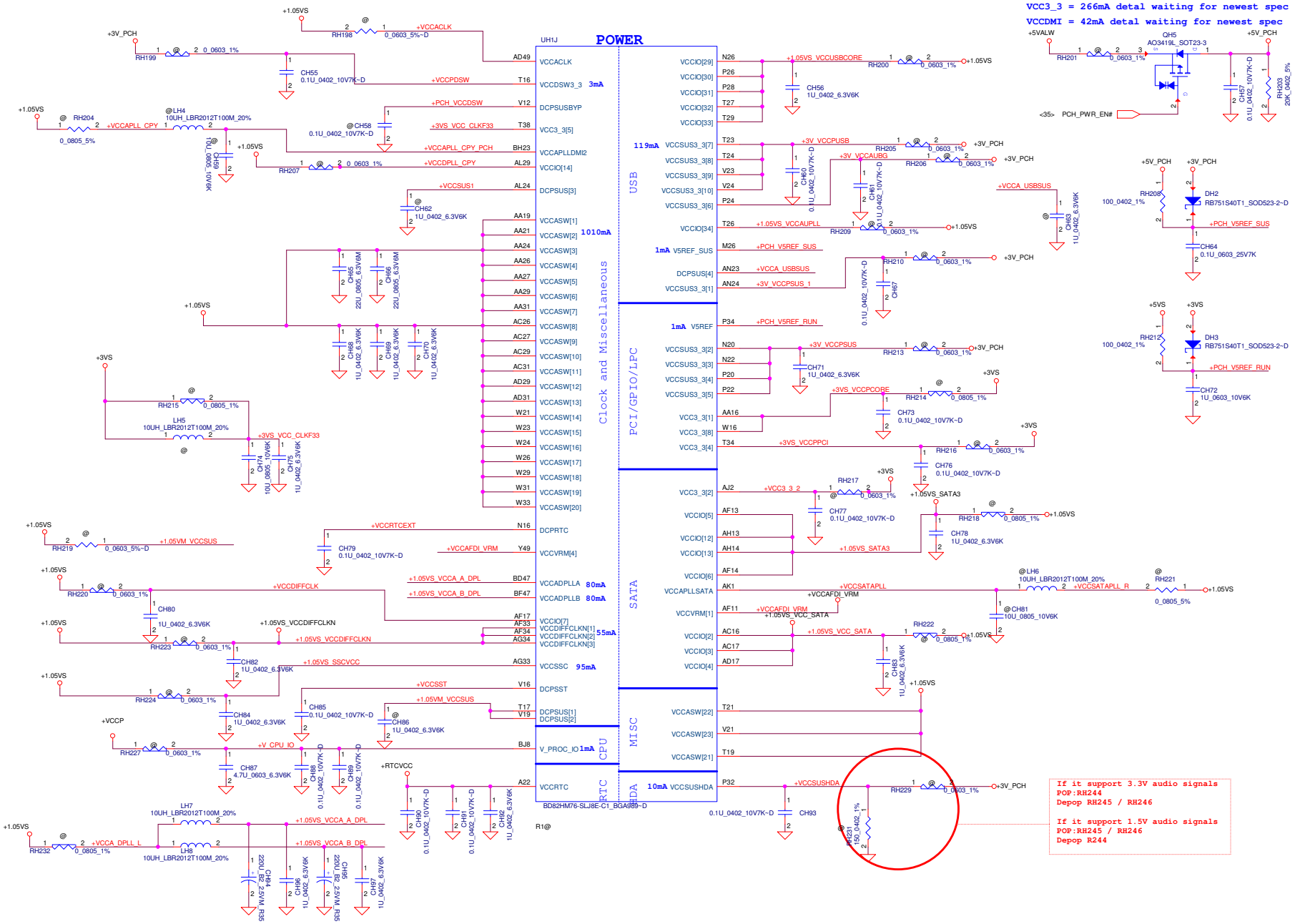
Compal Electronics, Inc.

Title: **PCH (6/8) PWR**

Size: | Document Number: **LA-9104P** | Rev: 1.0

Date: Wednesday, August 29, 2012 | Sheet 18 of 57



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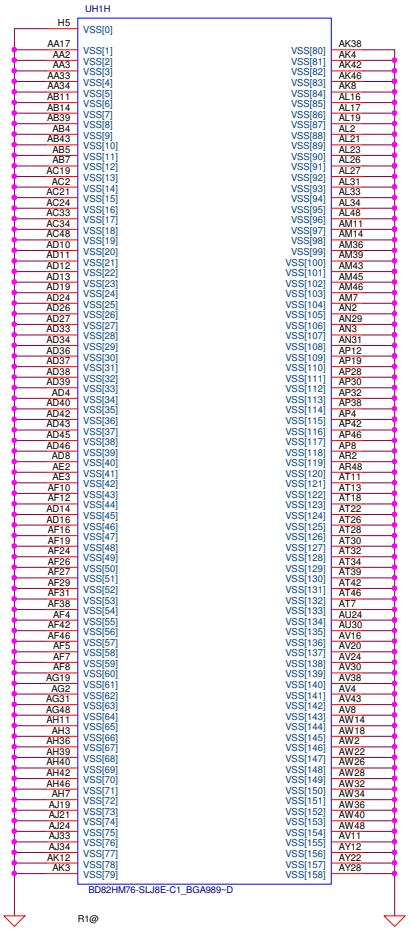
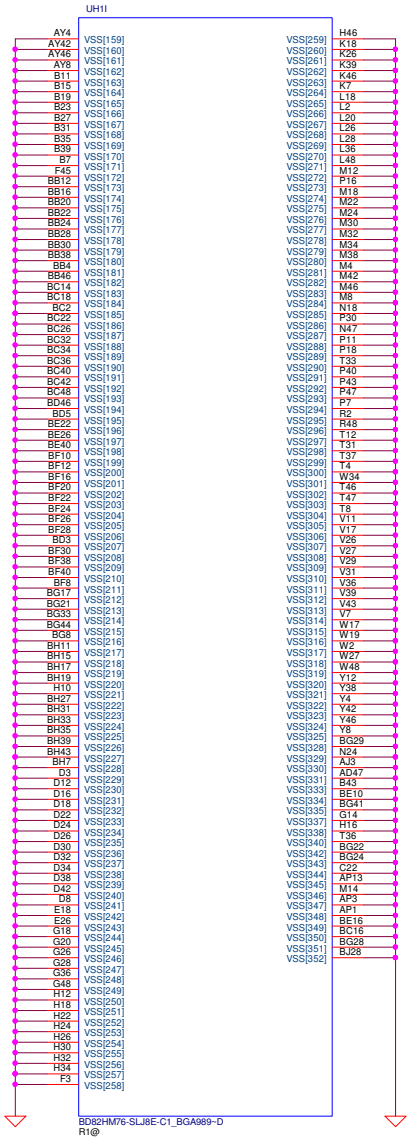
Compal Electronics, Inc.

Title: **PCH (7/8) PWR**

Size | Document Number: **LA-9104P** | Rev: 1.0

Date: Wednesday, August 29, 2012 | Sheet 19 of 57





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Issued Date	2012/08/22	Deciphered Date	2013/08/31	Title: PCH (8/8) VSS
				Size: Document Number: LA-9104P — Rev: 1.0
				Date: Wednesday, August 29, 2012 — Sheet 20 of 57

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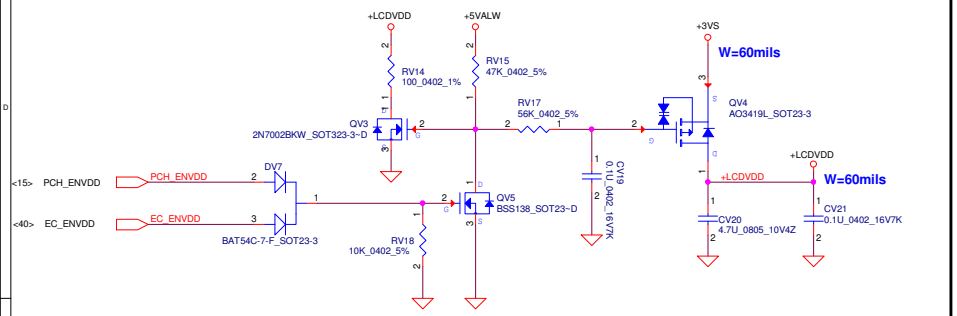
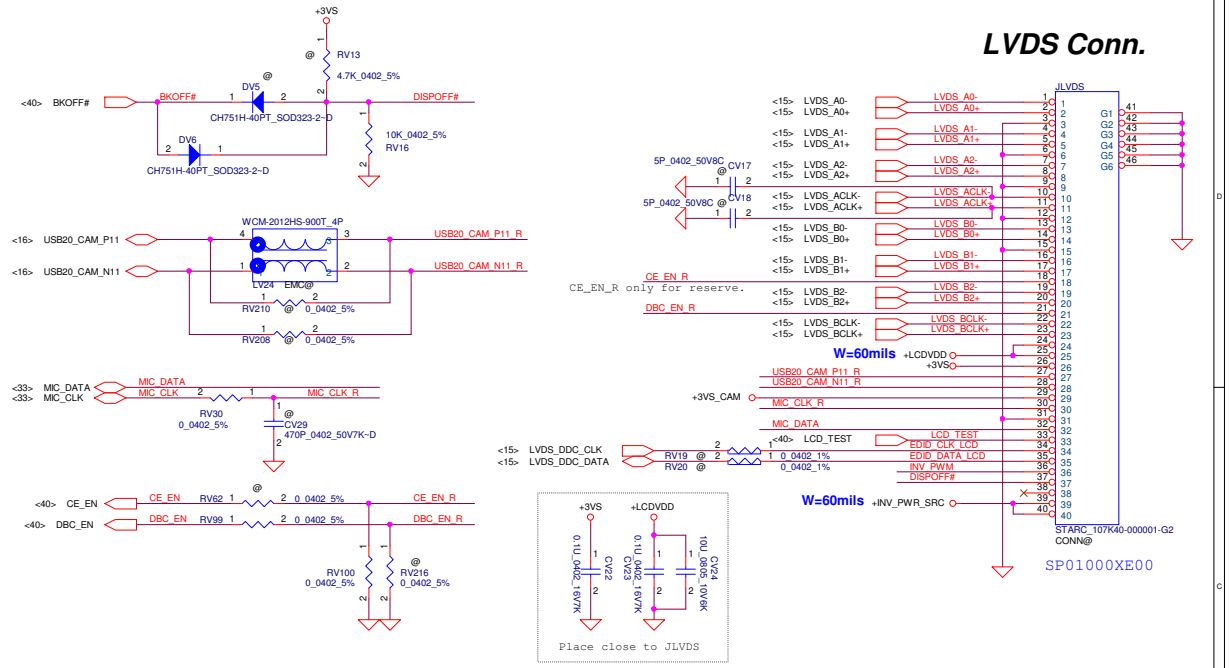
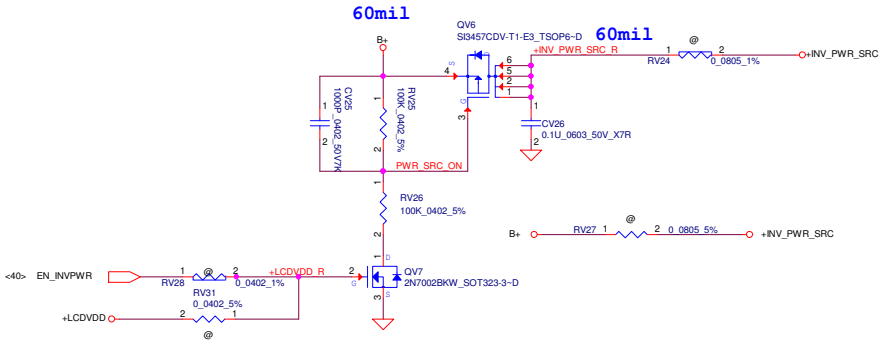
LCD PWR CTRL



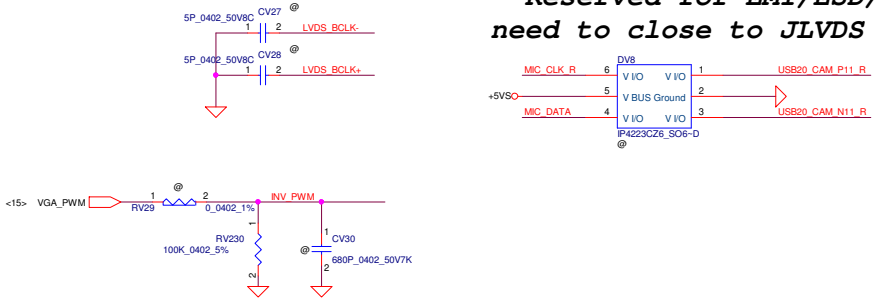
LVDS Conn.



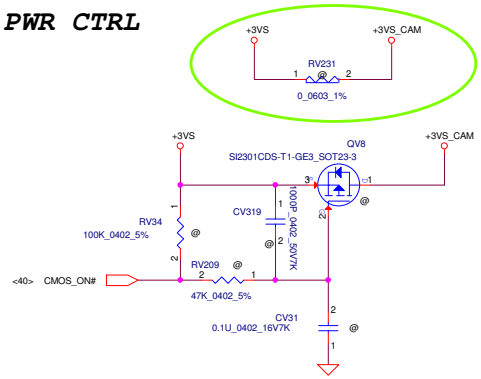
LCD backlight PWR CTRL



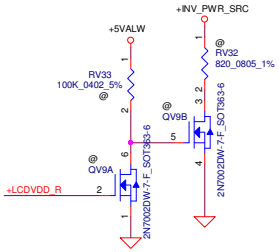
* Reserved for EMI/ESD/RF need to close to JLVDS



Webcam PWR CTRL



* Reserved for LCD sequence tuning



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Compal Electronics, Inc.

Title: LVDS/webcam

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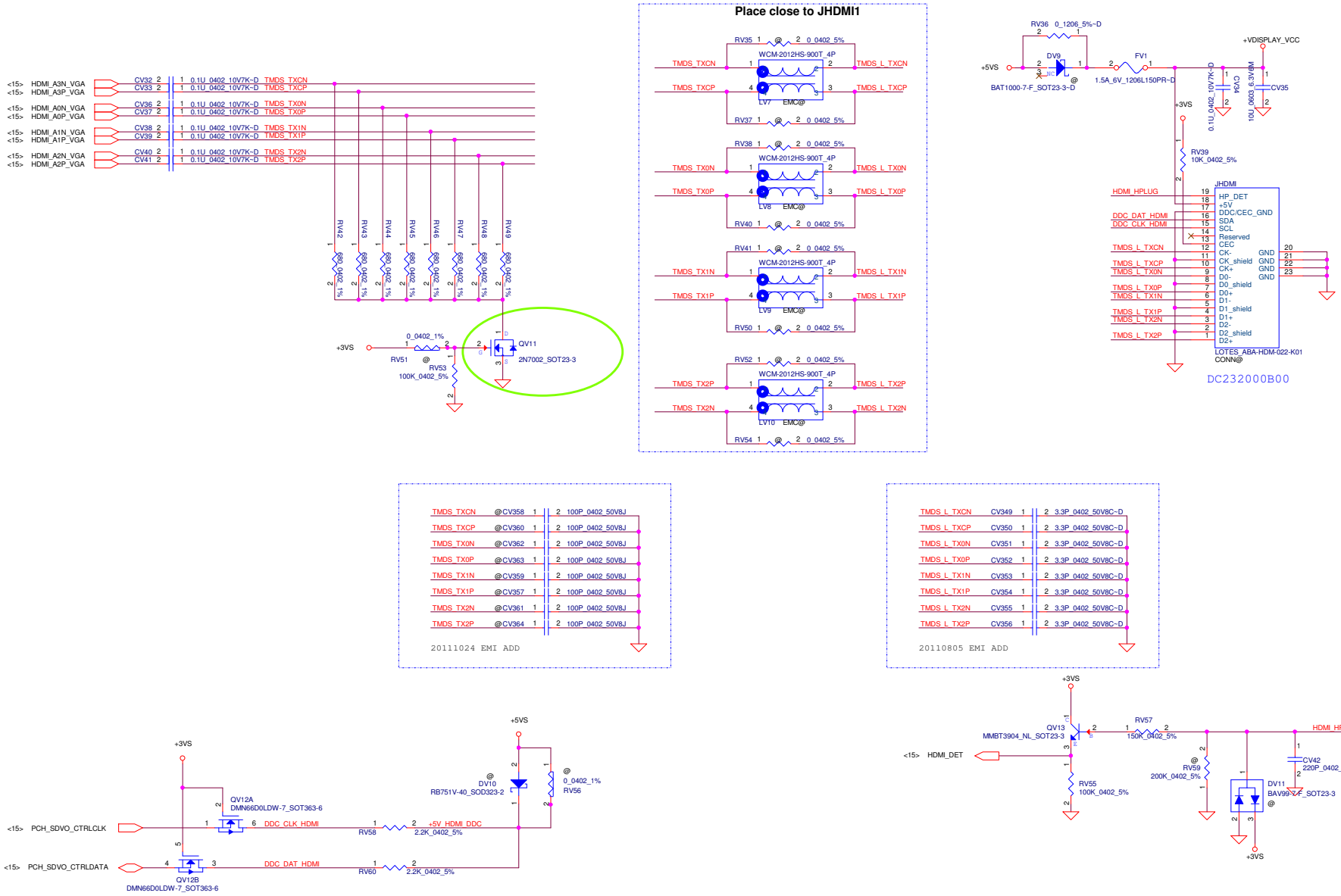
W=40mils



46@ ROYALTY HDMI W/LOGO

Part Number	Description
RO00000002HM	HDMI W/Logo:RO00000002HM

Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

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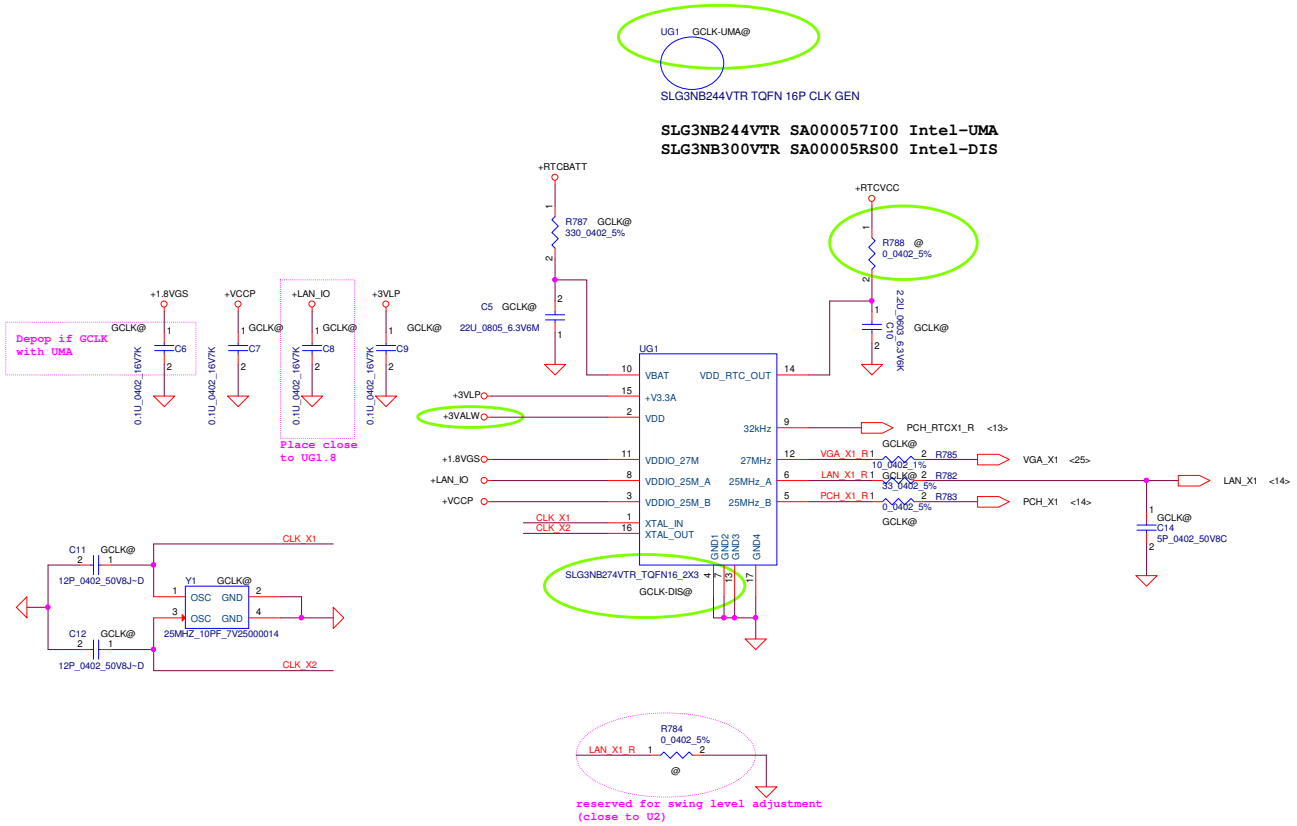
Compal Electronics, Inc.

Title: **HDMI**

Size | Document Number: **LA-9104P** | Rev: 1.0

Date: Wednesday, August 29, 2012 | Sheet 22 of 57



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Compal Electronics, Inc.

Title: **GCLK**

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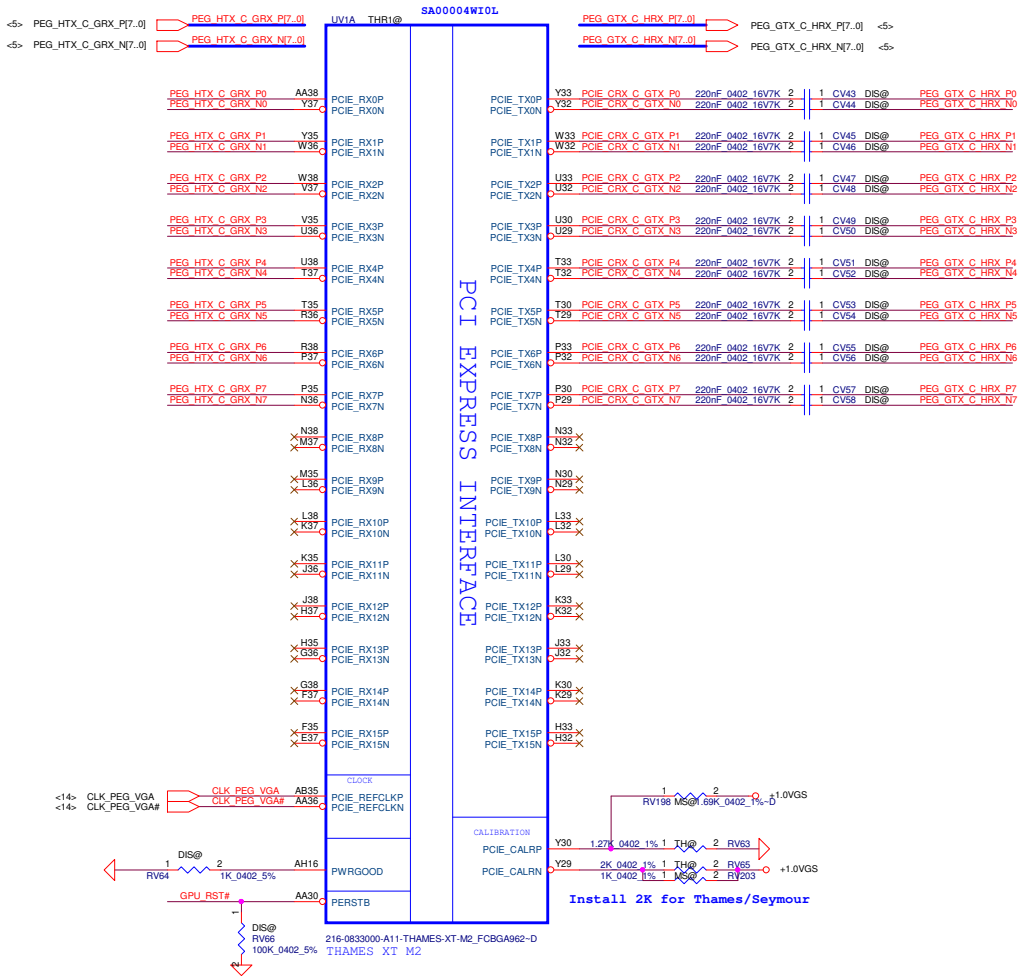
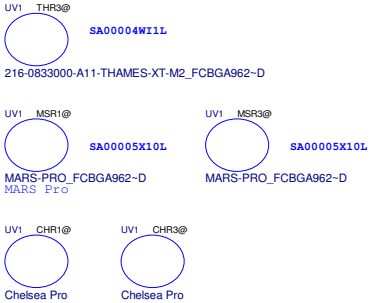
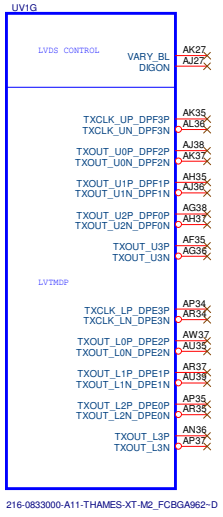
GFX PCIE LANE REVERSAL

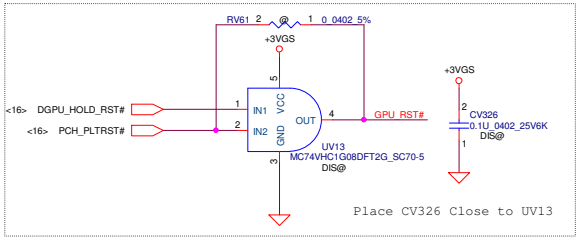


Install 2K for Thames/Seymour



LVDS Interface





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				Date: Wednesday, August 29, 2012 — Sheet 24 of 57

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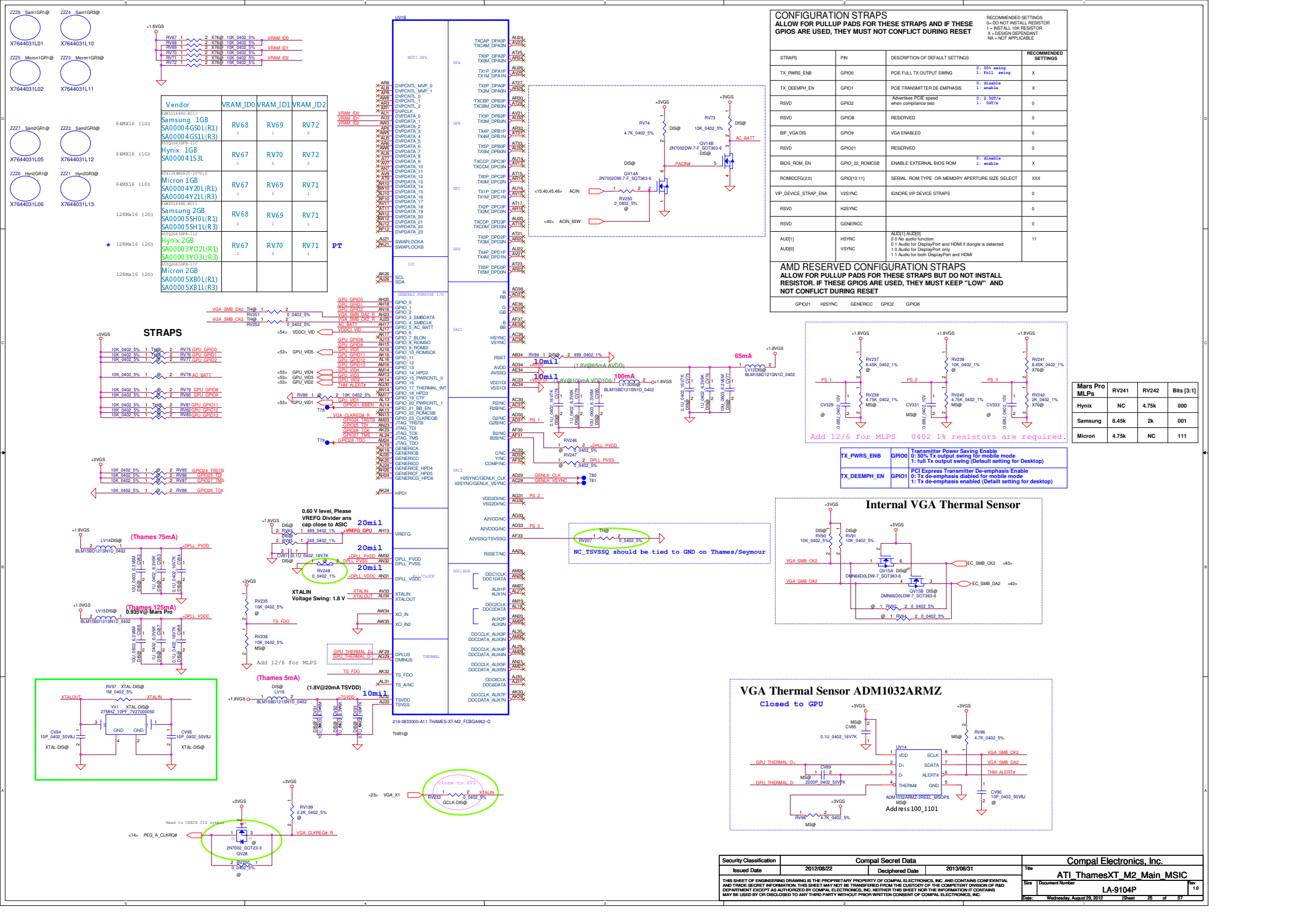
CONFIGURATION STRAPS
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET
RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE
STRAPS | PIN | DESCRIPTION OF DEFAULT SETTINGS | RECOMMENDED SETTINGS
TX_PWRS_ENB | GPIO0 | PCIE FULL TX OUTPUT SWING 0: 50% swing 1: Full swing | X
TX_DEEMPH_EN | GPIO1 | PCIE TRANSMITTER DE-EMPHASIS 0: disable 1: enable | X
RSVD | GPIO2 | Advertises PCIE speed when compliance test 0: 2.5GT/s 1: 5GT/s | 0
RSVD | GPIO8 | RESERVED | 0
BIF_VGA DIS | GPIO9 | VGA ENABLED | 0
RSVD | GPIO21 | RESERVED | 0
BIOS_ROM_EN | GPIO_22_ROMCSB | ENABLE EXTERNAL BIOS ROM 0: disable 1: enable | X
ROMIDCFG(2:0) | GPIO[13:11] | SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT | XXX
VIP_DEVICE_STRAP_ENA | V2SYNC | IGNORE VIP DEVICE STRAPS | 0
RSVD | H2SYNC | | 0
RSVD | GENERICC | | 0
AUD[1] AUD[0] | HSYNC VSYNC | AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI | 11
AMD RESERVED CONFIGURATION STRAPS
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET
GPIO21 H2SYNC GENERICC GPIO2 GPIO8
Vendor | VRAM_ID0 | VRAM_ID1 | VRAM_ID2
Samsung 1GB SA00004G50L(R1) SA00004G51L(R3) | RV68 0 | RV69 1 | RV72 0
Hynix 1GB SA000041S3L | RV67 1 | RV70 0 | RV72 0
Micron 1GB SA00004Y20L(R1) SA00004Y21L(R3) | RV67 1 | RV69 1 | RV71 1
Samsung 2GB SA00005SH0L(R1) SA00005SH1L(R3) | RV68 0 | RV69 1 | RV71 1
Hynix 2GB SA00003YO2L(R1) SA00003YO3L(R3) | RV67 1 | RV70 0 | RV71 1
Micron 2GB SA00005XB0L(R1) SA00005XB1L(R3) | | | |
64MX16 (1G)
128Mx16 (2G)
PT
STRAPS
Add 12/6 for MLPS 0402 1% resistors are required.
Mars Pro MLPs | RV241 | RV242 | Bits [3:1]
Hynix | NC | 4.75k | 000
Samsung | 8.45k | 2k | 001
Micron | 4.75k | NC | 111
TX_PWRS_ENB | GPIO0 | Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN | GPIO1 | PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Defailt setting for desktop)
Internal VGA Thermal Sensor
VGA Thermal Sensor ADM1032ARMZ
Closed to GPU
Address:100_1101
NC_TSVSSQ should be tied to GND on Thames/Seymour
0.60 V level, Please VREFG Divider ans cap close to ASIC
XTALIN Voltage Swing: 1.8 V
(Thames 75mA)
(Thames 125mA)
0.935V@ Mars Pro
(Thames 5mA)
(1.8V@20mA TSVDD)
Add 12/6 for MLPS
Need to CHECK CIS symbol
Security Classification | Compal Secret Data
Issued Date 2012/08/22 | Deciphered Date 2013/08/31
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ATI_ThamesXT_M2_Main_MSIC
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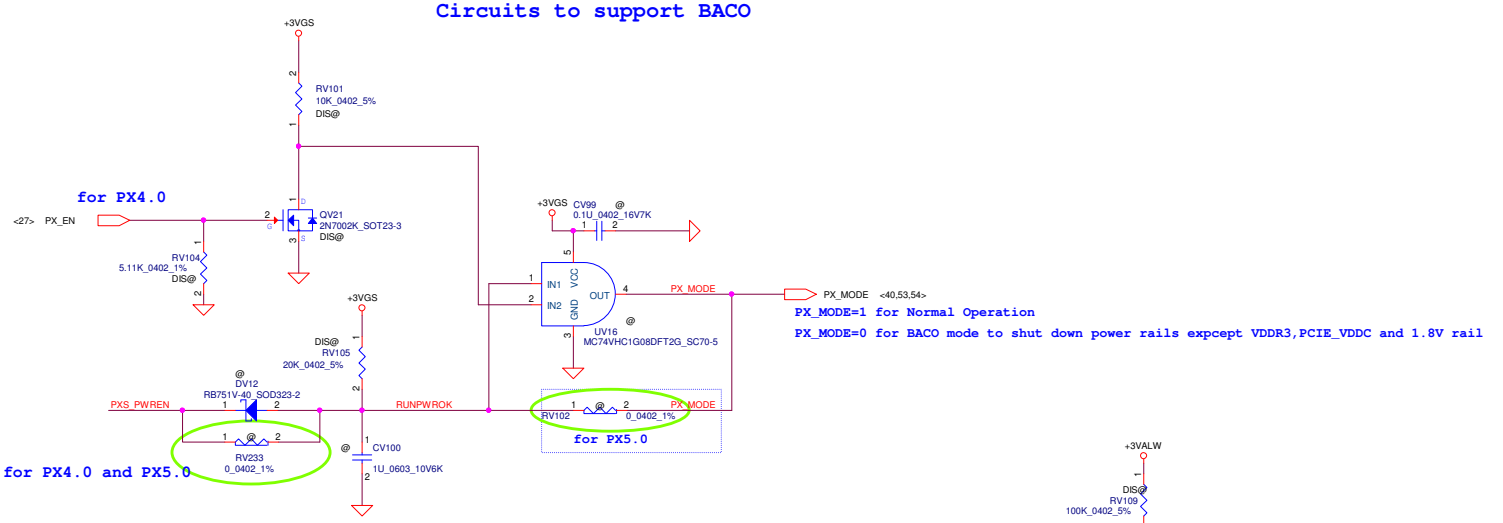
Circuits to support BACO

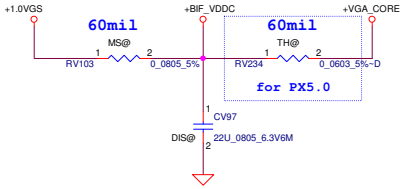
Switch circuits in BACO desingns for Thanes/Seymour only

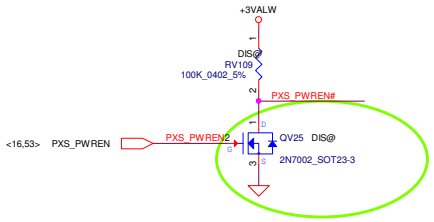
55mA@1.0V, in BACO mode



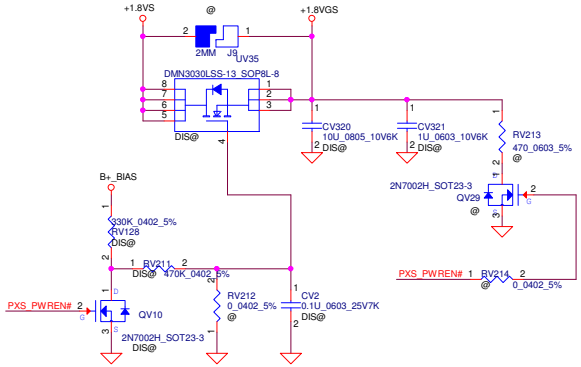
PX_MODE=1 for Normal Operation

PX_MODE=0 for BACO mode to shut down power rails expcept VDDR3,PCIE_VDDC and 1.8V rail

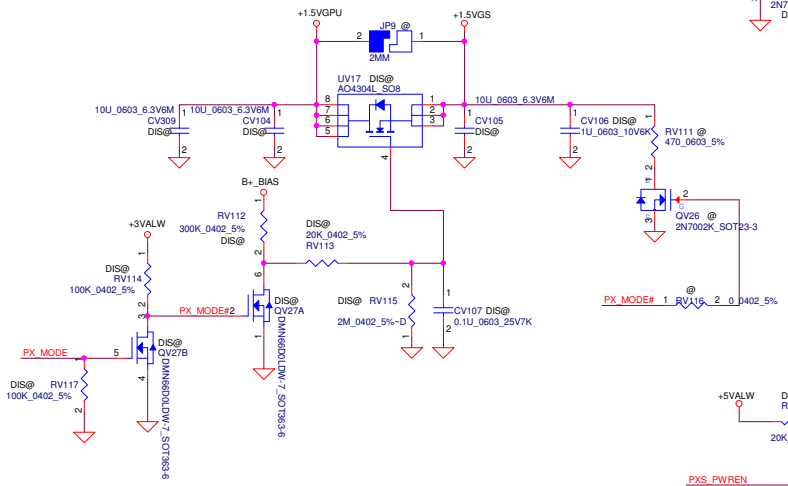




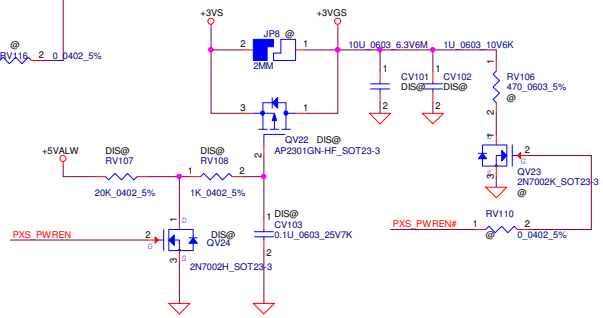
+1.8VS TO +1.8VGS



+1.5VGPU TO +1.5VGS



+3.3VS TO +3.3VGS



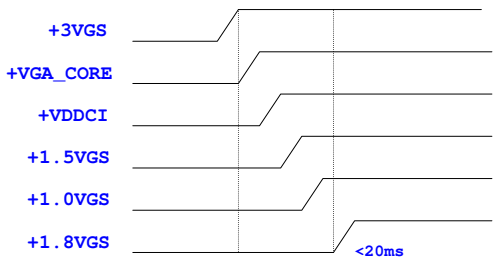
Note:

PX4.0 +VGA_CORE,VDDCI,+1.5VGS ON

PX4.0 +3VGS, +1.0VGS,+1.8VGS OFF

PX5.0 +3VGS,+VGA_CORE,VDDCI,+1.5VGV,+1.0VGS,+1.8VGS OFF

Power Seguence of Thames and Mars Pro



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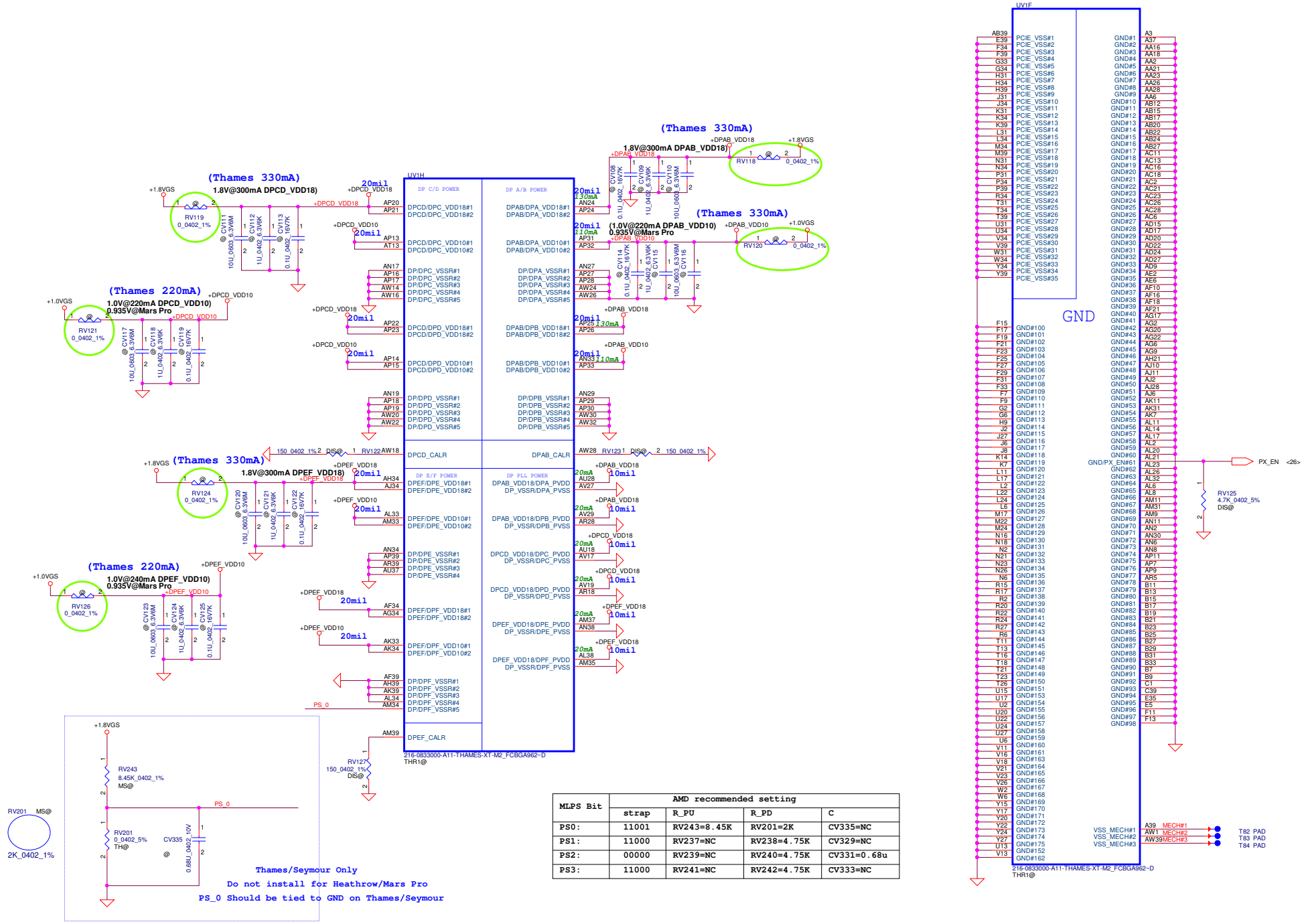

MLPS Bit	AMD recommended setting			
	strap	R_PU	R_PD	C
PS0:	11001	RV243=8.45K	RV201=2K	CV335=NC
PS1:	11000	RV237=NC	RV238=4.75K	CV329=NC
PS2:	00000	RV239=NC	RV240=4.75K	CV331=0.68u
PS3:	11000	RV241=NC	RV242=4.75K	CV333=NC

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Title: ATI_ThamesXT_M2_PWR_GND

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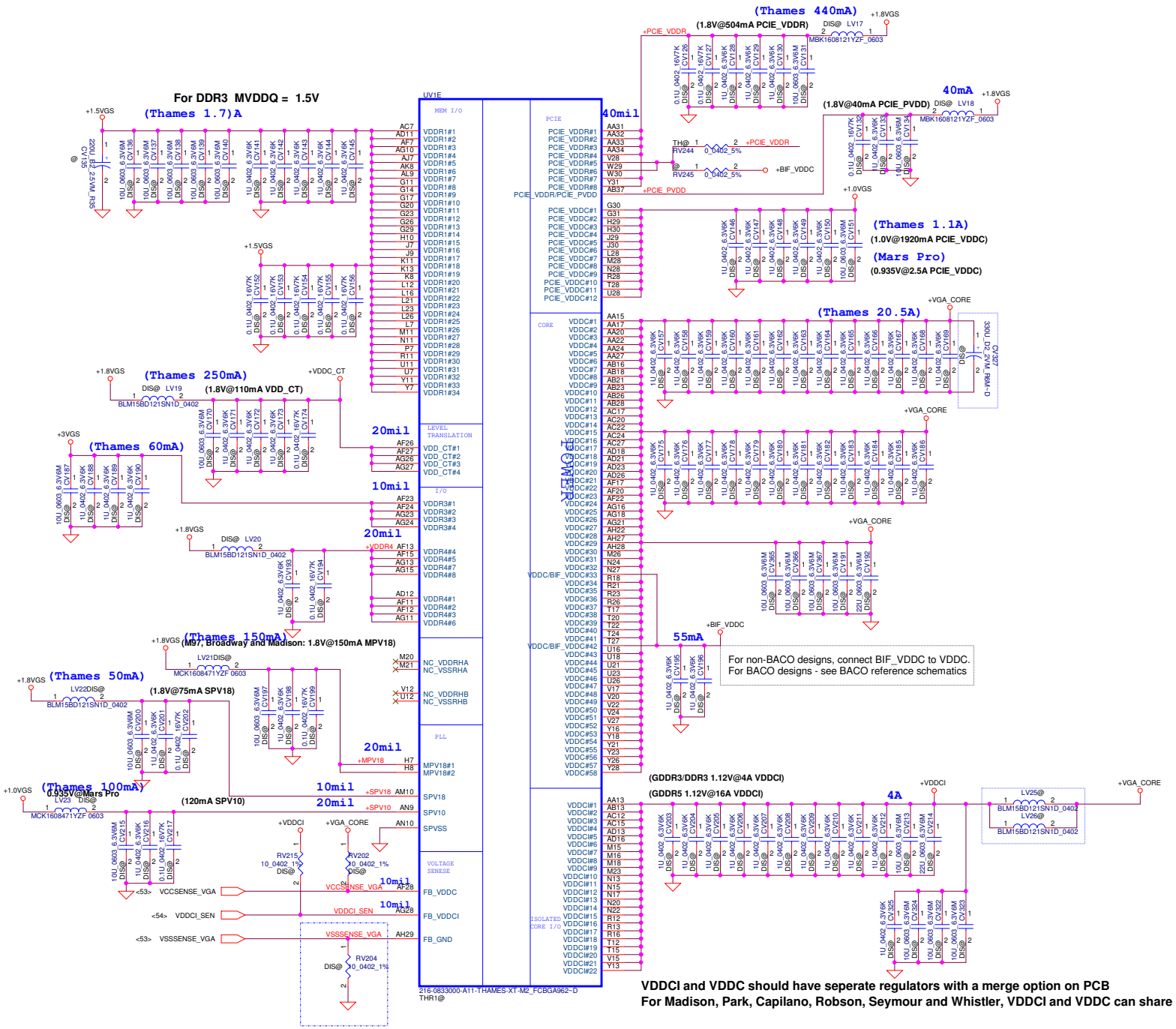

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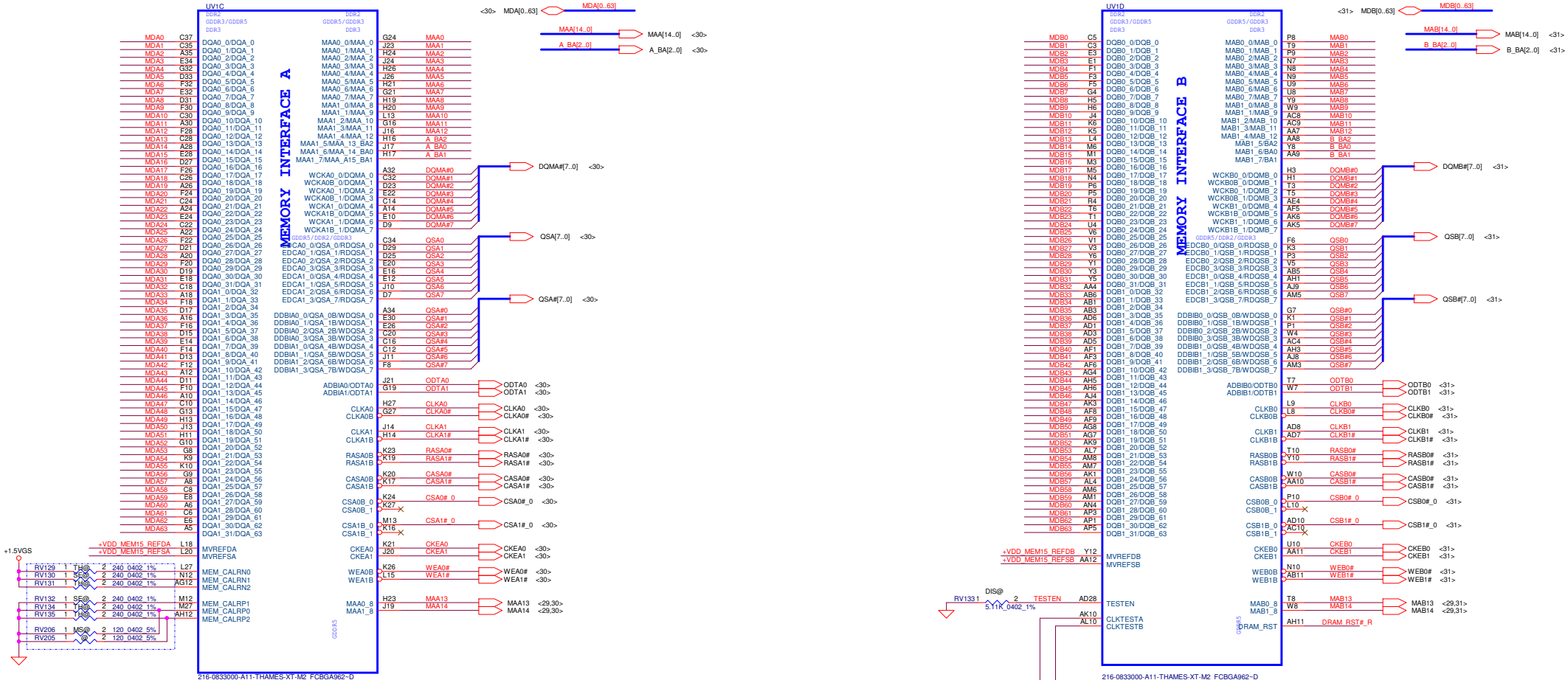

Co-lay Thames/Seymour/Mars Pro

	Thames M2	Seymour M2	Mars Pro
RV129	TH@	@	@
RV130	@	SE@	@
RV131	TH@	@	@
RV132	@	SE@	@
RV134	TH@	@	@
RV135	TH@	@	@
RV206	@	@	MS@
RV205	@	@	@

This basic topology should be used for DRAM_RST for DDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.
Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

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Title: ATI_ThamesXT_M2_MEM IF

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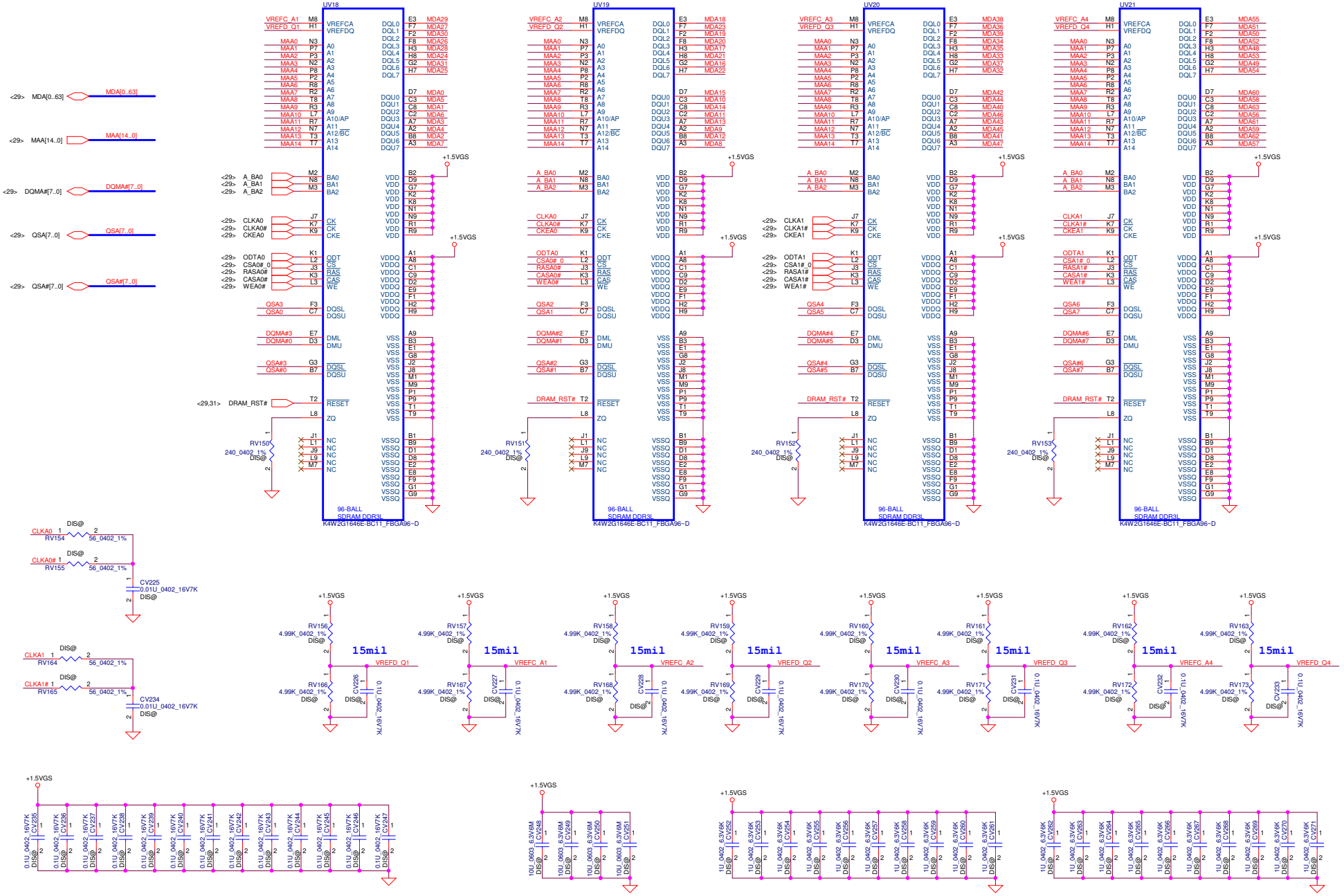
CHANNEL A: 256MB/512MB DDR3



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Title: ATI_ThamesXT_M2_VRAM_A

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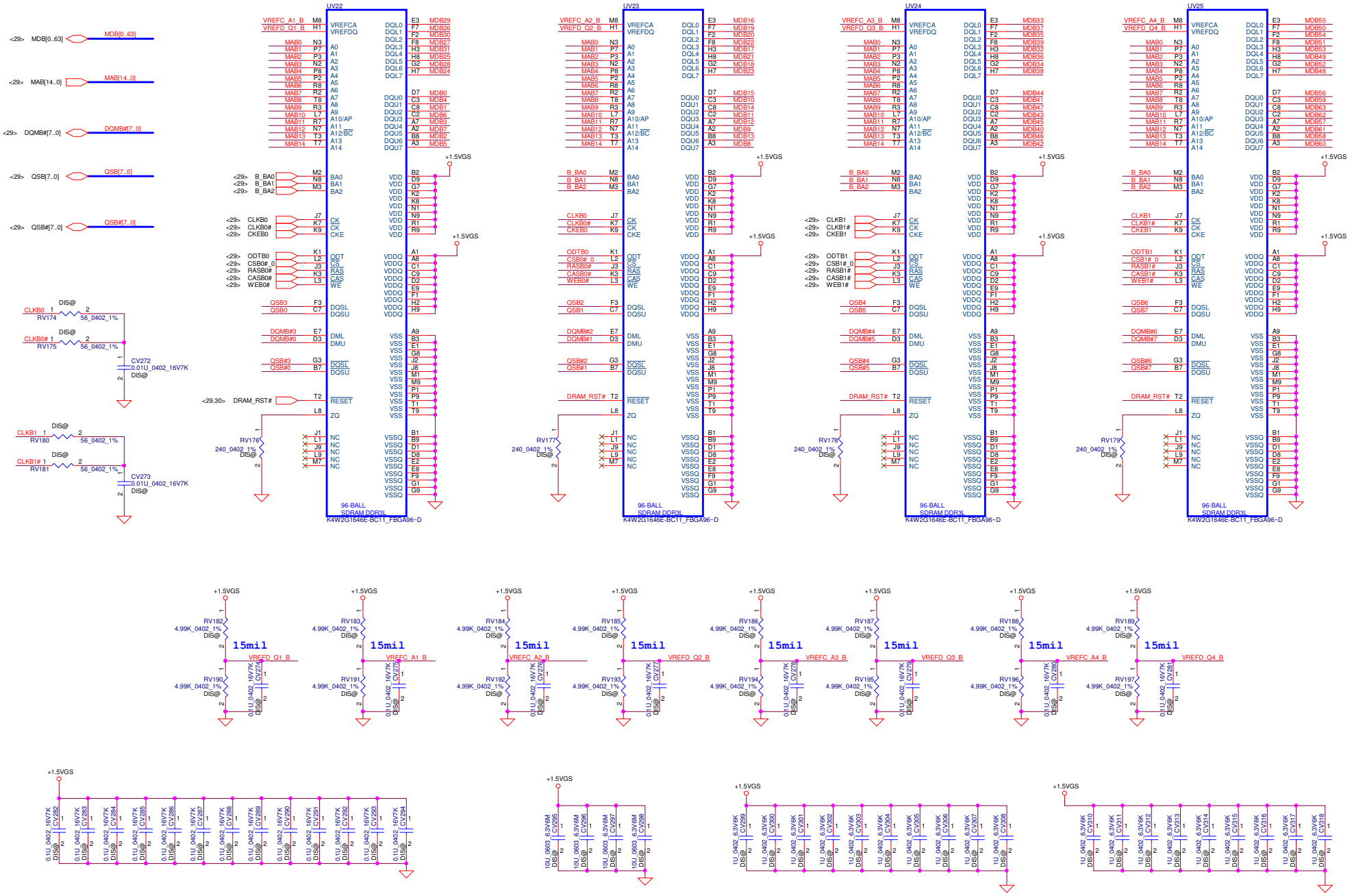
CHANNEL B: 256MB/512MB DDR3



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Compal Electronics, Inc.

Title: ATI_ThamesXT_M2_VRAM_B

Size | Document Number: LA-9104P | Rev: 1.0

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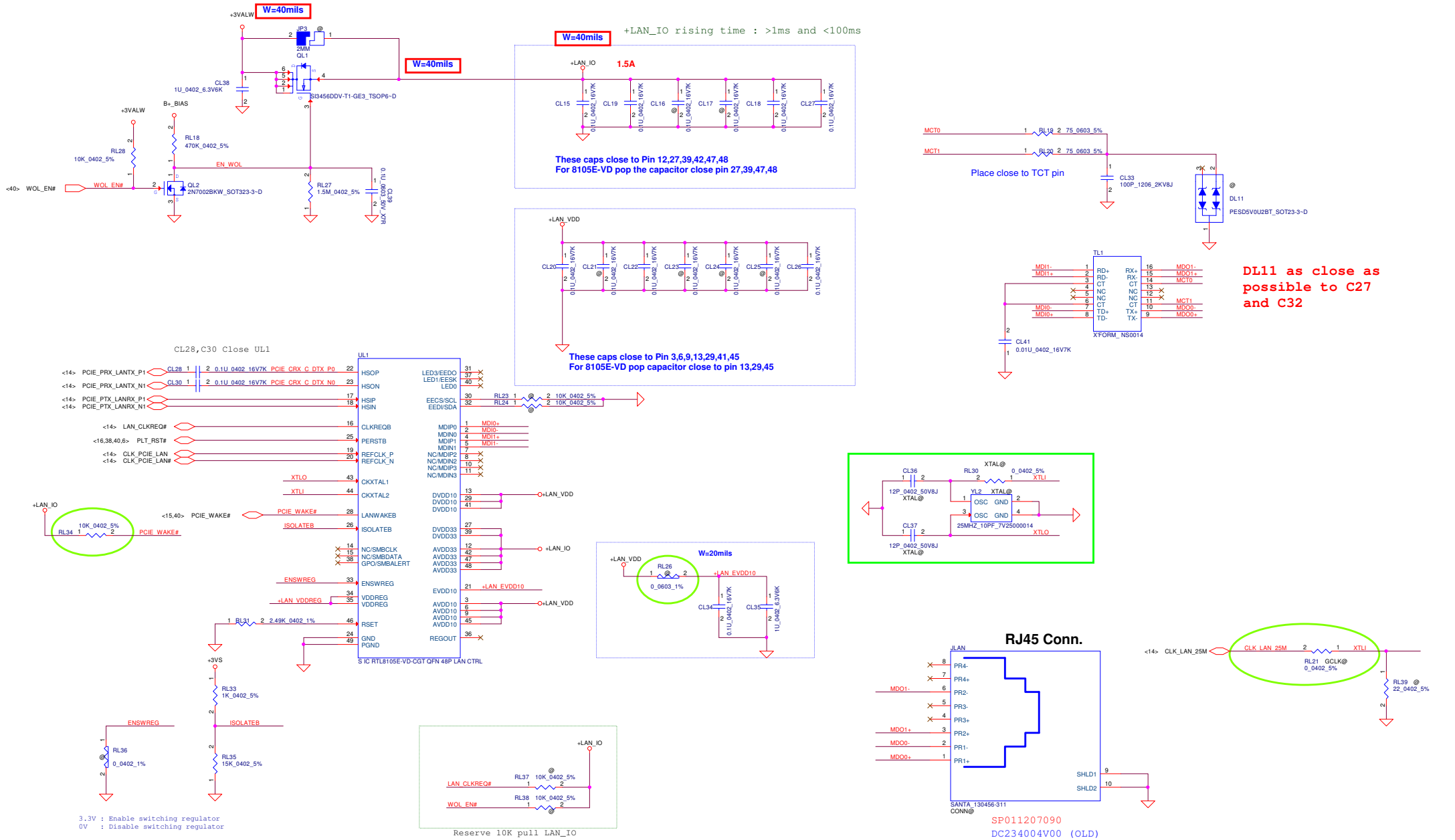

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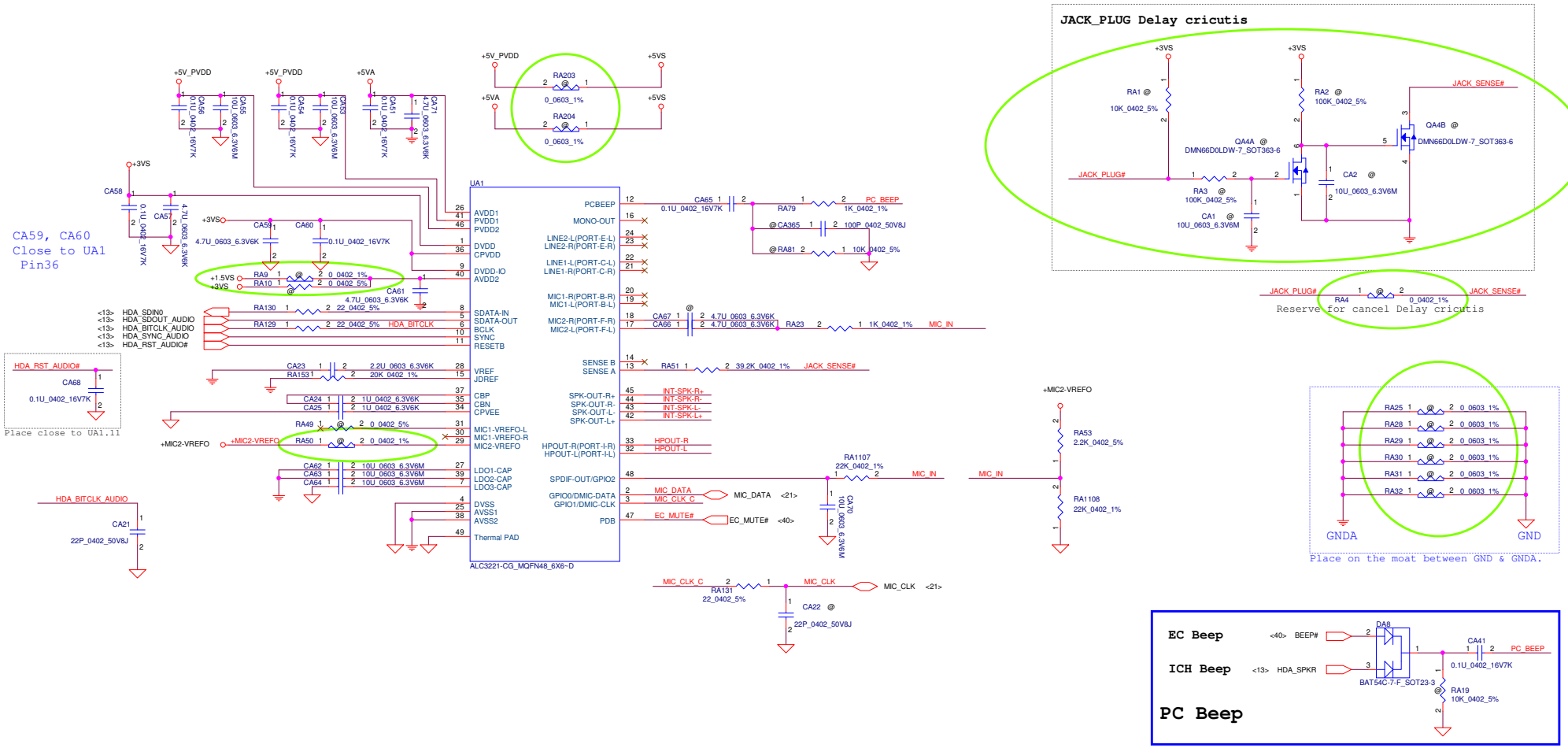
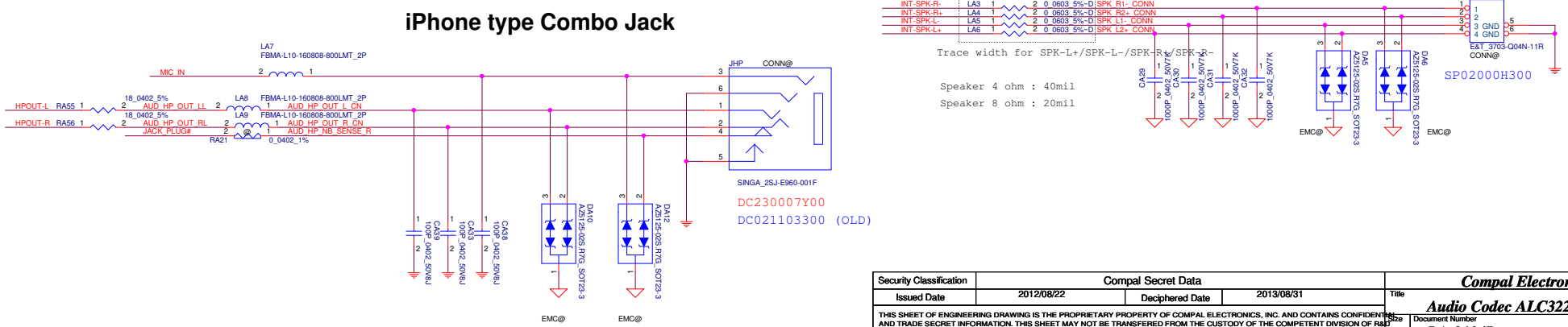
Title: **LAN RTL8105E**

Size: | Document Number: **LA-9104P** | Rev: 1.0

Date: Wednesday, August 29, 2012 | Sheet 32 of 57





Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

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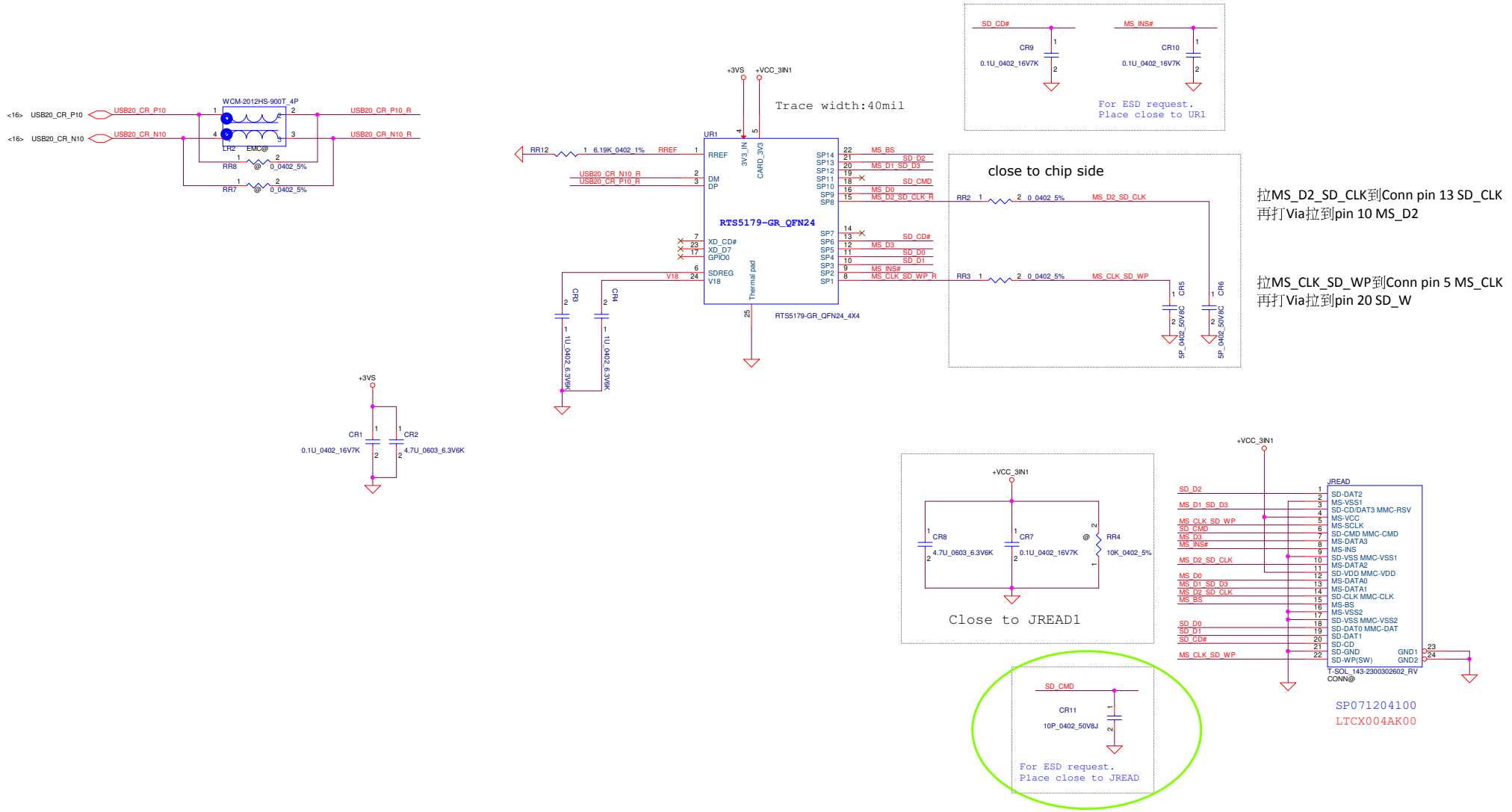
Compal Electronics, Inc.

Title: **Audio Codec ALC3221**

Size | Document Number: **LA-9104P** | Rev: 1.0

Date: Wednesday, August 29, 2012 | Sheet 33 of 57



拉MS_D2_SD_CLK到Conn pin 13 SD_CLK
再打Via拉到pin 10 MS_D2

拉MS_CLK_SD_WP到Conn pin 5 MS_CLK
再打Via拉到pin 20 SD_W

Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

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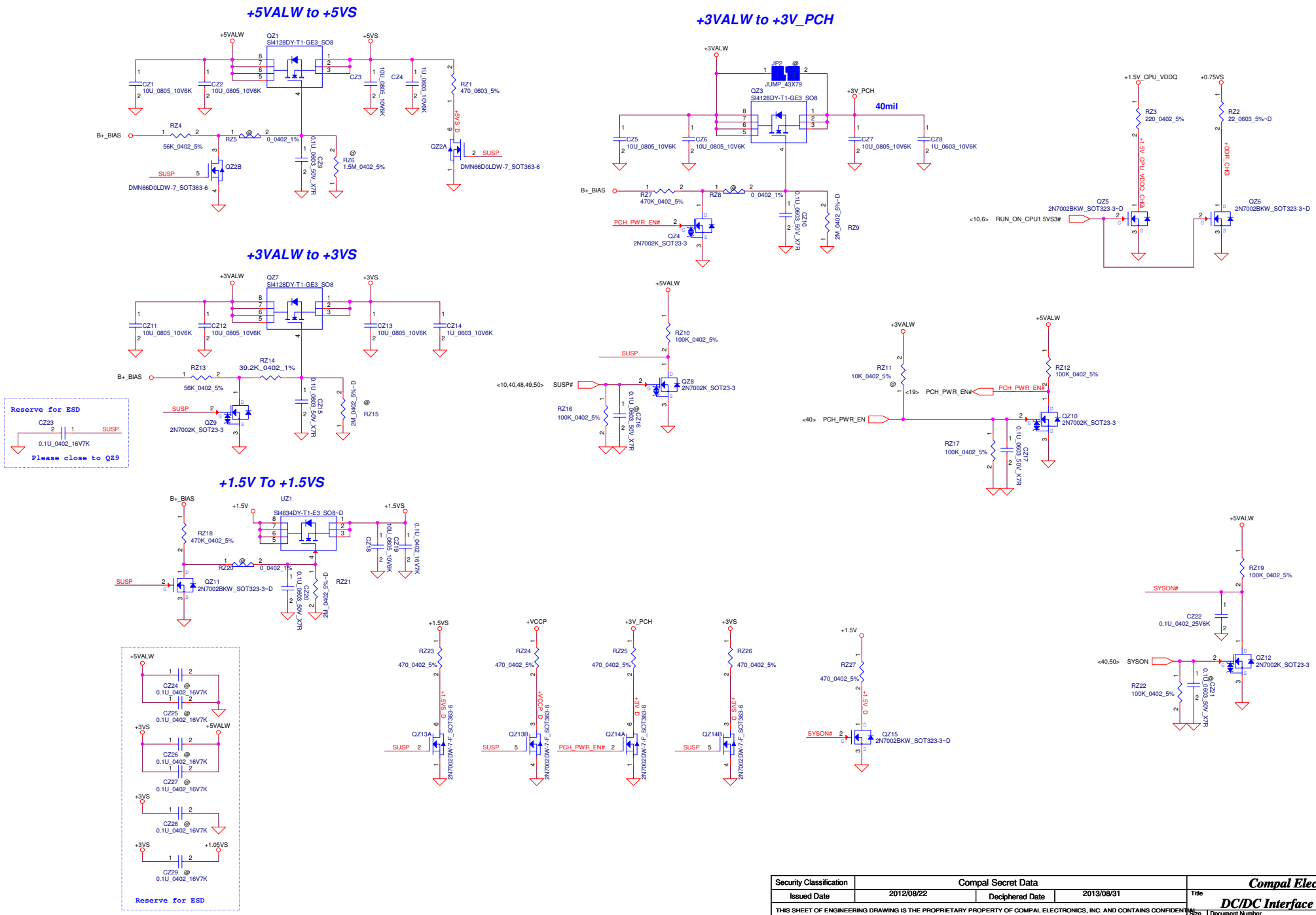
Compal Electronics, Inc.

Title: **Card Reader RTS5179**

Size | Document Number: **LA-9104P** | Rev: 1.0

Date: Wednesday, August 29, 2012 | Sheet 34 of 57



Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

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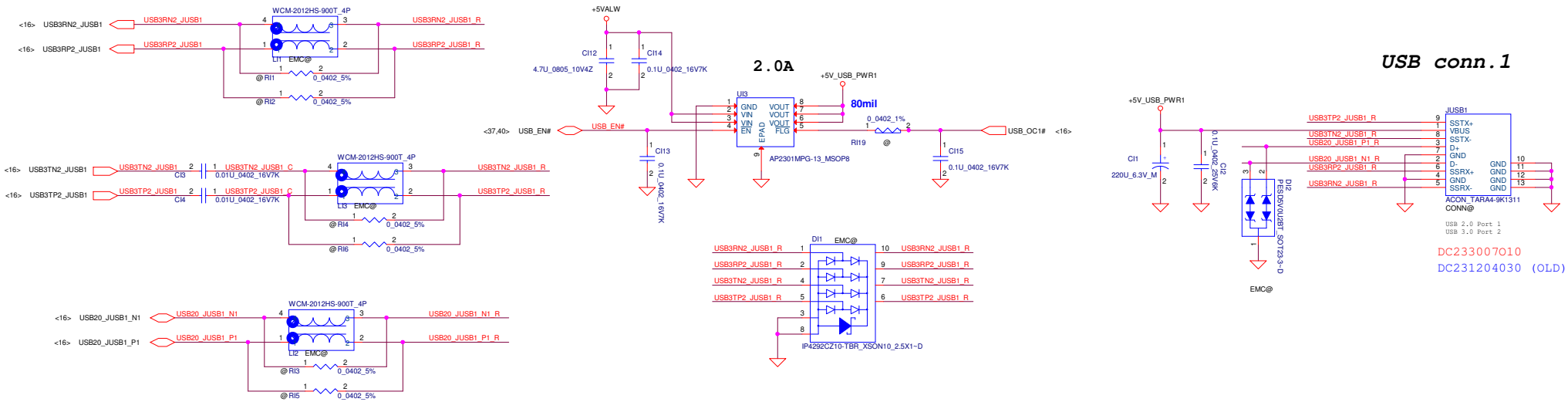
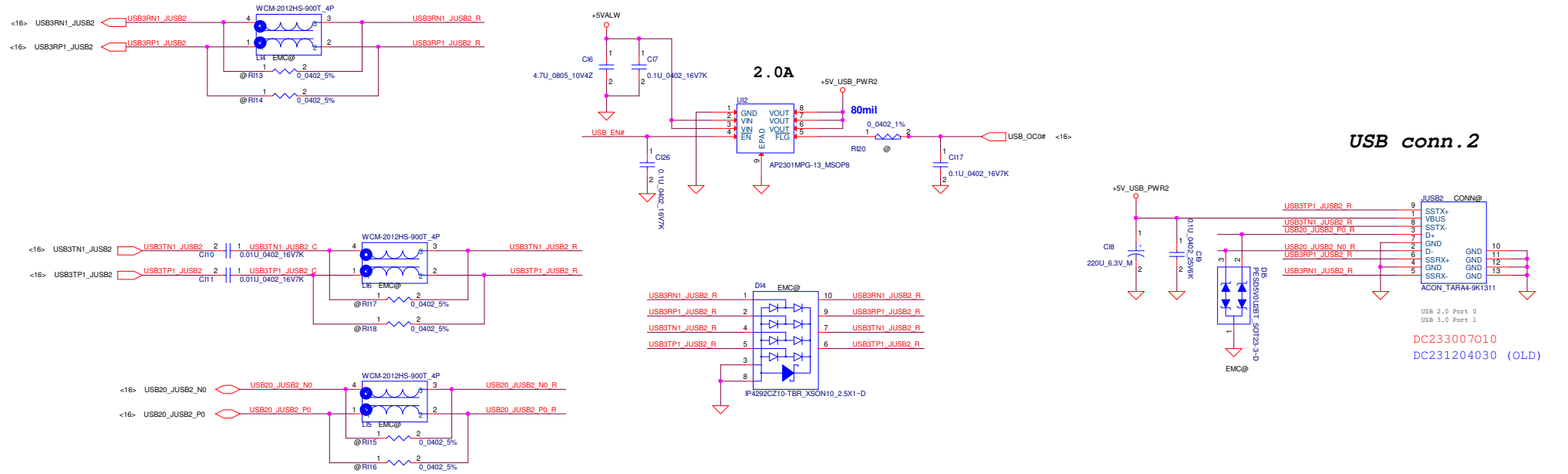
Compal Electronics, Inc.

Title: **DC/DC Interface**

Size | Document Number: **LA-9104P** | Rev: 1.0

Date: Wednesday, August 29, 2012 | Sheet 35 of 57





Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

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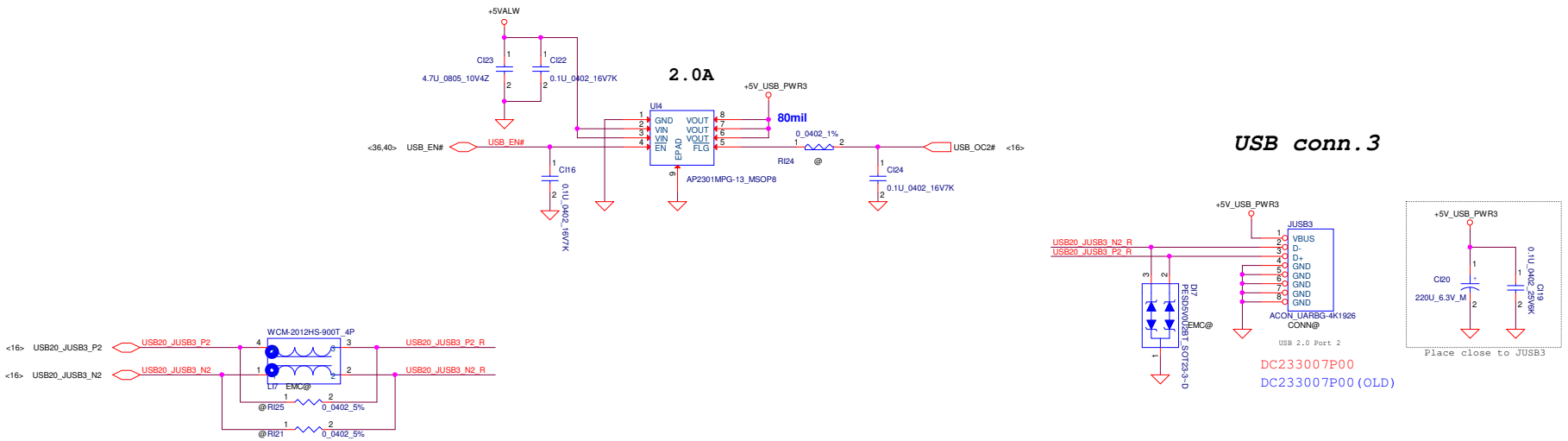
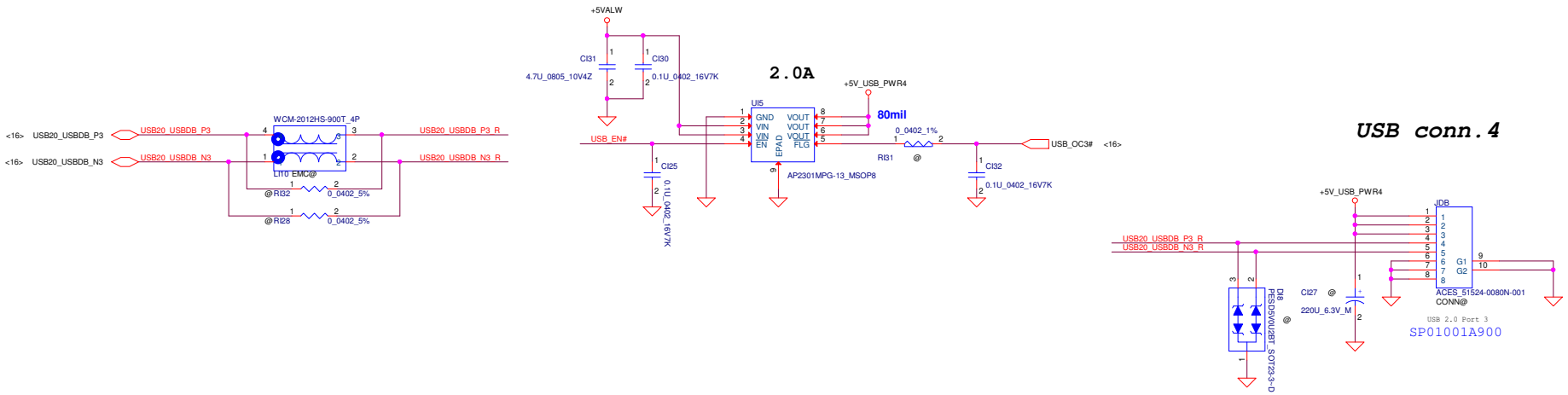
Compal Electronics, Inc.

Title: USB3.0

Size: | Document Number: LA-9104P | Rev: 1.0

Date: Wednesday, August 29, 2012 | Sheet 36 of 57





Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/08/22	Deciphered Date	2013/08/31	Title: MB to USB2.0 DB
				Size: Document Number: LA-9104P — Rev: 1.0
				Date: Wednesday, August 29, 2012 — Sheet 37 of 57

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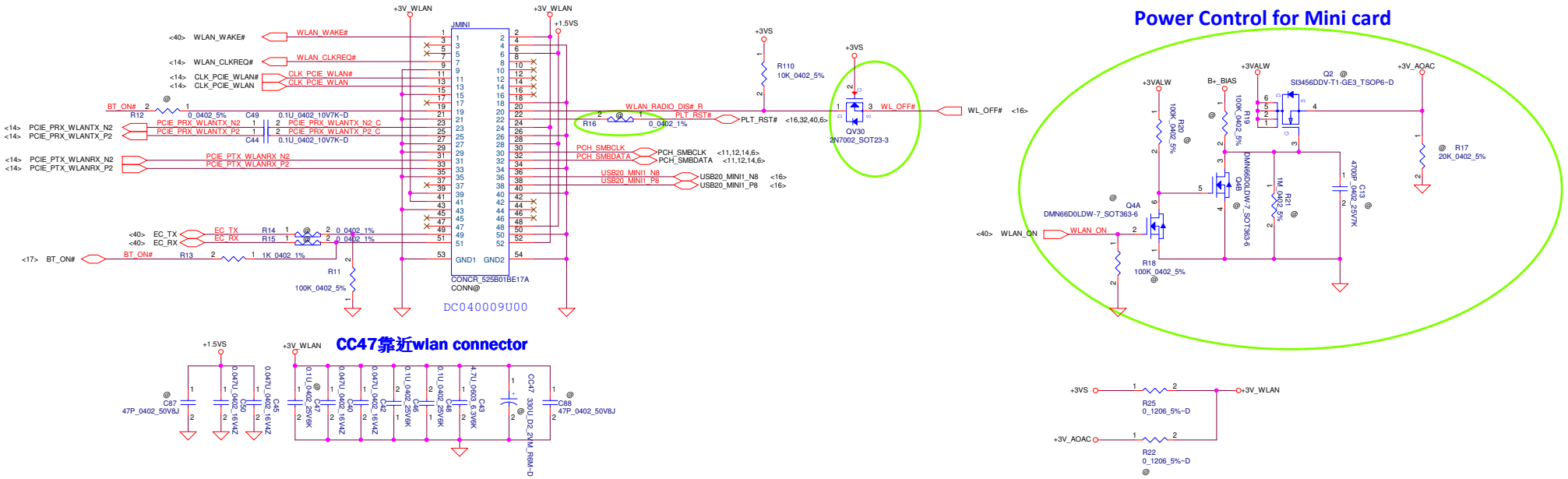
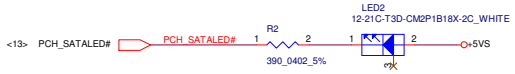
Mini WLAN/WIMAX H=6.7

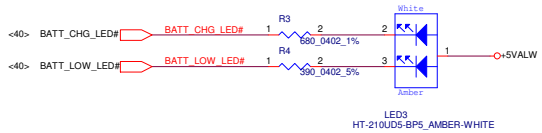


CC47靠近wlan connector

HDD LED

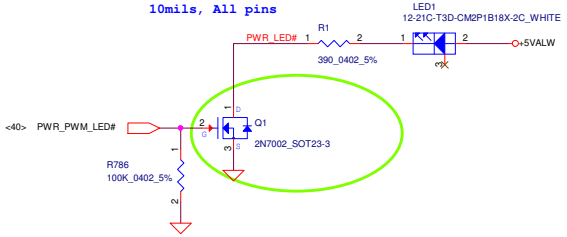


Battery LED

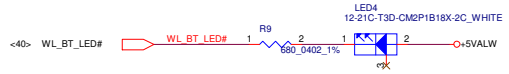


Power LED

10mils, All pins



Wireless LED



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/08/22	Deciphered Date	2013/08/31	Title: Mini Card/LED
				Size / Document Number: LA-9104P / Rev: 1.0
				Date: Wednesday, August 29, 2012 / Sheet 38 of 57

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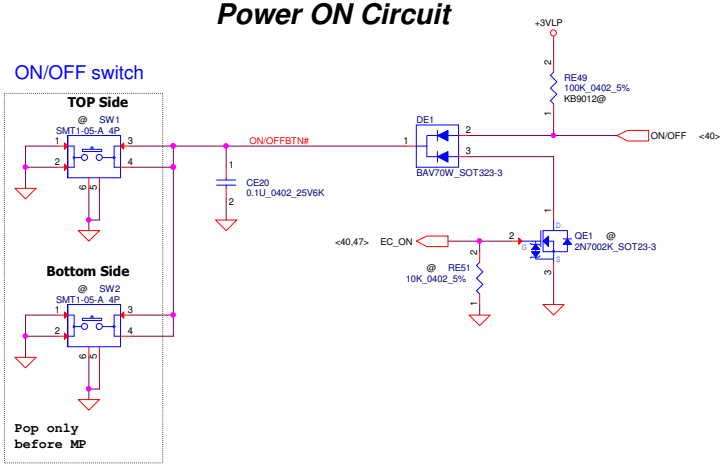
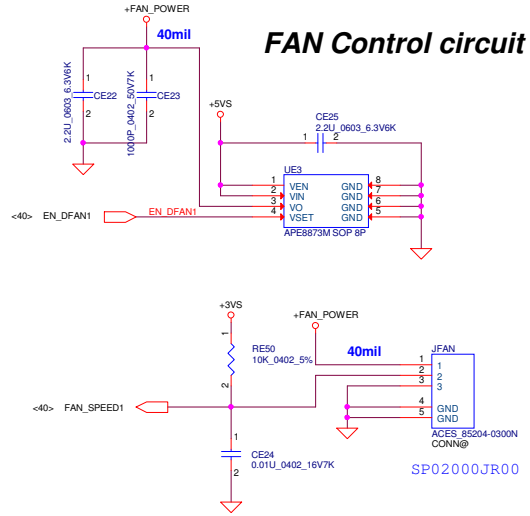
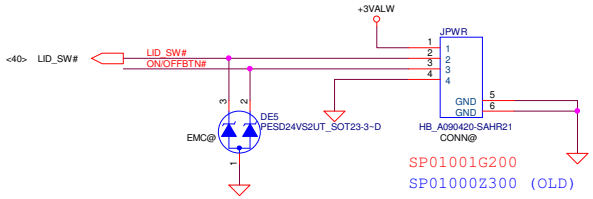
Power ON Circuit



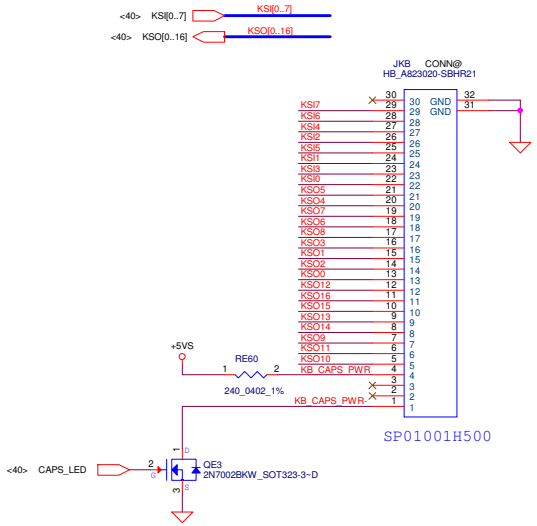
FAN Control circuit



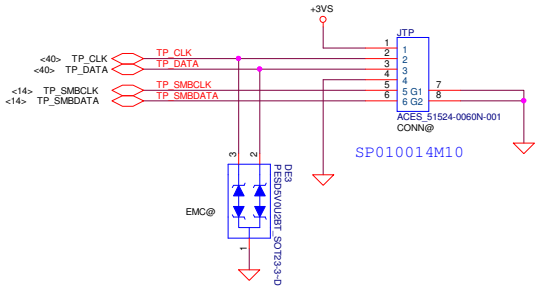
POWER/B



INT_KBD Conn.



Touch pad



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Compal Electronics, Inc.

Title: **FAN/TP/KB/PWR SW**

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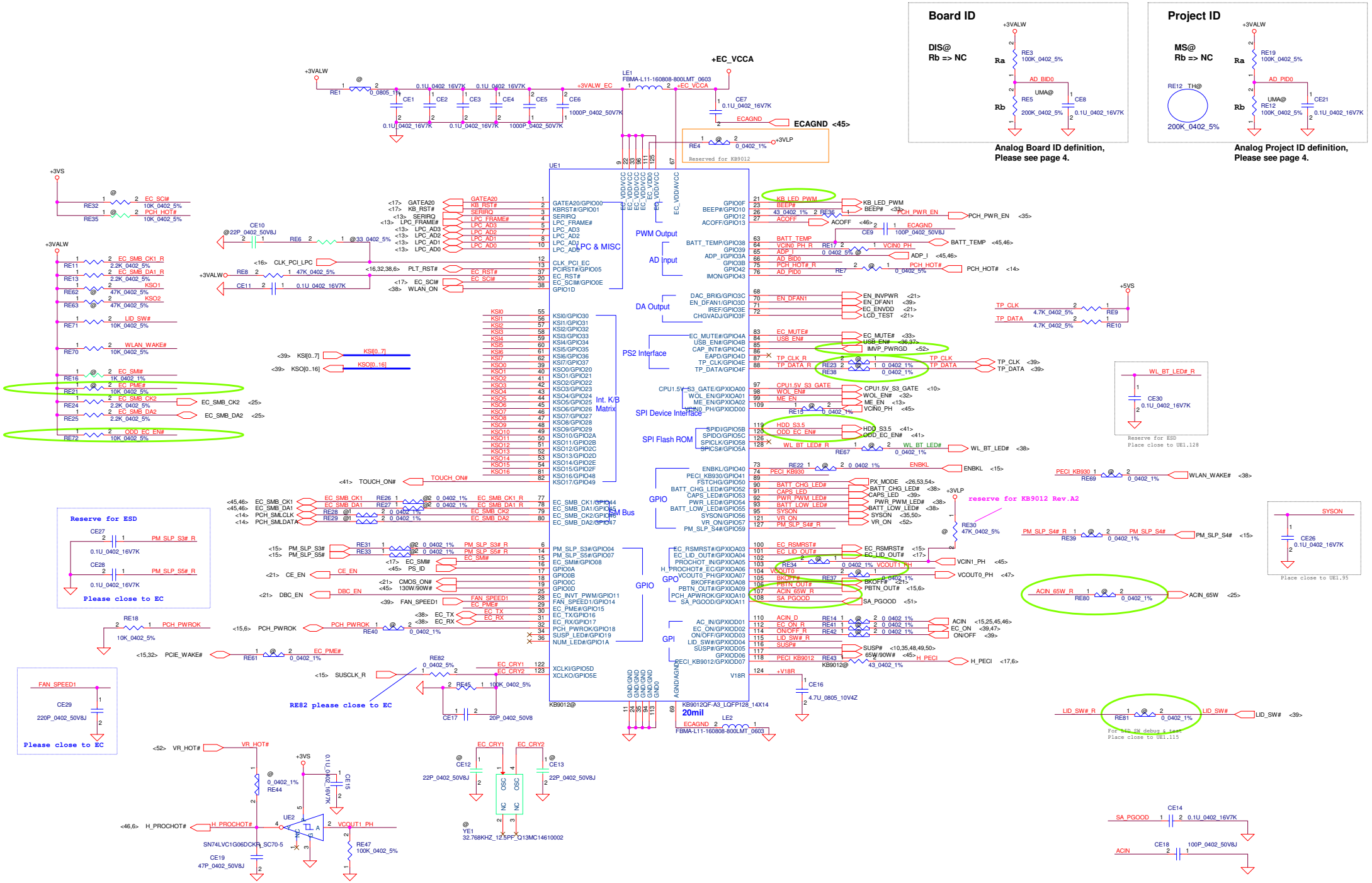
Date: Wednesday, August 29, 2012 | Sheet 39 of 57


Board ID
DIS@
Rb => NC
Analog Board ID definition, Please see page 4.
Project ID
MS@
Rb => NC
Analog Project ID definition, Please see page 4.
+EC_VCCA
ECAGND <45>
UE1
PWM Output
AD Input
DA Output
PS2 Interface
SPI Device Interface
SPI Flash ROM
GPIO
GPI
LPC & MISC
Int. K/B Matrix
SM Bus
Reserve for ESD
Please close to EC
RE82 please close to EC
reserve for KB9012 Rev.A2
20mil
KB9012QF-A3_LQFP128_14X14
Compal Electronics, Inc.
EC ENE-KB9012
LA-9104P
Security Classification
Compal Secret Data
Issued Date
2012/08/22
Deciphered Date
2013/08/31
Date: Wednesday, August 29, 2012
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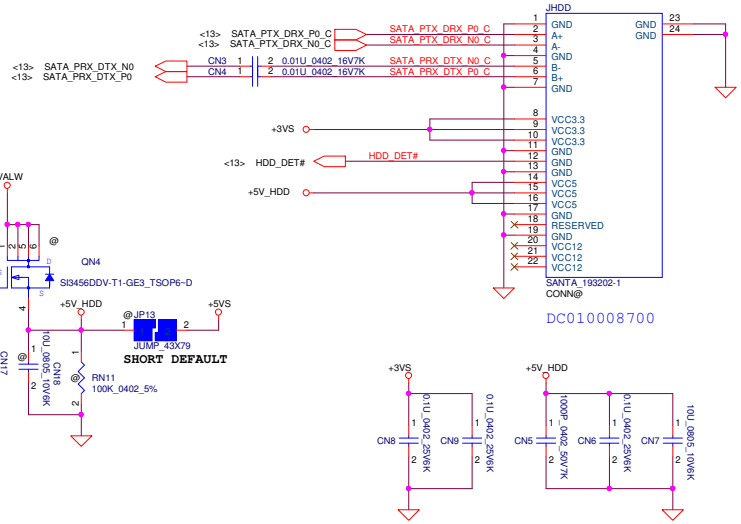
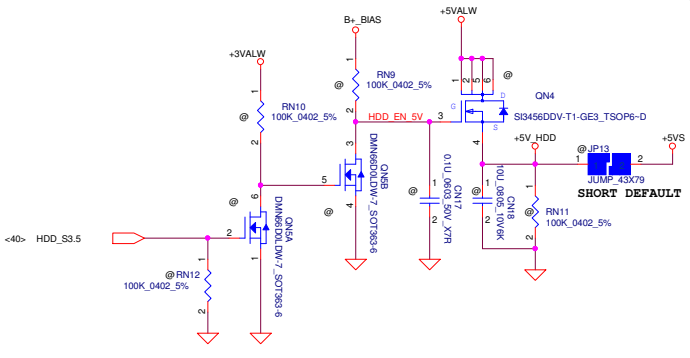
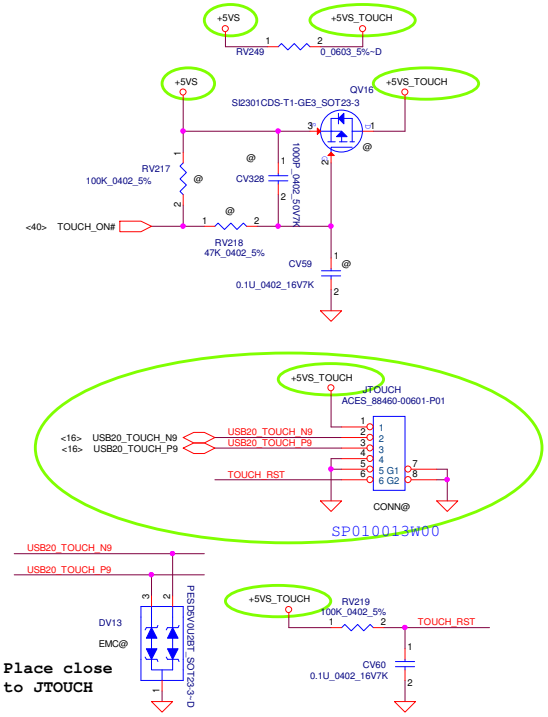
SATA HDD Conn.



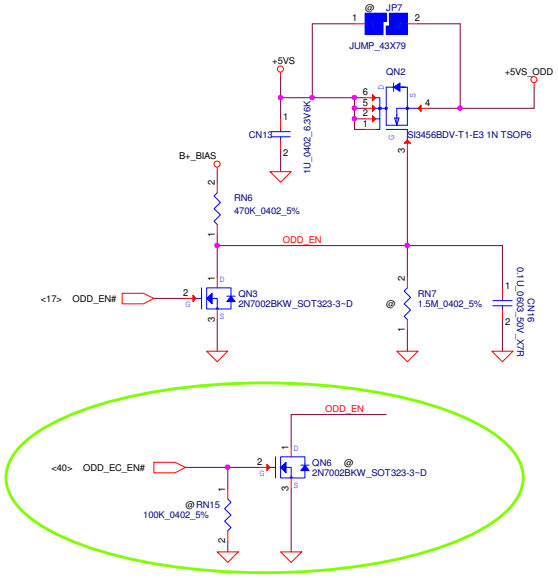
+5V_HDD Source



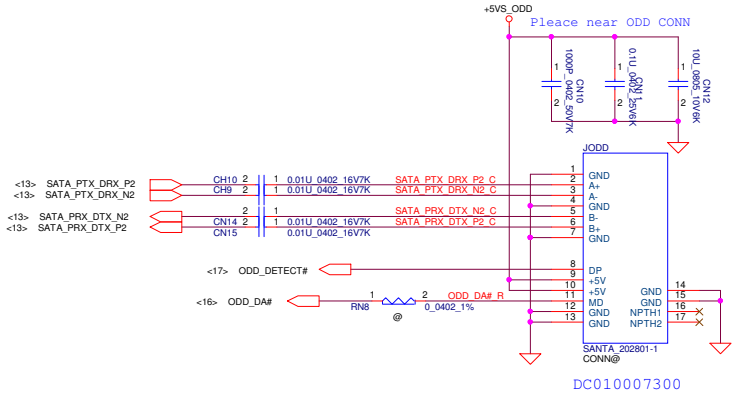
* Touch Screen Panel



ODD Power Control



SATA ODD Conn.



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: HDD / ODD

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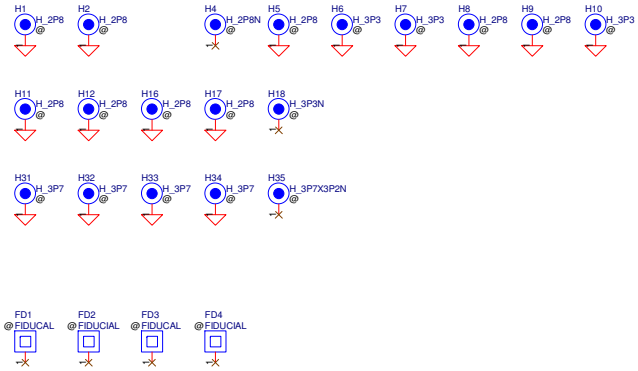
Screw Hole



Security Classification	Compal Secret Data		
Issued Date	2012/08/22	Deciphered Date	2013/08/31

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Compal Electronics, Inc.

Title: **Screw Hole**

Size | Document Number: **LA-9104P** | Rev: 1.0

Date: Wednesday, August 29, 2012 | Sheet 42 of 57

Version Change List (P. I. R. List) Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	21,39	LVDS	2012/05/17	SED	Add FHD Panel CE_ENABLE, DBC_ENABLE function from SED request	Add CE_EN, DBC_EN control pin to EC	0.2
2	21	LVDS	2012/05/22	SED	Follow SED team request disable CE_EN function	Change RV62 to DE-POP and RV100 to POP for disable CE_EN function	0.2
3	33	Audio codec	2012/05/23	CODEC	Follow CODEC vendor suggestion	Add AUDIO JACK PLUG delay circuit, Spearate NET JACK_PLUG to => JACK_SENSE# & => JACK_PLUG#	0.2
4	16,21	Touch Screen	2012/05/29	HW	Add touch screen function	Add RV217, RV218, RV219, RV249, CV59, CV60, CV328, DV13, QV16, JTOUCH	0.2
5	39	Board ID	2012/05/30	HW	Board ID change for PT	Change RE5 from 8.2k_0402(SD028820180) to 33k_0402(SD028330280)	0.2
6	21,39	Touch Screen	2012/05/30	HW	Add touch screen function power control	Add NET "TOUCH_ON#" from JTOUCH to UE1.82(KB9012) for TOUCH SCREEN PANEL power control	0.2
7	33	Audio codec	2012/05/30	HW	Follow RealTek suggestion remove, delete reserve MUTE circuit	Delete D1,QA1,QA2,QA3,RA24,RA26,RA60,RA62,RA68,RA109,CA72,CA73	0.2
8	15,16, 39,41	ESD	2012/05/30	ESD	ESD ask CAP for reserve	Reserve 0.1u/0402 CH104,CZ23,CH105,CE27,CE29	0.2
9	14	Green CLK	2012/05/30	HW	For Green CLK test	Change RH31,RH41,RV232 0ohm form "GCLK@" to "@" for break the clock signal to device	0.2
10	10,26,41	DC/DC	2012/05/31	HW	Change "+1.5V_CPU_VDDQ", "+1.5VS", "+1.5VGS" derating	Change RC150 330K/0402 to 2M/0402, RC151 100K/0402 to 470K/0402, RZ18 100K/0402 to 470K/0402, RV115 0/0402 to 2M/0403	0.2
11	41	DC/DC	2012/05/31	HW	For power sequence trunning	Change RZ15 to DE-POP	0.2
12	06,15,16, 39,41	ESD	2012/05/31	ESD	Follow ESD team request	Change 0.1u/0402 from "@" to POP	0.2
13	32	Green CLK	2012/06/15	HW	Change for Green CLK bom control	Change RL21,RL30 from "@" to "GCLK@"	0.2
14	41	DC/DC	2012/06/15	HW	For WLAN card power sequence issue	Change RZ4,RZ13 from 470K/0402 56K/0403	0.2
15	35,41	Schematic page modify	2012/06/18	HW	Schematic page modify for easily maintain.	Swap Page. 35 & Page 41.	0.2
16	41	ODD	2012/06/18	HW	Change component location for easily maintain.	Move CH9,CH10 from Page.13 to Page.41	0.2
17	39	FAN	2012/06/29	HW	Fan speed noise issue	Reserve 220p/0402 CE24	0.2
18	6	CPU	2012/06/29	ESD	System boot-up shot down issue.	Change CC151 from POP to "@"	0.2
19	21,35, 39,40,41	Circuit adjuest	2012/07/01	HW	Circuit & page adjust for OAK 15" & OAK 17"	1. Swap P.35 & P.41and move touch screen circuit from P.21 to P.41. 2. Swap P.39 & P.40 page no	0.2
20	40	LID SW	2012/07/01	HW	LID SW need a trace for debug and switch.	Add RE81 for LID SW.	0.2
21	25	GPU	2012/07/01	HW	Follow AMD request, MarsPro will used MPLs.	Change RV75,RV76,RV81 from "DIS@" to "TH@"	0.2
22	29	GPU	2012/07/01	HW	Follow AMD request, MEM_CALRP2 is not need for Mars ASIC now.	Change RV205 from "MS@" to "@"	0.2
23	38	MINI card	2012/07/03	HW	Power Control for Mini card didn't need	Change R17 to "@"	0.2
24	6	XDP	2012/07/06	HW	S3 return hang issue	Change RC89 from "@" to POP	0.2
25	23	GREEN CLK	2012/07/09	HW	Follow Green CLK FAE suggestion	1. Change UG1.2(+3VLP) & UG1.8(+3VALW) connect to +LAN_IO 2. Add R787 connect from +RTCBATT to C5.2 & UG1.10 3. Change C14 from 0.1u to 5p/0402 4. Change C8 connect from +3V_ALW to +LAN_IO 5. Add R788 0ohm/0402 from +RTCVCC to UG1 for GCLK & DH1 select	0.2
26	35	MOAT	2012/07/09	ESD	For ESD request reserve CAP.	Reserve those CAP for ESD MOAT.	0.2
27	18	LVDS	2012/07/10	HW	Change RES and reserve CAP for LVDS issue	Change RH185 from 0ohm-short to 0ohm/0805, and reserve CH106 1U/0402	0.2
28	13	PCH	2012/07/11	ESD	Follow ESD team request	Add RH44,RH48,RH70 & NET PCH_JTAG_TMS_R, PCH_JTAG_TDI_R, PCH_JTAG_TDO_R for break signal trace	0.2
29	40	PCH	2012/07/11	ESD	Follow ESD team request	1.Change NET NAME "N59110727" to "WL_BT_LED#_R" 2. Reserve 0.1u/0402 on "WL_BT_LED#_R" for ESD	0.2
30	21	LVDS	2012/07/11	HW	Reserve for CE function for LVDS connector	Change CE_EN_R from dummy to JLVDS.18	0.2
31	32	Connector	2012/07/12	ME	For ME request	Change JLAN CPN from "DC234004V00" to "SP011207090"	0.2
32	40	FAN	2012/07/16	HW	For FAN_SPEED1 noise issue	Change CE29 from "@" to POP	0.2
33	14	Touch PAD	2012/07/17	SED	Change Touch PAD SMBUS port for SMBUS issue	Change Touch PAD SMBUS port for SMB0 to SMB	1.0
34	32	GREEN CLK	2012/07/19	HW	Follow Silego FAE request	Change RL21 from 510 ohm to 0 ohm/0402	1.0
35	41	Touch Screen	2012/08/07	SED	Follow SED team request change JTOUCH USB signal conatct.	Change JTOUCH Pin define.	1.0
36	34	Card Reader	2012/08/14	ESD	Follow ESD team request	Reserve CR11 100p/0402 close to JREAD	1.0
37	23	GREEN CLK	2012/08/16	HW	Fixed GCLK output abnormal issue	Change UG1.2(UG1/VDD) from +LAN_IO to+3VALW	1.0
38	33	CODEC	2012/08/16	HW	The issue already fixed by new CODEC.	Remove delay circuit and POP RA4	1.0
39	23	GREEN CLK	2012/08/17	HW	For RTC discharge issue	De-pop R788	1.0
40	32,34	LAN	2012/08/17	HW	For LAN Chip abnormal leakage issue	Pop RL34 and de-pop RE21	1.0
41	34	Card Reader	2012/08/20	ESD	Follow ESD team request	Change CR11 from 100p/0402 to 10p/0402 and POP	1.0

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Version Change List (P. I. R. List) Page 2

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
42	41	Touch Screen	2012/08/20	SED	Follow SED team request	Change Touch screen power rail for +3VS to +5VS	1.0
43	38	LED	2012/08/20	HW	Change LED light	Change LED1,LED2,LED4 CPN from SC500006000 to SC50000DC00	1.0
44	38	WLAN	2012/08/20	HW	Remove AOAC function power control	Change R18,R19,R20,R21,C13,Q2,Q4 component BOM structure to "@"	1.0
45	41	Touch Screen	2012/08/20	HW	Add EC control for Touch Screen function	Add RN15 & QN6 and relative circuit connect	1.0
46	40	BATMAN2	2012/08/21	HW	For BATMAN2	Add RE82 0ohm/0402 between trace SUSCLK_R & EC_CRY2	1.0
47	14,17	PCH	2012/08/21	HW	For SYSTEM S3 leakage issue	Change RH79.2 & RH245.2 connect from +3V_PCH to +3VS	1.0

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Issued Date	2012/08/22	Deciphered Date	2013/08/31

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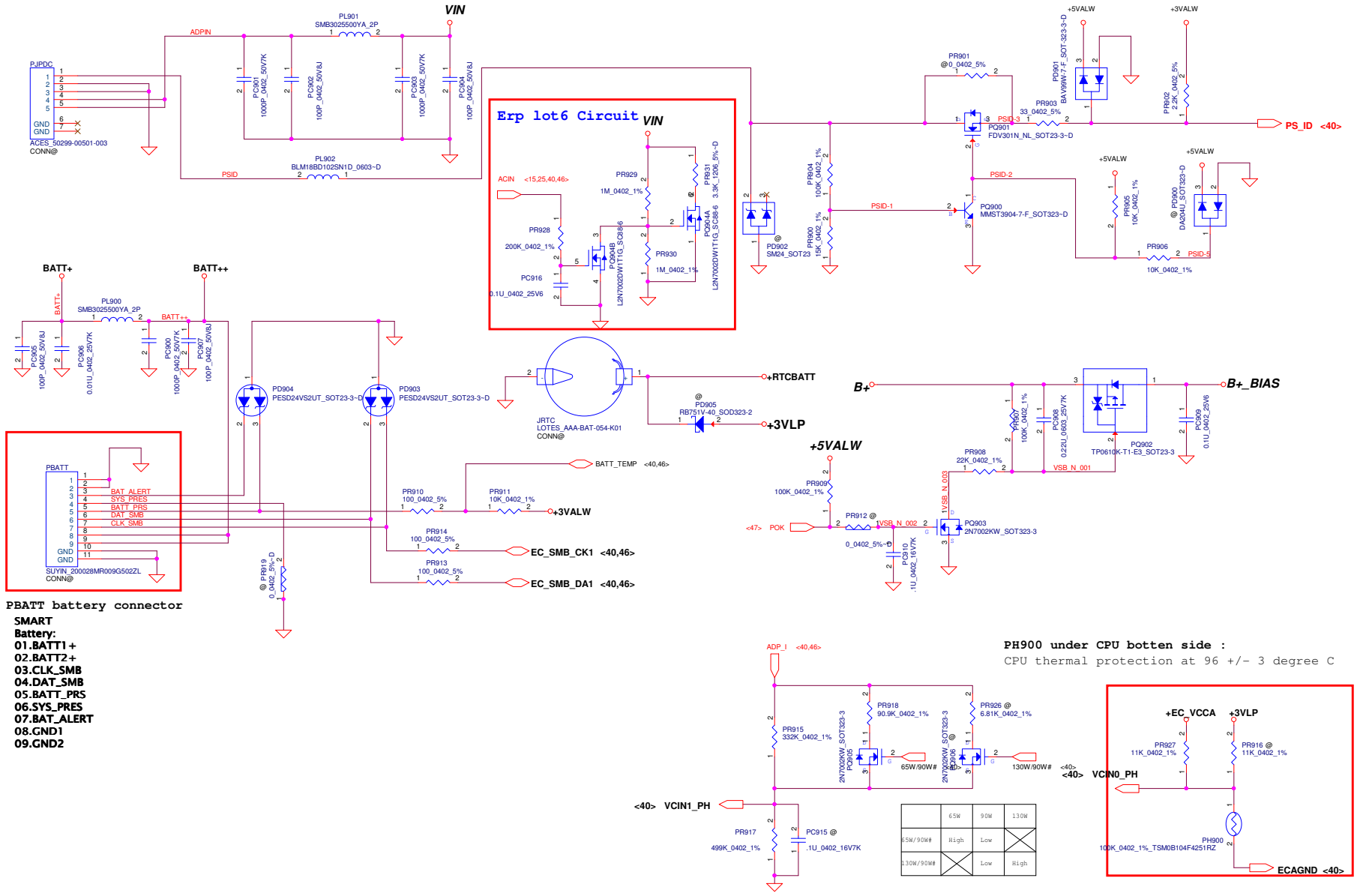
Compal Electronics, Inc.

Title: HW-PIR

Size | Document Number: LA-9104P | Rev: 1.0

Date: Wednesday, August 29, 2012 | Sheet 44 of 57



	65W	90W	130W
65W/90W#	High	Low	
130W/90W#		Low	High

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Issued Date	2012/08/22	Deciphered Date	2013/08/31

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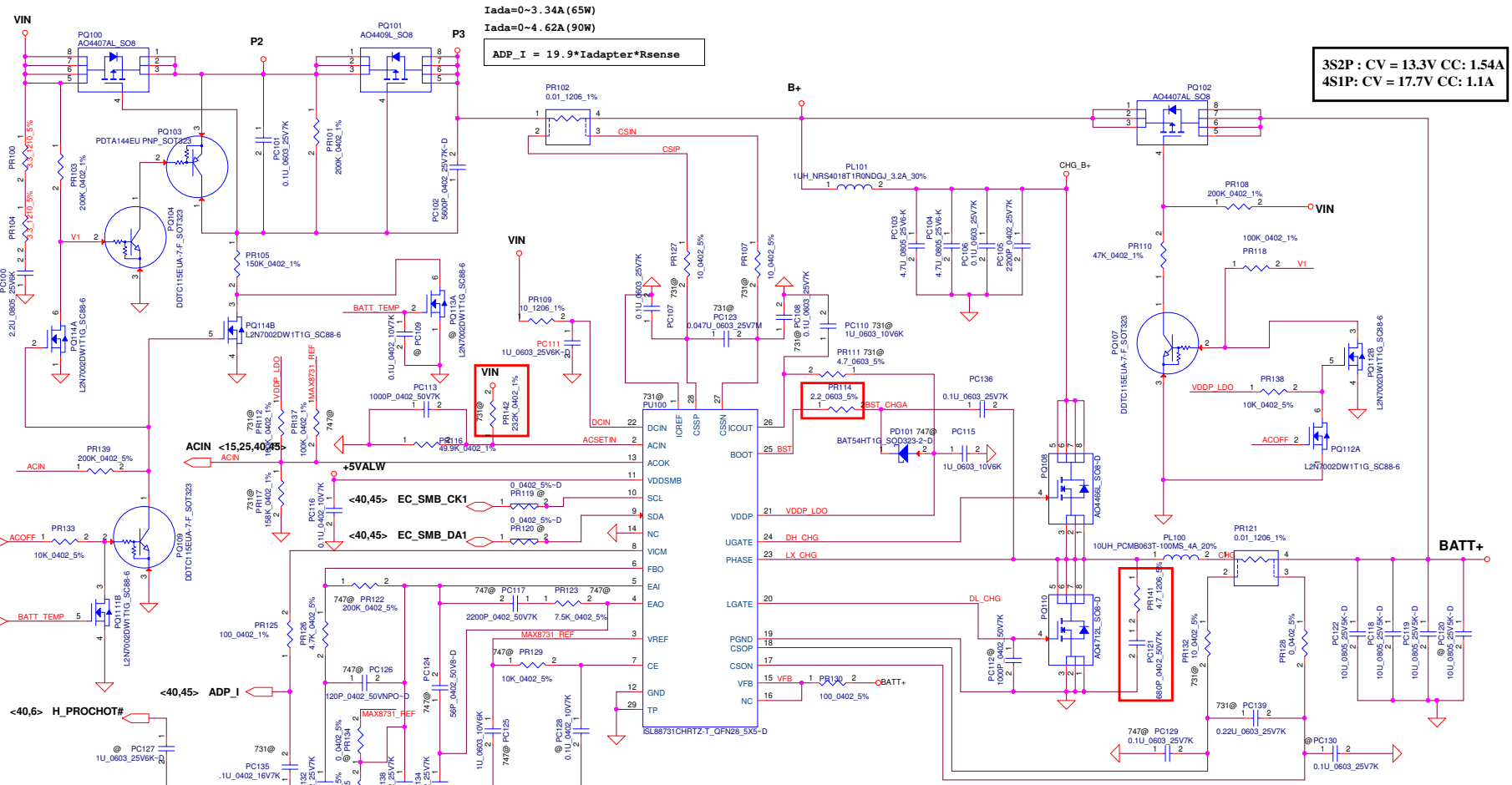
Compal Electronics, Inc.

Title: PWR_DCIN/BATT CONN/OTP

Size: | Document Number: LA-9104P | Rev: 1.0

Date: Wednesday, August 29, 2012 | Sheet 45 of 57



	ISL88731C	BQ24747
PU100	ISL88731C	BQ24747
PR137	@	100k
PR112	100k	@
PR117	158k	@
PR142	232k	324k
PC135	0.1u	220p
PC132	0.01u	@

	ISL88731C	BQ24747
PR122	@	200k
PR123	@	7.5k
PR129	@	10k
PC117	@	2200p
PC124	@	56p
PC126	@	120p
PC125	@	1u

	ISL88731C	BQ24747
PC134	0.01u	@
PC129	@	0.1u
PC139	0.22u	0.1u
PR132	10	0
PR111	4.7	@
PC110	1u	@
PD101	@	BAT54HT1G

	ISL88731C	BQ24747
PC108	0.1u	@
PR127	10	0
PR107	10	0
PC123	0.047u	0.1u

731@ for ISL88731C

747@ for BQ24747

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Compal Electronics, Inc.

Title: PWR_CHARGER

Size | Document Number: LA-9104P | Rev: 1.0

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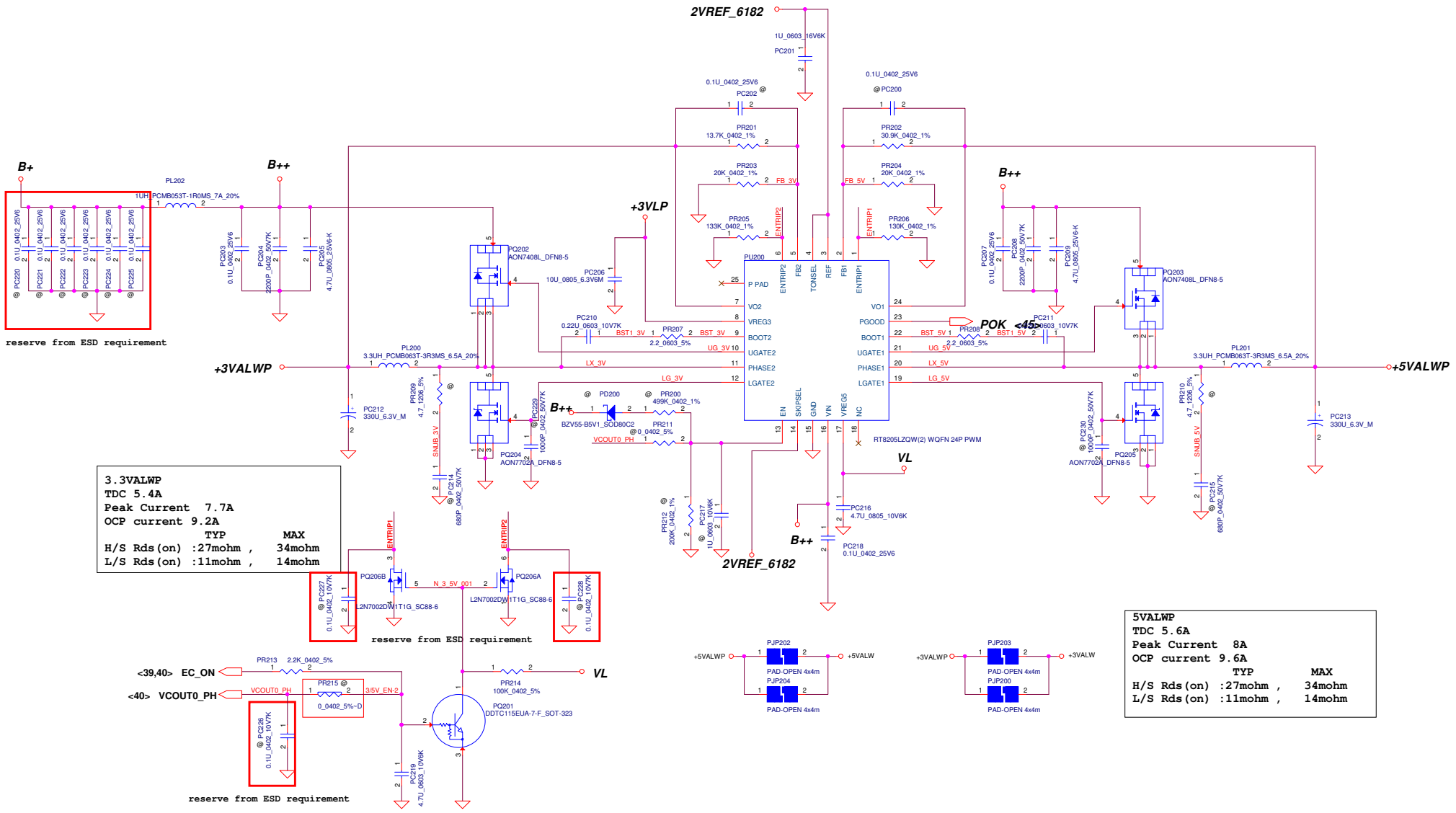

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Compal Electronics, Inc.

Title: PWR_3.3VALWP/5VALWP

Size | Document Number: LA-9104P | Rev: 1.0

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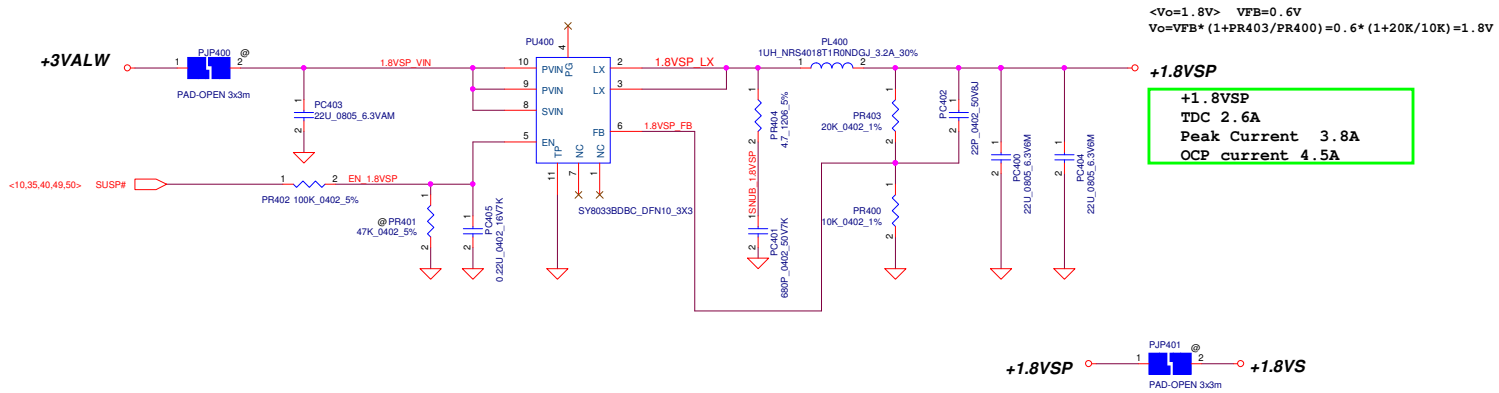

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Compal Electronics, Inc.

Title: **PWR_1.8VSP**

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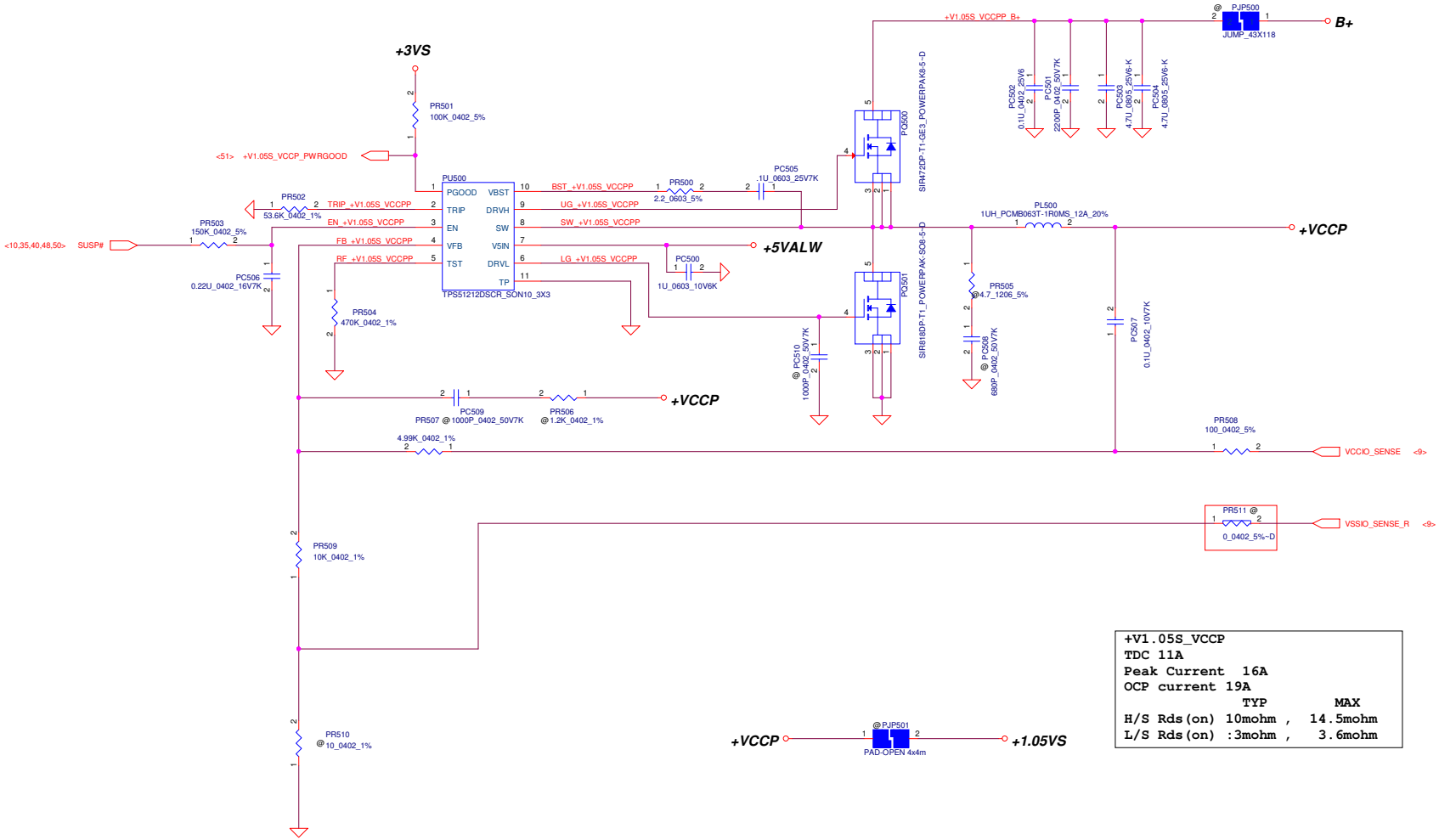

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Issued Date	2012/08/22	Deciphered Date	2013/08/31

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Compal Electronics, Inc.

Title: **PWR_+VCCIO**

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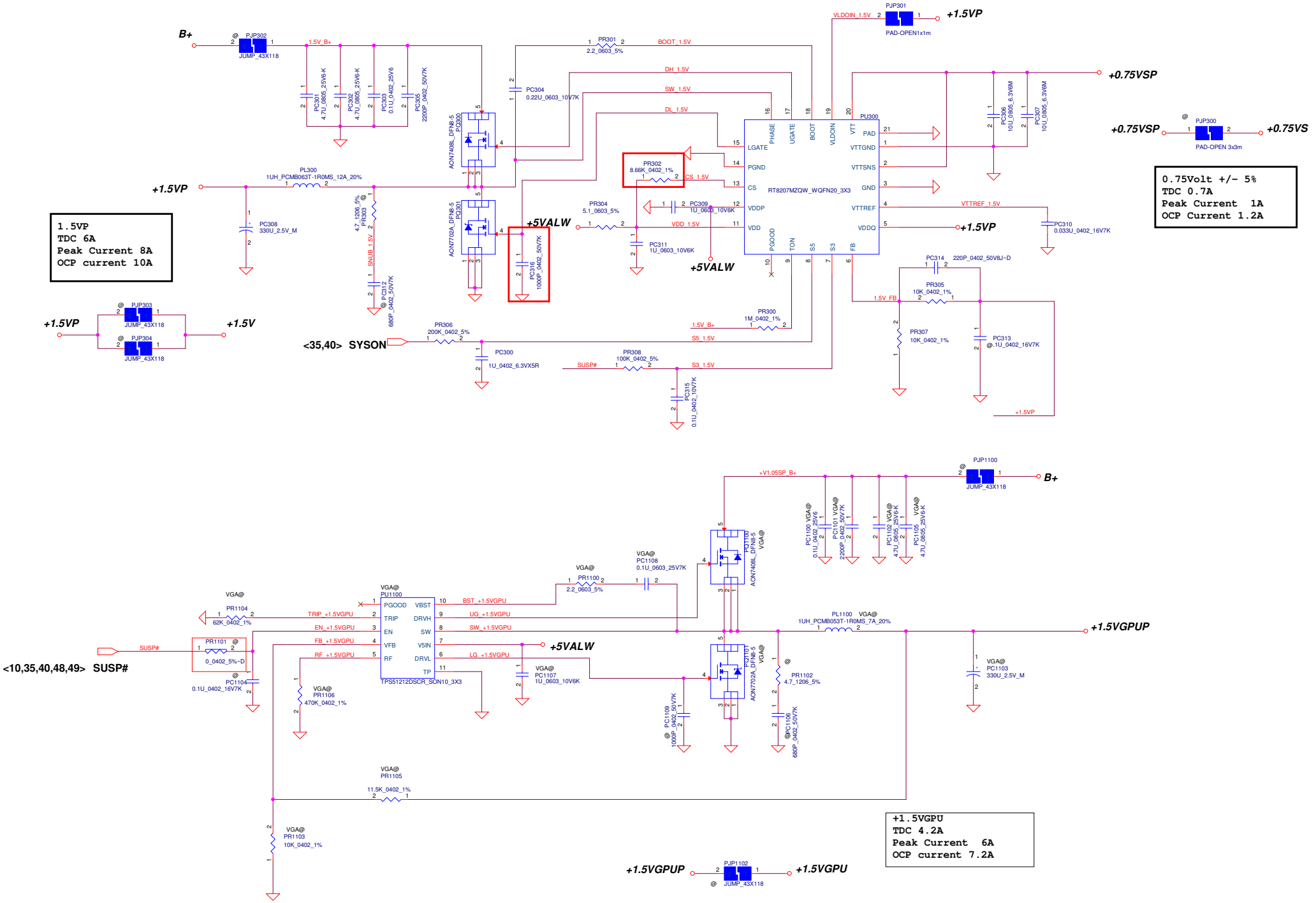

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Compal Electronics, Inc.

Title: PWR_+1.5VP/+1.5VGPUP/0.75VSP

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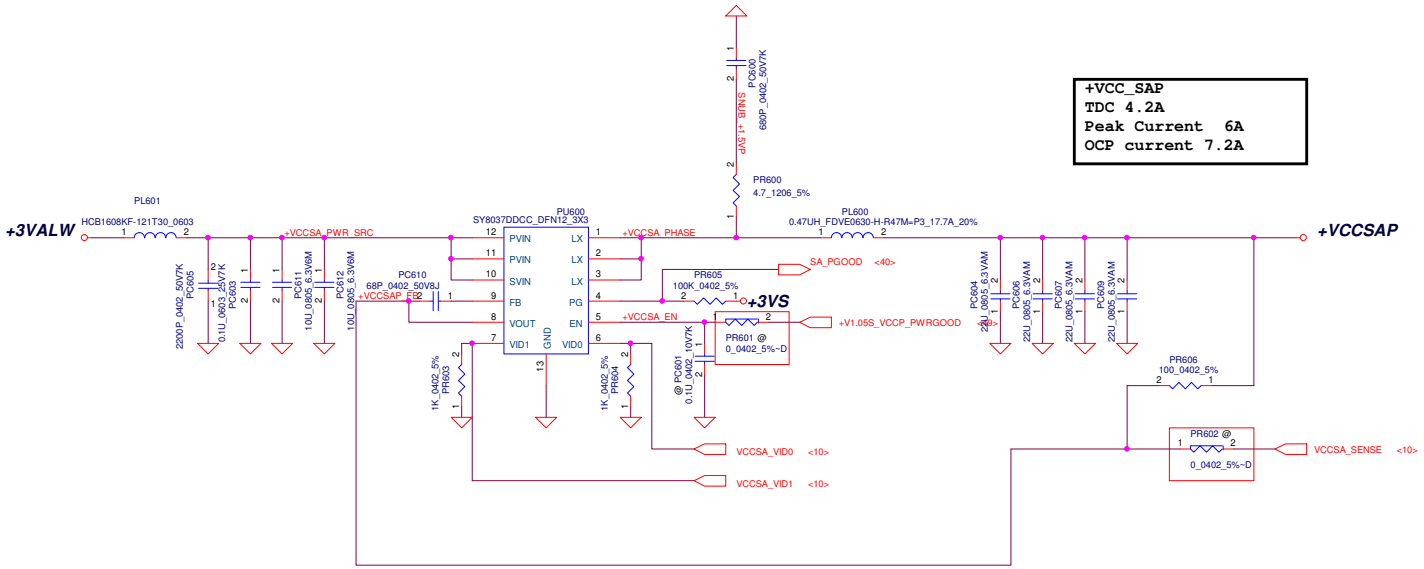
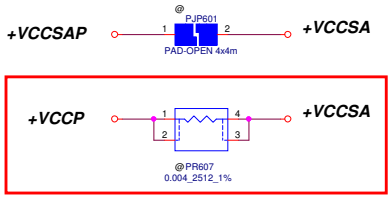
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

output voltage adjustable network

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A



The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.



reserve for Pentium and Celeron only

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Compal Electronics, Inc.

Title: PWR_+VCCSAP

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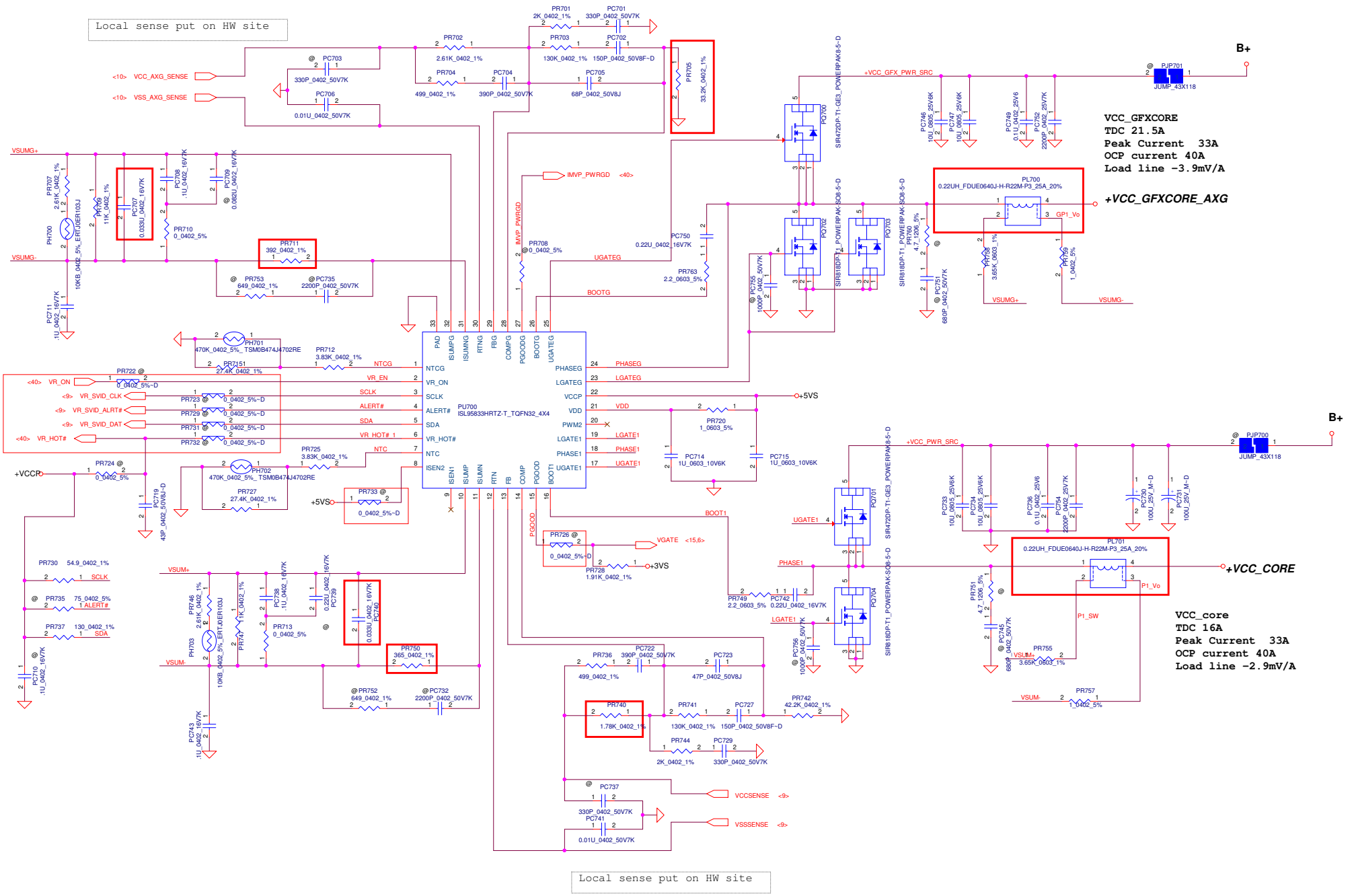

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Compal Electronics, Inc.

Title: **PWR_VCORE**

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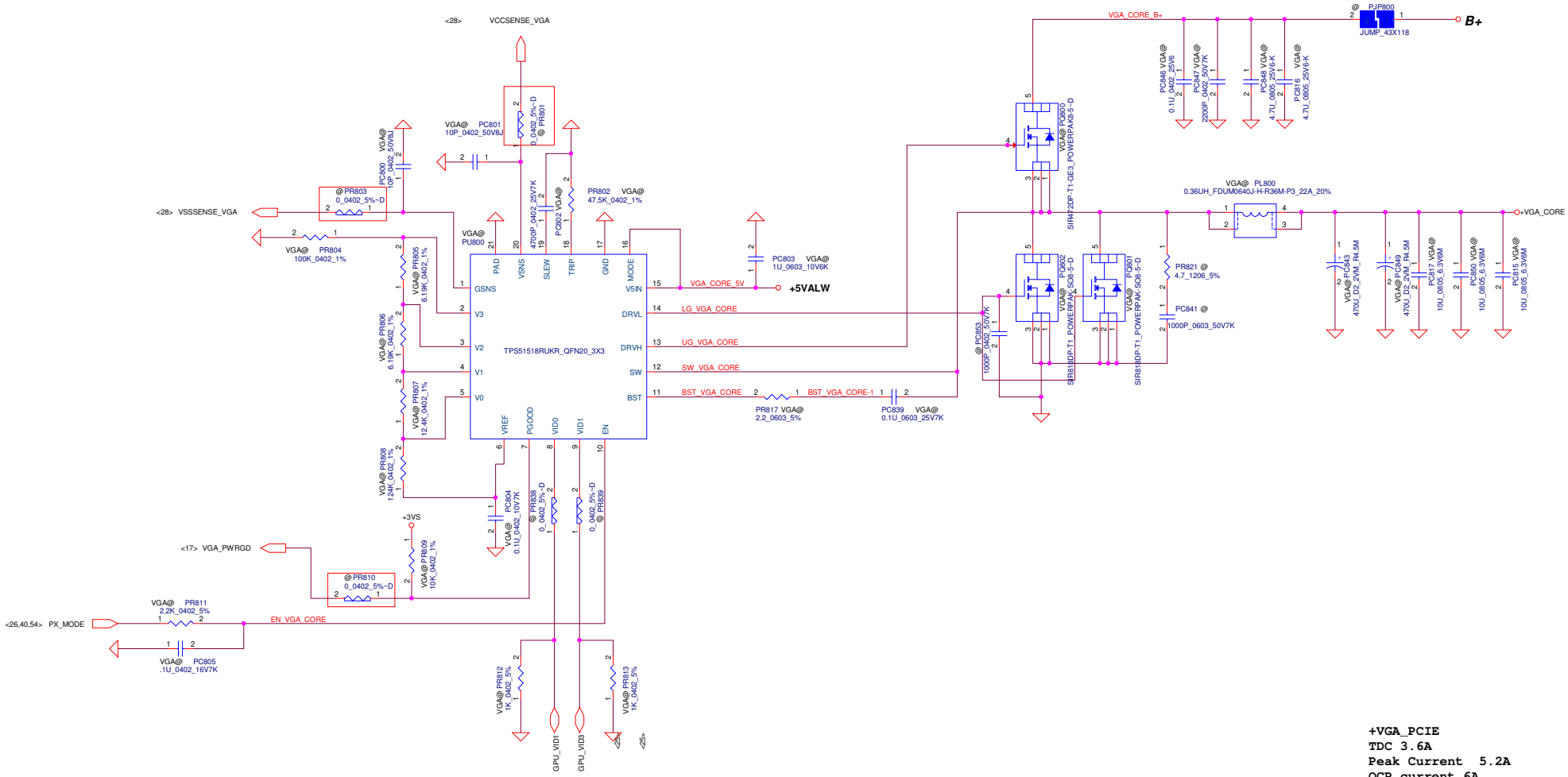
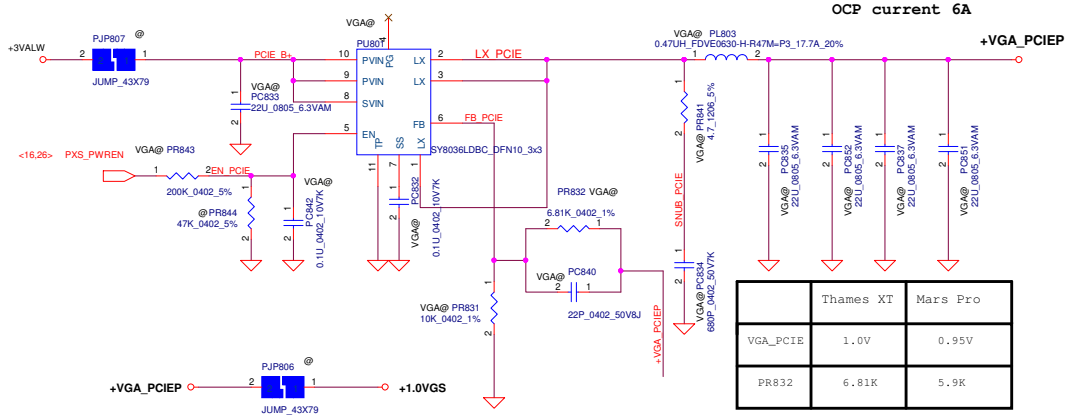


Thames XT

GPU_VID3 (GPIO15)	GPU_VID1 (GPIO20)	Core Voltage Level
1	1	0.8V
1	0	0.85V
0	1	0.9V
0	0	1.0V

+VGA_CORE
TDC 20A
Peak Current 30A
OCP current 36A
FSW=350kHz
DCR 1.4mohm +/-5%

+VGA_PCIE
TDC 3.6A
Peak Current 5.2A
OCP current 6A



	Thames XT	Mars Pro
VGA_PCIE	1.0V	0.95V
PR832	6.81K	5.9K

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Compal Electronics, Inc.

Title: **PWR_VGA_CORE/VGA_PCIE**

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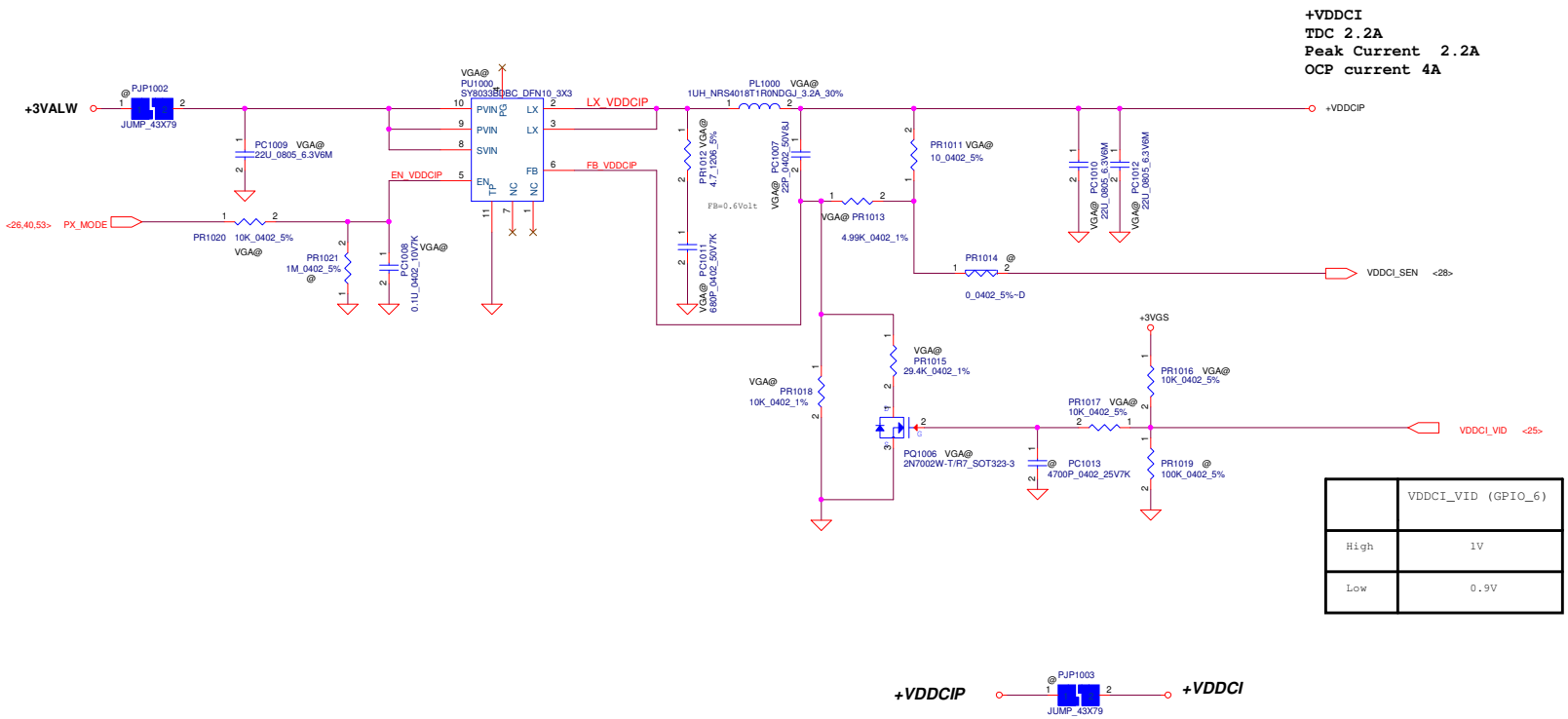

	VDDCI_VID (GPIO_6)
High	1V
Low	0.9V

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Issued Date	2012/08/22	Deciphered Date	2013/08/31

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Compal Electronics, Inc.

Title: **PWR_+VDDCIP**

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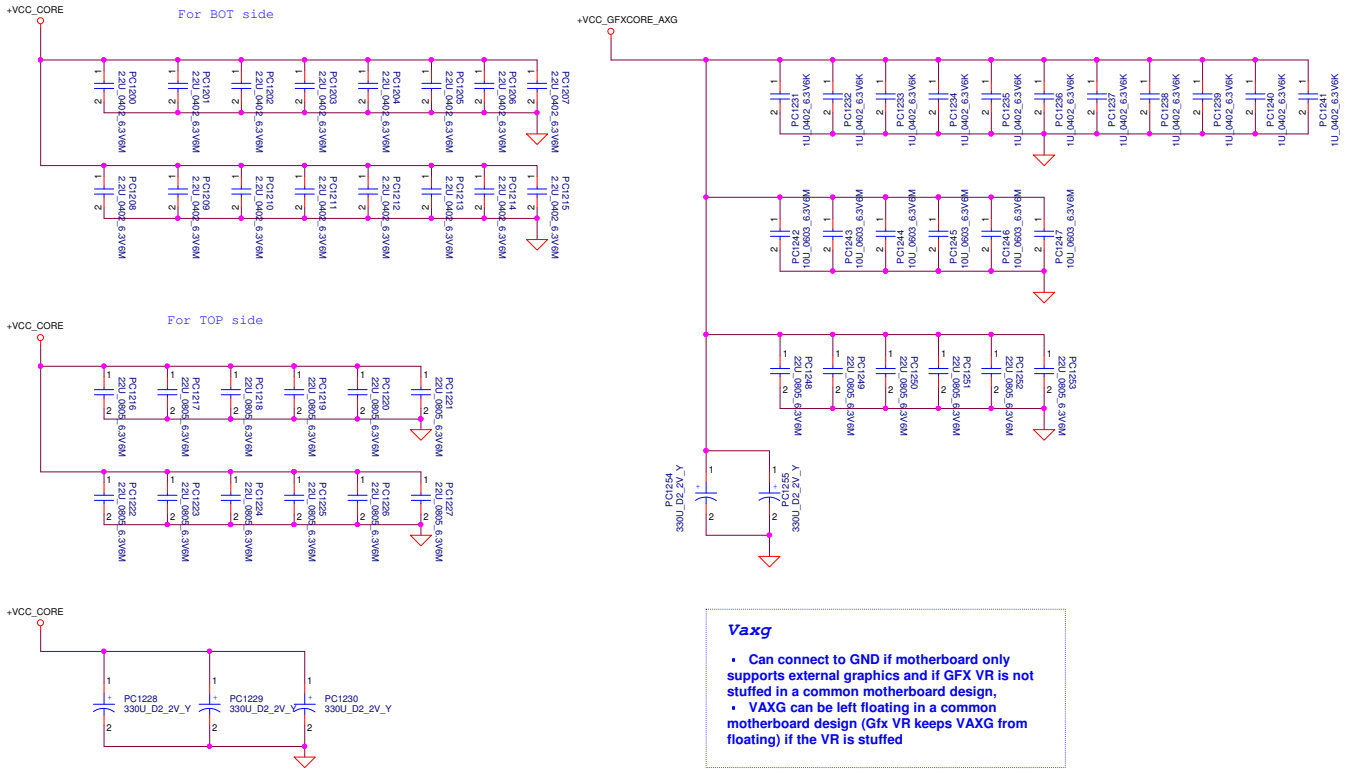
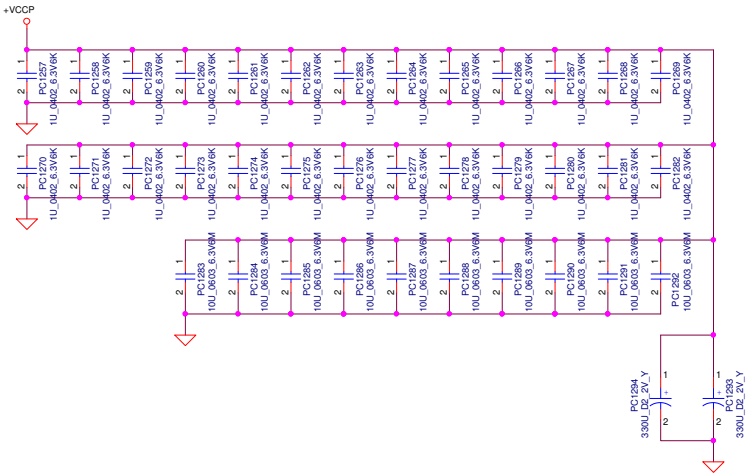


Vaxg

- **Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,**
- **VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed**



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Compal Electronics, Inc.

Title: **PWR_PROCESSOR DECOUPLING**

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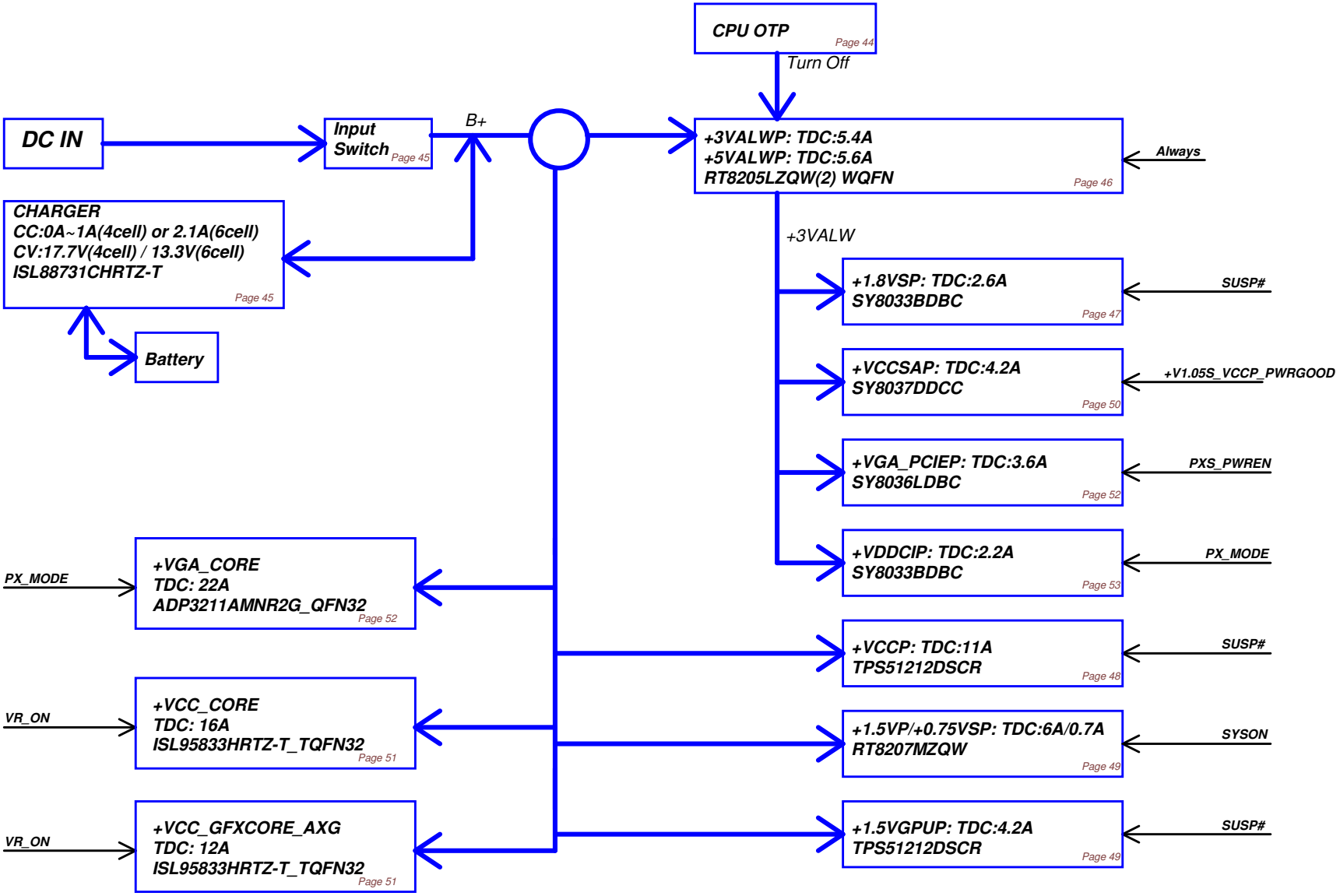
Power block



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Compal Electronics, Inc.

Title: PWR_POWER BLOCK DIAGRAM

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Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	51	VCORE	12/05/11	Morris	adjust VR parameter	change PL700 and PL701 from 0.36u to 0.22u change PC707 and PC740 from 0.047u to 0.033u change PR750 from 649 to 365 change PR711 from 649 to 392 change PR740 from 1.91k to 1.78k change PR705 from 150k to 33.2k	X00
2	44 45 46	DCIN/BATT CONN/OTP CHARGER 3.3VALWP/5VALWP	12/05/11	Morris	follow SSI memo for part shortage issue	change PQ112,PQ114,PQ1111,PQ206,PQ904 from SB00000CQ00 to SB00000PV00	X00
3	49	+1.5VP/1.5VDGPU/0.75VSP	12/05/15	Morris	design change	change PR302 from 12k to 8.66k	X00
4	50	+VCCSAP	12/05/23	Morris	for Pentium and Celeron special BOM	add PR607 and reserve	X00
5	49	+1.5VP/1.5VDGPU/0.75VSP	12/07/06	Morris	design change to reduce low-side mosfet induce	add PC316 1000pf	X01
6	45	CHARGER	12/07/17	Morris	from EMI request	change PR114 from 0 to 2.2 add PR141 and PC121	X01
7	45	CHARGER	12/07/17	Morris	design change to solve Battery LED is still on after unplug AC when SUT in S3S4S5 issue	change PR142 from 210k to 232k for ISL88731C (X76) change PR142 from 309k to 324k for BQ24747 (X76)	X01
8	44	DCIN/BATT CONN/OTP	12/07/17	Morris	revise OTP setting to 96C from thermal request	change PR927 from 12.1k to 11k	X01

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