

Compal Confidential

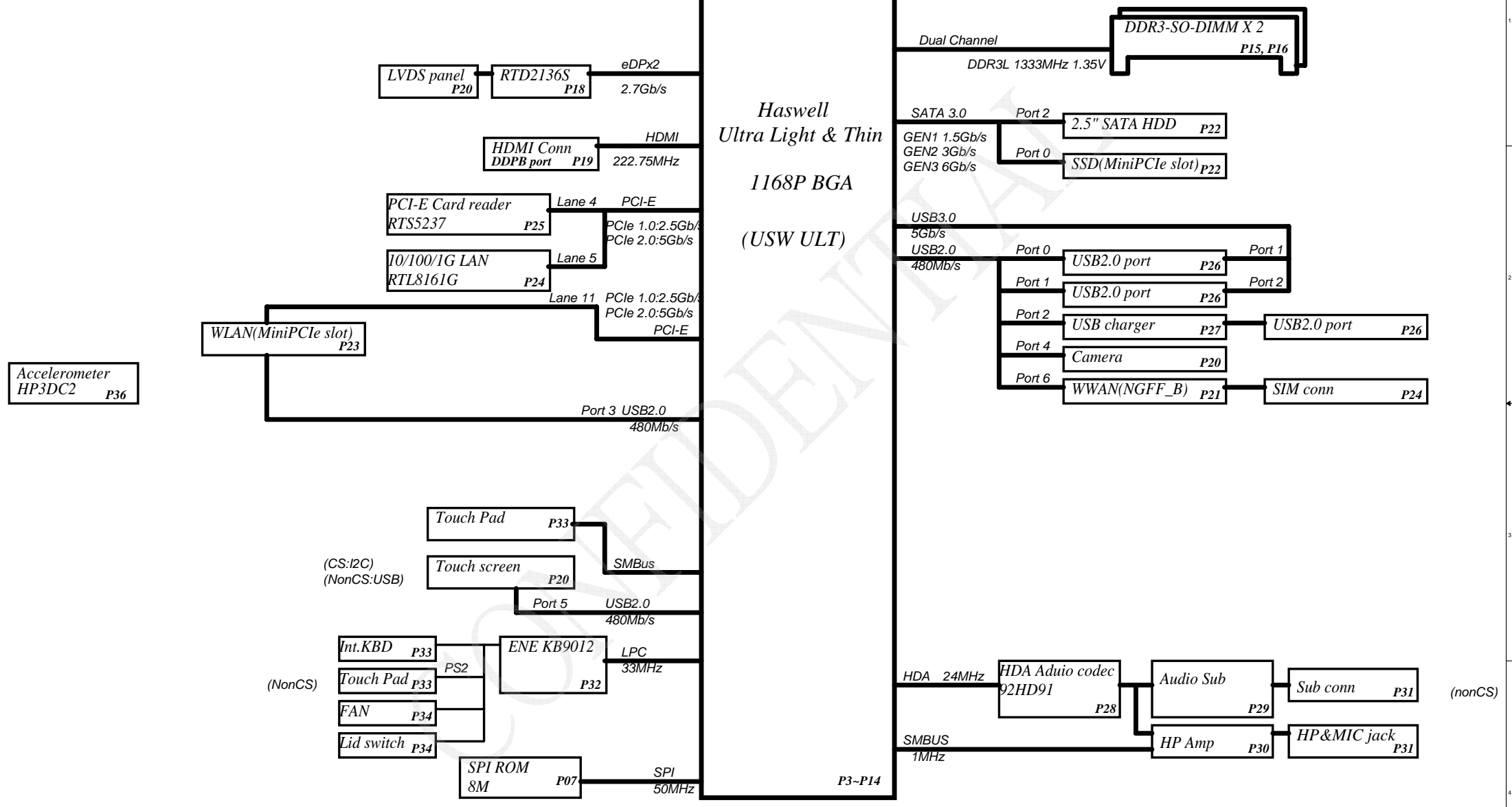
Hasswell M/B Schematics Document

Intel ULV Processor with LPDDR3/DDR3L

Date : 2013/04/10

Version 1.0

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	SCHEMATIC, MB A9315
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				4019LR	A
Date:	Monday, October 21, 2013	Sheet	1	of	49



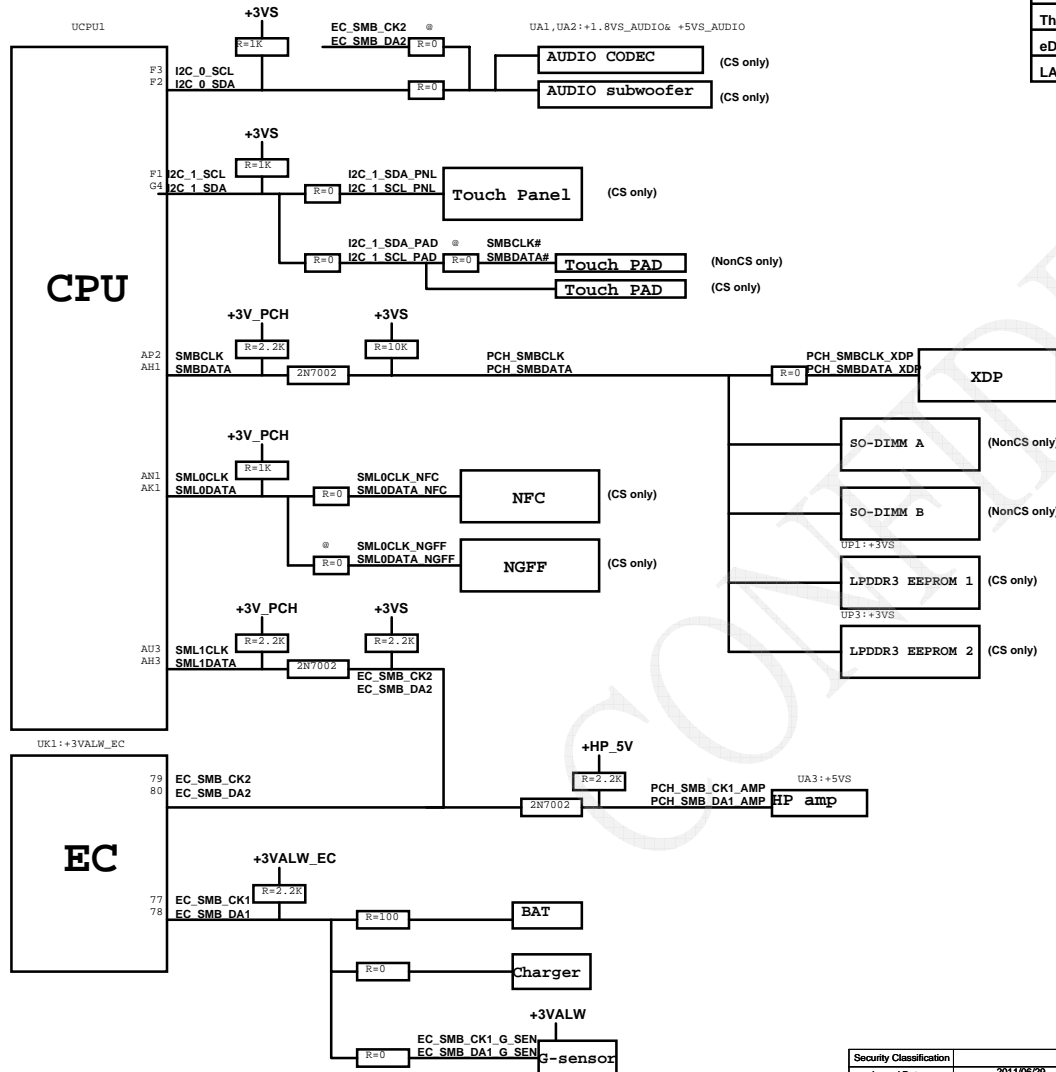
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Document Number	4019LR	Rev	A	Date	Monday, October 21, 2013
Sheet	2	of	49		

Power rail	Control (EC)	Source (CPU)
+RTCVCC	X	X
VIN	X	X
BATT+	X	X
B+	X	X
+VL	X	X
+3VL	X	X
+5VALW	EC_ON	X
+3VALW	EC_ON	X
+3VALW_EC	EC_ON	X
+3V_PCH	PCH_PWR_EN	X
+1.05V	SUSP#	
+1.8V	SYSON	PM_SLP_S5# / PM_SLP_S4#
+1.2V_1.35V	SYSON	PM_SLP_S5# / PM_SLP_S4#
+5VS	SUSP#	PM_SLP_S3#
+3VS	SUSP#	PM_SLP_S3#
+1.8VS	SUSP#	PM_SLP_S3#
+1.5VS	SUSP#	PM_SLP_S3#
+1.05VS	SUSP#	PM_SLP_S3#
+1.05VS_MODPHY	X	MPHY_PWREN
+0.6V_0.675VS	X	SM_PG_CTRL
+VCC_CORE	X	VR12.5_VR_ON

@ is NO SMT part (empty)

<Power gating GPIO,wake ,INT and RST>

Device	Power gating GPIO	Enable (ON)		RST/IRQ	Wake/INT
		CPU	IC HW part		
NGFF SSD	X(Not support)				
NGFF WWAN	X(Not support)				
NGFF WLAN/BT					
WLAN (MiniPCIe) *	GPIO83	H	H	Load switch	GPIO34 * GPIO54 *
USB3.0 CONN	GPIO13	L	L	USB switch	
USB3.0 CONN(Charger)	GPIO43	H	H	USB charger	
Card reader (PCI-E)	GPIO60	H	H	Load switch	GPIO93 GPIO94
USB2.0 Camera	GPIO25	H	H	Load switch	
Touch Panel	GPIO89	H	H	Load switch	GPIO52 GPIO50
Touch Pad -NonCS					
Touch Pad -CS *	GPIO88	L	L	PMOS	GPIO55 *
WWAN	GPIO84	H	H	Load switch	
SATA HDD/SSD	GPIO90	H	H	Load switch	GPIO38 X(Not support)
mSATA	GPIO86	H	H	Load switch	DEVSLP2#/GPIO39
Audio DSP + codec	GPIO76	H	H	Load switch	X(Not support)
Thermal (EC)	X(Not support)				
eDP*	V			Load switch	
LAN (PCI-E)	GPIO12	H	L	Load switch	GPIO91 GPIO92



<USB2.0 port>

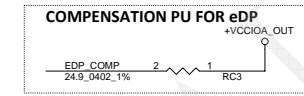
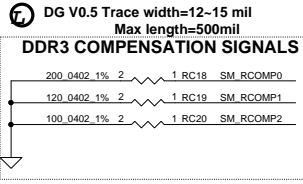
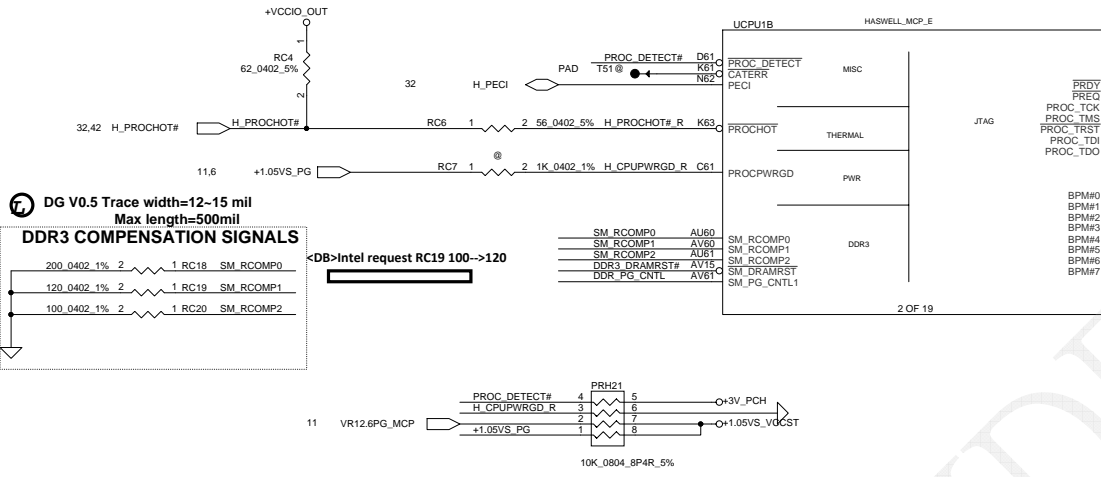
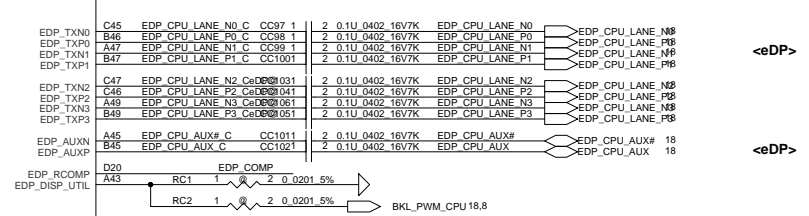
USB2.0 port	DESTINATION	
	CS	NonCS
0	USB 2.0(left side)	USB 2.0(left side)
1	USB 2.0(left side)	USB 2.0(left side)
2	USB 2.0(right side)	USB 2.0(right side)
3	WLAN (NGFF)	WLAN (MiniPCIe)
4	Camera	Camera
5	No contact	Touch screen
6	WWAN	WWAN
7	Finger printer	Finger printer

<PCI-E,SATA,USB3.0>

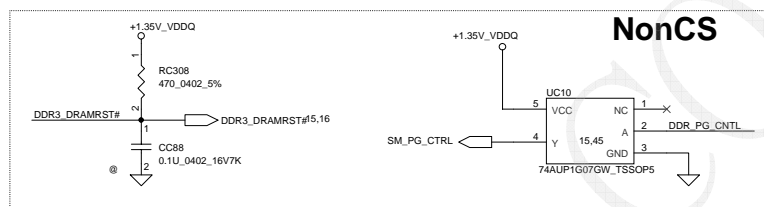
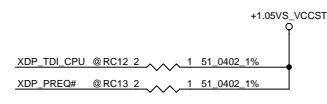
Lane#	PCI-E	SATA	USB3.0	DESTINATION	
				CS	NonCS
1			1	USB3.0	USB3.0
2			2	USB3.0	USB3.0
3	1		3	X(Not support)	X(Not support)
4	2		4	Card reader(PCI-E)	Card reader(PCI-E)
5	3			10/100/1000 LAN	10/100/1000 LAN
6	4				
7					
8					
9	5				
10					
11		3		WLAN (NGFF)	WLAN (MiniPCIe)
12		2			
13	6	1		2.5"HDD	2.5"HDD
14		0		SSD(mSATA)	SSD(mSATA)



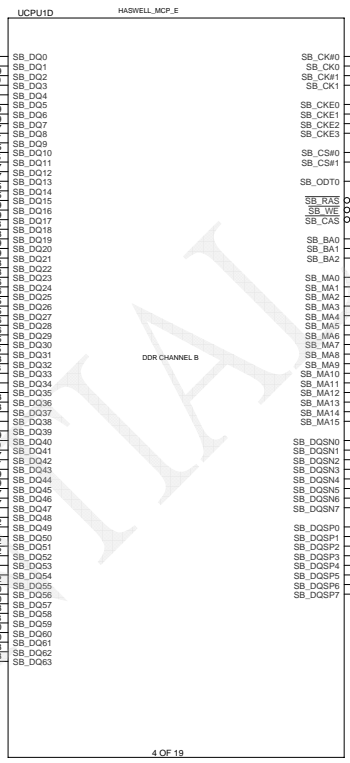
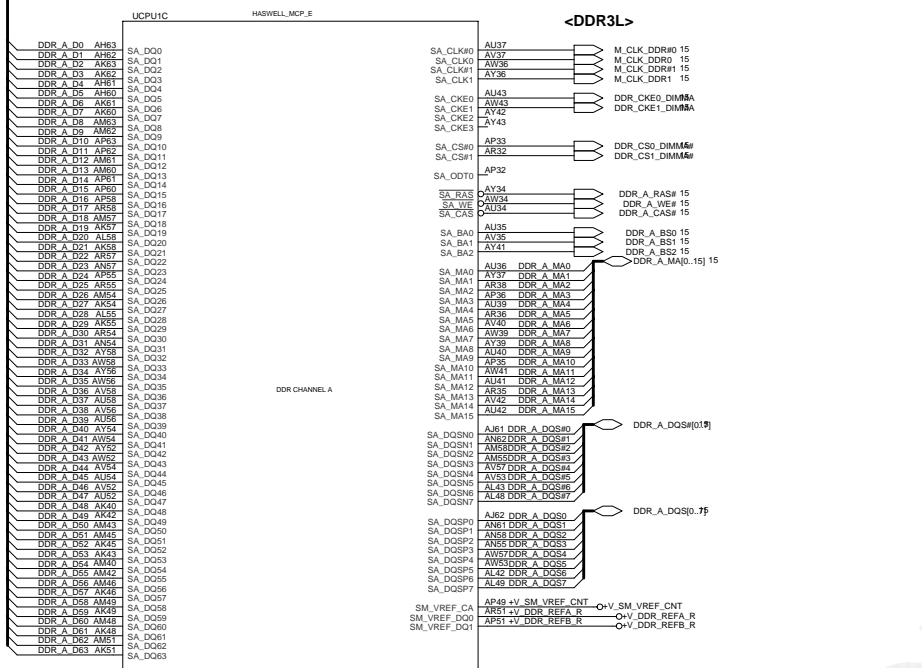
CC97-CC102 must be closed to connector not CPU



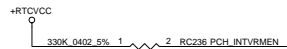
DG V0.9 PEG_COMP Trace width=20mil and spacing=25mil Max length=100mil



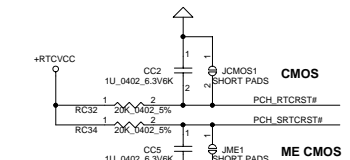
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Document Number	4019LR		Rev A	
Date	Monday, October 21, 2013		Sheet 4 of 49	



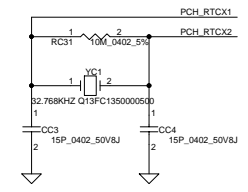
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Date: Monday, October 21, 2013				Sheet 5 of 49



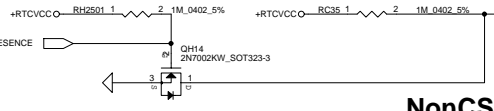
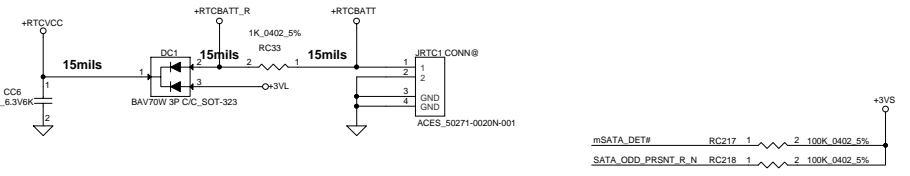
INTVTRMEN
 * H : Integrated VRM enable
 L : Integrated VRM disable



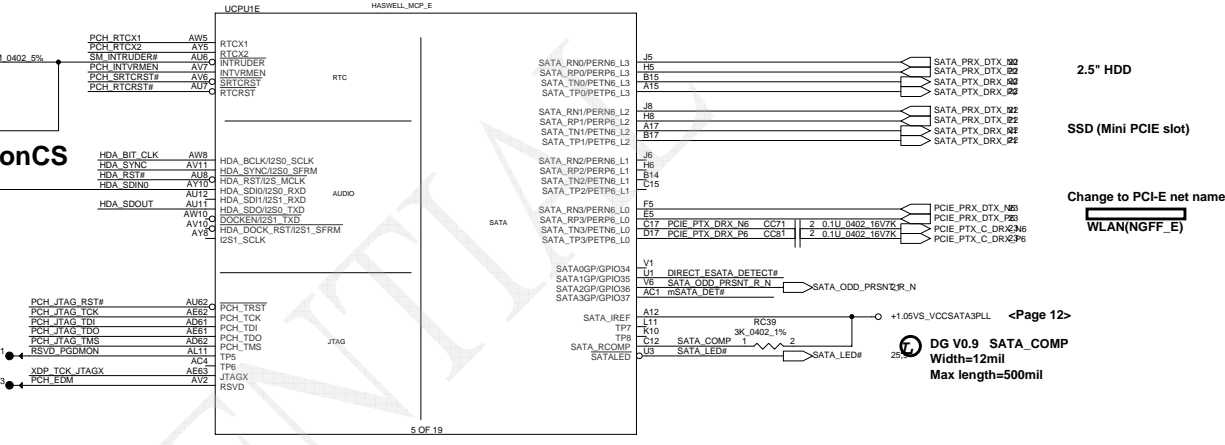
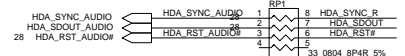
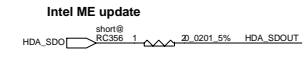
NonCS



RTC BAT conn



NonCS



2.5" HDD

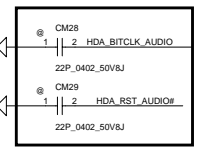
SSD (Mini PCIE slot)

Change to PCI-E net name
WLAN(NGFF_E)

R3d

R4

9/17 add RF solution



R5

<XDP>

<PCH site>

<PCH site>

<XDP>

<PCH site>

<XDP>

XDP_TCK:XDP contact with CPU No 0ohm(R55)

<PCH site>

<PCH site>

<PCH site>

Contact ok

<CPU site>

<CPU site>

<CPU>

<XDP>

<PCH site>

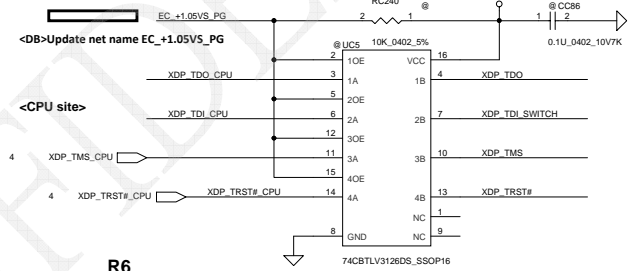
<PCH site>

<CPU and XDP>

<CPU and XDP>

<CPU and XDP>

<XDP>



<DB>Update net name EC_+1.05VS_PG

<CPU site>

<CPU site>

<CPU site>

<CPU site>

<CPU>

<XDP>

<PCH site>

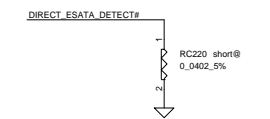
<PCH site>

<CPU and XDP>

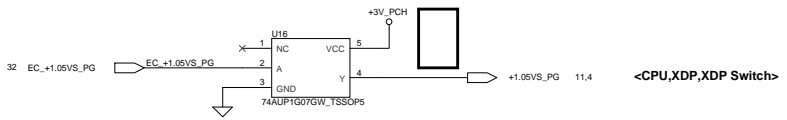
<CPU and XDP>

<CPU and XDP>

<XDP>



SI# 2012.11.01 Change PH to R-PAK in page 4



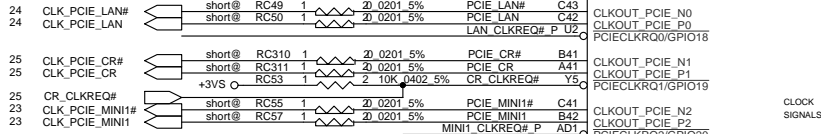
<EC output>

<CPU,XDP,XDP Switch>

Topolog	Description	Best Use for	Resistors Stuffed	Resistors uStuffed
Default Setting: Dual TCK Scan Chains (also known as "Shared JTAG" in other document)	In this topology, the CPU JTAG chain will be controlled by TCK0 and TCK1 will control the PCH JTAG chain.	- Run control oper. - ME/Sx debug	R1d,R2,R3d, R4,R5,J1d J2d,J3d* J4d and Rs5*	J1s, J2s, J3s R6,R7,R8,R9
Single TCK scan chain (also known as "Common JTAG" in other document)	In this topology, PCH TDI-TDO and CPU TDI-TDO will be chained to form one JTAG scan chain controlled by TCK0	- Boundary Scan/ Manufacturing est	J1s,J2s,J3s** R2,R4,R5,R5s**	R1d,r3d,J1d,J2d J3s** ,J4d, R6,R7,R8,R9

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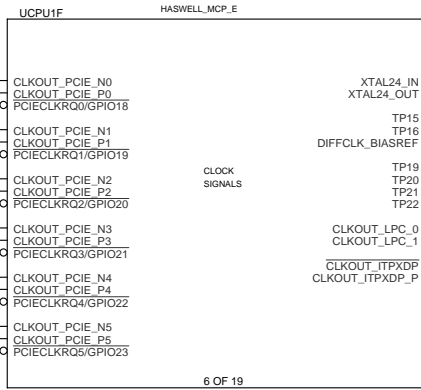
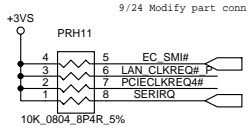
PCIE LAN



PCIE Card reader

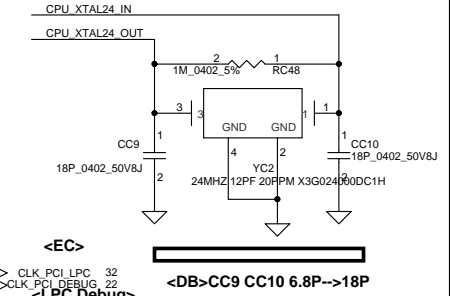
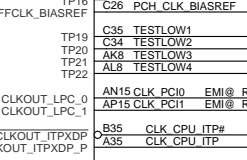
WLAN

Vince/29 remove for UMA only



CPU_XTAL24_IN

CPU_XTAL24_OUT



<Page12>

<EC>

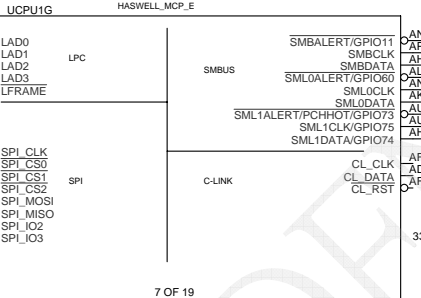
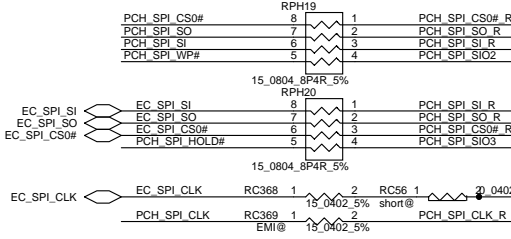
<DB>CC9 CC10 6.8P-->18P

<LPC Debug>

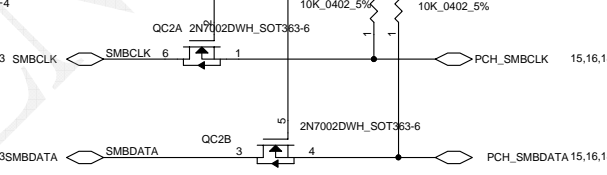
<XDP CLK reserve TP>

<DB>Add XDP CLK

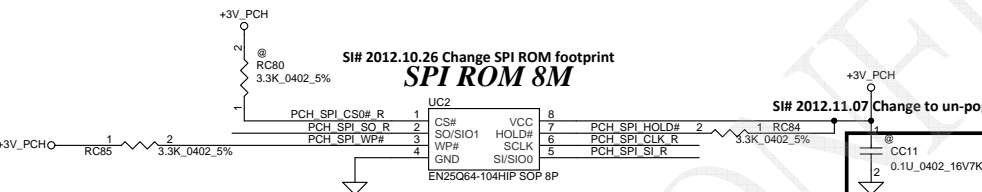
SI# 2012.10.25 Change SPI ROM damping to R-PAK



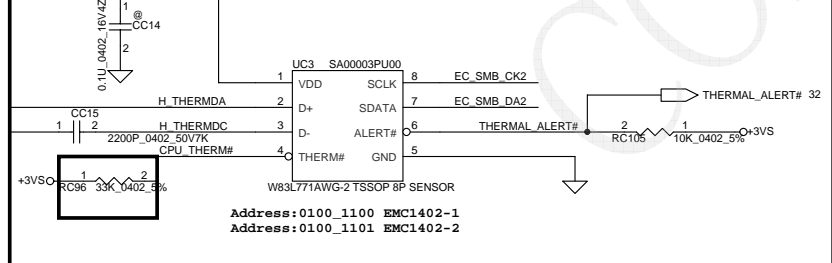
<DB>No sensor hub



SI# 2012.10.30 Support quad IO function
SI# 2012.11.12 Change power rail to +3V_PCH for ENE fix code

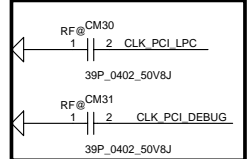


CPU THERMAL SENSOR



9/13 change RC96 10K to 33K for EC
Thermal sensor SMBus address -->0111_100xb (0x78h)

Table with columns: Security Classification, Issued Date, Deciphered Date, Title, and Document Number. Includes Compal Secret Data and SCHEMATIC, MB A9315.



PV# 2013.01.31 Pop CM30,CM31 to solve RF issue

PV# 2013.01.30 Add test point

DSWODVREN - On Die DSW VR Enable

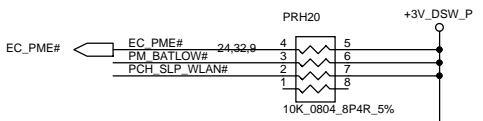
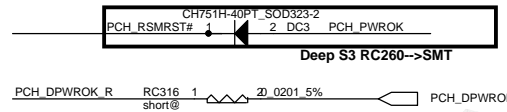
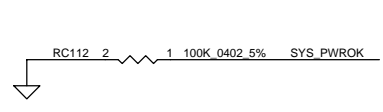
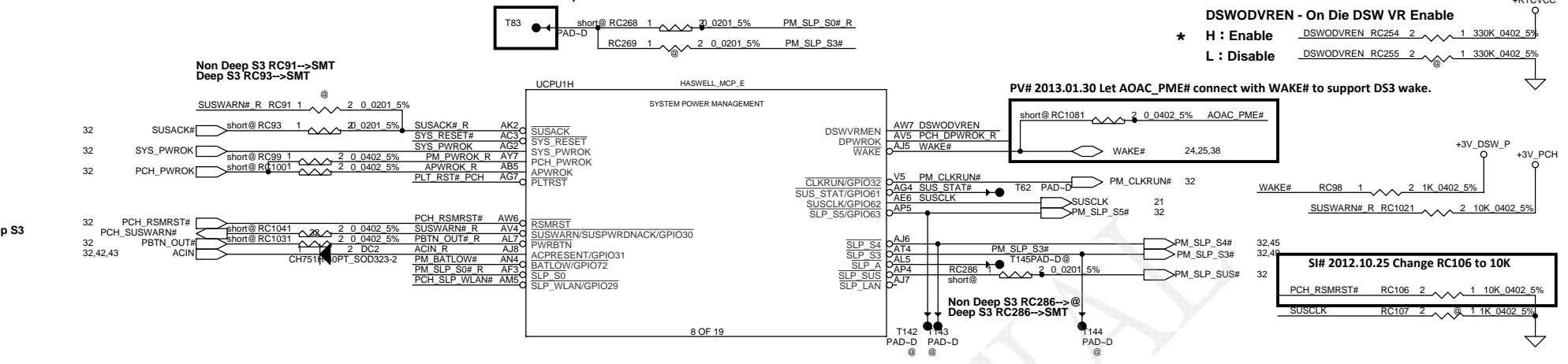
* H : Enable DSWODVREN RC254 2 1 330K 0402 5%
 L : Disable DSWODVREN RC255 2 1 330K 0402 5%

Non Deep S3 RC91-->SMT
 Deep S3 RC93-->SMT

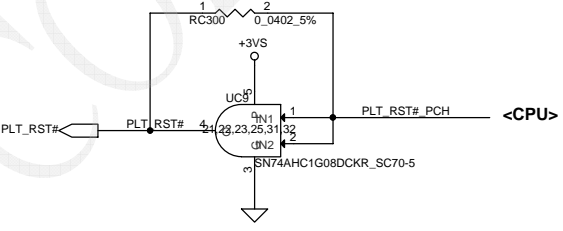
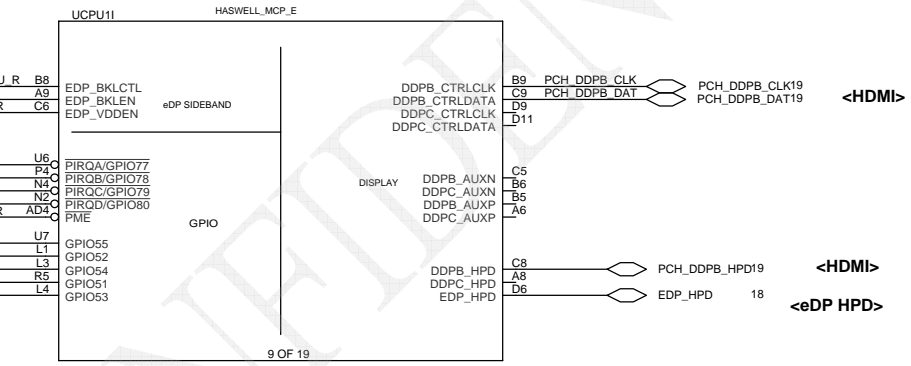
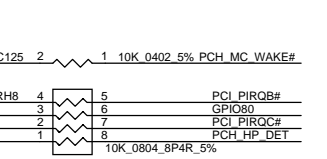
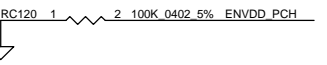
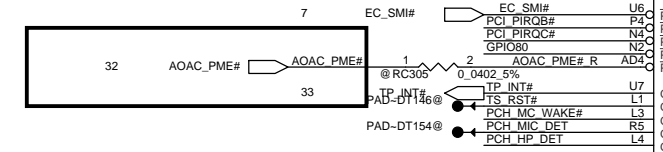
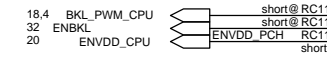
PV# 2013.01.30 Let AOAC_PME# connect with WAKE# to support DS3 wake.

Deep S3

SI# 2012.10.25 Change RC106 to 10K



PANEL_BKEN_CPU PD 100K on Page20



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				Custom	A
				Date	Monday, October 21, 2013
				Sheet	8 of 49

9/12 reserve EC_FB_CLAMP_TGL_REQ# on GPIO16
 9/12 reserve DGPU_GC6_EN on GPIO17

9/13 remove EC_FB_CLAMP_TGL_REQ# for UMA only

9/12 reserve DGPU_HOLD_RST# on GPIO58

No sensor hub
 No sensor hub

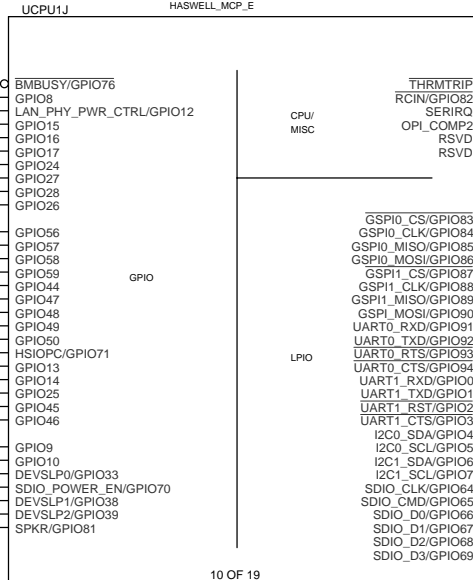
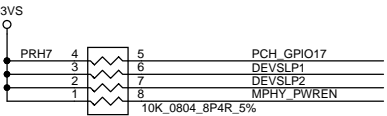
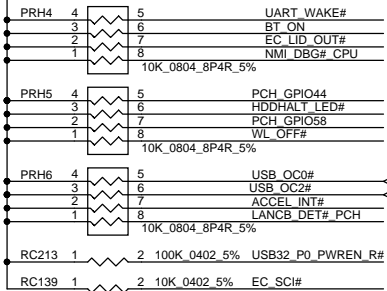
No sensor hub

<DB>CS only PCH_HP_DET#

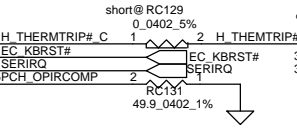
PCH_GPIO81(HDA_SPKR):NonCS only

SI# 2012.10.25 Change ACCEL_INT#(PCH_GPIO80) to GPIO46

+3V_PCH



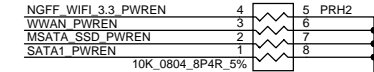
DG V0.9 PCH_OPIRCOMP
 Width=12mil,spacing=12mil
 Max length=500mil



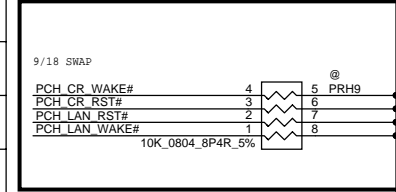
9/13 remove EC_FB_CLAMP_TGL_REQ# for UMA only

Boot BIOS Strap

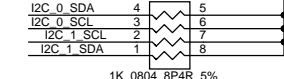
PCH_GPIO86	Boot BIOS Location
0	SPI



	GPIO47 LPDDR3_ID1	GPIO48 LPDDR3_ID2	GPIO49 LPDDR3_ID3
Hynix 8G/1600 H9CCNNN8JTMLAR	0	0	0
Samsung 8G/1600 K4E8E304EB-EGCE	0	0	1
Elpida 8G/1600 EDF8132A1MC-GD-F	0	1	0



SI# 2012.11.07 Change RC360,PRH9,RC290 to un-pop



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			Rev A Sheet 9 of 49

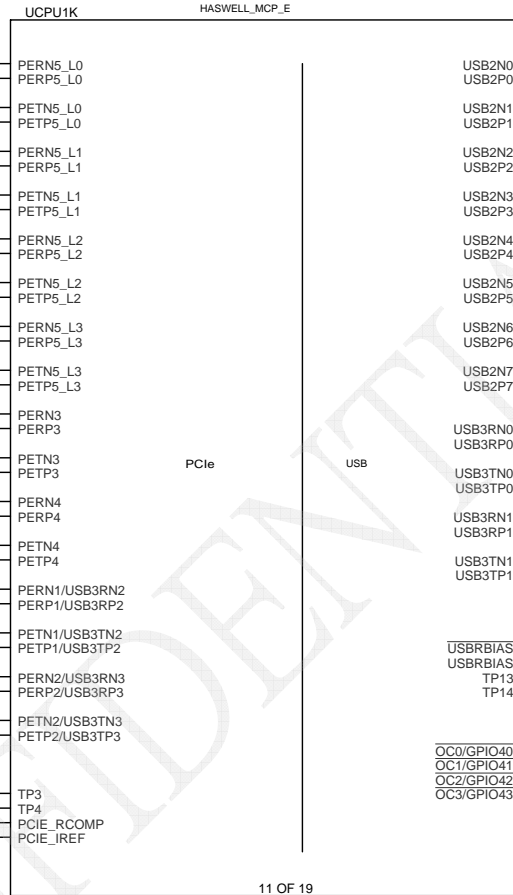
Vince8/29 remove for UMA only

10/100/1G LAN

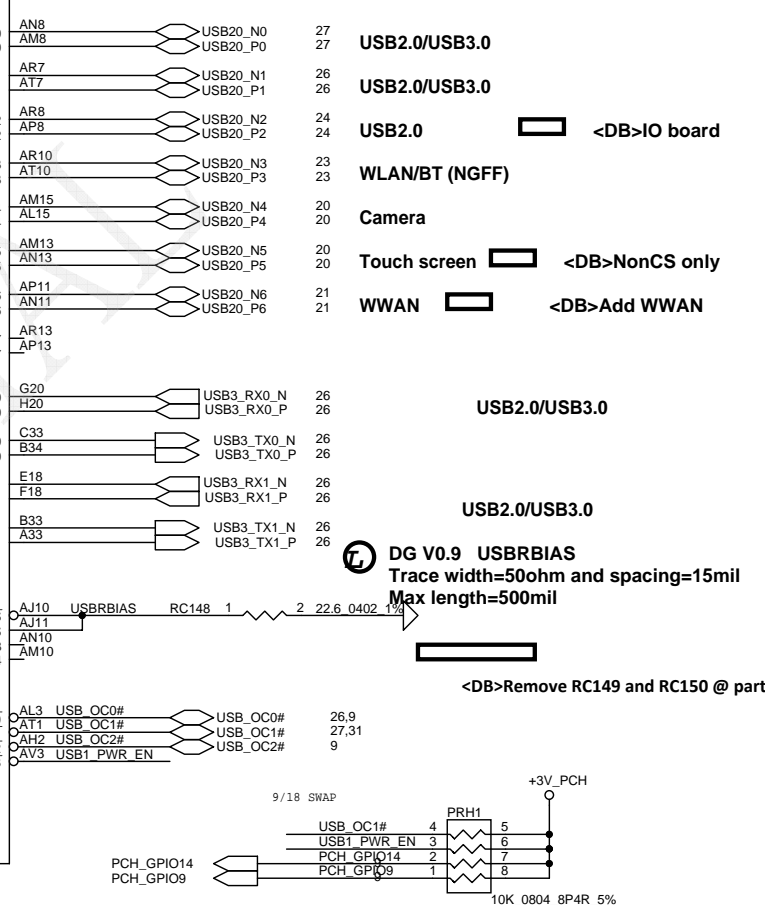
PCI-E Card reader

<Page12>

DG V0.9 PCIE_RCOMP
 Width=12mil,spacing=12mil
 Max length=500mil

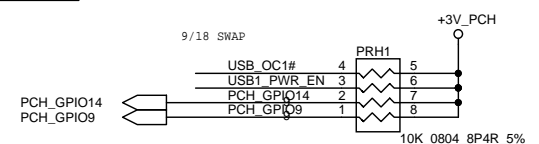


11 OF 19



DG V0.9 USBRBIAS
 Trace width=50ohm and spacing=15mil
 Max length=500mil

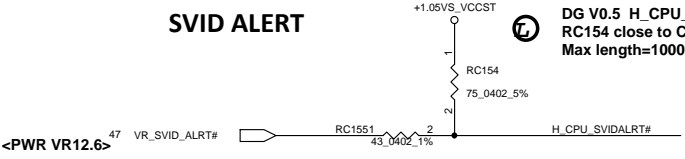
<DB>Remove RC149 and RC150 @ part



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Date:	Monday, October 21, 2013	Sheet	10	of	49

+VCC_CORE@1000mA

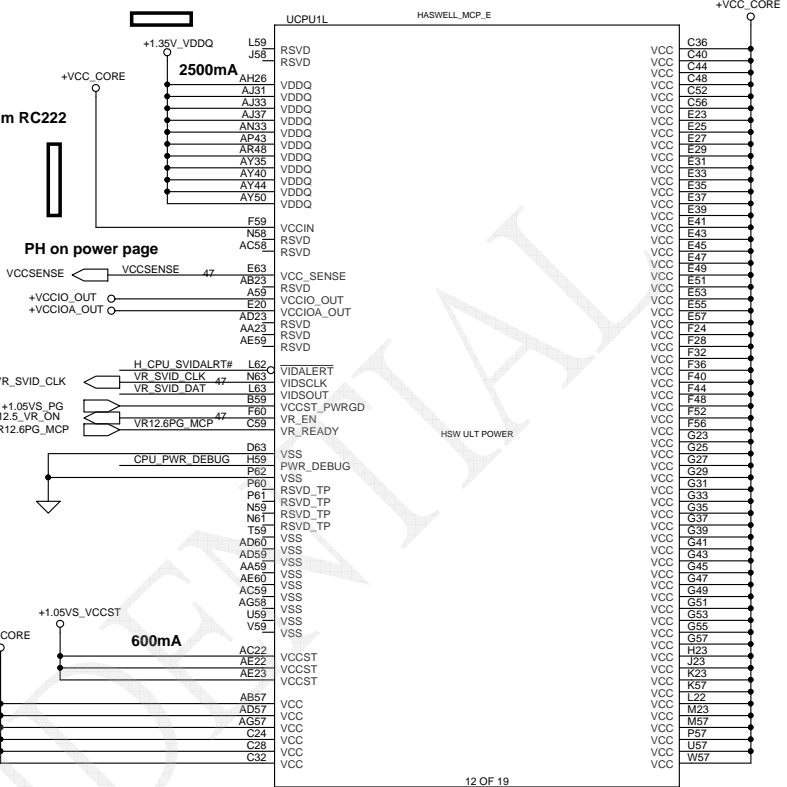
SVID ALERT



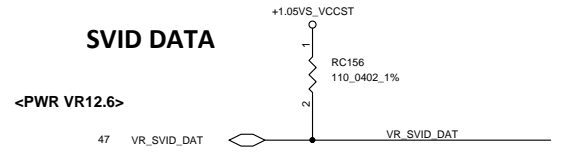
DG V0.5 H_CPU_SVIDALRT#
 RC154 close to CPU-300mil
 Max length=1000-2000mil

VCC_SENSE

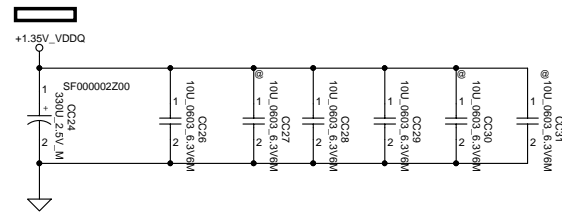
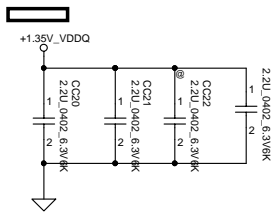
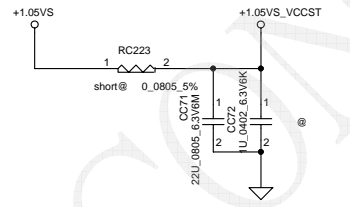
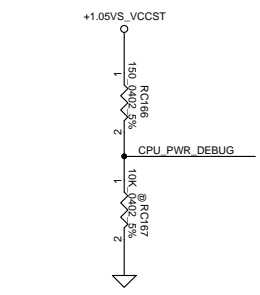
<PWR VR12.6>
<VR IV and CPU>
<EDP_COMP power rail>



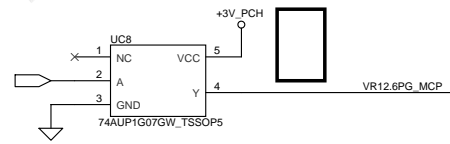
SVID DATA



DG V0.5 VIDSOUT
 RC156 close to CPU-500mil
 Max length=1000-2000mil

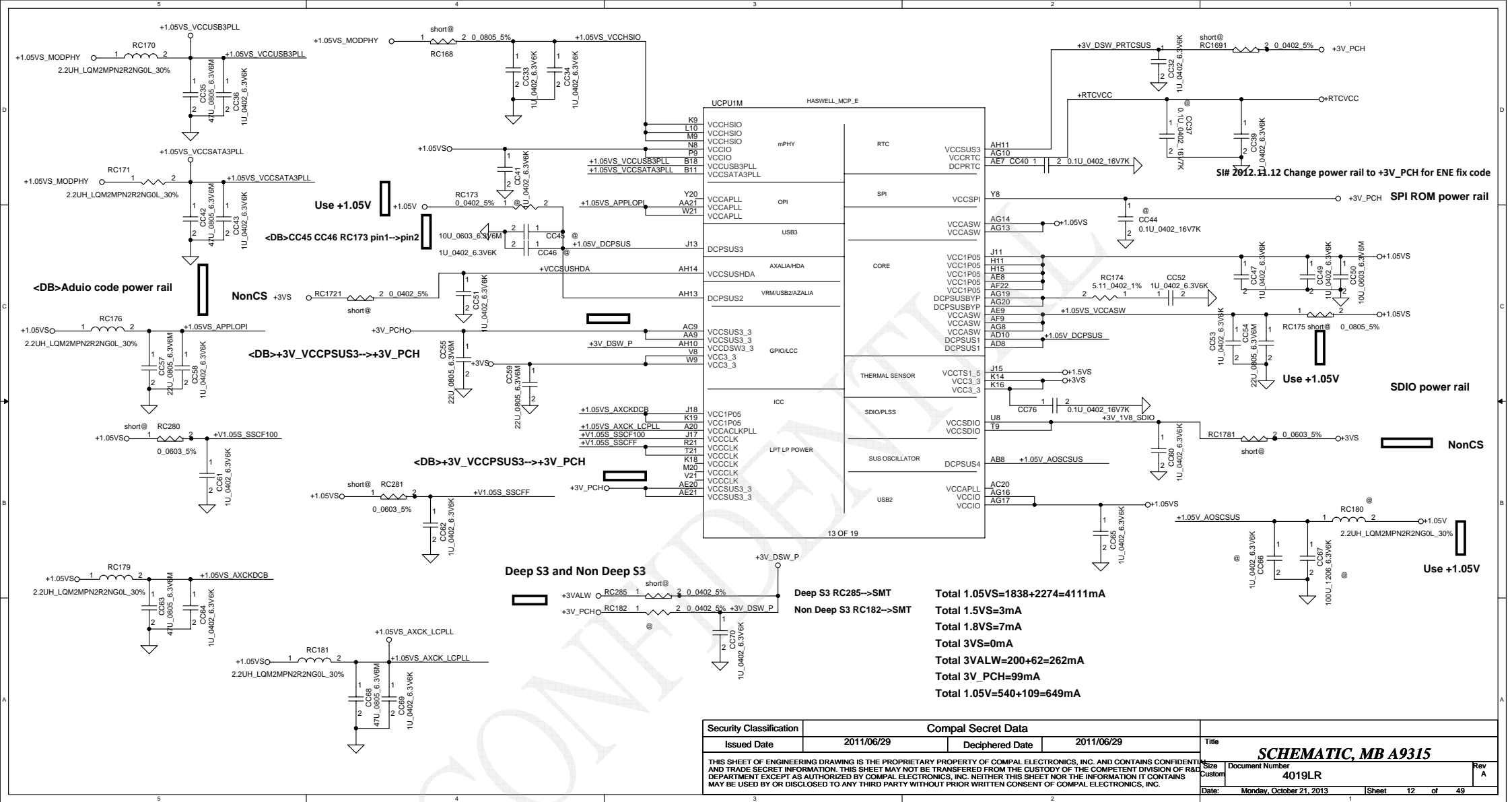


SI# 2012.11.01 Change PH to R-PAK in page 4



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				Custom	4019LR
				Date:	Monday, October 21, 2013
				Sheet	11 of 49
				Rev	A

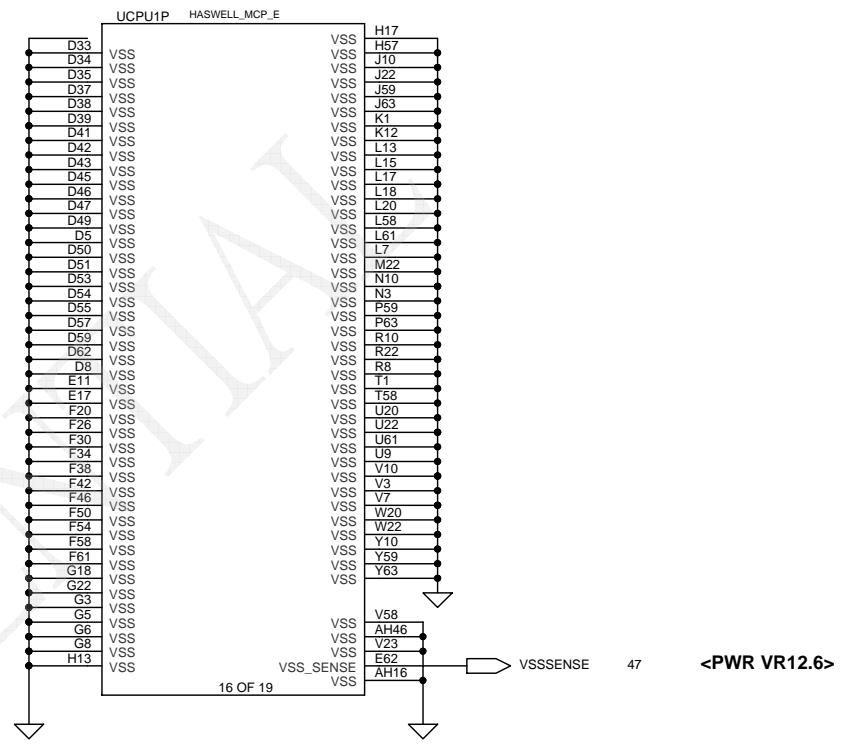
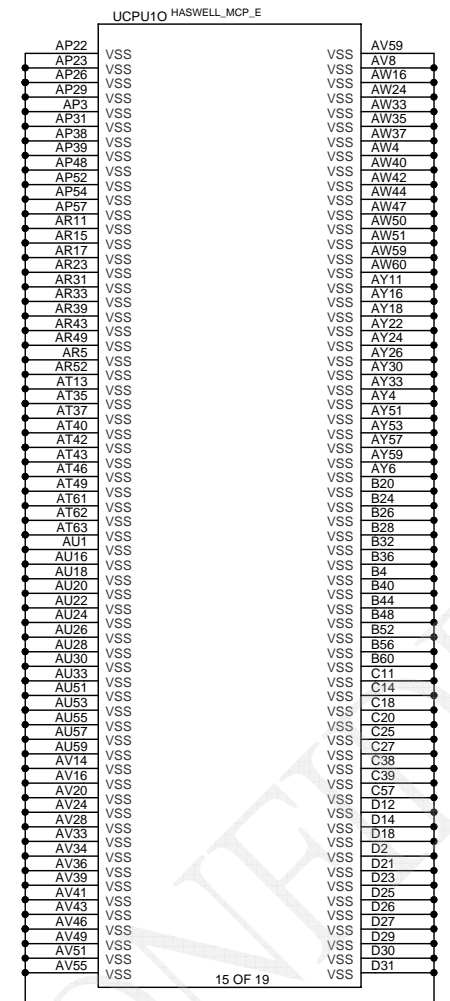
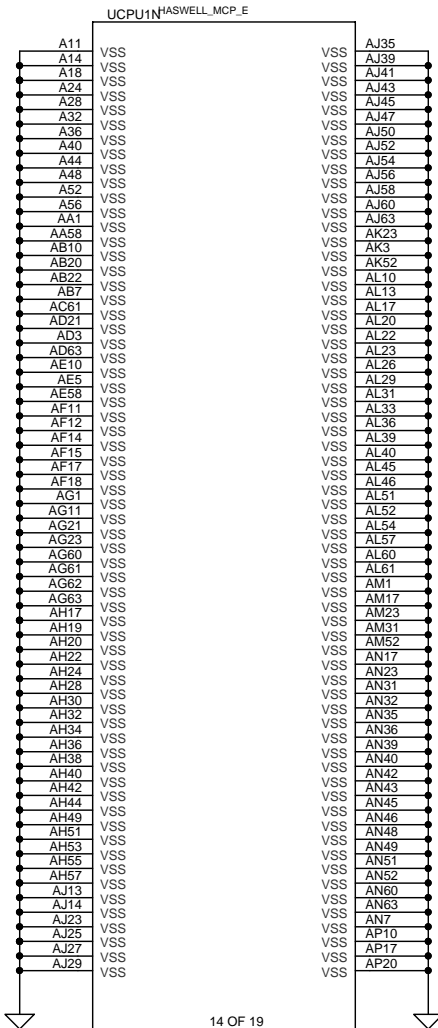
SCHEMATIC, MB A931S



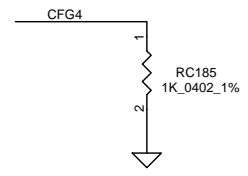
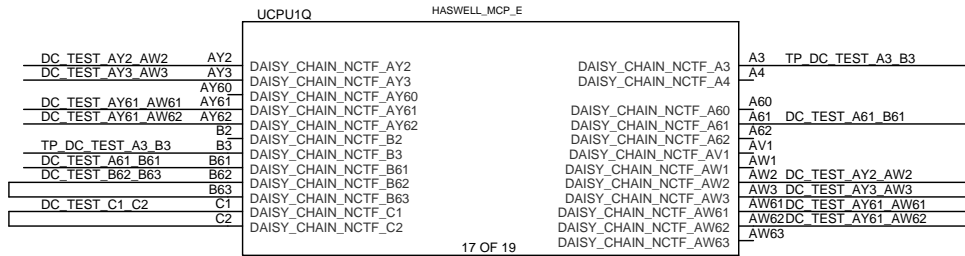
Deep S3 and Non Deep S3

Deep S3 RC285-->SMT	Total 1.05VS=1838+2274=4111mA
Non Deep S3 RC182-->SMT	Total 1.5VS=3mA
	Total 1.8VS=7mA
	Total 3VS=0mA
	Total 3VALW=200+62=262mA
	Total 3V_PCH=99mA
	Total 1.05V=540+109=649mA

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			Rev A	Sheet 12 of 49



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Date: Monday, October 21, 2013				Sheet 13	of 49

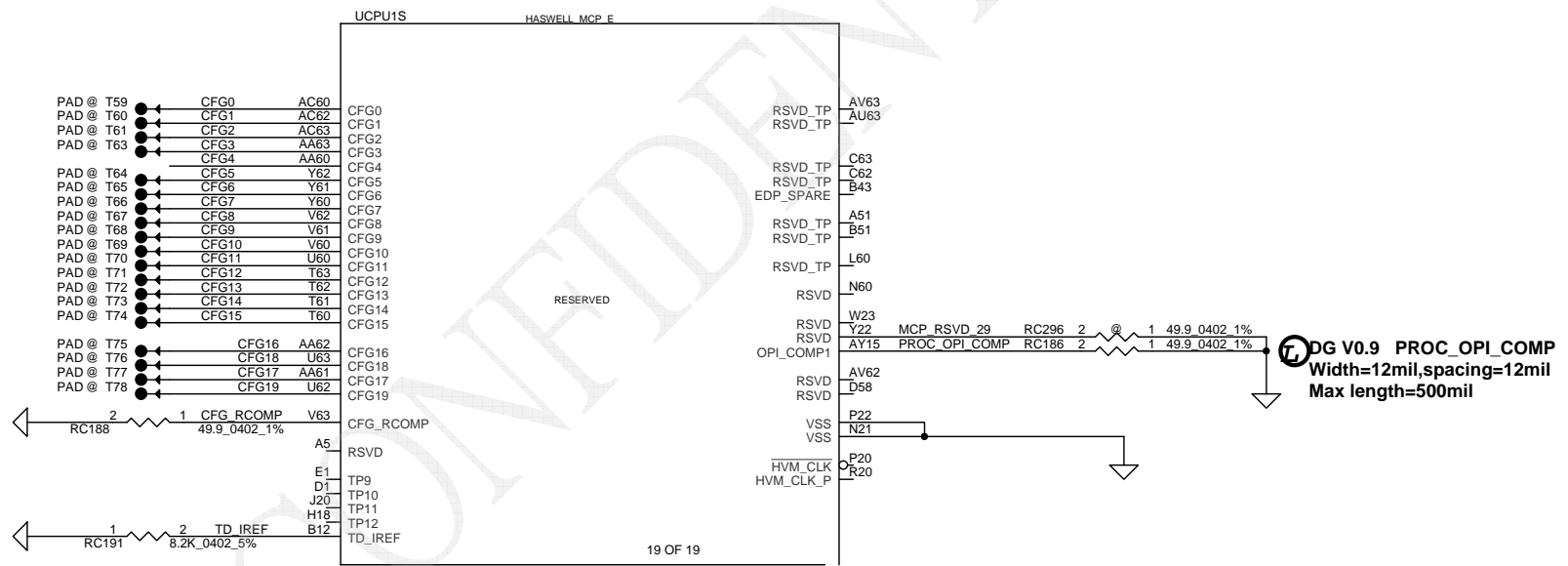
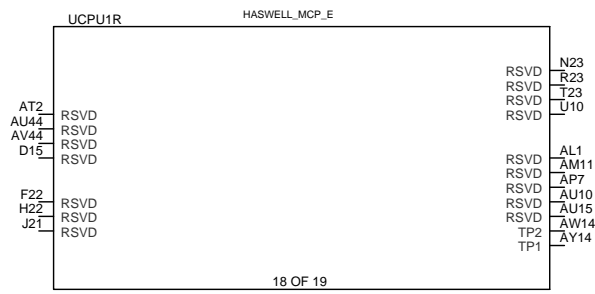


Display Port Presence Strap

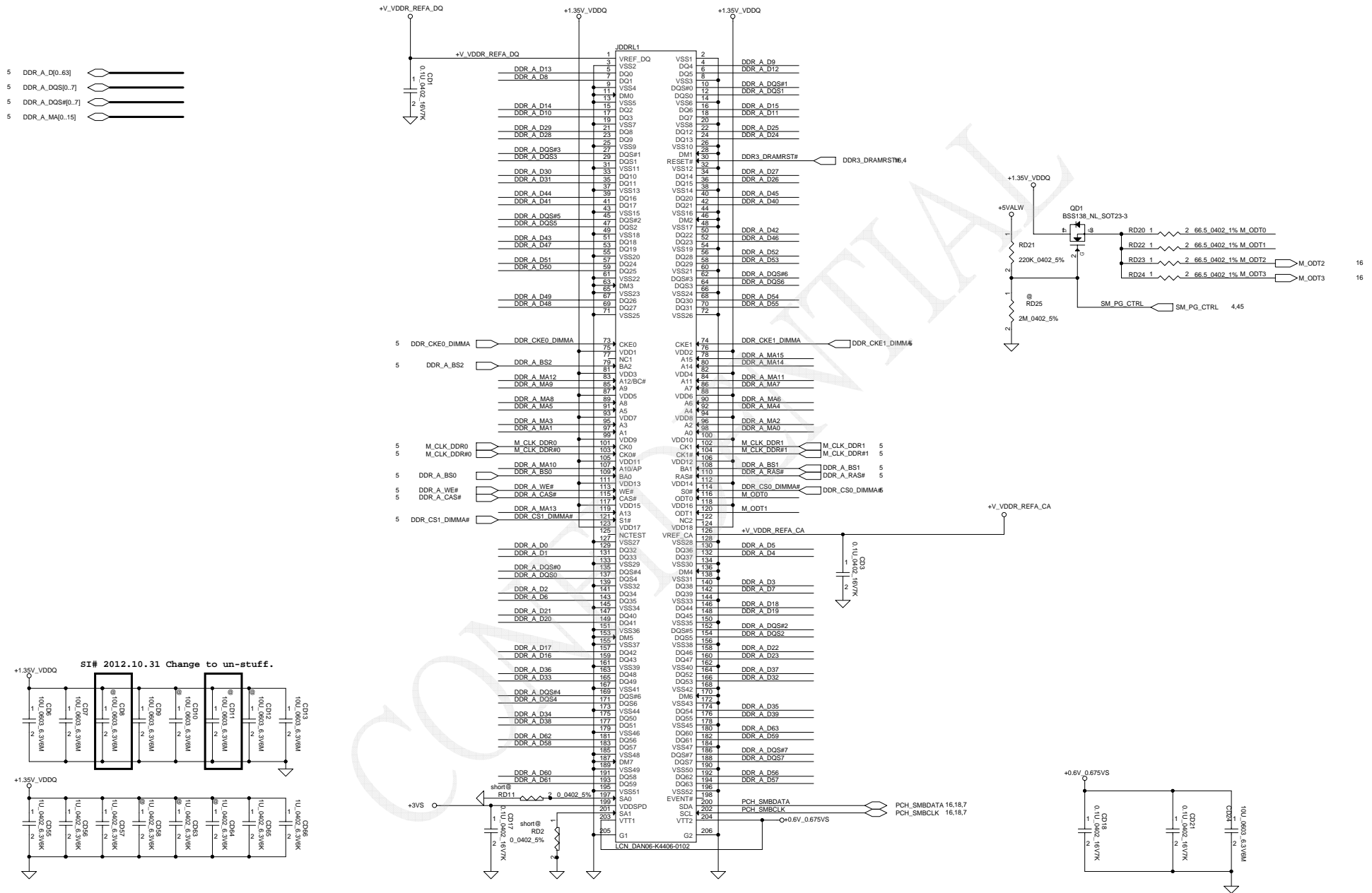
CFG4

1 : Disabled; No Physical Display Port attached to Embedded Display Port

*** 0 : Enabled; An external Display Port device is connected to the Embedded Display Port**

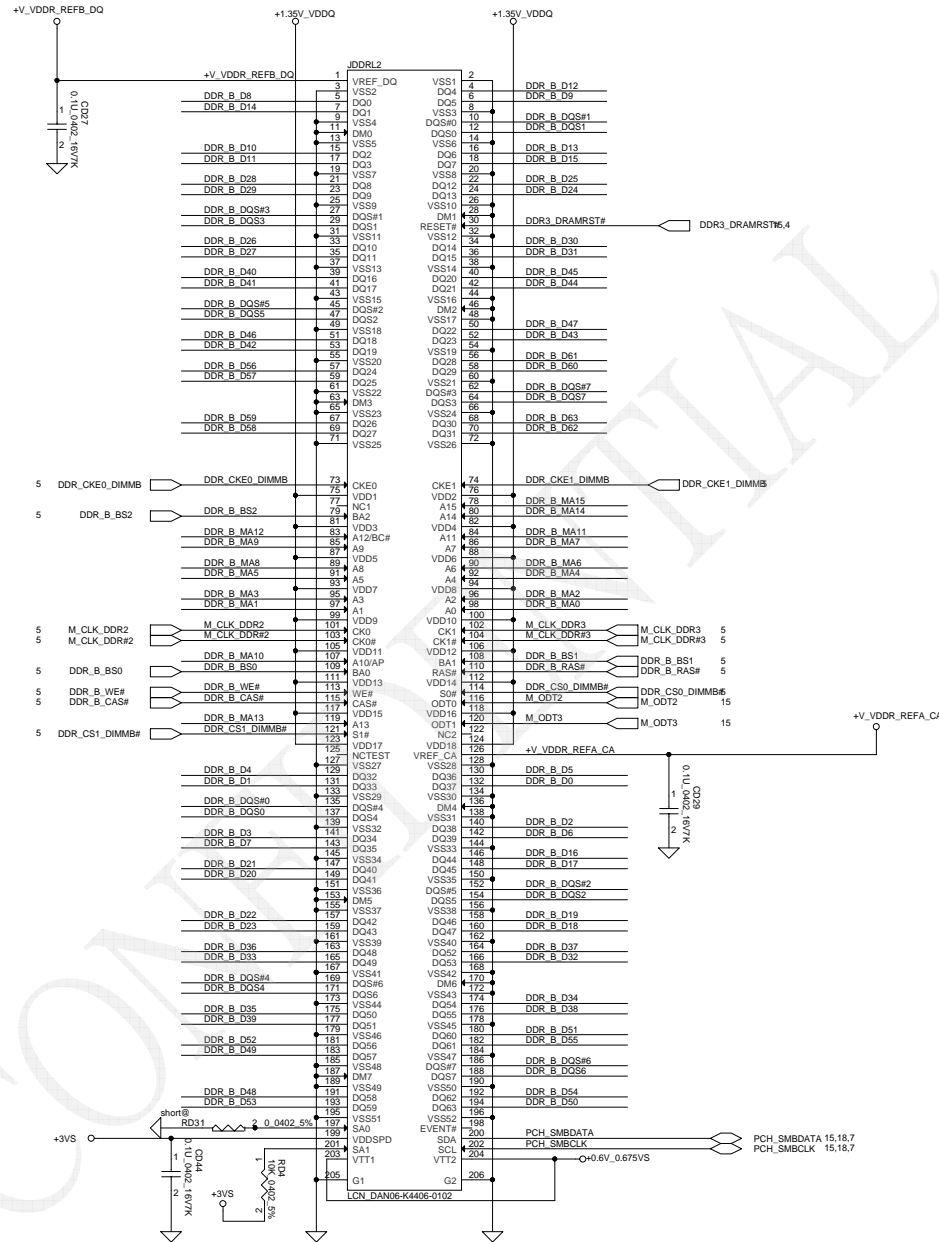


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Date:	Monday, October 21, 2013	Sheet	14	of	49

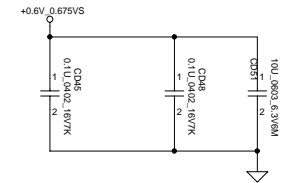
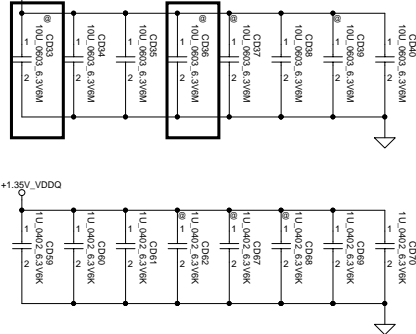


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Date:	Monday, October 21, 2013	Sheet:	15 of 49

- 5 DDR_B_D[0..63]
- 5 DDR_B_DQS[0..7]
- DDR_B_DQS#
- 5 DDR_B_MA[0..15]

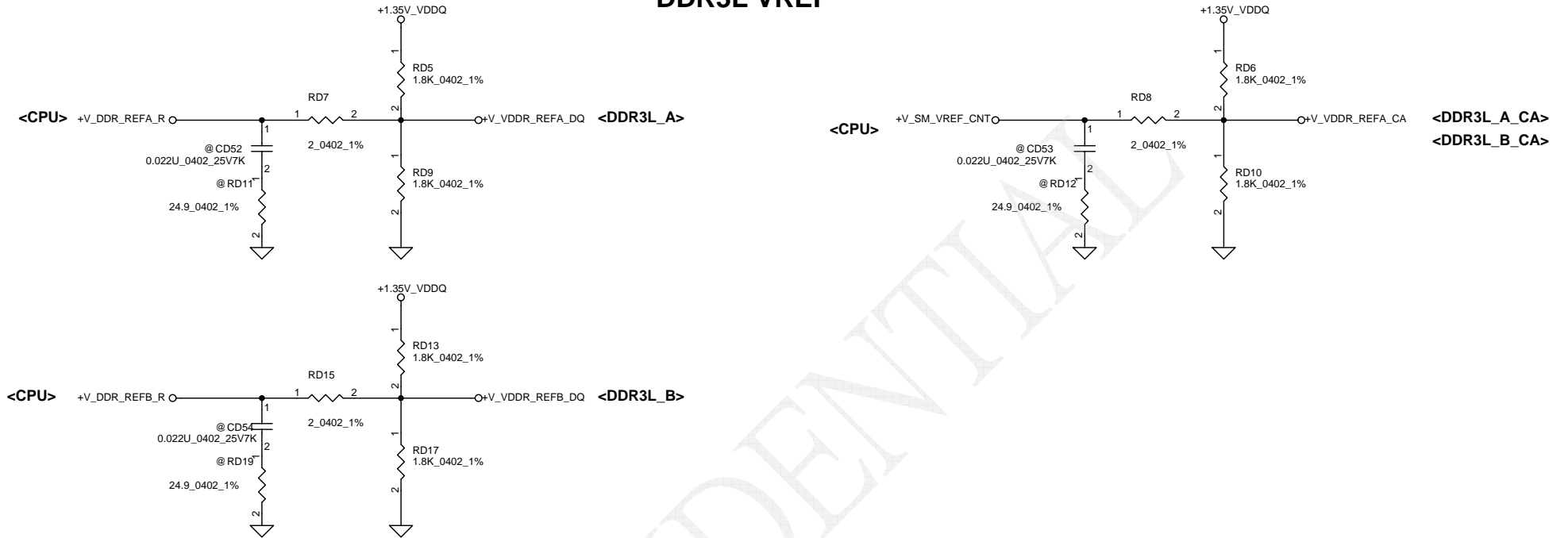


+1.35V_VDDQ SI# 2012.10.31 Change to un-stuff.



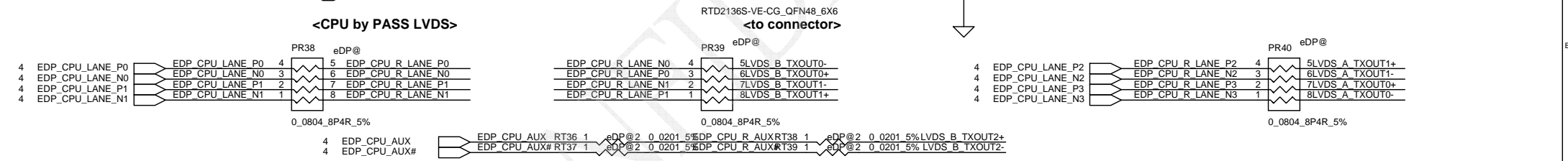
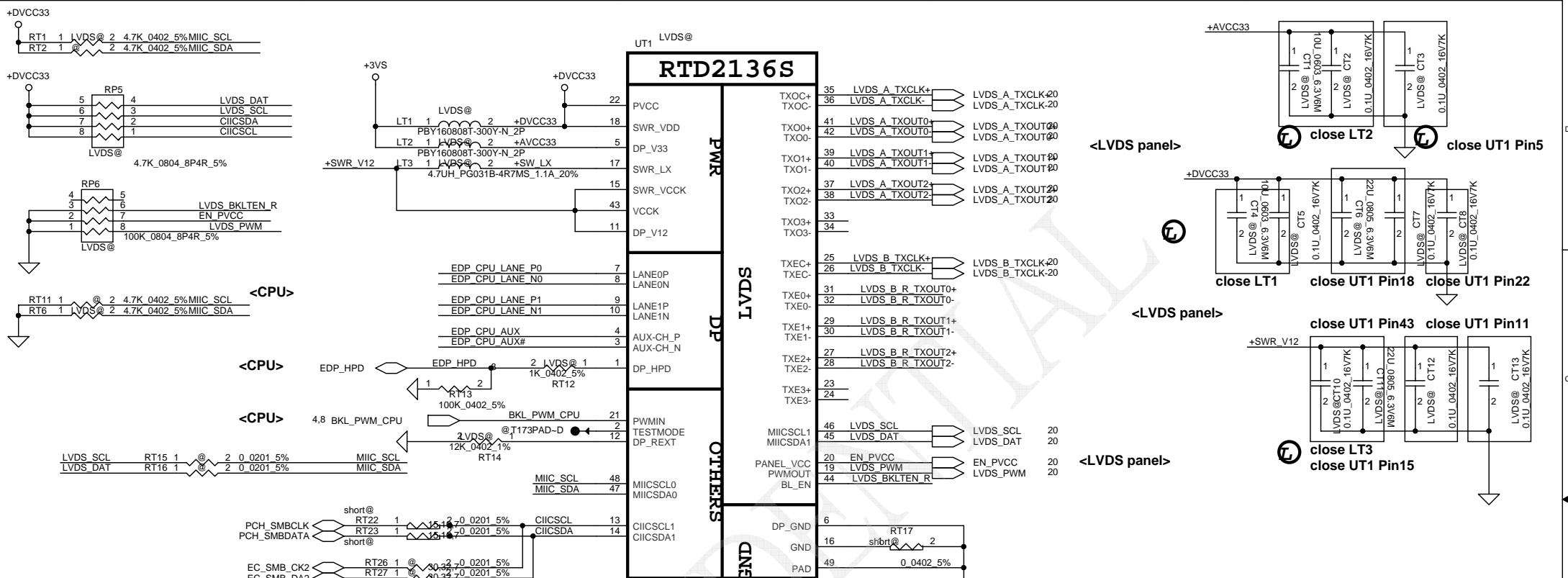
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Date:	Monday, October 21, 2013	Sheet	16	of 49

DDR3L VREF



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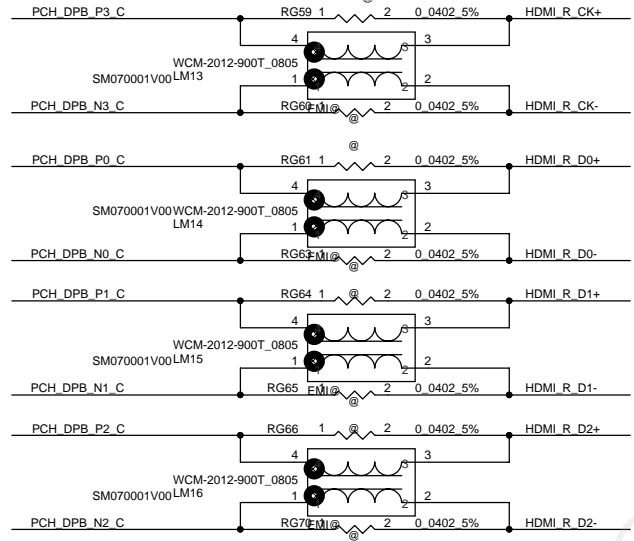
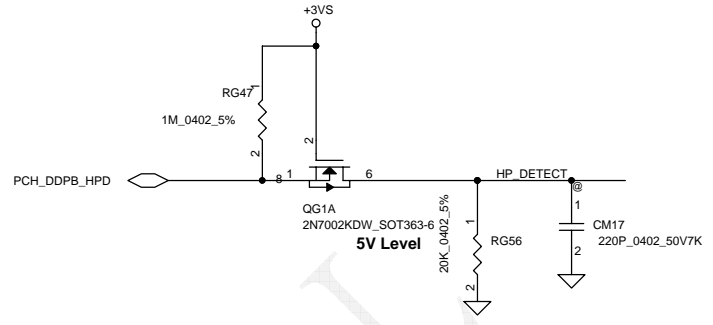
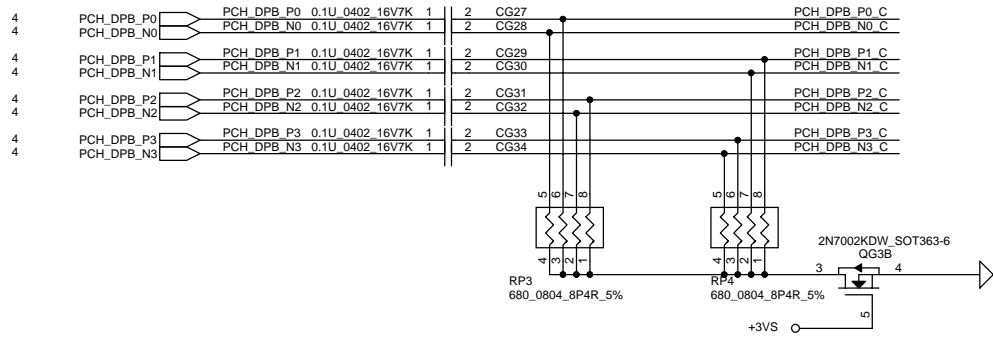
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				Date	Monday, October 21, 2013
				Sheet	17 of 49



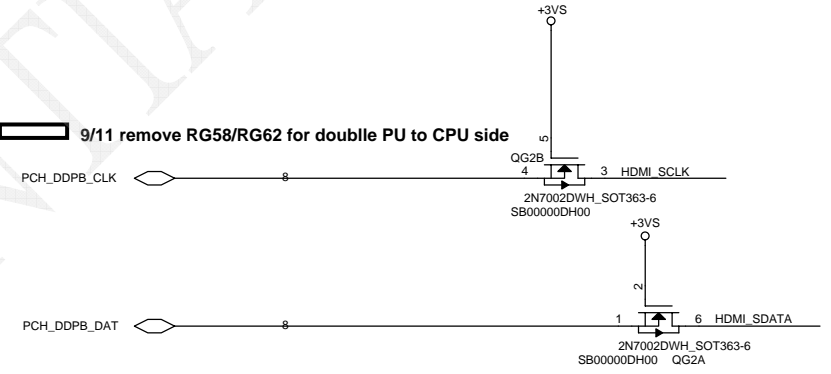
SI# 2012.10.25 Change UT3 footprint



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Size B	Document Number	Date:		Sheet
	4019LR	Monday, October 21, 2013		18 of 49

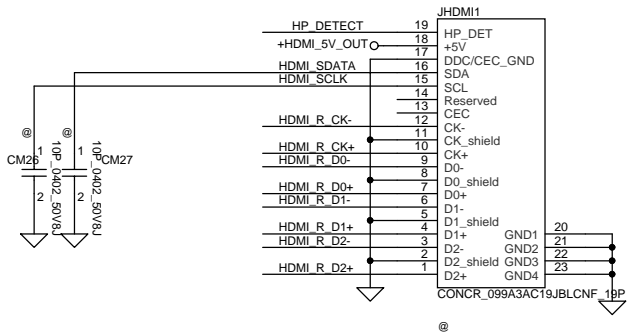
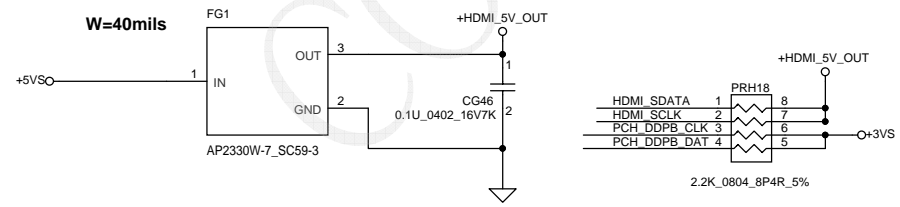


9/11 remove RG58/RG62 for double PU to CPU side



5V PULL UP IN CONNECTER SIDE

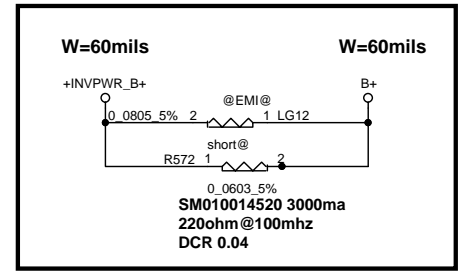
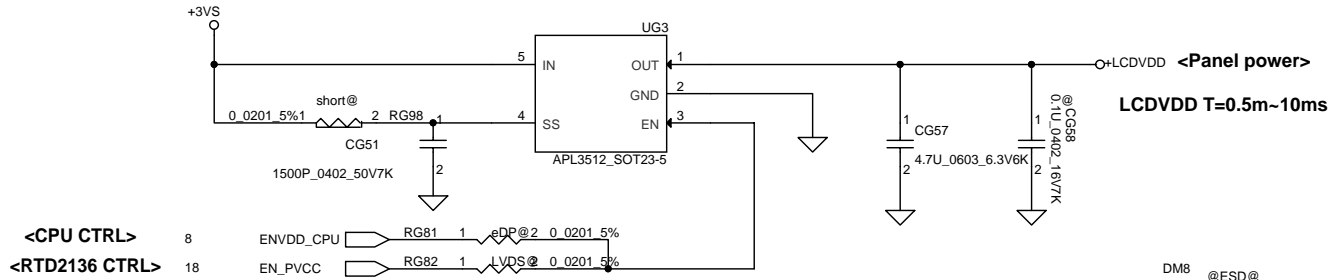
HDMI Conn.



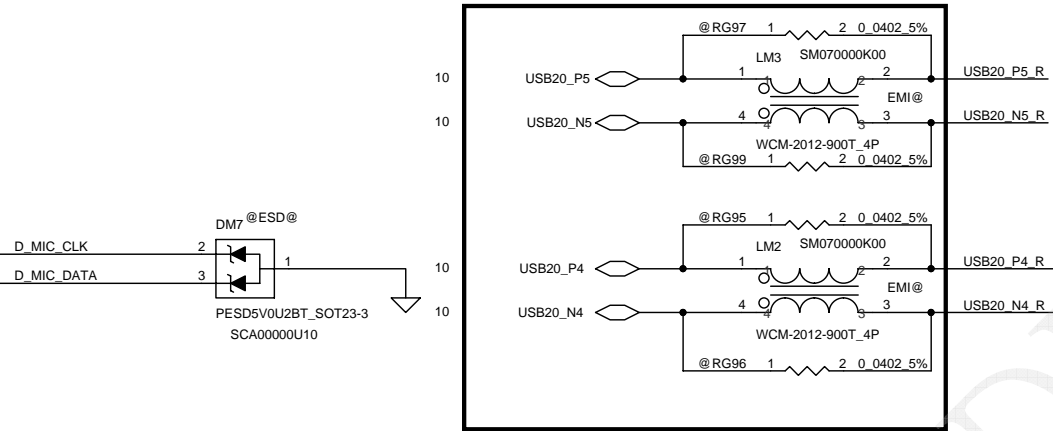
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Date: Monday, October 21, 2013				Sheet 19 of 49	

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SCHEMATIC, MB A9315

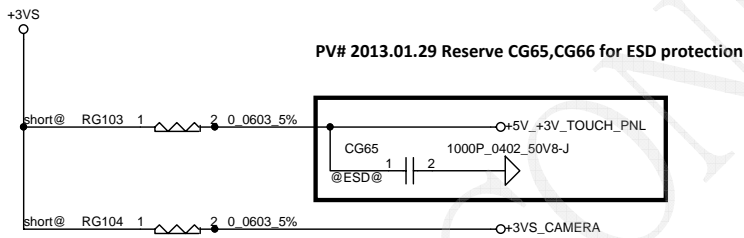
Rev A



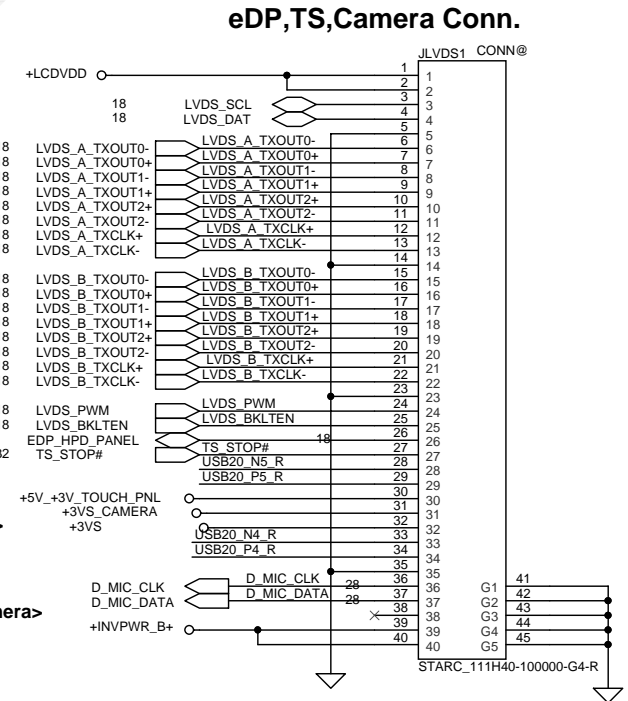
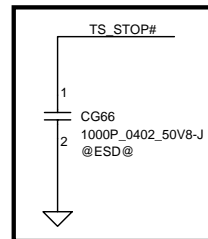
PV# 2013.01.24 Add R572 to support FHD black light current.



SI# 2012.10.25 Add RG103 short pad for touch panel and RG104 for CAMERA, and reserve UG4, CG53, CG54

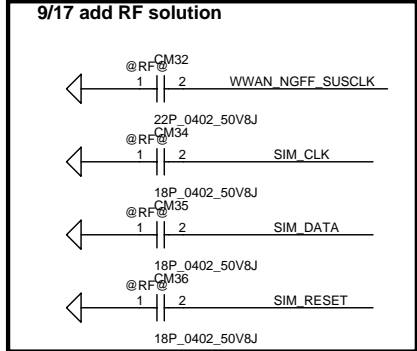
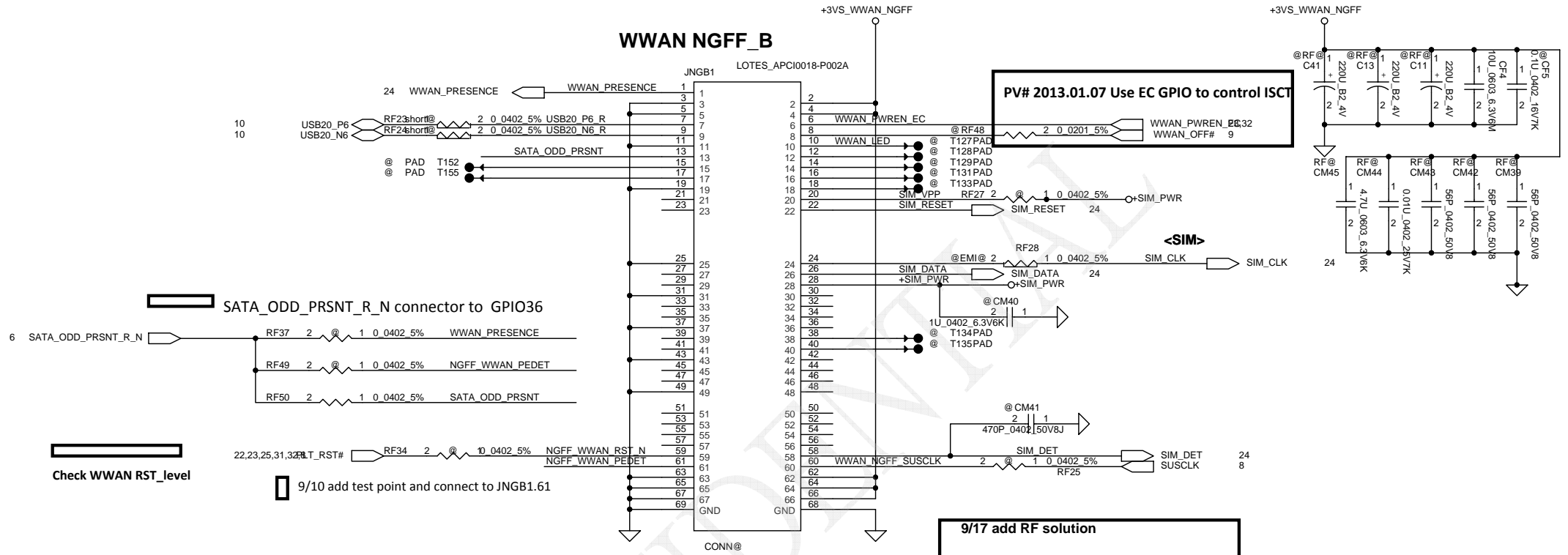


SI# 2012.10.25 Add TS_STOP# to control touch screen power on/off.
<USB Touch panel>
<Touch panel>
<Camera and DMIC>



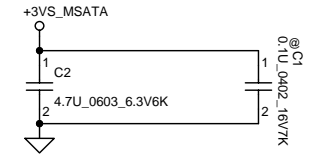
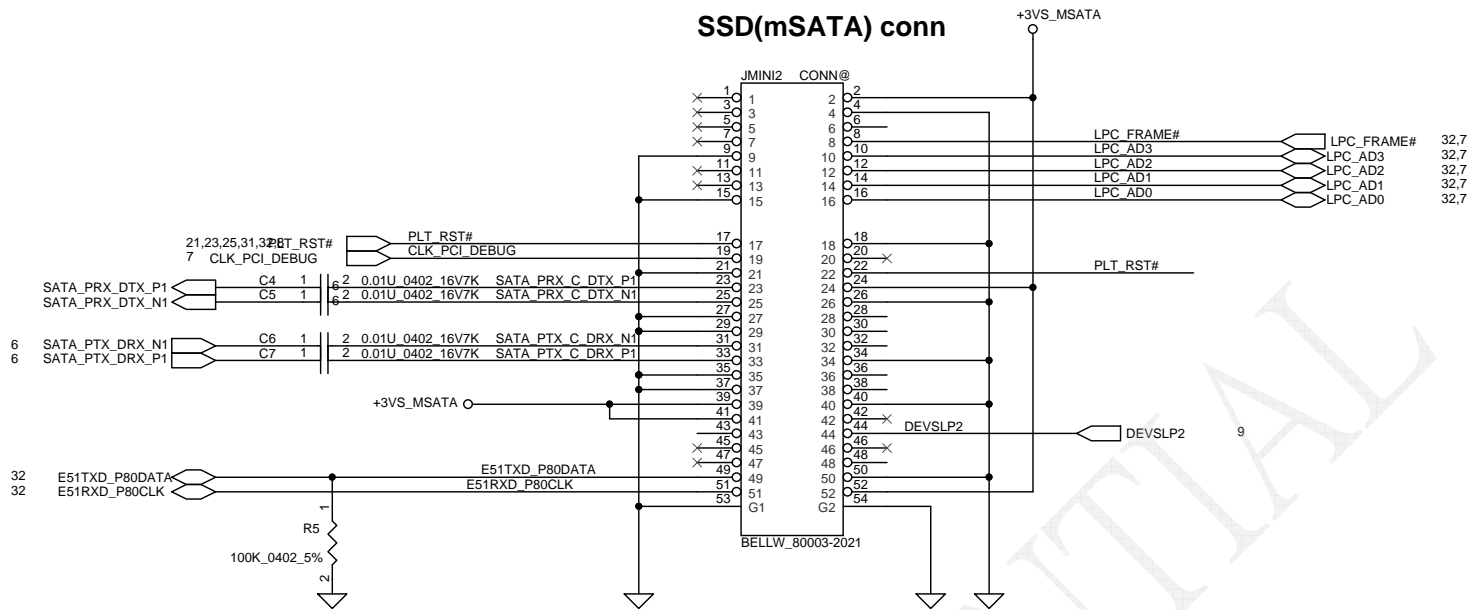
PV# 2013.01.23 Change D_MIC signals to pin36,37

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				4019LR
				Rev A
Date: Monday, October 21, 2013		Sheet 20 of 49		



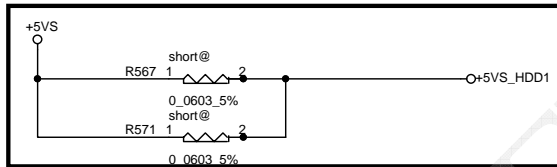
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				Date: Monday, October 21, 2013	Rev A
				Sheet 21	of 49

SSD(mSATA) conn

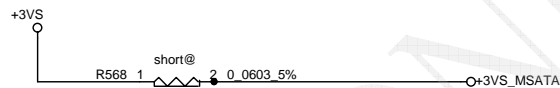


SATA2 (mSATA SSD)

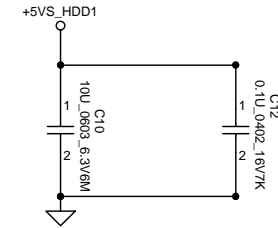
9/5 change Q23 +5VALW/+3VALW to +5VS/+3VS



PV# 2013.01.24 Add R572 to support HDD heavy loading current.

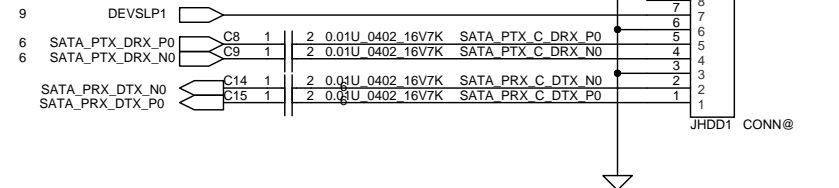


SI# 2012.10.25 Add R567 short pad for HDD and R568 for mSATA, and reserve Q23, C538, C542

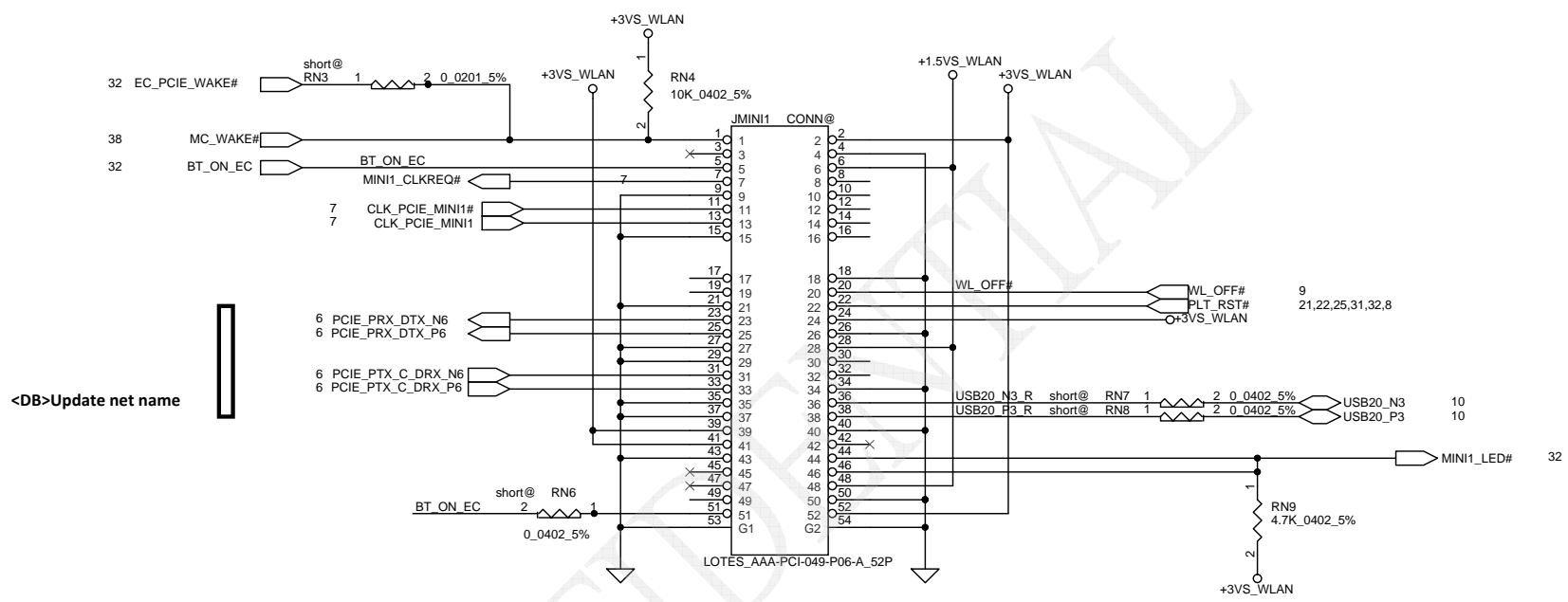
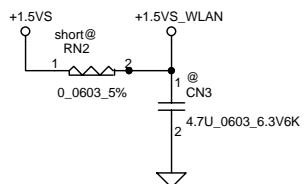
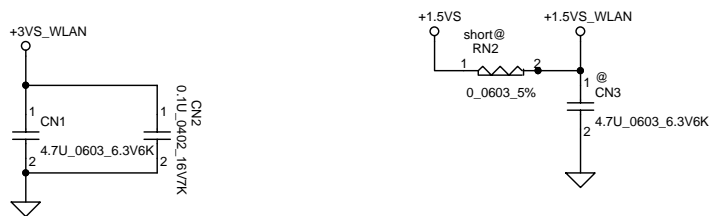


SATA 1 (2.5" HDD)

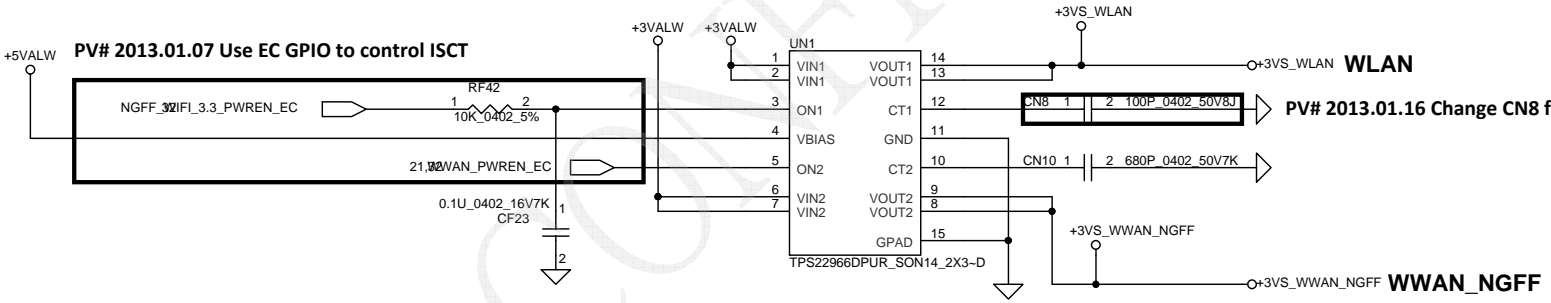
<SATA port 0>



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Date:	Monday, October 21, 2013	Sheet	22	of	49

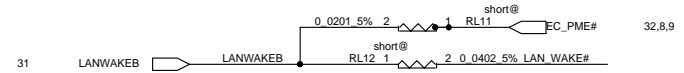
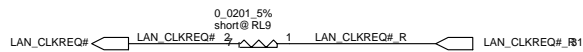


<DB>Update net name

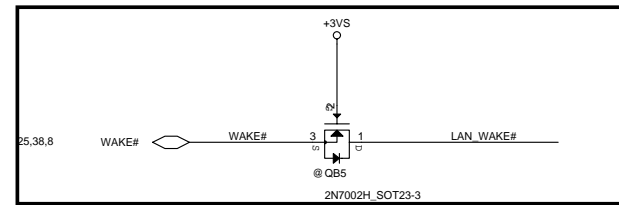
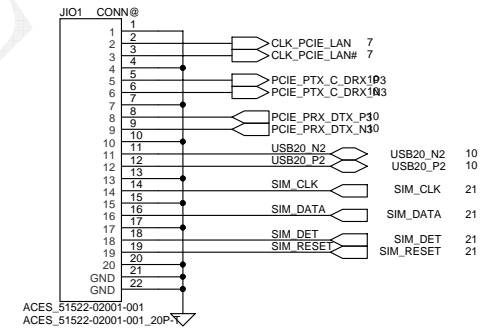


PV# 2013.01.16 Change CN8 from 680p to 100p to adjust WLAN power rising time.

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Date:	Monday, October 21, 2013	Sheet	23	of	49



20 Pin FFC

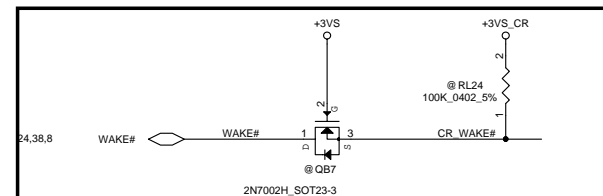
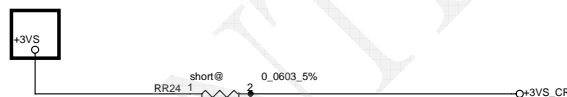
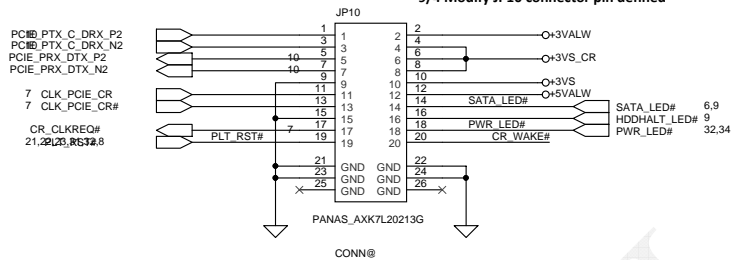


PV# 2013.01.07 Add QB5 abd RL23 to support OBFF

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				4019LR	Rev A
				Date:	Monday, October 21, 2013
				Sheet	24 of 49

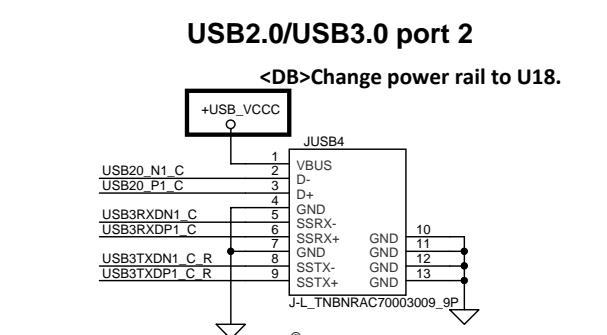
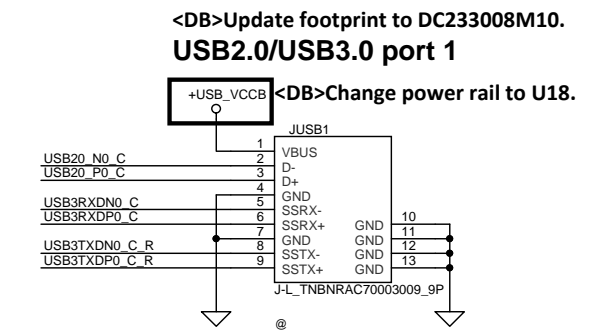
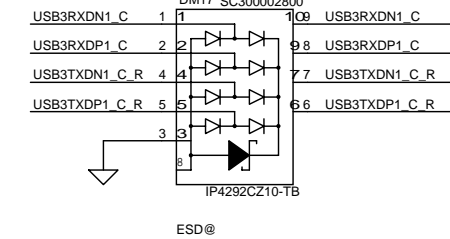
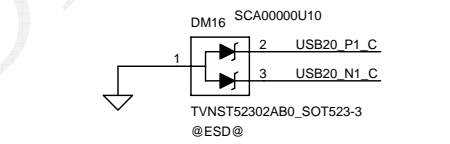
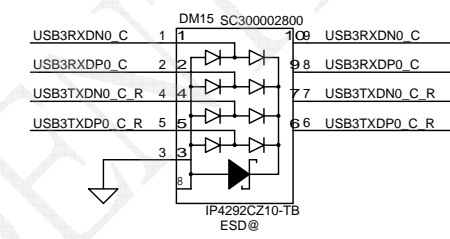
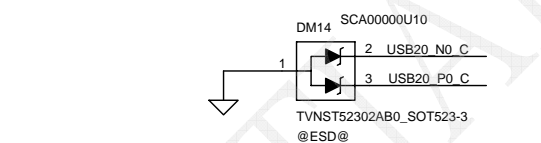
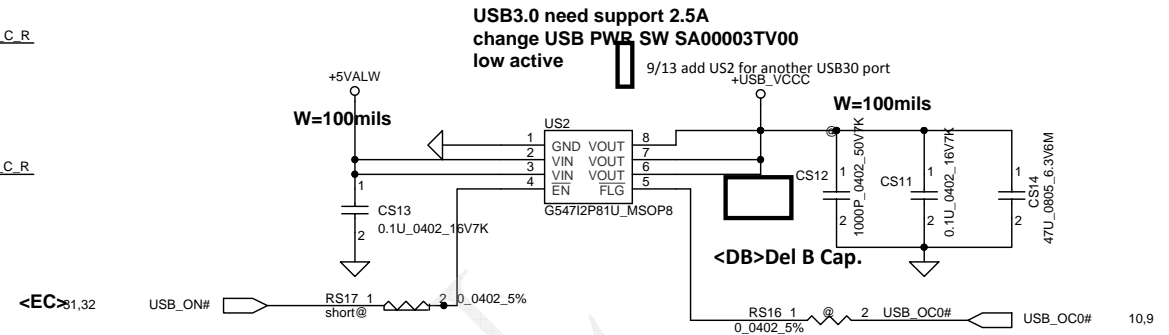
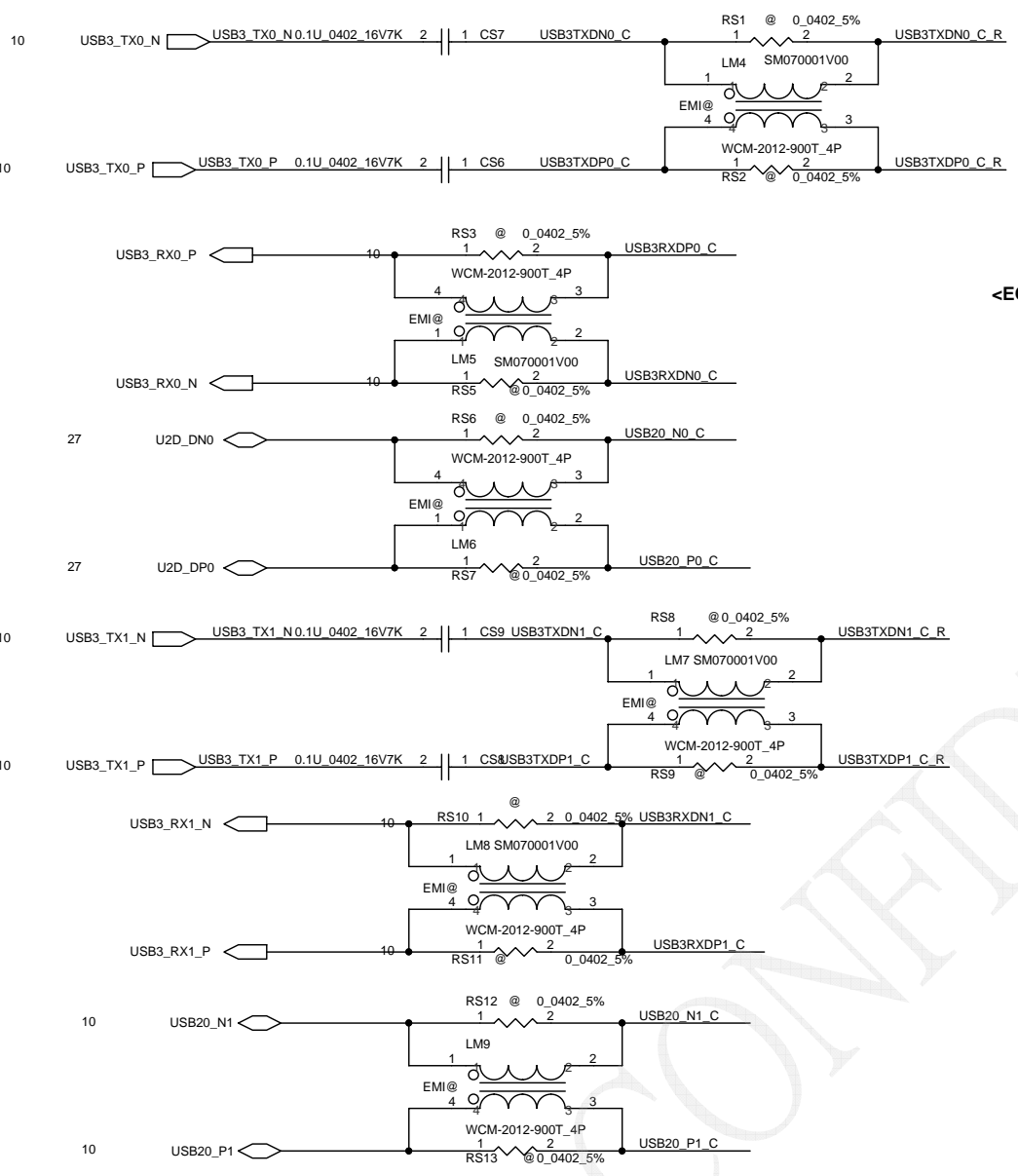
Card reader conn

9/4 Modify JP10 connector pin defined

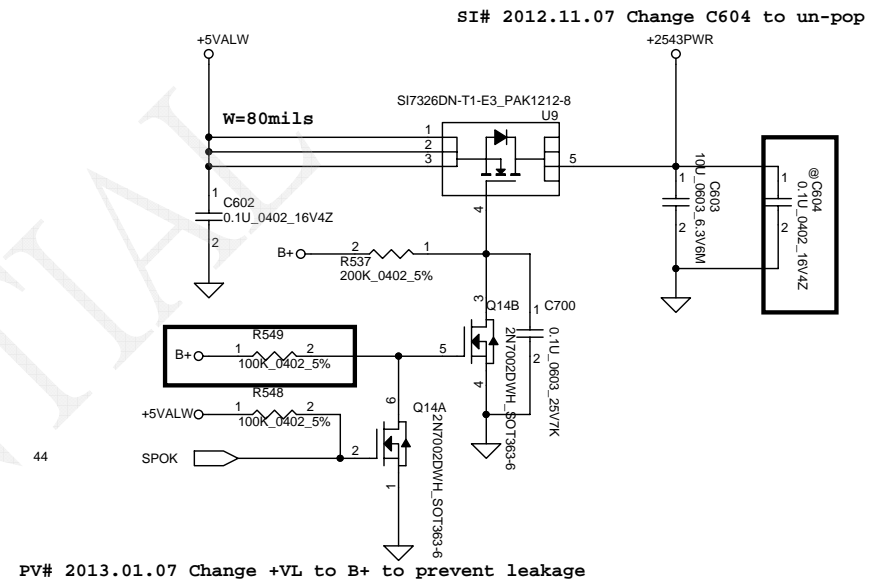
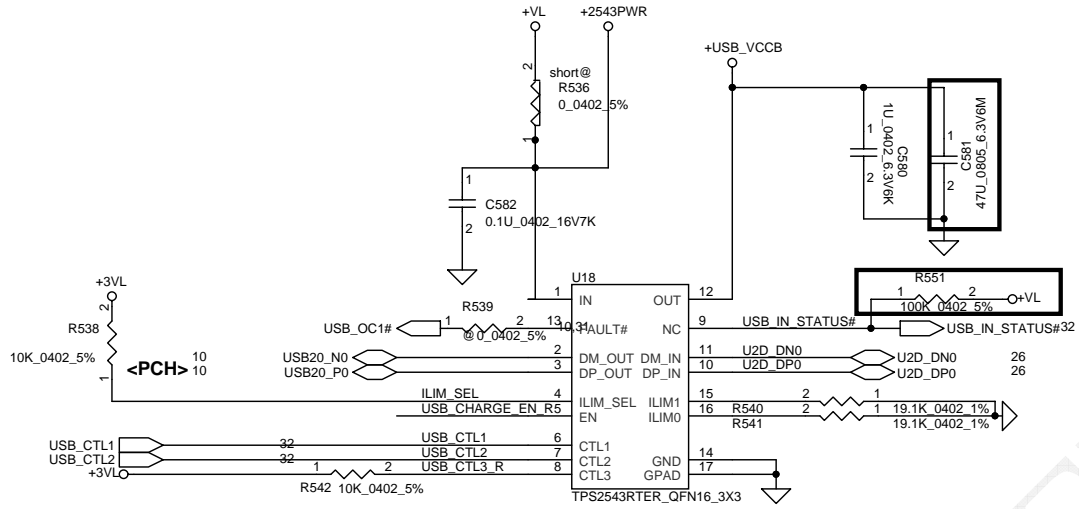


PV# 2013.01.23 Add QB7 abd RL24 to support OBFF

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				Date:	Monday, October 21, 2013
				Sheet	25 of 49
				Rev	A

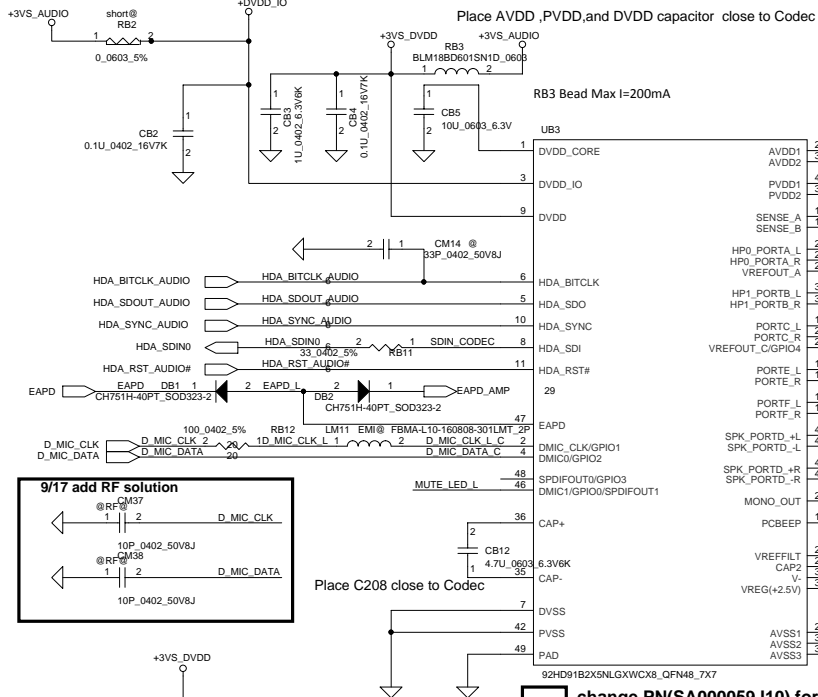


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Date:	Monday, October 21, 2013	Sheet	26	of	49	

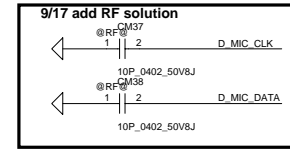
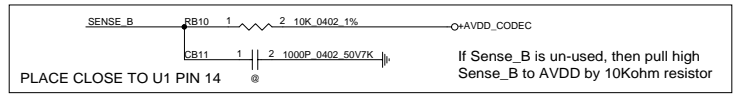
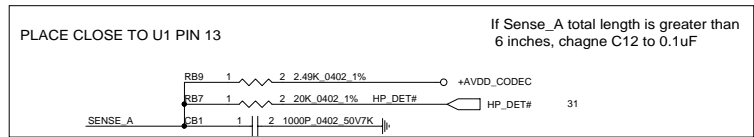


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Date:	Monday, October 21, 2013	Sheet	27	of	49

DVDD_IO should match with HDA Bus level (optional for 3.3V signaling or 1.5V signaling)



Notes:
Keep PVDD supply and power traces routed on the DGND plane.
Keep away from AGND and other analog signals

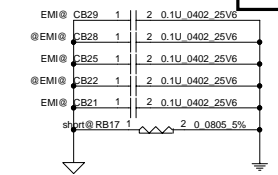


Place C208 close to Codec

change PN(SA00059J10) for 92HD91B2X5NLGXWCX8

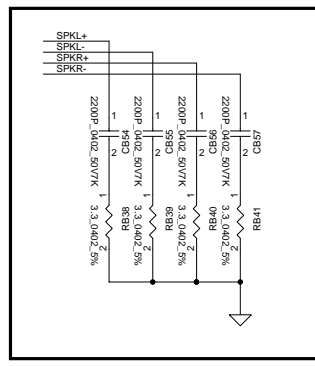
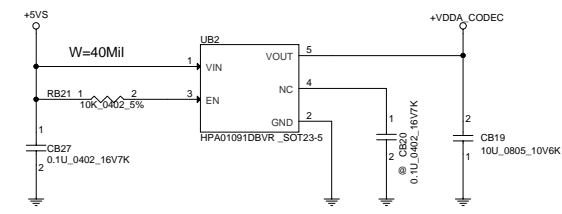
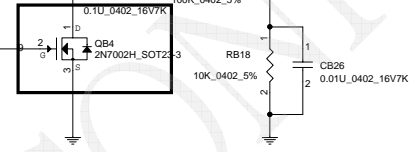
Place C209, C210, CA87, CA89 close to Codec

9/18 add reserve CB28, CB29 and stuff CB25, CB22, CB21 0.1uF



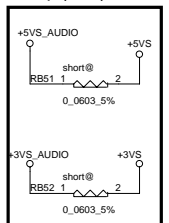
PV# 2013.01.07 Change QB4 to dual package

SB Beep



Place need close UB3

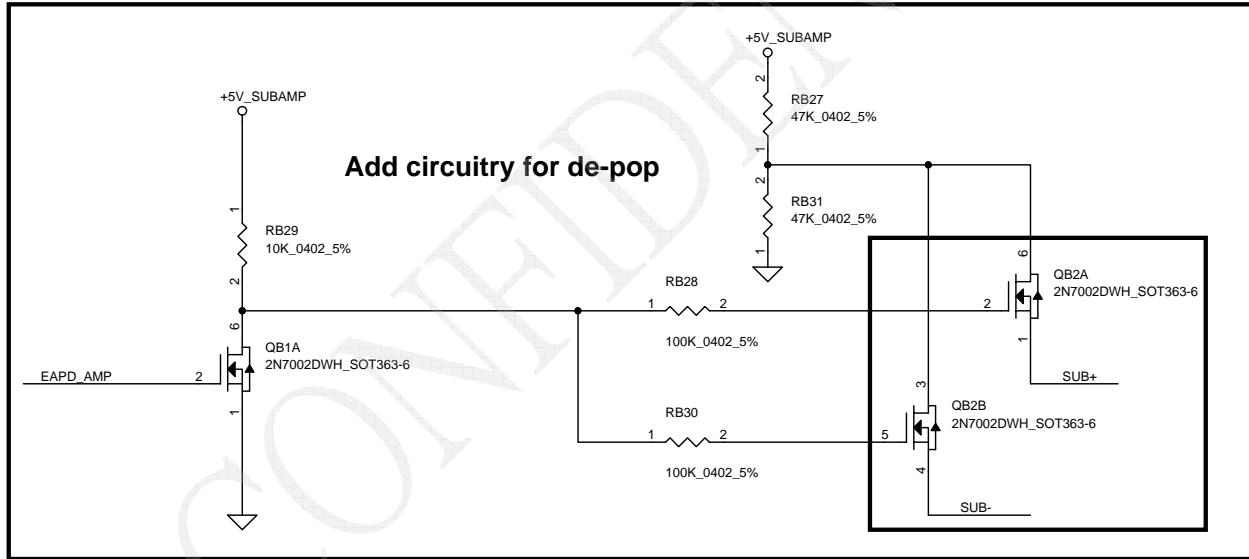
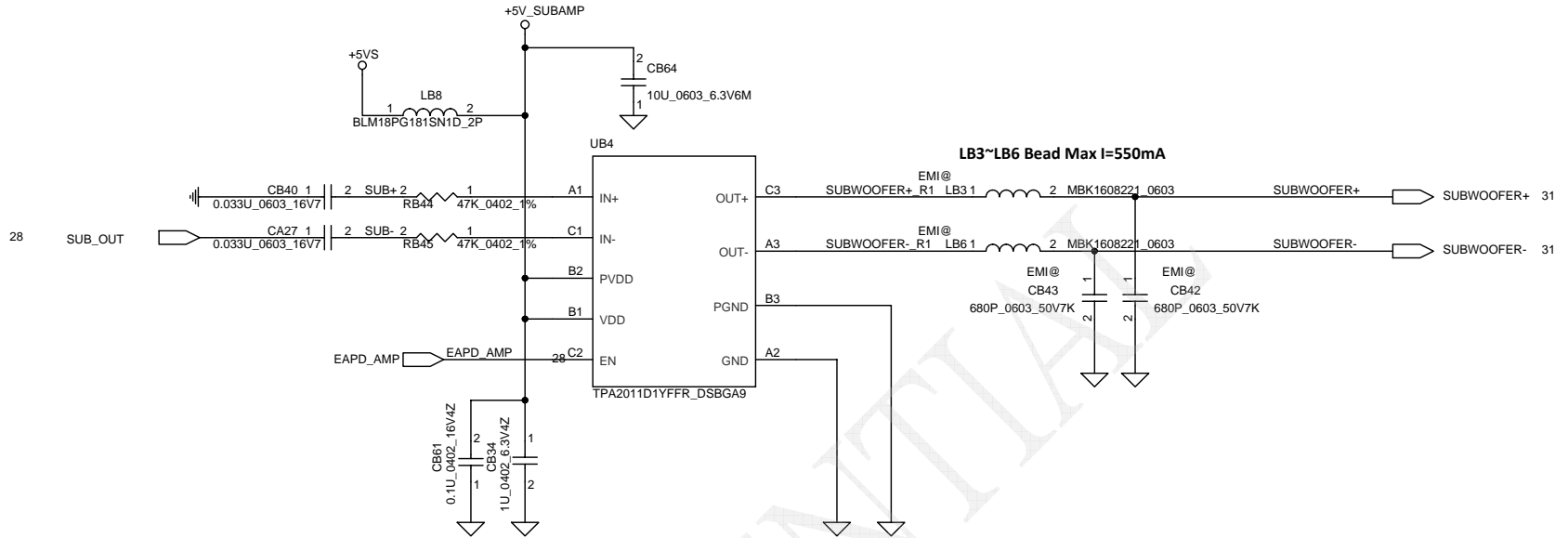
S# 2012.10.25 Add RB51 short pad for Audio 5VS PWR and RB52 for Audio 3VS PWR, and reserve QB5, CB65, CB66



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Subwoofer AMP TPA2011 = HPA01086YFFR

DB> TPA2012 Change to TPA2011

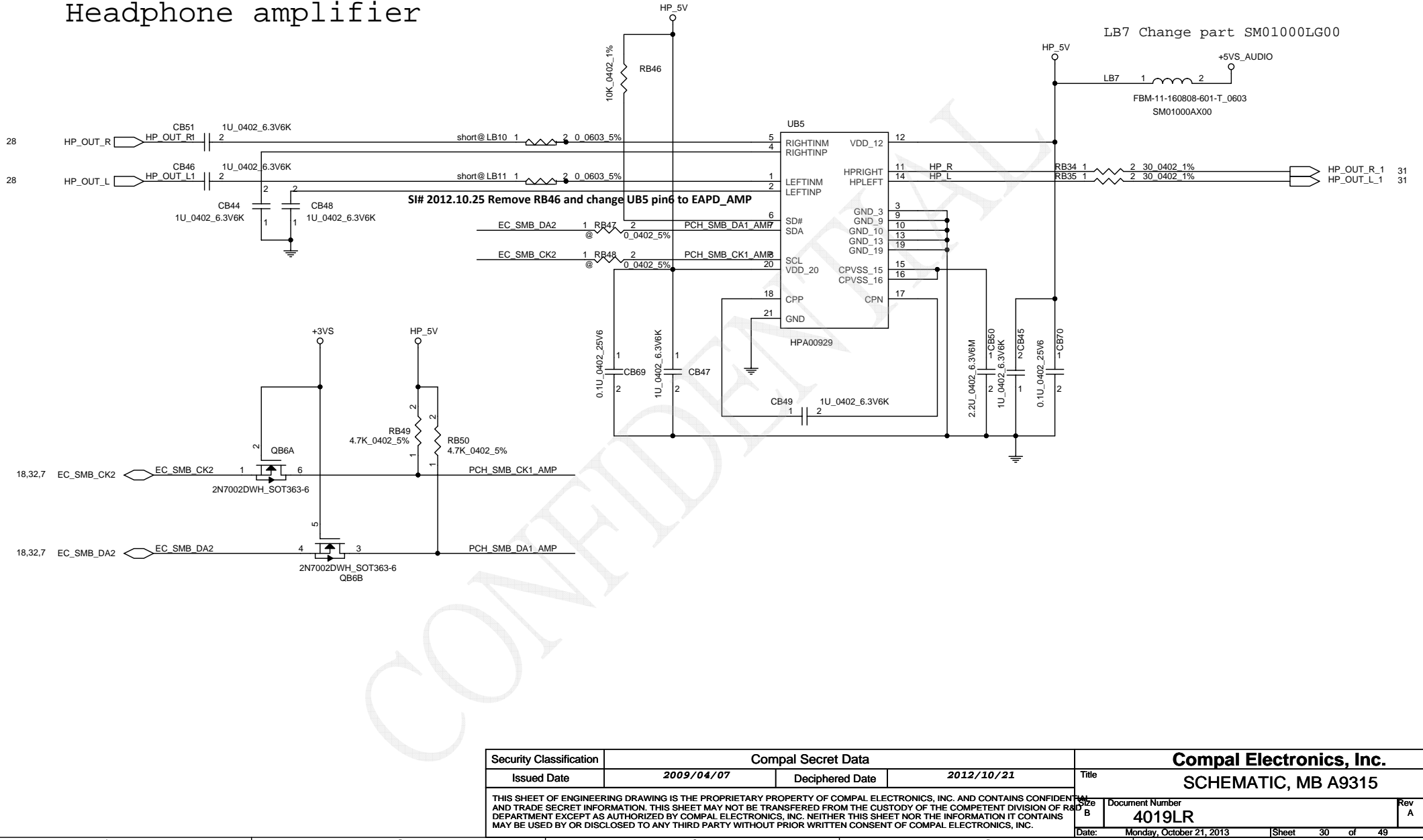


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				Date:	Monday, October 21, 2013
				Sheet	29 of 49

Headphone AMP TPA6130A2 = HPA00929

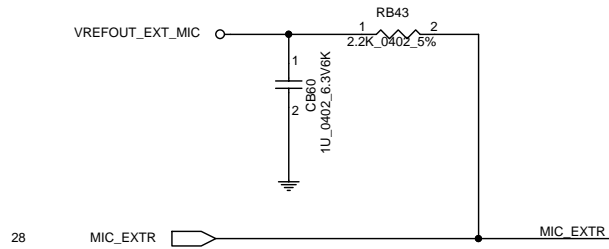
DB> HPA01196 Change to HPA00929

Headphone amplifier

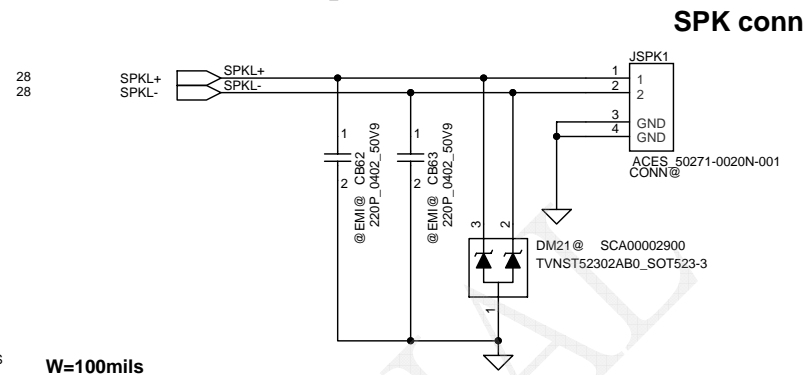


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			Sheet 30 of 49	Rev A

Ext. Mic

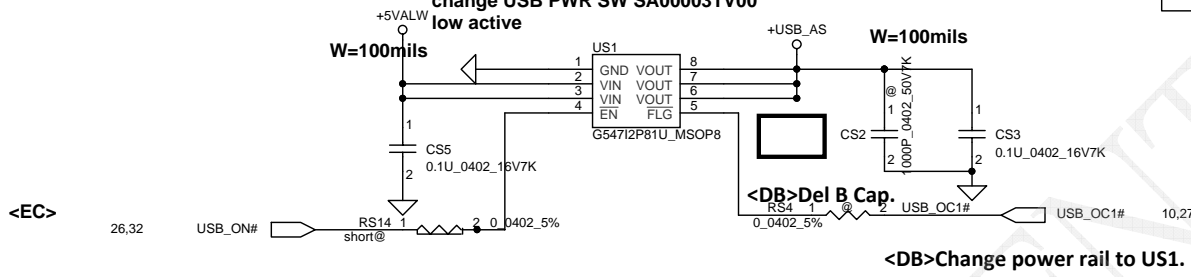


Front Speaker Connector 1



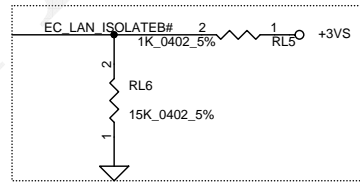
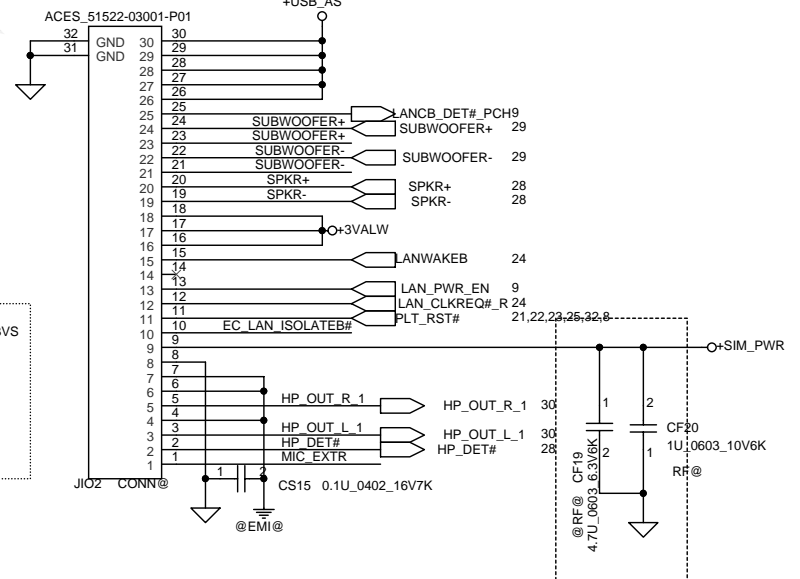
SPK conn

USB3.0 need support 2.5A
change USB PWR SW SA00003TV00
low active



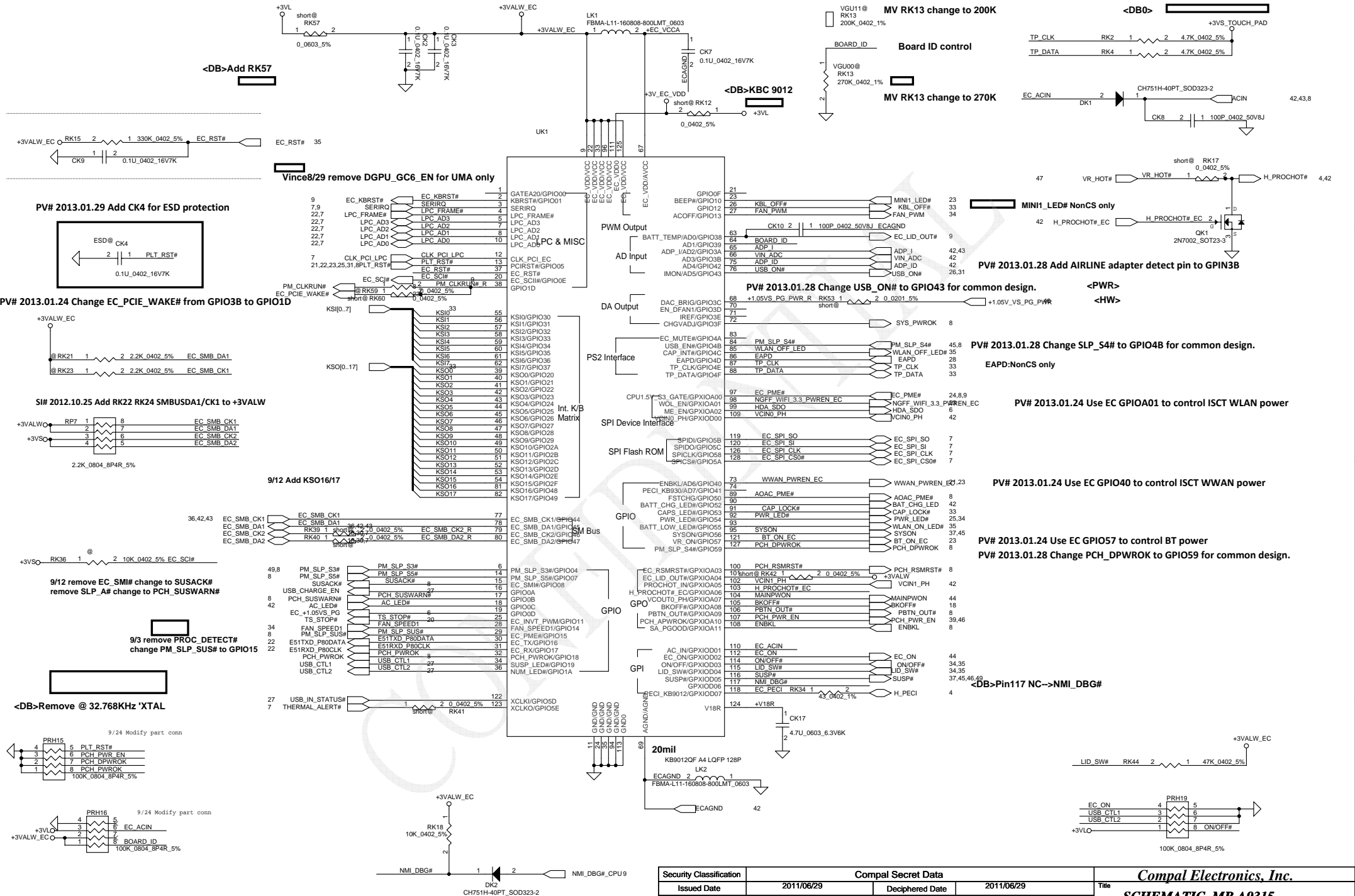
<DB>Del B Cap.
<DB>Change power rail to US1.

30 Pin FFC



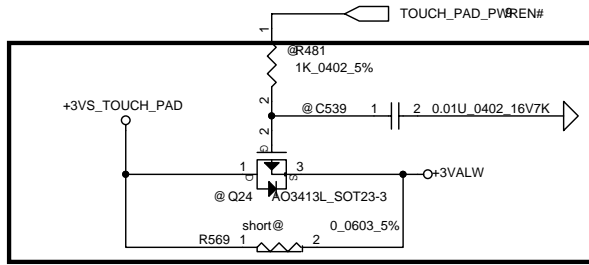
10/30 RF add, near JIO1 connector.

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Part No	Document Number	Rev	Date	Sheet	of
	4019LR	A	Monday, October 21, 2013	31	49

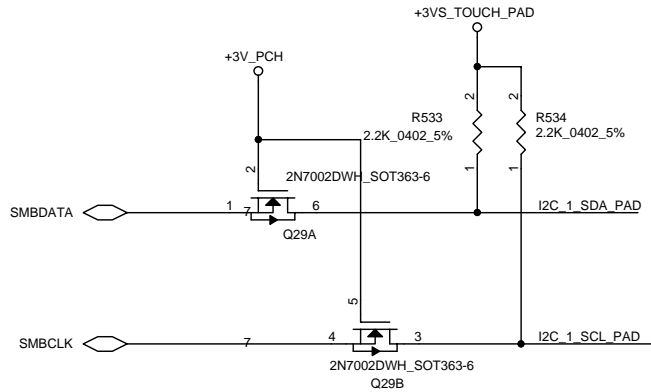


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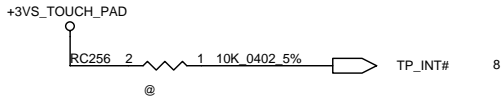
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Title	SCHEMATIC, MB A9315		
Size	Document Number	Rev	A
Custom	4019LR		
Date:	Monday, October 21, 2013	Sheet	32 of 49



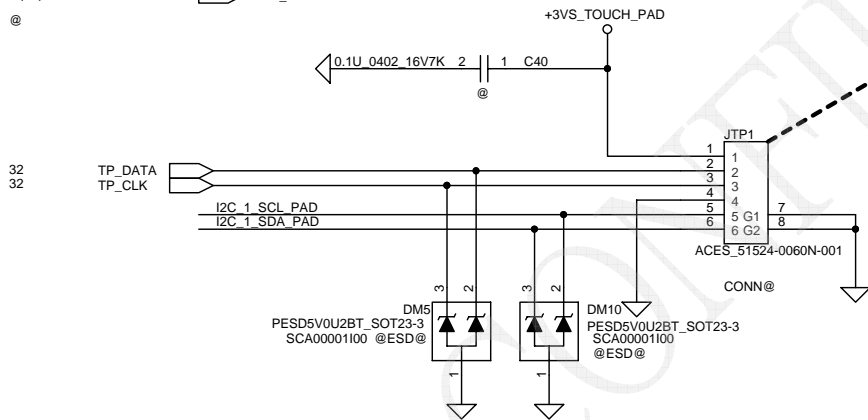
SI# 2012.10.25 Add R569 short pad for Touch PAD PWR, and reserve Q24, R569, R481



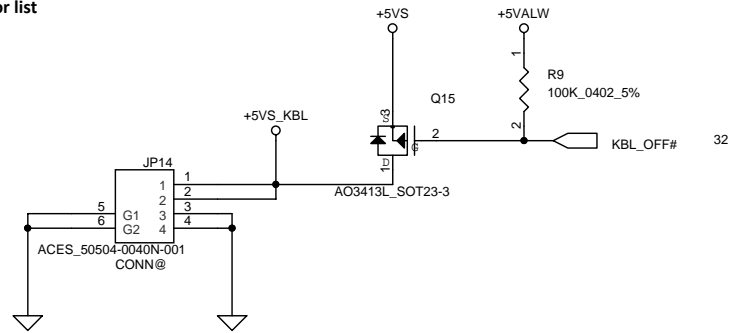
Touch pad conn



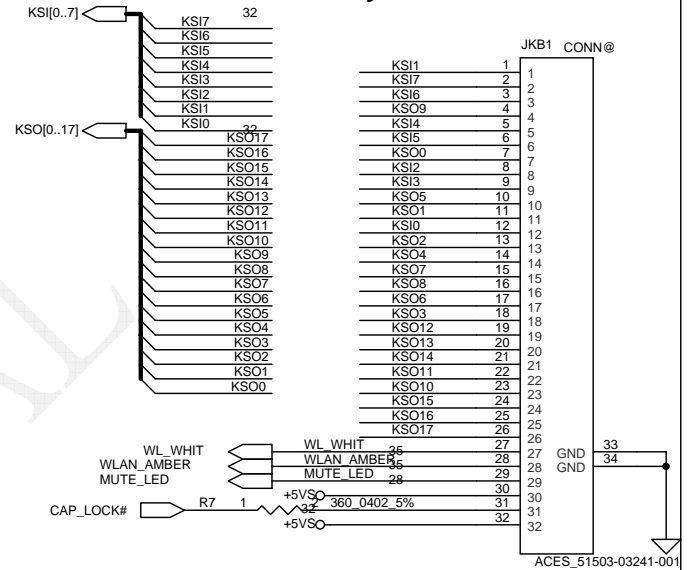
PV# 2012.01.08 Change TP connector to 6 pin and pin define



Waiting for connector list

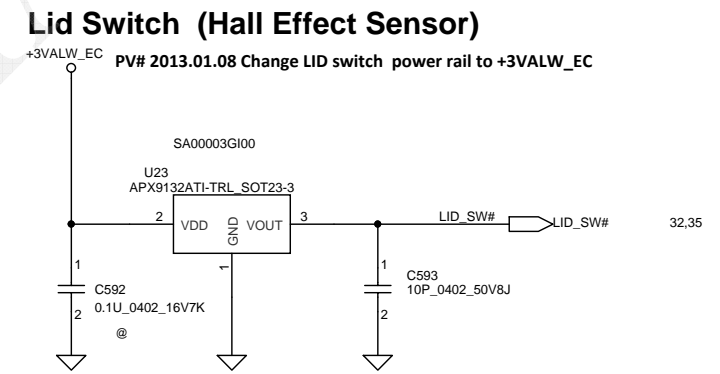
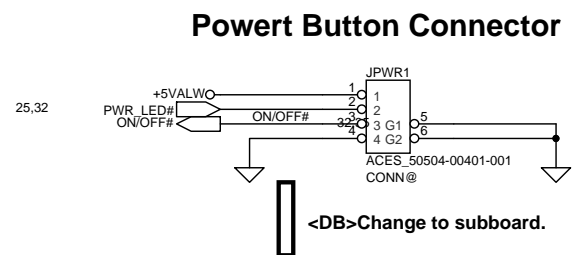
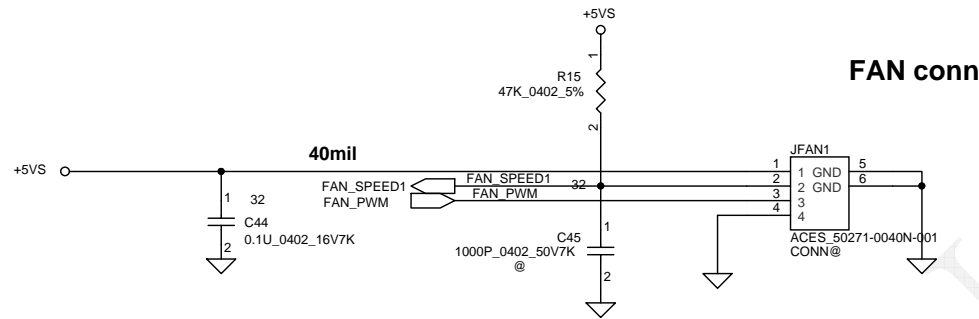


Keyboard conn



Keyboard backlight Conn

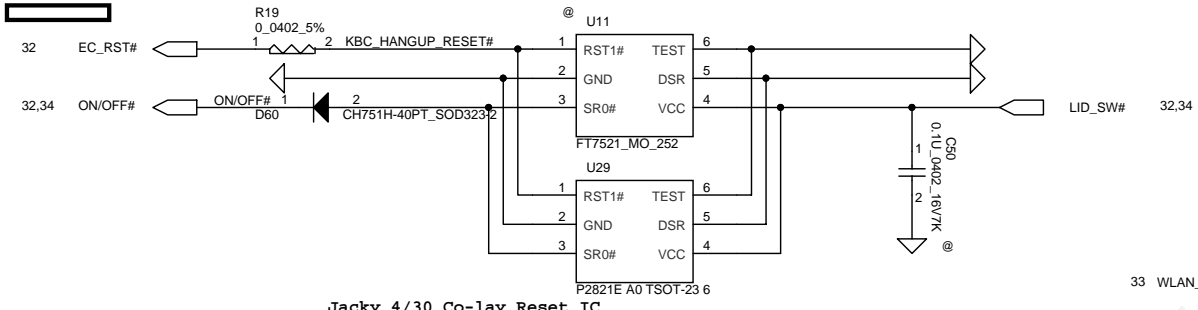
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Document Number	4019LR				Rev A
Date:	Monday, October 21, 2013	Sheet	33	of	49



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				4019LR
				Date: Monday, October 21, 2013
				Sheet 34 of 49

<DB> RST1# connect to EN_3V_5V

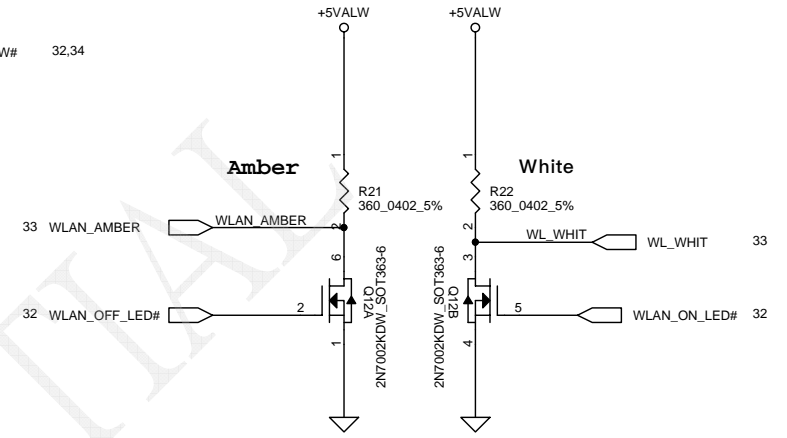
Reset IC



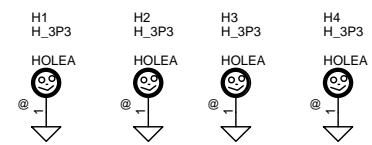
Jacky 4/30 Co-lay Reset IC

Amber

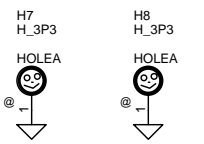
White



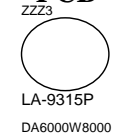
CPU



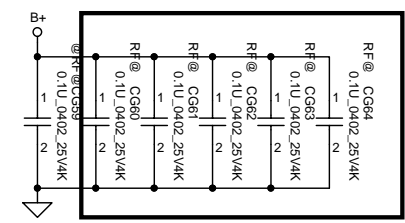
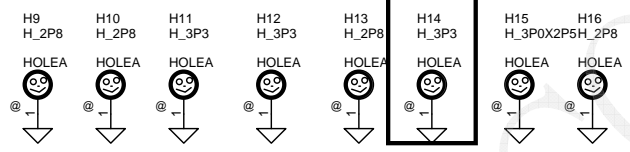
Card reader



PCB



SI# 2012.10.31 Add H14 for WLAN stand off

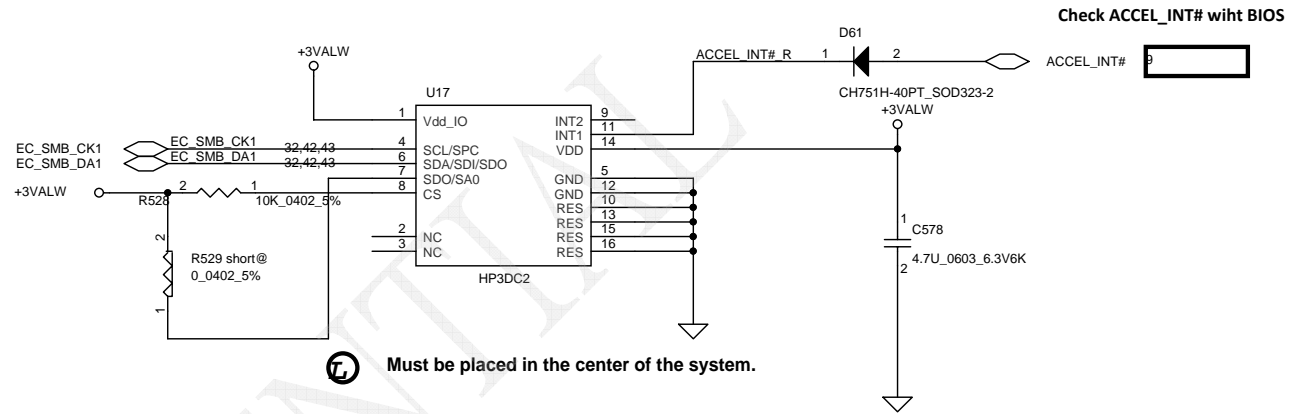


PV# 2013.01.30 Add CG60~CG64 for RF.

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Date: Monday, October 21, 2013				Sheet	35 of 49	

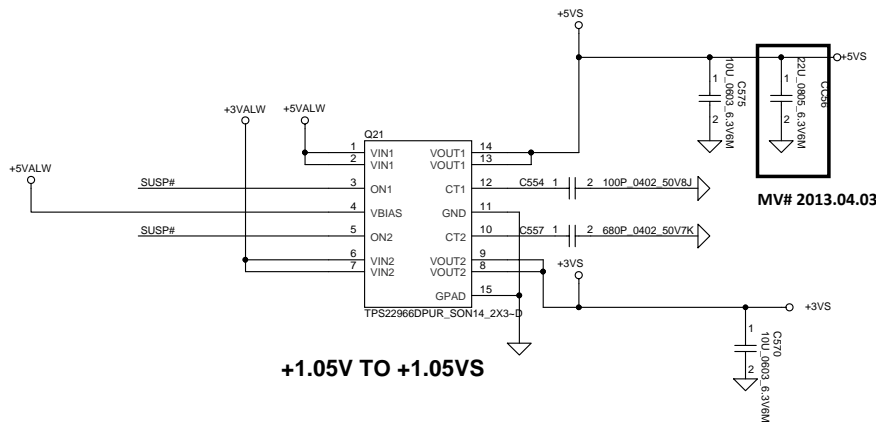
ACCELEROMETER

Sensor hub -->G-sensor

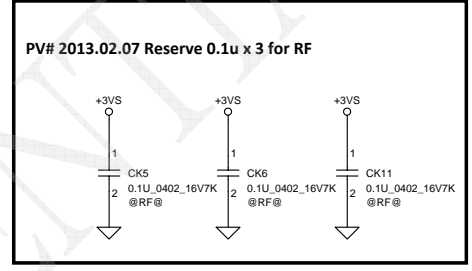
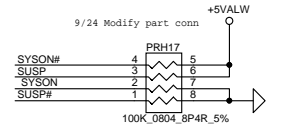
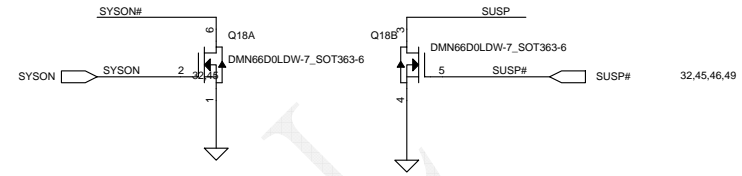
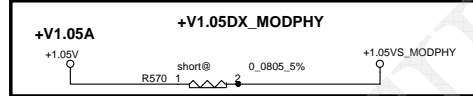


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				4019LR	A
Date:	Monday, October 21, 2013	Sheet	36	of	49



+1.05V TO +1.05VS



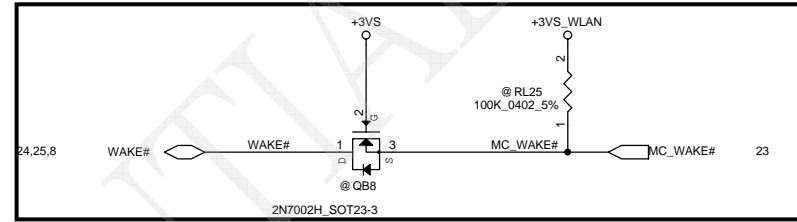
AO4430L
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 VGS(Th) max=2.5V
 Rds Max=5.5m @VGS=10V
 Rds Max=7.5m @VGS=4.5V

CPU +V1.05DX_MODPHY
 Max Rdson <6m ohm
 1840mA

AO4430L
 VGS Max=+/- 20V
 VGS(Th) max=2.5V
 Rds Max=5.5m @VGS=10V
 Rds Max=7.5m @VGS=4.5V

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				Custom	4019LR
				Date:	Monday, October 21, 2013
				Sheet	37 of 49
				Rev	A

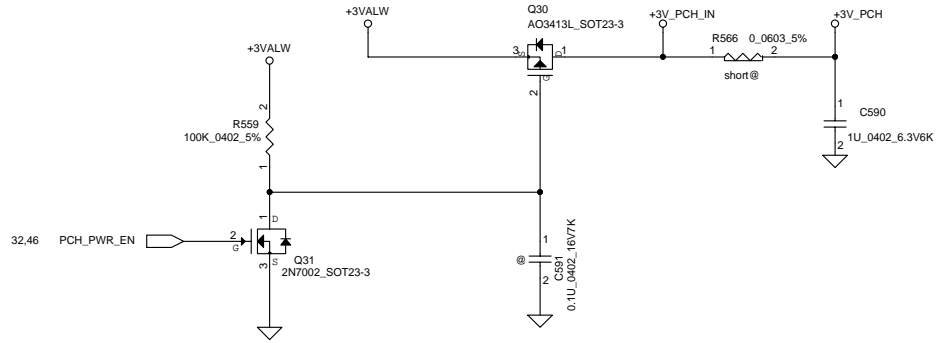
NGFF and WLAN



PV# 2013.01.23 Add QB8 abd RL25 to support OBFF

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				Custom	4019LR
Date:	Monday, October 21, 2013	Sheet	38	of	49



<DB>NonCS no +1.8VS and low switch-->PMOS

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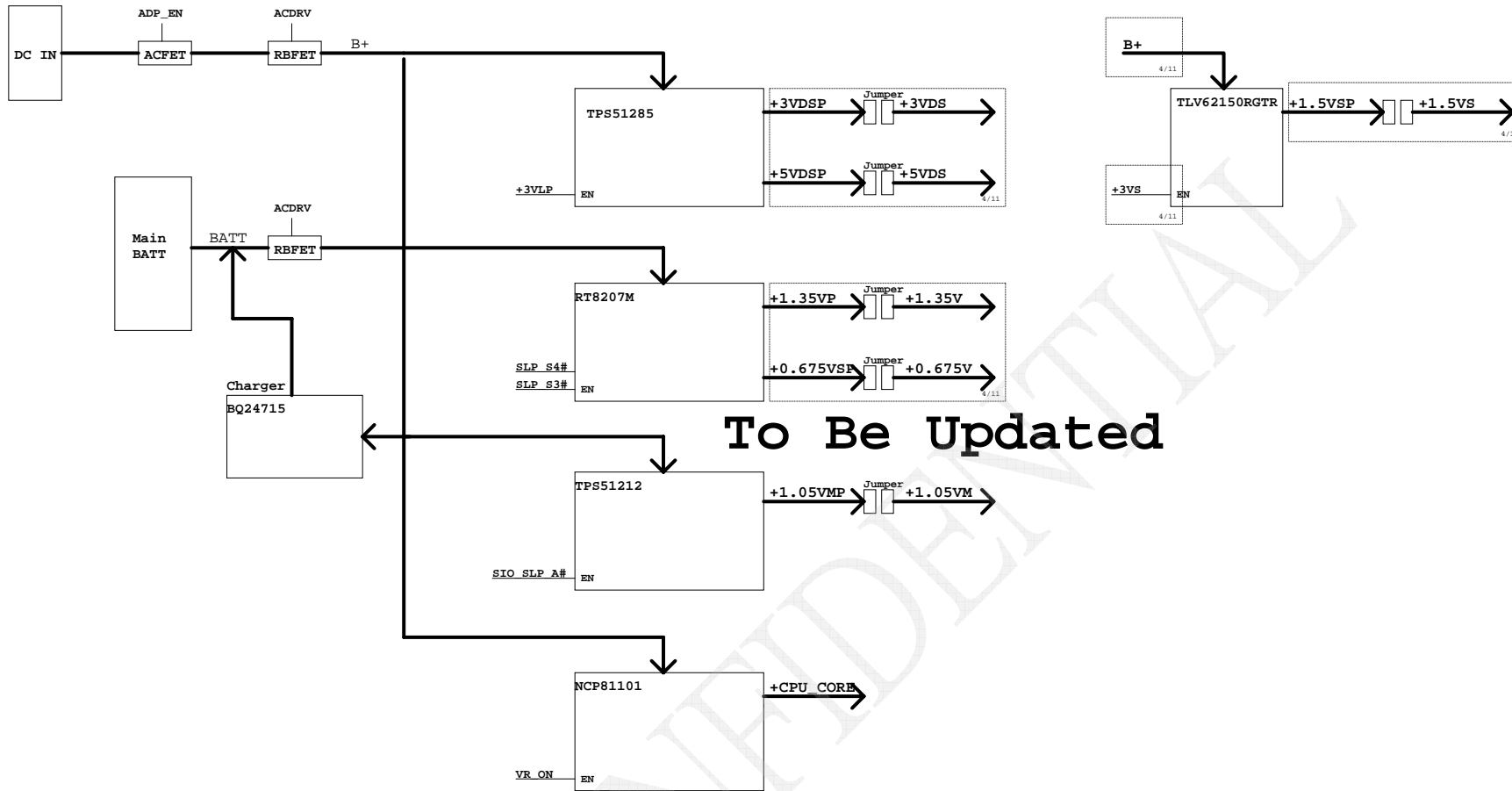
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				Date:	Monday, October 21, 2013	Sheet	39	of	49

Headphone and Mic conn

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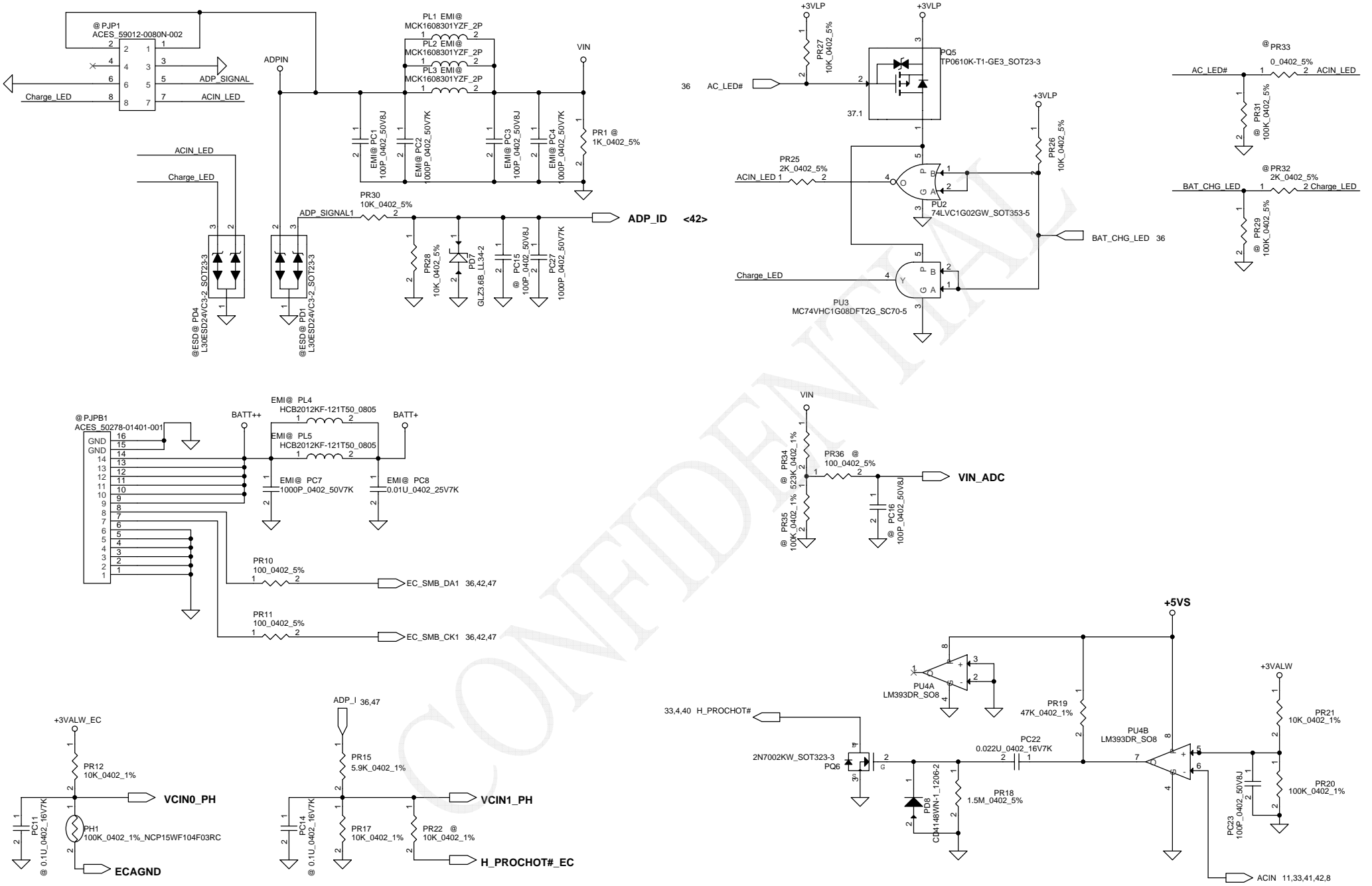
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Size	Document Number	Date	Monday, October 21, 2013	Sheet 40 of 49
Custom	4019LR			

Compal Electronics, Inc.

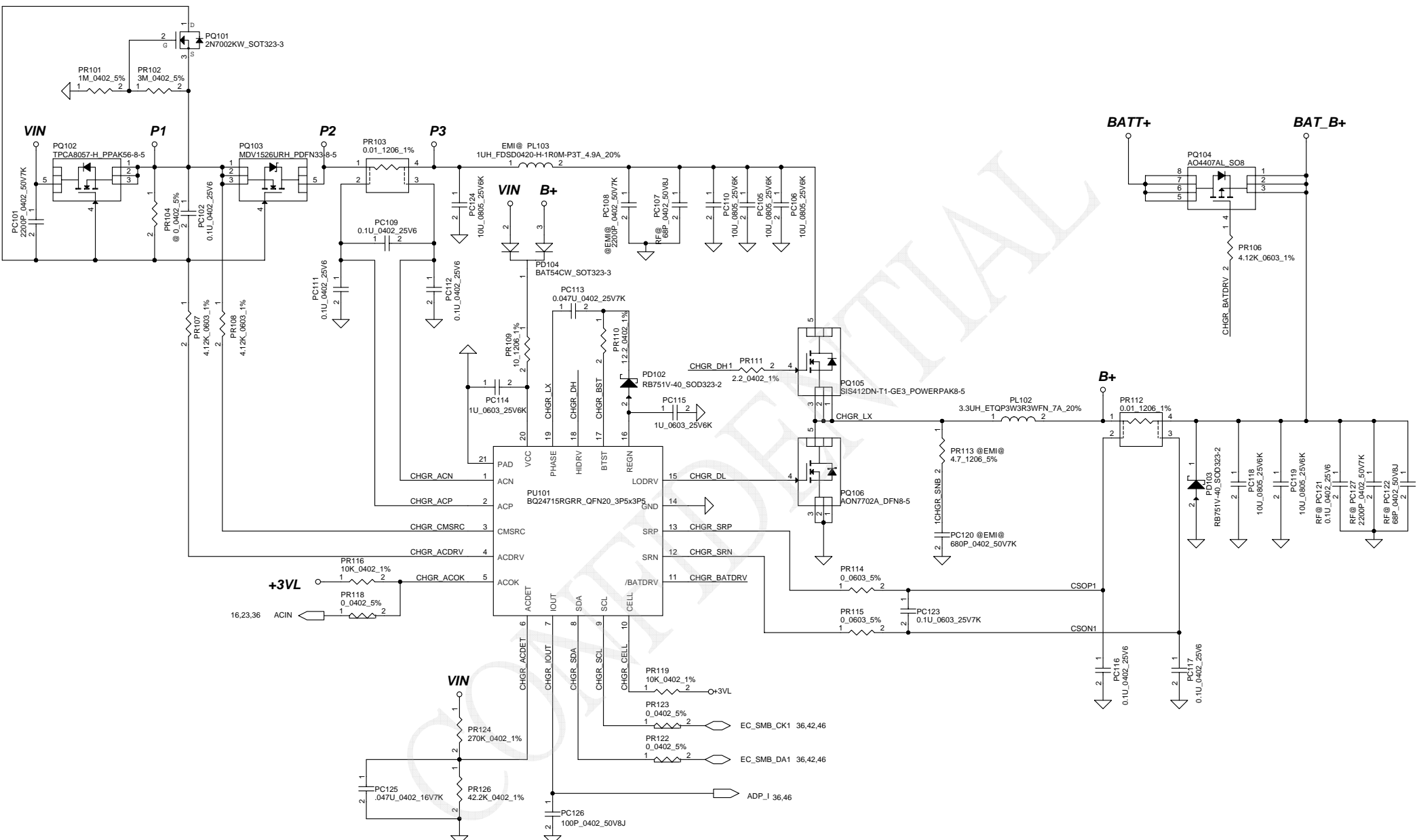


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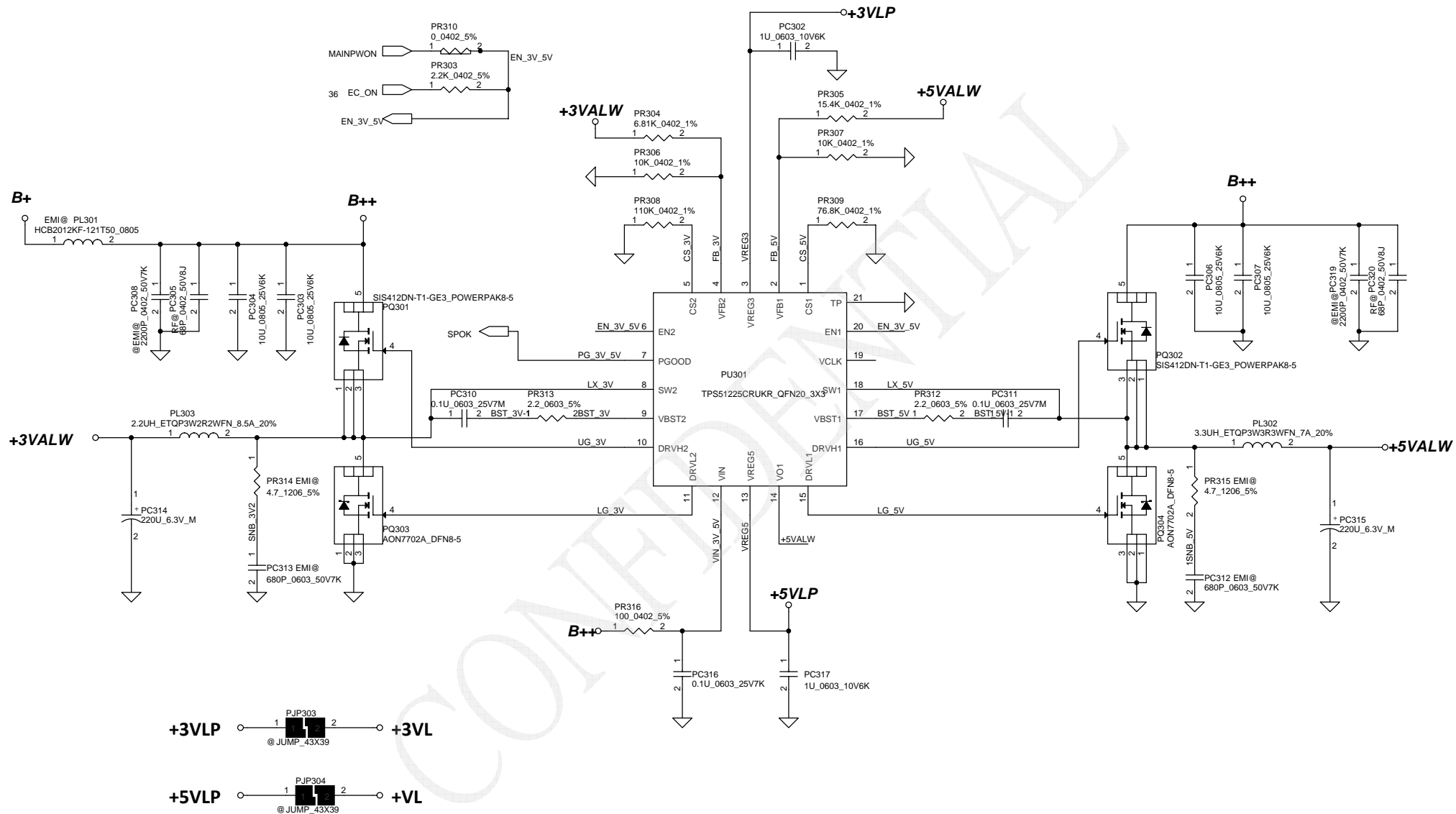
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				Date:	Monday, October 21, 2013
				Sheet	41 of 49



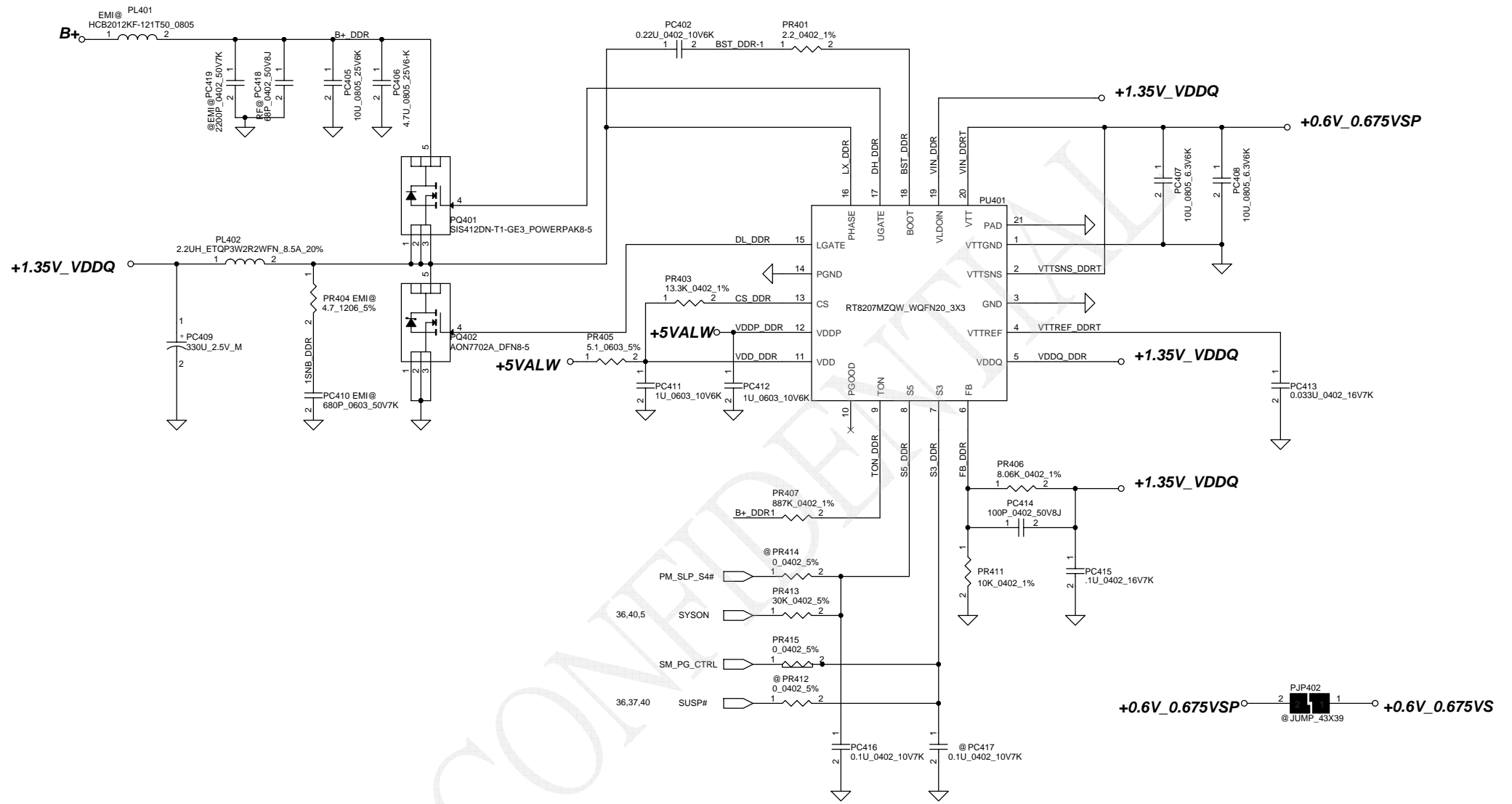
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Document Number	4019LR				Rev
Date:	Monday, October 21, 2013	Sheet	42	of	49



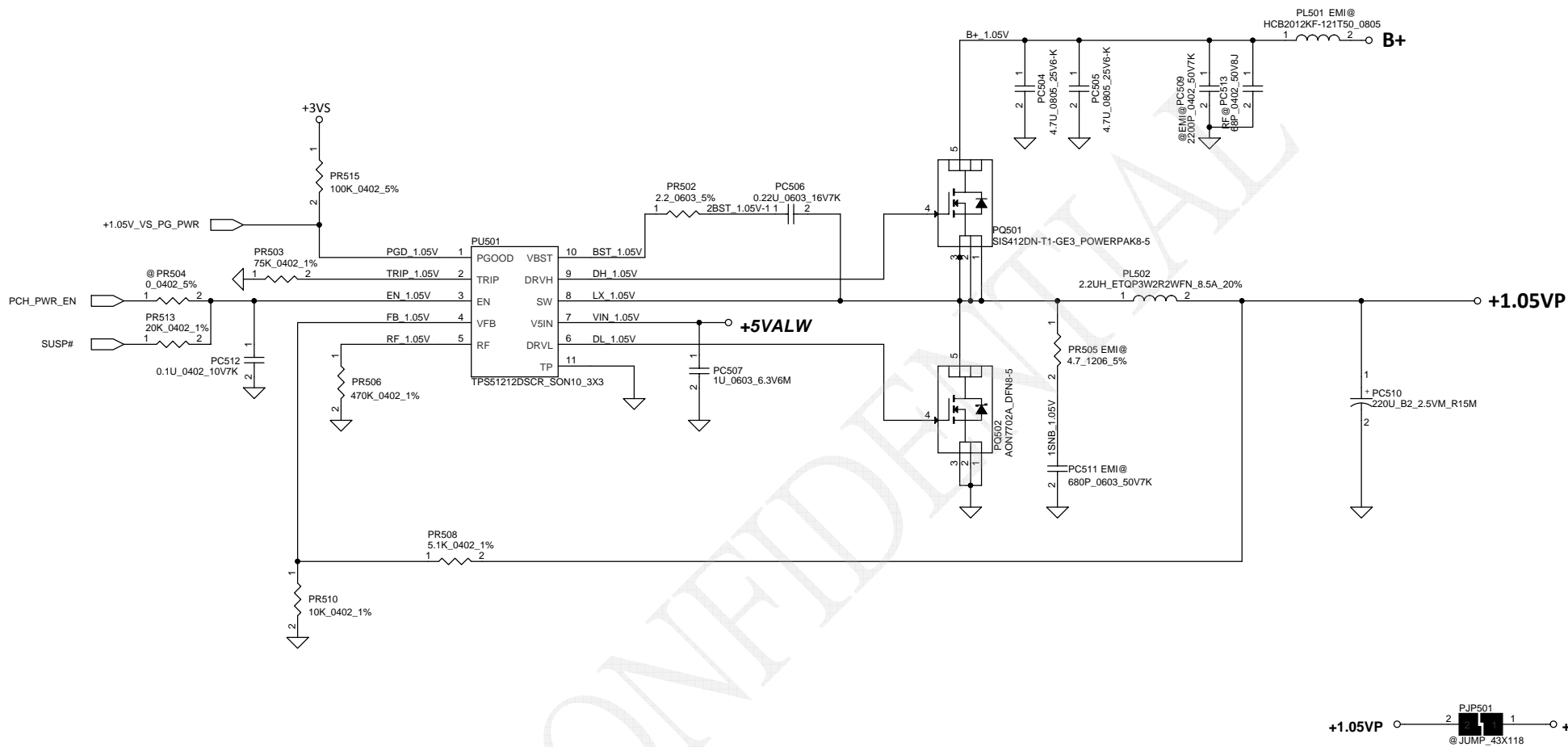
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				4019LR
Date: Monday, October 21, 2013				Sheet 43 of 49



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Document Number	4019LR	Rev	A	Date	Monday, October 21, 2013
Sheet	44	of	49		

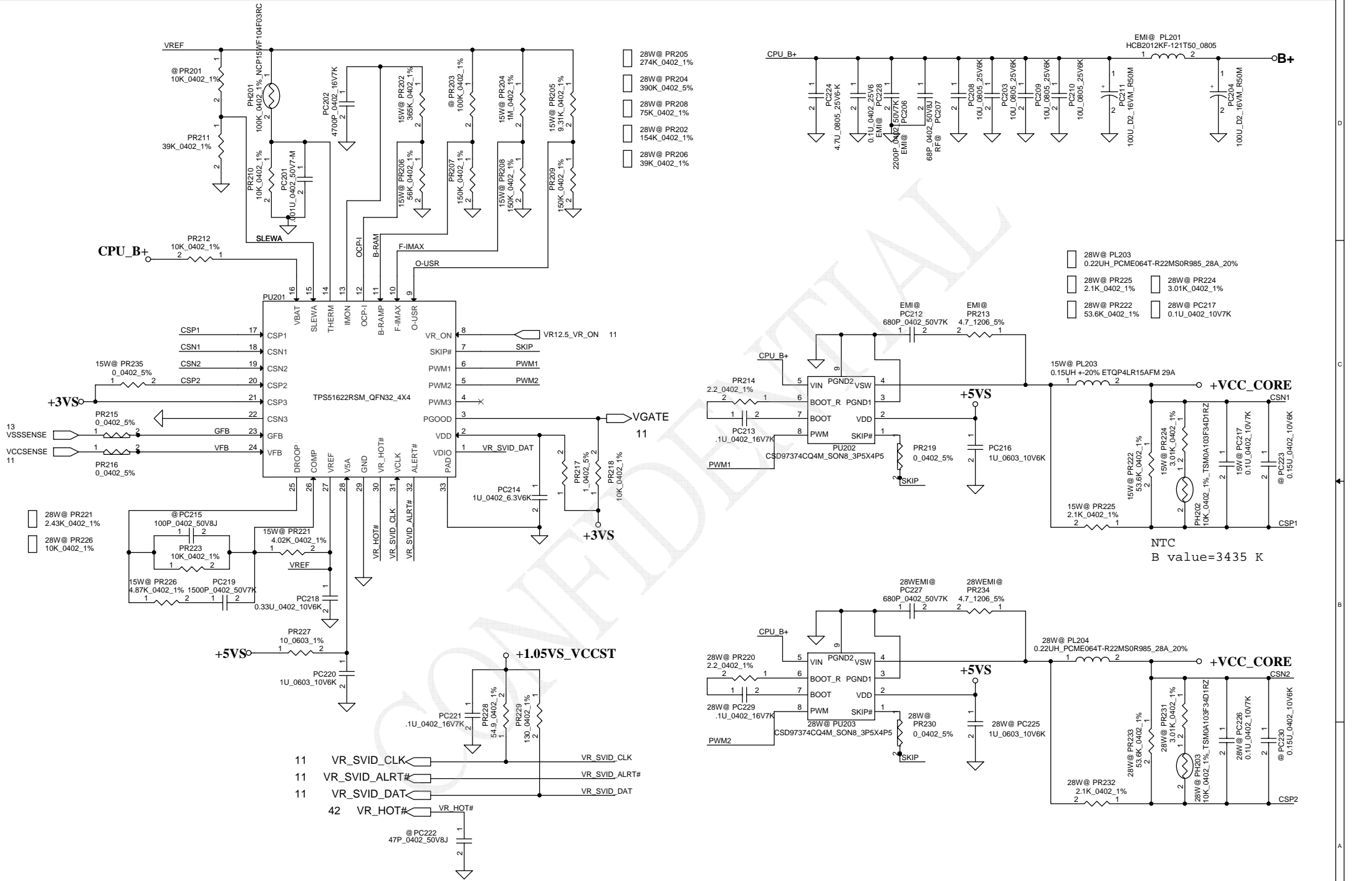


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Date:	Monday, October 21, 2013	Sheet	45	of	49



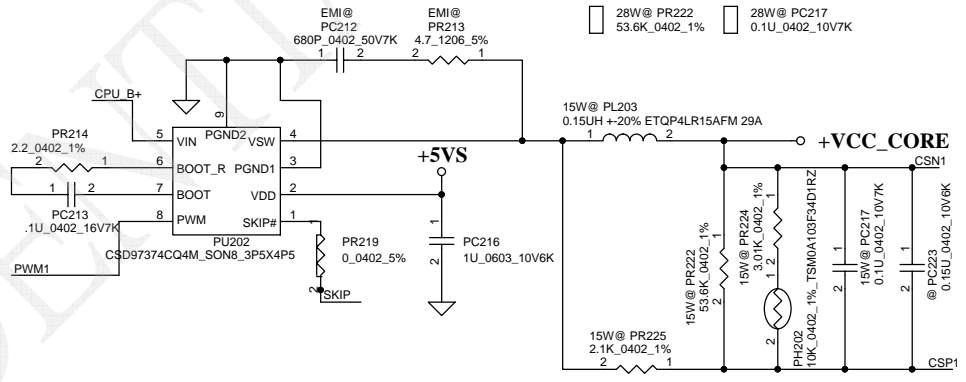
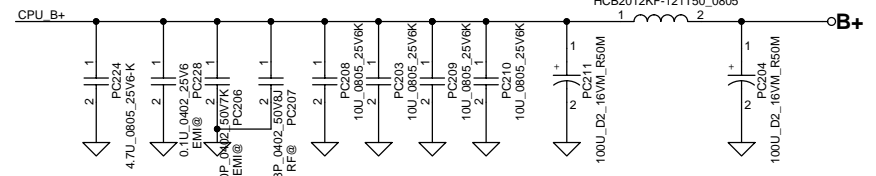
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Date:	Monday, October 21, 2013		Sheet	46 of 49	

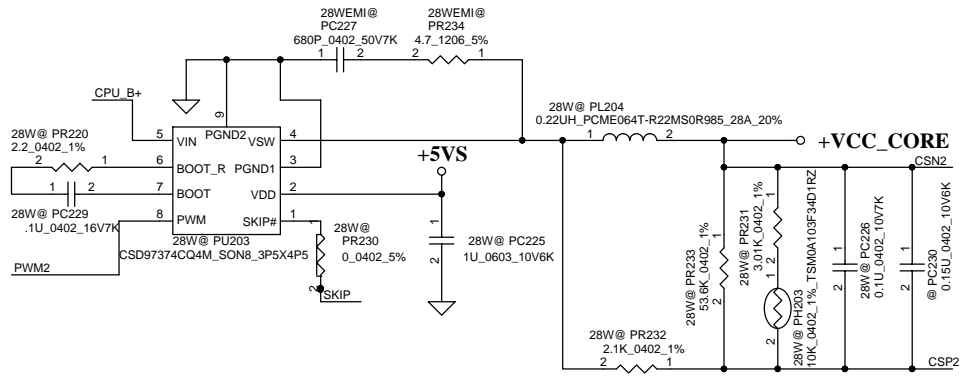


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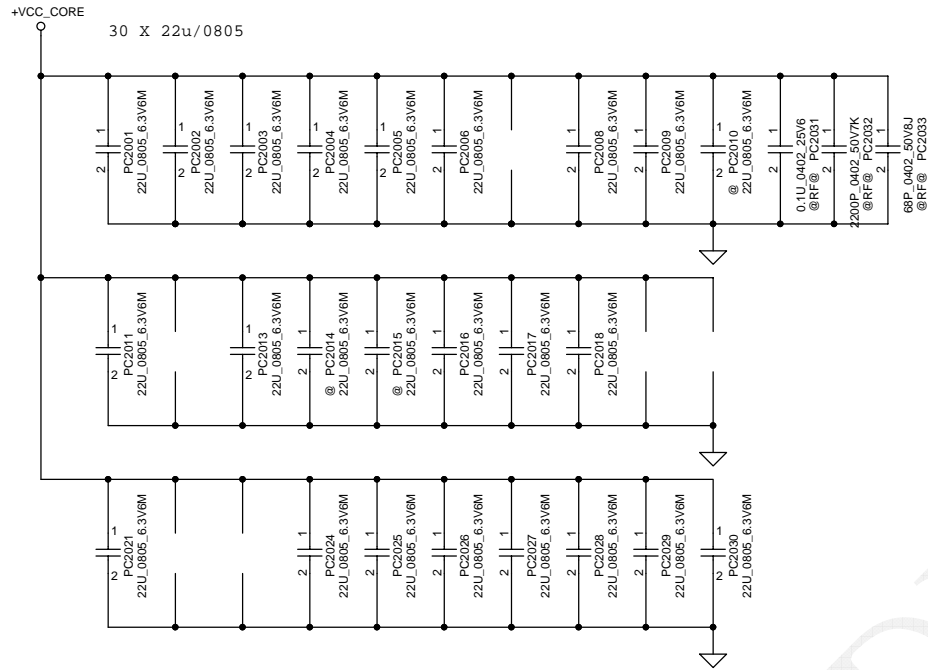


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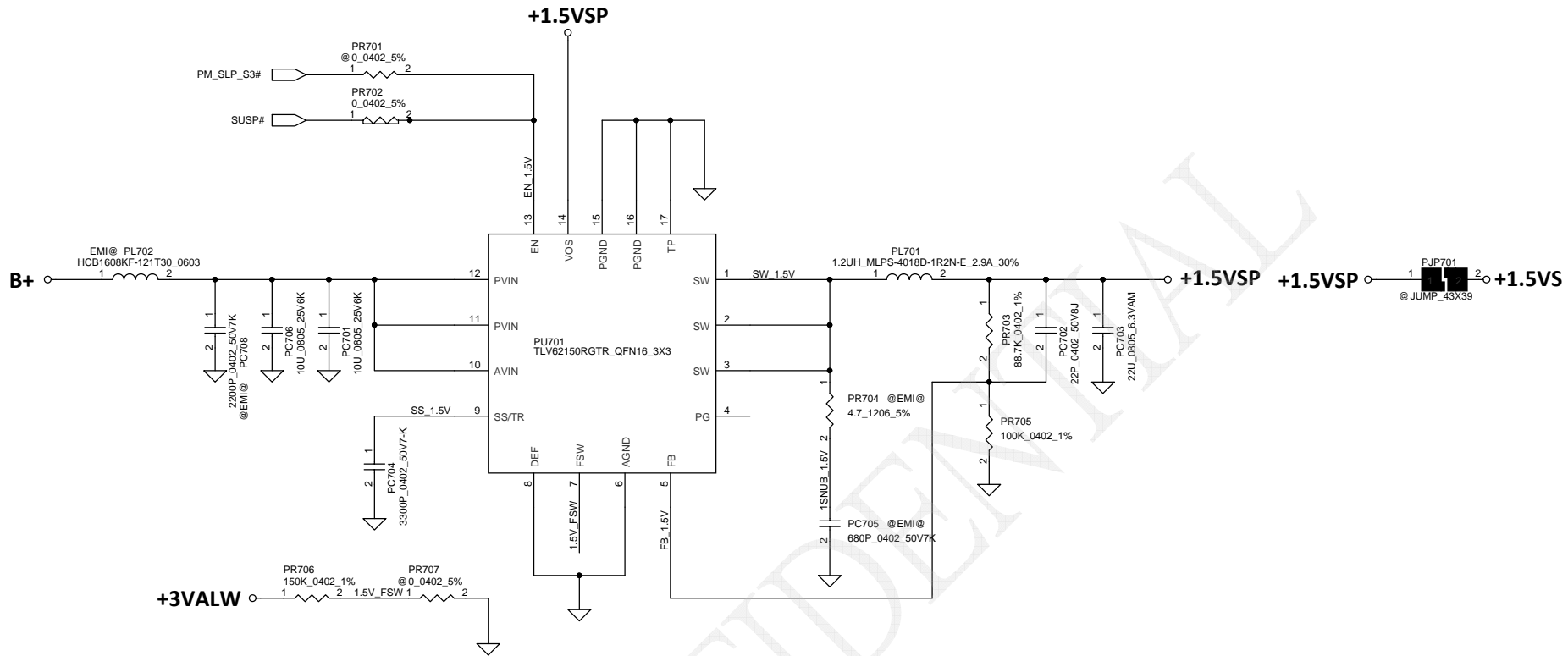


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Size	Document Number	Date	Monday, October 21, 2013	Sheet	47 of 49
	4019LR				



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Date:	Monday, October 21, 2013	Sheet	48	of	49



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Date: Monday, October 21, 2013				Sheet	49 of 49