

LCFC Confidential

CG520 NM-A804

M/B Schematics Document

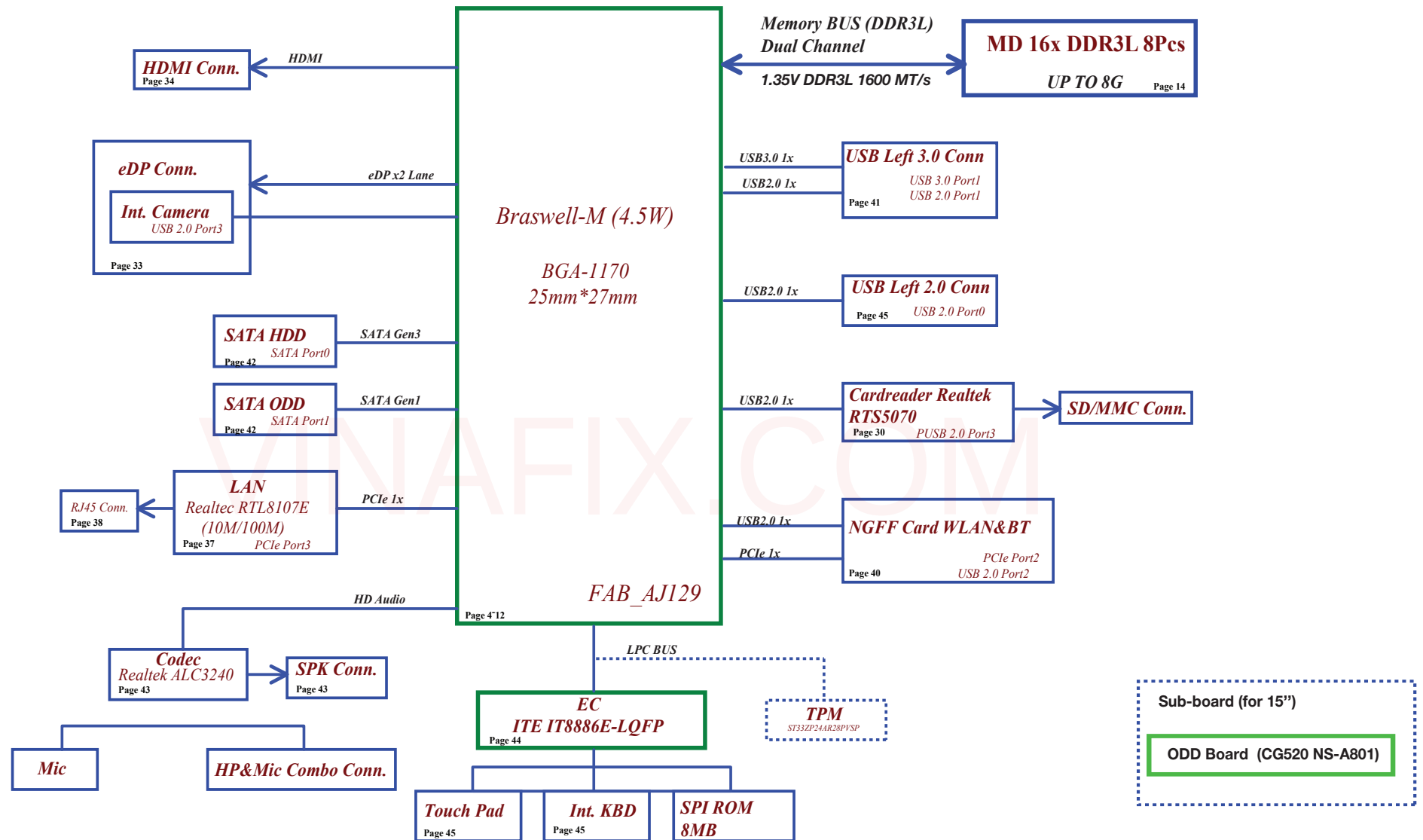
Intel Braswell M-Processor with DDRIII

2015-10-11

REV: 1.0

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Security Classification		LC Future Center Secret Data		Title		
Issued Date	2015/10/08	Deciphered Date	2015/03/23	Cover Page		
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Power Plane State	B+	+3VALW +3VL	+3VALW_SOC +1.0VALW +1.8VALW	+1.35V	+5VS +3VS +1.5VS +0.68VS CPU_CORE GFX_CORE
S0	○	○	○	○	○
S3	○	○	○	○	✗
S5 S4/AC Only	○	○	○	✗	✗
S5 S4 Battery only	○	✗	✗	✗	✗
S5 S4 AC & Battery don't exist	✗	✗	✗	✗	✗

SIGNAL STATE	SLP_S1#	SLP_S3#	SLP_S4#	+VALW		+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	ON	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	ON	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	ON	OFF	OFF	OFF

SMBUS Control Table

	SOURCE	VGA	BATT	IT8986E	SODIMM	WLAN WiMAX	Thermal Sensor		Module	charger
EC_SMB_CK1 EC_SMB_DA1	EC +3VALW	X	V	V +3VALW	X	X	X	X	X	V
EC_SMB_CK2 EC_SMB_DA2	EC +3VS	V +3VGS	X	V +3VS	X	X	V +3VS	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	V +3VS	V +3VS	X	V +3VALW_PCH	X	X

EC SM Bus1 address		EC SM Bus2 address		PCH SM Bus address	
Device		Device	Address	Device	Address
Smart Battery	0001 011X b	Thermal Sensor EMC1403-2	1001_100xb(reserve)	DDR DIMMA	1010 000Xb
Charger	need to update	VGA	0x9E(base on NV default)	Wlan	Rsvd
				TP	need to update

SIGNAL STATE	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

XHCI	Port	Port device
USB 3.0	0	USB Port (Left Side)
	1	USB3.0 Card Reader
USB 2.0	0	USB Port (Left Side)
	1	USB Port (Right Side)
	2	BT
	3	Camera
	4	USB Port (Right Side)
USB HUB	1	
	2	
	3	
	4	

PCIE PORT LIST

Port	Device
1	Discrete GPU
2	Discrete GPU
3	WLAN
4	LAN
5	
6	
7	
8	

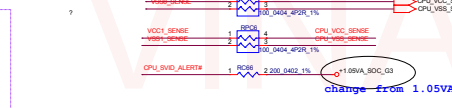
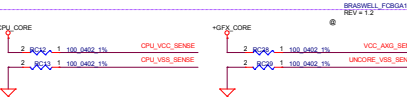
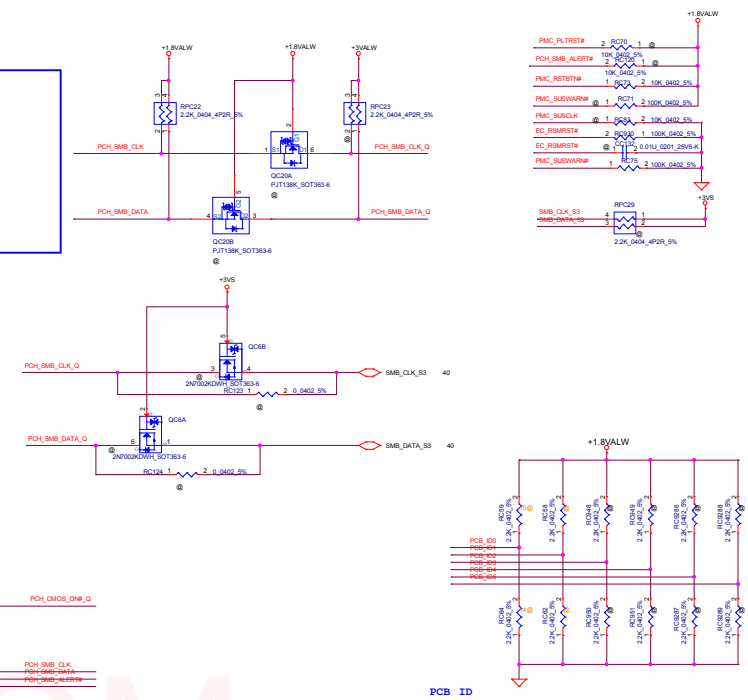
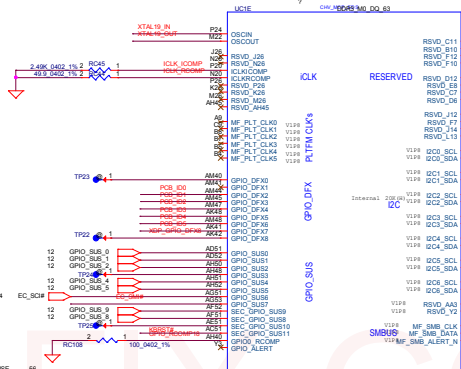
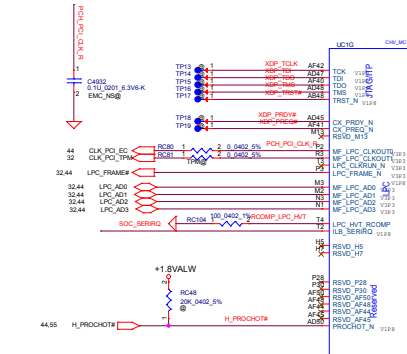
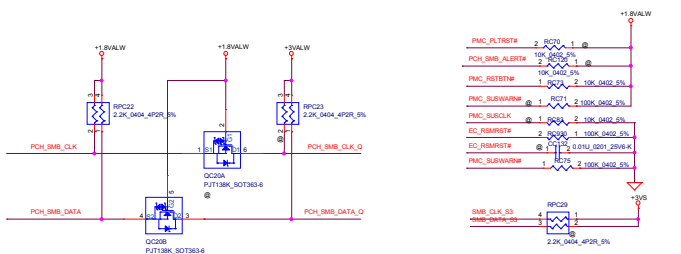
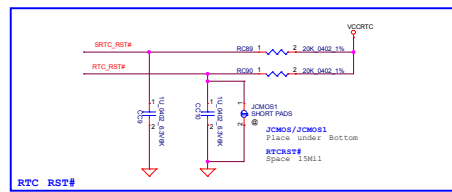
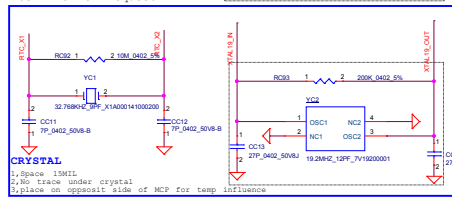
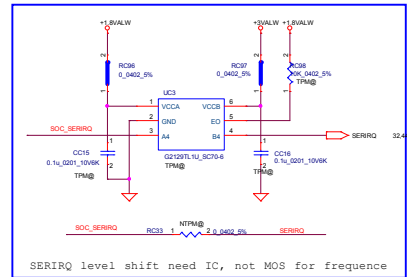
BOM Structure Table

[illegible]

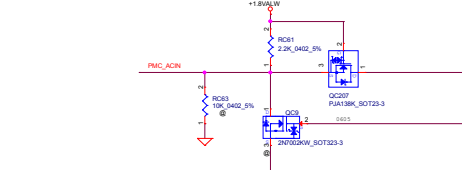
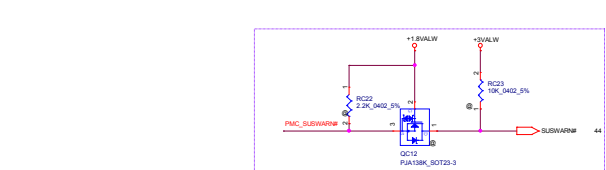
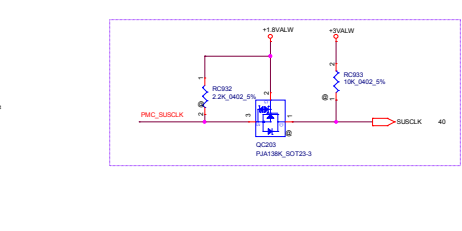
DDI PORT LIST

Port	Device
DDI0	DP TO VGA
DDI1	eDP
DDI2	HDMI

32.768K need change to SJ100001M0P,
as intel EDS New request



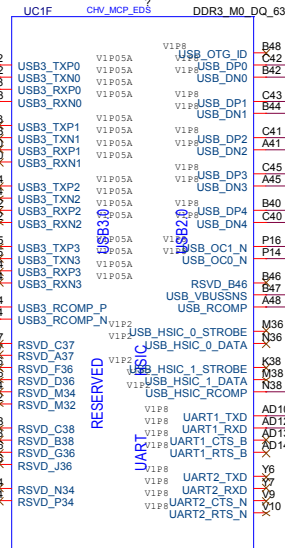
PCB ID	PCB 100	PCB 101	PCB 102	PCB 103	PCB 104	PCB 105	Description
0	X	X	X	X	X	X	Reserved
1	X	X	X	X	X	X	Reserved
2	X	X	X	X	X	X	Reserved
3	X	X	X	X	X	X	Reserved
4	X	X	X	X	X	X	Reserved
5	X	X	X	X	X	X	Reserved
6	X	X	X	X	X	X	Reserved
7	X	X	X	X	X	X	Reserved
8	X	X	X	X	X	X	Reserved
9	X	X	X	X	X	X	Reserved
10	X	X	X	X	X	X	Reserved
11	X	X	X	X	X	X	Reserved
12	X	X	X	X	X	X	Reserved
13	X	X	X	X	X	X	Reserved
14	X	X	X	X	X	X	Reserved
15	X	X	X	X	X	X	Reserved
16	X	X	X	X	X	X	Reserved
17	X	X	X	X	X	X	Reserved
18	X	X	X	X	X	X	Reserved
19	X	X	X	X	X	X	Reserved
20	X	X	X	X	X	X	Reserved
21	X	X	X	X	X	X	Reserved
22	X	X	X	X	X	X	Reserved
23	X	X	X	X	X	X	Reserved
24	X	X	X	X	X	X	Reserved
25	X	X	X	X	X	X	Reserved
26	X	X	X	X	X	X	Reserved
27	X	X	X	X	X	X	Reserved
28	X	X	X	X	X	X	Reserved
29	X	X	X	X	X	X	Reserved
30	X	X	X	X	X	X	Reserved
31	X	X	X	X	X	X	Reserved
32	X	X	X	X	X	X	Reserved
33	X	X	X	X	X	X	Reserved
34	X	X	X	X	X	X	Reserved
35	X	X	X	X	X	X	Reserved
36	X	X	X	X	X	X	Reserved
37	X	X	X	X	X	X	Reserved
38	X	X	X	X	X	X	Reserved
39	X	X	X	X	X	X	Reserved
40	X	X	X	X	X	X	Reserved
41	X	X	X	X	X	X	Reserved
42	X	X	X	X	X	X	Reserved
43	X	X	X	X	X	X	Reserved
44	X	X	X	X	X	X	Reserved
45	X	X	X	X	X	X	Reserved
46	X	X	X	X	X	X	Reserved
47	X	X	X	X	X	X	Reserved
48	X	X	X	X	X	X	Reserved
49	X	X	X	X	X	X	Reserved
50	X	X	X	X	X	X	Reserved
51	X	X	X	X	X	X	Reserved
52	X	X	X	X	X	X	Reserved
53	X	X	X	X	X	X	Reserved
54	X	X	X	X	X	X	Reserved
55	X	X	X	X	X	X	Reserved
56	X	X	X	X	X	X	Reserved
57	X	X	X	X	X	X	Reserved
58	X	X	X	X	X	X	Reserved
59	X	X	X	X	X	X	Reserved
60	X	X	X	X	X	X	Reserved
61	X	X	X	X	X	X	Reserved
62	X	X	X	X	X	X	Reserved
63	X	X	X	X	X	X	Reserved
64	X	X	X	X	X	X	Reserved
65	X	X	X	X	X	X	Reserved
66	X	X	X	X	X	X	Reserved
67	X	X	X	X	X	X	Reserved
68	X	X	X	X	X	X	Reserved
69	X	X	X	X	X	X	Reserved
70	X	X	X	X	X	X	Reserved
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73	X	X	X	X	X	X	Reserved
74	X	X	X	X	X	X	Reserved
75	X	X	X	X	X	X	Reserved
76	X	X	X	X	X	X	Reserved
77	X	X	X	X	X	X	Reserved
78	X	X	X	X	X	X	Reserved
79	X	X	X	X	X	X	Reserved
80	X	X	X	X	X	X	Reserved
81	X	X	X	X	X	X	Reserved
82	X	X	X	X	X	X	Reserved
83	X	X	X	X	X	X	Reserved
84	X	X	X	X	X	X	Reserved
85	X	X	X	X	X	X	Reserved
86	X	X	X	X	X	X	Reserved
87	X	X	X	X	X	X	Reserved
88	X	X	X	X	X	X	Reserved
89	X	X	X	X	X	X	Reserved
90	X	X	X	X	X	X	Reserved
91	X	X	X	X	X	X	Reserved
92	X	X	X	X	X	X	Reserved
93	X	X	X	X	X	X	Reserved
94	X	X	X	X	X	X	Reserved
95	X	X	X	X	X	X	Reserved
96	X	X	X	X	X	X	Reserved
97	X	X	X	X	X	X	Reserved
98	X	X	X	X	X	X	Reserved
99	X	X	X	X	X	X	Reserved
100	X	X	X	X	X	X	Reserved



LEFT USB (3.0)

41 USB30_TX_P0
41 USB30_TX_N0
41 USB30_RX_P0
41 USB30_RX_N0

USB30_TX_P0
USB30_TX_N0
USB30_RX_P0
USB30_RX_N0



41 USB20_P0
41 USB20_N0
41 USB20_P1
41 USB20_N1
30 USB20_P2
30 USB20_N2
40 USB20_P3
40 USB20_N3
33 USB20_P4
33 USB20_N4
41 USB_OC1#
41 USB_OC0#

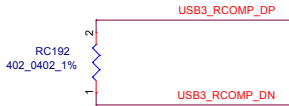
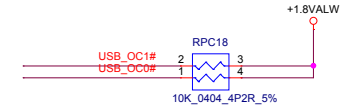
LEFT USB (3.0)

LEFT USB (2.0)

Card reader (2.0)

BT

Camera



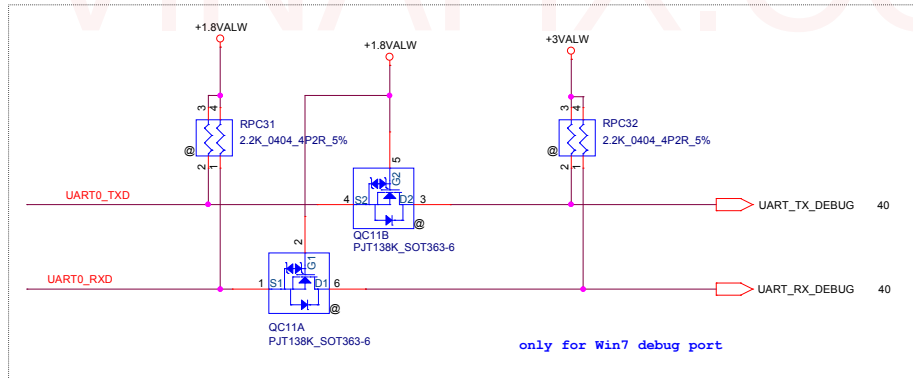
USB3_RCOMP_DP
USB3_RCOMP_DN

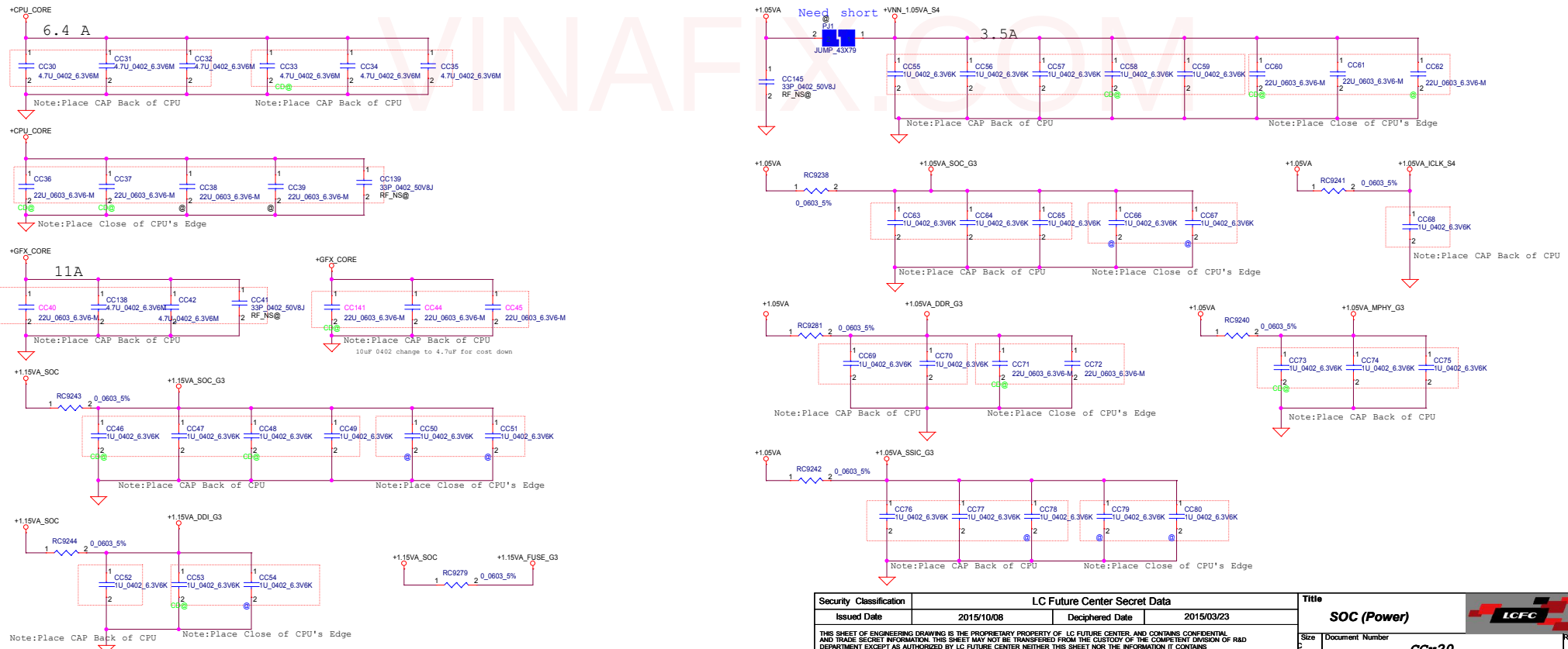
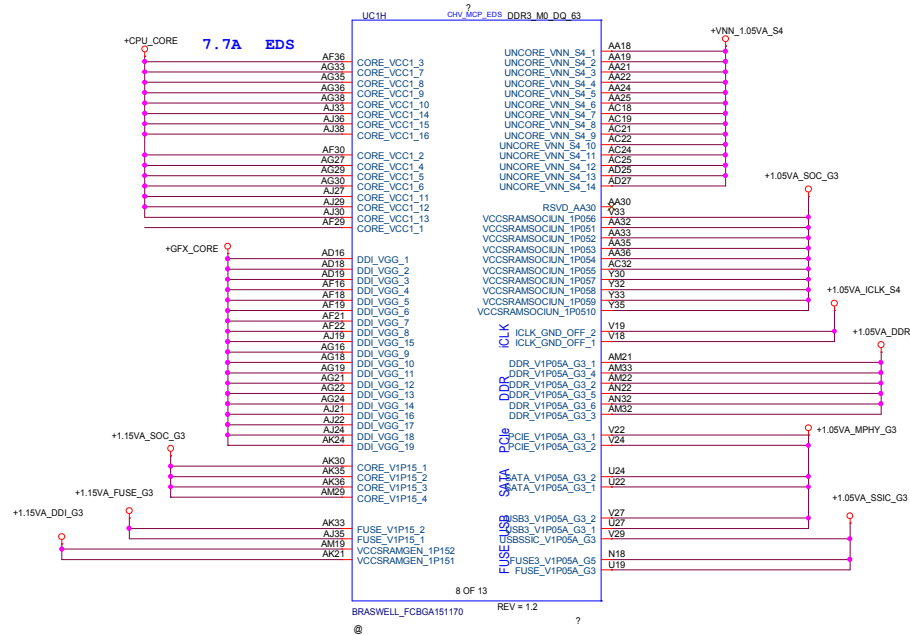
RSVD_C37
RSVD_A37
RSVD_F36
RSVD_D36
RSVD_M34
RSVD_M32
RSVD_C38
RSVD_B38
RSVD_G36
RSVD_J36
RSVD_N34
RSVD_P34

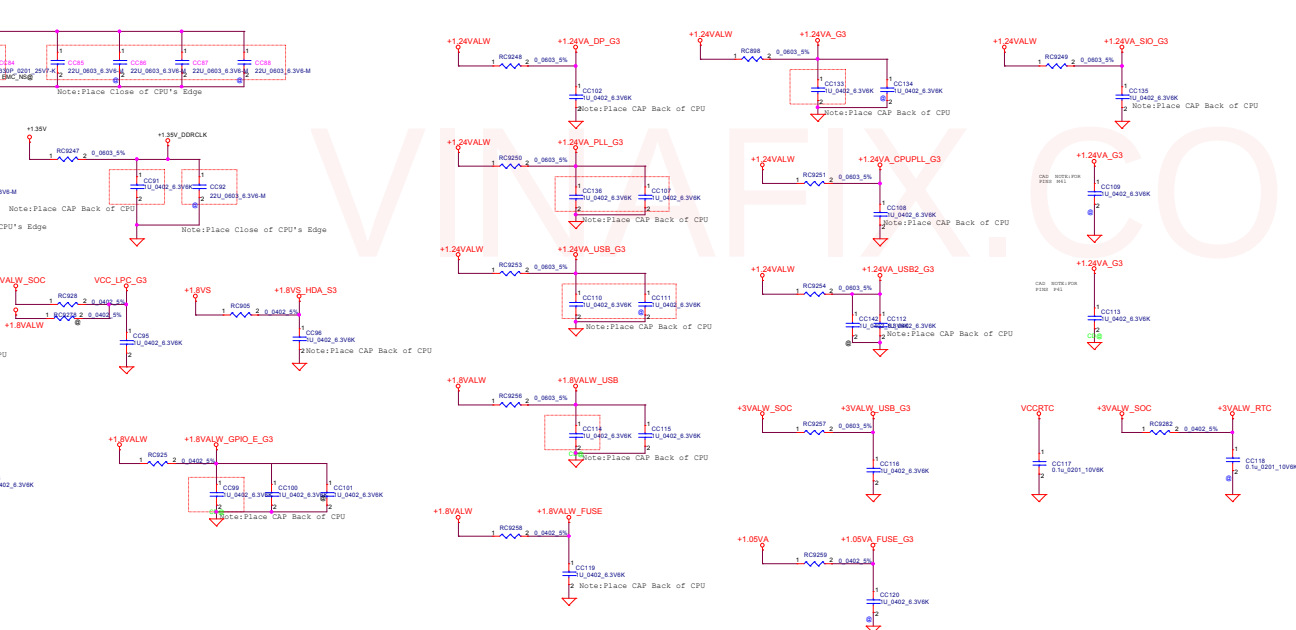
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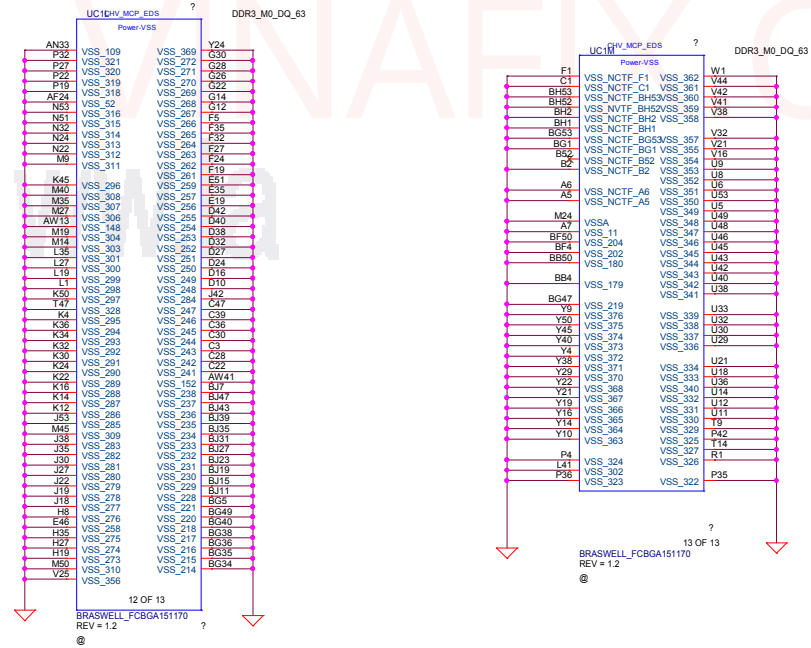
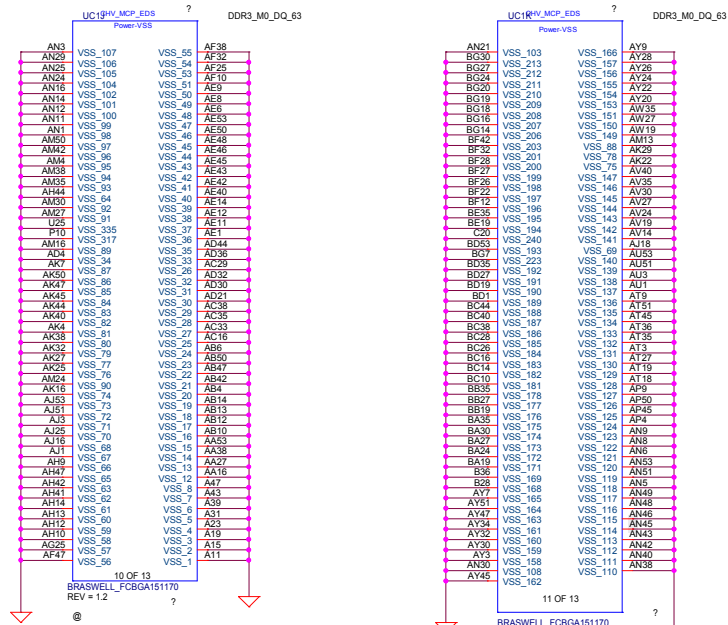
?

only for Win7 debug port



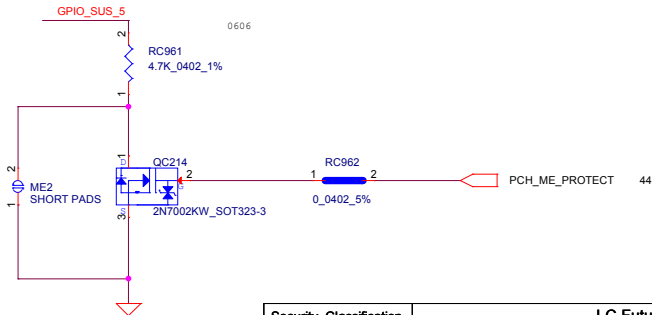
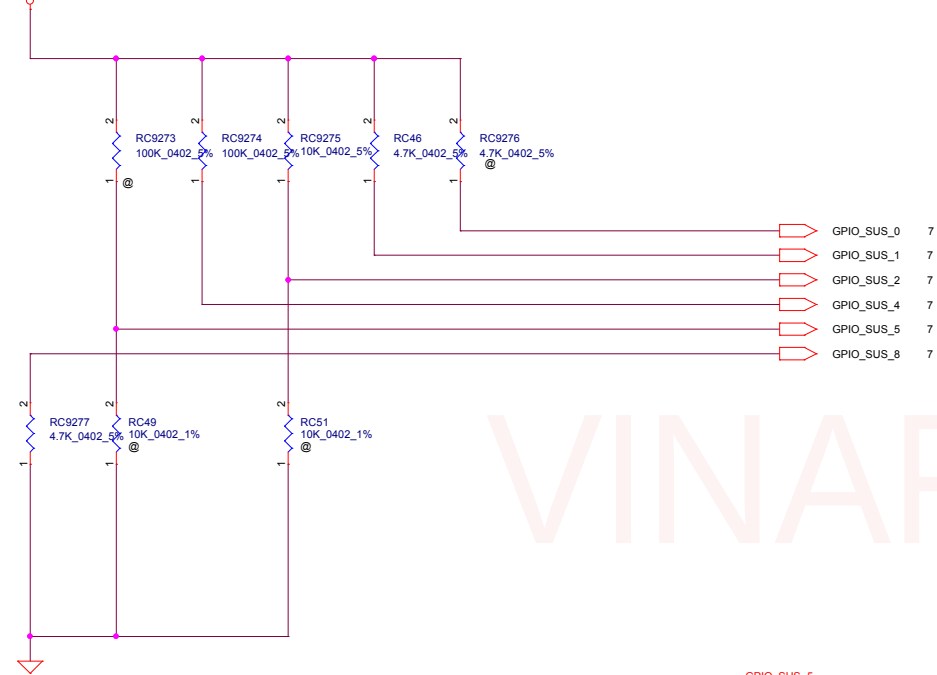




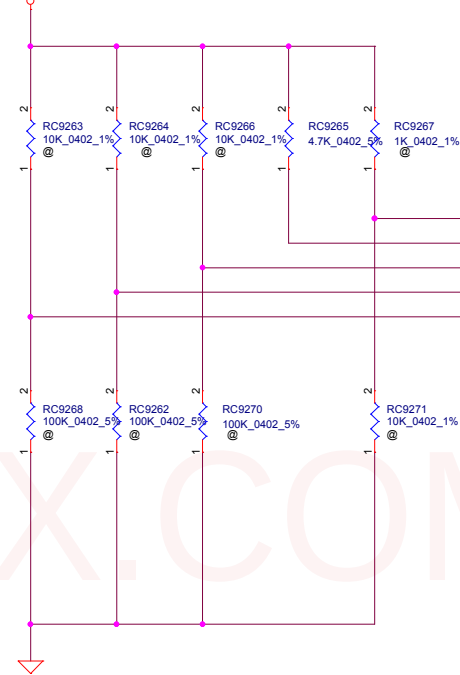


Hardware STRAPS (Follow up CRB)

+1.8VALW



+1.8VALW



GPIO_SUS_6
EC_SC#
GPIO_CAM_8
GPIO_CAM_9
GPIO_CAM_11

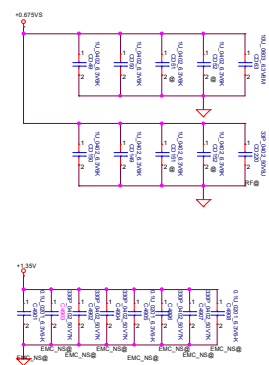
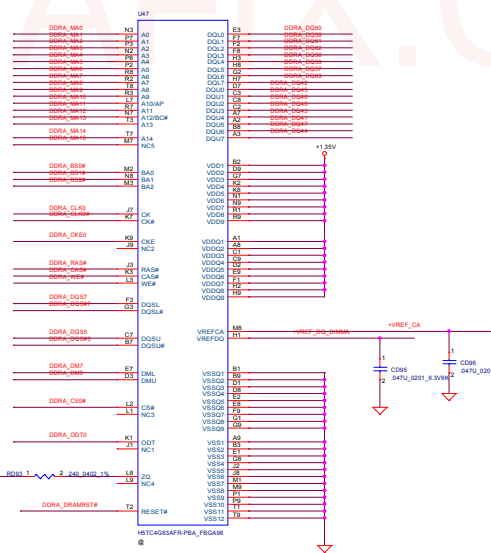
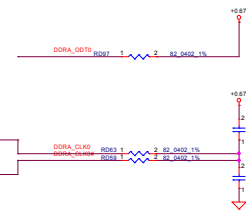
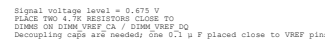
7
7.44
4
4
4

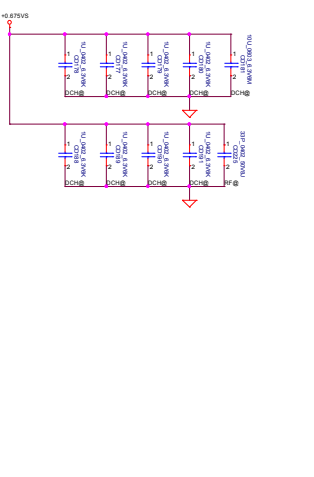
Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_SUS[0]	DDI0 Detect	Weak internal (20k PD)	0 = DDI0 not detected 1 = DDI0 detected
GPIO_SUS[1]	DDI1 Detect	Weak internal (20k PD)	0 = DDI1 not detected 1 = DDI1 detected
GPIO_SUS[2]	Top Swap (A16) override	Weak internal (20k PU)	0 = Change Boot Loader address 1 = Normal Operation
GPIO_SUS[3]	MIPI-DSI Display Detect	Weak internal (20k PD)	0 = DSI Port not detected 1 = DSI Port detected Note: DSI is not POR for BSW. This strap will not enable DSI on BSW. Leave the pin floating if GPIO functionality is not used.
GPIO_SUS[4]	Boot BIOS Strap (BBS)	Weak internal (20k PU)	0 = No SPI (Default) 1 = SPI
GPIO_SUS[5]	Flash Descriptor Security Override	Weak internal (20k PU)	0 = Not supported 1 = Normal Operation
GPIO_SUS[6]	Halt Boot Strap	Weak internal (20k PU)	1 = Normal Operation Note: This strap MUST be High at RSMRST_N de-assert to ensure proper platform operation and use of GPIO_DFX[8:0]
GPIO_SUS[8]	PLLs, ICLK, USB2, DDI SFR Supply Select	Weak internal (20k PU)	0 = Supply is 1.25V 1 = Supply is 1.35V
GPIO_SUS[9]	ICLK, USB2, DDI SFR Bypass	Weak internal (20k PD)	0 = No bypass 1 = Bypass with 1.05V
GPIO_CAMERASB08	ICLK Xtal OSC Bypass	Weak internal (20k PD)	0 = No Bypass (Default) 1 = Bypass
GPIO_CAMERASB09	CCU SUS RO Bypass	Weak internal (20k PD)	0 = No Bypass (Default) 1 = Bypass
GPIO_CAMERASB11	RTC OSC Bypass	Weak internal (20k PD)	0 = No Bypass (Default) 1 = Bypass

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2015/10/08		2015/03/23			
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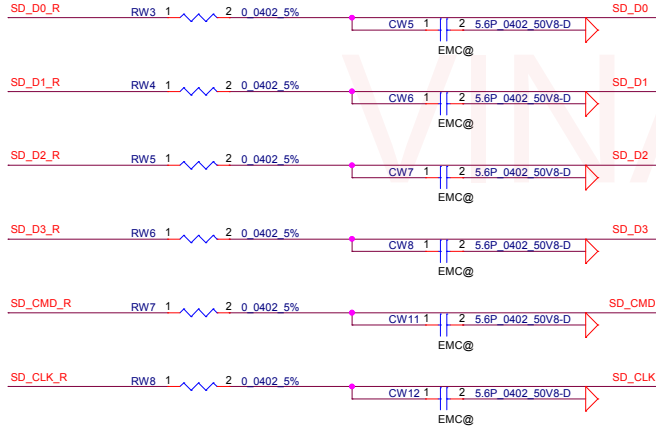
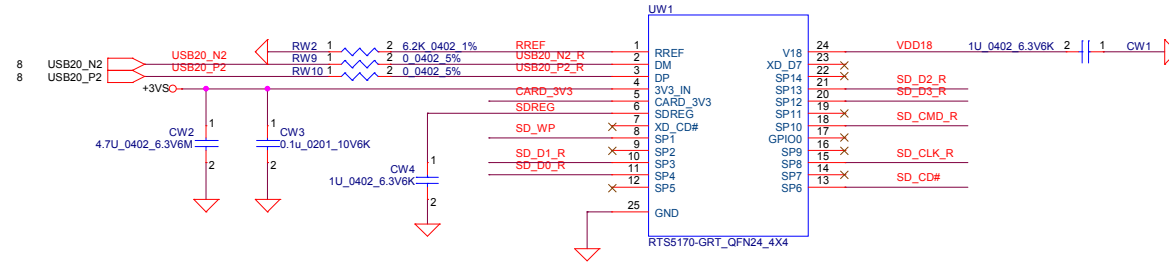
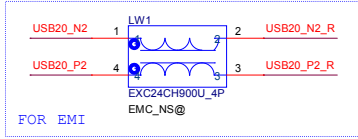
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				Sheet 27	Rev 1.0

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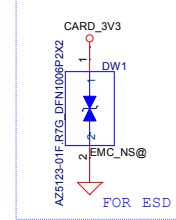
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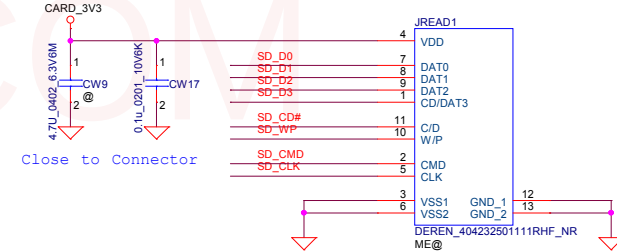
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Close to Connector



SD / MMC



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Document Number		CGx20		Rev	
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		57		1.0	

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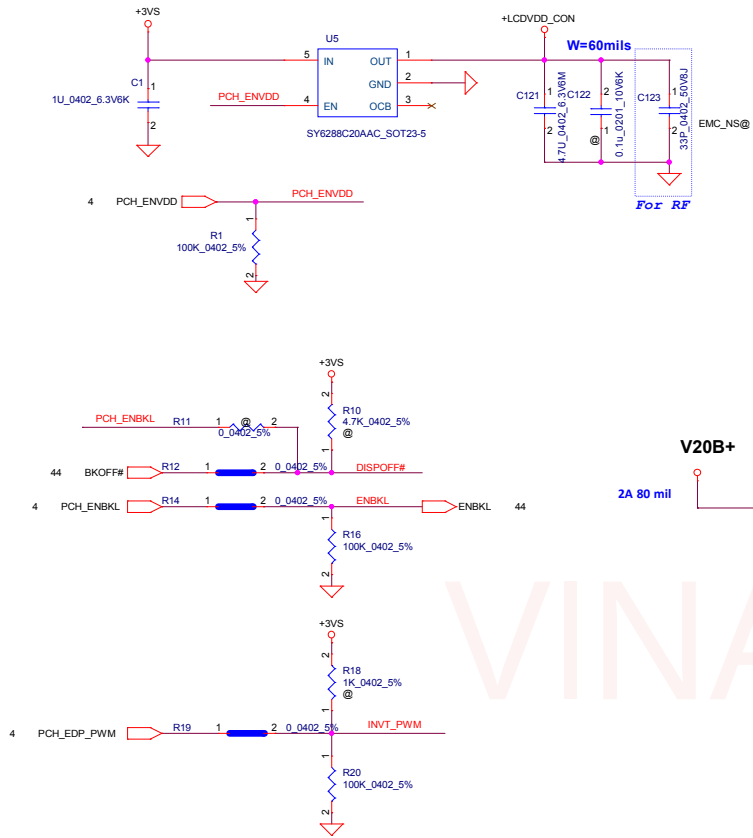
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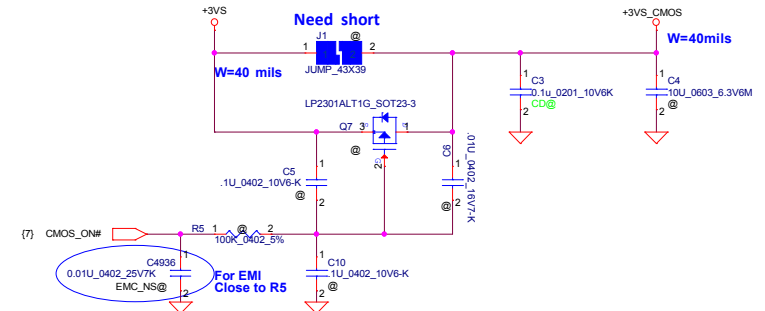
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LCD POWER CIRCUIT

W=60mils

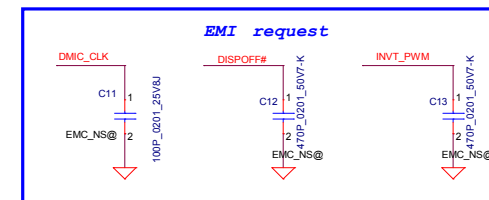
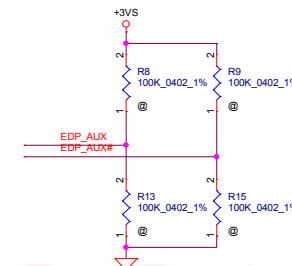
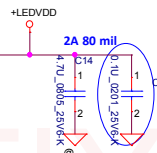


CMOS Camera

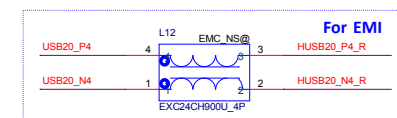
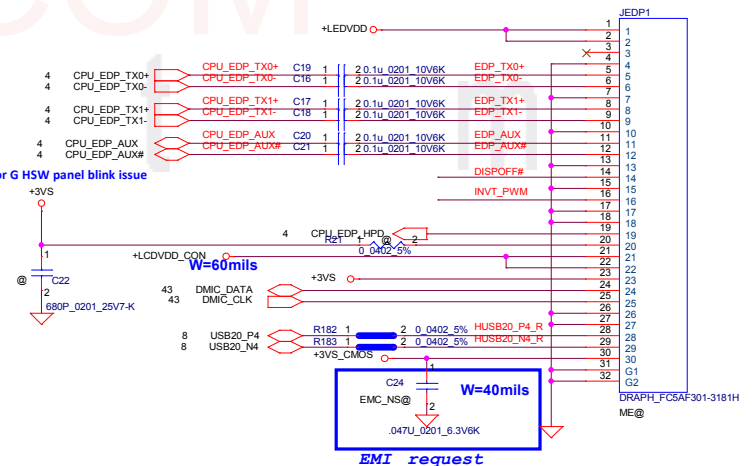


V20B+

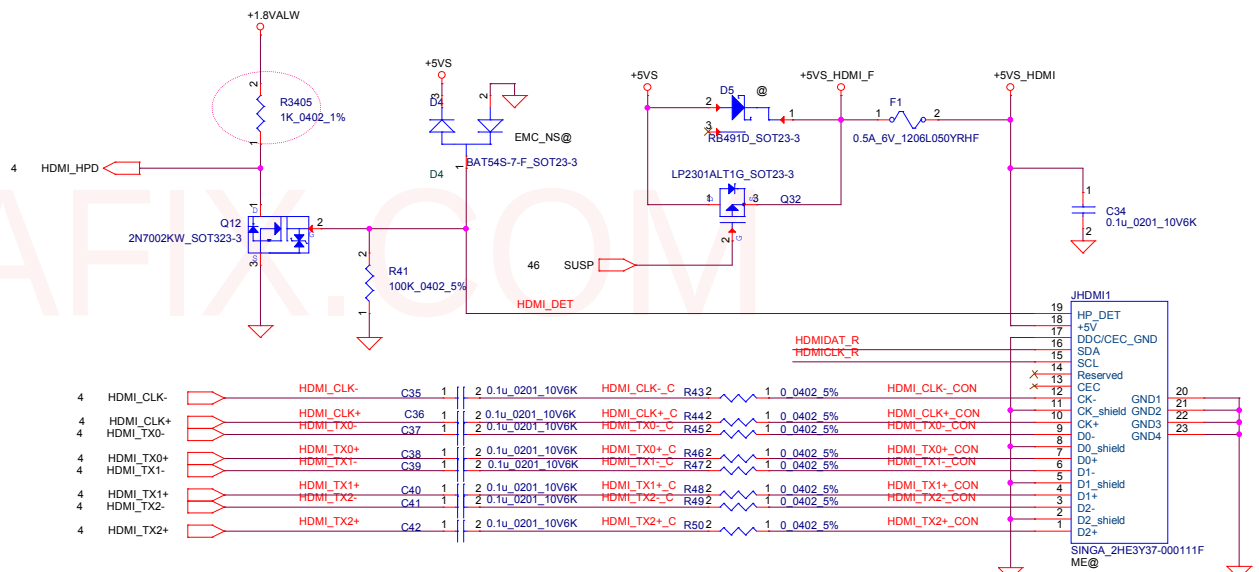
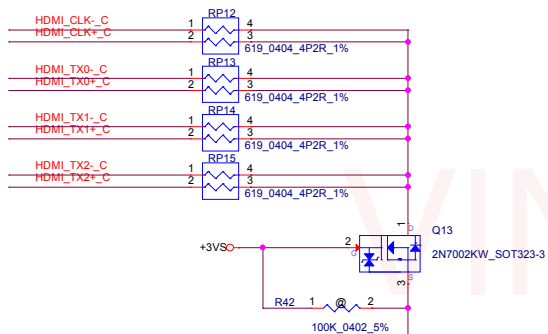
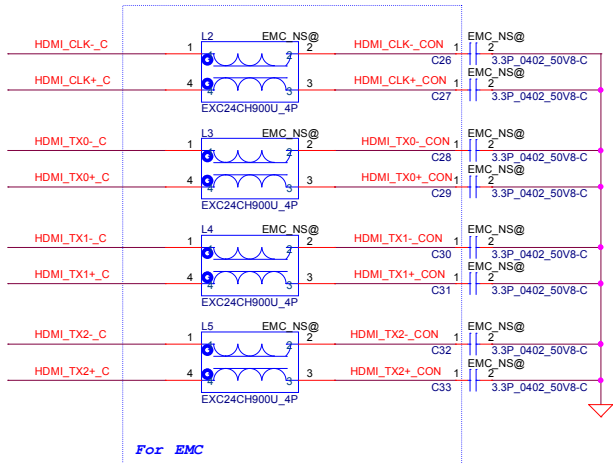
2A 80 mil



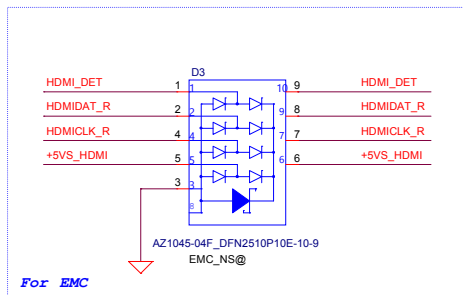
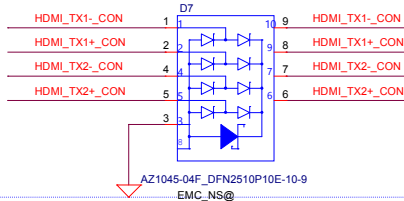
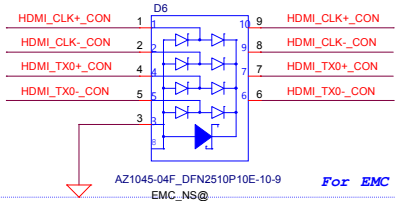
C23 0.1u for G HSW panel blink issue



Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/10/08	Deciphered Date	2015/03/23	eDP/ CMOS/Touch screen	
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Close to JHDMI1



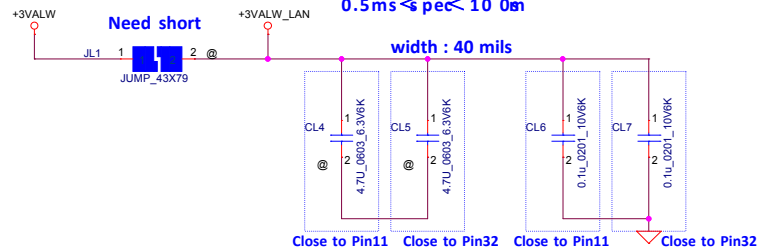
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Date:				Tuesday, December 08, 2015	
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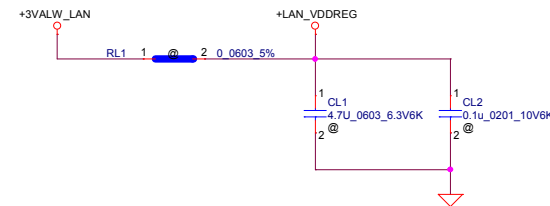
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				Custom	CGx20	1.0
				Date:	Tuesday, December 08, 2015	Sheet 36 of 57

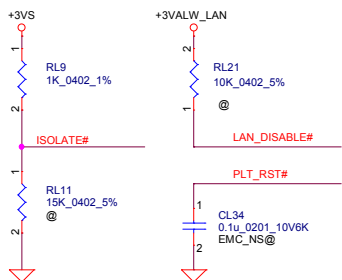
+3VALW TO +3VALW_LAN



+3VALW_LAN rising time (10%~90%)
0.5ms < t_{spec} < 10.0ms

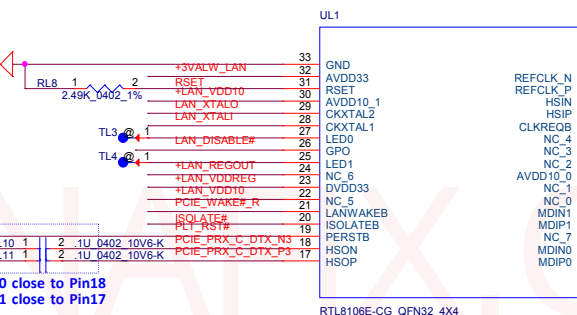


40,44 LAN_WAKE# RL6 1 2 0.0402 5% PCIE_WAKE#_R

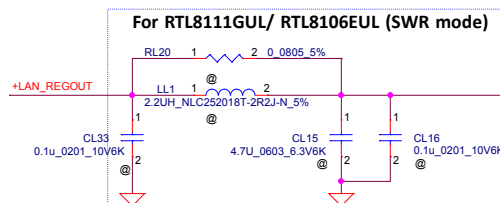
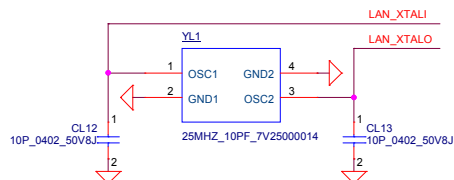


7,32,40,44 PLT_RST#
6 PCIE_PRX_DTX_N3
6 PCIE_PRX_DTX_P3

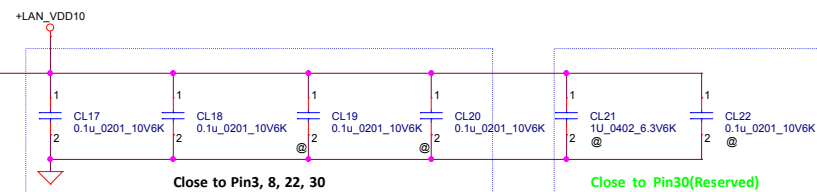
CL10 1 2 .1U 0402 10V6-K
CL11 1 2 .1U 0402 10V6-K
CL10 close to Pin18
CL11 close to Pin17



100M LAN



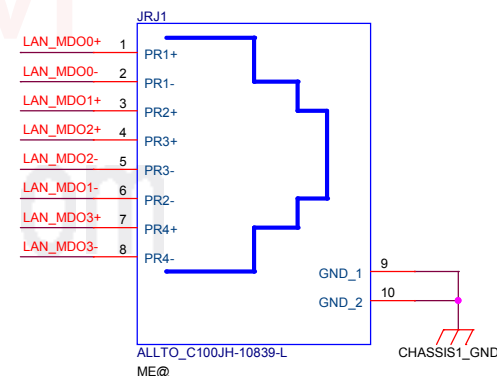
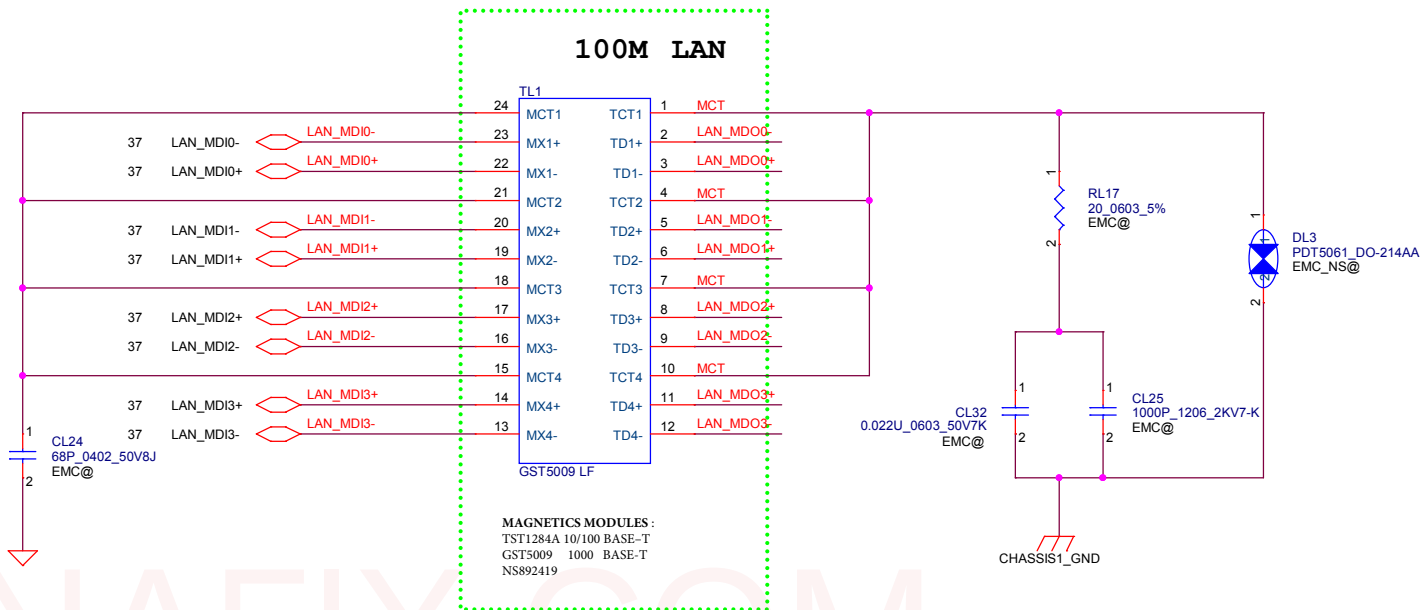
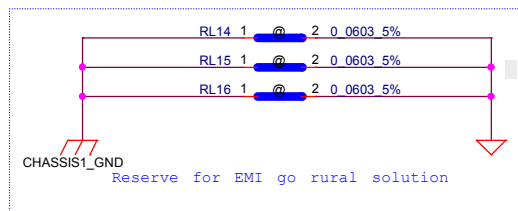
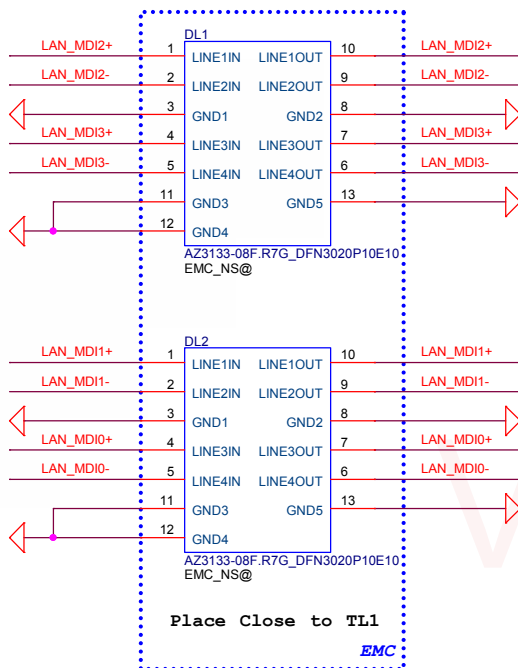
Layout Note: LL1 must be within 200mil to Pin24,
CL15,CL16 must be within 200mil to LL1
+LAN_REGOUT: Width =60mil



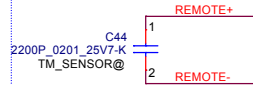
LAN_CLKREQ#_R RL18 2 0.0402 5% LAN_CLKREQ# 6

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LAN_RTL8106EUL		CGx20	
Size	Custom	Document Number	Rev 1.0
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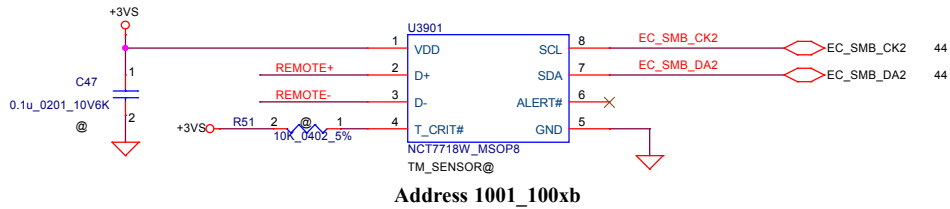


Close to U3901

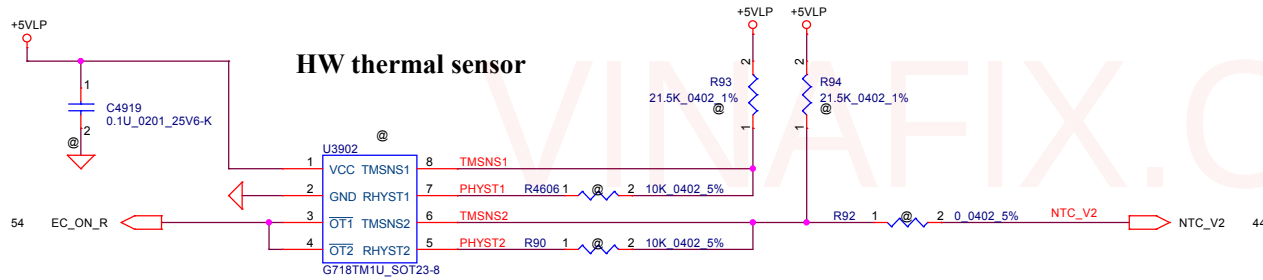


REMOTE+/- R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

SMSC thermal sensor placed near DIMM

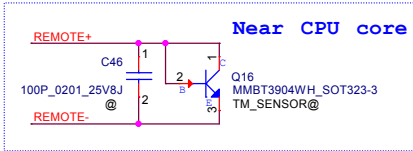
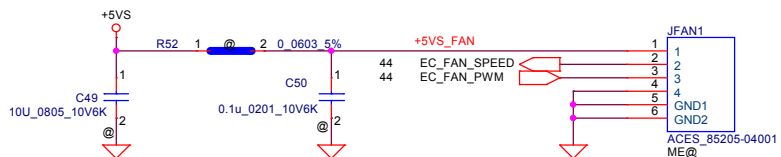


HW thermal sensor

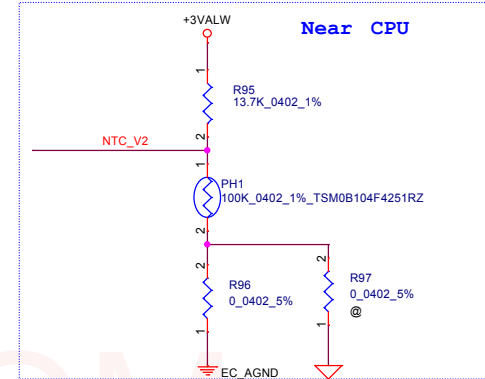


over temperature threshold:
 $RSET=3 \times RTMH$
 $92 \pm 30C$
Hysteresis temperature threshold.
 $RHYST=(RSET \times RTML) / (3 \times RTML - RSET)$
 $56 \pm 30C$

FAN Conn



Baytrail SOC use thermal sensor to read the thermal,
Baytrail don't has PECI signal

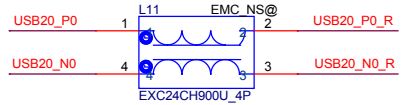
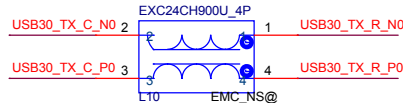
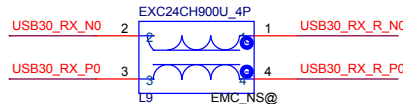
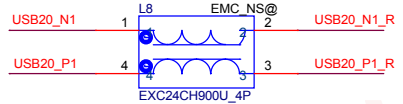
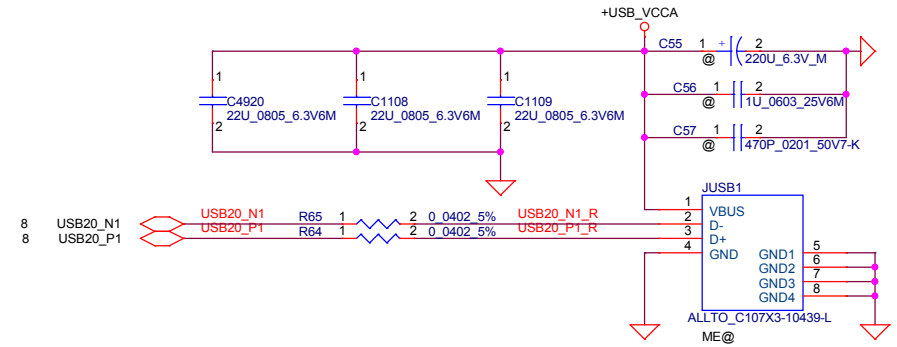
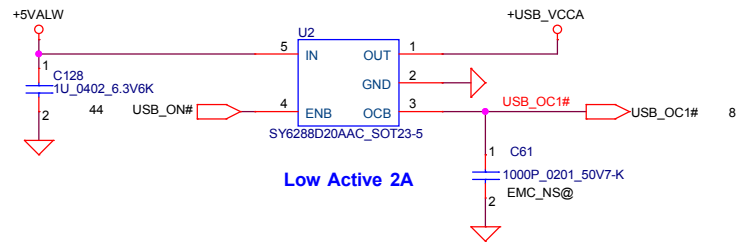


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Size	Document Number			Rev	
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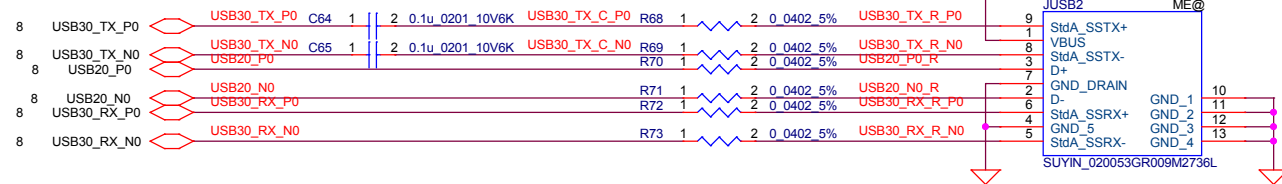
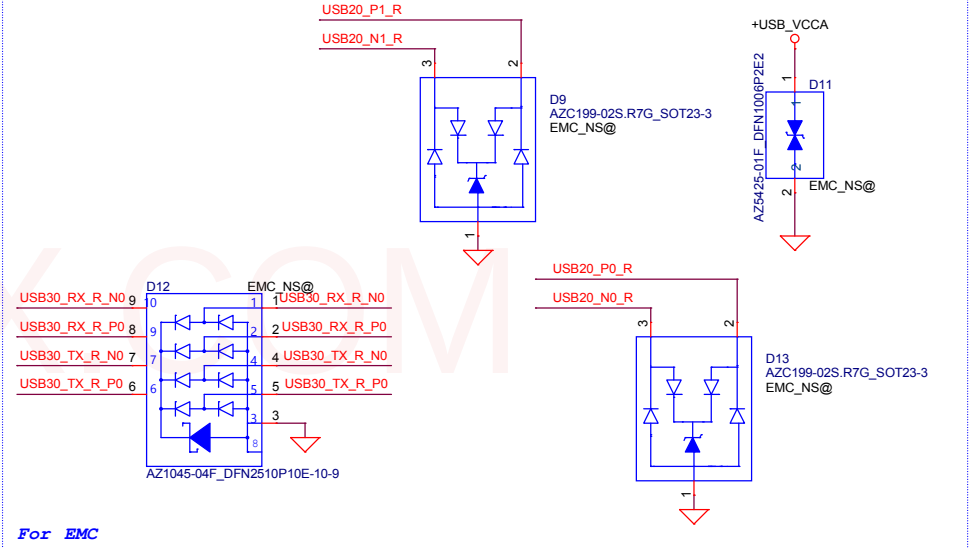
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Issued Date		2015/10/08		Deciphered Date		2015/03/23				NGFF WLAN					
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LEFT SIDE USB PORT X2

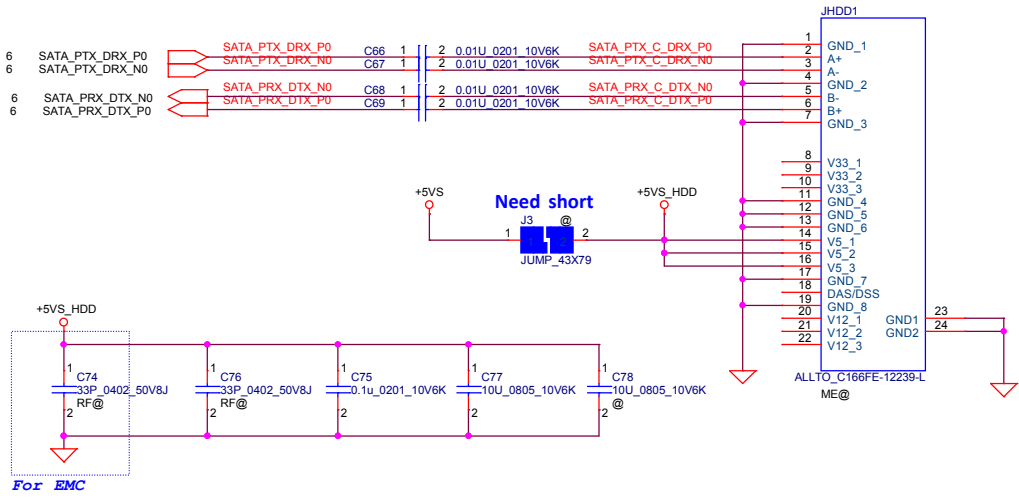


For EMC

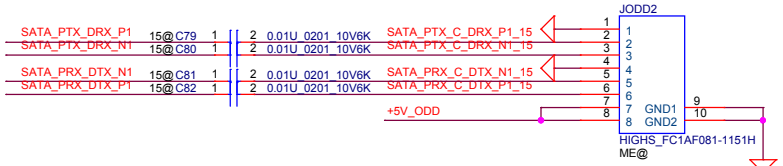


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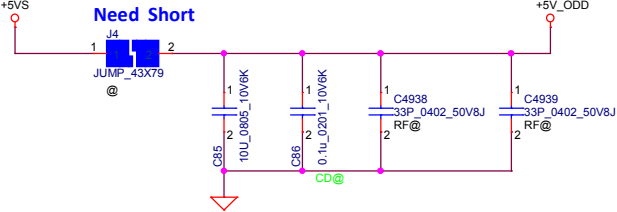
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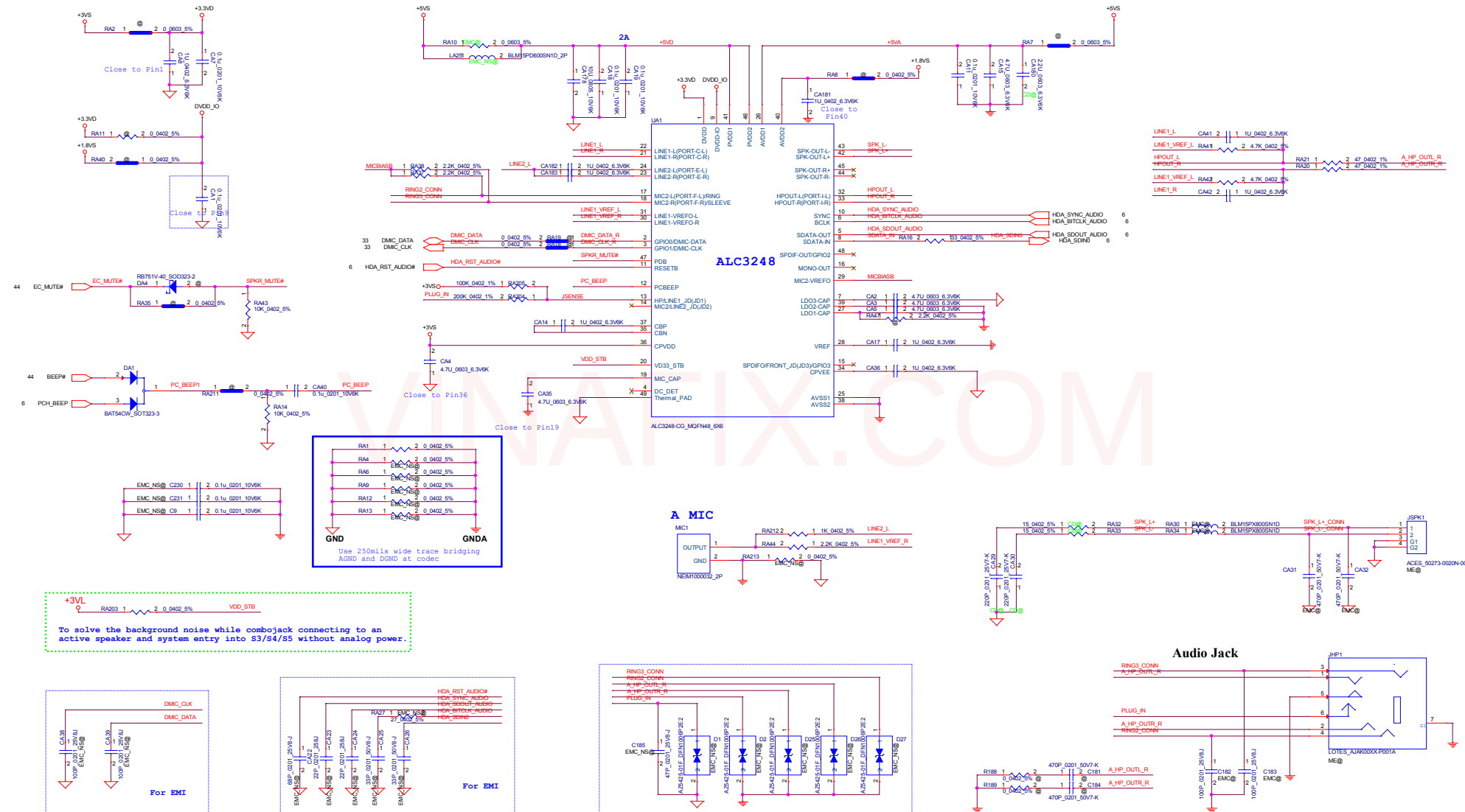


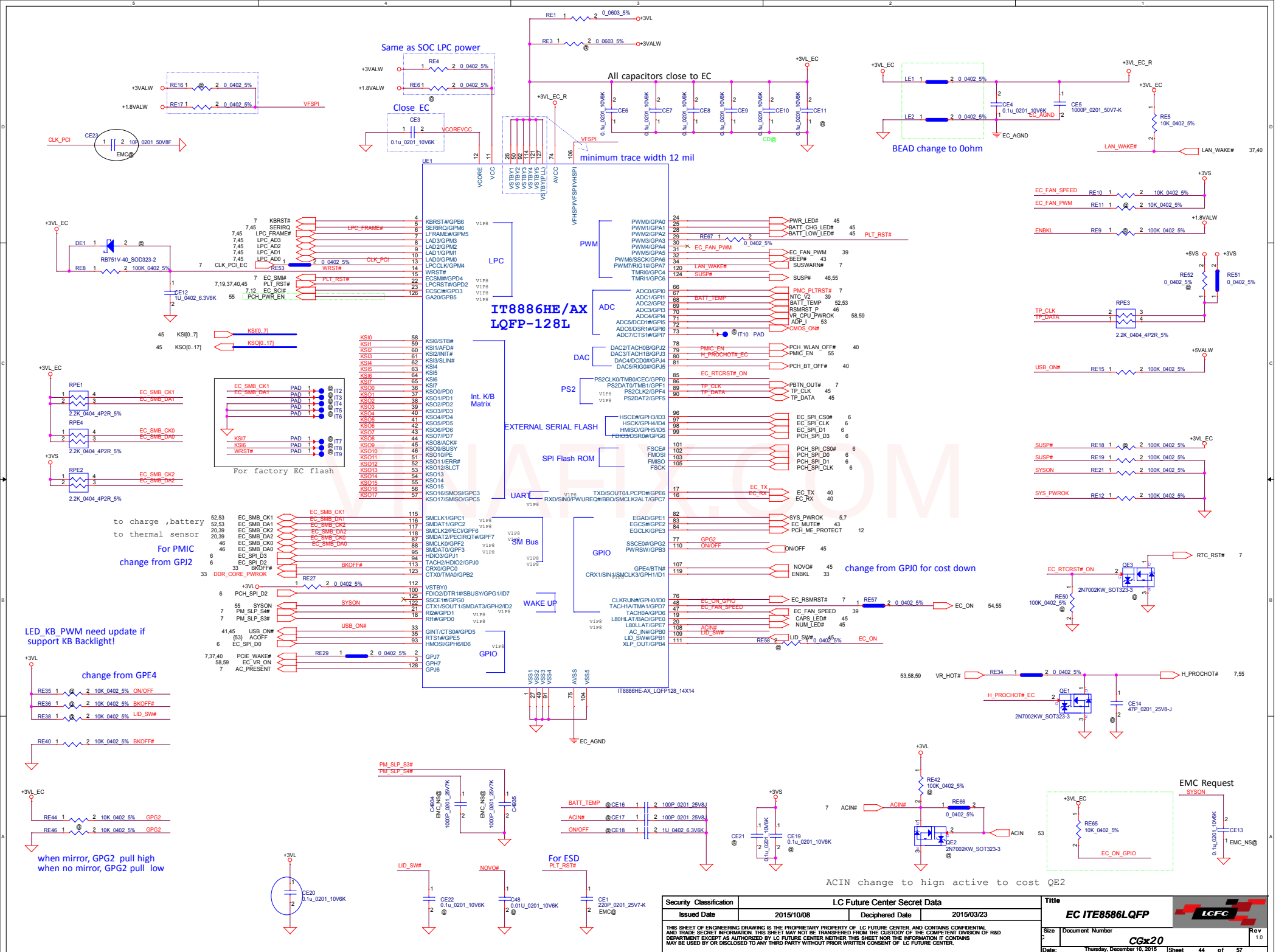
FOR 15"
SATA ODD FFC Conn



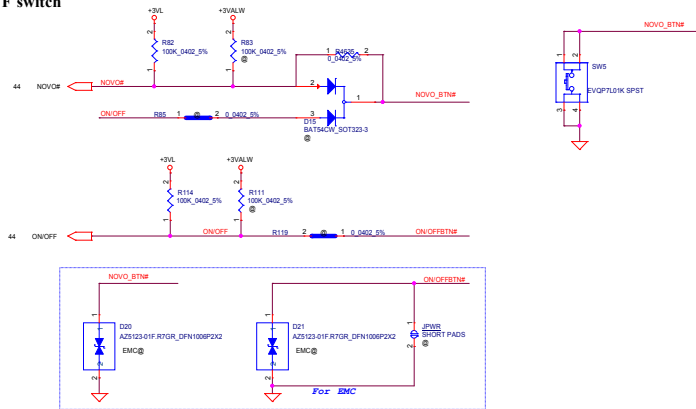
Need Short



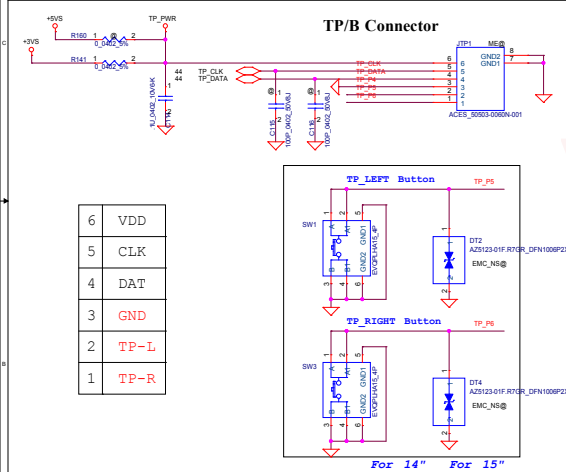
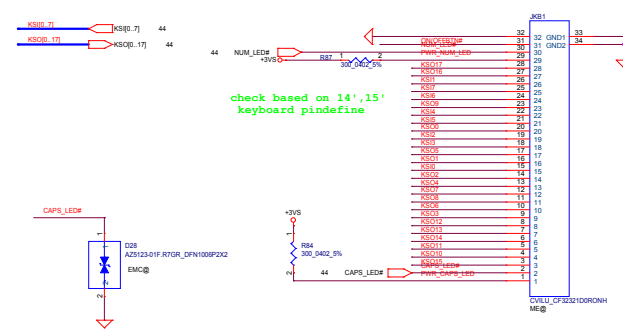




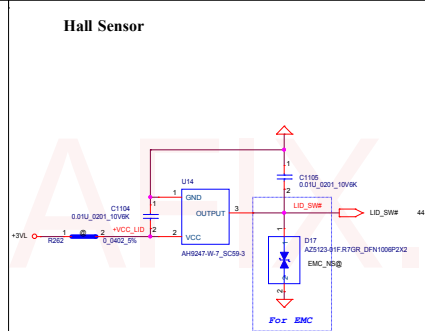
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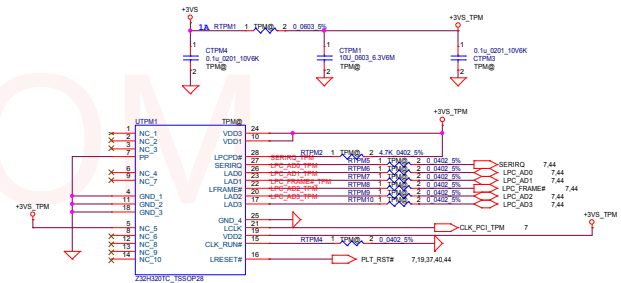
K/B Connector



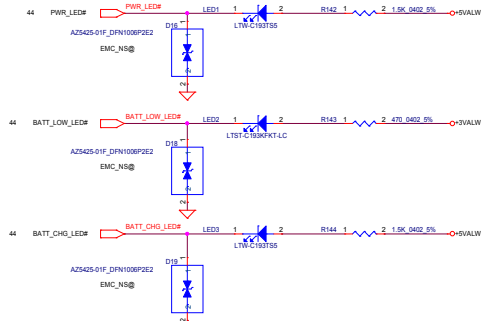
Hall Sensor



TPM



LED

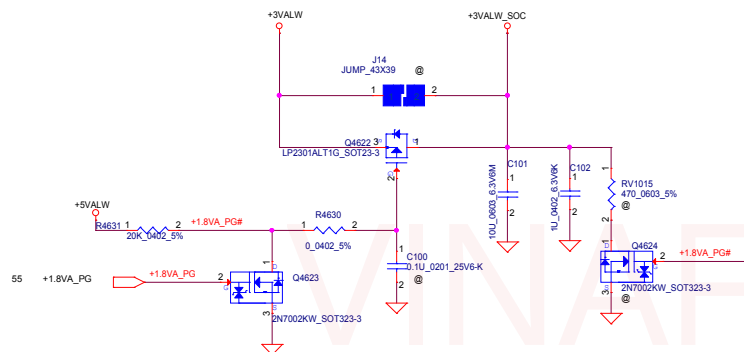
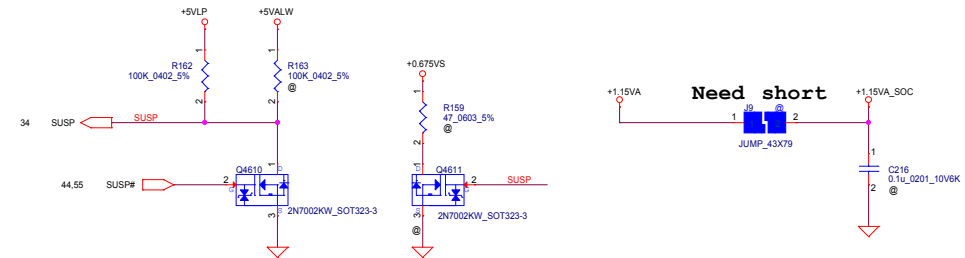
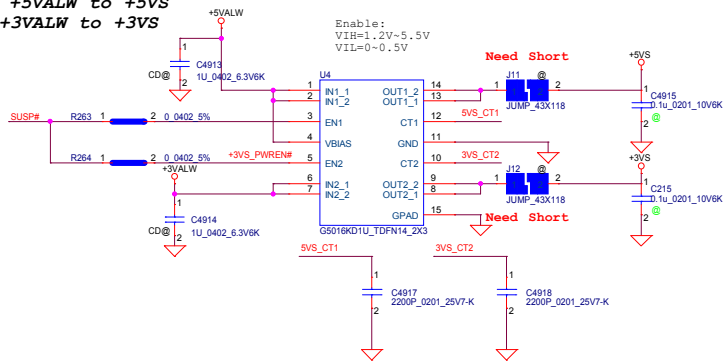


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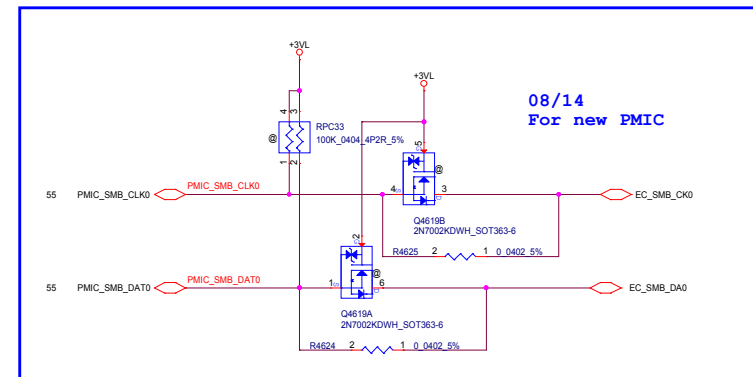
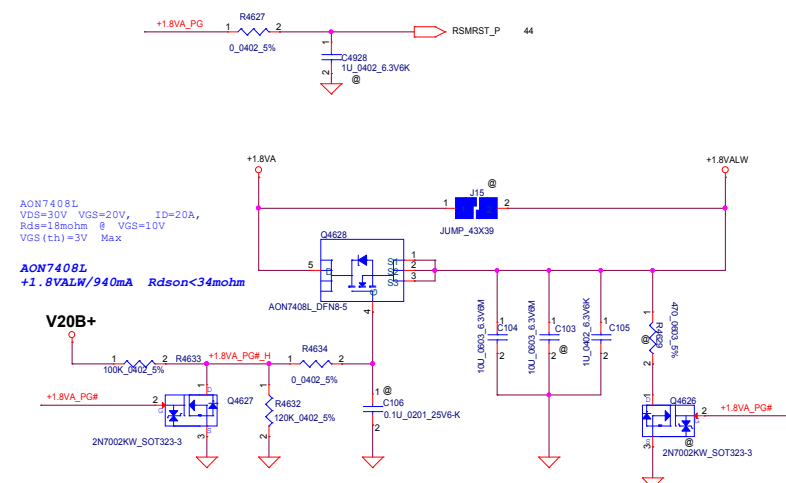
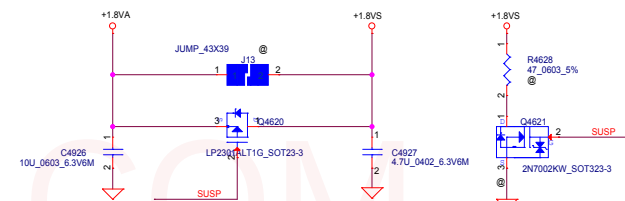
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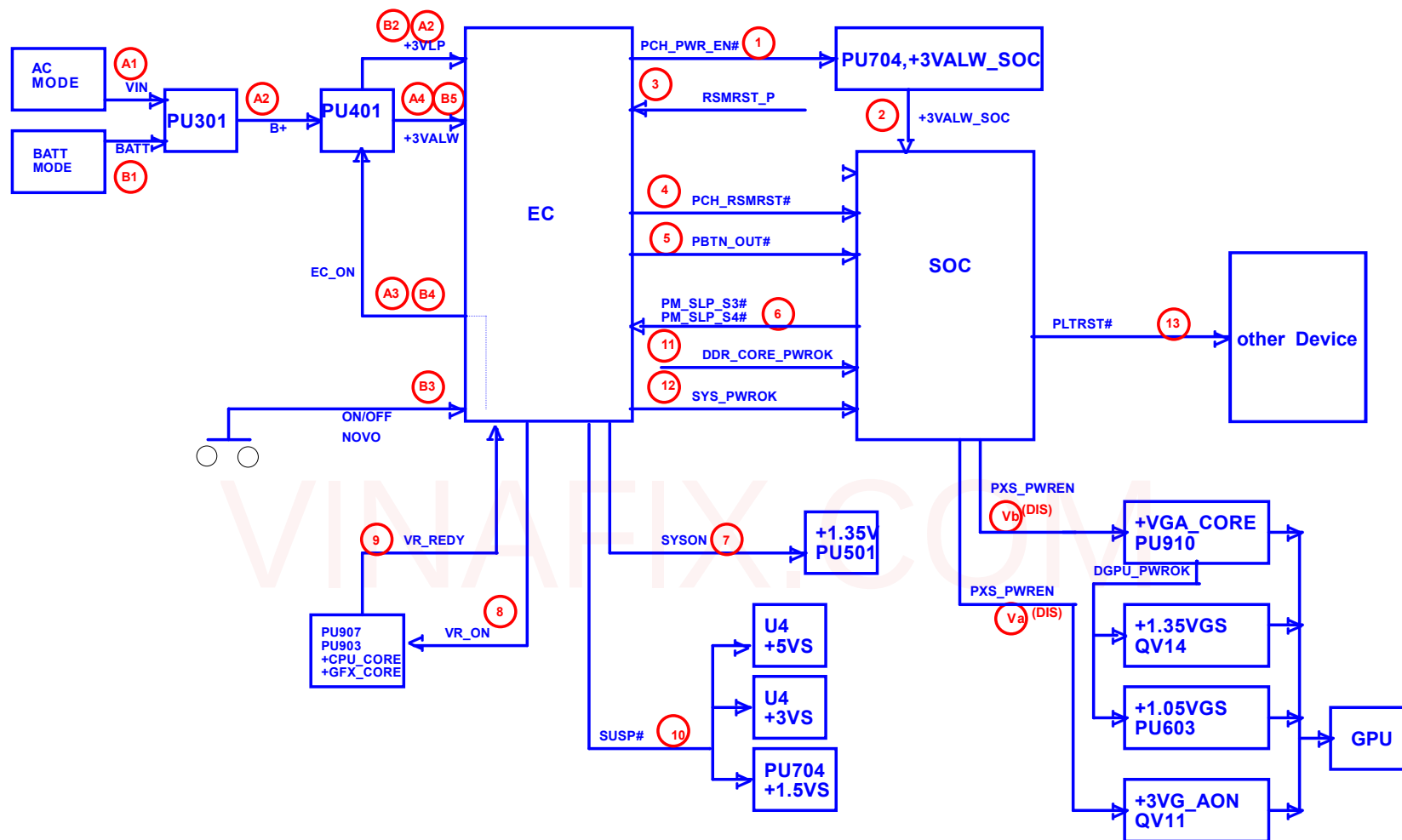
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+5VALW to +5VS
+3VALW to +3VS



+1.5VS is 1.8V voltage rail
(CPU HD Audio Rail support 1.8V, Codec also Support 1.8V)

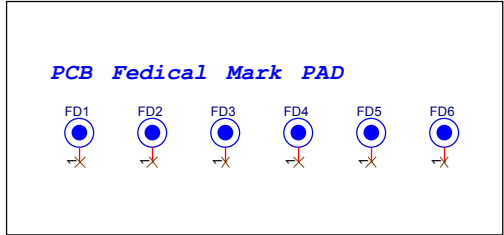
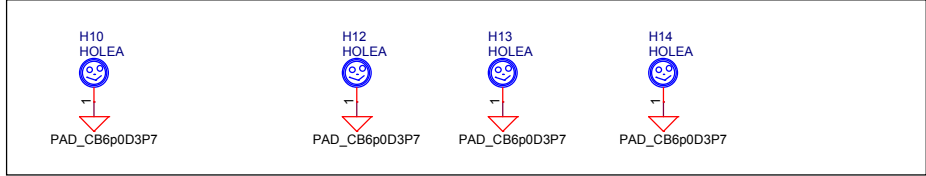
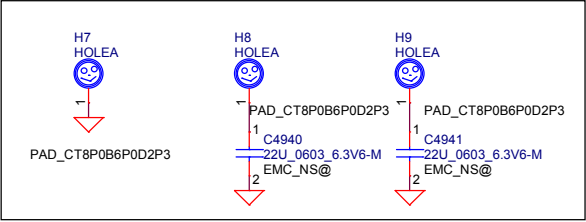
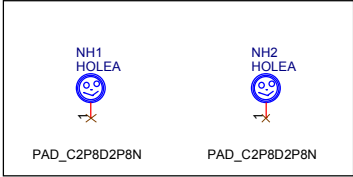
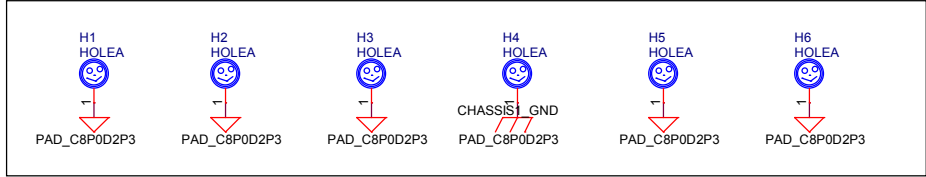




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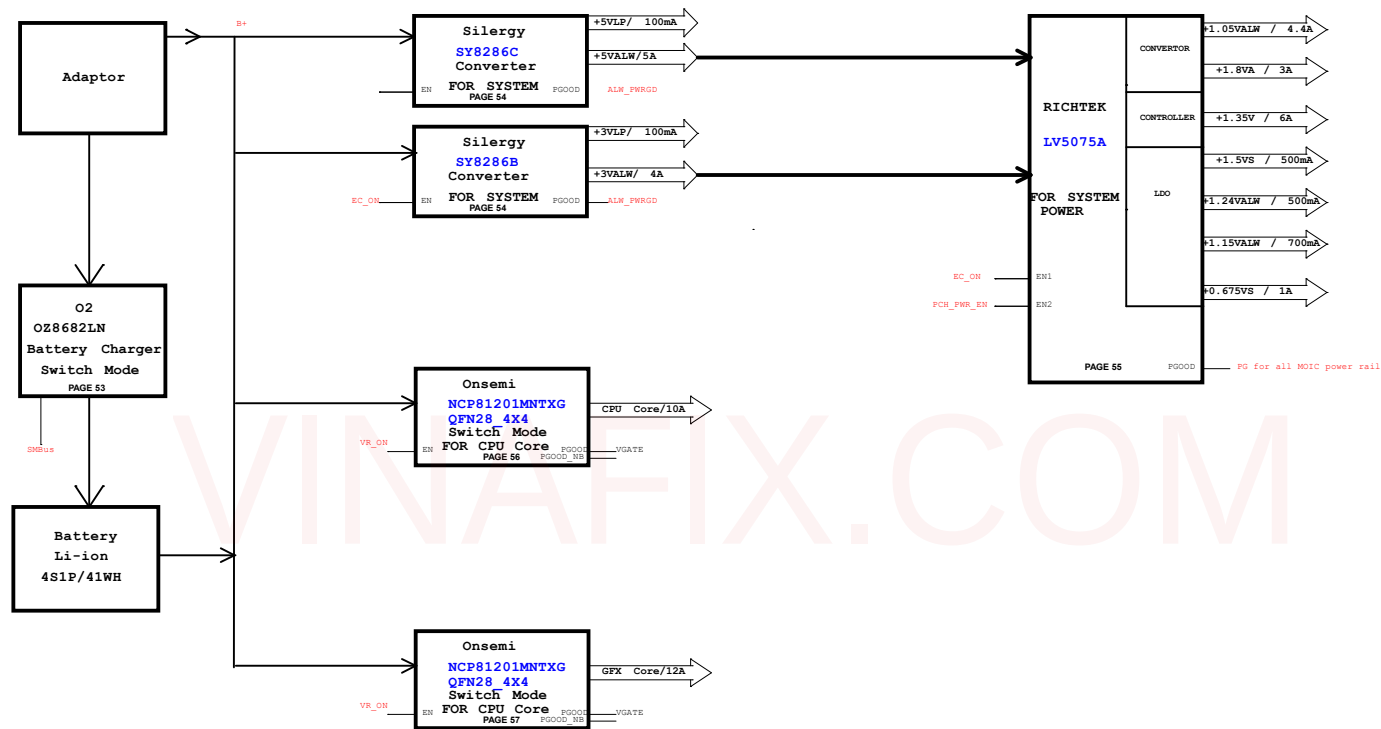
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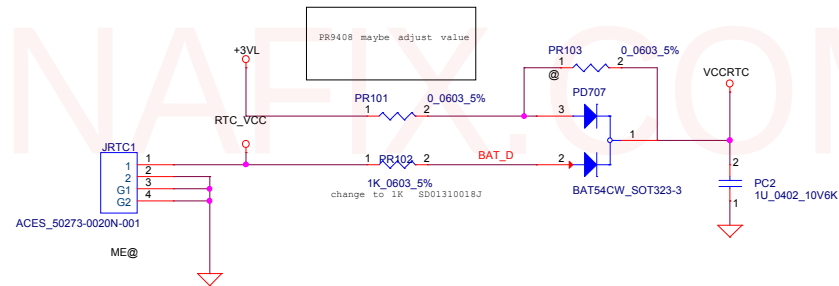
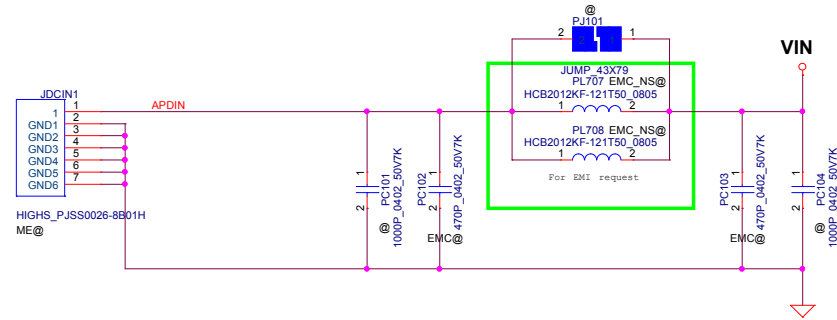




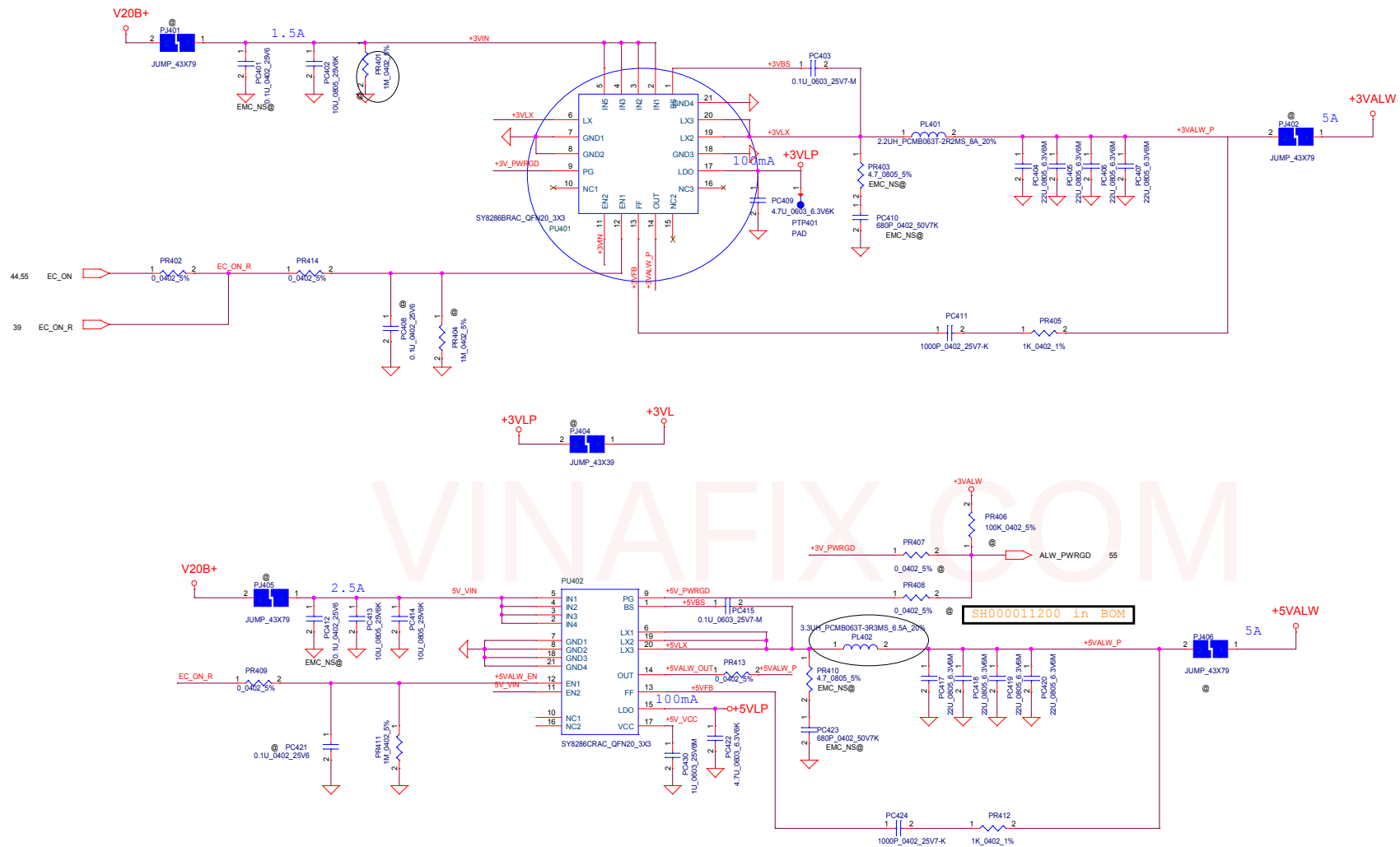
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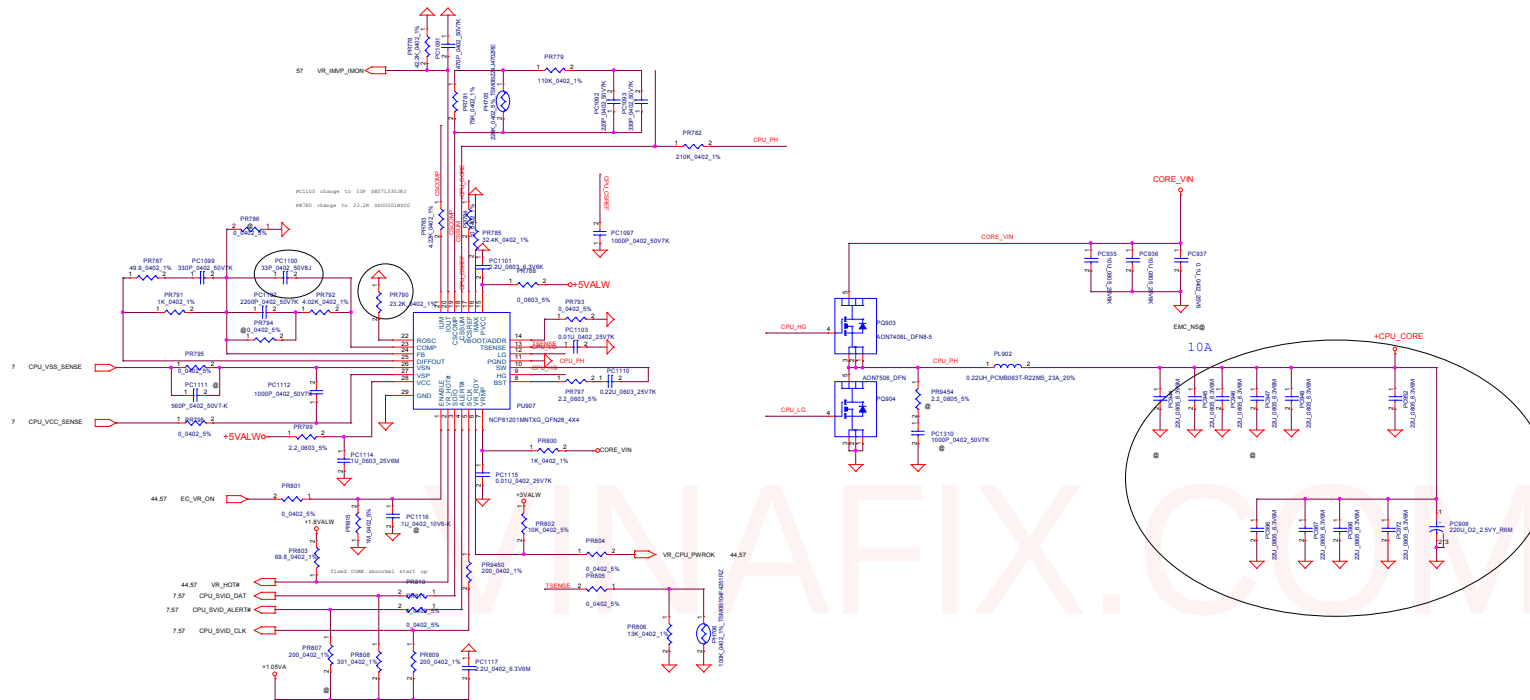
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