R63 INTEL SYSTEM DIAGRAM

01

+3V/+5V S5 PG.36
+1.05V PG.37
CPU Core PG.40~41
DDR3L PG.38
Charge PG.35
Dis-Charge PG.39
+VGACORE PG.42
+1.5 VGA PG.43
+1.0V/+1.8/ +3 VGA PG.44

SODIMM1 Max. 4GB PG.12 — 1600MT/s DDR3 L Channel A
SODIMM2 Max. 4GB PG.13 — 1600MT/s DDR3 L Channel B

INTEL Haswell
Processor : Daul / Quad Core
Power : 37 / 47 (Watt)
Package : rPGA947
Size : 37.5 x 37.5 (mm)
PG.2~5

PCI-E x8 — AMD Mars / SUN XT 29mm X 29mm TDP 35W / 25W PG.14~20
DDR3 900MHz — VRAM 128Mx16x8,128bit PG.21~22
eDP (5.4Gb/s)
DDI (5.4Gb/s)

FDI DMI

HDD PG.33 — SATA0
ODD PG.33 — SATA1

INTEL PCH
Lynx Point
Power : 3.5 Watt
Package : FCBGA695
Size : 20 x 20 (mm)
PG.6~11

eDP — RTD 2136 S/R DP to LVDS Converter PAGE 23 — LVDS Interface — LVDS PG.25
DP Port B — HDMI PG.26
CRT — CRT PG.25

PCI-E x 1 LANE2 LANE1
LAN RTL8166EH 10/100 PG.30
WLAN BT COMBO PG.34 — USB 2.0 PORT10

PCI-E x 1 LANE3
Accelerometer PG.34 — SMBUS
Card Reader RTS5237 PG.27

KBC EnE KB3940QF A1 PG.31 — LPC
KB PG.32 | TP PG.32 | ROM PG.31 | FAN PG.32

USB 3.0 — USB3.0 Ports X2 PG.29 | Webcam PG.25
USB 2.0 PORT1,2 PORT4 PORT0,1 — USB2.0 Ports PG.29

AUDIO CODEC ALC 3227 PG.28
Speaker PG.28
HP/MIC PG.29
Analog MIC PG.29

Stackup
TOP
GND
IN1
IN2
VCC
BOT

NB5

PROJECT : R63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

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Haswell Processor (DMI,PEG,FDI)

Haswell Processor (CLK,MISC,JTAG)

02

U24A

DMI_TXN0 DMI_TXN1 DMI_TXN2 DMI_TXN3 → D21 C21 B21 A21 DMI_RX#[0] DMI_RX#[1] DMI_RX#[2] DMI_RX#[3]

DMI_TXP0 DMI_TXP1 DMI_TXP2 DMI_TXP3 → D20 C20 B20 A20 DMI_RX[0] DMI_RX[1] DMI_RX[2] DMI_RX[3]

DMI_RXN0 DMI_RXN1 DMI_RXN2 DMI_RXN3 → D18 C17 B17 A17 DMI_TX#[0] DMI_TX#[1] DMI_TX#[2] DMI_TX#[3]

DMI_RXP0 DMI_RXP1 DMI_RXP2 DMI_RXP3 → D17 C18 B18 A18 DMI_TX[0] DMI_TX[1] DMI_TX[2] DMI_TX[3]

DMI

FDI_TXN0 FDI_TXN1 FDI_TXP0 FDI_TXP1 → P33 N32 R33 P32 FDI_TX#[0] FDI_TX#[1] FDI_TX[0] FDI_TX[1]

FDI_INT → J29 FDI_INT

FDI_CSYNC → R71 *0_4/S FDI_CSYNC_R → H29 FDI_CSYNC

FDI

DPB_LANE0_N DPB_LANE1_N DPB_LANE2_N DPB_LANE3_N → T28 T30 U29 U31 DDIB_TX#[0] DDIB_TX#[1] DDIB_TX#[2] DDIB_TX#[3]

DPB_LANE0_P DPB_LANE1_P DPB_LANE2_P DPB_LANE3_P → U28 U30 V29 V31 DDIB_TX[0] DDIB_TX[1] DDIB_TX[2] DDIB_TX[3]

IN_D2# IN_D1# IN_D0# IN_CLK# / IN_D2 IN_D1 IN_D0 IN_CLK

DDIC_TX#[0] DDIC_TX#[1] DDIC_TX#[2] DDIC_TX#[3] → T34 U35 U32 U33 U34

DDIC_TX[0] DDIC_TX[1] DDIC_TX[2] DDIC_TX[3] → V35 T32 V33

DDID_TX#[0] DDID_TX#[1] DDID_TX#[2] DDID_TX#[3] → P29 N28 P31 N30

DDID_TX[0] DDID_TX[1] DDID_TX[2] DDID_TX[3] → R29 P28 R31 P30

Intel(R) DDI

FDI_CSYNC & FDI_INT
Trace length < 10000 Mils
Impendance = 50 ohm

eDP_RCOMP → E24 eDP_RCOMP

6,24,25 EDP_DISP_UTIL → R59 *0_4 → INT_eDP_HPD_Q → P27 EDP_DISP_UTIL

eDP_HPD

24 EDP_AUXP EDP_AUXN → N27 M27 eDP_AUX eDP_AUX#

24 EDP_TXP0 EDP_TXP1 → R35 P34 eDP_TX[0] eDP_TX[1]

24 EDP_TXN0 EDP_TXN1 → P35 N34 eDP_TX#[0] eDP_TX#[1]

eDP

HSW_RPGA_EDS_PGA

PCI EXPRESS* - GRAPHICS

PEG_COMP → E23

PEG_RCOMPO

PEG_RX#[0..7] 14 → M29 K28 M31 L30 M33 L32 M35 L34 PEG_RX#0 PEG_RX#1 PEG_RX#2 PEG_RX#3 PEG_RX#4 PEG_RX#5 PEG_RX#6 PEG_RX#7

PEG_RX#[0] PEG_RX#[1] PEG_RX#[2] PEG_RX#[3] PEG_RX#[4] PEG_RX#[5] PEG_RX#[6] PEG_RX#[7] PEG_RX#[8] PEG_RX#[9] PEG_RX#[10] PEG_RX#[11] PEG_RX#[12] PEG_RX#[13] PEG_RX#[14] PEG_RX#[15] → E29 D28 E31 D30 E35 D34 E33 E32

PEG_RX[0..7] 14 → L29 L28 L31 K30 L33 K32 L35 K34 PEG_RX0 PEG_RX1 PEG_RX2 PEG_RX3 PEG_RX4 PEG_RX5 PEG_RX6 PEG_RX7

PEG_RX[0] PEG_RX[1] PEG_RX[2] PEG_RX[3] PEG_RX[4] PEG_RX[5] PEG_RX[6] PEG_RX[7] PEG_RX[8] PEG_RX[9] PEG_RX[10] PEG_RX[11] PEG_RX[12] PEG_RX[13] PEG_RX[14] PEG_RX[15] → F29 E28 F31 E30 F35 E34 F33 D32

PEG_TX#[0] PEG_TX#[1] PEG_TX#[2] PEG_TX#[3] PEG_TX#[4] PEG_TX#[5] PEG_TX#[6] PEG_TX#[7] PEG_TX#[8] PEG_TX#[9] PEG_TX#[10] PEG_TX#[11] PEG_TX#[12] PEG_TX#[13] PEG_TX#[14] PEG_TX#[15] → H35 H34 J33 H32 J31 G30 C33 B32 B31 A30 B29 A28 B27 A26 B25 A24

C_PEG_TX#0 C_PEG_TX#1 C_PEG_TX#2 C_PEG_TX#3 C_PEG_TX#4 C_PEG_TX#5 C_PEG_TX#6 C_PEG_TX#7

PEG_TX[0] PEG_TX[1] PEG_TX[2] PEG_TX[3] PEG_TX[4] PEG_TX[5] PEG_TX[6] PEG_TX[7] PEG_TX[8] PEG_TX[9] PEG_TX[10] PEG_TX[11] PEG_TX[12] PEG_TX[13] PEG_TX[14] PEG_TX[15] → J35 G34 H33 G32 H31 H30 B33 A32 C31 B30 C29 B28 C27 B26 C25 B24

C_PEG_TX0 C_PEG_TX1 C_PEG_TX2 C_PEG_TX3 C_PEG_TX4 C_PEG_TX5 C_PEG_TX6 C_PEG_TX7

HSW_RPGA_EDS_PGA

H_PECI (50ohm)
Route on microstrip only
Spacing > 18 mils
Trace Length: 15 inch

TP50 SKTOCC# → AP32
TP46 TP_CATERR# → AN32

HPECI Ra,Ca need placement close to EC.
9,31 EC_PECI → R537 43_4 → H_PECI
Ra
Ca
C770 *47P/50V_4

4/30 CRB 1.0 Add
+VCCST → AR27

PROCHOT# (50ohm)
Trace Length <11 inches
31,40 H_PROCHOT# → R263 56.2/F_4 → H_PROCHOT# R → AK31
C38 Cb
Cb need placment near VR
47P/50V_4

THERMTRIP# (50ohm)
Trace Length: 1.1~12 inches
9,31 PM_THRMTRIP#R → PM_THRMTRIP# R → AM30
Rb need placment near PCH
4/30 CRB 1.0 Add
+1.05VO R354 *100/F_4 Rb → AM35

PM_SYNC (50ohm)
Trace Length: 1~11.25 inches
6 PM_SYNC → R533 *0_4/S → PM_SYNC_R → AT28
C729 *0.1U/10V_4

H_PWRGOOD (50ohm)
Trace Length: 1~11.25 inches
9 H_PWRGOOD → R502 *0_4/S → H_PWRGOOD_R → AL34
R503 10K_4

PM_DRAM_PWRGD_R → AC10

CPU RESET#
9,31 CPU_PLTRST#R
8,14,27,30,31,34 PLTRST# → R531 *1.5K/F_4 → R532 *750/F_4 → AT26
CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches
7/26: DB phase modify

U24B

SKTOCC# CATERR# PECI FC_AK31 PROCHOT# THERMTRIP# PM_SYNC UNCOREPWRGOOD SM_DRAMPWROK RESET# → MISC THERMAL PWR MANAGEMENT

HSW_RPGA_EDS_PGA

CLOCKS

BCLK BCLK# → E26 D26 CLK_CPU_BCLKP CLK_CPU_BCLKN → CLK_CPU_BCLKP 8 CLK_CPU_BCLKN 8

SSC_DPLL_REF_CLK SSC_DPLL_REF_CLK# → E27 F27 CLK_DPLL_SSCLKP CLK_DPLL_SSCLKN → CLK_DPLL_SSCLKP 8 CLK_DPLL_SSCLKN 8

DPLL_REF_CLK DPLL_REF_CLK# → H28 G28 CLK_DPLL_NSCCLKP CLK_DPLL_NSCCLKN → CLK_DPLL_NSCCLKP 8 CLK_DPLL_NSCCLKN 8

Host CLK:
Trace length < 11000 MILS
Trace spacing = 15 ,20 MILS, Impendence 90 ohm

DDR3 MISC

SM_DRAMRST# → AN3 CPU_DRAMRST#

SM_RCOMP[0] SM_RCOMP[1] SM_RCOMP[2] → AP3 AR3 AP2 SM_RCOMP_0 SM_RCOMP_1 SM_RCOMP_2 → R250 100/F_4, R526 75/F_4, R525 100/F_4

SM_RCOMP[0] W:12mils/S:15mils/L: 500mils,
SM_RCOMP[1] W:12mils/S:15mils/L: 500mils,
SM_RCOMP[2] W:12mils/S:15mils/L: 500mils,

JTAG & BPM

CPU XDP

PRDY# PREQ# → AR29 AT29 XDP_PRDY# XDP_PREQ# → TP100 TP57
TCK TMS TRST# → AM34 AN33 AM33 XDP_TCLK XDP_TMS XDP_TRST# → TP42 TP41 TP94
TDI TDO → AM31 AL33 XDP_TDI_R XDP_TDO → TP36 TP39
DBR# → AP33 XDP_DBRST# → R524 *1K_4 +3V → XDP_DBRST# 6
BPM#[0] BPM#[1] BPM#[2] BPM#[3] BPM#[4] BPM#[5] BPM#[6] BPM#[7] → AR30 AN31 AN29 AP31 AP30 AN28 AP29 AP28 XDP_BPM0 XDP_BPM1 XDP_BPM2 XDP_BPM3 XDP_BPM4 XDP_BPM5 XDP_BPM6 XDP_BPM7 → TP101 TP53 TP59 TP99 TP95 TP56 TP97 TP58

SM_DRAMPWROK Processor Input.
To change the resistor values in the DRAMPWROK logic to reduce the leakage on VDDPWRGOOD

+3VS5
PM_DRAM_PWRGD_C (50ohm)
Trace Length: < 1 inches
10/22: SI modify
R75 100K_4 R66 100K_4 C44 0.1U/10V_4
+1.35V_CPU R80 1.8K/F_4 DG 498556 -> 1.8K
U2 74AHC1G09GW
38 51216PG R65 *0_4/S 4PM_DRAM_PWRGD_C R78 0_4 PM_DRAM_PWRGD_R
10/12: SI modify
C929 0.047U/10V_4
D15 *MEK500V-40 10/15: SI Del
R79 3.3K_4 C930 *0.047U/10V_4 DG 498556 -> 3.3K
PM_DRAM_PWRGD (50ohm)
Trace Length: 2~7 inches
PM_DRAM_PWRGD_R (50ohm)
Trace Length: 0.5~1 inches

DDR3 DRAM RESET

DDR3_DRAMRST#_R (50ohm)
Trace Length < 6 inches
+1.35VSUS R471 *1K_4 R785 *0_4/S
12,13 DDR3_DRAMRST# R472 *0_4/S → CPU_DRAMRST#
10/18: SI modify
CPU_DRAMRST#_R Q29 *ME2N7002E
8 DRAMRST_CNTRL_PCH R468 *0_4 R464 *4.99K/F_4
31 DRAMRST_CNTRL_EC R467 *0_4 C628 *0.047U/10V_4
8,12,13 DRAMRST_CNTRL_DDR
FOR DS3
0529 remove R825 pull hi due to EC is output pin

+VCCIO_OUT 4,40
+VCCIOA_OUT 4
+1.05V 4,9,10,11,31,34,37
+1.35V_CPU 3,4,12,13,38
+1.35VSUS 3,4,12,13,38
+3VS5 6,7,9,10,34,36,38,39,42,44
+3V 6,7,8,9,10,12,13,14,23,24,25,26,27,28,29,30,31,32,33,34,39,40,42,44

4/30 CRB V1.0 -> 10K
+VCCIO_OUT → R218 10K_4
INT_eDP_HPD_Q → Q12 ME2N7002E → EDP_HPD 24,25
R219 100K_4

PEG x8 disable (UMA only remove)

14 PEG_TX[0..7]

C_PEG_TX0 C688 0.22U/10V_4 PEG_TX0
C_PEG_TX1 C705 0.22U/10V_4 PEG_TX1
C_PEG_TX2 C698 0.22U/10V_4 PEG_TX2
C_PEG_TX3 C708 0.22U/10V_4 PEG_TX3
C_PEG_TX4 C699 0.22U/10V_4 PEG_TX4
C_PEG_TX5 C690 0.22U/10V_4 PEG_TX5
C_PEG_TX6 C715 0.22U/10V_4 PEG_TX6
C_PEG_TX7 C730 0.22U/10V_4 PEG_TX7

0.22uF AC coupling Caps for PCIE GEN1/2/3

14 PEG_TX#[0..7]

C_PEG_TX#0 C697 0.22U/10V_4 PEG_TX#0
C_PEG_TX#1 C707 0.22U/10V_4 PEG_TX#1
C_PEG_TX#2 C703 0.22U/10V_4 PEG_TX#2
C_PEG_TX#3 C714 0.22U/10V_4 PEG_TX#3
C_PEG_TX#4 C704 0.22U/10V_4 PEG_TX#4
C_PEG_TX#5 C700 0.22U/10V_4 PEG_TX#5
C_PEG_TX#6 C716 0.22U/10V_4 PEG_TX#6
C_PEG_TX#7 C733 0.22U/10V_4 PEG_TX#7

0.22uF AC coupling Caps for PCIE GEN1/2/3

DP & PEG Compensation

+VCCIOA_OUT → R138 24.9/F_4 eDP_RCOMP

eDP_RCOMP
Trace length < 100 Mils
Trace Width 20 Mils Trace Spacing 25 Mils

+VCCIOA_OUT → R132 24.9/F_4 PEG_COMP

PEG_RCOMP
Trace length < 400 MILS
Trace width = 12 MILS
Trace spacing = 15 MILS

Processor pull-up (CPU)

H_PROCHOT# R257 62_4 +VCCIO_OUT
CLK_DPLL_SSCLKP R128 *10K_4
CLK_DPLL_SSCLKN R129 *10K_4

XDP_TDO R234 51_4
XDP_TMS R239 *51_4 +1.05V
XDP_TDI_R R226 *51_4
XDP_PREQ# R269 *51_4
XDP_TCLK R246 51_4
XDP_TRST# R519 51_4
check

NB5

PROJECT : R63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 1/4 (PCIE&DMI&FDI)	1A

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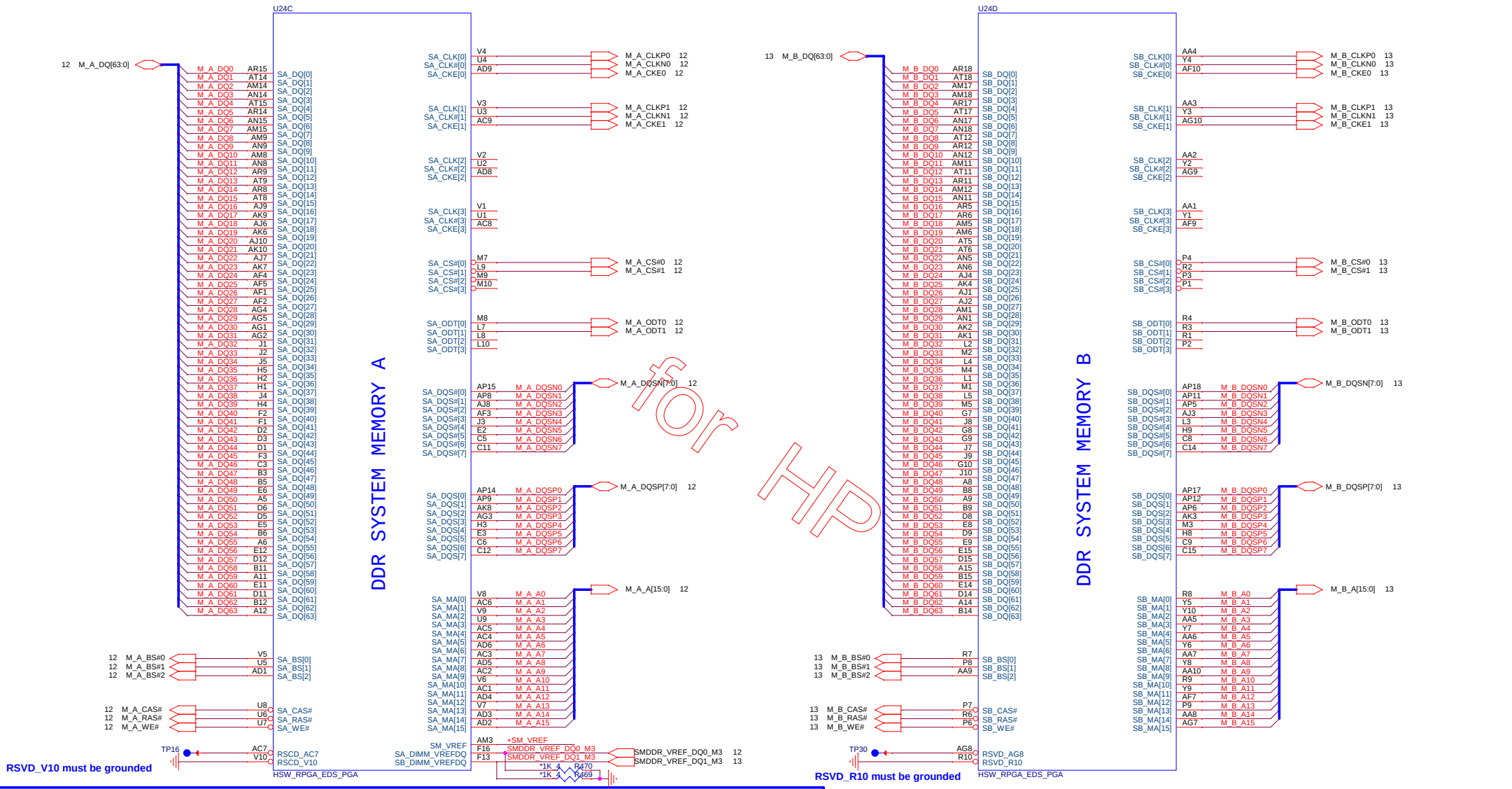
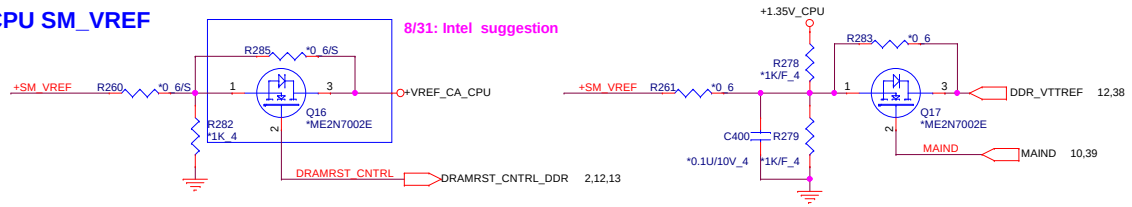
Haswell Processor (DDR3)

03



CPU SM_VREF

8/31: Intel suggestion



+1.35V_CPU 2,4,12,13,38
+VREF_CA_CPU 12

NB5	PROJECT : R63 Quanta Computer Inc.	
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Haswell Processor (POWER)

04

POWER

+VCCIN 95A

U24F

+VCC_CORE

+1.35V_CPU 4.2A

+1.35V_CPU

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

HSW_RPGA_EDS_PGA

VDDQ Output Decoupling Recommendations

330uFx2	7343	BOT socket side
22uFx11	0805	5 onTOP, 6 on BOT inside socket cavity
10uFx10	0805	5 onTOP, 5 on BOT inside socket cavity

VCC Output Decoupling Recommendations

470uFx4	7343	TOP socket side
22uFx8	0805	4 on TOP, 4 on BOT near socket edge
22uFx11	0805	TOP, inside socket cavity
10uFx11	0805	BOT, inside socket cavity

+VCCIOA_OUT 2
+VCCIO_OUT 2,40
+VCCIO_PCH 10
+1.5V 6,7,8,10,28,34,38,44
+1.35V_CPU 2,3,12,13,38
+1.05V 2,9,10,11,31,34,37
+VCC_CORE 40,41
+VCCST 2
+1.35VSUS 2,3,12,13,38

IO Thrm Protect

+3VPCU

For 65 degree, 1.8v limit, (SW)

R774 16.5K/F_4

THRM_MOINTOR 31

C62 0.1U/10V_4

R775 3.3K/F_4

For 75 degree, 1.2v limit, (HW)

THRM_MOINTOR1 31

R776 100K_4 NTC

C54 0.1U/10V_4

4/30: CRB 1.0 add

+1.05V R256 *0_8 +VCCST

C392 *22U/6.3VS_8

C381 *22U/6.3VS_8

Power Test Propose

+1.05V R60 150/F_4 PWR_DEBUG_R R62 *10K_4

+1.05V R510 *0_8 +VCCIO_OUT C753 10U/6.3V_6

+1.05V R462 0_6 +VCCIO_PCH

CRB 1.0 stuff C631 *4.7U/6.3V_6

4/30: DG 498550

Haswell PWR_DEBUG requires a 150-Ohm pull-up resistor to PCH 1.05-V VCC Core when routed to XDP

Layout note: It is recommended to shield VIDSOUT signal by routing it in between the VIDSCLK and VIDALERT# signals.

SVID CLK

H_CPU_SVIDCLK VR_SVID_CLK 40

7/26: DB sch modify, Del R23

SVID DATA

+VCCIO_OUT R253 130/F_4 H_CPU_SVIDDAT VR_SVID_DATA 40

Place PU resistor close to CPU

Place PU resistor close to VR

DG V0.7 -> 110 Ohm
SCH V0.7 -> 130 Ohm

Place PU resistor close to CPU
The VIDALERT# signal must have a damping resistor to prevent overshoot

SVID ALERT

C337 0.1U/10V_4 +VCCIO_OUT R247 75/F_4 H_CPU_SVIDALRT# R248 43_4 VR_SVID_ALERT# 40

DG V0.7 -> 44 Ohm
SCH V0.7 -> 43 Ohm

Sense resistor should be placed within 2 inches (50.8 mm) of the processor socket

Trace Impendence 50 ohm

CPU VDDQ

+1.35V_CPU +1.35VSUS C235 0.1U/10V_4 C225 *0.1U/10V_4

Placement close to CPU.

Note: please keep plane is enough for VDDQ 4.2A

PROJECT : R63
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	SNB 3/4 (POWER)	1A

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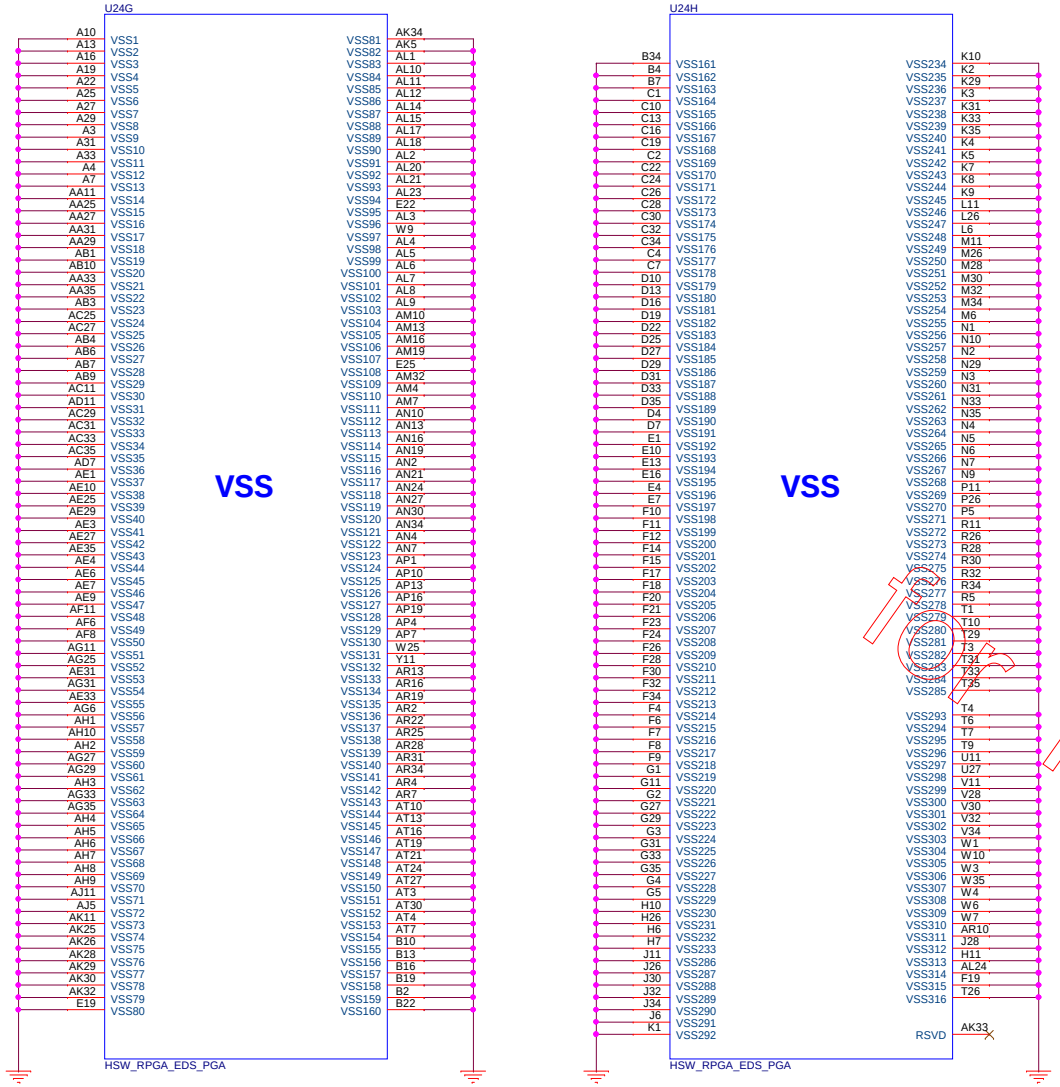
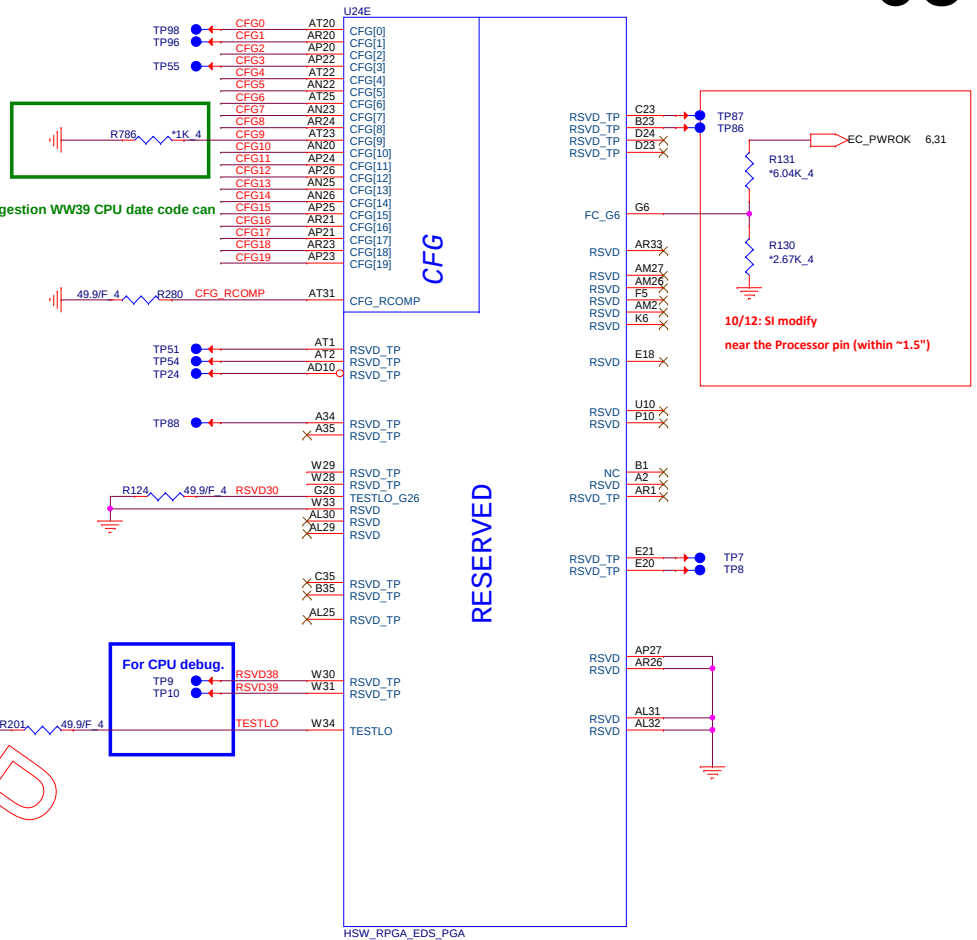
Haswell Processor (GND)



Haswell Processor (RESERVED, CFG)



05

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

CFG[3] (PHYSICAL_DEBUG_ENABLED (DFX PRIVACY))

0 Enable; SET DFX ENABLED BIT IN DEBUG

1 , Disable;

CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PROJECT : R63
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	SNB 4/4 (GND)	1A

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Lynx Point (DMI,FDI,PM)

Lynx Point (DDI)

06

U33C

U33D

DMI

FDI

System Power Management

LVDS

CRT

Digital Display Interface

INT. HDMI

LPT_PCH_M_EDS/BGA

PD Res place close to PCH

PCH to Res routeing 37.5 ohm Impedance.
Res to connector filter routeing 50ohm Impedance.

5/16 for DS3

for DS3

DG V0.7 -> 33 ohm
SCH V0.7 -> 0 ohm

DAC_IREF (50ohm)
Trace length < 500 MILS
Trace spacing = 30 MILS

12/17 PV modify

Reserve from EMI request

Reserve for power on sequence

+3V_DEEP_SUS 7,8,9,10,39
+3V_RTC 7,10,11
+1.05V 2,4,9,10,11,31,34,37
+3VPCU 4,7,9,11,25,31,32,34,35,36
+3VS5 2,7,9,10,34,36,38,39,42,44
+3V 2,7,8,9,10,12,13,14,23,24,25,26,27,28,29,30,31,32,33,34,39,40,42,44
+5V 7,23,26,28,29,32,33,34,39

PCH Pull-high/low(CLG)

for DS3

10/14: SI phase modify

10/12: SI phase modify

INT HDMI Detect Function

System PWR_OK(CLG)

7/26 DB Modify

10/17: SI Modify change to 10 Kohm

7/26 DB Modify

On Die DSW VR Enable
High = Enable (Default)
Low = Disable

PROJECT : R63
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	PCH 1/6 (DMI/FDI/VIDEO)	1A

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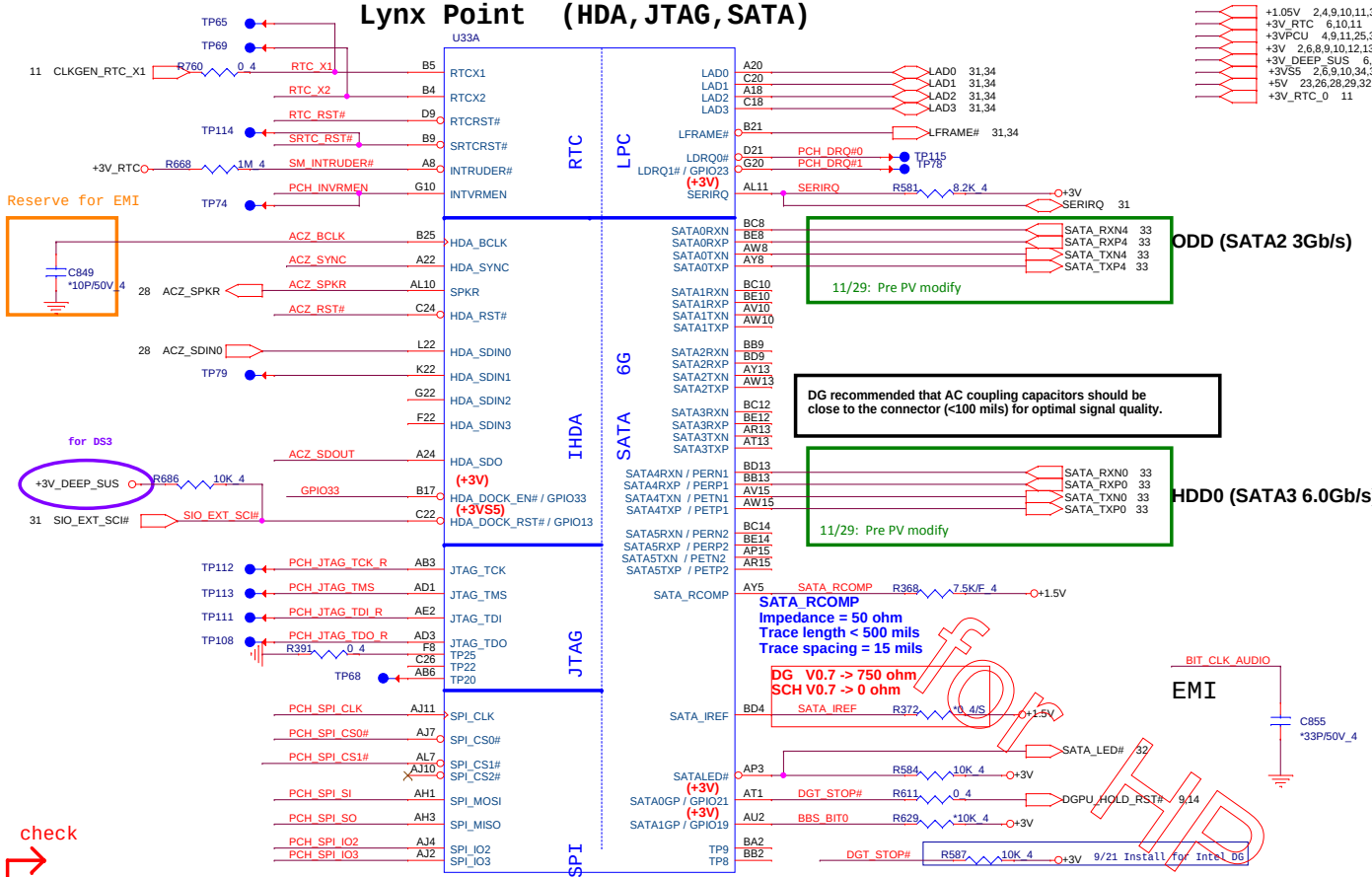
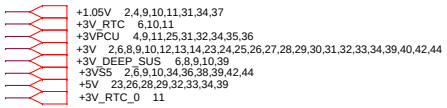
Lynx Point (HDA,JTAG,SATA)

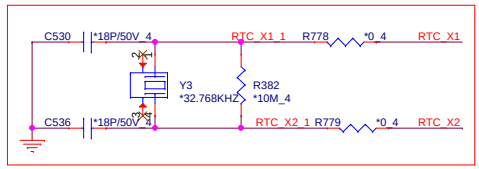




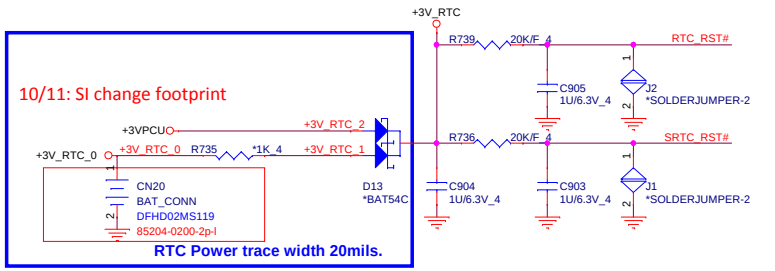
10/18: SI Modify

RTC Clock 32.768KHz

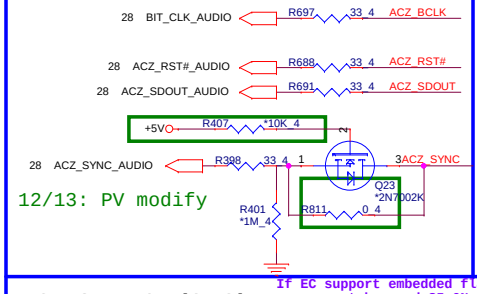
07



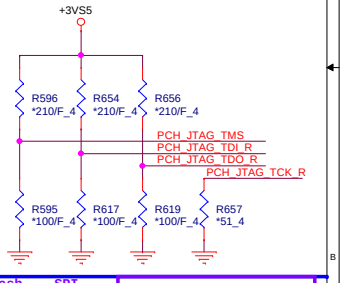
RTC Circuitry(RTC)



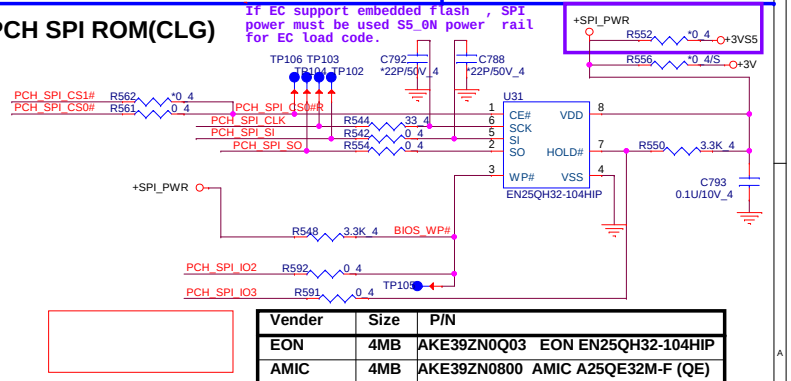
HDA Bus(CLG)



PCH JTAG Debug(CLG)



PCH SPI ROM(CLG)



Vender	Size	P/N
EON	4MB	AKE39ZN0Q03 EON EN25QH32-104HIP
AMIC	4MB	AKE39ZN0800 AMIC A25QE32M-F (QE)
Socket		DFHS08FS023

10/18: Del R350 , R344

check

PCH Strap Table

LPT_PCH_M_EDS/BGA

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	ACZ_SPKR R569 *1K_4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (Int PU)	R563 *1K_4 PCI_GNT3# 8
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	0 = Disable 1 = Enable	PCH_INVRMEN R389 330K_4 +3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R680 *0_4 +3V 10/18: SI Modify [Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location: 1 1 SPI; 1 0 LPC	
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		BBS_BIT0 R613 *1K_4 R390 *1K_4 BBS_BIT1 8
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+VCC_HDA_IO R684 *1K_4 ACZ_SYNC 12/13: PV modify
HDA_SDO	Flash Descriptor Security	PWROK	0 = Security Effect (Int PD) 1 = Can be Overridden	31 GPIO33_E ACZ_SDOUT R693 *1K_4 +VCC_HDA_IO
GPIO8	RSVD	RSMRST#	Internel PU	R621 *1K_4 BT_OFF# 9,34
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Int PU)	R571 *1K_4 PLL_ODVR_EN 9
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	PCH_SPI_SI R374 *1K_4 +3V
GPIO62 / SUSCLK	PLL On-Die Voltage Regulator Enable	RSMRST#	0 = Disable 1 = Enable (Int PU)	R564 *1K_4 PCH_SUSCLK 6,31

NB5

PROJECT : R63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 2/6 (SATA/HDA/SPI)	1A
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Lynx Point (PCI,USB,NVRAM)

Lynx Point (PCI-E,SMBUS,CLK)

08

PCI/USBOC# Pull-up(CLG)

USB3.0

USB2.0

USB2.0/USB3.0 COMBO 1st

USB2.0/USB3.0 COMBO 2nd

Webcam

Touch screen

12/11: PV modify

Right_USB

WLAN

check

MPC Switch Control	
MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)

PLTRST#(CLG)

7/26 DB modify

PEG Clock detect (SG only)

7/26 DB modify

SMBus/Pull-up(CLG)

12/18 PV modify

CLK_REQ/Strap Pin(CLG)

7/26 DB modify

SG : Rb ; UMA : Ra

CLOCK TERMINATION for FCIM

PCIE Clock

WLAN

LAN

GPU

Remove for UMA only.

SMBus/Pull-up(CLG)

RF

10/12: SI modify

change 25M to small size

10/18: SI modify

PROJECT : R63
Quanta Computer Inc.

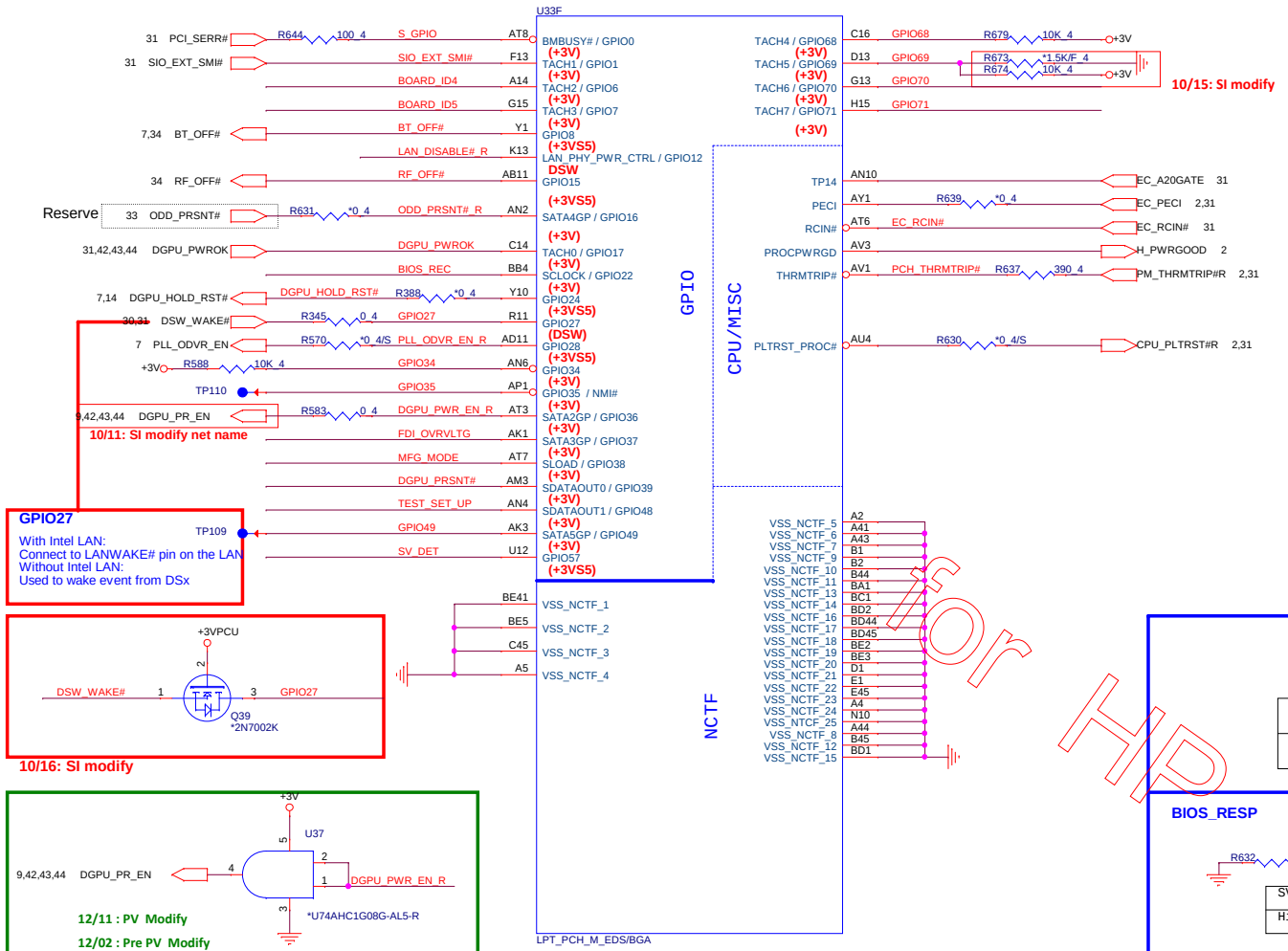
NB5

PCH 3/6 (PCIE/USB/CLK)

Size: Custom | Rev: 1A

Date: Monday, December 24, 2012 | Sheet 8 of 44

Lynx Point (GPIO,VSS_NCTF,RSVD)



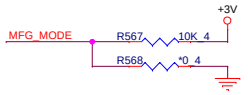
Clock Gen Power OK (CLG)

+3V_DEEP_SUS 6,7,8,10,39
+3VS5 2,6,7,10,34,36,38,39,42,44
+3V 2,6,7,8,10,12,13,14,23,24,25,26,27,28,29,30,31,32,33,34,39,40,42,44
+5VS5 23,29,30,34,36,37,38,39,40,41,42,43,44

09

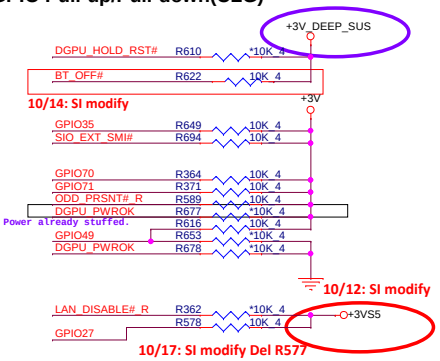
PCH MISC PU /PD

MFG-TEST



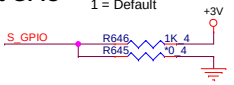
GPIO Pull-up/Pull-down(CLG)

for DS3

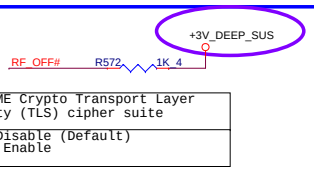


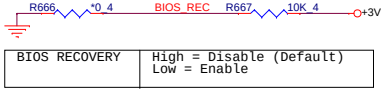
Swap GPIO

0 = SGPIO
1 = Default

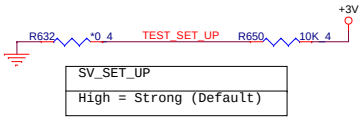


for DS3





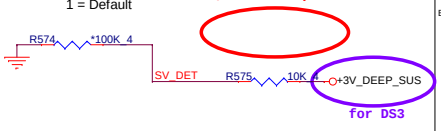
BIOS_RESP



SV Detect

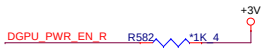
0 = SV Detect
1 = Default

10/17: SI modify



GPIO36

Internal PD



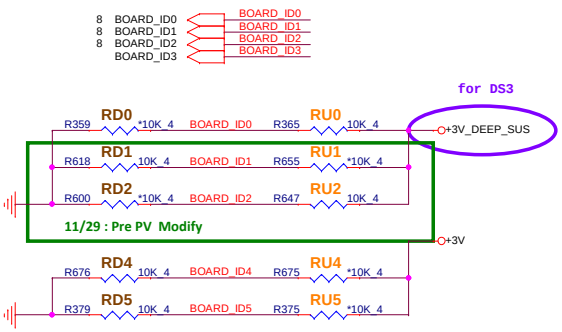
SATA3GP/GPIO37

TLS Confidentiality

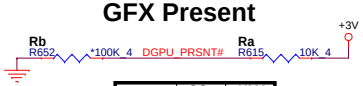
0 = TLS no confidentiality (Int PD)
1 = TLS with confidentiality

BOARD ID SETTING

Model	BOARD_ID5	BOARD_ID4		BOARD_ID2	BOARD_ID1	BOARD_ID0
DB R63 UMA				0	0	0
DB R63 DIS				0	0	1
SI R63 UMA				0	0	0
SI R63 DIS				0	0	1
PV R63 UMA				1	0	0
PV R63 DIS				1	0	1



GFX Present



	SG	UMA
Stuff	Ra	Rb
NC	Rb	Ra

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Quanta Computer Inc.

NB5

Size	Document Number	Rev
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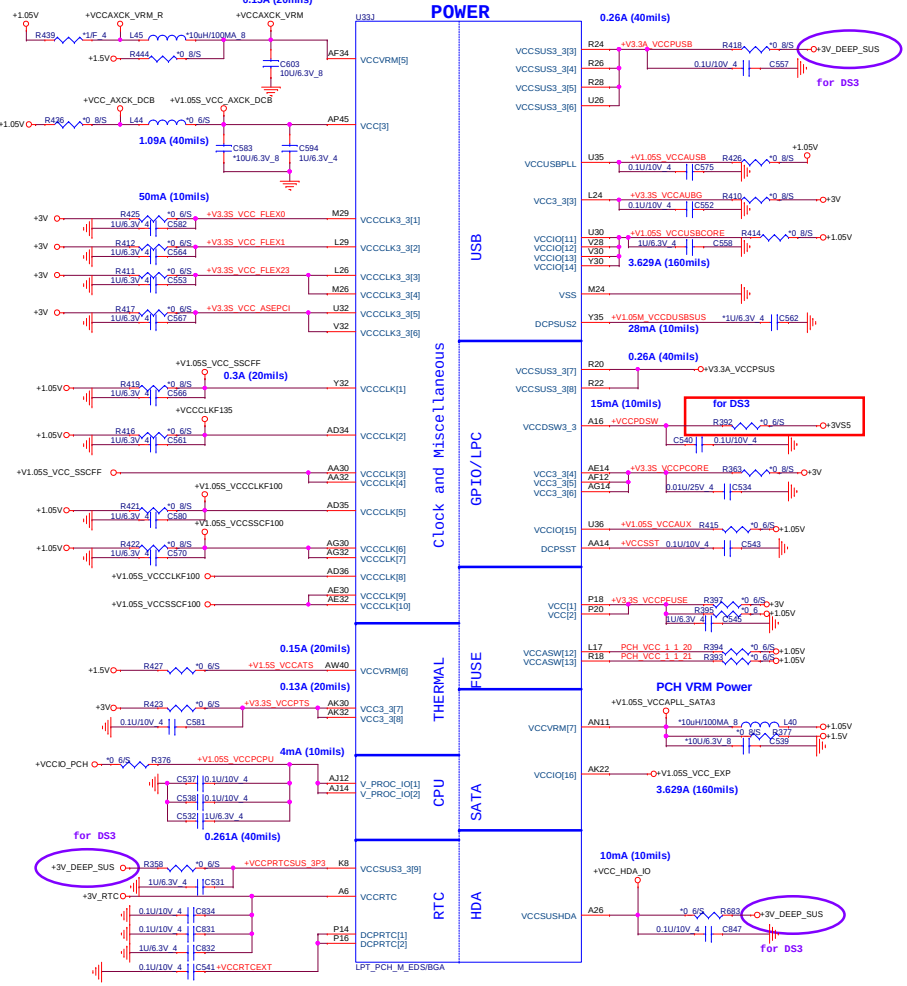
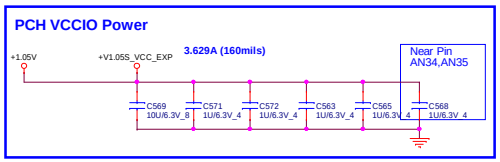
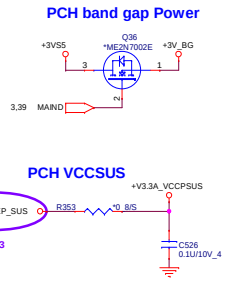
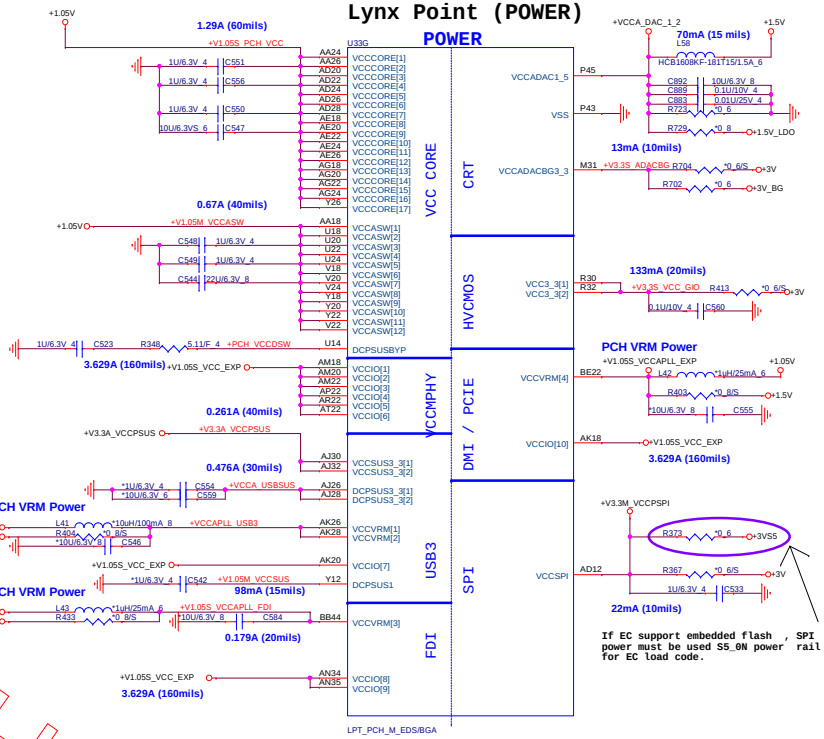
Lynx Point (POWER)

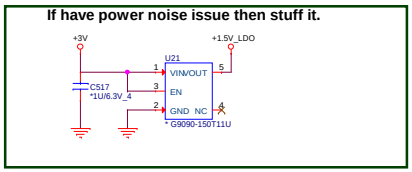


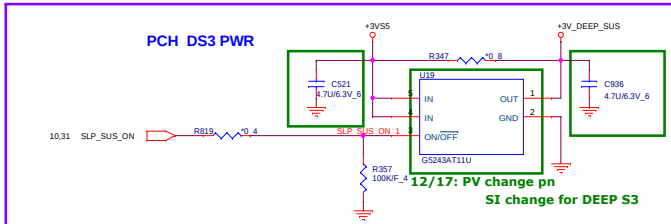


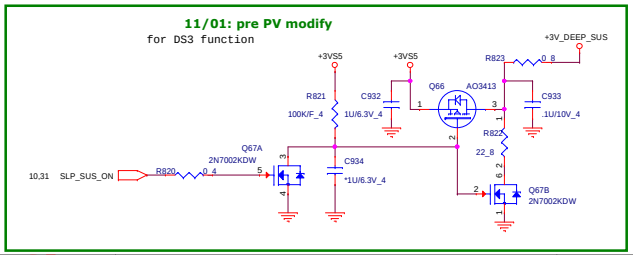


Lynx Point (POWER)









NB5	PROJECT : R63 Quanta Computer Inc.
Size: Custom	Document Number: PCH 5/6 (POWER) Rev: 1A
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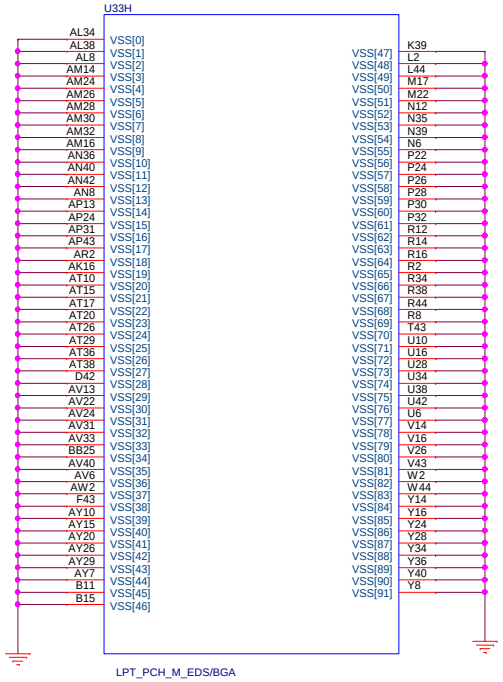
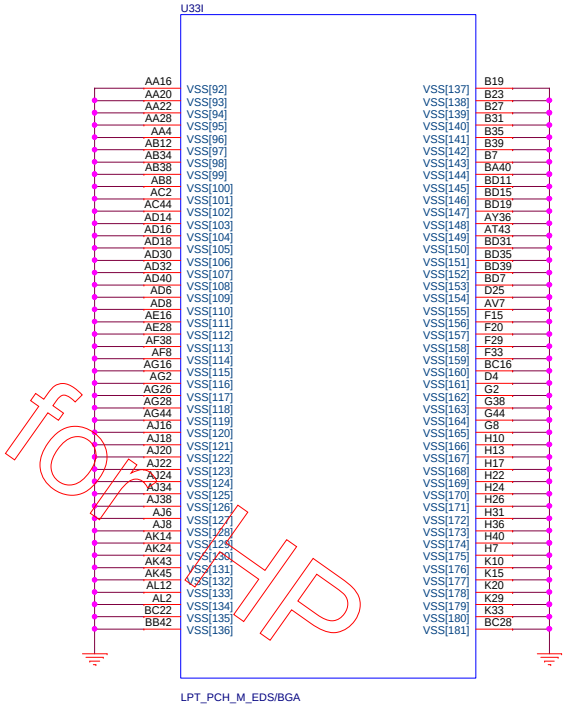
Lynx Point (GND)

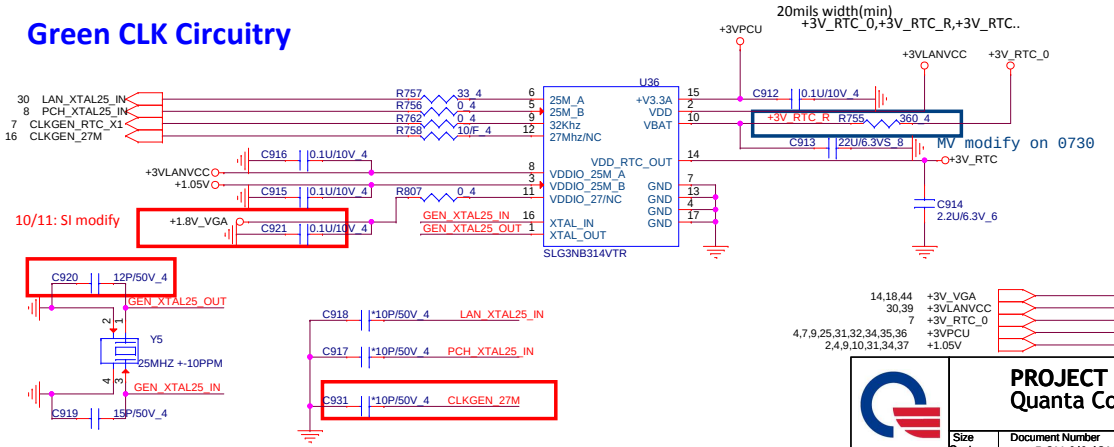


Lynx Point (GND)

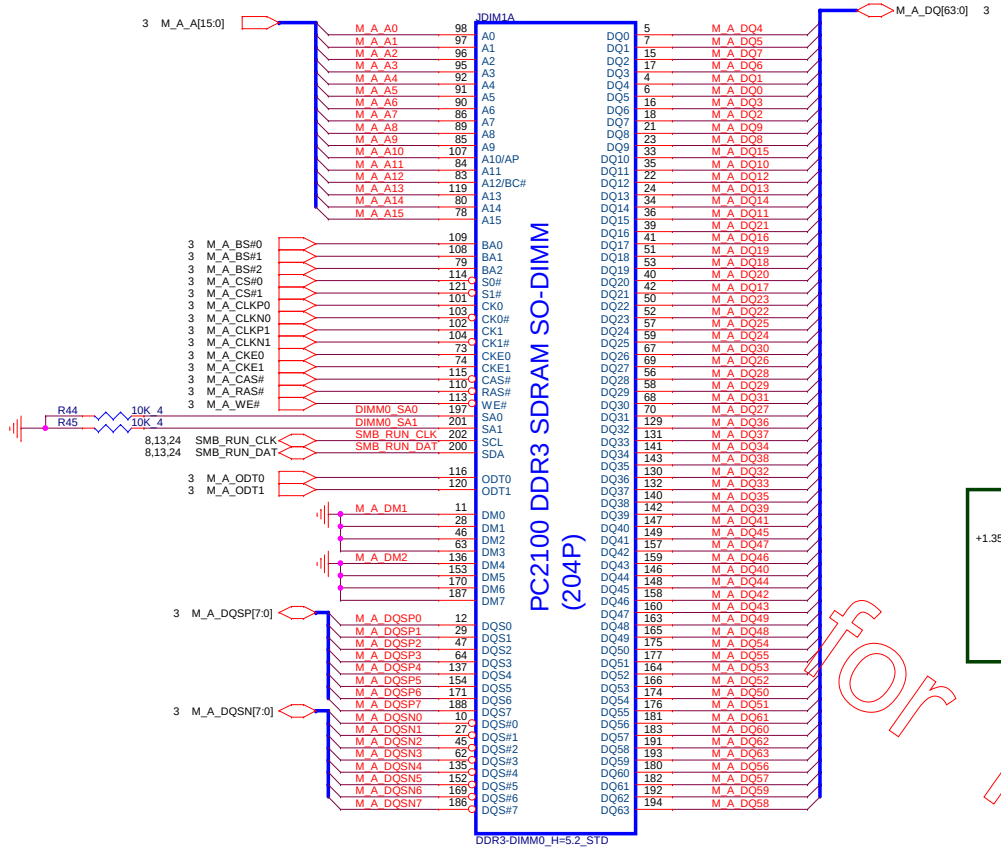


	U36 P/N
UMA	AL3NB244000
DIS	AL000314000

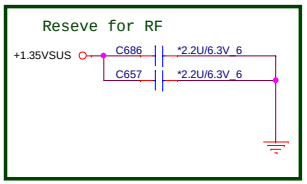
Green CLK Circuitry



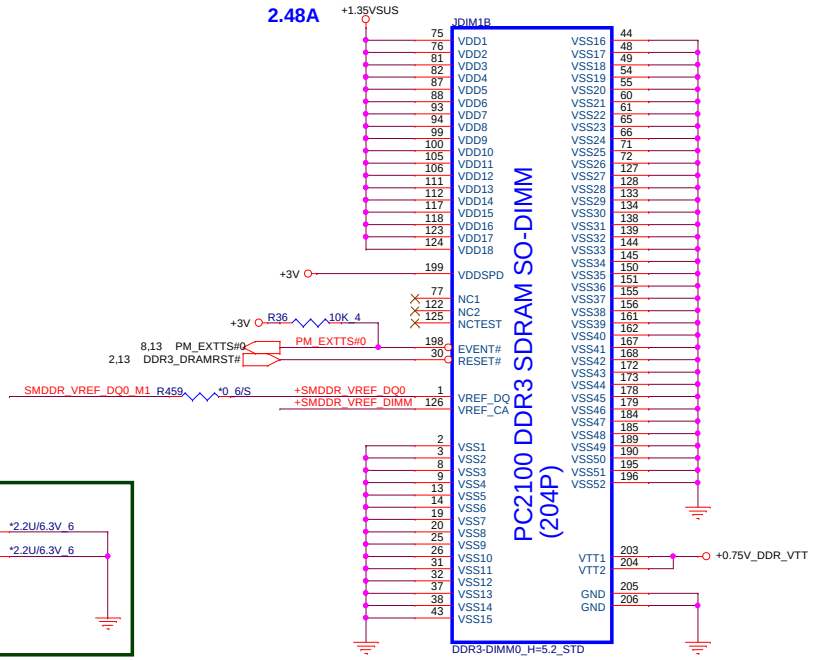
PROJECT : R63	
Quanta Computer Inc.	
NB5	
Size: Custom	Document Number: PCH 6/6 (GND)
Rev: 1A	
Date: Monday, December 24, 2012	Sheet 11 of 44



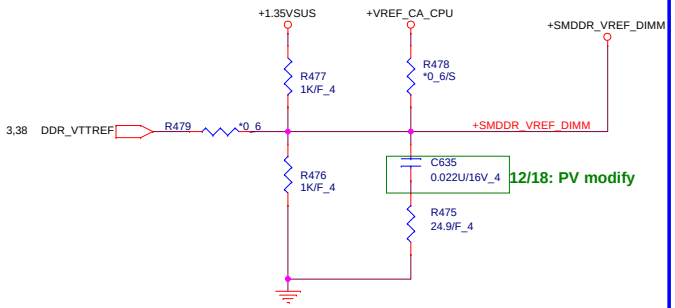
Reseve for RF



2.48A

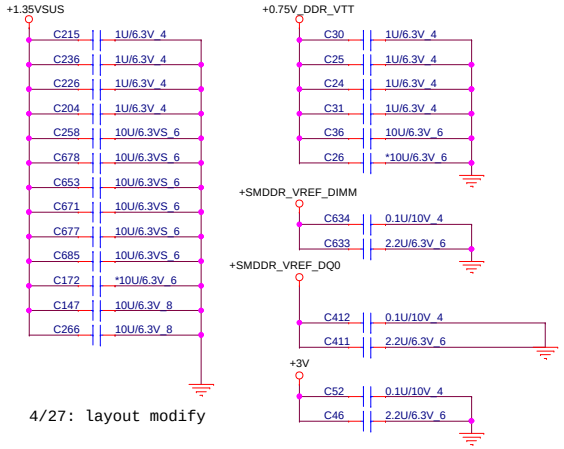


+SMDDR_VREF_DIMM 13
+VREF_CA_CPU 3
+0.75V_DDR_VTT 13,38,39
+1.35VSUS 2,3,4,13,38
+3V 2,6,7,8,9,10,13,14,23,24,25,26,27,28,29,30,31,32,33,34,39,40,42,44



12/18: PV modify

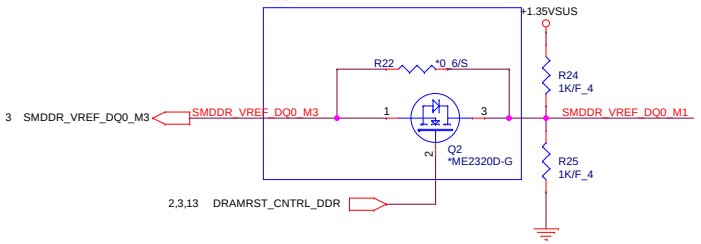
Place these Caps near So-Dimm0.



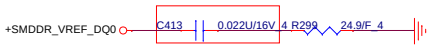
4/27: layout modify

VREF DQ0 M1 Solution

8/31: Intel suggestion



10/17: SI modify



NB5

PROJECT : R63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM0-RVS (5.2H)	1A

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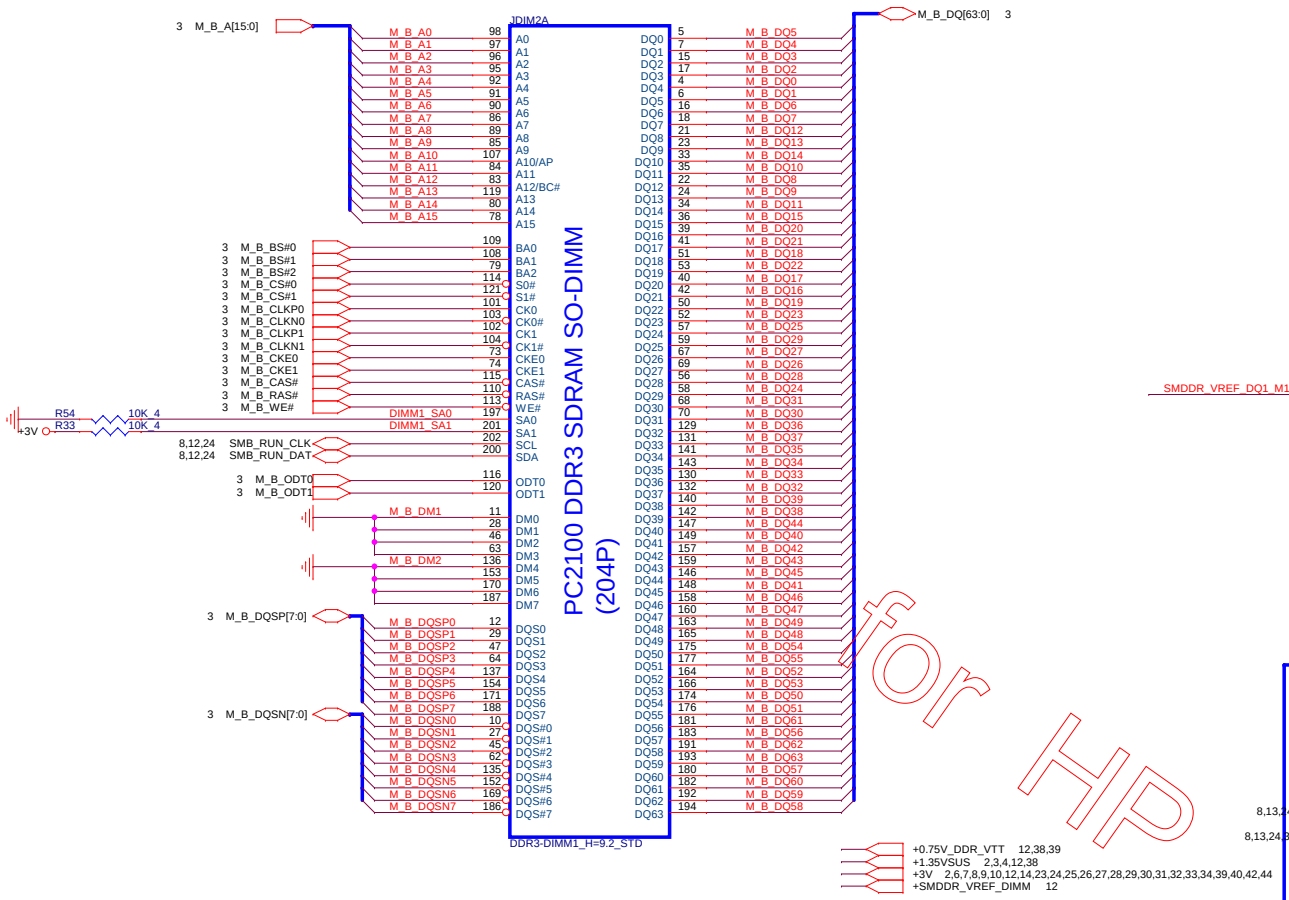
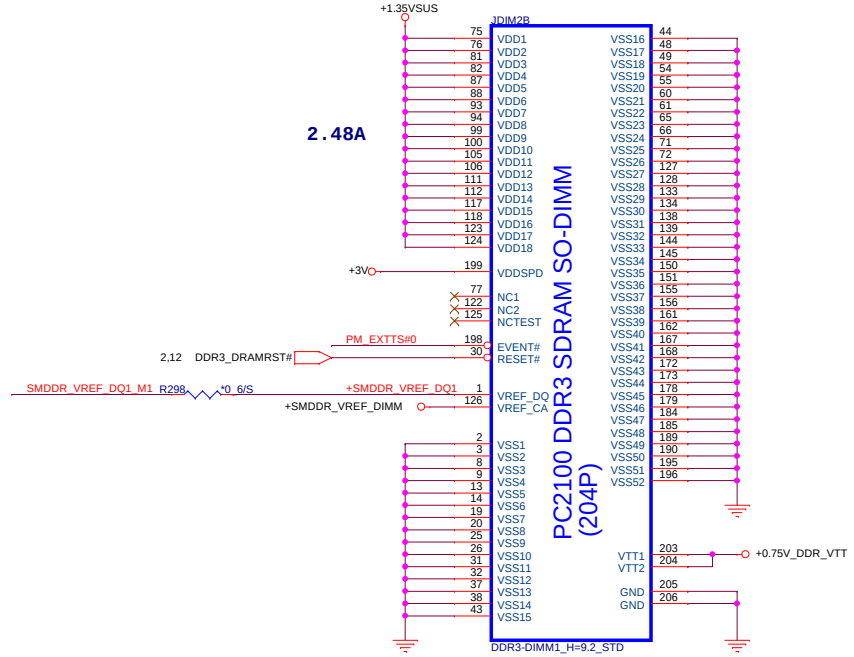
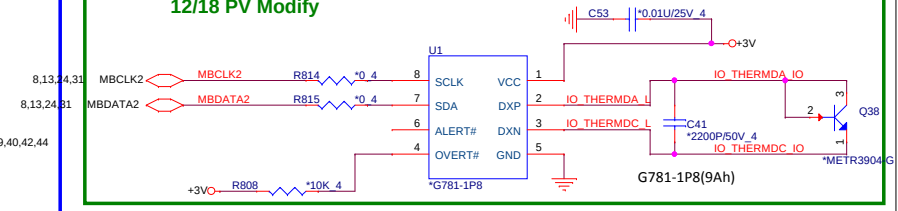


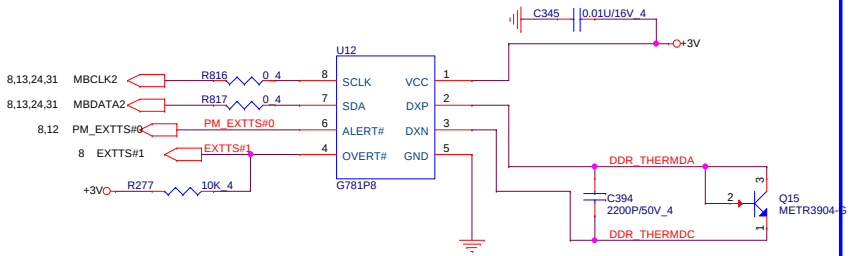


Local Thermal Sensor

12/18 PV Modify

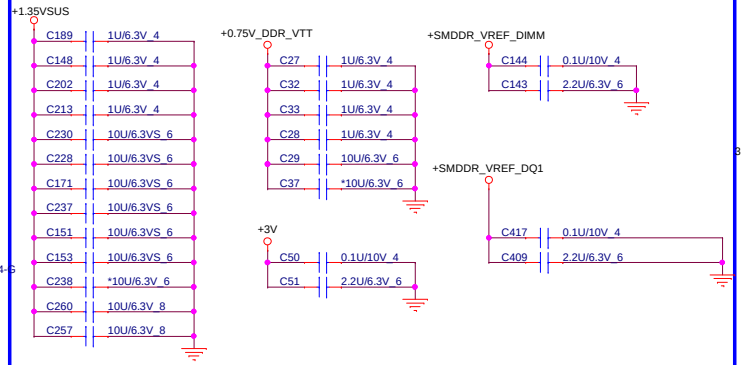


DDR Thermal Sensor

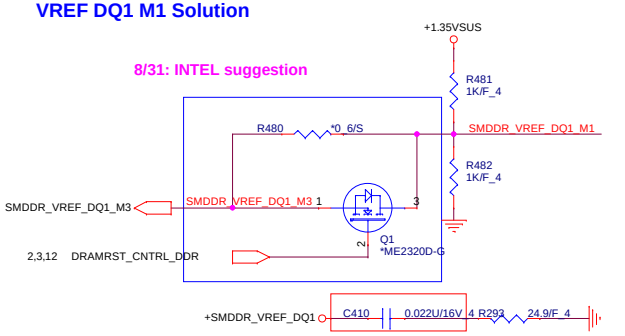


Address: G781P8(98h)

Place these Caps near So-Dimm1.



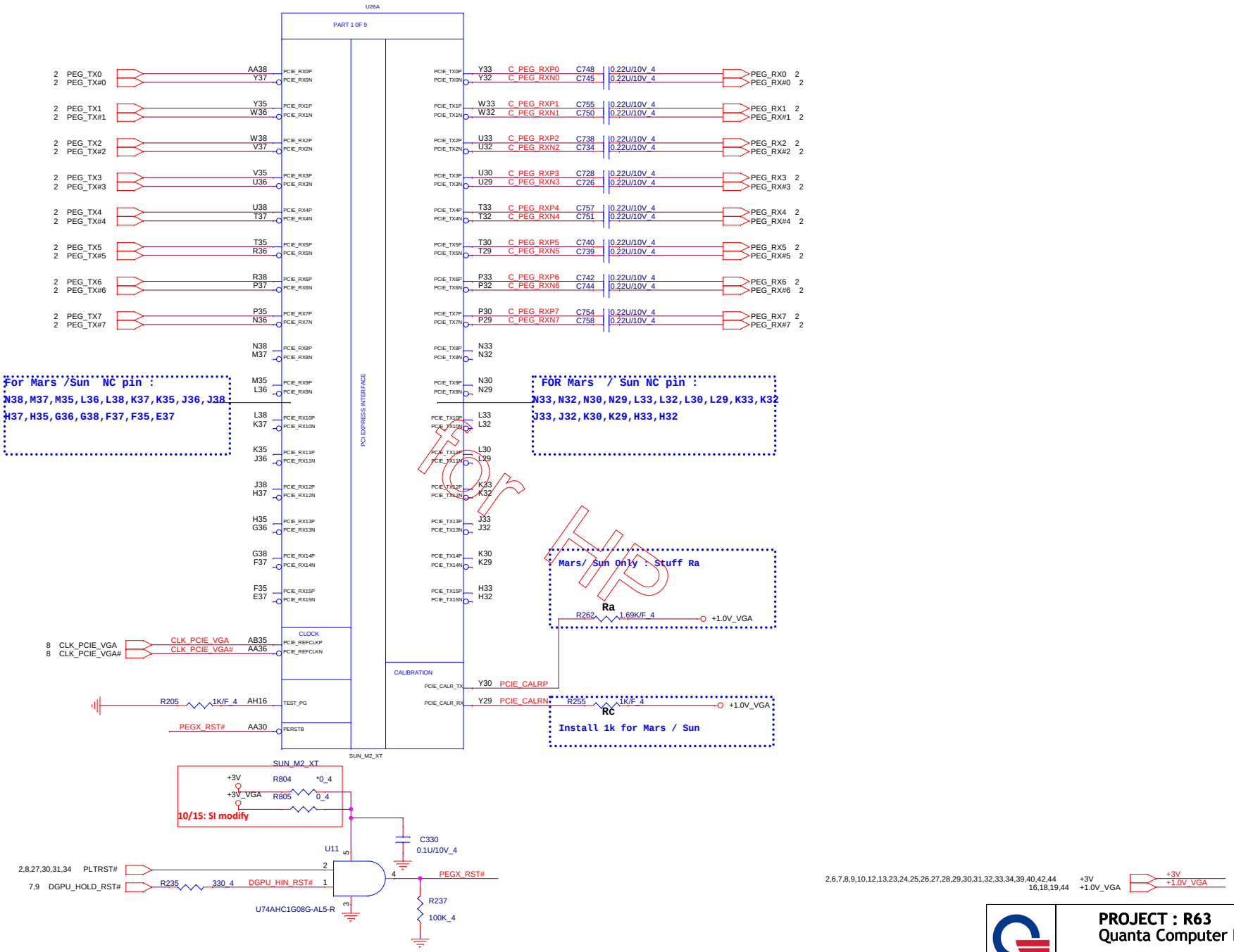
VREF DQ1 M1 Solution



PROJECT : R63
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	DDR3 DIMM1-RVS (9.2H)	1A
Date: Friday, December 21, 2012	Sheet 13 of 44	



NB5	PROJECT : R63 Quanta Computer Inc.	
Size: Custom	Document Number: THAMES_PCIE_Interface	Rev: 1A
Date: Friday, December 21, 2012	Sheet 14 of 44	

For Mars / Sun : AR1/AW8/AR3/AR8/AU8: NC pin

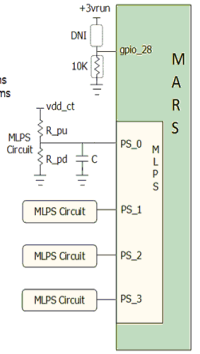
For Sun only : AD28 /AC28 /AJ21 /AR21: NC pin

For Mars / Sun : DP A to D Port: all NC pin

For Sun only :
AP10 /AV11 /AT11 /AR12 /AW12 / AU12 /AP12 : NC pin

MLPS Implementation

- Connect GPIO_28 to 10K pulldown to enable MLPS
- If any of PS_0/1/2/3 is not used, leave "no connect"
- R_pu, R_pd and C must be properly populated per tables below
- Place MLPS circuit components as close to the ASIC as possible
- Total DC resistance of trace between PS pin and C should be less than 2 ohms
- Total DC resistance of trace between C and ground should be less than 2 ohms
- Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance



Capacitor Lookup Table

C (nF)	Bits(5,4)
680	00
82	01
10	10
NC	11

Resistor Divider Lookup Table

R_pu (Ohm)	R_pd (Ohm)	Bits(3,2,1)
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Pin/Bit	Name	Description	Default	Legacy
PS_0[3:1]	romidcfg[2:0]	Memory aperture size or ROM type select: If bios_rom_en = 0, romidcfg[2:0] define memory aperture size If bios_rom_en = 1, romidcfg[2:0] define ROM type	xxx	gpio_13 gpio_12 gpio_11
PS_0[4]	n/a	Reserved	1	genlk_vsync
PS_1[1]	bif_gen3_en_a	PCIe Gen3 capability: 1=Gen3 supported, 0=Gen3 not supported	x	gpio_2
PS_1[2]	bif_clk_pm_en	PCIe Clk PM capability: 1 = CLKREQB supported	x	gpio_8
PS_1[3]	n/a	Reserved		genlk_clk
PS_1[4]	tx_pwrs_enb	PCIe Tx power savings: 0=50% swing, 1=full swing	x	gpio_0
PS_1[5]	tx_deemph_en	PCIe Tx de-emphasis: 1=Tx de-emphasis enabled	x	gpio_1
PS_2[1]	n/a	Reserved		n/a
PS_2[2]	n/a	Reserved		n/a
PS_2[3]	bios_rom_en	Enable external BIOS ROM: 1=External ROM connected	x	gpio_22
PS_2[4]	vga_dis	VGA disable: 1=Disable this GPU as the system's VGA controller	0	gpio_9
PS_2[5]	n/a	Reserved		n/a
PS_3[1]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[2]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[3]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[5] PS_3[4] PS_0[5]	aud_port_cp[2] aud_port_cp[1] aud_port_cp[0]	3-bit field indicating number of audio-capable display outputs	xxx	n/a

BIT5 => BIT1

PS0	=>	11001
PS1	=>	00001
PS2	=>	00000
PS3	=>	11000

VENDOR	R231	R232
HYNIX 2G	NA	4.75K
MICRON 2G	8.45K	2K
SAM 2G	4.53K	2K
HYNIX 1G	6.98K	4.99K
MICRON 1G	4.53K	4.99K
SAM 1G	3.24K	5.62K

PS3 BIT3=>BIT1	ID	Memory Type	Configuration	PN	Channel Size
000	0	Hynix	H5TC4G63AFR-11C	256Mx16 *4 pces	AKD5PGWTW08 IC SDRAM(96P)H5TC4G63AFR-11C	2G
001	1	Micron	MT41J256M16HA-093G:E	256Mx16 *4 pces	AKD5PZSTL01 IC SDRAM(96P)MT41J256M16HA-093G:E	2G
010	2	Samsung	K4W4G1646B-HC1A	256Mx16 *4 pces	AKD5PZDT501 IC SDRAM(96P)K4W4G1646B-HC1A	2G
011	3	Hynix	H5TC2G63FRR-11C	128Mx16 *4 pces	AKD5MZDTW03 IC SDRAM(96P)H5TC2G63FRR-11C	1G
100	4	Micron	MT41J128M16JT-093G:E	128Mx16 *4 pces		1G
101	5	Samsung	K4W2G1646E-BC1A	128Mx16 *4 pces	AKD5MGGT535 IC SDRAM(96P)K4W2G1646E-BC1A	1G

Fo Mars/ Sun
Change La, Lb
Bead to 0 ohm

Memory Type	
DDR3	27-MHz (± 30 ppm) crystal connected to XTALIN/XTALOUT, or 27-MHz (1.8 V) oscillator connected to XTALIN.
GDDR5	27-MHz (3.3 V) oscillator connected to XO_IN, and 100-MHz (3.3 V) oscillator connected to XO_IN2. (By default, this clock should not be spread since internal spreading is used.)

La
+1.8V_VGA — L23 *0_6/S — +1.8V_DPLL_PVDD
C259 10U/6.3V_8 | C264 1U/6.3V_4 | C265 0.1U/10V_4
Display Phase Lock Loop Power
DPLL_PVDD : 1.8V @ 75mA

Lb
+1.0V_VGA — L21 *0_6/S — +1.0V_DPLL_VDDC
C253 10U/6.3V_8 | C268 1U/6.3V_4 | C267 0.1U/10V_4
1.0V(125mA DPLL_VDDC)
DPLL_PVSS
DPLL_VDDC : 0.935V @ 140mA

+1.8V_MPLL_PVDD — HCB1608KF-471T10 L35
C441 10U/6.3V_8 | C437 1U/6.3V_4 | C438 0.1U/10V_4
MPLL_PVDD : 1.8V @ 150mA

+1.8V_SPLL_PVDD — L16 FCM1005KF-121T03
C167 10U/6.3V_8 | C176 1U/6.3V_4 | C191 0.1U/10V_4
SPLL_PVDD : 1.8V @ 75mA

+1.0V_SPLL_VDDC — L19 HCB1608KF-471T10
C181 10U/6.3V_8 | C222 1U/6.3V_4 | C216 0.1U/10V_4
1.0V(125mA DPLL_VDDC)
SPLL_PVSS
SPLL_VDDC : 0.935V @ 150mA

DPEF_VDD18

Ra R212 *0_4
Rb R249 *0_4
reserve Ra, Rb for future ASIC

10/14: SI modify

U26I — PART 9 OF 9 — SUN_M2_XT

AM32	DPLL_PVDD	
AN31	DPLL_VDDC	
AN32	DPLL_PVSS	
H7	MPLL_PVDD	
H8	MPLL_PVDD	
AM10	SPLL_PVDD	
AN9	SPLL_VDDC	
AN10	SPLL_PVSS	
AF30	NC_XTAL_PVDD	
AF31	NC_XTAL_PVSS	

PLL5XTAL

XTALIN AV33 — 0_4 R759 — CLKGEN_27M 11
XTALIN AV33 — *0_4 R792 — EVGA-XTALI — *22P/50V_4 C244
R207 *10M_4 | Y2 *7A27000010 | C2
XTALOUT AU34 — *0_4 R793 — EVGA-XTALO — *22P/50V_4 C245
11/29: Pre PV modify

XO_IN AW34 — TP129
12/13: PV modify del

XO_IN2 AW35 — R487 *0_4

CLKTESTA AK10 CLKTESTA
CLKTESTB AL10 CLKTESTB
C193 *0.1U/10V_4 | C227 *0.1U/10V_4
R171 *51.1/F_4 | R191 *51.1/F_4
for ASIC
Debug only,
for clock observation,
if not needed, DNI

route 50ohms
single-ended/
100ohms diff and keep short

U26F — PART 6 OF 9 — SUN_M2_XT

PCIE_VSS: AB39, E39, F34, F39, G33, G34, H31, H34, H39, J31, J34, K31, K34, K39, L31, L34, M34, M39, N31, N34, P31, P34, P39, R34, T31, T34, T39, U31, U34, V34, V39, W31, W34, Y34, Y39

GND: F15, F17, F19, F21, F23, F25, F27, F29, F31, F33, F7, F9, G2, G6, H9, J2, J27, J6, J8, K14, K7, L11, L17, L2, L22, L24, L6, M17, M22, M24, N16, N18, N2, N21, N23, N26, N6, R15, R17, R2, R20, R22, R24, R27, R6, T11, T13, T16, T18, T21, T23, T26, U15, U17, U2, U20, U22, U24, U27, U6, V11, V16, V18, V21, V23, V26, W2, W6, Y15, Y17, Y20, Y22, Y24, Y27

GND: A3, A37, AA16, AA18, AA2, AA21, AA23, AA26, AA28, AA6, AB12, AB15, AB17, AB20, AB22, AB24, AB27, AC11, AC13, AC16, AC18, AC2, AC21, AC23, AC26, AC28, AC6, AD15, AD17, AD20, AD22, AD24, AD27, AD9, AE2, AE6, AF10, AF16, AF18, AF21, AG17, AG2, AG20, AG22, AG6, AG9, AH21, AJ10, AJ11, AJ2, AJ28, AJ6, AK11, AK31, AK7, AL11, AL14, AL17, AL2, AL20, AL23, AL26, AL32, AL6, AL8, AM11, AM31, AM9, AN11, AN2, AN30, AN6, AN8, AP11, AP7, AP9, AR5, B11, B13, B15, B17, B19, B21, B23, B25, B27, B29, B31, B33, B7, B9, C1, C39, E35, E5, F11, F13

VSS_MECH: A39, AW1, AW39

AG22 is nc pin

14,18,19,44 +1.0V_VGA → +1.0V_VGA
11,15,18,19,44 +1.8V_VGA → +1.8V_VGA

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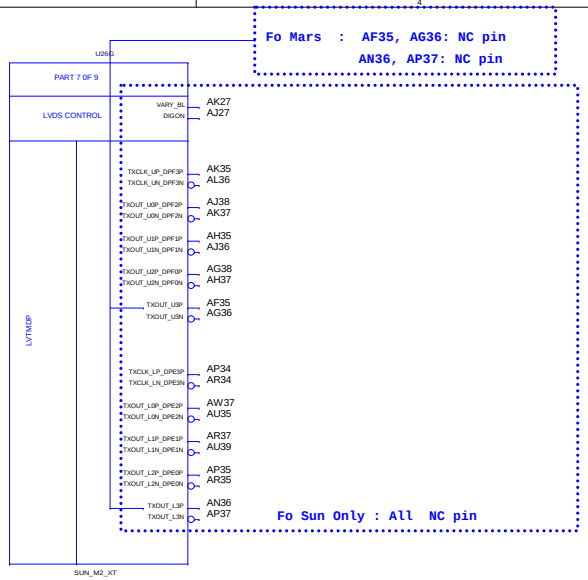
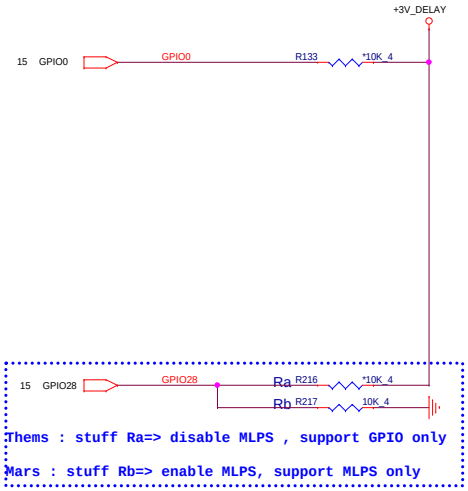




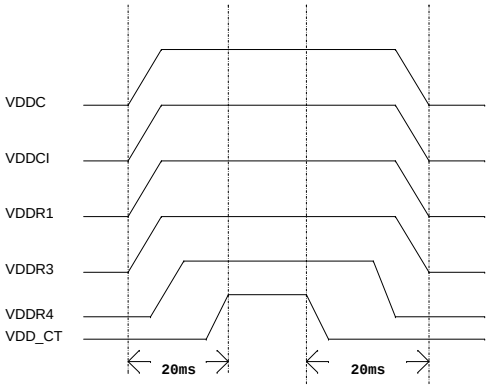
CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET				
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	X
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50%_Tx output swing 1: Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIE Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIE Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1
BIF_VGA DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	XXX
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	X
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled, It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled	X
			NOTE: ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOS ARE USEED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET	
RESERVED RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA NA	GENLK_CLK GPIO8 GPIO21 GENERICC	Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)	0 0 0 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0	
0	128M	0	0	0	+VGA_CORE
0	256M	0	0	1	+VGA_CORE
0	64M	0	1	0	+1.5V_VGA
0	32M	0	1	1	+3.3V_Delay
0	512M	1	0	0	+1.8V_VGA
0	1G	1	0	1	+1.8V_VGA
0	2G	1	1	0	
0	4G	1	1	1	

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

Power Up/Down Sequence



NB5

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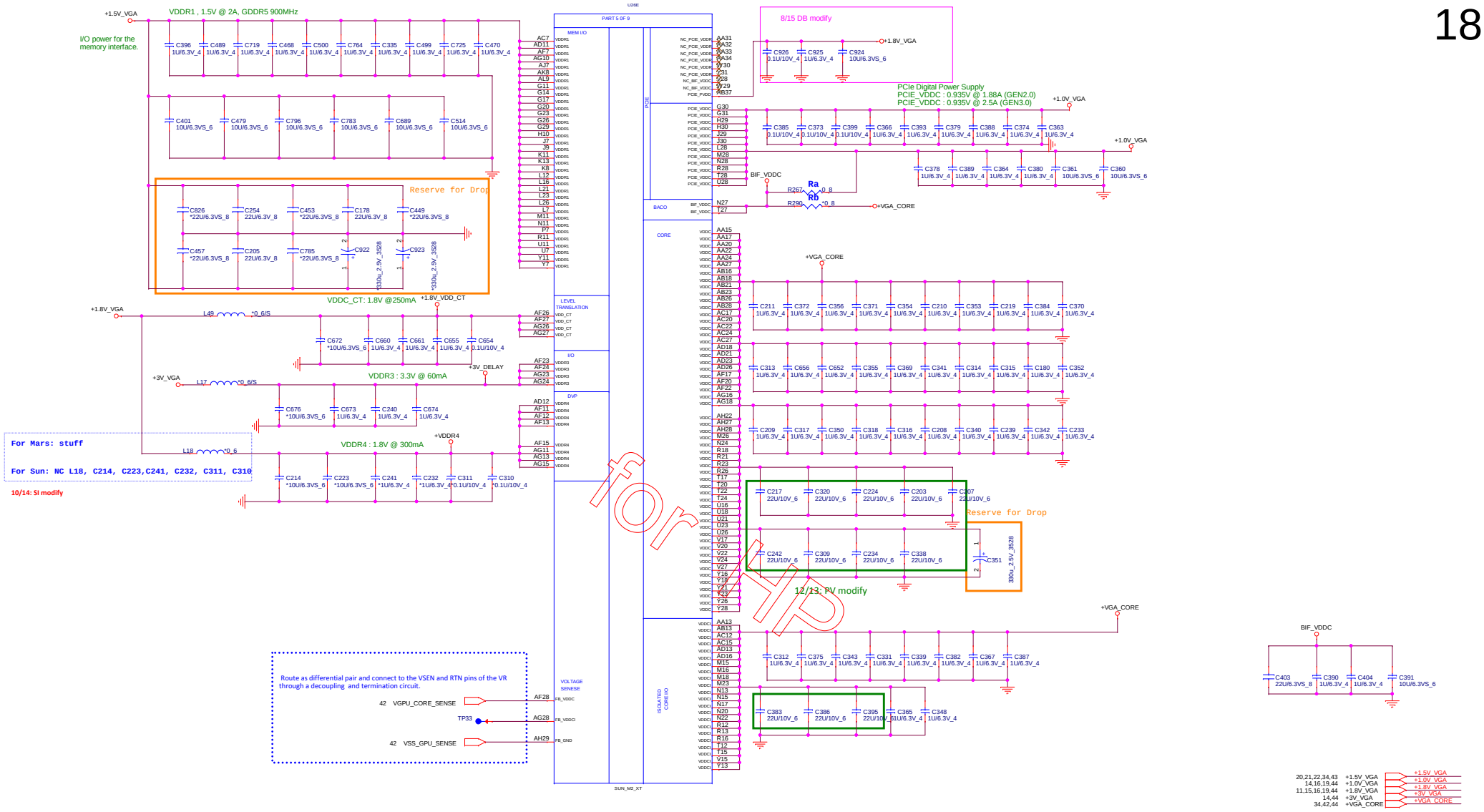

Support BACO Mode

Note1. 1. No BACO Support :BIF_VDDC shorts with VDDC (Install Ra)

2. BACO Support: Refer to the BACO reference schematics/Application note for detail about BIF_VDDC Rail if BACO is Supported (Uninstall Ra)

PX_EN = 0, for Normal Operation
PX_EN = 1, for BACO MODE

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For Mars : L20 sutff
For Sun: L20 , C247 , C246 , C252 NC

+1.0V_VGA
DPAB_VDD10
L20 *0_6
C247 *0.1U/10V_4
C246 *1U/6.3V_4
C252 *10U/6.3VS_6
10/14: SI modify

U26H
PART 8 0F 9
DP_VDDR
DP_VDDC
DP GND
CALIBRATION

DP_VDDC: AP31, AP32, AN33, AP33
DP_VDDR: AN24, AP24, AP25, AP26, AU28, AV29
DP_VDDC: AP13, AT13, AP14, AP15
DP_VDDC: AL33, AM33, AK33, AK34
DP_VDDR: AP20, AP21, AP22, AP23, AU18, AV19
DP_VDDR: AH34, AJ34, AF34, AG34, AM37, AL38
DP_VSSR: AN27, AP27, AP28, AW24, AW26, AN29, AP29, AP30, AW30, AW32, AN17, AP16, AP17, AW14, AW16, AN19, AP18, AP19, AW20, AW22, AN34, AP39, AR39, AU37, AF39, AH39, AK39, AL34, AV27, AR28, AV17, AR18, AN38, AM35
DPAB_CALR: AW28
DPCD_CALR: AW18
DPEF_CALR: AM39

10/14: SI modify

DPEF_VDD10
L25 *0_6
C291 *0.1U/10V_4
C290 *1U/6.3V_4
C293 *10U/6.3VS_6

For Mars : L25 sutff
For Sun : L25/ C293/C290/C291 NC

10/14: SI modify

For Mars : L26 sutff
For Sun: L26 , C279 , C281 , C282 NC

+1.8V_VGA
DPEF_VDD18
L26 *0_6
C279 *10U/6.3VS_6
C281 *1U/6.3V_4
C282 *0.1U/10V_4

10/14: SI modify

R495 *150/F_4

For Mars : R495 sutff
For Sun : R495 NC

10/14: SI modify DEL R754

For Mars : R754 sutff
For Sun : R754 NC

14,16,18,44 +1.0V_VGA
11,15,16,18,44 +1.8V_VGA
+1.0V_VGA
+1.8V_VGA

SUN_M2_XT

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21 VMA_ODT0 — VMA_ODT0
21 VMA_ODT1 — VMA_ODT1
21 VMA_RAS0# — VMA_RAS0#
21 VMA_RAS1# — VMA_RAS1#
21 VMA_CAS0# — VMA_CAS0#
21 VMA_CAS1# — VMA_CAS1#
21 VMA_WE0# — VMA_WE0#
21 VMA_WE1# — VMA_WE1#
21 VMA_CS0# — VMA_CS0#
21 VMA_CS1# — VMA_CS1#
21 VMA_CKE0 — VMA_CKE0
21 VMA_CKE1 — VMA_CKE1
21 VMA_CLK0 — VMA_CLK0#
21 VMA_CLK1 — VMA_CLK1#
21 VMA_WDQS[7..0] — VMA_WDQS[7..0]
21 VMA_RDQS[7..0] — VMA_RDQS[7..0]
21 VMA_DM[7..0] — VMA_DM[7..0]
21 VMA_DQ[63..0] — VMA_DQ[63..0]
21 VMA_MA[14..0] — VMA_MA[14..0]
21 VMA_BA0 — VMA_BA0
21 VMA_BA1 — VMA_BA1
21 VMA_BA2 — VMA_BA2

For Sun : ALL NC PIN

U26C
PART 3 OF 9
GDDR5/DDR3
MEMORY INTERFACE A

VMA_DQ0	C37	DQA0_0	
VMA_DQ1	C35	DQA0_1	
VMA_DQ2	A35	DQA0_2	
VMA_DQ3	E34	DQA0_3	
VMA_DQ4	G32	DQA0_4	
VMA_DQ5	D33	DQA0_5	
VMA_DQ6	F32	DQA0_6	
VMA_DQ7	E32	DQA0_7	
VMA_DQ8	D31	DQA0_8	
VMA_DQ9	F30	DQA0_9	
VMA_DQ10	C30	DQA0_10	
VMA_DQ11	A30	DQA0_11	
VMA_DQ12	F28	DQA0_12	
VMA_DQ13	C28	DQA0_13	
VMA_DQ14	A28	DQA0_14	
VMA_DQ15	E28	DQA0_15	
VMA_DQ16	D27	DQA0_16	
VMA_DQ17	F26	DQA0_17	
VMA_DQ18	C26	DQA0_18	
VMA_DQ19	A26	DQA0_19	
VMA_DQ20	F24	DQA0_20	
VMA_DQ21	C24	DQA0_21	
VMA_DQ22	A24	DQA0_22	
VMA_DQ23	E24	DQA0_23	
VMA_DQ24	C22	DQA0_24	
VMA_DQ25	A22	DQA0_25	
VMA_DQ26	F22	DQA0_26	
VMA_DQ27	D21	DQA0_27	
VMA_DQ28	A20	DQA0_28	
VMA_DQ29	F20	DQA0_29	
VMA_DQ30	D19	DQA0_30	
VMA_DQ31	E18	DQA0_31	
VMA_DQ32	C18	DQA1_0	
VMA_DQ33	A18	DQA1_1	
VMA_DQ34	F18	DQA1_2	
VMA_DQ35	D17	DQA1_3	
VMA_DQ36	A16	DQA1_4	
VMA_DQ37	F16	DQA1_5	
VMA_DQ38	D15	DQA1_6	
VMA_DQ39	E14	DQA1_7	
VMA_DQ40	F14	DQA1_8	
VMA_DQ41	D13	DQA1_9	
VMA_DQ42	F12	DQA1_10	
VMA_DQ43	A12	DQA1_11	
VMA_DQ44	D11	DQA1_12	
VMA_DQ45	F10	DQA1_13	
VMA_DQ46	A10	DQA1_14	
VMA_DQ47	C10	DQA1_15	
VMA_DQ48	G13	DQA1_16	
VMA_DQ49	H13	DQA1_17	
VMA_DQ50	J13	DQA1_18	
VMA_DQ51	H11	DQA1_19	
VMA_DQ52	G10	DQA1_20	
VMA_DQ53	G8	DQA1_21	
VMA_DQ54	K9	DQA1_22	
VMA_DQ55	K10	DQA1_23	
VMA_DQ56	G9	DQA1_24	
VMA_DQ57	A8	DQA1_25	
VMA_DQ58	C8	DQA1_26	
VMA_DQ59	E8	DQA1_27	
VMA_DQ60	A6	DQA1_28	
VMA_DQ61	C6	DQA1_29	
VMA_DQ62	E6	DQA1_30	
VMA_DQ63	A5	DQA1_31	
MVREFDA	L18	MVREFDA	
MVREFSA	L20	MVREFSA	
	L27	NC_MEM_CALRN0	
	N12	NC_MEM_CALRN1	
	AG12	NC_MEM_CALRN2	
	M12	NC_MEM_CALRP1	
	M27	MEM_CALRP0	
	AH12	MEM_CALRP2	

For Sun : ALL NC PIN

MAA0_0/MAA_0	G24	VMA_MA0	
MAA0_1/MAA_1	J23	VMA_MA1	
MAA0_2/MAA_2	H24	VMA_MA2	
MAA0_3/MAA_3	J24	VMA_MA3	
MAA0_4/MAA_4	H26	VMA_MA4	
MAA0_5/MAA_5	J26	VMA_MA5	
MAA0_6/MAA_6	H21	VMA_MA6	
MAA0_7/MAA_7	G21	VMA_MA7	
MAA1_0/MAA_8	H19	VMA_MA8	
MAA1_1/MAA_9	H20	VMA_MA9	
MAA1_2/MAA_10	L13	VMA_MA10	
MAA1_3/MAA_11	G16	VMA_MA11	
MAA1_4/MAA_12	J16	VMA_MA12	
MAA1_5/MAA_BA2	H16	VMA_BA2	
MAA1_6/MAA_BA0	J17	VMA_BA0	
MAA1_7/MAA_BA1	H17	VMA_BA1	
WCKA0_0/DQMA_0	A32	VMA_DM0	
WCKA0B_0/DQMA_1	C32	VMA_DM1	
WCKA0_1/DQMA_2	D23	VMA_DM2	
WCKA0B_1/DQMA_3	E22	VMA_DM3	
WCKA1_0/DQMA_4	C14	VMA_DM4	
WCKA1B_0/DQMA_5	A14	VMA_DM5	
WCKA1_1/DQMA_6	E10	VMA_DM6	
WCKA1B_1/DQMA_7	D9	VMA_DM7	
EDCA0_0/QSA_0	C34	VMA_RDQS0	
EDCA0_1/QSA_1	D29	VMA_RDQS1	
EDCA0_2/QSA_2	D25	VMA_RDQS2	
EDCA0_3/QSA_3	E20	VMA_RDQS3	
EDCA1_0/QSA_4	E16	VMA_RDQS4	
EDCA1_1/QSA_5	E12	VMA_RDQS5	
EDCA1_2/QSA_6	J10	VMA_RDQS6	
EDCA1_3/QSA_7	D7	VMA_RDQS7	
DDBIA0_0/QSA_0B	A34	VMA_WDQS0	
DDBIA0_1/QSA_1B	E30	VMA_WDQS1	
DDBIA0_2/QSA_2B	E26	VMA_WDQS2	
DDBIA0_3/QSA_3B	C20	VMA_WDQS3	
DDBIA1_0/QSA_4B	C16	VMA_WDQS4	
DDBIA1_1/QSA_5B	C12	VMA_WDQS5	
DDBIA1_2/QSA_6B	J11	VMA_WDQS6	
DDBIA1_3/QSA_7B	F8	VMA_WDQS7	
ADBIA0/ODTA0	J21	VMA_ODT0	
ADBIA1/ODTA1	G19	VMA_ODT1	
CLKA0	H27	VMA_CLK0	
CLKA0B	G27	VMA_CLK0#	
CLKA1	J14	VMA_CLK1	
CLKA1B	H14	VMA_CLK1#	
RASA0B	K23	VMA_RAS0#	
RASA1B	K19	VMA_RAS1#	
CASA0B	K20	VMA_CAS0#	
CASA1B	K17	VMA_CAS1#	
CSA0B_0	K24	VMA_CS0#	
CSA0B_1	K27		
CSA1B_0	M13	VMA_CS1#	
CSA1B_1	K16		
CKEA0	K21	VMA_CKE0	
CKEA1	J20	VMA_CKE1	
WEA0B	K26	VMA_WE0#	
WEA1B	L15	VMA_WE1#	
MAA0_8/MAA_13	H23	VMA_MA13	
MAA1_8/MAA_14	J19	VMA_MA14	
MAA0_9/MAA_15	M21	TP61	
MAA1_9/RSVD	M20	TP60	

J19
For Mars : MAA_14
For Sun : NC

M21
For Mars : MAA_15
For Sun : NC

M20
For Mars : RSVD
For Sun : NC

8/15: DB MODIFY

+1.5V_VGA
R331 40.2/F_4
C466 *1U/6.3V_4
R330 100/F_4

PLACE MVREFD DIVIDERS
AND CAPS CLOSE TO ASIC

+1.5V_VGA
R327 40.2/F_4
C462 *1U/6.3V_4
R328 100/F_4

R295 120/F_4

For MARS / SUN
Re stuff 120 ohm 1%

8/15: DB MODIFY

SUN_M2_XT

22 VMB_ODT0 — VMB_ODT0
22 VMB_ODT1 — VMB_ODT1
22 VMB_RAS0# — VMB_RAS0#
22 VMB_RAS1# — VMB_RAS1#
22 VMB_CAS0# — VMB_CAS0#
22 VMB_CAS1# — VMB_CAS1#
22 VMB_WE0# — VMB_WE0#
22 VMB_WE1# — VMB_WE1#
22 VMB_CS0# — VMB_CS0#
22 VMB_CS1# — VMB_CS1#
22 VMB_CKE0 — VMB_CKE0
22 VMB_CKE1 — VMB_CKE1
22 VMB_CLK0 — VMB_CLK0#
22 VMB_CLK1 — VMB_CLK1#
22 VMB_WDQS[7..0] — VMB_WDQS[7..0]
22 VMB_RDQS[7..0] — VMB_RDQS[7..0]
22 VMB_DM[7..0] — VMB_DM[7..0]
22 VMB_DQ[63..0] — VMB_DQ[63..0]
22 VMB_MA[14..0] — VMB_MA[14..0]
22 VMB_BA0 — VMB_BA0
22 VMB_BA1 — VMB_BA1
22 VMB_BA2 — VMB_BA2

+1.5V_VGA
R317 40.2/F_4
C440 1U/6.3V_4
R321 100/F_4

PLACE MVREFD DIVIDERS
AND CAPS CLOSE TO ASIC

+1.5V_VGA
R159 40.2/F_4
C157 1U/6.3V_4
R145 100/F_4

U26D
PART 4 OF 9
GDDR5/DDR3
MEMORY INTERFACE B

VMB_DQ0	C5	DQB0_0	
VMB_DQ1	C3	DQB0_1	
VMB_DQ2	E3	DQB0_2	
VMB_DQ3	E1	DQB0_3	
VMB_DQ4	F1	DQB0_4	
VMB_DQ5	F3	DQB0_5	
VMB_DQ6	F5	DQB0_6	
VMB_DQ7	G4	DQB0_7	
VMB_DQ8	H5	DQB0_8	
VMB_DQ9	H6	DQB0_9	
VMB_DQ10	J4	DQB0_10	
VMB_DQ11	K6	DQB0_11	
VMB_DQ12	K5	DQB0_12	
VMB_DQ13	L4	DQB0_13	
VMB_DQ14	M6	DQB0_14	
VMB_DQ15	M1	DQB0_15	
VMB_DQ16	M3	DQB0_16	
VMB_DQ17	M5	DQB0_17	
VMB_DQ18	N4	DQB0_18	
VMB_DQ19	P6	DQB0_19	
VMB_DQ20	P5	DQB0_20	
VMB_DQ21	R4	DQB0_21	
VMB_DQ22	T6	DQB0_22	
VMB_DQ23	T1	DQB0_23	
VMB_DQ24	U4	DQB0_24	
VMB_DQ25	V6	DQB0_25	
VMB_DQ26	V1	DQB0_26	
VMB_DQ27	V3	DQB0_27	
VMB_DQ28	Y6	DQB0_28	
VMB_DQ29	Y1	DQB0_29	
VMB_DQ30	Y3	DQB0_30	
VMB_DQ31	Y5	DQB0_31	
VMB_DQ32	AA4	DQB1_0	
VMB_DQ33	AB6	DQB1_1	
VMB_DQ34	AB1	DQB1_2	
VMB_DQ35	AB3	DQB1_3	
VMB_DQ36	AD6	DQB1_4	
VMB_DQ37	AD1	DQB1_5	
VMB_DQ38	AD3	DQB1_6	
VMB_DQ39	AD5	DQB1_7	
VMB_DQ40	AF1	DQB1_8	
VMB_DQ41	AF3	DQB1_9	
VMB_DQ42	AF6	DQB1_10	
VMB_DQ43	AG4	DQB1_11	
VMB_DQ44	AH5	DQB1_12	
VMB_DQ45	AH6	DQB1_13	
VMB_DQ46	AJ4	DQB1_14	
VMB_DQ47	AK3	DQB1_15	
VMB_DQ48	AF8	DQB1_16	
VMB_DQ49	AF9	DQB1_17	
VMB_DQ50	AG8	DQB1_18	
VMB_DQ51	AG7	DQB1_19	
VMB_DQ52	AK9	DQB1_20	
VMB_DQ53	AL7	DQB1_21	
VMB_DQ54	AM8	DQB1_22	
VMB_DQ55	AM7	DQB1_23	
VMB_DQ56	AK1	DQB1_24	
VMB_DQ57	AL4	DQB1_25	
VMB_DQ58	AM6	DQB1_26	
VMB_DQ59	AM1	DQB1_27	
VMB_DQ60	AN4	DQB1_28	
VMB_DQ61	AP3	DQB1_29	
VMB_DQ62	AP1	DQB1_30	
VMB_DQ63	AP5	DQB1_31	
MVREFDB	Y12	MVREFDB	
MVREFSB	AA12	MVREFSB	

MAB0_0/MAB_0	P8	VMB_MA0	
MAB0_1/MAB_1	T9	VMB_MA1	
MAB0_2/MAB_2	P9	VMB_MA2	
MAB0_3/MAB_3	N7	VMB_MA3	
MAB0_4/MAB_4	N8	VMB_MA4	
MAB0_5/MAB_5	N9	VMB_MA5	
MAB0_6/MAB_6	U9	VMB_MA6	
MAB0_7/MAB_7	U8	VMB_MA7	
MAB1_0/MAB_8	Y9	VMB_MA8	
MAB1_1/MAB_9	W9	VMB_MA9	
MAB1_2/MAB_10	AC8	VMB_MA10	
MAB1_3/MAB_11	AC9	VMB_MA11	
MAB1_4/MAB_12	AA7	VMB_MA12	
MAB1_5/BA2	AA8	VMB_BA2	
MAB1_6/BA0	Y8	VMB_BA0	
MAB1_7/BA1	AA9	VMB_BA1	
WCKB0_0/DQMB_0	H3	VMB_DM0	
WCKB0B_0/DQMB_1	H1	VMB_DM1	
WCKB0_1/DQMB_2	T3	VMB_DM2	
WCKB0B_1/DQMB_3	T5	VMB_DM3	
WCKB1_0/DQMB_4	AE4	VMB_DM4	
WCKB1B_0/DQMB_5	AF5	VMB_DM5	
WCKB1_1/DQMB_6	AK6	VMB_DM6	
WCKB1B_1/DQMB_7	AK5	VMB_DM7	
EDCB0_0/QSB_0	F6	VMB_RDQS0	
EDCB0_1/QSB_1	K3	VMB_RDQS1	
EDCB0_2/QSB_2	P3	VMB_RDQS2	
EDCB0_3/QSB_3	V5	VMB_RDQS3	
EDCB1_0/QSB_4	AB5	VMB_RDQS4	
EDCB1_1/QSB_5	AH1	VMB_RDQS5	
EDCB1_2/QSB_6	AJ9	VMB_RDQS6	
EDCB1_3/QSB_7	AM5	VMB_RDQS7	
DDBIB0_0/QSB_0B	G7	VMB_WDQS0	
DDBIB0_1/QSB_1B	K1	VMB_WDQS1	
DDBIB0_2/QSB_2B	P1	VMB_WDQS2	
DDBIB0_3/QSB_3B	W4	VMB_WDQS3	
DDBIB1_0/QSB_4B	AC4	VMB_WDQS4	
DDBIB1_1/QSB_5B	AH3	VMB_WDQS5	
DDBIB1_2/QSB_6B	AJ8	VMB_WDQS6	
DDBIB1_3/QSB_7B	AM3	VMB_WDQS7	
ADBIB0/ODTB0	T7	VMB_ODT0	
ADBIB1/ODTB1	W7	VMB_ODT1	
CLKB0	L9	VMB_CLK0	
CLKB0B	L8	VMB_CLK0#	
CLKB1	AD8	VMB_CLK1	
CLKB1B	AD7	VMB_CLK1#	
RASB0B	T10	VMB_RAS0#	
RASB1B	Y10	VMB_RAS1#	
CASB0B	W10	VMB_CAS0#	
CASB1B	AA10	VMB_CAS1#	
CSB0B_0	P10	VMB_CS0#	
CSB0B_1	L10		
CSB1B_0	AD10	VMB_CS1#	
CSB1B_1	AC10		
CKEB0	U10	VMB_CKE0	
CKEB1	AA11	VMB_CKE1	
WEB0B	N10	VMB_WE0#	
WEB1B	AB11	VMB_WE1#	
MAB0_8/MAB_13	T8	VMB_MA13	
MAB1_8/MAB_14	W8	VMB_MA14	
MAB0_9/MAB_15	U12	TP52	
MAB1_9/RSVD	V12	TP49	
DRAM_RST	AH11	DRAM_RST	

need check

8/15 Modify

SUN_M2_XT

DRAM_RST — R162 10/F_4 — R170 51_4 — DRAM_RST_M — DRAM_RST_M 21,22
R163 4.99K/F_4
C177 120P/50V_4

18,21,22,34,43 +1.5V_VGA — +1.5V_VGA

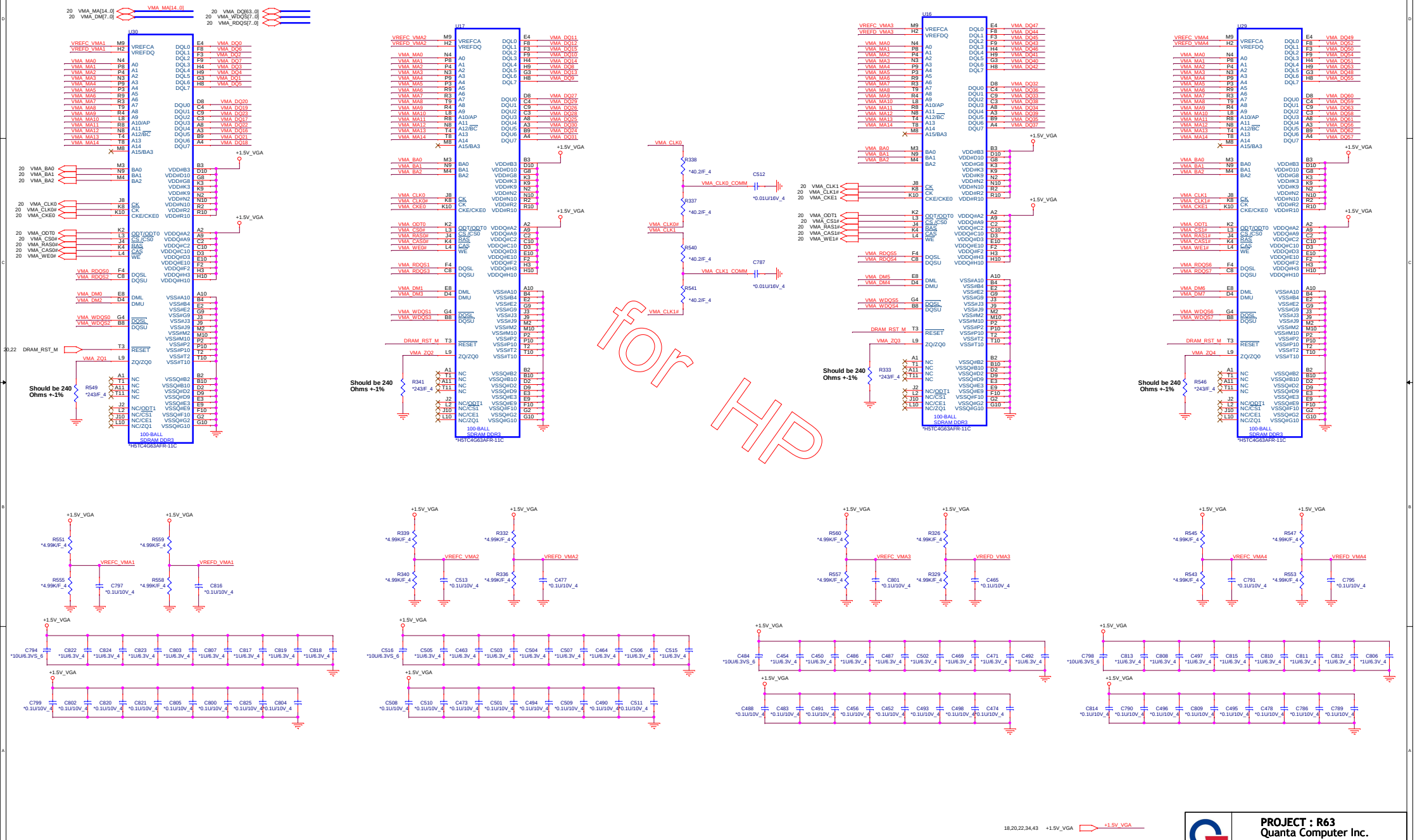
NB5

PROJECT : R63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	THAMES_MEM_Interface	1A

Date: Friday, December 21, 2012 | Sheet 20 of 44

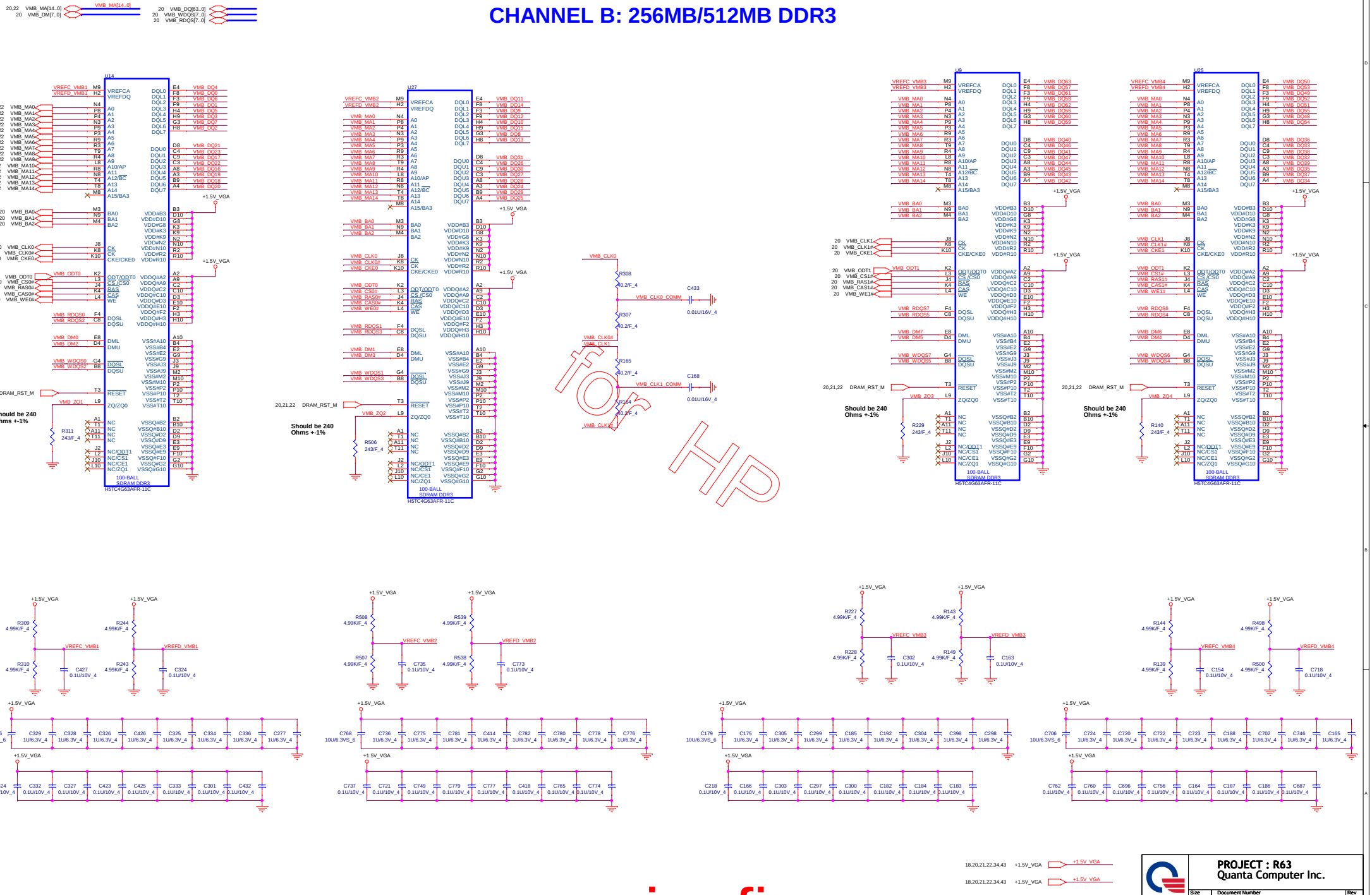
CHANNEL A: 256MB/512MB DDR3



18,20,22,34,43 +1.5V_VGA +1.5V_VGA

NB5	PROJECT : R63 Quanta Computer Inc.	
Size: Custom	Document Number: VRAM-A (DDR3 BGA96)	Rev: 3A
Date: Friday, December 21, 2012	Sheet 21 of 44	

CHANNEL B: 256MB/512MB DDR3



PROJECT : R63	
Quanta Computer Inc.	
NB5	
Size: Custom	Document Number: VRAM-B (DDR3 BGA96)
Rev: 1A	
Date: Friday, December 21, 2012	Sheet 22 of 44

7,26,28,29,32,33,34,39 +5V
2,6,7,8,9,10,12,13,14,24,25,26,27,28,29,30,31,32,33,34,39,40,42,44 +3V
29,30,34,36,37,38,39,40,41,42,43,44 +5VS5
26 +5V_HDMIC

CRT PORT

10/24: SI modify

12/13: PV modify

6 CRT_R
6 CRT_G
6 CRT_B
6 HSYNC_COM
6 VSYNC_COM
6 DDCCLK
6 DDCDATA

CRT_R L15 BLM18BB470 CRT_R1
CRT_G L14 BLM18BB470 CRT_G1
CRT_B L13 BLM18BB470 CRT_B1

R112 150/F_4
R104 150/F_4
R100 150/F_4

C131 22P/50V_4
C115 22P/50V_4
C125 22P/50V_4
C101 22P/50V_4
C102 22P/50V_4
C138 22P/50V_4

EMI

CRT CONN CN9
DFDS15FR362
dsub-dsd-15atxb-15p

CRTDDCDAT2 C170 *470P/50V_4
CRTHSYNC C199 10P/50V_4
CRTVSYNC C200 10P/50V_4
CRTDDCCLK2 C174 *470P/50V_4
+5V_HDMIC

HSYNC_COM
VSYNC_COM
DDCCLK
DDCDATA

+5V
+3V
+5V_CRT2
C134 0.22U/25V_6
CRT_BYP

U7
VCC_SYNC
VCC_DDC
BYP
VCC_VIDEO
VIDEO_1
VIDEO_2
VIDEO_3
GND
SYNC_OUT2
SYNC_OUT1
SYNC_IN2
SYNC_IN1
DDC_IN1
DDC_IN2
DDC_OUT1
DDC_OUT2
TPD7S019

CRT_VSYNC1 R157 22_4 CRTVSYNC
CRT_HSYNC1 R156 22_4 CRTHSYNC
VSYNC_COM
HSYNC_COM
DDCCLK
DDCDATA
VGA_DDC_CLK_RT
VGA_DDC_DAT_RT
R148 2.2K_4
R160 2.2K_4
CRTDDCCLK2
CRTDDCDAT2

DDCCLK R168 2.7K_4
DDCDATA R169 2.7K_4
+3V

+5V_HDMIC
+5V_HDMIC
MEK500V-40 D3
+5V_CRT2
C146 0.1U/10V_4

9/29 EMI request
+5VS5
C609 0.1U/10V_4
C64 0.1U/10V_4
C71 0.1U/10V_4

9/27 EMI request

HOLE

H27 *spad-r63-8np
H16 *h-tc354bc315ic150d110p2
H5 *h-c354ic150d110p2
H6 *h-c354ic150d110p2
H4 *h-c354ic150d110p2

12/20: PV add

H20 *H-C315IC150D110P2
H22 *h-c197d110p2
H21 *h-c315ic150d110p2
H3 *H-C197D110P2
H17 *h-tc276bc315d236p2
H26 *H-C87D87N
H25 *spad-re197x79np

10/17: SI modify add H25

11/30: Pre PV modify add H26

12/13: PV modify H26 Del gnd

FAN hole
H2 *O-LX9-1

PCH BKT
H19 h-tc177bc276ic162d122p2
H18 h-tc177bc276ic162d122p2
Nut PN:MBUL1001010

CPU BKT
H11 *intel-cpu-bkt2

VGA BKT
H15 *H-TC248BC197D150P2
H14 *H-TC248BC197D150P2
H10 *H-TC248BC197D150P2

THERMAL BKT
H9 h-tc177bc276ic162d122p2
H1 *h-tc256bc276d168x155p2
H24 *h-e315x278d110p2

KB lock
H13 *H-TC354BC315IC150D110P2
H8 *H-TC354BC315IC150D110P2

NB5

PROJECT : R63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT,Hole	1A
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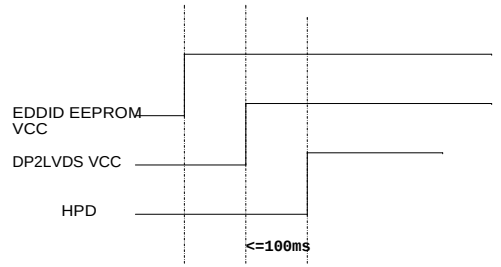
RTD2136S Power Up Sequence 24



Reserve for co layout EDP CON, EDP only please stuff

RTD2136 Dual Channel only

Pine 18: keep 80 Mile Trace

RTD2136R

IC底部需接GND

Use 1% Res on R2178

Reserve

Default

Reserve

12/13: PV modify

*M24C64

Reserve

keep 80 Mile Trace

USING 60R 2A

CLOSE TO Pin22

Close to Pin18
C2142 close to IC side

USING 60R 1A

Close to Pin5

L8: need use CV-4709MN00 for Vendor suggestion

Close to Pin17

Close to Pin11

Close to Pin43

SWR MODE	LDO MODE
Stuff L8	Stuff R86

PROJECT : R63
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	RTD2136	1A

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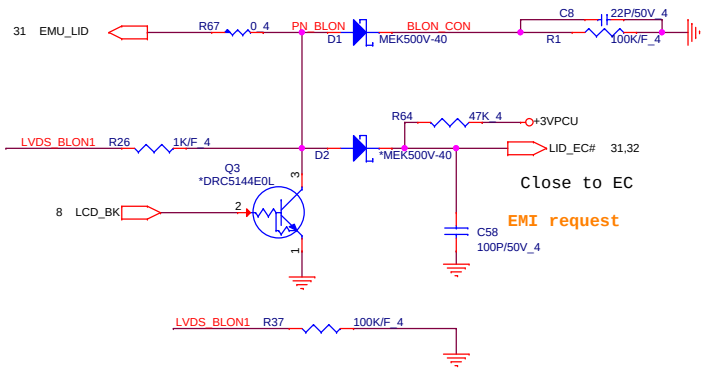
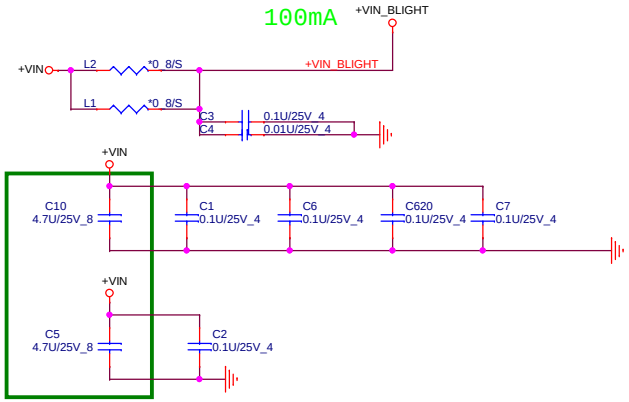
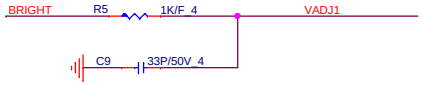
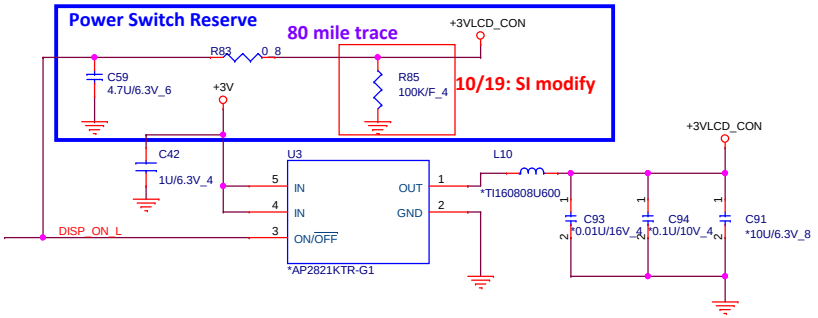
LID Switch

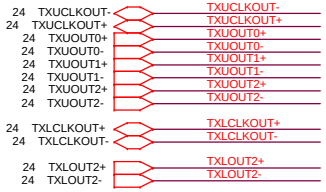


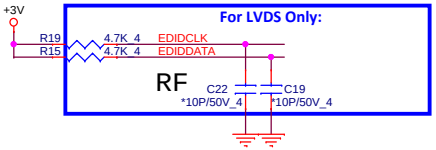


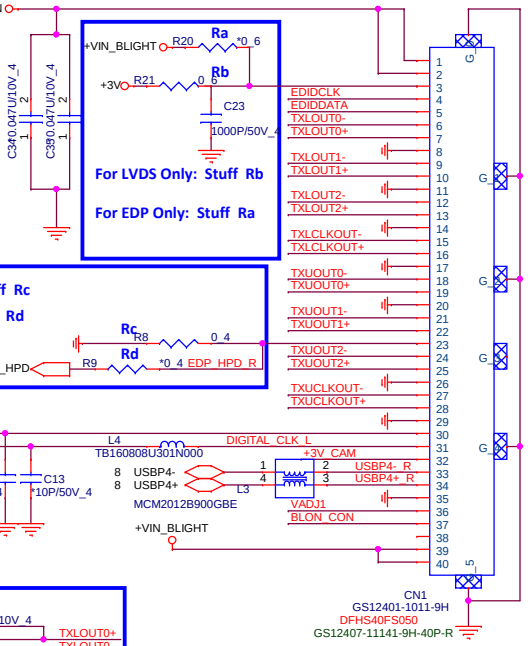
12/17: PV modify pn for 0.85 height

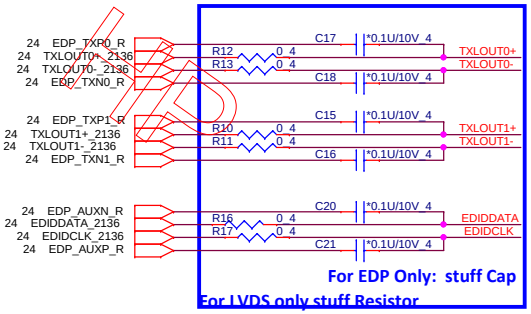


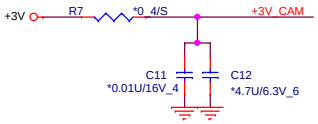


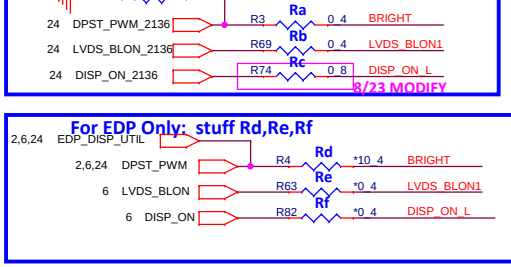


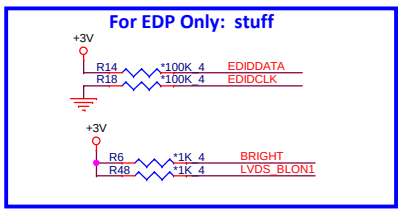


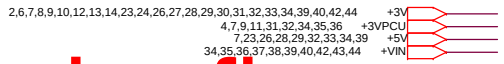












for

PROJECT : R63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN/LID/CAM	1A
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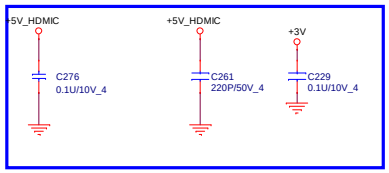
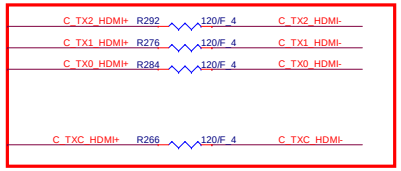
NB5

7,23,28,29,32,33,34,39 +5V
23 +5V_HDMIC
2,6,7,8,9,10,12,13,14,23,24,25,27,28,29,30,31,32,33,34,39,40,42,44 +3V

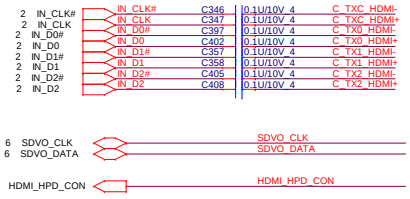
EMI request



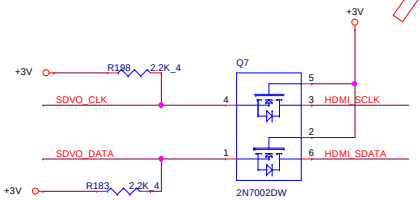
10/14: SI for EMI request

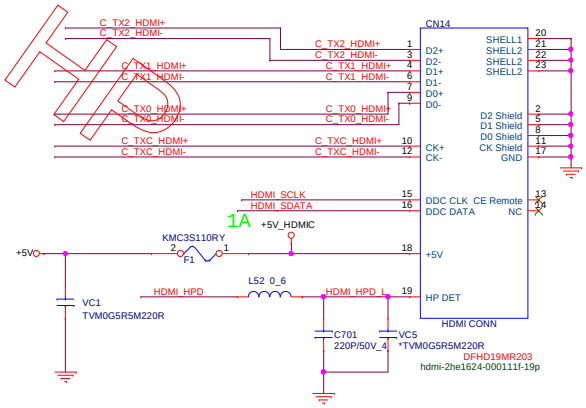


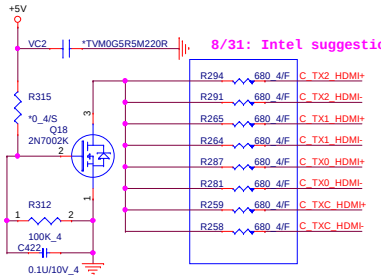
close to HDMI conn

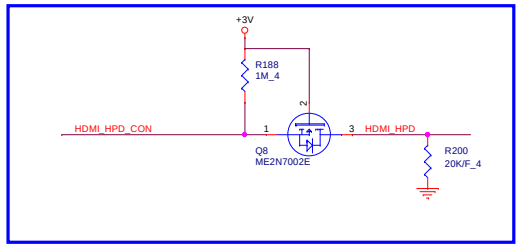


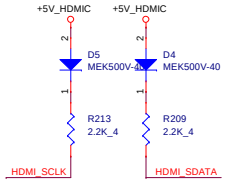
Close to HDMI Connector











NB5

PROJECT : R63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDMI CONN	1A

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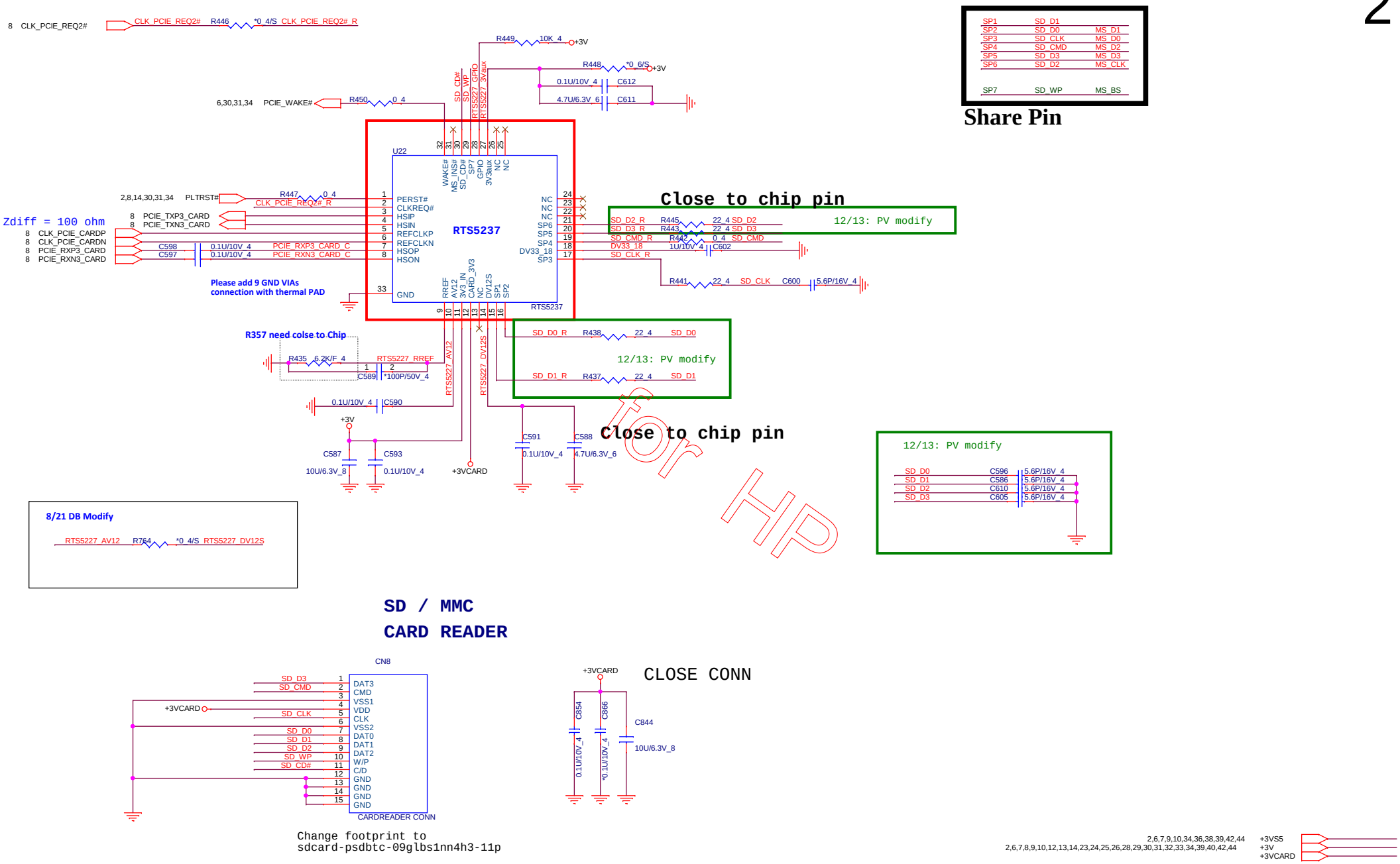
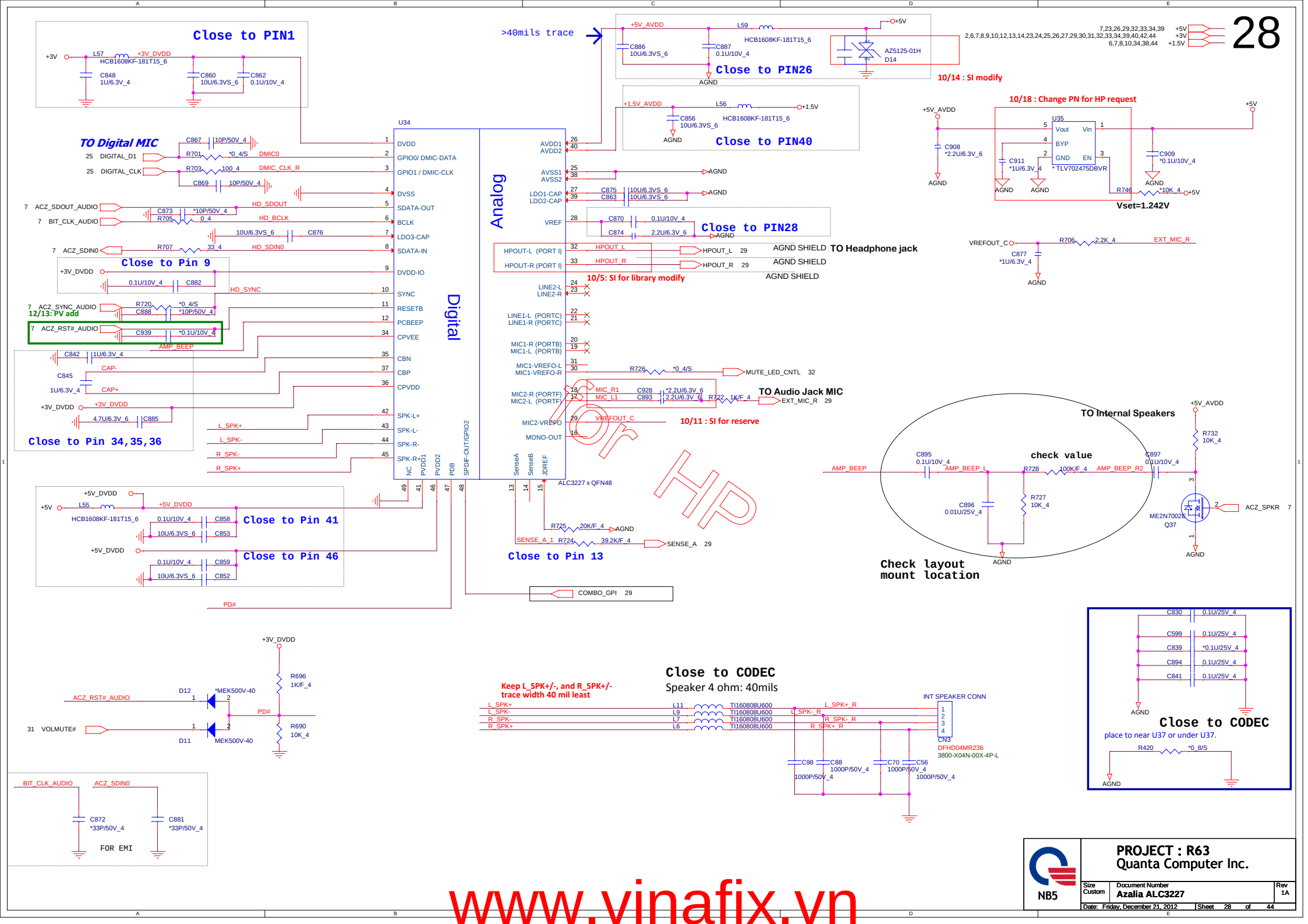


PROJECT : R63
Quanta Computer Inc.

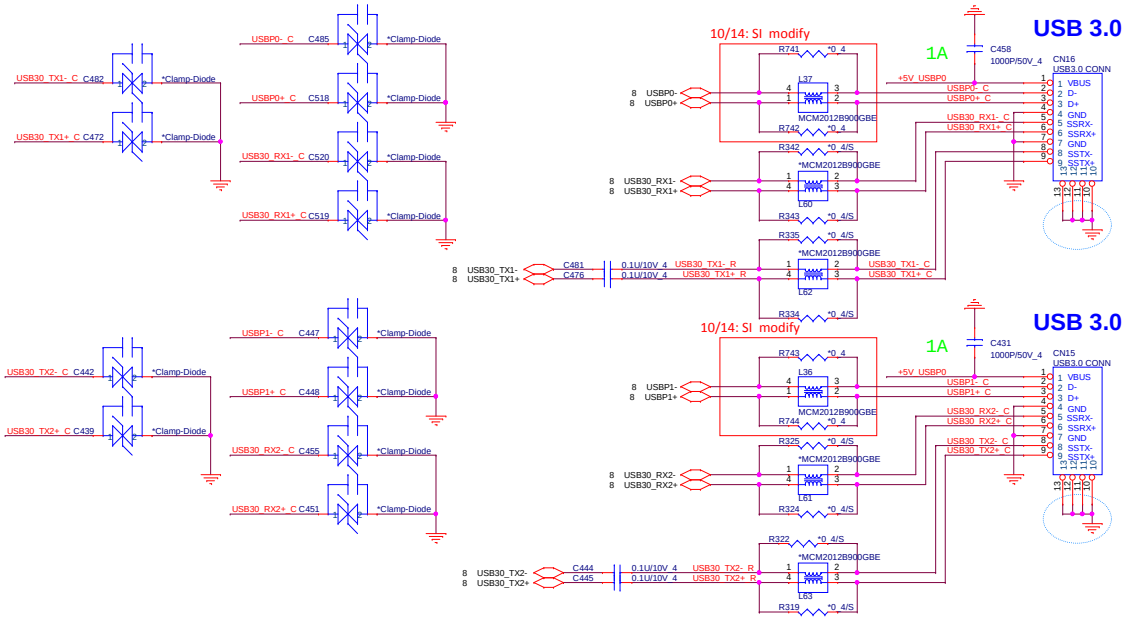
Size	Document Number	Rev
Custom	RTS5229 & CR SOCKET	1A

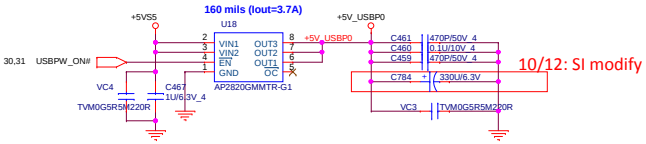
NB5

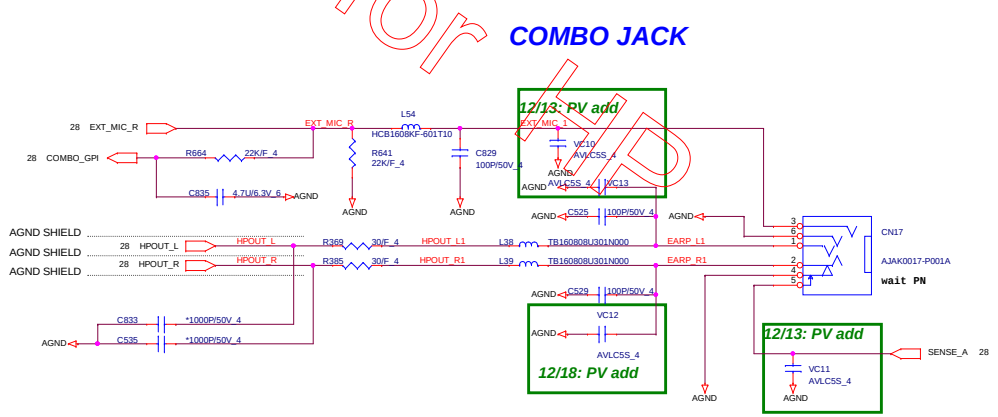
Date: Friday, December 21, 2012 Sheet 27 of 44

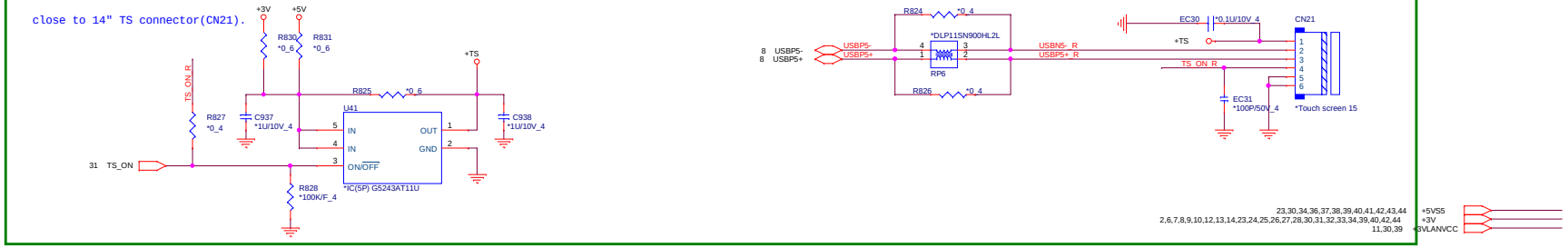


NB5	PROJECT : R63 Quanta Computer Inc.	
Size: Custom	Document Number: Azalia ALC3227	Rev: 1A
Date: Friday, December 21, 2012	Sheet 28 of 44	



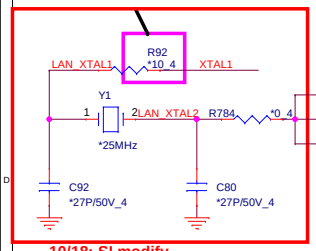






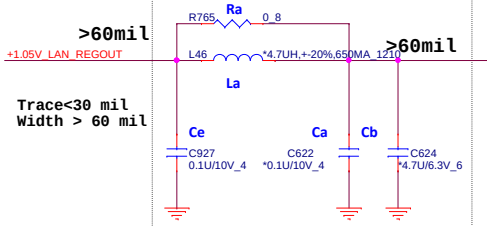
PROJECT : R63
Quanta Computer Inc.
NB5
Size Custom | Document Number USB/BT/Audio JacK | Rev 1A
Date: Friday, December 21, 2012 | Sheet 29 of 44

For EMI 0 ~ 22 ohm



10/18: SI modify

Power trace Layout 寬度> 60mil



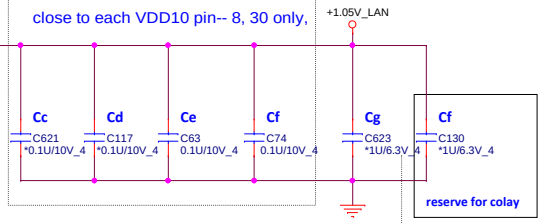
Trace<30 mil
Width > 60 mil

For GbE
Stuff La, Ca ,Cb

For 10/100
NA: La, Ca ,Cb
STUFF : Ra, Ce

For GbE
* Place Cc,Cd,Ce,Cf
close to each VDD10 pin-- 3, 22, 8 , 30

For 10/100 NA Ce,Cf
* Place Ce , Cf
close to each VDD10 pin-- 8, 30 only,

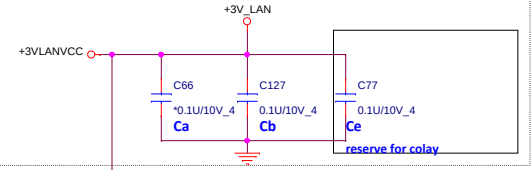


For GbE
* Place Cf close to each VDD10 pin-- 22 (reserve)

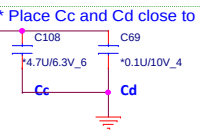
For 10/100
* Place Cg close to each VDD10 pin-- 30 (reserve)

For 10/100
* Stuff Cb and Ce only, close to each VDD33 pin-- 23, 32

For GIGA
* Stuff Ca and Cb only, close to each VDD33 pin-- 11, 32



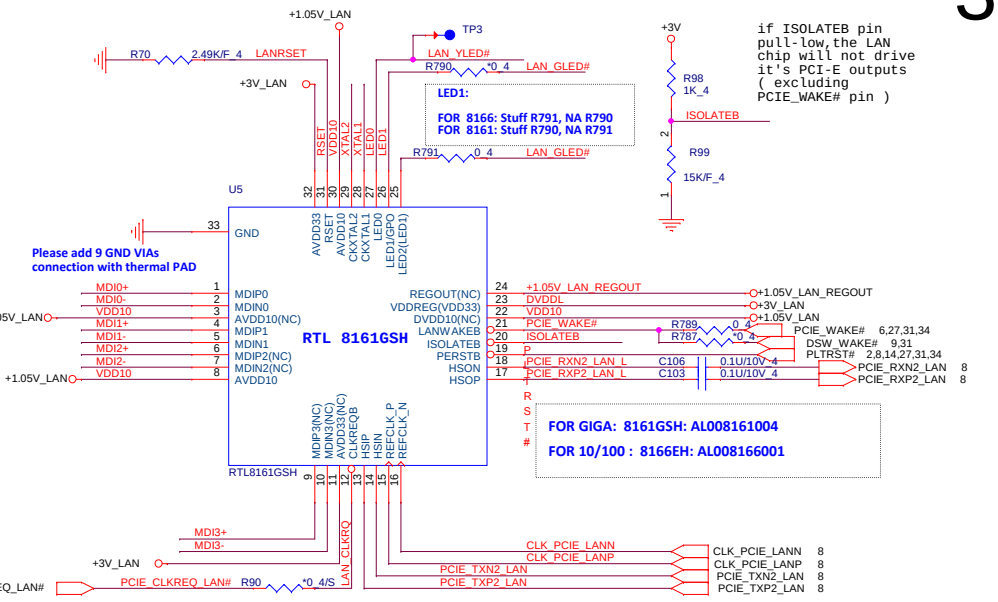
* Place Cc and Cd close to each VDD33 pin-- 23



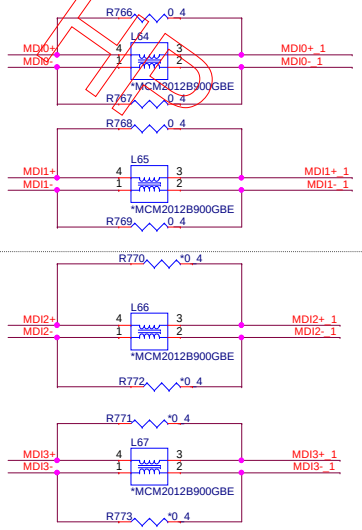
For GIGA
Stuff Cc ,Cd

For 10/100
NA: Cc, Cd

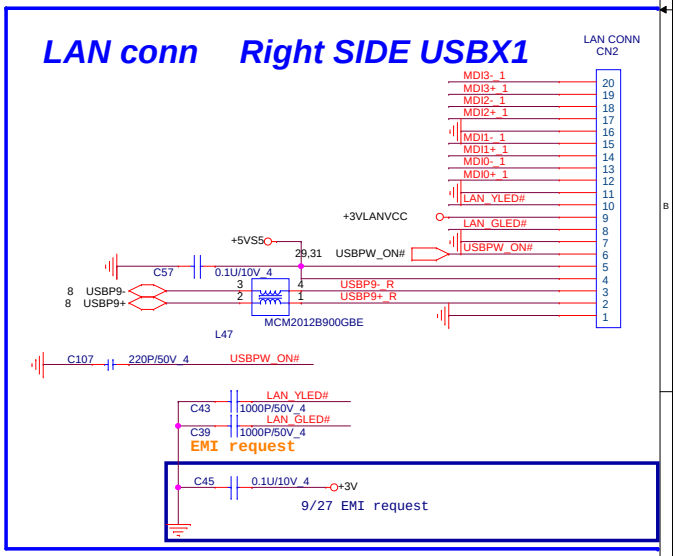
Remove For Not Using SWR mode



For 10/100 only



LAN conn Right SIDE USBX1



For GiGA

BOT:GST5009B LF,DB0Z06LAN00

FCE :NS892407 ,DB0LL1LAN00

For 10/100

BOT: TST1284R LF DB0EL5LAN00

FCE :NS892408 ,DB0EF7LAN01

2,6,7,8,9,10,12,13,14,23,24,25,26,27,28,29,31,32,33,34,39,40,42,44 +3V
11,39 +3VLANVCC

NB5	PROJECT : R63 Quanta Computer Inc.	
Size: Custom	Document Number: RTL 8105E/RJ45	Rev: 1A
Date: Friday, December 21, 2012	Sheet 30 of 44	

adapter Type check

Change to 1SS355 as Current loss

adapter select for EC

Hi ==> DIS/SG

Low ==>UMA

2M byte SPI EC ROM

Socket: DFHS08FS023

EON AKE38ZN0802 EN25QH16-104HIP

AMIC AKE38ZN0Q00 A25LQ16M-F/Q

AKE38ZN0802

SOIC8-8-1_27

PROCHOT control

For +VIN noise

Open Drain need pu high

500mA

for Battery charge/charge and cap board

for CPU thermal

For GPU thermal

For Gsensor

12/12: PV Modify

10/17: SI Modify

10/17: SI Modify

Reserve for ENE timing issue

If use PCH SUSCLK should change to 20P.

12/19: PV add

FOR SG/DIS

10/14: SI add BOM ID

10/14: SI modify

KB3940QF A1

PROJECT : R63

Quanta Computer Inc.

NB5

Size Custom | Document Number EC (KB3940 A1)/ROM | Rev 1A

Date: Friday, December 21, 2012 | Sheet 31 of 44

KEYBOARD Con.

31 MY[0..17] MY[0..17]
31 MX[0..7] MX[0..7]

KB CONN 50698-03201-001-32p-l
DFFC32FR035

MX1 MX7 MX6 MY9 MX4 MX5 MY0 MX2 MX3 MY5 MY1 MX0 MY2 MY4 MY7 MY8 MY6 MY3 MY12 MY13 MY14 MY11 MY10 MY15 MY16 MY17

SATA_LED

C902 *AVLC 5S
7 SATA_LED#
8 ACC_LED#
SATA_LED#
SATA_R_LED1
R734 39_6
+3V
LED2
LED 3P WHITE/AMBER
(Amber)
R733 200/F_6
C899 *AVLC 5S

KEYBOARD PULL-UP

RP2: MY6 MY3 MY12 MY13 → MY15 MY10 MY11 MY14
RP1: MY9 MY0 MY5 MY1 → MY8 MY7 MY4 MY2
+3VPCU
*10P8R-8.2K
R173 *8.2K_4 MY16
R176 *8.2K_4 MY17

MY5 C109 *220P/50V_4
MY6 C142 *220P/50V_4
MY3 C145 *220P/50V_4
MY7 C140 *220P/50V_4
MY8 C141 *220P/50V_4
MY9 C76 *220P/50V_4
MY10 C173 *220P/50V_4
MY11 C169 *220P/50V_4
MY1 C128 *220P/50V_4
MY2 C136 *220P/50V_4
MY4 C139 *220P/50V_4
MY0 C96 *220P/50V_4
MX4 C82 *220P/50V_4
MX6 C73 *220P/50V_4
MX3 C104 *220P/50V_4
MX2 C97 *220P/50V_4
MX7 C67 *220P/50V_4
MX0 C133 *220P/50V_4
MX5 C90 *220P/50V_4
MX1 C61 *220P/50V_4
MY12 C149 *220P/50V_4
MY13 C152 *220P/50V_4
MY14 C156 *220P/50V_4
MY15 C190 *220P/50V_4
MY16 C201 *220P/50V_4
MY17 C206 *220P/50V_4

31 CAPSLED#
R185 200/F_6
R191 200/F_6
+3VPCU
CAPSLED#_R
MUTE_LED_CNTL_R
WIRELESS_ON_R
WIRELESS_OFF_R
+3V
CN6

28 MUTE_LED_CNTL
Q6 2N7002K
R147 10K/F_4
SI, add Mute LED feature

EC KB3930 has included K/B pull-up resistor and function

9/15 SI for H/W.

+5V +3V
R196 1K/F_4
R777 *200/F_6
R195 *200/F_6
Q10 DRC5144E0L
31 WIRELESS_ON
WIRELESS_ON_R

+5V
R199 1K/F_4
R208 *200/F_6
Q9 DRC5144E0L
31 WIRELESS_OFF
WIRELESS_OFF_R

+3VPCU
R440 39_6
LED1
3P WHITE LED
12/20 PV modify
PWR_LED
C601 *AVLC 5S
DEEP_PWRLED#
C607 1000P/50V_4
C604 1000P/50V_4

POWER BOTTON CONNECT

100mA
C116 *4.7U/6.3V_6
C114 1U/10V_4
C113 0.1U/10V_4
+3VPCU
25,31 LID_EC#
31 NBSWON1#
31,32 PWR_LED#
R116 *0_4
DEEP_PWRLED# R117 *0_4/S
CN4
PWR BTN CONN
DFFC06MR001
88513-0601-6P-L-SMT

1. +3VPCU(LIDSWITCH PWR)
2. +3VPCU(LIDSWITCH PWR)
3. LIDSWITCH
4.POWERON#
5. PWRLED#
6. GND

+3VPCU
R120 10K/F_4
C110 PWR_LED# *0.1U/10V_4
C112 LID_EC# 0.1U/10V_4
C111 NBSWON1# 0.1U/10V_4
31,32 PWR_LED#
Q5 DRC5144E0L
C135 0.1U/10V_4
DEEP_PWRLED#
for EC into Deep Sleep in S3 Mode

TOUCH PAD Con.

+3VSUS
R318 4.7K_4 TP_SMB_CLK
R323 4.7K_4 TP_SMB_DATA

change to +3VSUS
close conn

+3VSUS
R304 4.7K_4 TPCLK
R303 4.7K_4 TPDATA

88513-0601-6P-L-SMT
DFFC06MR001
PWR BTN CONN

C429 10P/50V_4
31 TPCLK
31 TPDATA
L34 TB160808B470N001
L33 TB160808B470N001
C428 10P/50V_4
TPCLK-1
TPDATA-1
TP_SMB_DATA
TP_SMB_CLK
CN7

25 mils

+3VSUS C430 0.1U/10V_4

+3VSUS
Q19 *2N7002DW
TP_SMB_CLK
TP_SMB_DATA
SMB_PCH_CLK 8
SMB_PCH_DAT 8

PV , HP request Image sensor
SMBUS reserve to PCH

4,7,9,11,25,31,34,35,36 +3VPCU
7,23,26,28,29,33,34,39 +5V
39 +3VSUS
2,6,7,8,9,10,12,13,14,23,24,25,26,27,28,29,30,31,33,34,39,40,42,44 +3V

NB5

PROJECT : R63
Quanta Computer Inc.

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Custom	LED/KB/SW/TP	1A

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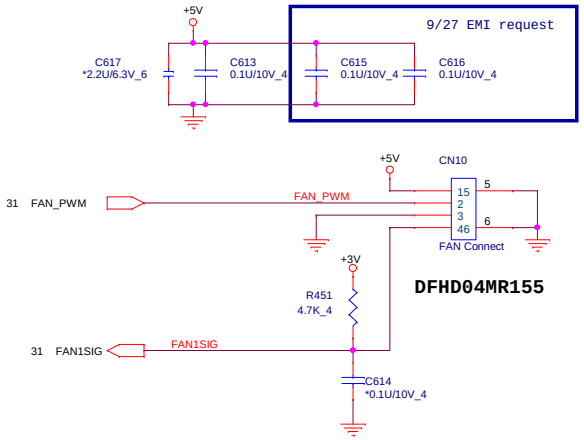
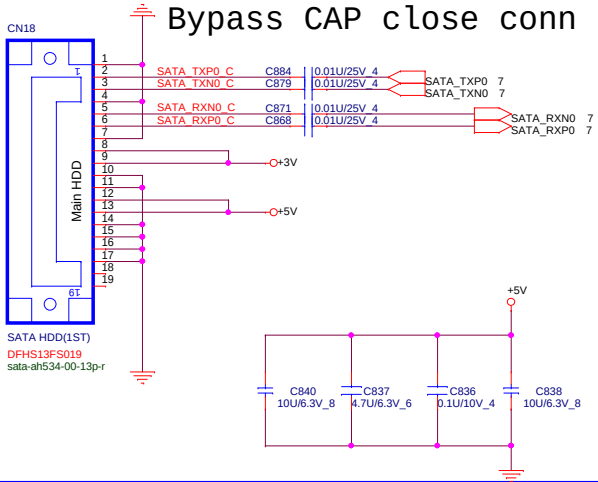
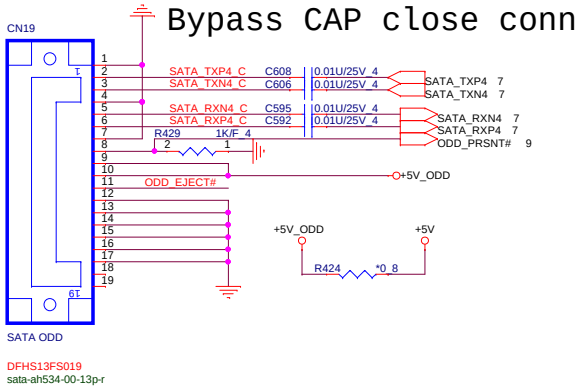
CPU FAN

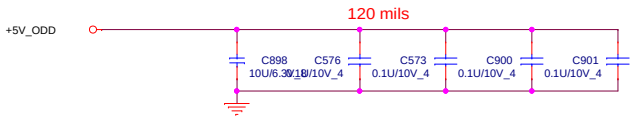


SATA HDD CONNECTOR



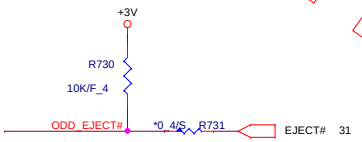
SATA ODD CONNECTOR



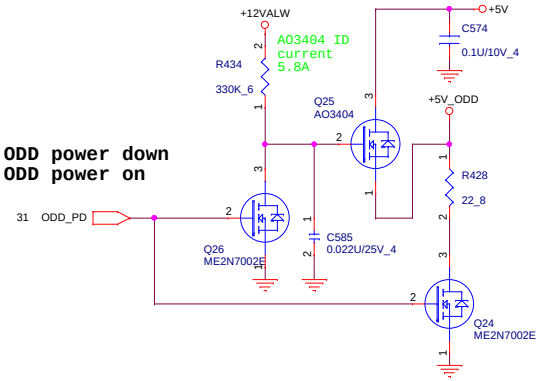


for HP

follow INTEL DG change eject PU to +3V.



High : ODD power down
Low : ODD power on



2,6,7,8,9,10,12,13,14,23,24,25,26,27,28,29,30,31,32,34,39,40,42,44 +3V
4,7,9,11,25,31,32,34,35,36 +3VPCU
7,23,26,28,29,32,34,39 +5V
35,39,44 +12VALW

NB5	PROJECT : R63 Quanta Computer Inc.	
Size: Custom	Document Number: HDD/ODD/FAN	Rev: 1A
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Mini PCI-E Card 1
WLAN

7,9 BT_OFF# D6 MEK500V-40

7/26 DB modify

+3V_AOAC R465 4.7K_4 FOR KBC DEBUG

+5V R463 *0_6 +MINIEC_5V

EC debug pin

31 EC_DEBUG1

CN13

	Reserved	+3.3V	
	Reserved	GND	
	Reserved	+1.5V	
	Reserved	LED_WPAN#	
	Reserved	LED_WLAN#	
	Reserved	LED_WWAN#	
	Reserved	GND	
	Reserved	USB_D+	
	GND	USB_D-	
	PETp0	GND	
	PETn0	SMB_DATA	
	GND	SMB_CLK	
	GND	+1.5V	
	PERp0	GND	
	PERn0	+3.3Vaux	
	GND	PERST#	
	Reserved	W_DISABLE#	
	Reserved	GND	
	GND	Reserved	
	REFCLK+	Reserved	
	REFCLK-	Reserved	
	GND	Reserved	
	CLKREQ#	Reserved	
	BT_CHCLK	+1.5V	
	BT_DATA	GND	
	WAKE#	+3.3V	

MINI PCIE H=11
DFHS52FR097
MIPCI-C-1759513-52P-LDV-SMT

8 PCIE_TXP1 PCIE_TXP1
8 PCIE_TXN1 PCIE_TXN1
8 PCIE_RXP1 PCIE_RXP1
8 PCIE_RXN1 PCIE_RXN1
8 CLK_33M_DEBUG
PLTRST#
8 CLK_PCIE_WLAN CLK_PCIE_WLAN
8 CLK_PCIE_WLAN# CLK_PCIE_WLAN#
8 PCIE_CLKREQ_WLAN# R461 *0_4 BT_COMBO_EN_R#
8 BT_COMBO_EN#
MINICAR_PME#

BT_DATA,BT_CHCLK,CLKREQ#
internal pull-DOWN 100k
ohm

R96 *4.7K_4 +3V_AOAC
R111 0_4 RF_LINK#
MINI_BLED
RF_LINK#
R801 0_4 RF_LINK# 31
R97 4.7K_4 +3V_AOAC
USBP10+ 8
USBP10- 8

10/12: SI reserve
R802 0_4
PLTRST# 2,8,14,27,30,31
RF_OFF# 9

INTEL WLAN
CARD PIN 20
W_DISABLE#
have
internal
pull-up 110k
ohm

LAD0 LAD0 7,31
LAD1 LAD1 7,31
LAD2 LAD2 7,31
LAD3 LAD3 7,31
LFRAME# LFRAME# 7,31

+1.5V
C126 0.01U/16V_4 C129 0.1U/10V_4 C132 10U/6.3VS_6

R473 0_8 +3V
+3V_AOAC
C86 0.1U/10V_4 C632 0.1U/10V_4 C639 0.1U/10V_4 C638 10U/6.3VS_6

+3V_AOAC
*DRC5144E0L Q31
6,27,30,31 PCIE_WAKE# MINICAR_PME#

+3V_AOAC R474 *10K/F_4
*DRC5144E0L Q30
31 EC_PCIE_WAKE#

12/21: PV modify

CLK_33M_DEBUG R84 *51_4 C78 *15P/50V_4

10/14: SI for EMI request

Reserve for AOAC function

+3VPCU +3VS5 +3V_AOAC
R68 *10K/F_4
C935 *0.022U/25V_4
Q28 *ME2303T1
R456 *100K/F_4
24mil
+3V_AOAC
Q27 *ME2N7002E
8 PCH_AOCS# R457 *0_4
31 EC_AOCS# R458 *0_4
C81 *10U/6.3V_8
C87 *.1U/10V_4
Q68 *2N7002E
31,37,38,39 MAINON

6,7,8,10,28,34,38,44 +1.5V
2,6,7,8,9,10,12,13,14,23,24,25,26,27,28,29,30,31,32,33,34,39,40,42,44 +3V
4,7,9,11,25,31,32,35,36 +3VPCU
7,23,26,28,29,32,33,39 +5V
2,6,7,9,10,36,38,39,42,44 +3VS5

Accelerometer Sensor

R245 *0_6/S +3V
R225 *0_6 +3V_AOAC
+G_SEN_PW
U10
HP3DC2TR
C319 0.1U/10V_4 C308 0.1U/10V_4
Vdd_IO VDD NC NC
8 ACCEL_INTH# D10 MEK500V-40 ACCEL_INTH#1 TP22
INT1 INT2 RESERVED RESERVED RESERVED RESERVED
R224 *0_4/S
31 MBDATA3
31 MBCLK3
SDO SDA SCL GND GND CS
+G_SEN_PW R221 *0_4/S
AL003DC2A00

+G_SEN_PW R496 4.7K_4 R497 4.7K_4
ACCEL_INTH#1 MBDATA3 C323 33P/50V_4
MBCLK3 C322 *33P/50V_4
C288 22P/50V_4

9/27 EMI request

+3VS5 +3V
C524 0.1U/10V_4 C640 0.1U/10V_4 C522 0.1U/10V_4 C641 0.1U/10V_4
C625 0.1U/10V_4 C83 0.1U/10V_4 C84 0.1U/10V_4 C630 0.1U/10V_4 C626 0.1U/10V_4 C527 0.1U/10V_4 C636 0.1U/10V_4 C637 0.1U/10V_4 C627 0.1U/10V_4 C629 0.1U/10V_4

SI for +VIN noise issue

+5VS5
EC4 EC2 EC3 EC5 0.01U/50V_4 +VIN
+3V
EC18 EC1 EC13 0.01U/50V_4 +VIN

10.14: SI modify.

EC23 EC24 EC25 EC26 *0.01U/25V_4
EC27 220P/50V_4
EC28 *0.1U/25V_4
EC29 *0.1U/25V_4
+3VPCU C446 *0.1U/10V_4
+5V C49 0.1U/10V_4 C48 0.1U/10V_4
+5VS5 C475 0.1U/10V_4 C480 0.1U/10V_4
+VGA_CORE C406 0.1U/10V_4

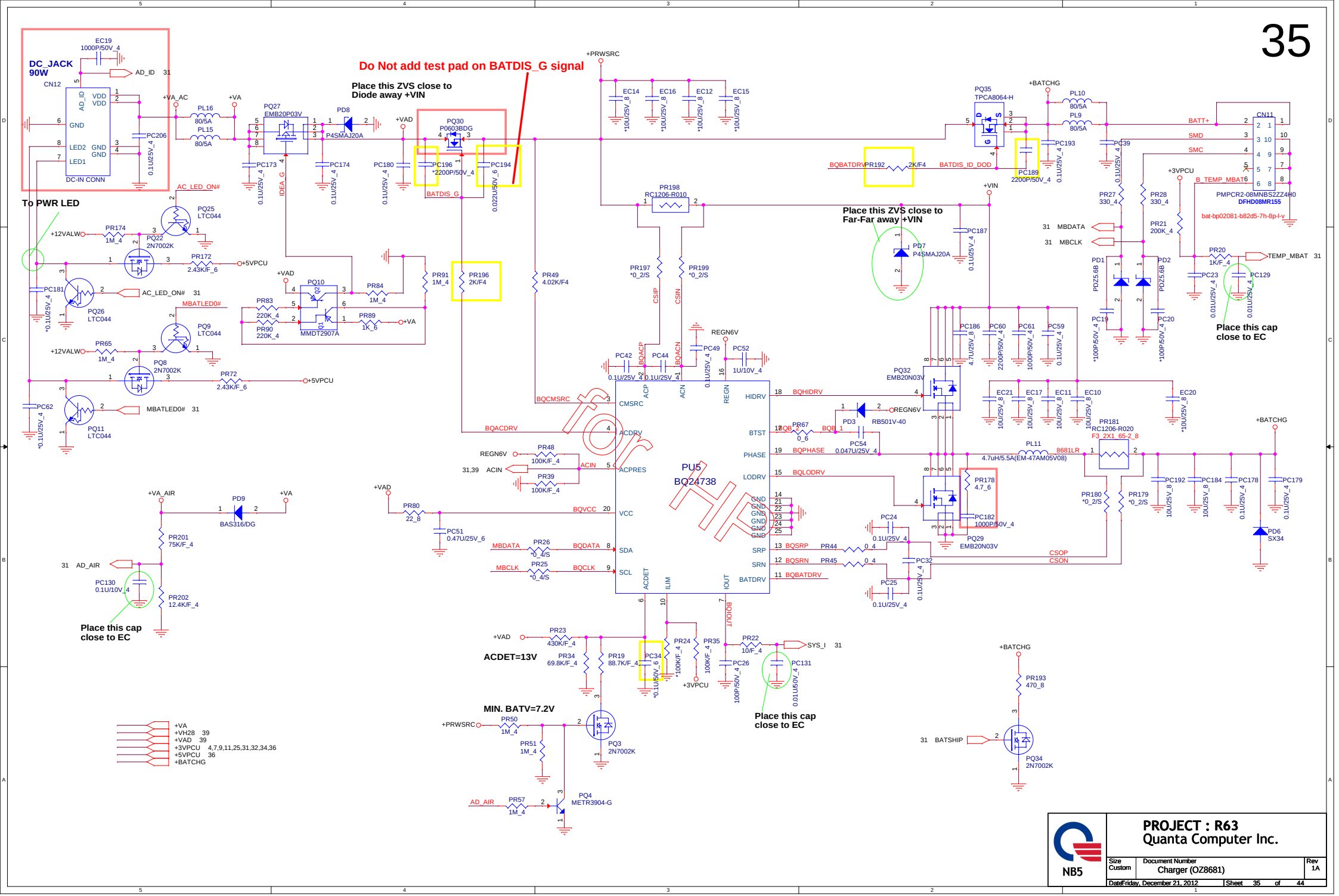
+5V EC7 0.01U/50V_4 +3V
+3V EC22 0.01U/50V_4 +1.5V_VGA
+5V EC6 0.01U/50V_4 +5VS5
+1.05V EC9 0.01U/50V_4 +5VS5
+3V EC8 0.01U/50V_4 +1.05V

2,6,7,8,9,10,12,13,14,23,24,25,26,27,28,29,30,31,32,33,34,39,40,42,44 +3V
32,39 +3VSUS
6,7,8,10,28,34,38,44 +1.5V
23,29,30,36,37,38,39,40,41,42,43,44 +5VS5

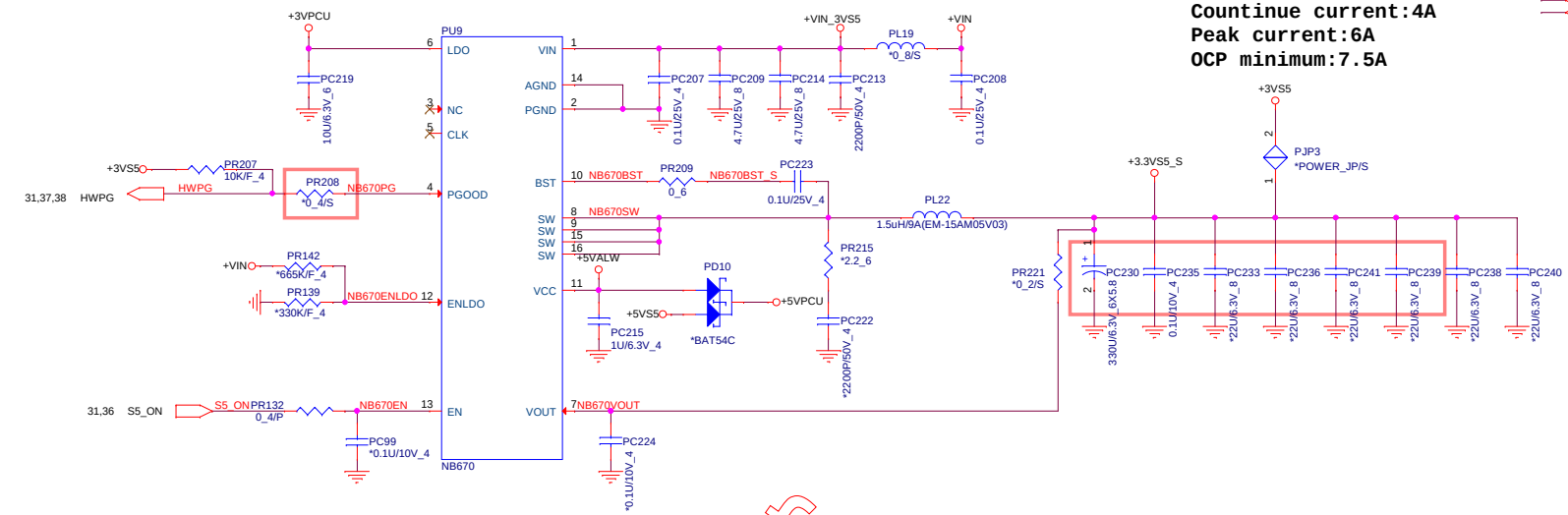
NB5

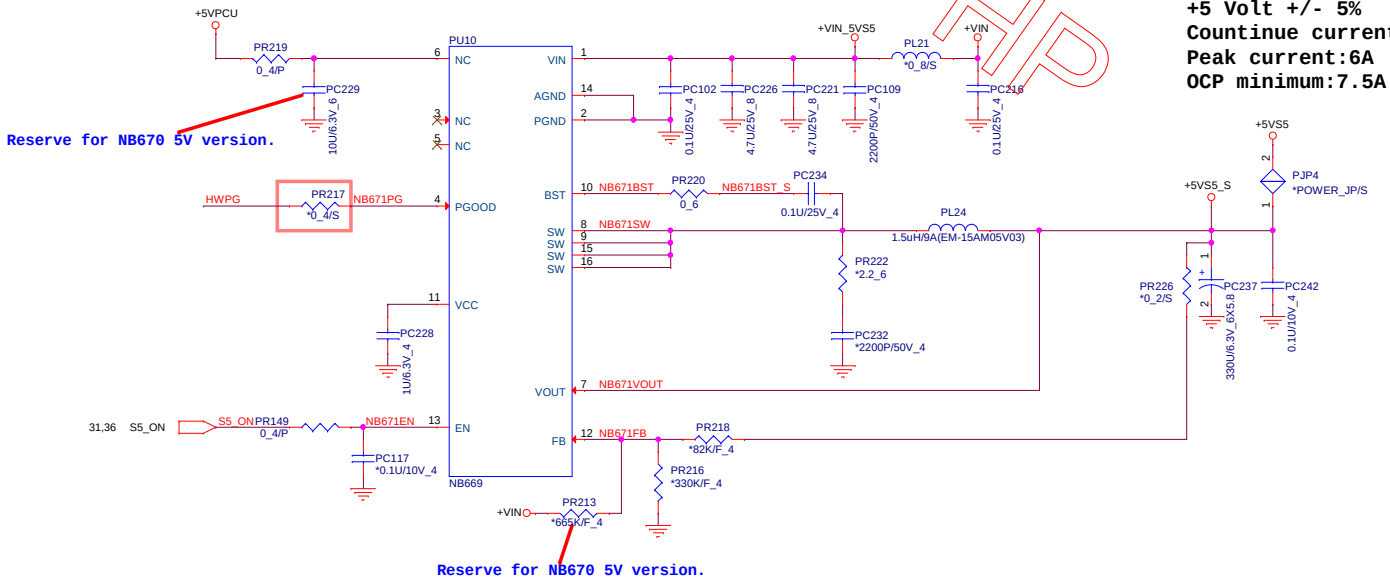
PROJECT : R63
Quanta Computer Inc.

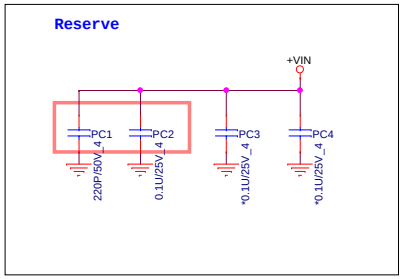
Size	Document Number	Rev
Custom	MINI PCIE CONN & G-sensor	1A
Date: Friday, December 21, 2012	Sheet 34 of 44	



PROJECT : R63	
Quanta Computer Inc.	
NB5	Size: Custom; Document Number: Charger (OZ8681); Rev: 1A
Date: Friday, December 21, 2012	Sheet 35 of 44





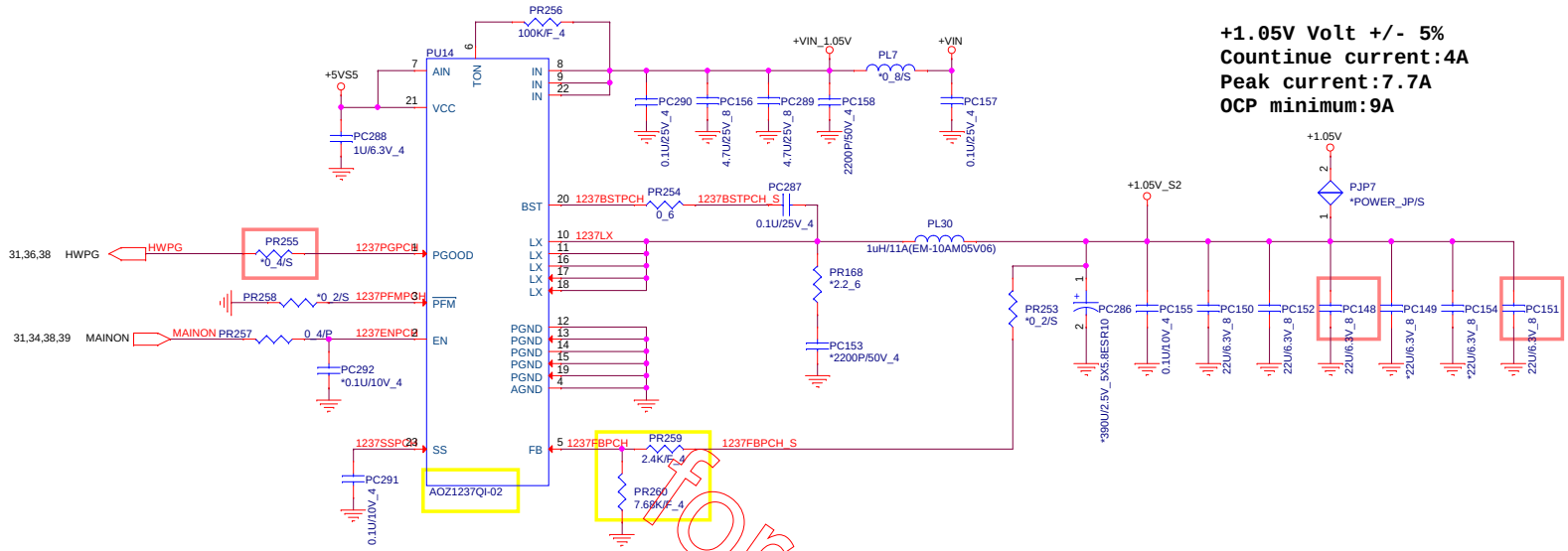


NB5

PROJECT : R63
Quanta Computer Inc.

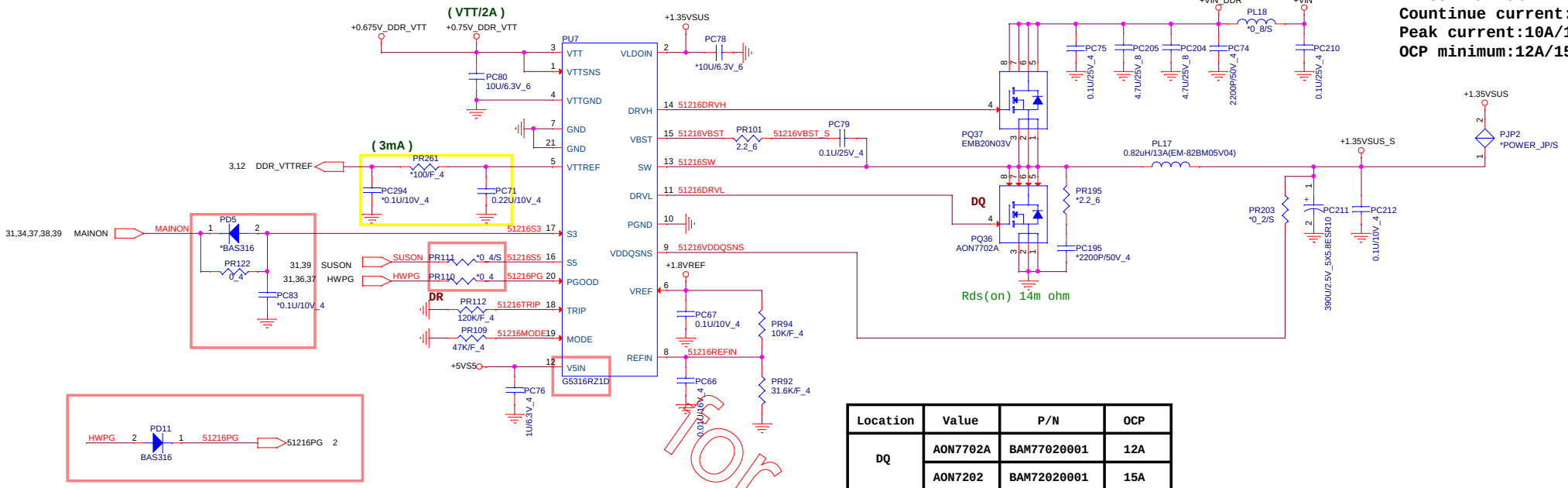
Size	Document Number	Rev
Custom	3/5VPCU(RT8243A)	1A

Date: Friday, December 21, 2012 Sheet 36 of 44



+1.35VSUS 2,3,4,12,13
+1.5V 6,7,8,10,28,34,44

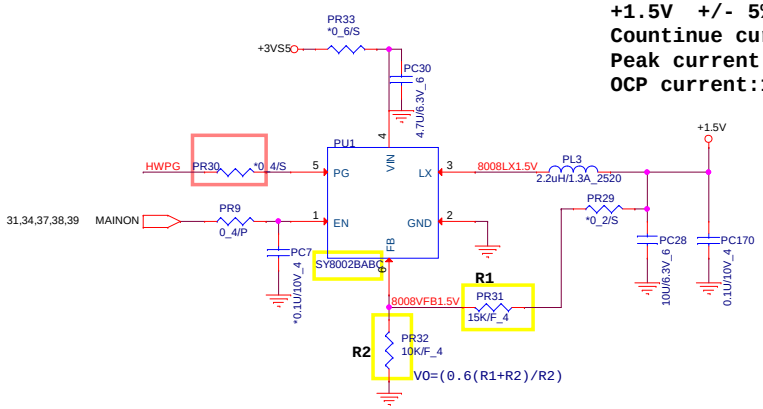
+1.35V +/- 5%
Countinue current:6A/8A
Peak current:10A/12A
OCP minimum:12A/15A



Location	Value	P/N	OCP
DQ	AON7702A	BAM77020001	12A
	AON7202	BAM72020001	15A

Location	Value	P/N	OCP
DR	120K	CS41202FB17	12A
	76.8K	CS37682FB00	15A

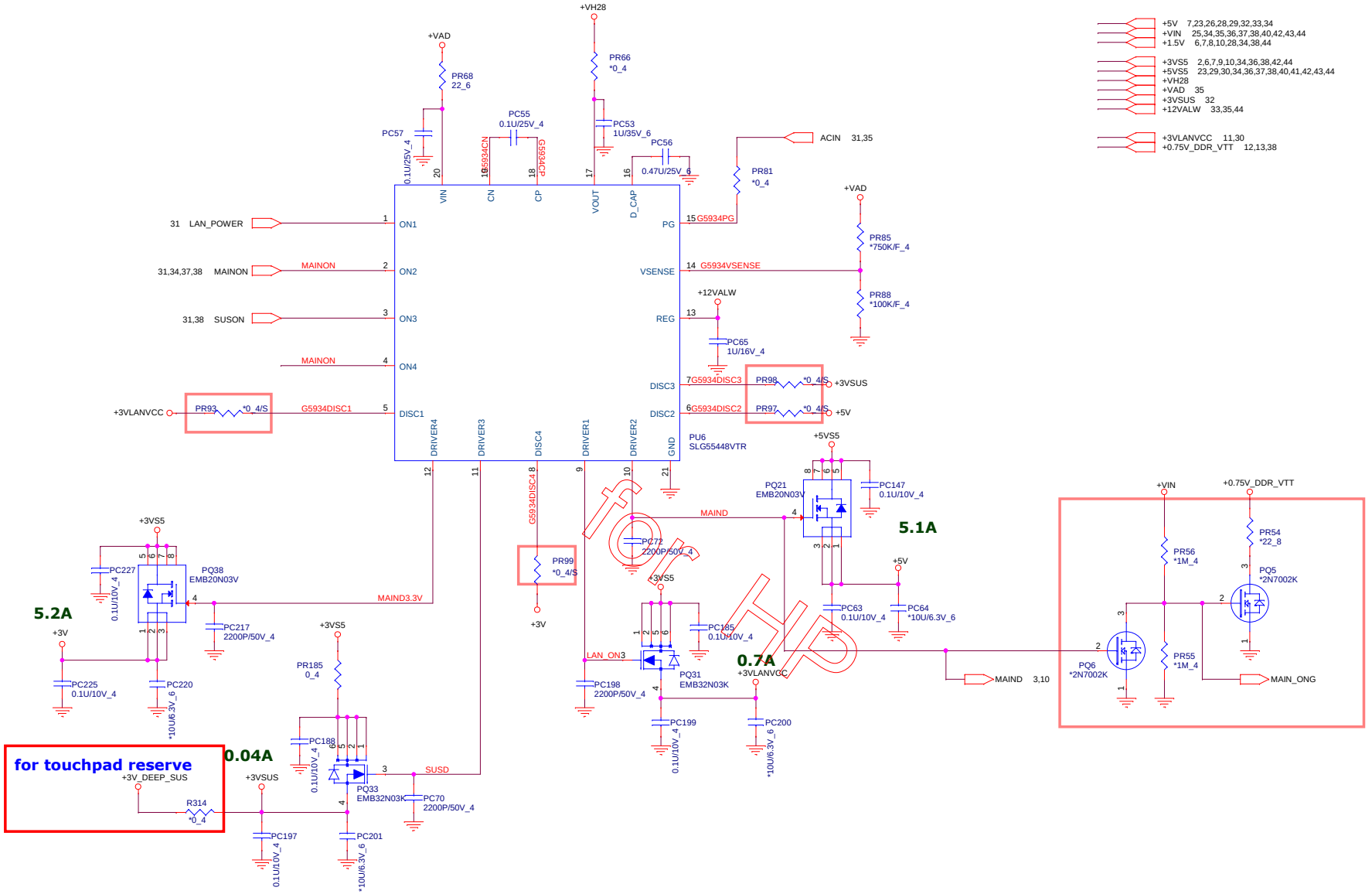
+1.5V +/- 5%
Countinue current:0.3A
Peak current:0.75A
OCP current:1.2A



NB5

PROJECT : R63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3L(APW8819)	1A
Date: Friday, December 21, 2012	Sheet 38 of 44	



PROJECT : R63	
Quanta Computer Inc.	
NB5	
Size: Custom	Document Number: Dis-charge IC (G5934)
Rev: 1A	
Date: Friday, December 21, 2012	Sheet 39 of 44

CPU	Re	PR18
37W	9.09K	CS29092FB27
47W	14.7K	CS31472FB14

PUT COLSE TO VCORE Phase 1 Inductor

Dummy Rc For 2 phase

Rc
PR8 *147K/F_6 SWN2
PR3 147K/F_6 SWN3
PR12 147K/F_6 SWN1

CPU	Rd	PR14
37W	43.2K	CS34322FB00
47W	66.5K	CS36652FB16

Dummy Ra and Ca For 2 phase

Ca PC6 *0.047U/25V_4 PR7 *20K/F_4 CSREF
Ra PR10 *5.11K/F_4 CSP2 SWN2 40,41
PC5 0.047U/25V_4 PR2 *20K/F_4 CSREF CSP3 PR1 5.11K/F_4 SWN3 40
PC13 0.047U/25V_4 PR11 *20K/F_4 CSREF CSP1 PR13 5.11K/F_4 SWN1 40

Rb PR4 0_4 +5VS5 CSP2

POP Rb for 2 phase

+VCC_CORE 4,41

PR191 220K_6 NTC PR5 75K/F_4 PR6 165K/F_4 81103GND
PC10 1200P/50V_4 PC17 1000P/50V_4 CSREF CSREF 40,41
PC14 *330P/50V_4 CSP3 CSP2 CSP1 CSSUM
CSCOMP DRON 41 81103_PWM 41
Re PR18 9.09K/F_4
Rd PR14 43.2K/F_4
81103HG3 PR173 1_6 81103HG3_G

+VCCIO_OUT PR76 130/F_4 PR77 *75/F_4 PR78 54.9/F_4 PC58 0.1U/10V_4 SDIO ALERT# SCLK
+VIN_VCC_CORE PR36 1K/F_4 PC29 0.01U/50V_4 81103GND
PR52 49.9/F_4 PC40 330P/50V_4 PC38 10P/50V_4 PR47 1K/F_4 PR43 5.9K/F_4
PR17 22.1K/F_4 PC22 470P/50V_4 81103GND

PU4 NCP81103
81103ILIM 81103IOUT 81103VRAMP 81103COMP 81103FB 81103DIFFOUT 81103VSN 81103VSP 81103VCC
ILIM IOUT VRMP COMP FB DIFFOUT VSN VSP VCC GND
CSCOMP CSSUM CSREF CSP3 CSP2 CSP1 DRON PWM2/IMAX HG3
BST3 SW3 LG3 PGND HG1 BST1 SW1 LG1 PVCC
PC18 0.22U/25V_6 PC41 0.22U/25V_6
81103SW3 81103LG3 81103HG1 81103SW1 81103LG1
EN VRHOT# SDIO ALERT# SCLK VR_RDY ROSC 81103RGSC TSENSE VBOOT 81103SEN VR_HOT# SDIO ALERT# SCLK VR_RDY 81103RGSC TSENSE VBOOT

4 VSS_SENSE
4 VCC_SENSE
PR70 0_4 PR53 1K/F_4 PR43 2200P/50V_4 PC48 1000P/50V_4 PR71 0_4
+5VS5 PR74 2_2_6 PC47 2.2U/6.3V_6 81103GND
PR170 *0_4/S
PC35 2.2U/6.3V_6 +5VS5
PR73 45.3K/F_4 81103GND
PC50 0.1U/10V_4 81103GND
PR64 25.5K/F_4 81103GND

31 VRON
+VCCIO_OUT PR75 *75/F_4
2,31 H_PROCHOT# PR60 *0_4/S
4 VR_SVID_DATA PR61 *0_4/S
4 VR_SVID_ALERT# PR62 *0_4/S
4 VR_SVID_CLK PR63 *0_4/S
6 IMVP_PWRGD PR58 *0_4/S
+3V PR79 10K/F_4
PR59 *0_4/S

TSENSE PR189 0_4/P PR194 8.25K/F_4 PR190 TH05-3L104FR

PUT COLSE TO VCORE HOT SPOT

PQ23 RJK03P3 PQ1 *RJK03S3 PQ28 RJK03P3 PQ7 *RJK03S3
81103HG3_G 81103SW3 81103LG3 81103HG1_G 81103SW1 81103LG1
PR82 1_6
PR177 4.7_6 PC175 1000P/50V_4 PR176 4.7_6 PC172 1000P/50V_4

+VIN_VCC_CORE PC165 PC15 PC166 4.7U/25V_8
PC160 0.1U/25V_4 PC161 2200P/50V_4 PL1 *0_8/S PL2 *0_8/S PC202 470U/25V_EC_10H PC9 0.1U/25V_4 +VIN
PL12 0.24uH/24A_7X7X4
PR186 *0_2/S PR86 10/F_4 CSREF
PR182 *0_2/S SWN3 40

+VIN_VCC_CORE PC46 PC183 PC45 4.7U/25V_8
PC176 0.1U/25V_4 PC177 2200P/50V_4
PL14 0.24uH/24A_7X7X4
+VCC_CORE PC203 PC190 PC191 PC68 PC128
*390U/2.5V_5X5.8ESR10 *330U/2.5V_6X4.5ESR12 *330U/2.5V_6X4.5ESR12 *330u_2.5V_7343 3300u_2V_7343
PR188 *0_2/S PR87 10/F_4 CSREF CSREF 40,41
PR184 *0_2/S SWN1 40

SV 37W CPU
VID1=1.8V
IccMax=55A
Icc_Dyn=35A
Icc_TDC=26A
R_LL=1.5m ohm
OCP~60A

For 37W CPU ; PC128 Placed 330uF_9 mohm
For 47W CPU ; PC128 Placed 560uF_4.5 mohm

CPU	PC128
37W	CH733RY8802
47W	CH756RM8802

CPU	Ra	Ca	Rb	Rc	Rd	Re		
37W	Dummy	Dummy	POP	Dummy	CS34322FB00	CS29092FB27	CH733RY8802	Dummy Page 41
47W	POP	POP	Dummy	POP	CS36652FB16	CS31472FB14	CH756RM8802	POP Page 41
R63 Location	PR10	PC6	PR4	PR8	PR14	PR18	PC128	

NB5

PROJECT : R63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPUCORE (NCP81103)	1A

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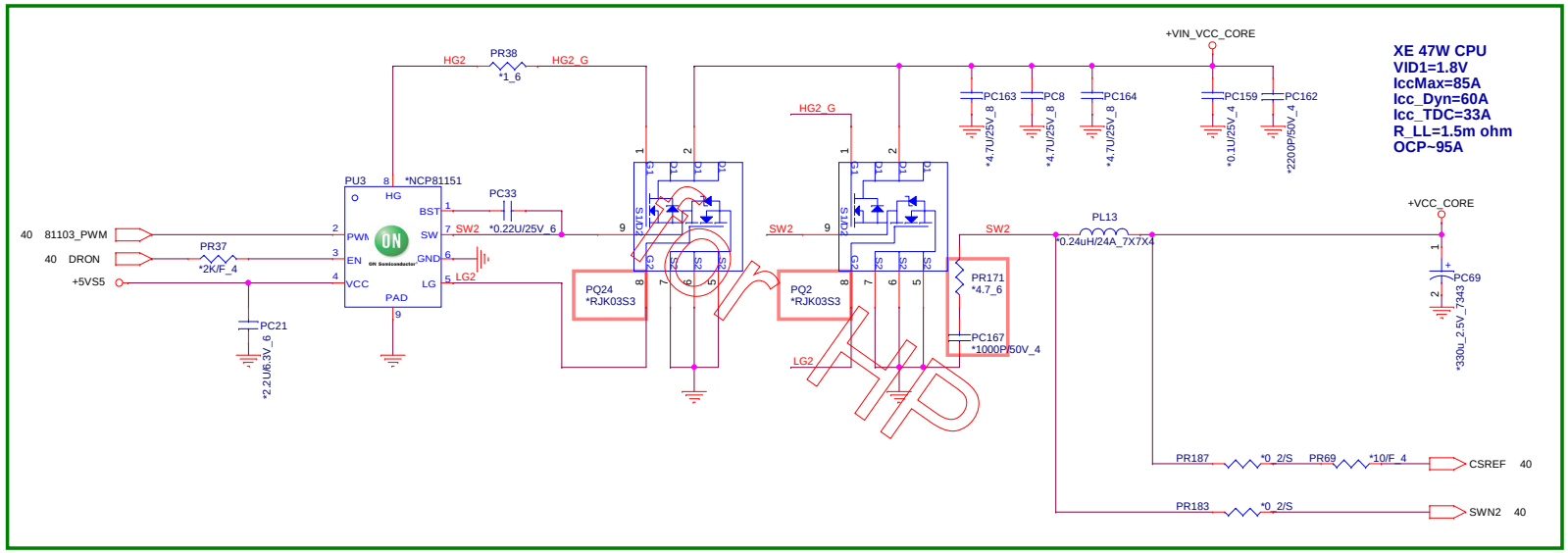

For 37W CPU
Dummy these components

+VCC_CORE 4,40

NB5

PROJECT : R63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NCP81151	1A

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VGA Core

GPIO10 GPIO12 GPIO16 GPIO20 GPIO15 Mars XT

PWRCNTL5	PWRCNTL4	PWRCNTL3	PWRCNTL2	PWRCNTL1	V-CORE
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V

Default

GPIO12 GPIO16 GPIO15 Thames XT

PWRCNTL4	PWRCNTL3	PWRCNTL1	V-CORE
0	1	0	1.0V
1	0	0	0.9V
1	0	1	0.875V

Default

+VGA_CORE 18,34,44

42

Mars (25W)

+VGA_CORE
Countinue current: 25A
Peak current: 30A
OCP minimum: 33A
L-L=0mV/A

DCR_1.4m ohm

DCR_1.4m ohm

PU8
NCP3218G

This NTC Close to Phase 1 MOSFET

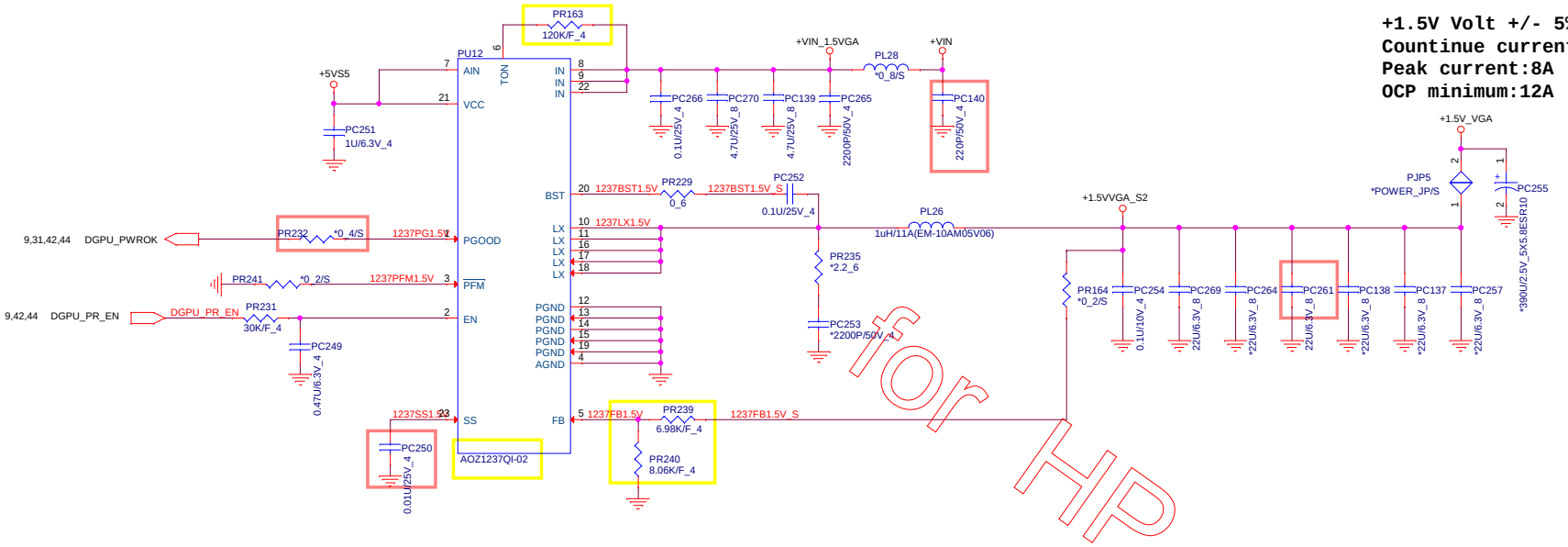
Close to Phase 1 Inductor

Shortest the net trace

PROJECT : R63
Quanta Computer Inc.

NB5

Size: Custom | Document Number: +VGACORE NCP3218G) | Rev: 1A
Date: Friday, December 21, 2012 | Sheet 42 of 44



NB5

PROJECT : R63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VGA POWER	A
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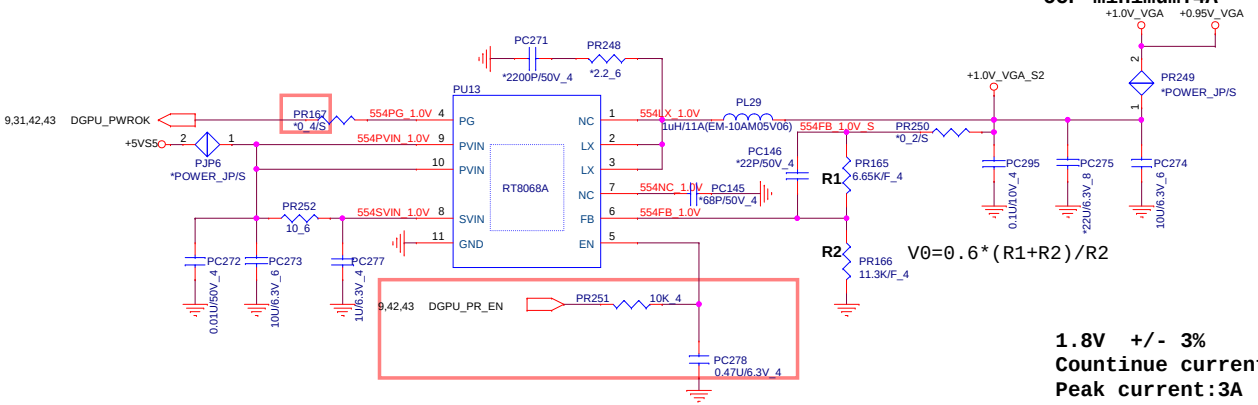
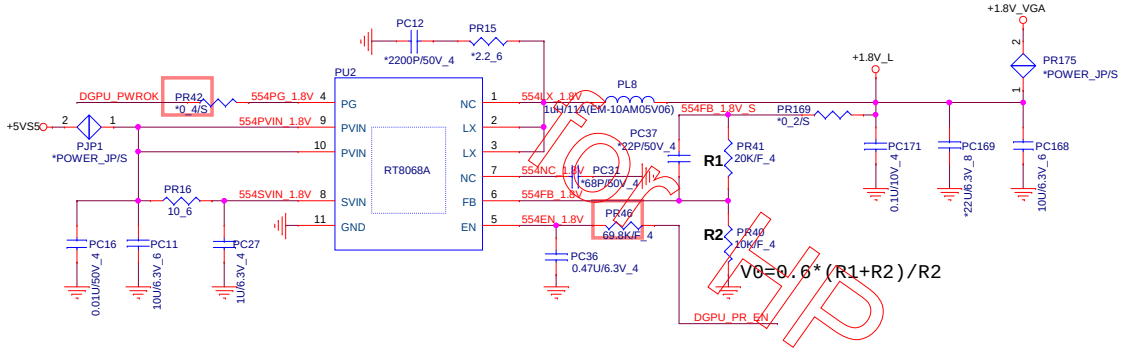
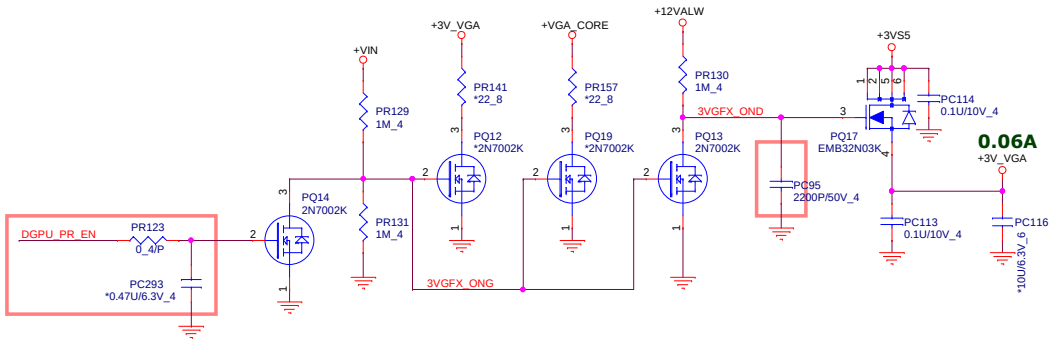
VGA TYPE	R2 Value	P/N	1.0V_VGA
Thems	10K	CS31002FB26	1.0V
MARS	11.3K	CS31132FB07	0.95V

+0.95V +/- 3%
Countinue current:2A
Peak current:3A
OCP minimum:4A

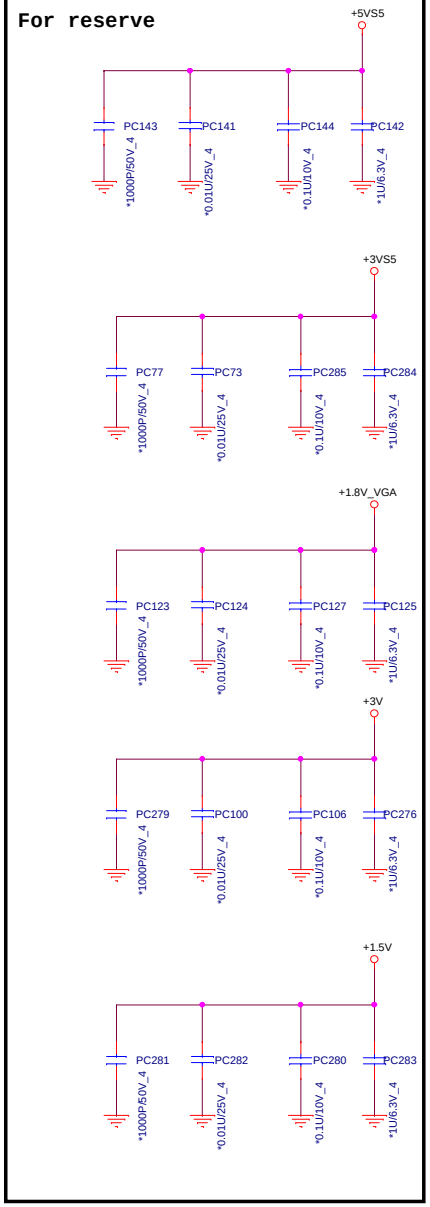


1.8V +/- 3%
Countinue current:2A
Peak current:3A
OCP minimum:4A





For reserve



+1.8V_VGA 11,15,16,18,19
+1.0V_VGA 14,16,18,19
+3V_VGA 14,18

NB5

PROJECT : R63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VGACORE (RT8208/1.8V)	1A

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