DJ1 Calpella UMA Schematics Document

Arrandale

Intel PCH

2010-04-23

REV : X01

DY : Nopop Component

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Cover Page	
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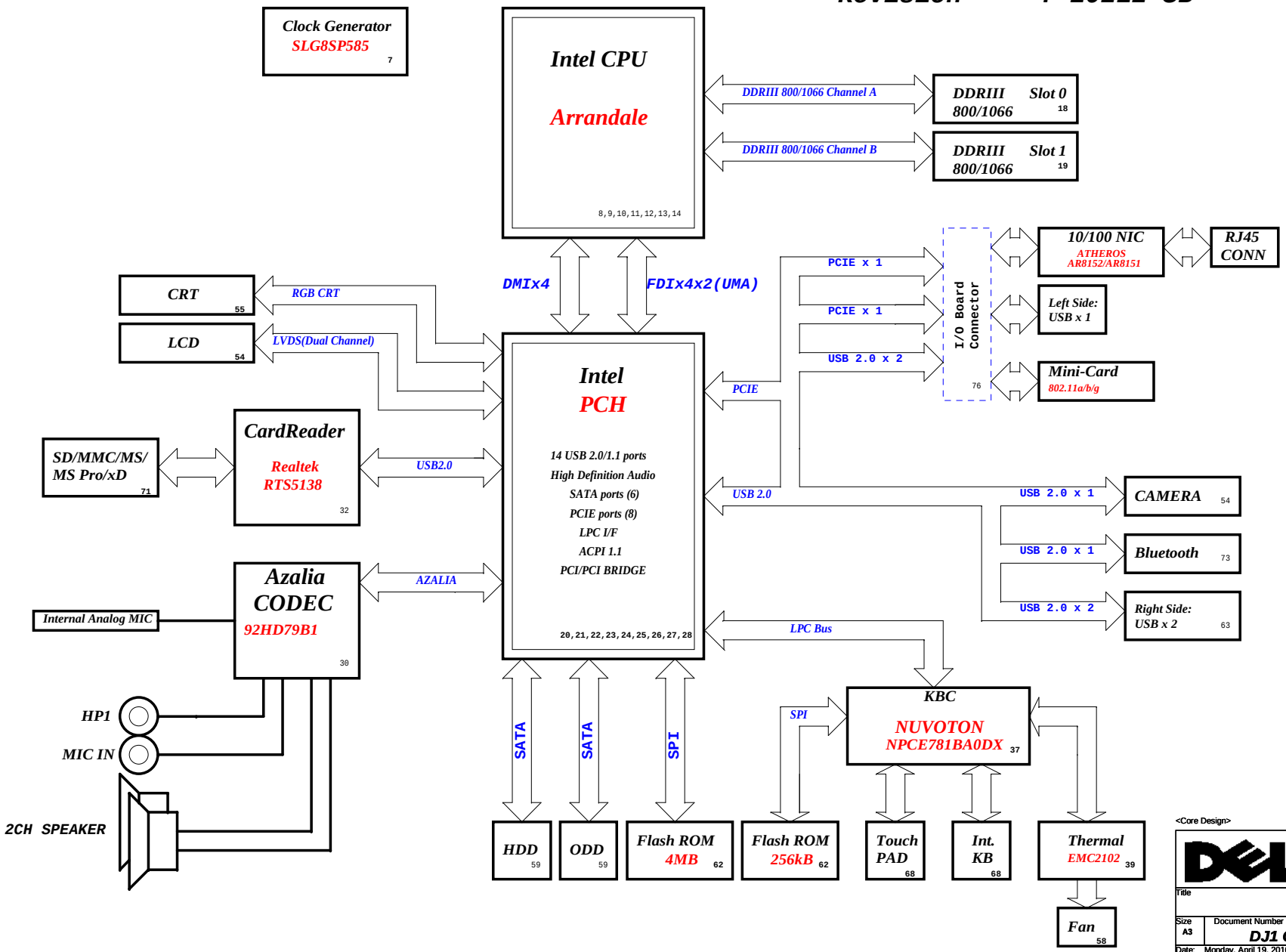
DJ1 UMA Block Diagram

Project code : 91.4EK01.001
PCB P/N : 48.4EK19.0SB
Revision : 10212-SB



CPU DC/DC ISL62882 47,48	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

SYSTEM DC/DC TPS51218 49	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VTT

SYSTEM DC/DC RT8205BGQW 46	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +5V_ALW +3.3V_ALW +15V_ALW

SYSTEM DC/DC RT8207GQW 50	
INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS +0.75V_DDR_VTT +V_DDR_REF

SYSTEM DC/DC TPS51611 53	
INPUTS	OUTPUTS
+PWR_SRC	+CPU_GFX_CORE

MAXIM CHARGER BQ24745	
INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC

SYSTEM DC/DC APL5930 51	
INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN

SYSTEM DC/DC Switches 42	
INPUTS	OUTPUTS
+1.5V_SUS +5V_ALW +3.3V_ALW	+1.5V_RUN +5V_RUN +3.3V_RUN

PCB LAYER

L1: Top
L2: VCC
L3: Signal
L4: Signal
L5 GND
L6: Bottom

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Title: Block Diagram

Size: A3 | Document Number: DJ1 Calpella UMA | Rev: X01

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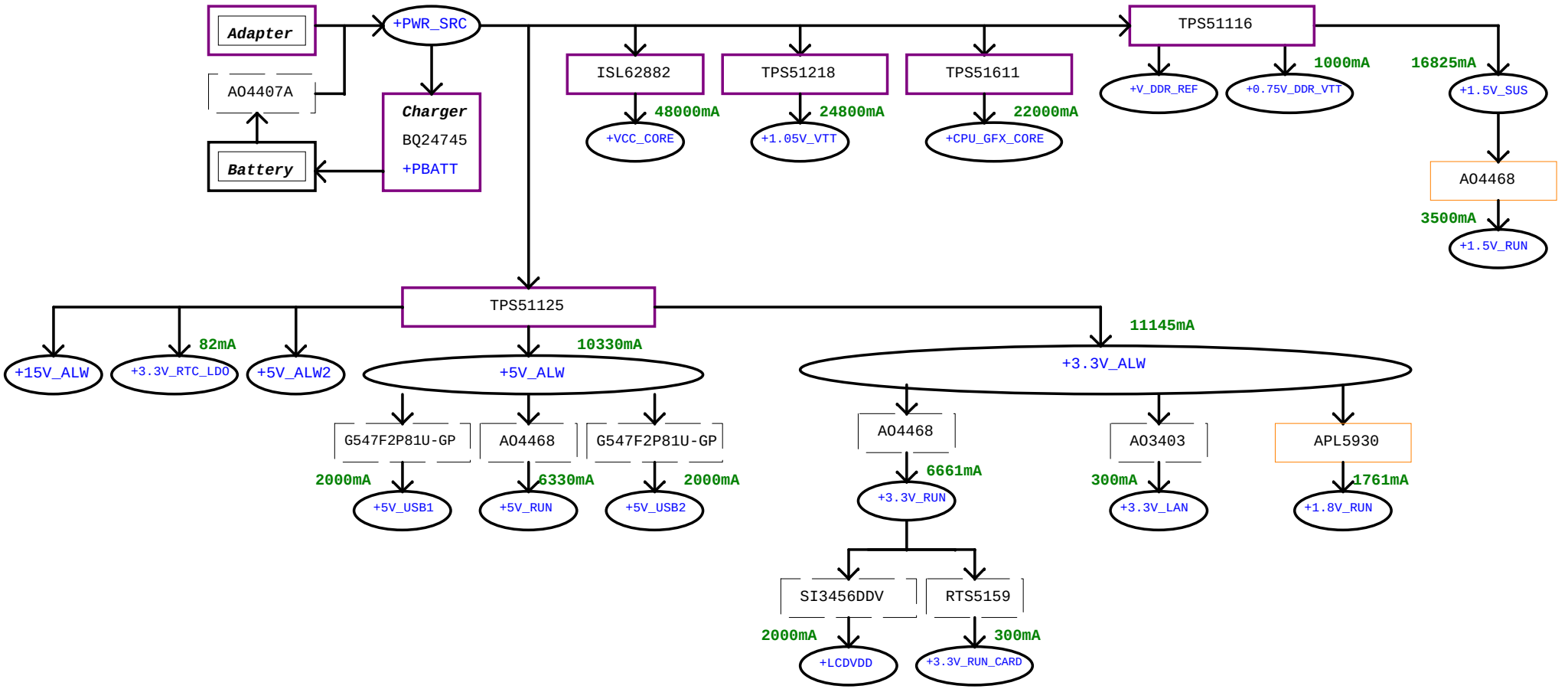

<Core Design>

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Title: Power Block Diagram

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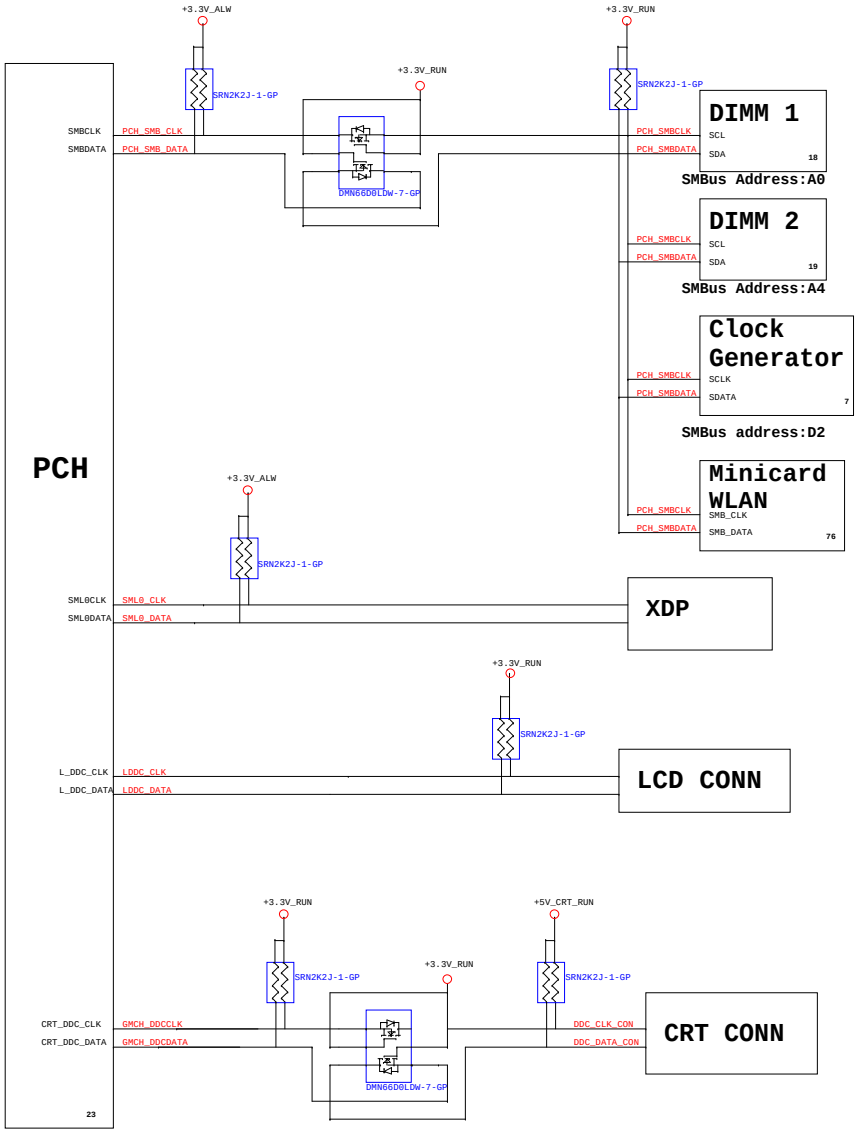
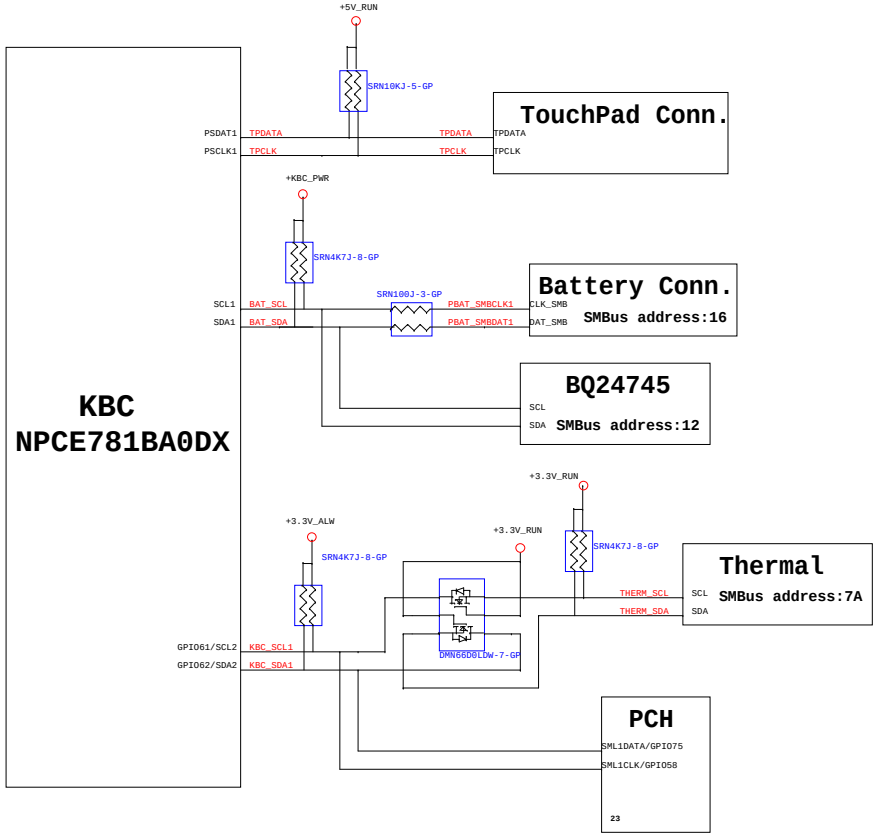
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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DELL Wistron Corporation
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Title: SMBUS Block Diagram

Size	Document Number	Rev
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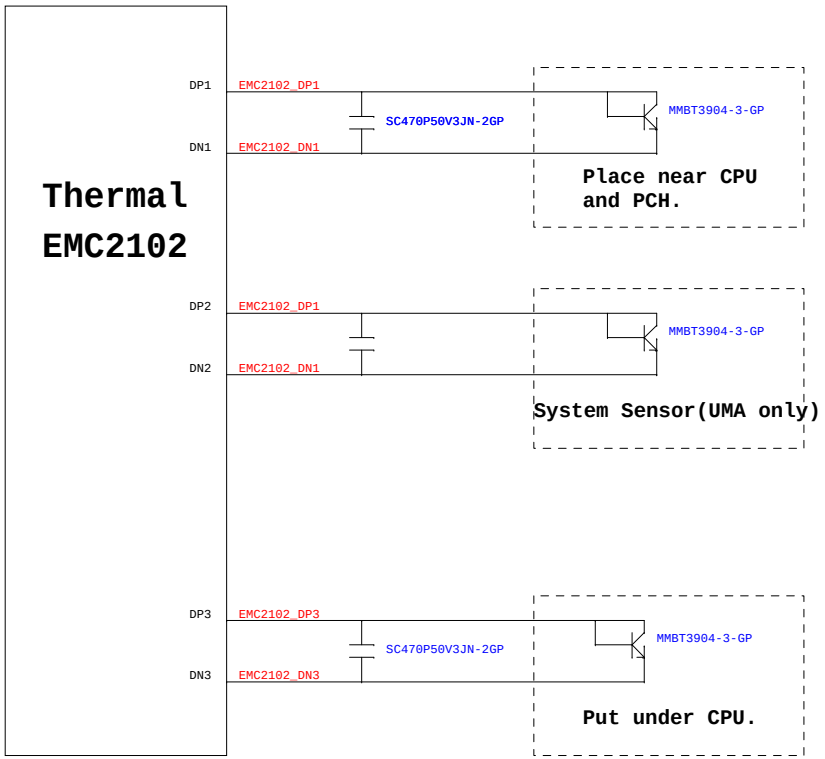
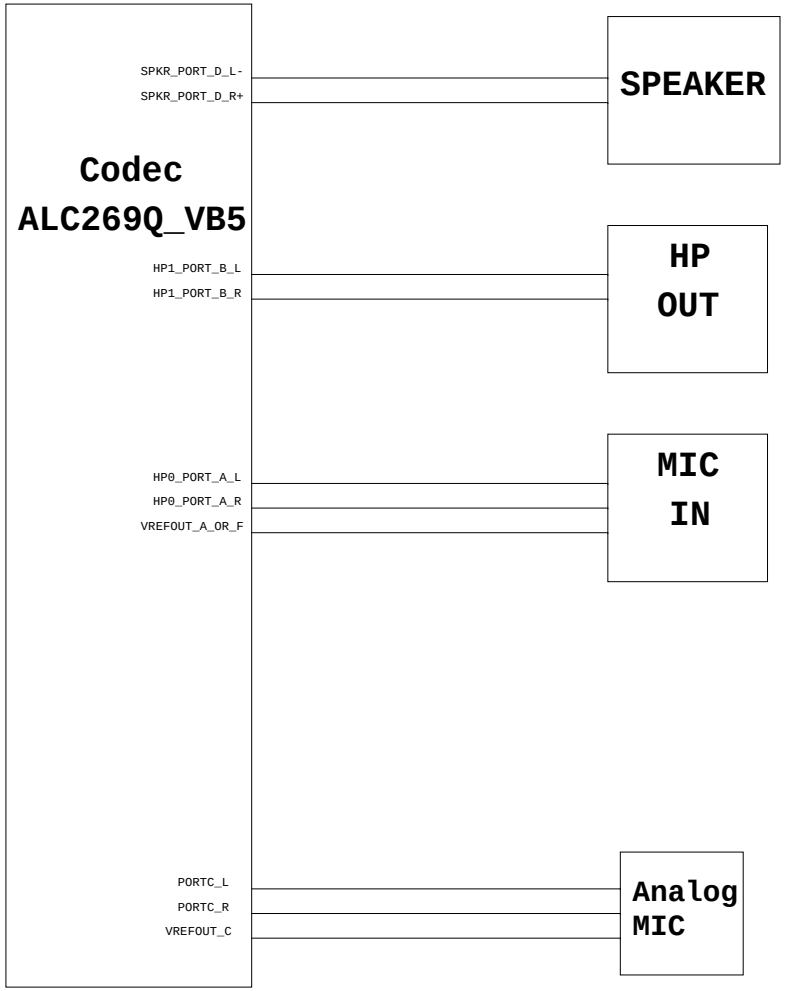
Thermal Block Diagram



Audio Block Diagram



<Core Design>

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Title: Thermal/Audio Block Diagram

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PCH Strapping

Calpella Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-k- 10-k weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-k weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#/GPIO51	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-k pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-k pull-down resistor.
GNT2#/ GPIO53	**Default - Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-k pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-k weak pull- up resistor. **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-k weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Calpella Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connected to the Embedded Display Port.	**1**
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	**1**
CFG[7]	**Reserved - Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** - Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	**0**

PCIE Routing

LANE2	MiniCard WLAN
LANE3	LAN

USB Table

USB	
Pair	Device
0	USB0 (I/O Board)
1	X
2	USB2
3	USB3
4	X
5	WLAN (I/O Board)
6	X
7	X
8	X
9	BLUETOOTH
10	CARD READER
11	CAMERA
12	X
13	X

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Title: *Table of Content*

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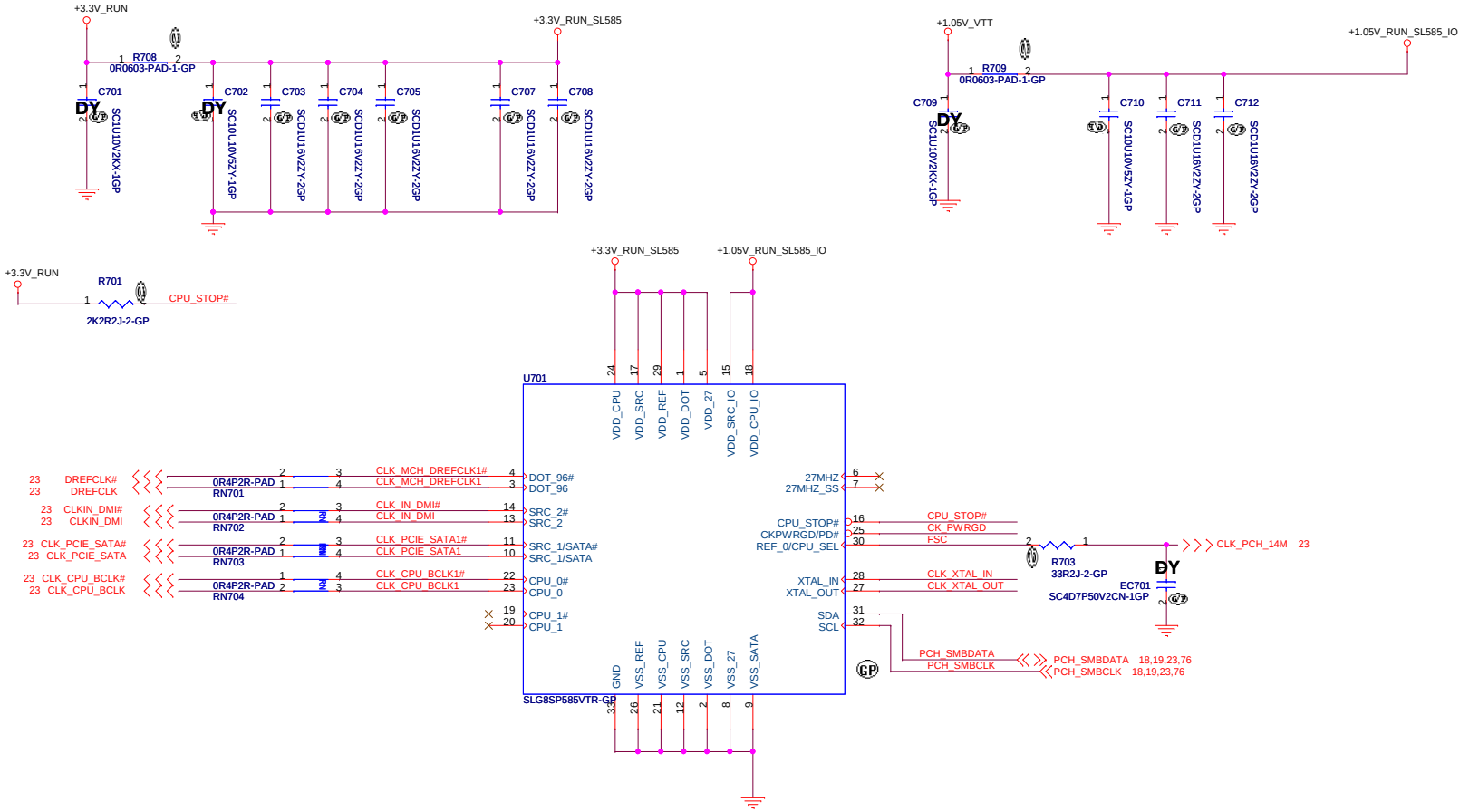
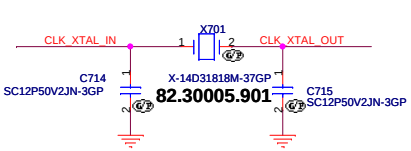
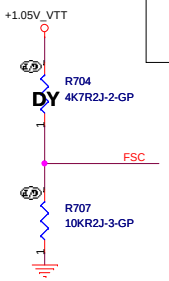
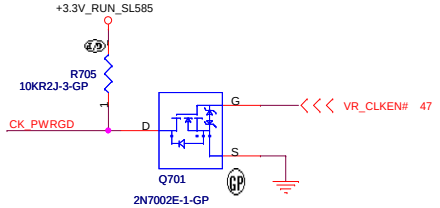
SSID = CLOCK



FSC	0	1
SPEED	133MHz (Default)	100MHz







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Title: *Clock Generator SLG8SP585*

Size | Document Number: *DJ1 Calpella UMA* | Rev: *X01*

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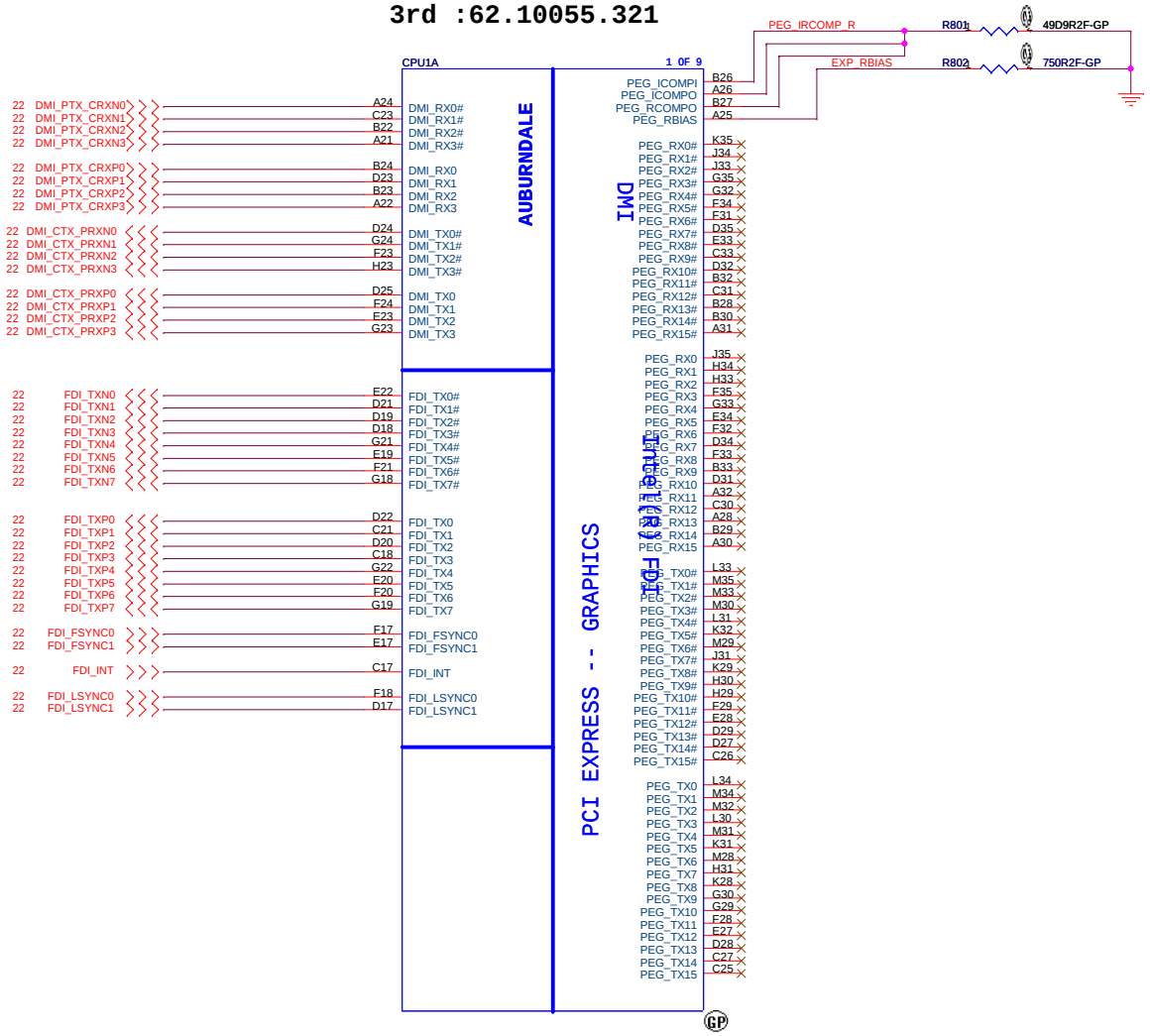
SSID = CPU

Main:62.10053.601
2nd :62.10040.611
3rd :62.10055.321



<Core Design>

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Title: CPU (PCIE/DMI/FDI)

Size | Document Number: DJ1 Calpella UMA | Rev: X01

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SSID = CPU

Processor Pullups

+1.05V_VTT

R902 1 49D9R2F-GP H_CATERR#
R933 1 68R2-GP H_PROCHOT#
R904 1 DY 68R2-GP H_CPURST#

Processor Compensation Signals

R901 1 20R2F-GP H_COMP3
R903 1 20R2F-GP H_COMP2
R905 1 49D9R2F-GP H_COMP1
R906 1 49D9R2F-GP H_COMP0
TPAD14-GP TP901 1 SKTOCC#_R

CPU1B

COMP3	AT23	H_COMP3
COMP2	AT24	H_COMP2
COMP1	G16	H_COMP1
COMP0	AT26	H_COMP0
SKTOCC#	AH24	SKTOCC#_R
CATERR#	AK14	H_CATERR#
PECI	AT15	25 H_PECI
PROCHOT#	AN26	47 H_PROCHOT#
THERMTRIP#	AK15	25,37,42 H_THERMTRIP#
RESET_OBS#	AP26	H_CPURST#
PM_SYNC	AL15	22 H_PM_SYNC
VCCPWRGOOD_1	AN14	
VCCPWRGOOD_0	AN27	25,42 H_PWRGD
SM_DRAMPWROK	AK13	22 PM_DRAM_PWRGD
VTTPWRGOOD	AM15	49 H_VTTPWRGD
TAPPWRGOOD	AM26	H_PWRGD_XDP
RSTIN#	AL14	21,37,70,76 PLT_RST#

R908 2 VCCPWRGOOD 0R0402-PAD
R912 2 VDDPWRGOOD_R 0R0402-PAD
R913 1 1K6R2F-GP
PLT_RST#_R R915 750R2F-GP

AUBURNDALE CLOCKS

BCLK	A16	BCLK_CPU_P_R
BCLK#	B16	BCLK_CPU_N_R
BCLK_ITP	AR30	BCLK_ITP_P
BCLK_ITP#	AT30	BCLK_ITP_N
PEG_CLK	E16	PEG_CLK_R
PEG_CLK#	D16	PEG_CLK#_R
DPLL_REF_SSCLK	A18	
DPLL_REF_SSCLK#	A17	

RN901 1 4 0R4P2R-PAD BCLK_CPU_P 25 BCLK_CPU_N 25
RN903 1 4 0R4P2R-PAD CLK_EXP_P 23 CLK_EXP_N 23

THERMAL DDR3 MISC

SM_DRAMRST#	F6	SM_DRAMRST#
SM_RCOMP0	AL1	SM_RCOMP_0
SM_RCOMP1	AM1	SM_RCOMP_1
SM_RCOMP2	AN1	SM_RCOMP_2
PM_EXT_TS0#	AN15	PM_EXTTS#0_C
PM_EXT_TS1#	AP15	PM_EXTTS#1_C

RN905 4 3 2 1 SRN10KJ-5-GP
0R4P2R-PAD RN906 4 3 2 1 PM_EXTTS#0 18 PM_EXTTS#1 19
PM_EXTTS#0_C 53

PWR MANAGEMENT

PRDY#	AT28	XDP_PRDY#
PREQ#	AP27	XDP_PREQ#
TCK	AN28	XDP_TCLK
TMS	AP28	XDP_TMS
TRST#	AT27	XDP_TRST#
TDI	AT29	XDP_TDI_R
TDO	AR27	XDP_TDO_R
TDI_M	AR29	XDP_TDI_M
TDO_M	AP29	XDP_TDO_M
DBR#	AN25	H_DBR#_R

R909 2 0R0402-PAD XDP_DBRESET#

BPM0#	AJ22	XDP_OBS0
BPM1#	AK22	XDP_OBS1
BPM2#	AK24	XDP_OBS2
BPM3#	AJ24	XDP_OBS3
BPM4#	AJ25	XDP_OBS4
BPM5#	AH22	XDP_OBS5
BPM6#	AK23	XDP_OBS6
BPM7#	AH23	XDP_OBS7

DDR_RST_GATE 25
C915 SCD047U16V2ZY-1GP
+1.5V_SUS
R934 1KR2J-1-GP
Q901 2N7002E-1-GP
DDR3_DRAMRST# 18,19
C903 SCD1U10V2KX-5GP
R935 DY 0R2J-2-GP
SM_DRAMRST# R988 100KR2J-1-GP

DDR3 Compensation Signals

SM_RCOMP_0 R907 100R2F-L1-GP-U
SM_RCOMP_1 R910 24D9R2F-L-GP
SM_RCOMP_2 R911 130R2F-1-GP

XDP_TMS R914 DY 51R2J-2-GP
XDP_TDI_R R916 DY 51R2J-2-GP
XDP_PREQ# R917 DY 51R2J-2-GP
XDP_TCLK R918 DY 51R2J-2-GP

1119

	R919	R920
S3 circuit	1.1k No Stuff	0.75k
Normal	1.27k	3k

+3.3V_RUN
U927 74LVC1G08GW-1-GP
37,42,49 VTT_PWRGD
VTT_PWRGD_R3 R977 1K6R2F-GP VDDPWRGOOD_R
37 VDDPWRGOOD_KBC R978 DY 1K6R2F-GP

+1.5V_RUN
R919 DY 1K1R2F-GP
VDDPWRGOOD_R
R937 750R2F-GP

XDP1 PAD-60P-GP

XDP_PREQ#	XDP_PRDY#	
XDP_OBS0	XDP_OBS1	
XDP_OBS2	XDP_OBS3	
XDP_OBS4	XDP_OBS5	
XDP_OBS6	XDP_OBS7	
BCLK_ITP_P	BCLK_ITP_N	
XDP_RST#_R	H_CPURST#	
XDP_TRST#	XDP_TDI	XDP_TMS
XDP_TCLK		

+1.05V_VTT
H_PWRGD R927 DY 1KR2J-1-GP H_CPUPWRGD_XDP
22 PM_PWRBTN#_R R929 DY 0R2J-2-GP PM_PWRBTN#_XDP
H_PWRGD_XDP R930 DY 0R2J-2-GP PCIE_CLK_XDP_P
C902 DY SCD1U16V2KX-3GP
23 SML0_DATA
23 SML0_CLK

+1.05V_VTT
C901 DY SCD1U16V2KX-3GP
R928 51R2J-2-GP
XDP_RST#_R R931 DY 1KR2J-1-GP H_CPURST#
XDP_DBRESET# 22
XDP_TDO
XDP_RST#_R R932 DY 0R2J-2-GP PLT_RST# 21,37,70,76

XDP_TDI_R	R921 DY 0R2J-2-GP	XDP_TDI
XDP_TDO_M	R922 DY 0R2J-2-GP	XDP_TDO
XDP_TDI_M	R925 DY 0R2J-2-GP	
XDP_TDO_R	R926	

R924 0R0402-PAD
XDP_TRST# R923 51R2J-2-GP

JTAG MAPPING

Scan Chain (Default)	Stuff --> R921, R924, R926 No Stuff --> R922, R925
CPU Only	Stuff --> R921, R922 No Stuff --> R924, R926, R925
GMCH Only	Stuff --> R926, R925 No Stuff --> R921, R922, R924

<Core Design>

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Title: CPU (THERMAL/CLOCK/PM)
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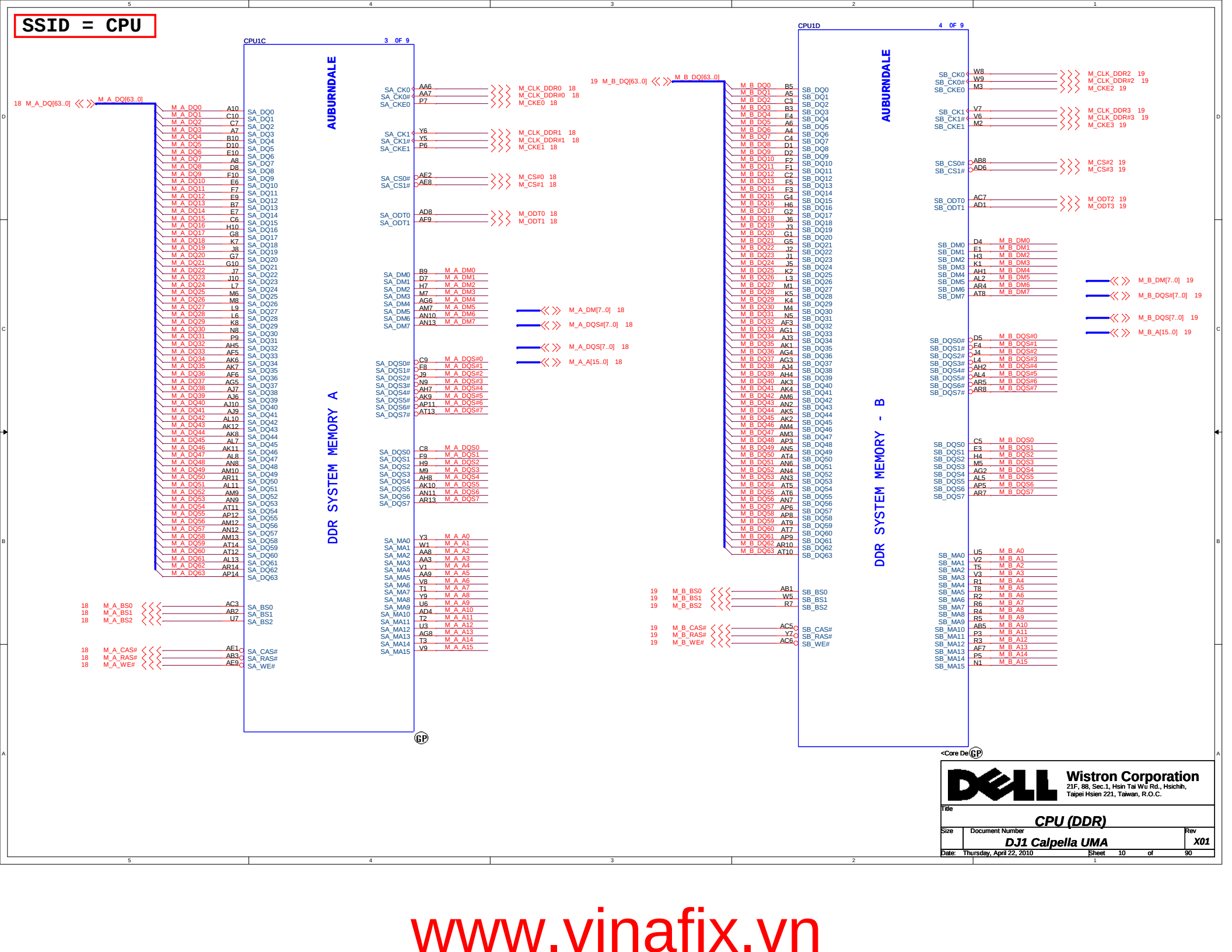
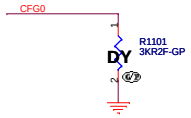
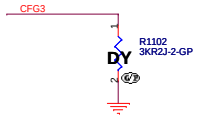


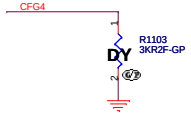
SSID = CPU



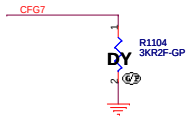
PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled



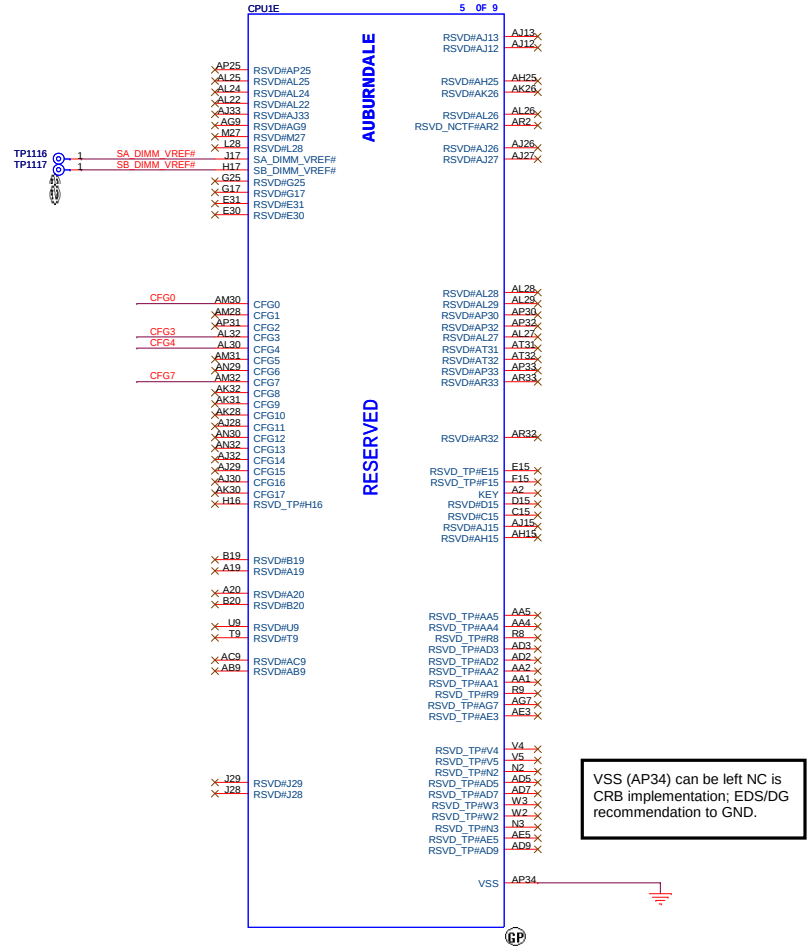
CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...



CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port



CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.



VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.

<Core Design>

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Title: CPU (RESERVED)

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SSID = CPU

PROCESSOR CORE POWER

48A

+VCC_CORE

C1206 C1207 C1208 C1209 C1220 C1210
C1212 C1213 C1214 C1215 C1223 C1224
C1225 C1226 C1227 C1229 C1230 C1231 C1232
C1235 C1236 C1237 C1238 C1240 C1241 C1242
C1243

SC10U6D3V5KX-1GP
SC10U6D3V5MX-3GP

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X01

CPU1F

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AUBURNDALE

AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26 AF35 AF34 AF33 AF32 AF31 AF30 AF29 AF28 AF27 AF26 AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26 AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26 AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26 V35 V34 V33 V32 V31 V30 V29 V28 V27 V26 U35 U34 U33 U32 U31 U30 U29 U28 U27 U26 R35 R34 R33 R32 R31 R30 R29 R28 R27 R26 P35 P34 P33 P32 P31 P30 P29 P28 P27 P26 — VCC

1.1V RAIL POWER

AH14 AH12 AH11 AH10 J14 J13 H14 H12 G14 G13 G12 G11 F14 F13 F12 F11 E14 E12 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11 — VTT0

+1.05V_VTT

C1216 C1201 C1202 C1217 C1218 C1203 C1219 C1204 C1205
SC10U6D3V5KX-1GP
SC10U10V5ZY-1GP
SC10U10V5ZX-1GP

C1211 C1221 C1222
SC10U6D3V5KX-1GP
SC10U6D3V5MX-3GP

CPU CORE SUPPLY

AF10 AE10 AC10 AB10 Y10 W10 U10 T10 J12 J11 J16 J15 — VTT0

C1233 C1234
SC10U6D3V5KX-1GP
SC10U6D3V5MX-3GP

Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V

POWER

CPU VIDS

PSI# — AN33 — PSI# 47

VID0 VID1 VID2 VID3 VID4 VID5 VID6 — AK35 AK33 AK34 AL35 AL33 AM33 AM35 — H_VID0 H_VID1 H_VID2 H_VID3 H_VID4 H_VID5 H_VID6 — H_VID[6..0] 47

PROC_DPRSLPVR — AM34 — PM_DPRSLPVR 47

VTT_SELECT — G15 — H_VTTVID1 — TP1201TPAD14-GP

H_VTTVID1 = Low, 1.1V
H_VTTVID1 = High, 1.05V

SENSE LINES

ISENSE — AN35 — IMVP_IMON 47

R1201 100R2F-L1-GP-U

VCC_SENSE — AJ34 — VCC_SENSE 47
VSS_SENSE — AJ35 — VSS_SENSE 47

VTT_SENSE — B15 — VTT_SENSE 49
VSS_SENSE_VTT — A15 — TP_VSS_SENSE_VTT — TP1202TPAD14-GP

R1204 100R2F-L1-GP-U

The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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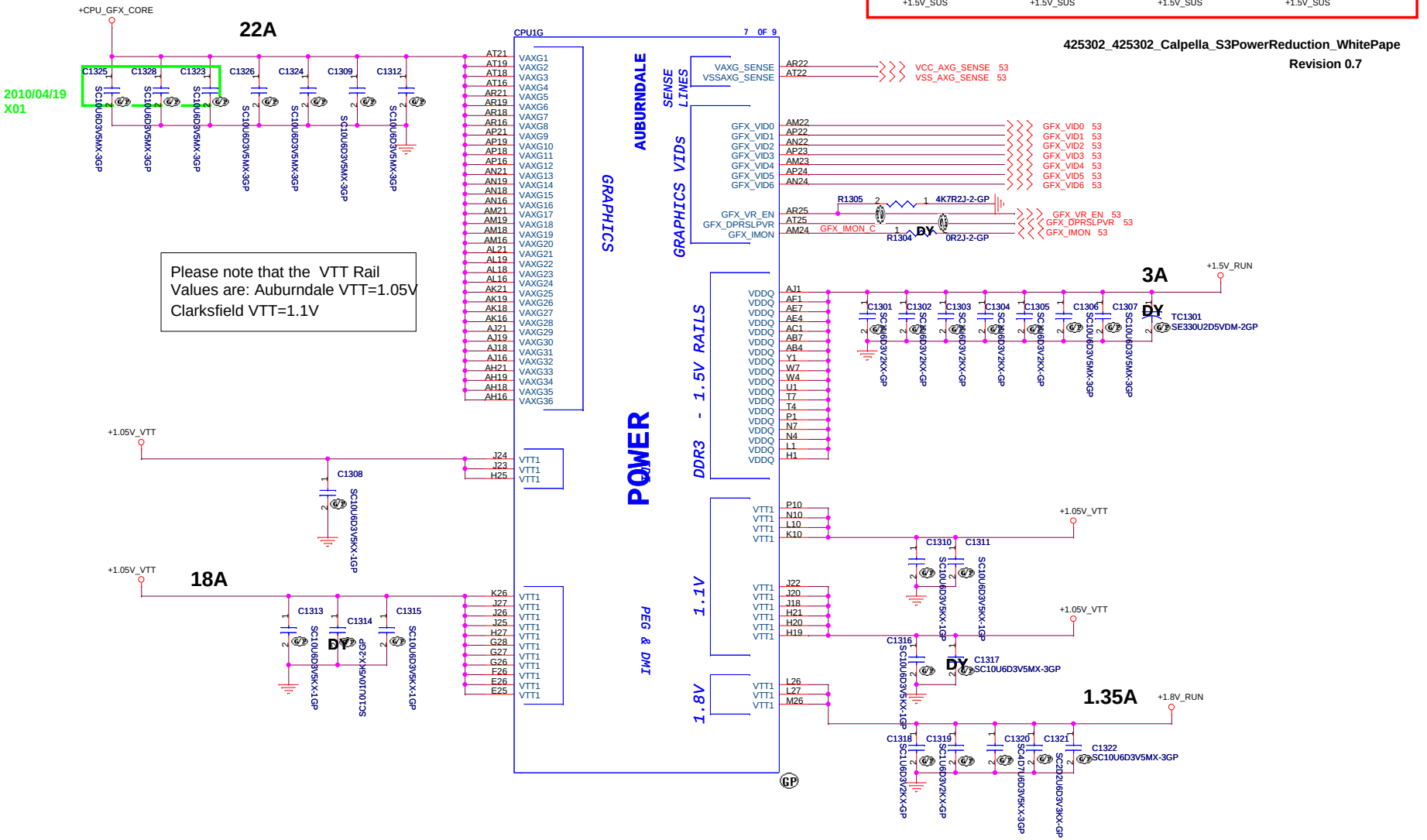
Title: CPU (VCC_CORE)
Size: Document Number: DJ1 Calpella UMA
Rev: X01
Date: Thursday, April 22, 2010 Sheet 12 of 90

SSID = CPU



425302_425302_Calpella_S3PowerReduction_WhitePape

Revision 0.7

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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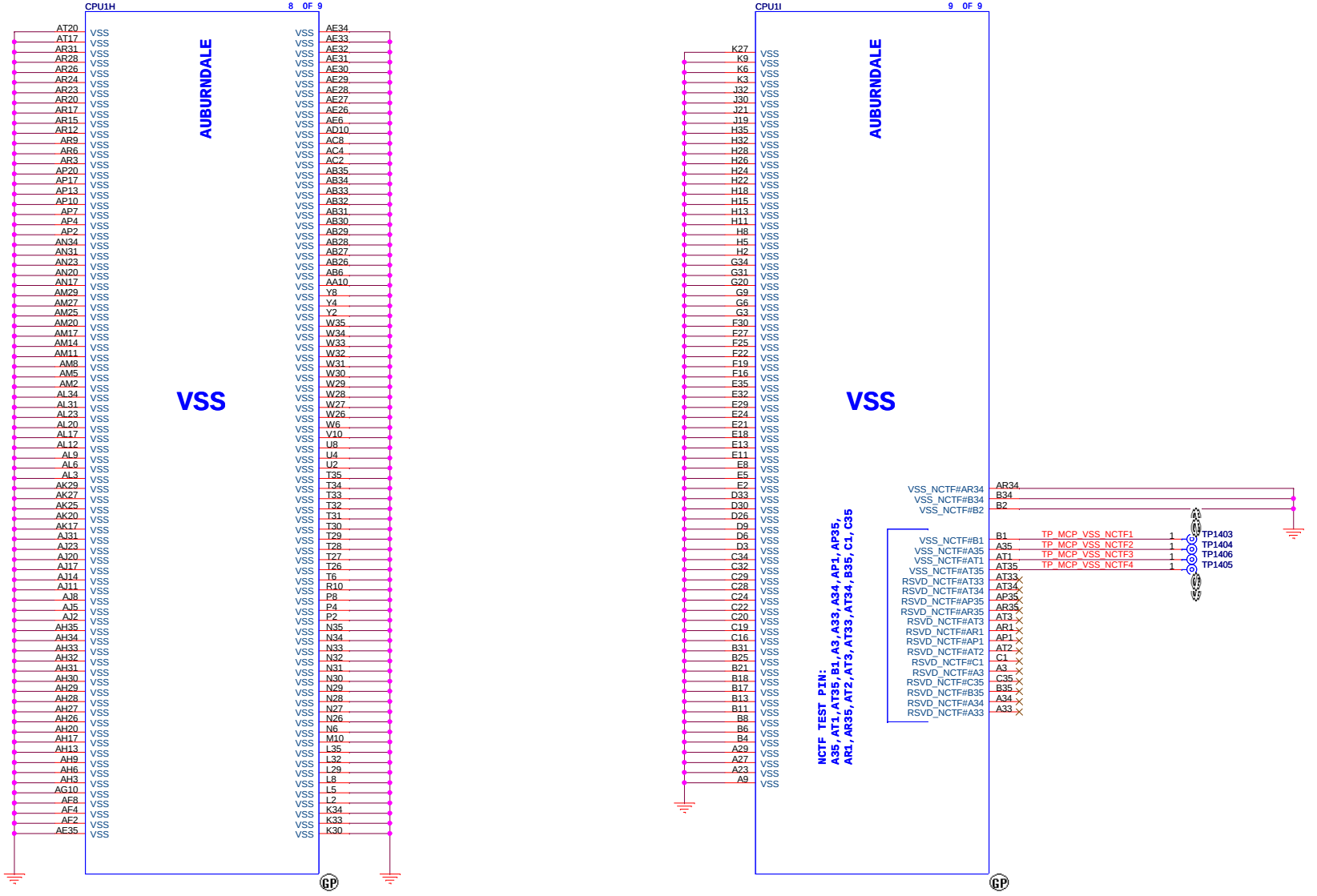
Title	CPU (VCC_GFXCORE)	
Size	Document Number: DJ1 Calpella UMA	Rev: X01
Date: Thursday, April 22, 2010	Sheet 13 of 90	

SSID = CPU



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU (VSS)	
Size	Document Number: DJ1 Calpella UMA	Rev: X01
Date: Friday, April 16, 2010	Sheet 14 of 90	

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<Core Design>

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Title: Reserved

Size: A3 | Document Number: DJ1 Calpella UMA | Rev: X01

Date: Friday, April 16, 2010 | Sheet 15 of 90

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<Core Design>

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Title: Reserved

Size: A3 | Document Number: DJ1 Calpella UMA | Rev: X01

Date: Friday, April 16, 2010 | Sheet 16 of 90

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<Core Design>

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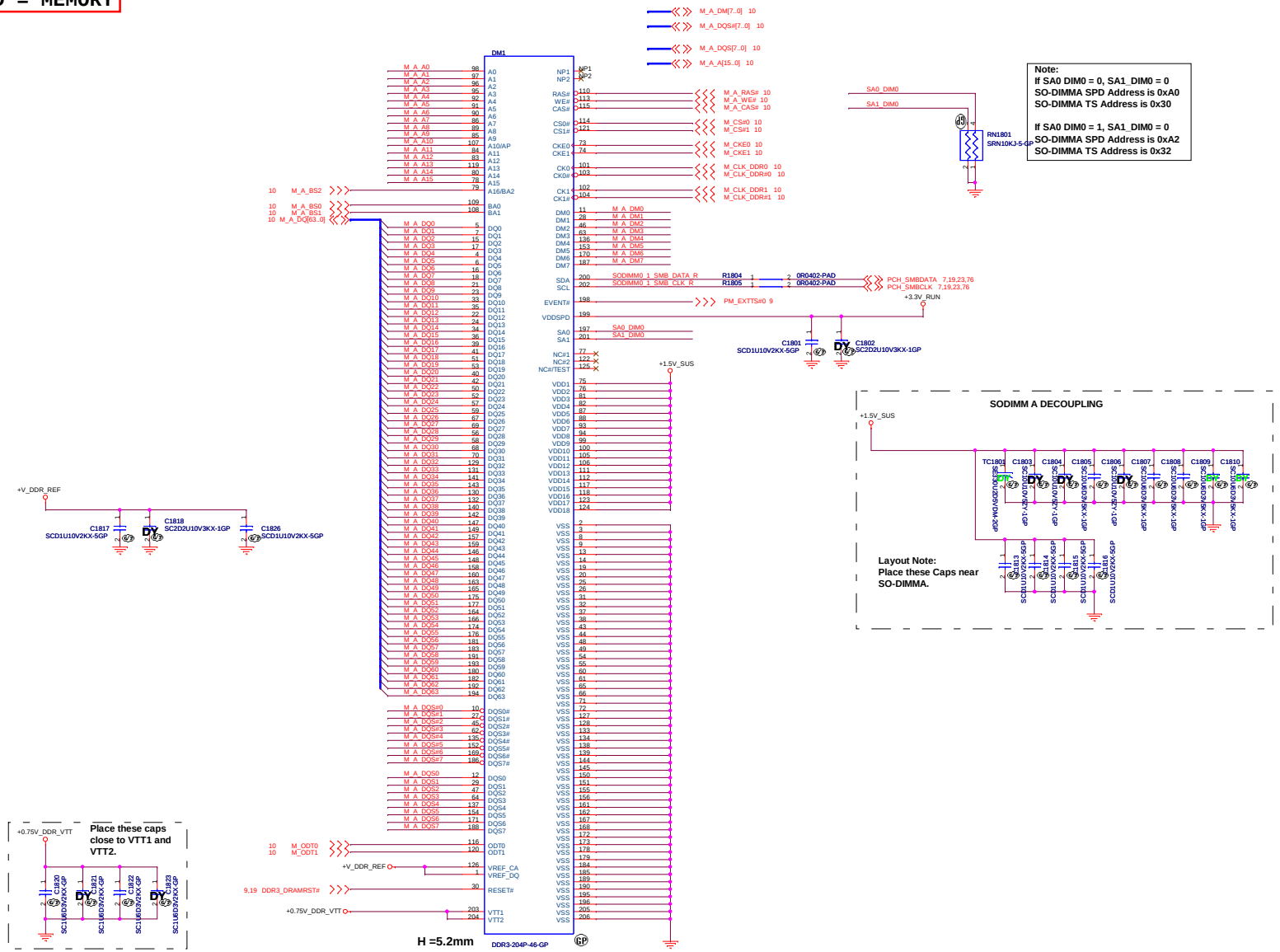
Title: Reserved

Size: A3 | Document Number: DJ1 Calpella UMA | Rev: X01

Date: Friday, April 16, 2010 | Sheet 17 of 90

SSID = MEMORY



62.10017.P11

<Core Design>

Wistron Corporation
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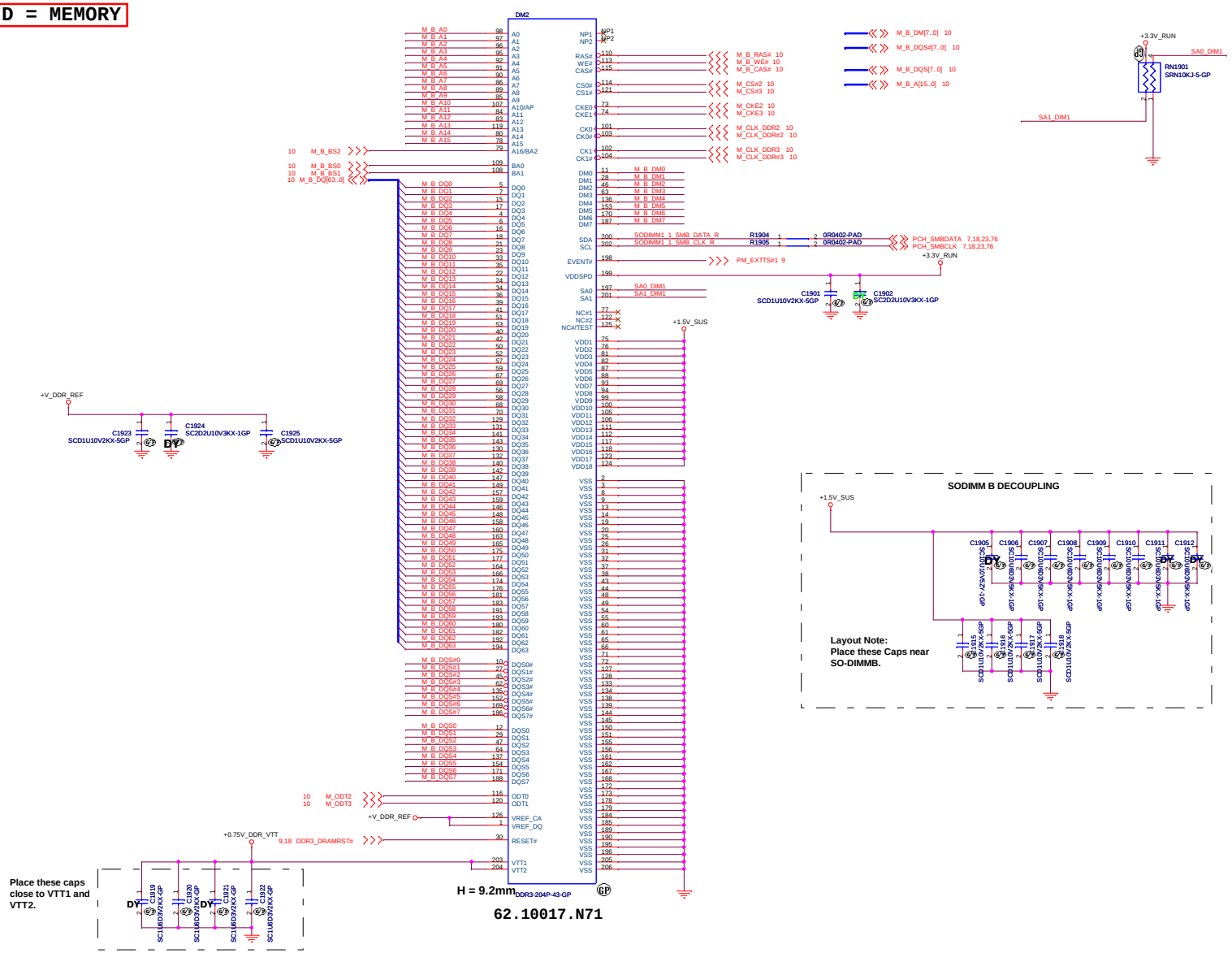
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM1

Size | Document Number: DJ1 Calpella UMA | Rev: X01

Date: Thursday, April 22, 2010 | Sheet 18 of 90

SSID = MEMORY



<Core Design>

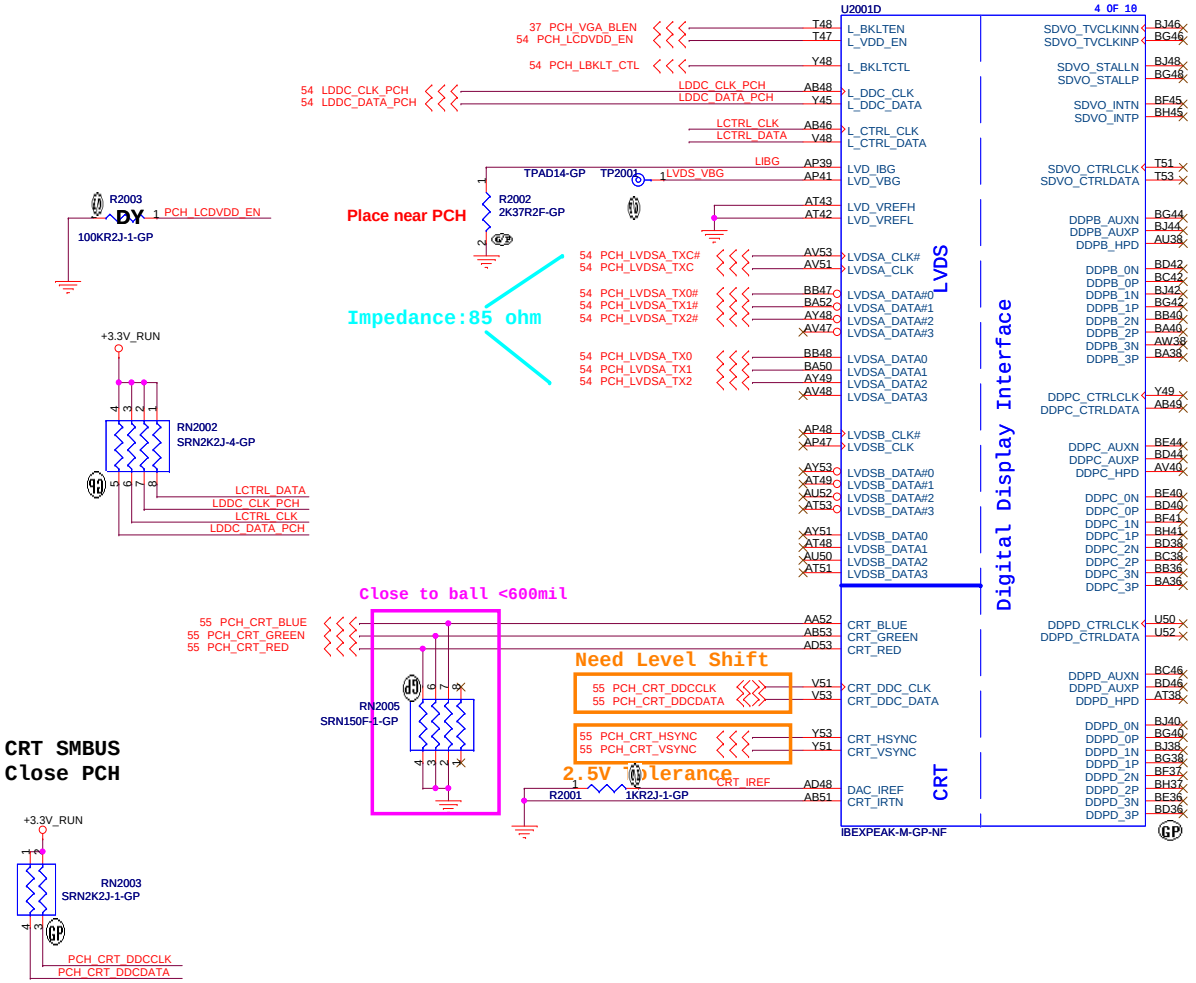
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM2

Size | Document Number: DJ1 Calpella UMA | Rev: X01

Date: Thursday, April 22, 2010 | Sheet 19 of 90

SSID = PCH



CRT SMBUS
Close PCH

<Core Design>

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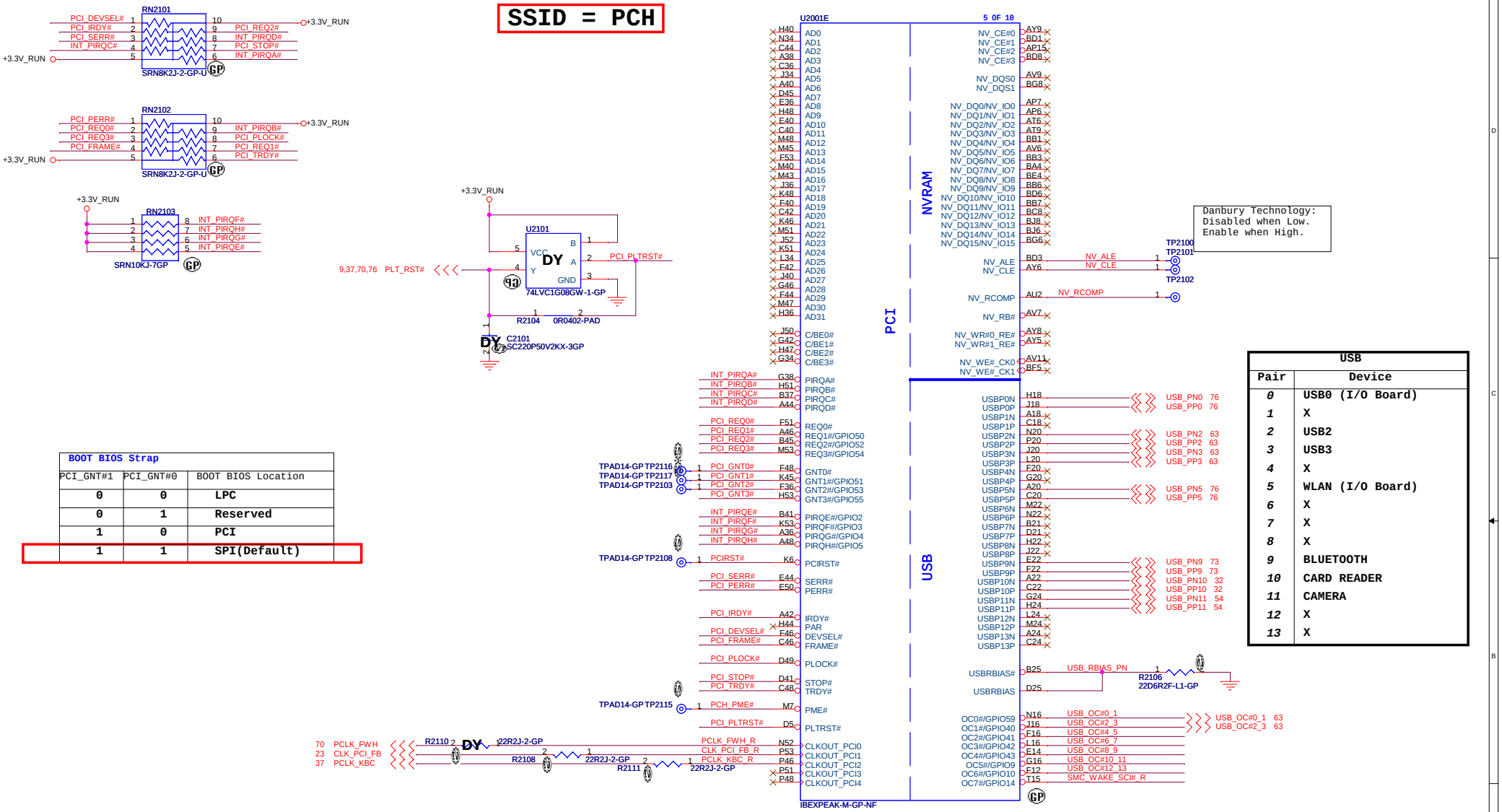
Title	PCH (LVDS/CRT/DDI)	
Size	Document Number: DJ1 Calpella UMA	Rev: X01
Date: Thursday, April 22, 2010	Sheet 20 of 90	

SSID = PCH



BOOT BIOS Strap		
PCI_GNT#1	PCI_GNT#0	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI(Default)

USB	
Pair	Device
0	USB0 (I/O Board)
1	X
2	USB2
3	USB3
4	X
5	WLAN (I/O Board)
6	X
7	X
8	X
9	BLUETOOTH
10	CARD READER
11	CAMERA
12	X
13	X

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

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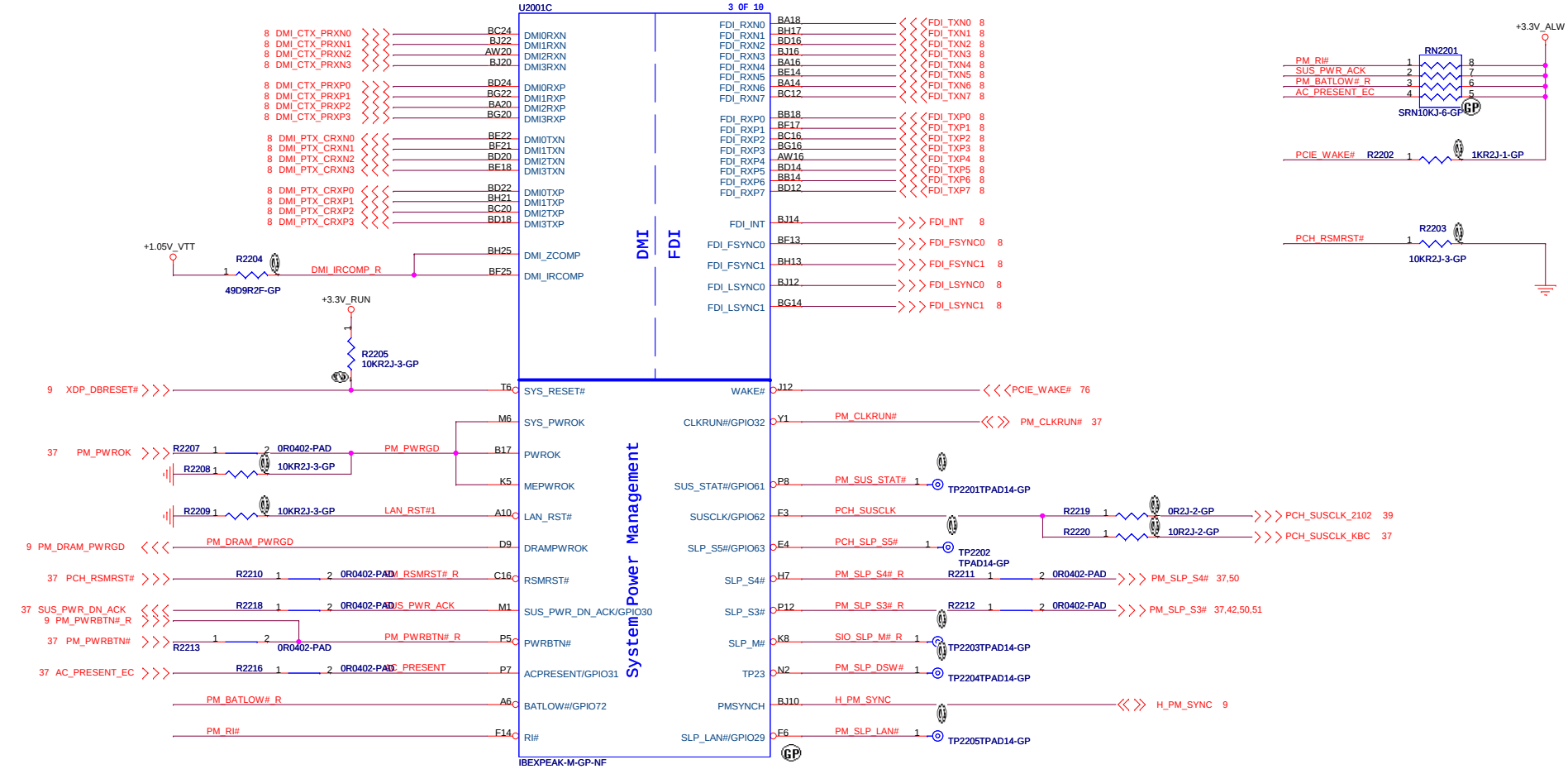
Title: PCH (PCI/USB/NVRAM)

Size: | Document Number: DJ1 Calpella UMA | Rev: X01

Date: Thursday, April 22, 2010 | Sheet 21 of 90

SSID = PCH



Option to " Disable " clkrun.
Pulling it down will keep the clks running.

<Core Design>

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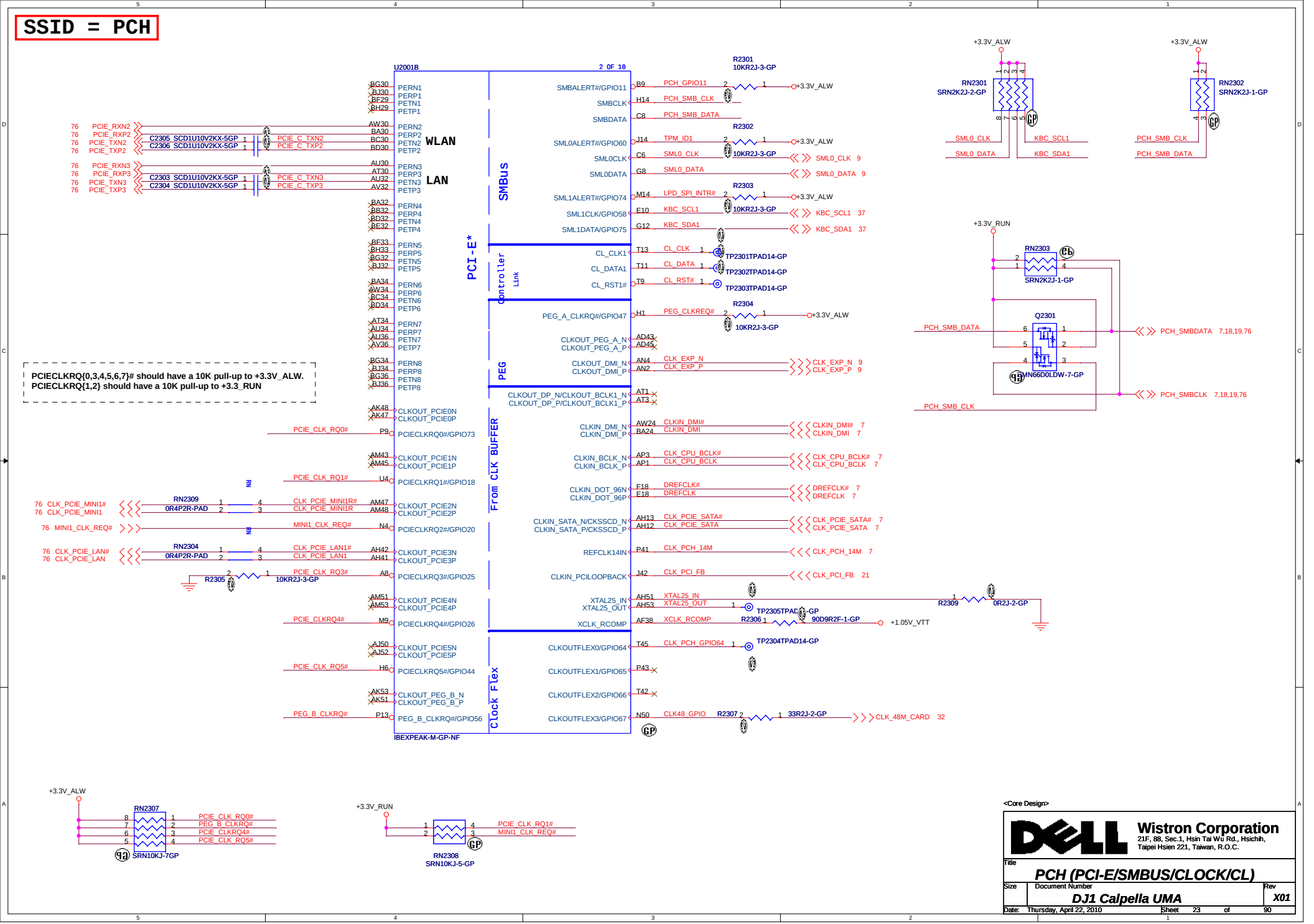
Title	PCH (DM I/FDI/PM)	
Size	Document Number: DJ1 Calpella UMA	Rev: X01
Date: Thursday, April 22, 2010	Sheet 22 of 90	

SSID = PCH



<Core Design>

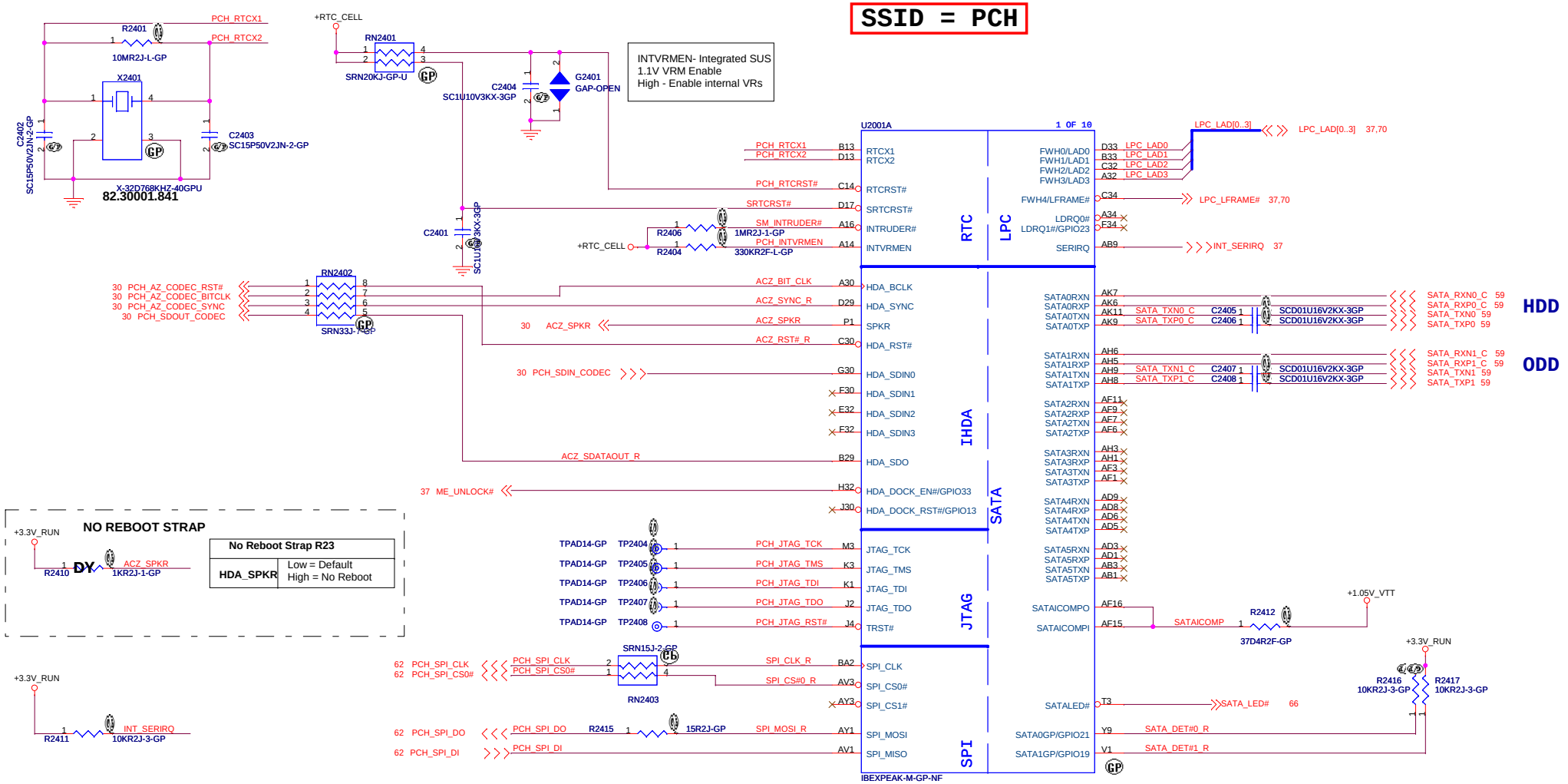
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI-E/SMBUS/CLOCK/CL)

Size | Document Number: DJ1 Calpella UMA | Rev: X01

Date: Thursday, April 22, 2010 | Sheet 23 of 90

SSID = PCH



<Core Design>

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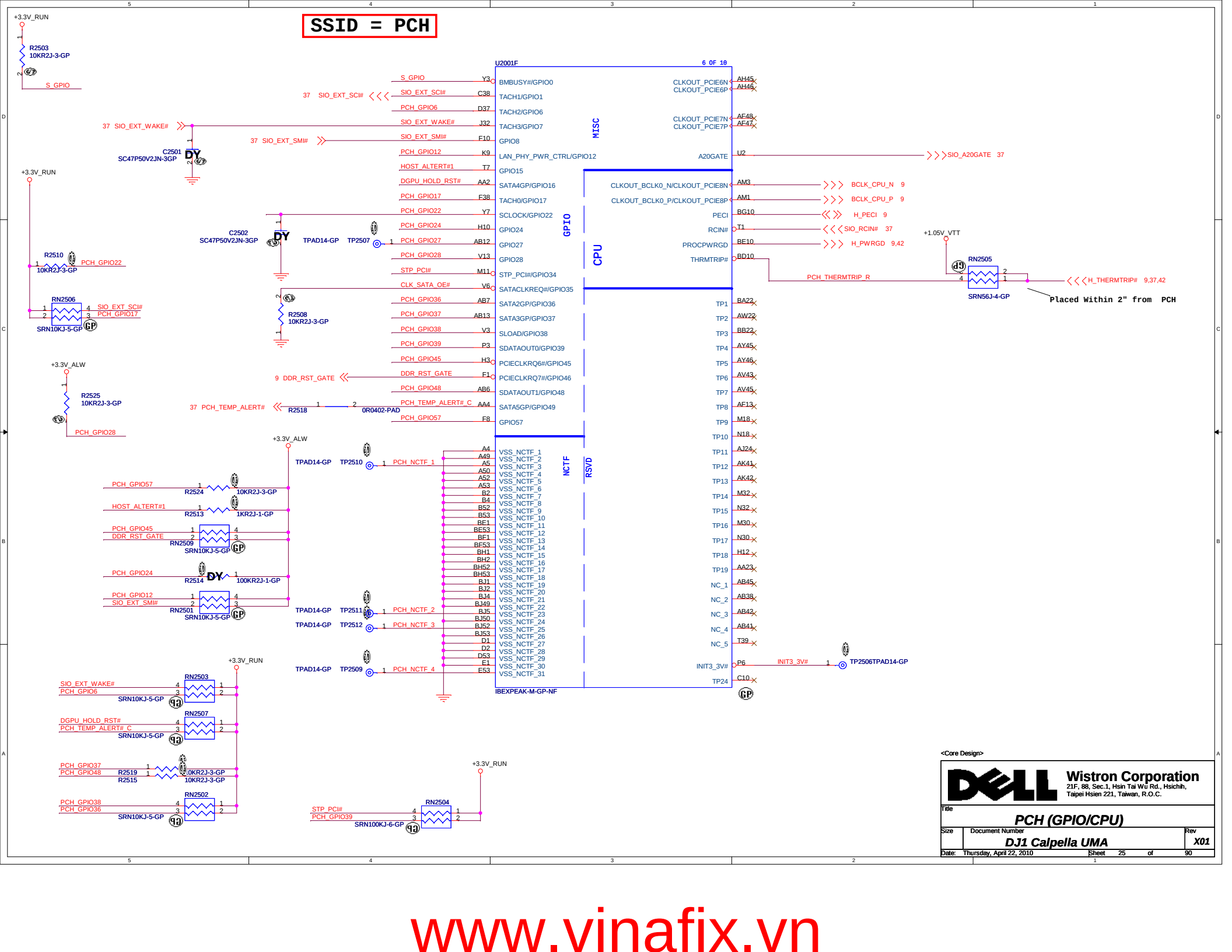
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (SPI/RTC/LPC/SATA/IHDA)

Size | Document Number: DJ1 Calpella UMA | Rev: X01

Date: Thursday, April 22, 2010 | Sheet 24 of 90

SSID = PCH



<Core Design>

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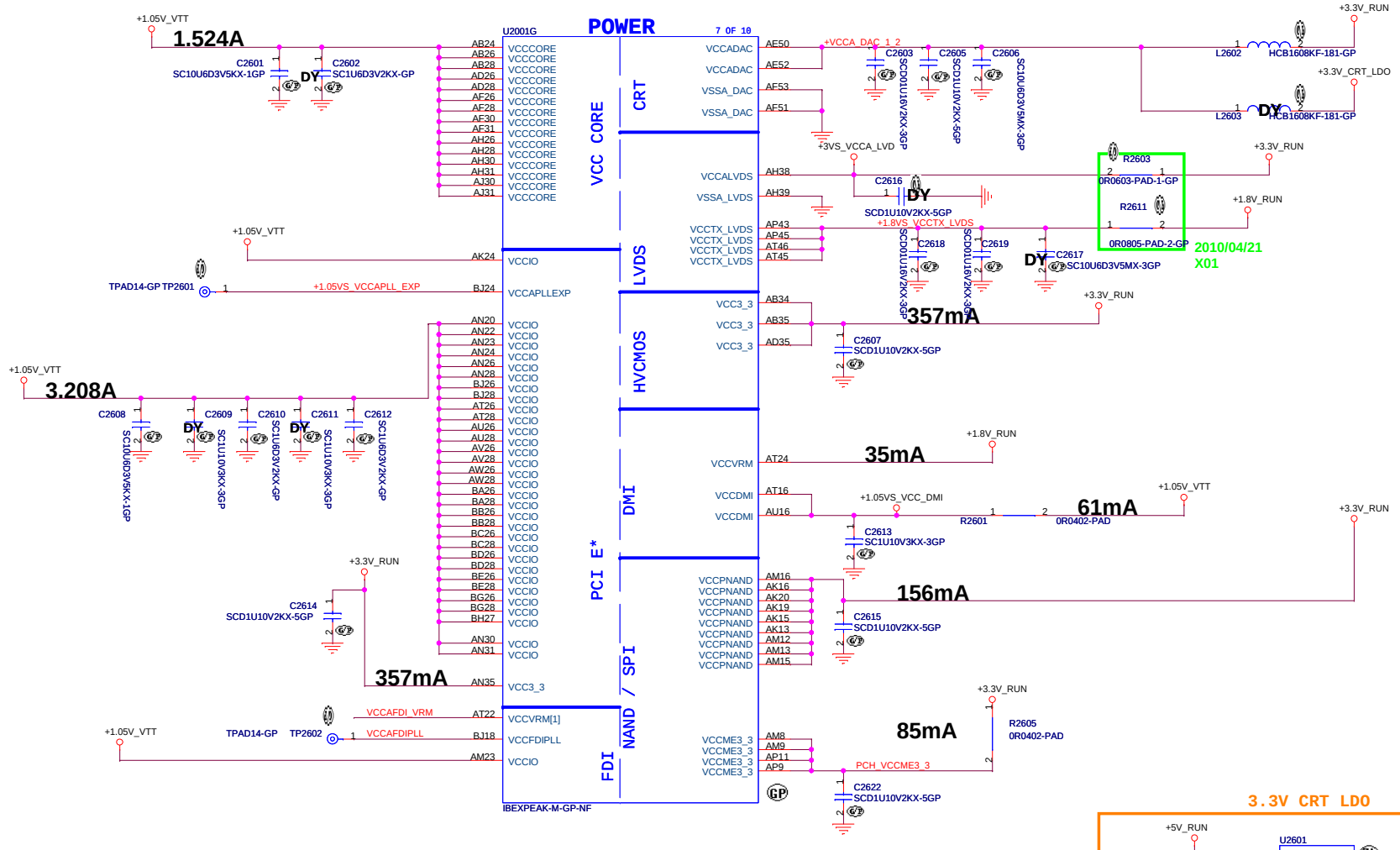
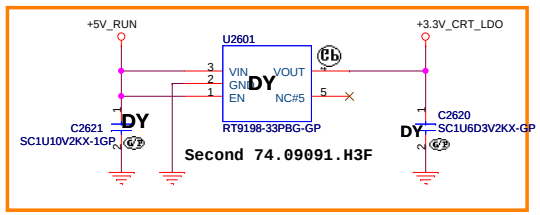
Title	PCH (GPIO/CPU)	
Size	Document Number: DJ1 Calpella UMA	Rev: X01
Date: Thursday, April 22, 2010	Sheet 25 of 90	

SSID = PCH



3.3V CRT LDO



<Core Design>

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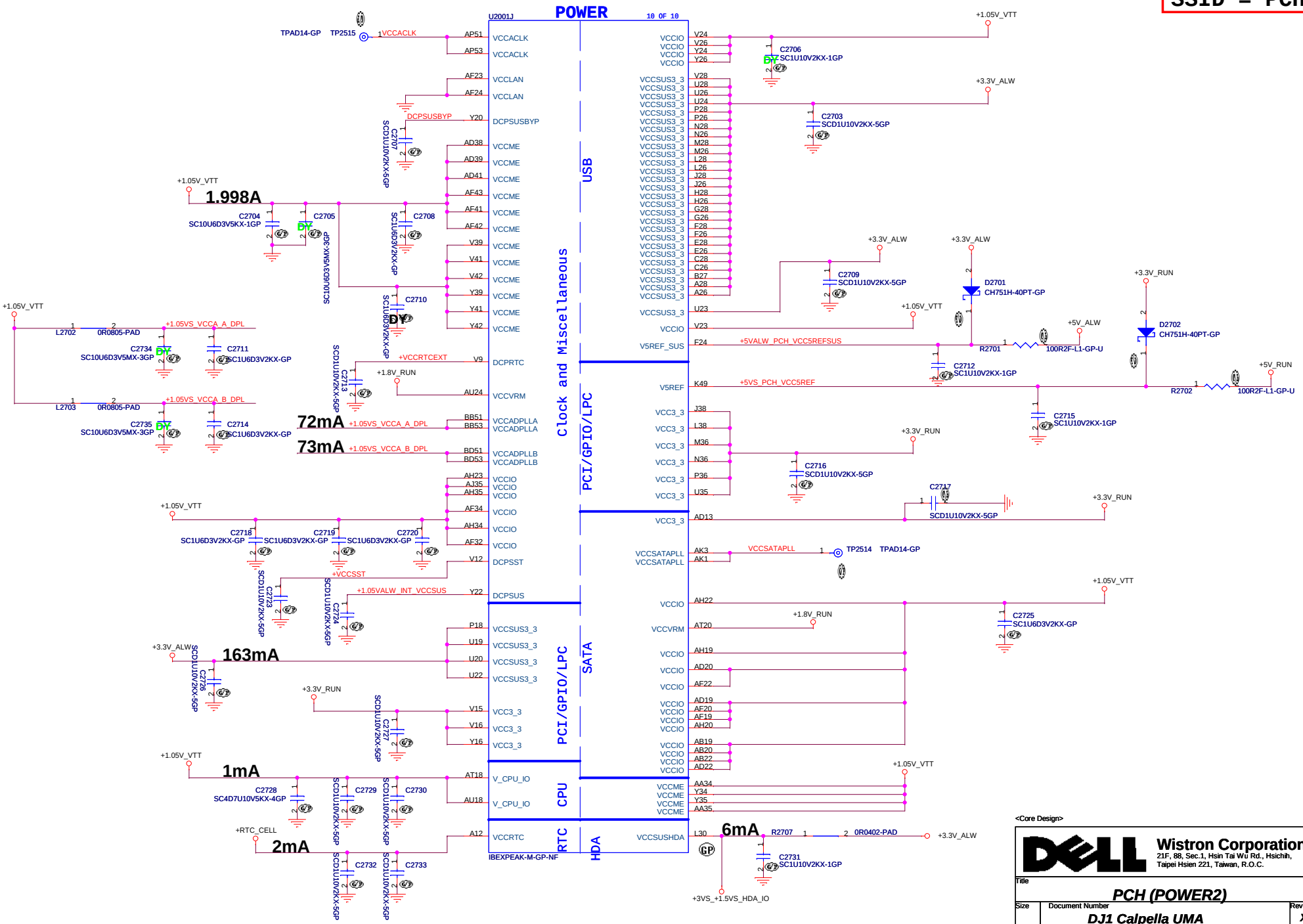
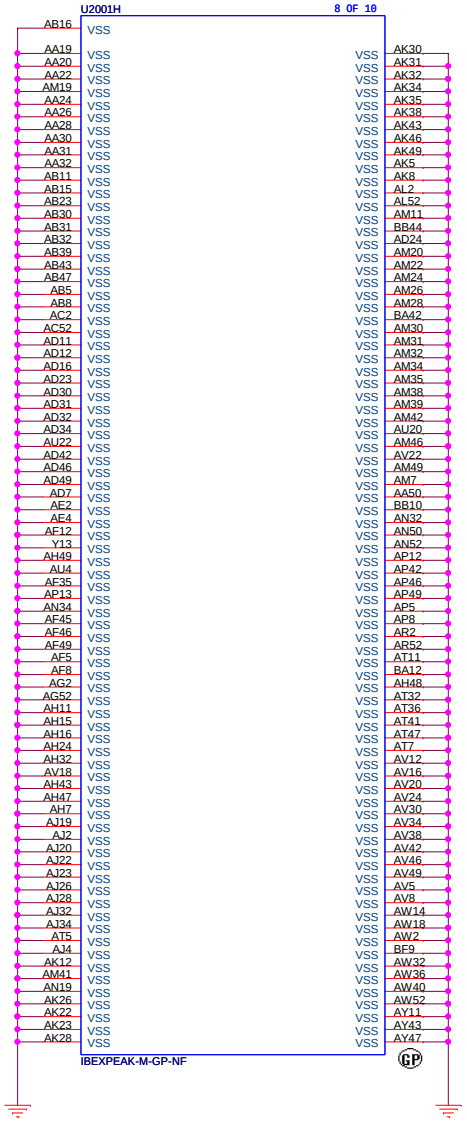
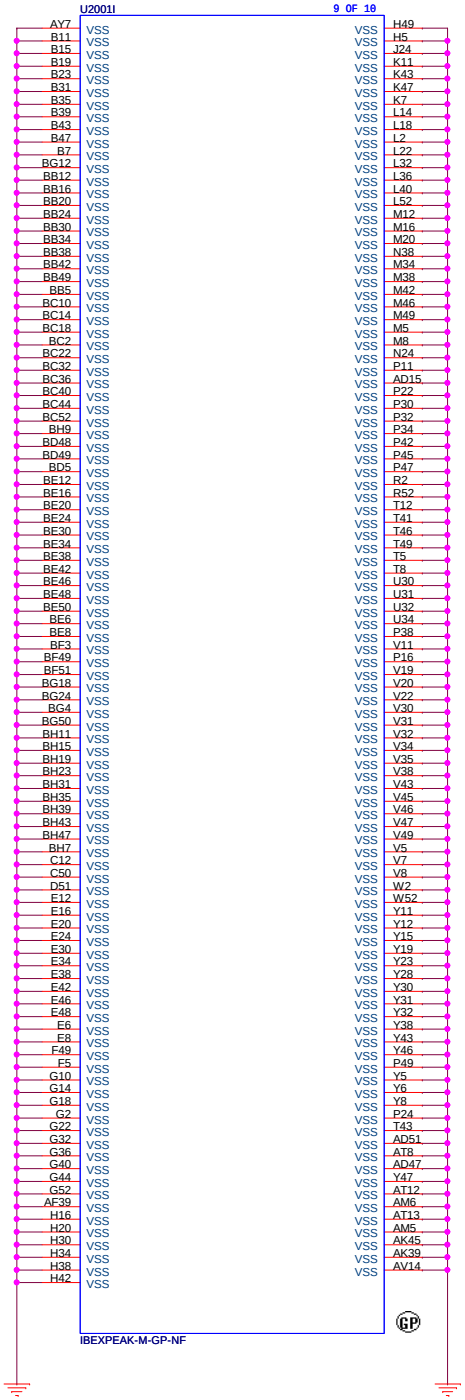
Title	PCH (POWER1)	
Size	Document Number: DJ1 Calpella UMA	Rev: X01
Date: Wednesday, April 21, 2010	Sheet 26 of 90	

SSID = PCH



SSID = PCH





<Core Design>

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Title	PCH (VSS)	
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<Core Design>

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Title: *Reserved*

Size: A3 | Document Number: *DJ1 Calpella UMA* | Rev: *X01*

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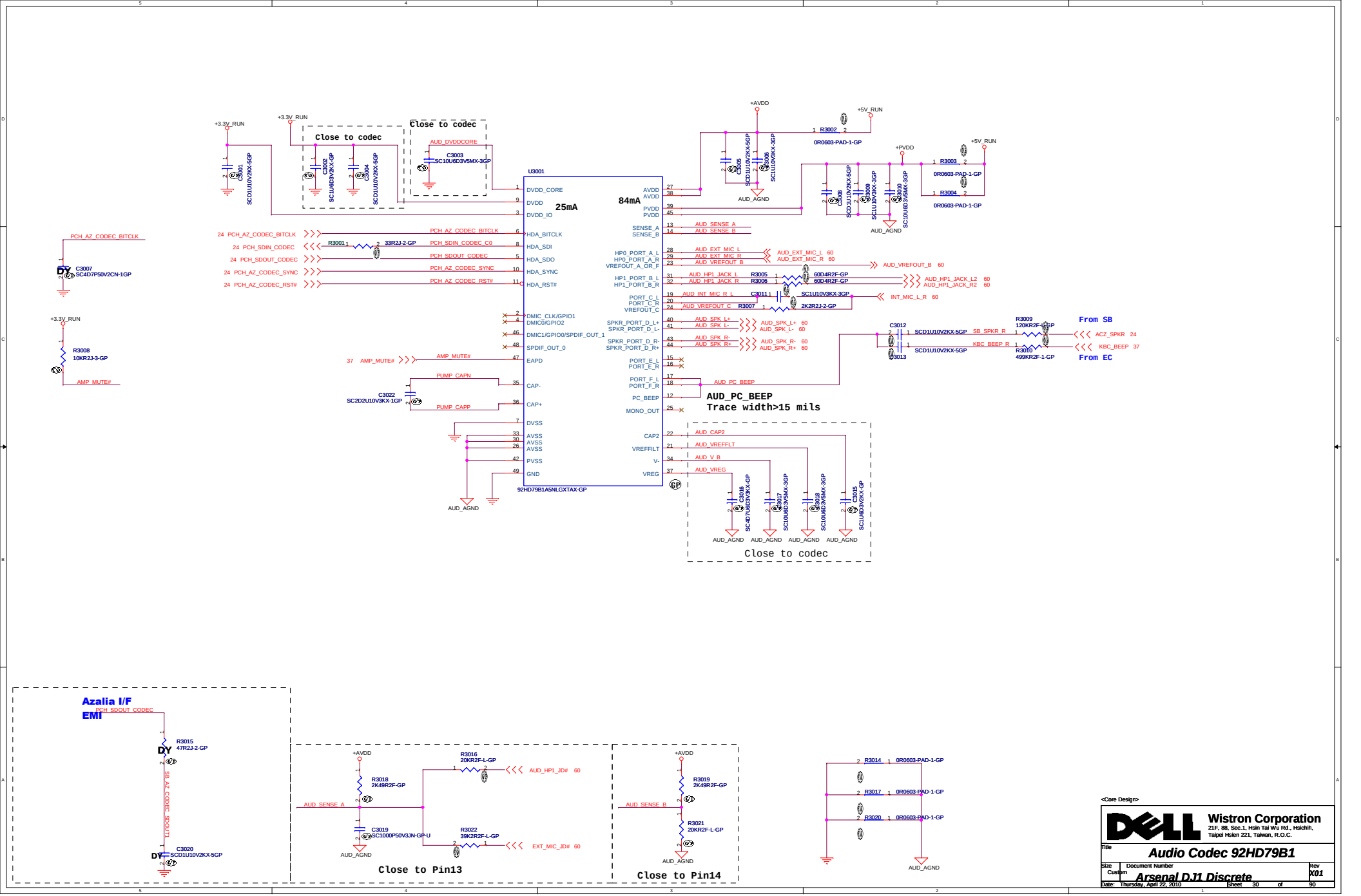

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<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title	Reserved	
Size: A3	Document Number: DJ1 Calpella UMA	Rev: X01
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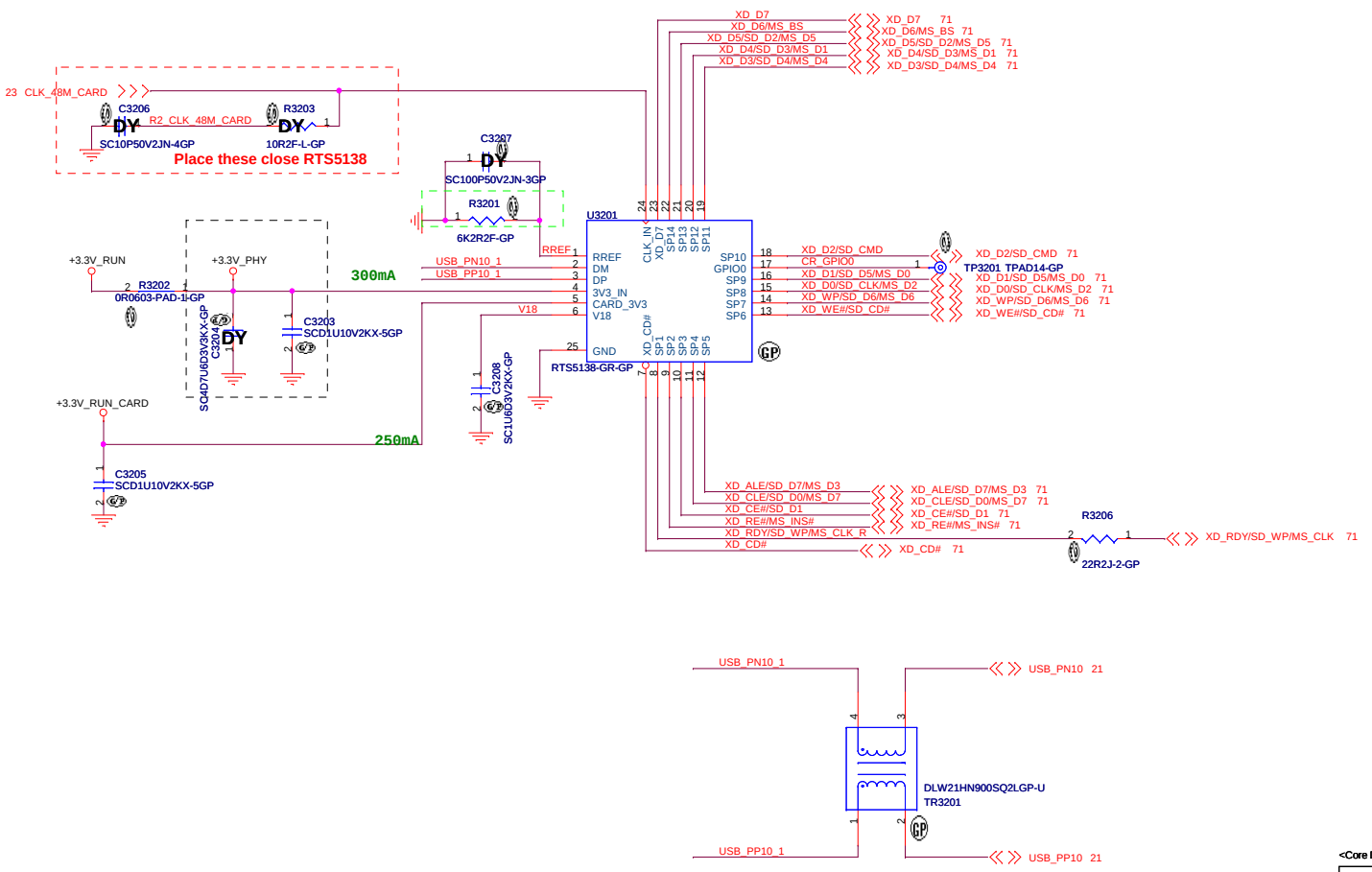
SSID = SDIO



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Card Reader-RTS5138

Size: Custom | Document Number: DJ1 Calpella UMA | Rev: X01

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: DJ1 Calpella UMA | Rev: X01

Date: Friday, April 16, 2010 | Sheet 33 of 90

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Reserved	
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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

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<Core Design>

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Title: Reserved

Size: A3 | Document Number: DJ1 Calpella UMA | Rev: X01

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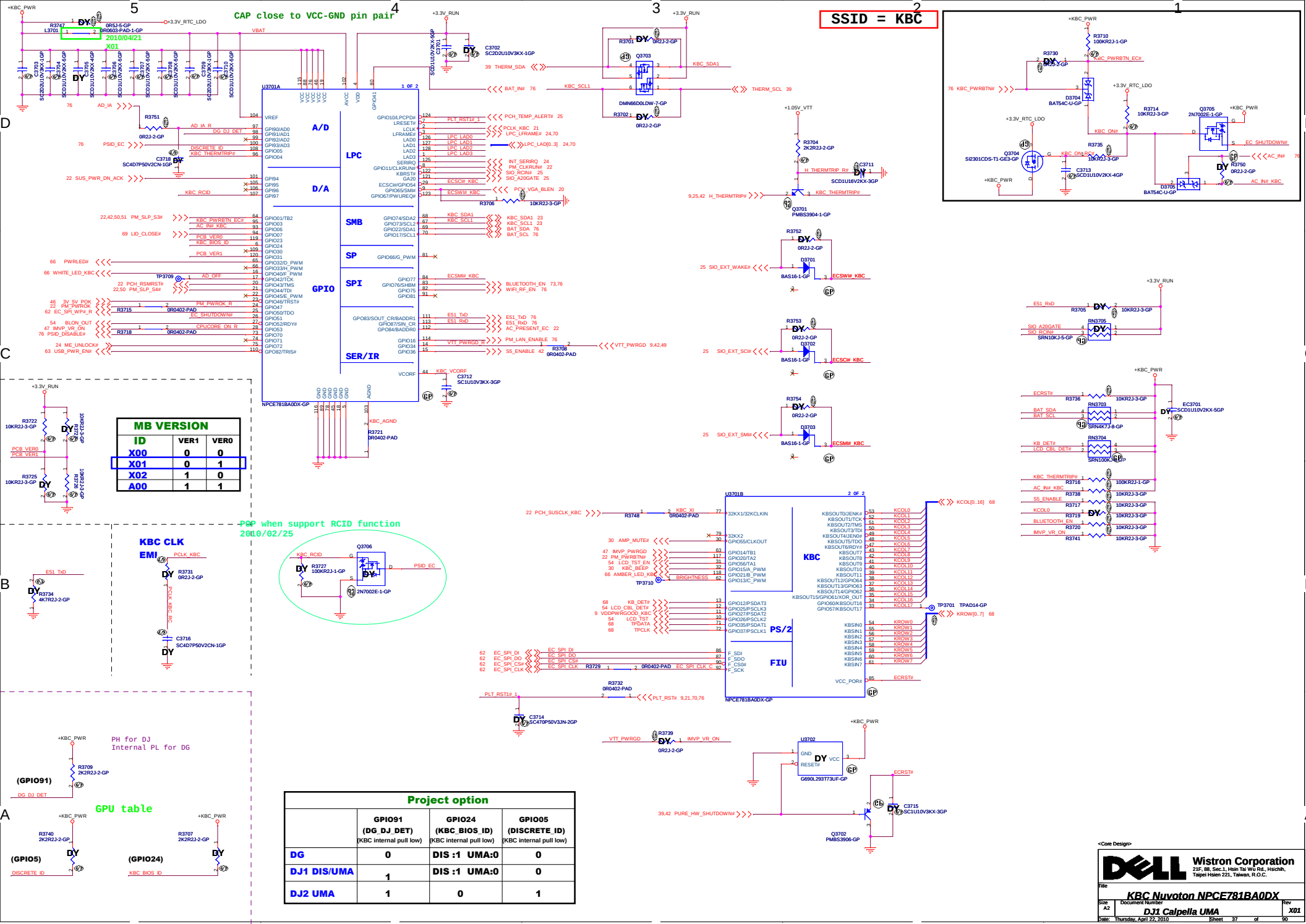

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<Core Design>

Wistron Corporation
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Title	Reserved	
Size: A3	Document Number: DJ1 Calpella UMA	Rev: X01
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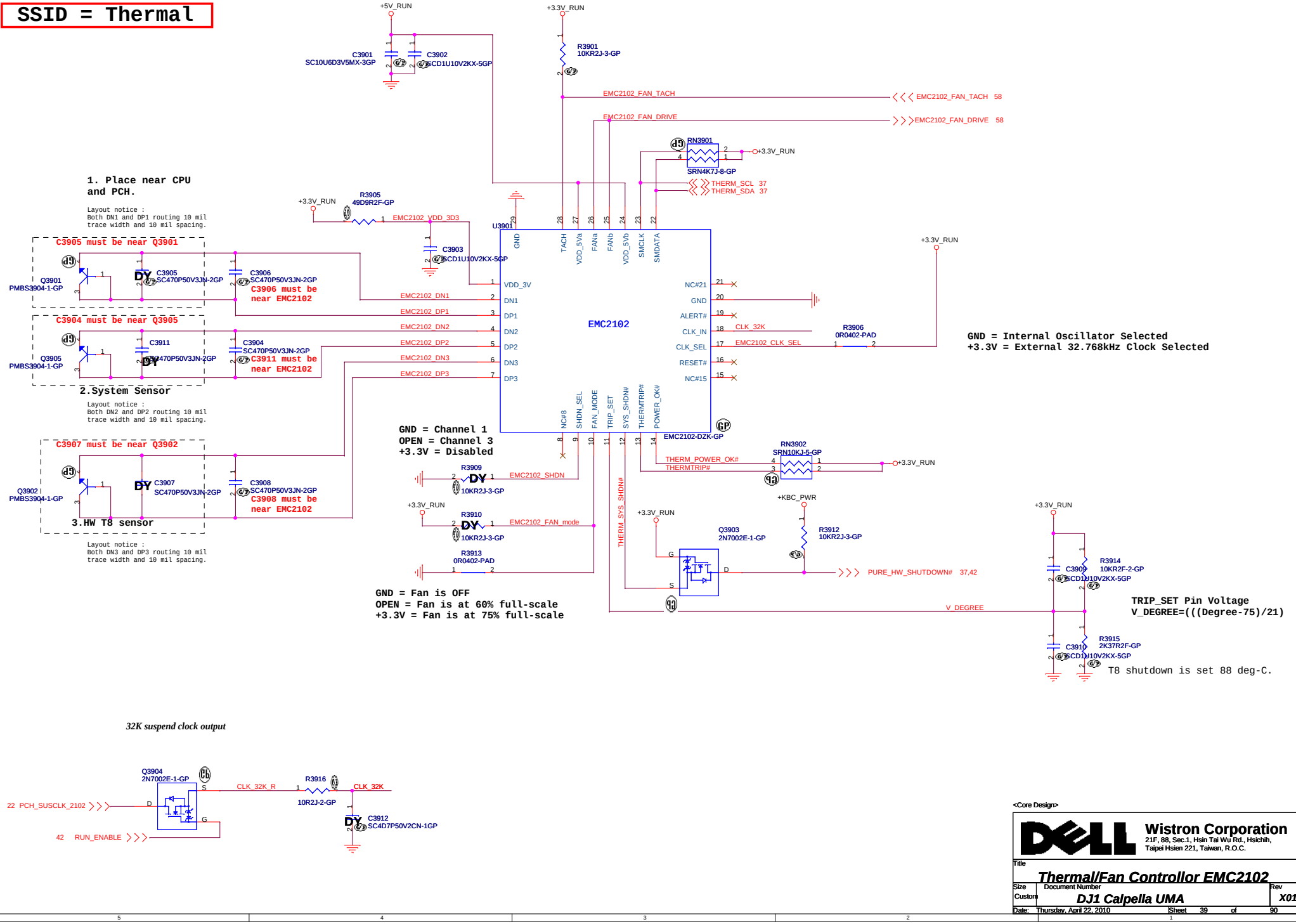
SSID = Thermal



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor EMC2102

Size	Document Number	Rev
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<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: DJ1 Calpella UMA | Rev: X01

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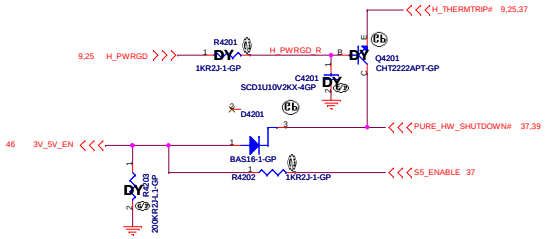
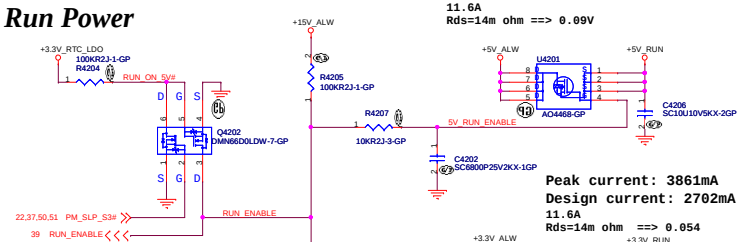
SSID = Reset.Suspend

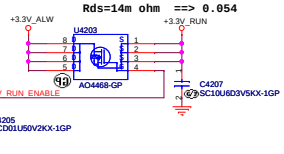


Peak current: 6370mA (HD:1100 ODD:2500)
Design current: 4459 mA
11.6A
Rds=14m ohm ==> 0.09V

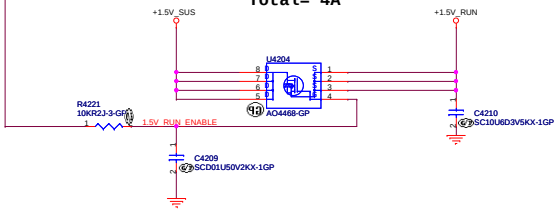
Run Power



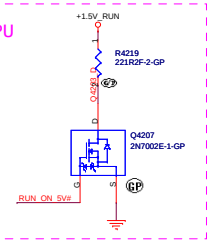
Peak current: 3861mA
Design current: 2702mA
11.6A
Rds=14m ohm ==> 0.054

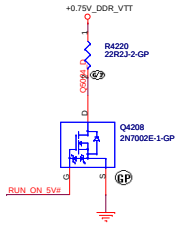


Total= 4A

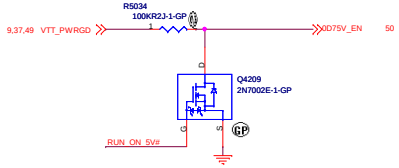


For CPU





425302_425302_Calpella_S3PowerReduction_WhitePape
Revision 0.7



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Power Plane Enable*

Size	Document Number	Rev
A2	*DJ1 Calpella UMA*	*X01*

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<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title	Reserved	
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<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

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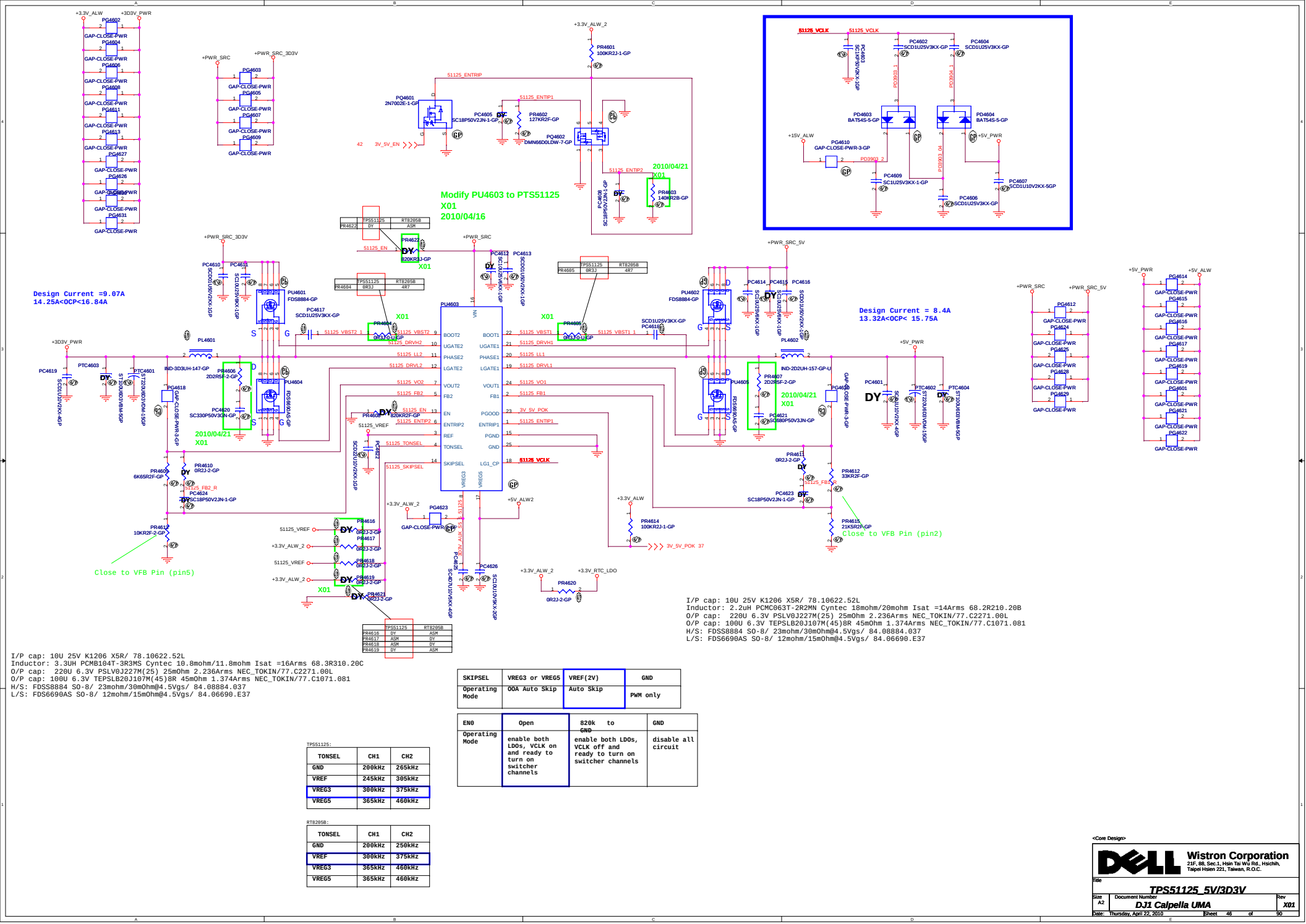


SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

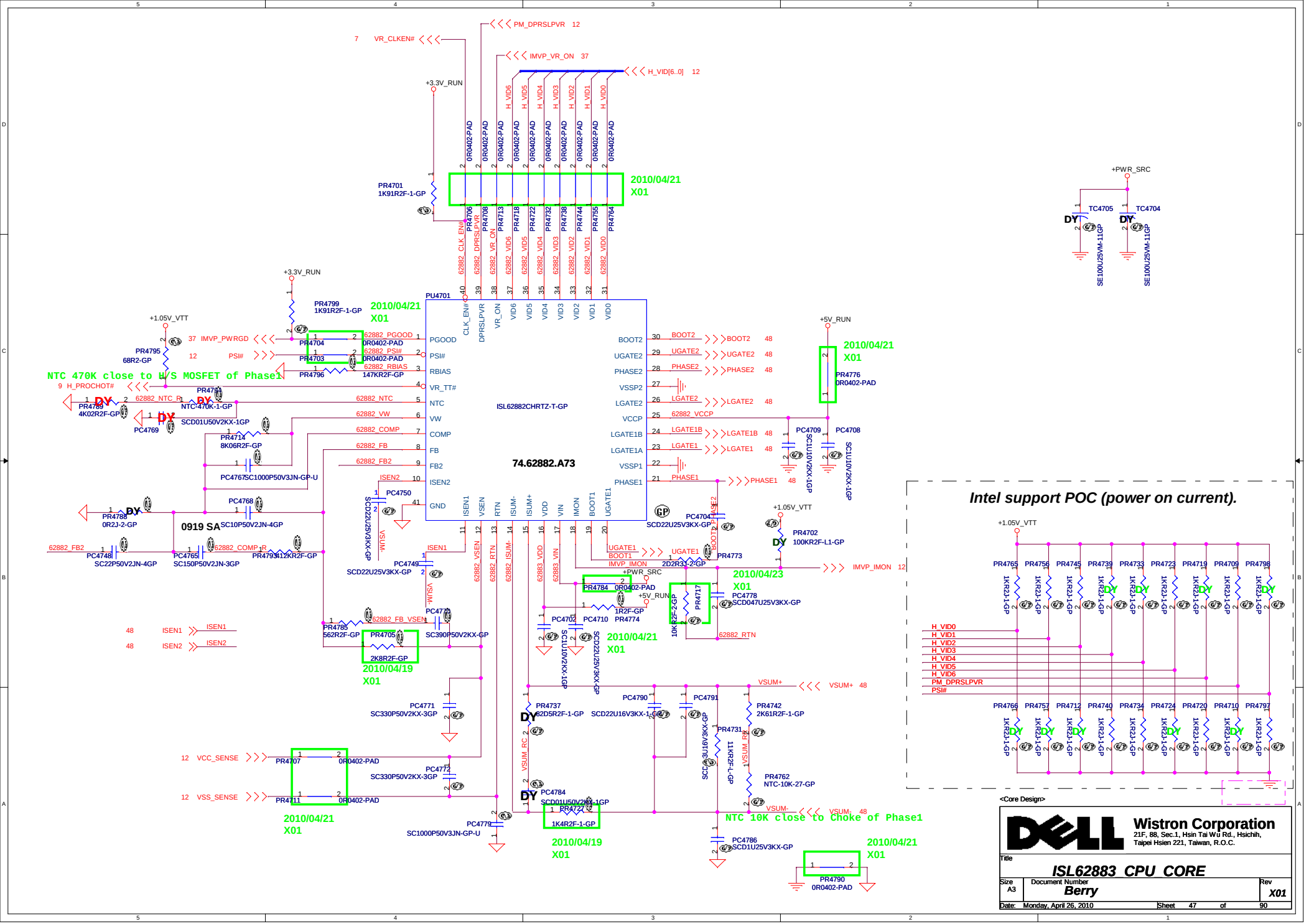
EN0	Open	820k to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

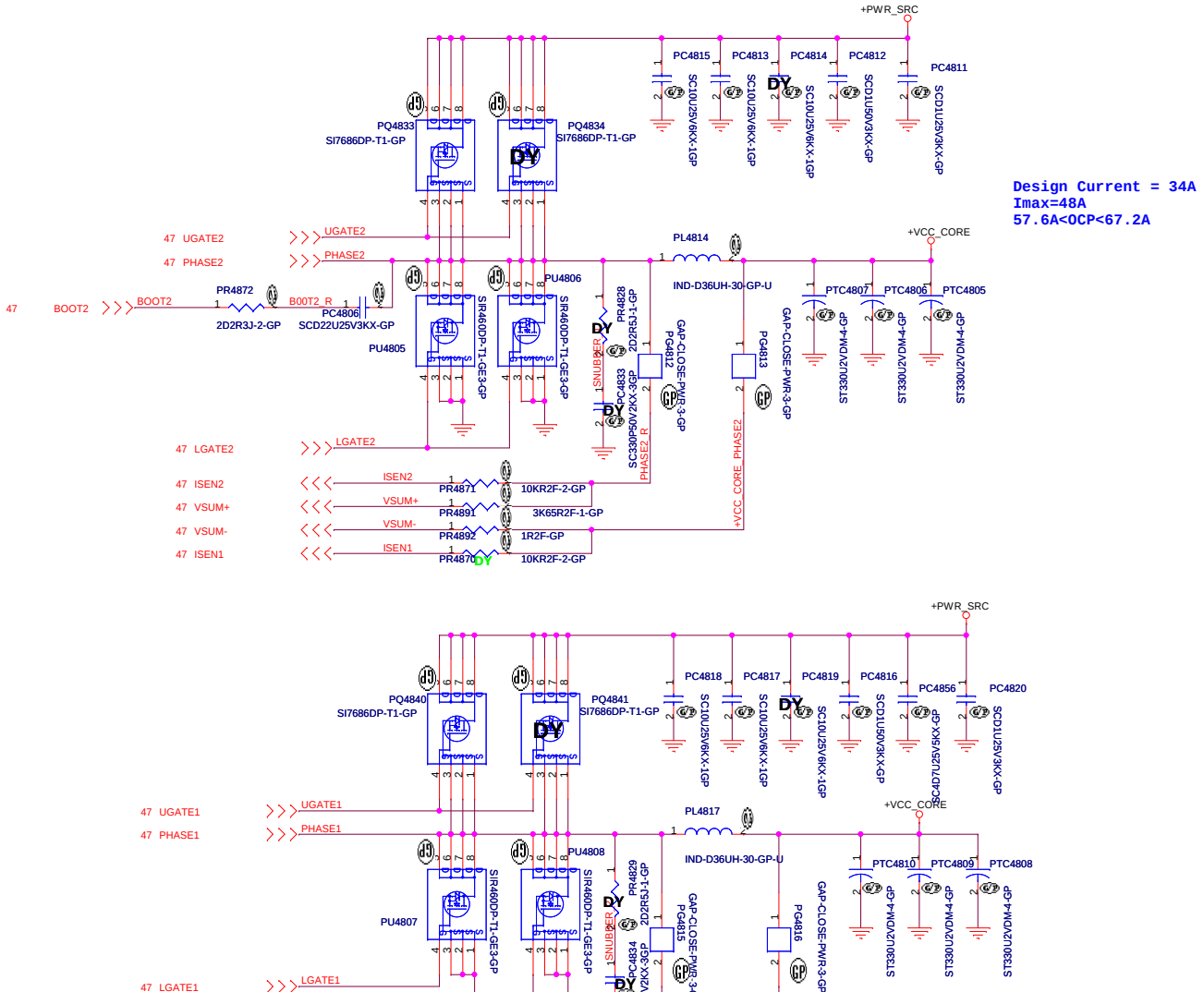
TPS51125:

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

RT8205B:

TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3	365kHz	460kHz
VREG5	365kHz	460kHz





I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.36UH PCMC104T-R36MN1R05J Cyntec 1.05mohm/ 68.R3610.20C
O/P cap: 330U 2V EEFSX0D331XE 6mOhm 3.4Arms Panasonic/79.33719.20L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

<Core Design>

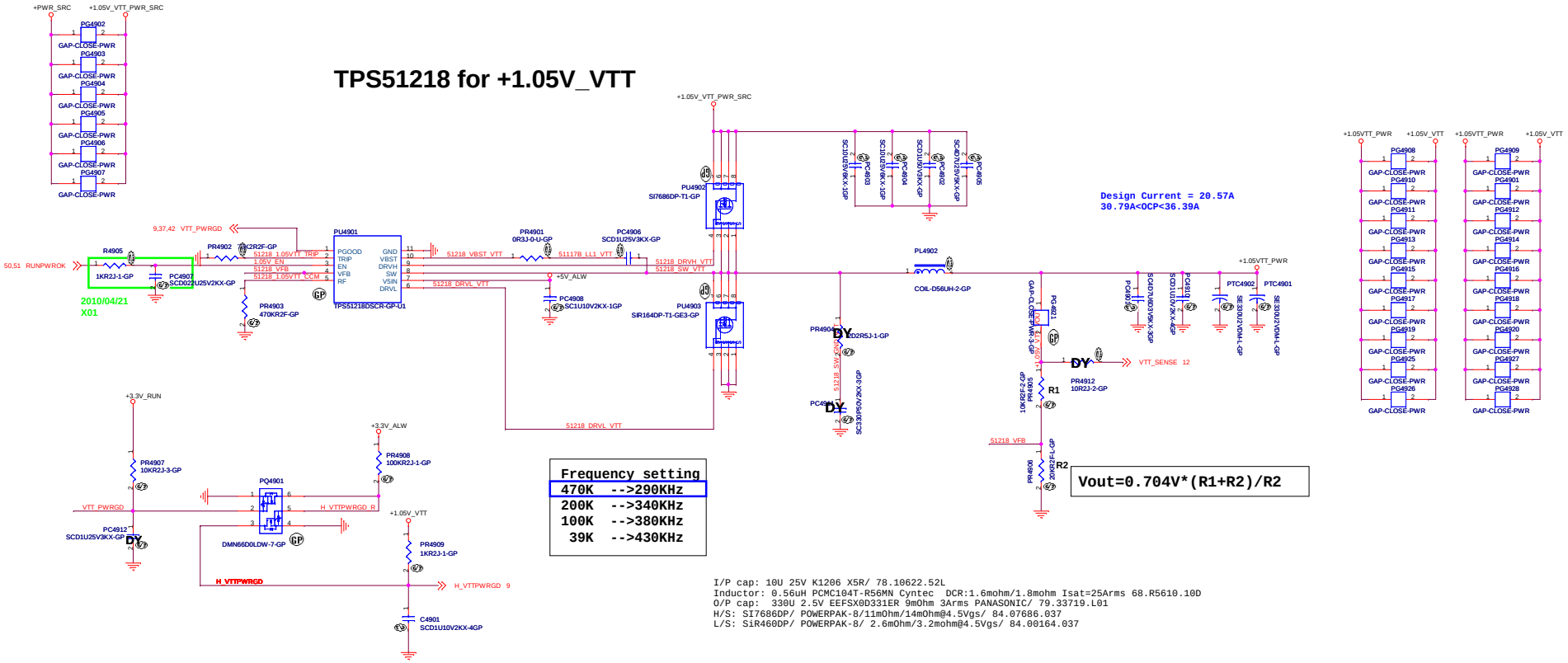
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL62883_CPU_CORE

Size	Document Number	Rev
A3	Berry	X01

Date: Thursday, April 22, 2010 Sheet 48 of 90

TPS51218 for +1.05V_VTT



Frequency setting
470K -->290KHz
200K -->340KHz
100K -->380KHz
39K -->430KHz

Vout=0.704V*(R1+R2)/R2

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.6mohm/1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2.5V EEFSX0D331ER 9mOhm 3Arms PANASONIC/ 79.33719.L01
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 2.6mOhm/3.2mohm@4.5Vgs/ 84.00164.037

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

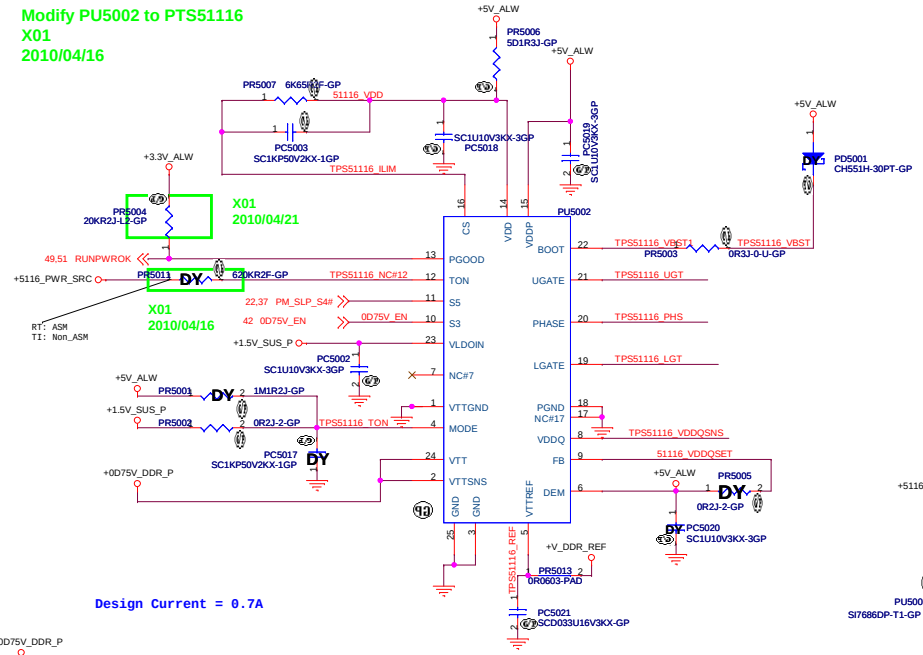
Title: TPS51218 +1.05V_VTT

Size	Document Number	Rev
A2	DJ1 Calpella UMA	X01

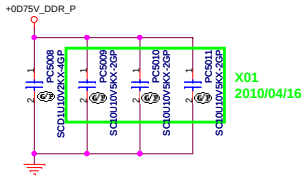
Date: Thursday, April 22, 2010 Sheet 49 of 90

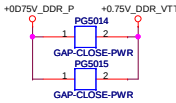
SSID = PWR.Plane.Regulator_1p5v0p75v

Modify PU5002 to PTS51116
X01
2010/04/16



Design Current = 0.7A

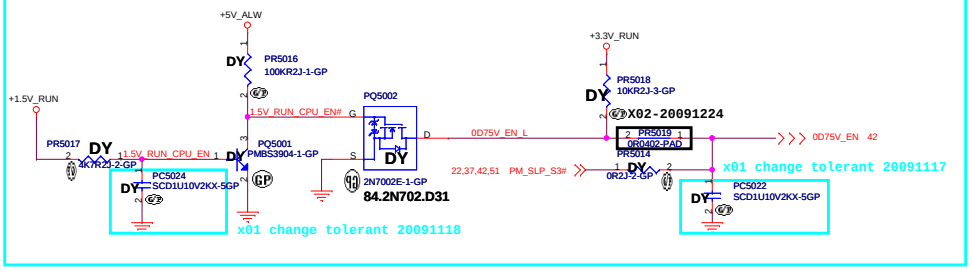


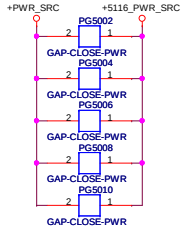


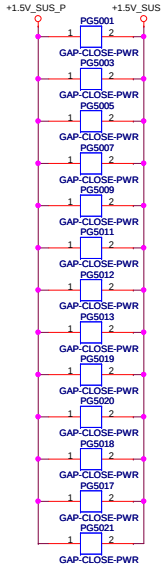
State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

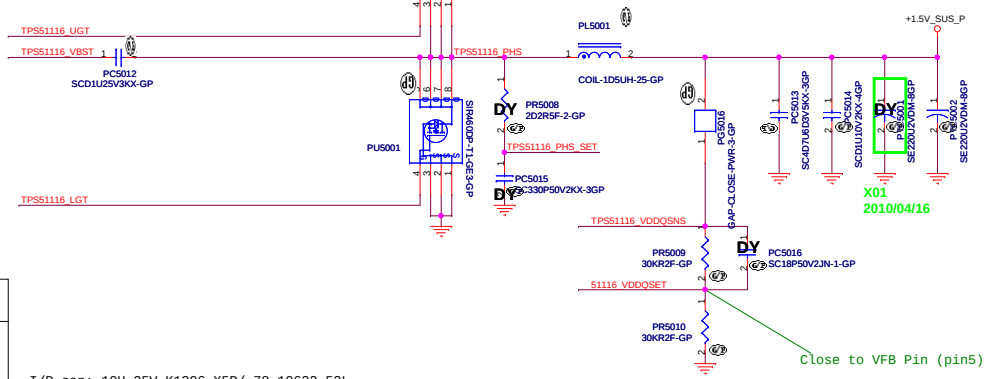
VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

S3 Power Reduction









I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5uH PCMC104T-1R5 Cyntec DCR:3.8mohm Isat=33Arms 68.1R510.10J
O/P cap: 220U 2V EEFCX0D221ER 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037
Switching freq-->400KHz

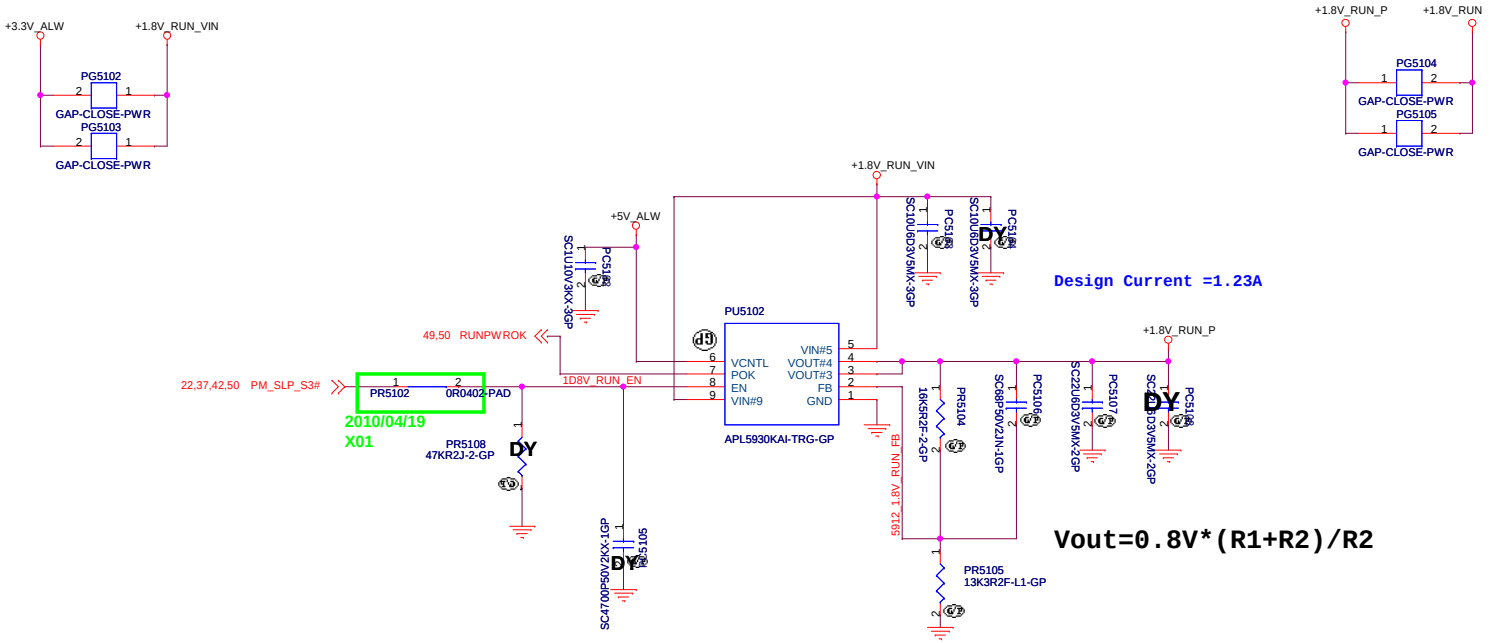
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51116_+1.5V_SUS
Size: Custom | Document Number: DJ1 Calpella UMA | Rev: X01
Date: Thursday, April 22, 2010 | Sheet 50 of 90

SSID = PWR.Plane.Regulator_1p8v

APL5930 for +1.8V_RUN



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	APL5930 +1.8V_RUN	
Size: A3	Document Number: DJ1 Calpella UMA	Rev: X01
Date: Thursday, April 22, 2010	Sheet 51 of 90	

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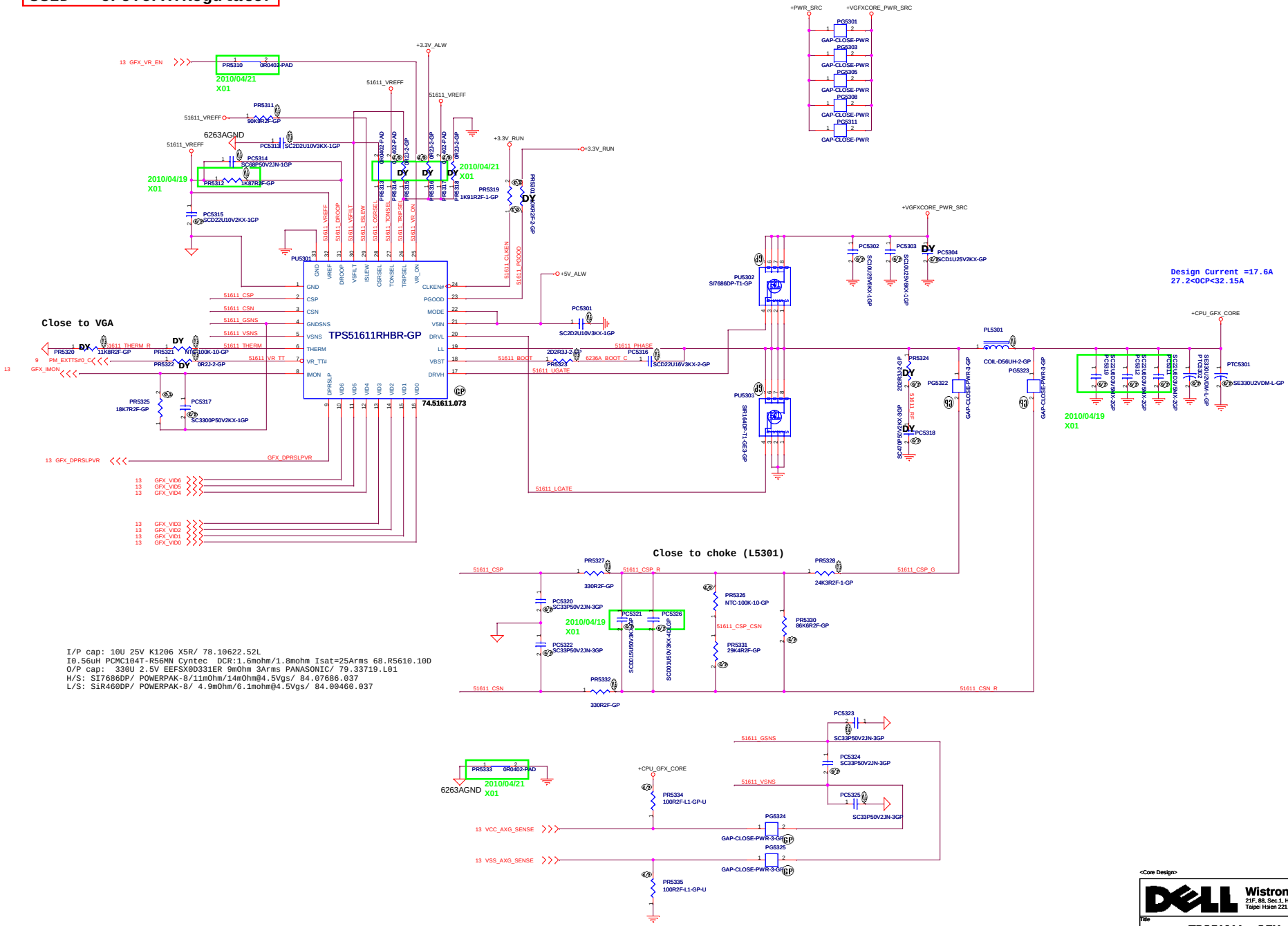
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Reserved	
Size: A3	Document Number: DJ1 Calpella UMA	Rev: X01
Date: Friday, April 16, 2010	Sheet 52 of 90	

SSID = CPU.GFX.Regulator



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

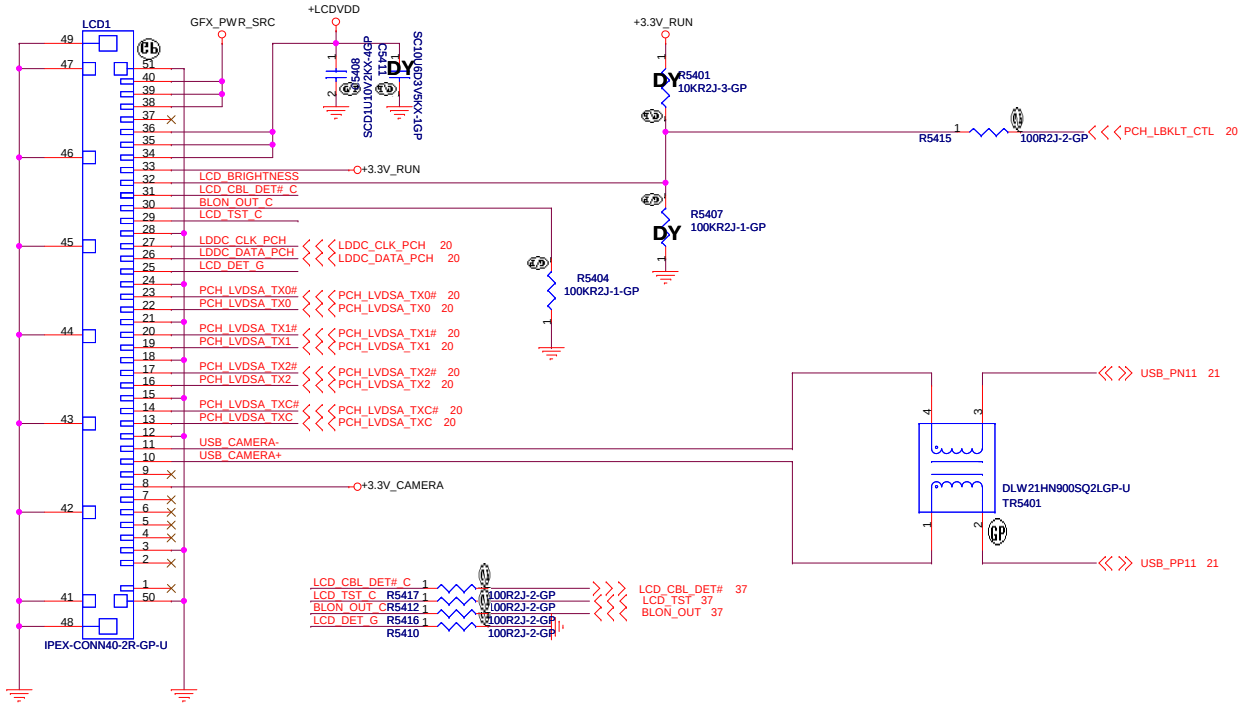
Title: TPS51611 +GFX_CORE

Size: A2 | Document Number: Arsenal DJ1 UMA | Rev: X01

Date: Thursday, April 22, 2010 | Sheet 53 of 90

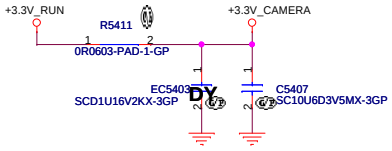
SSID = VIDEO

LVDS CONNECTOR



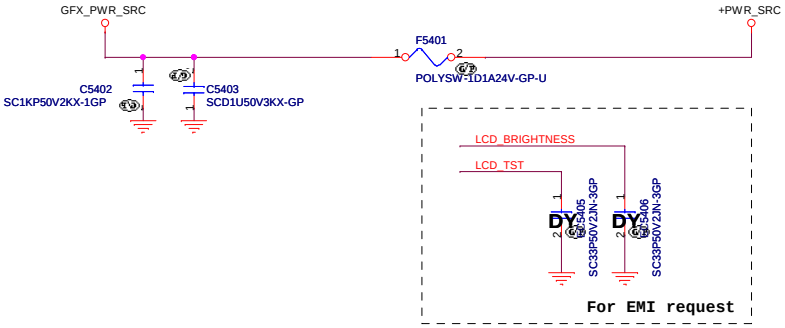
20.F1093.040

Camera Power



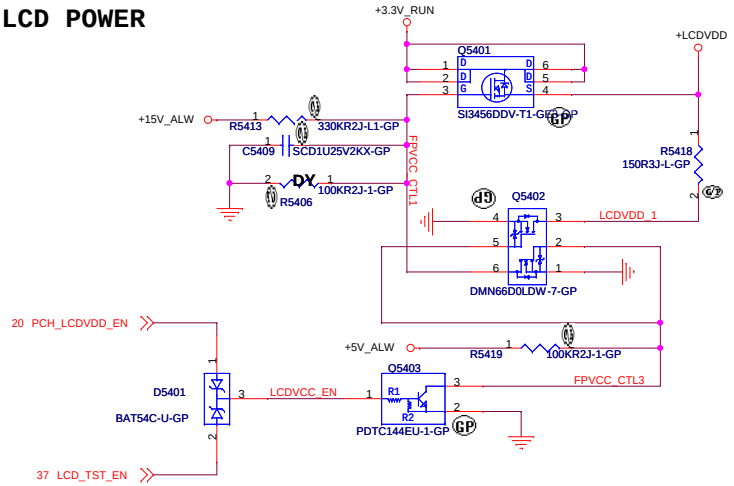
SSID = Inverter

INVERTER POWER



SSID = VIDEO

LCD POWER



<Core Design>

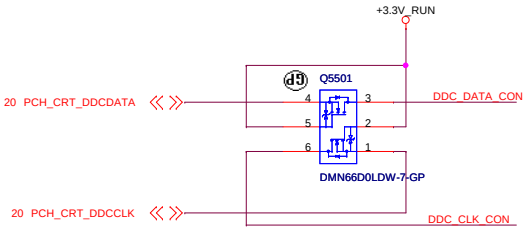
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

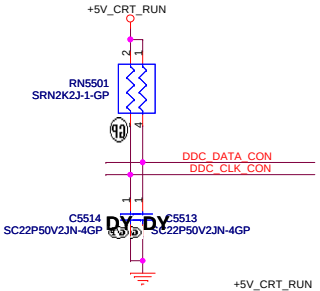
Title	LCD/Inverter Connector	
Size A3	Document Number DJ1 Calpella UMA	Rev X01
Date: Monday, April 26, 2010	Sheet 54 of 90	

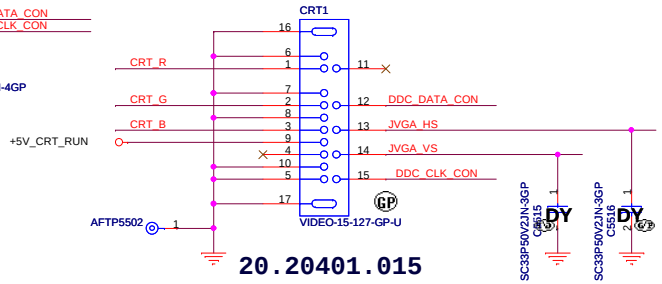
SSID = VIDEO

Layout Note:

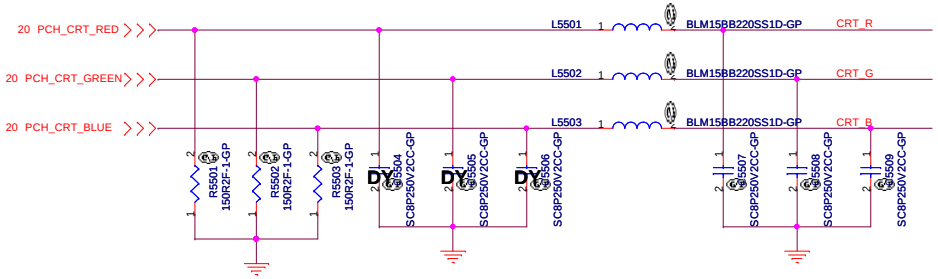
***Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.**
*** RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.**

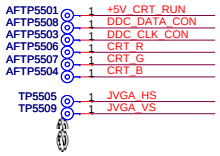




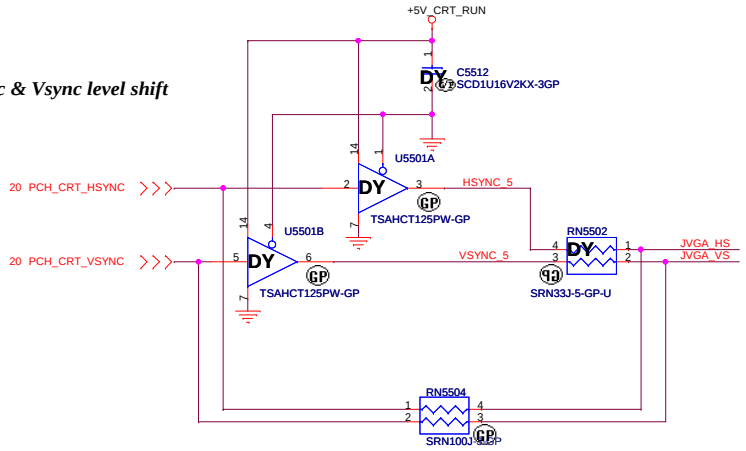


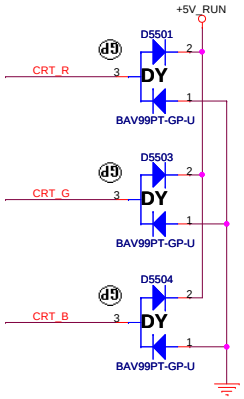
20.20401.015

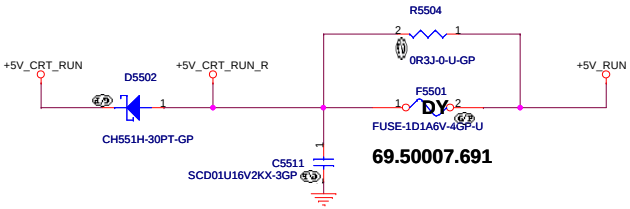




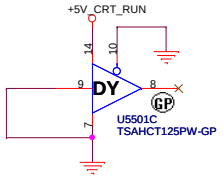
Hsync & Vsync level shift

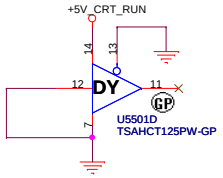






69.50007.691





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
CRT Connector		
Size	Document Number	Rev
	DJ1 Calpella UMA	X01
Date: Thursday, April 22, 2010	Sheet 55 of 90	

CLOSE TO TRANSFORMER

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: DJ1 Calpella UMA | Rev: X01

Date: Friday, April 16, 2010 | Sheet 56 of 90

(Blanking)

<Core Design>

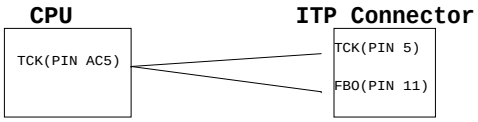
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	HDMI	
Size: A3	Document Number: DJ1 Calpella UMA	Rev: X01
Date: Friday, April 16, 2010	Sheet 57 of 90	

SSID = User.Interface

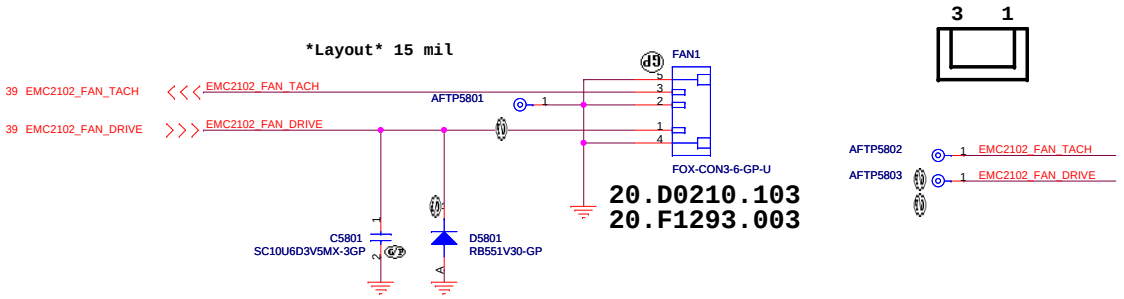
ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



SSID = Thermal

Fan Connector



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

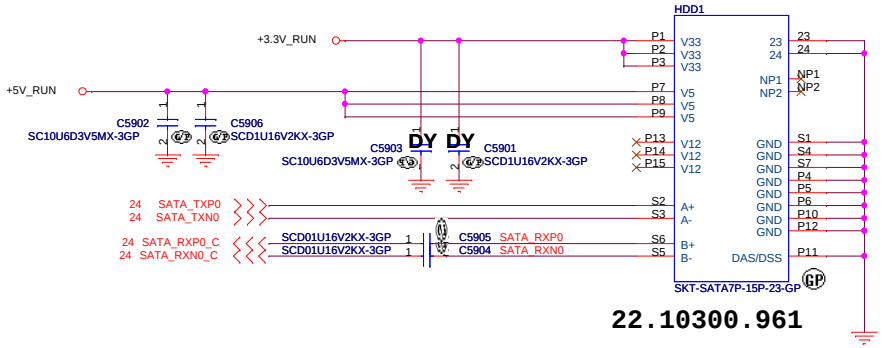
Title: ITP/Fan Connector

Size: A3 | Document Number: DJ1 Calpella UMA | Rev: X01

Date: Thursday, April 22, 2010 | Sheet 58 of 90

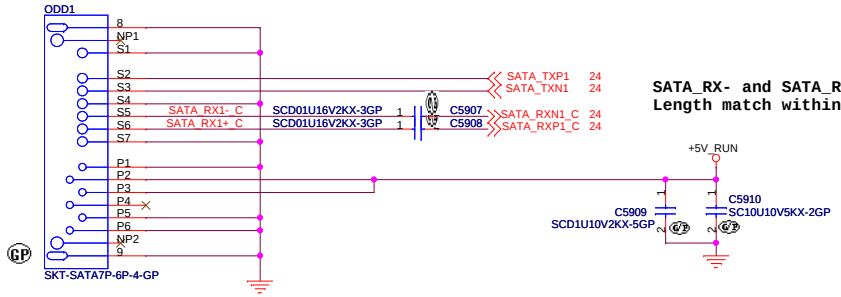
SSID = SATA

SATA HDD Connector



22.10300.961

ODD Connector



SATA_RX- and SATA_RX+ Trace Length match within 20 mil

22.10300.811
22.10300.421
22.10300.471

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

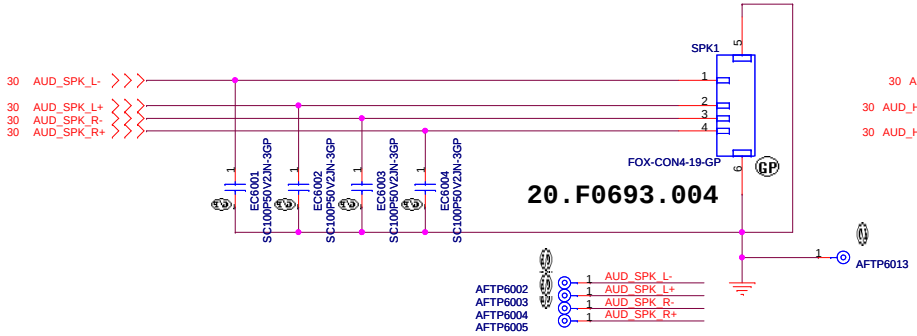
Size	Document Number	Rev
A3	DJ1 Calpella UMA	X01

Date: Thursday, April 22, 2010 Sheet 59 of 90

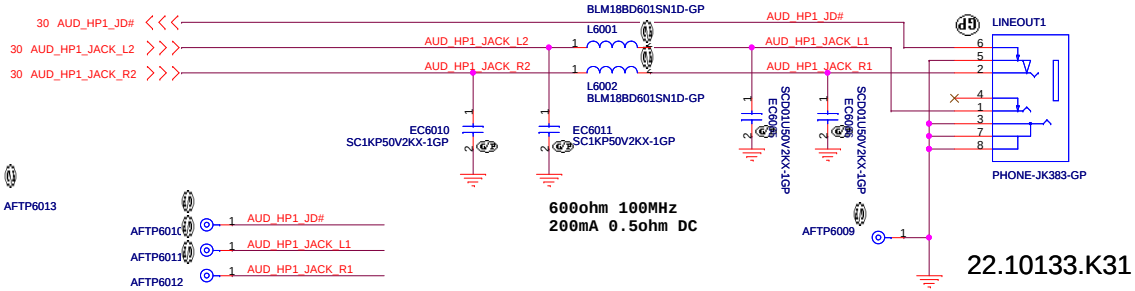
SSID = AUDIO

Speaker Connector

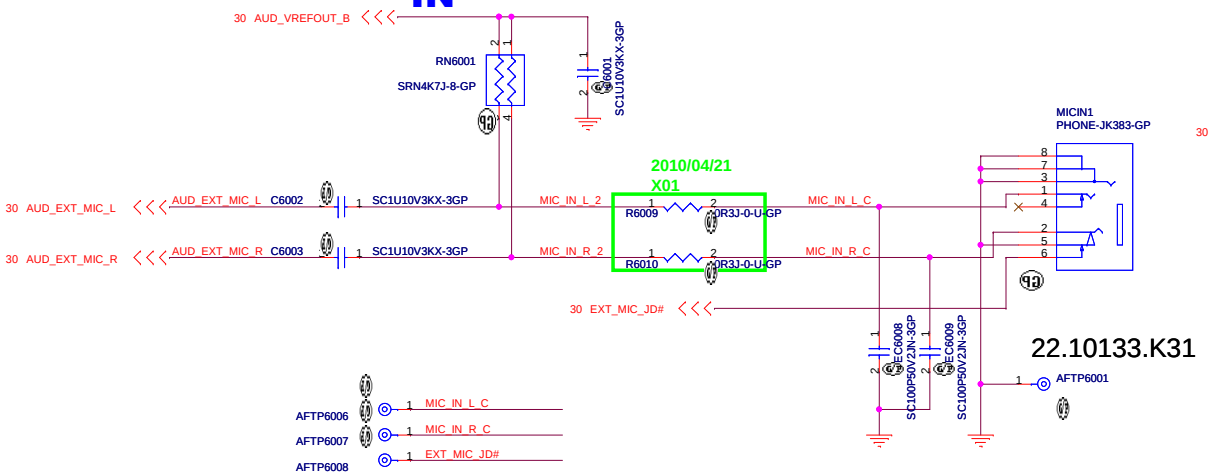
20.F0711.004



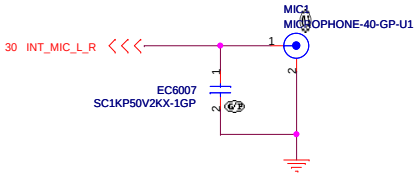
LINE1 OUT



MIC IN



Internal Microphone



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Audio Jack	
Size: A3	Document Number: DJ1 Calpella UMA	Rev: X01
Date: Thursday, April 22, 2010	Sheet 60 of 90	

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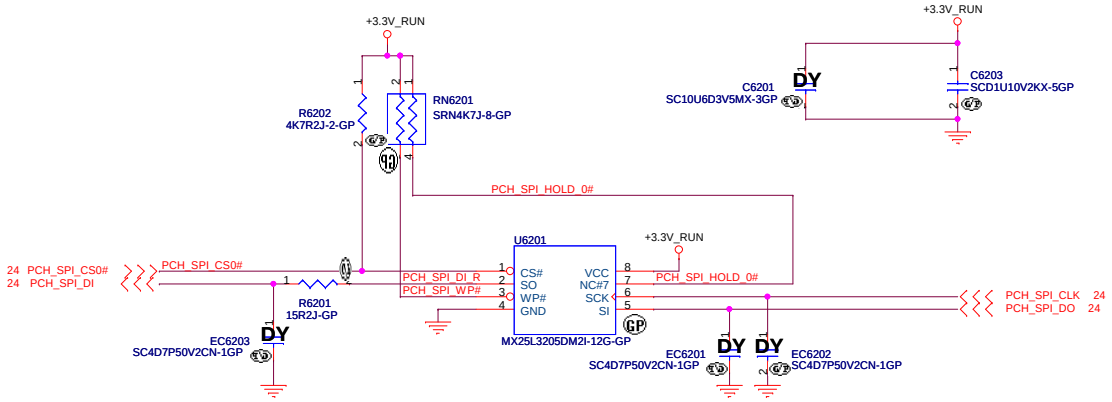
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

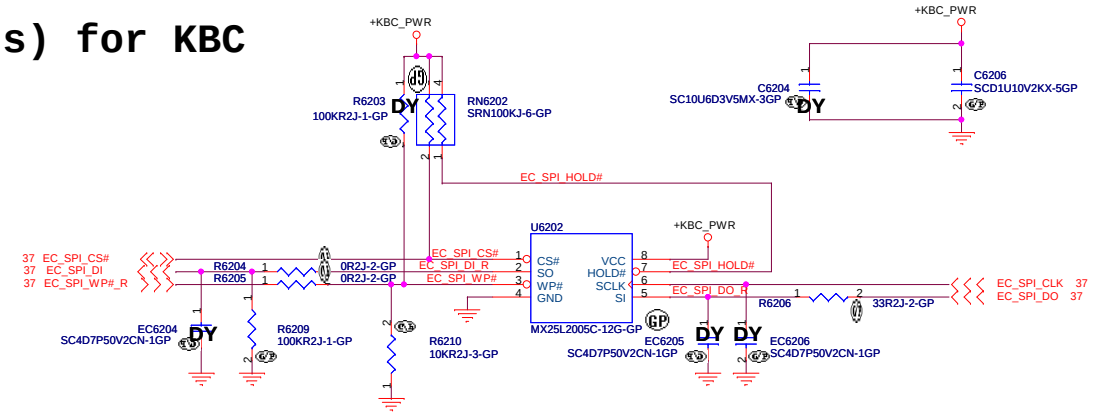
Title	Reserved	
Size: A3	Document Number: DJ1 Calpella UMA	Rev: X01
Date: Friday, April 16, 2010	Sheet 61 of 90	

SSID = Flash.ROM

SPI FLASH ROM (32M bits) for PCH

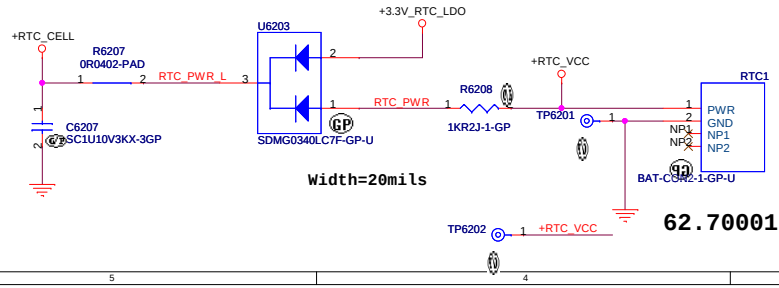


SPI FLASH ROM (2M bits) for KBC



SSID = RBATT

RTC Connector



62.70001.011

<Core Design>

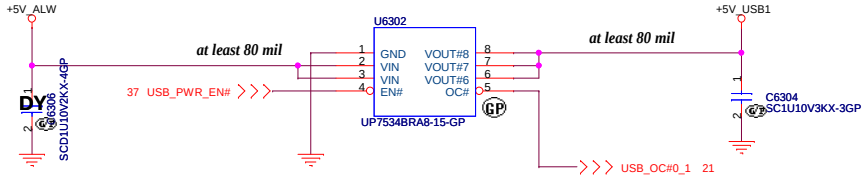
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Flash/RTC	
Size A3	Document Number DJ1 Calpella UMA	Rev X01
Date: Thursday, April 22, 2010	Sheet 62 of 90	

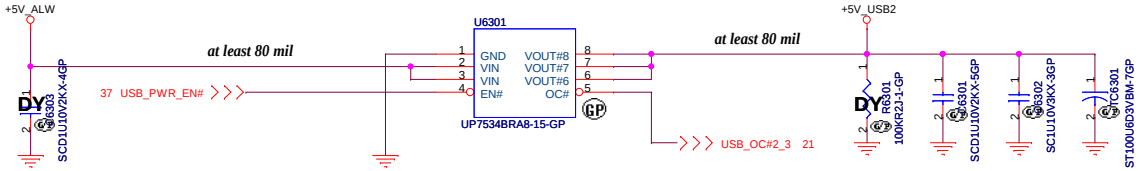
SSID = USB

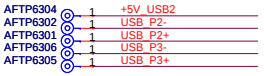
USB POWER SW
Main UP7534BRA8-15 P/N:74.07534.079
SEC AP2101MPG-13 P/N: 74.02101.079

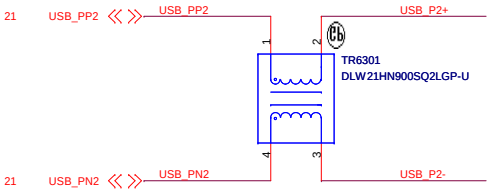
IO Board USB Power

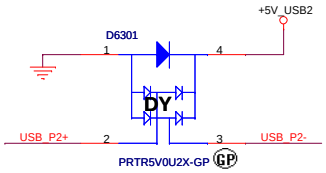


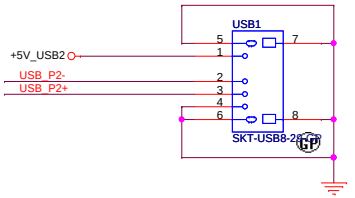
Right USB Power

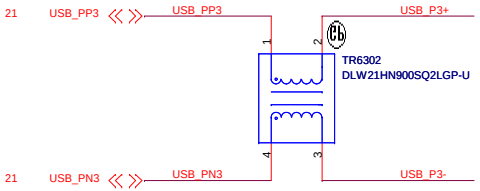


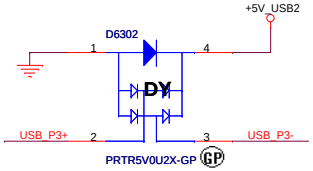


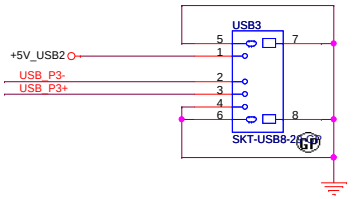












22.10254.451

<Core Design>

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Title: USB		
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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*		
Size: A3	Document Number: *DJ1 Calpella UMA*	Rev: *X01*
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<Core Design>

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Title: Reserved

Size: A3 | Document Number: DJ1 Calpella UMA | Rev: X01

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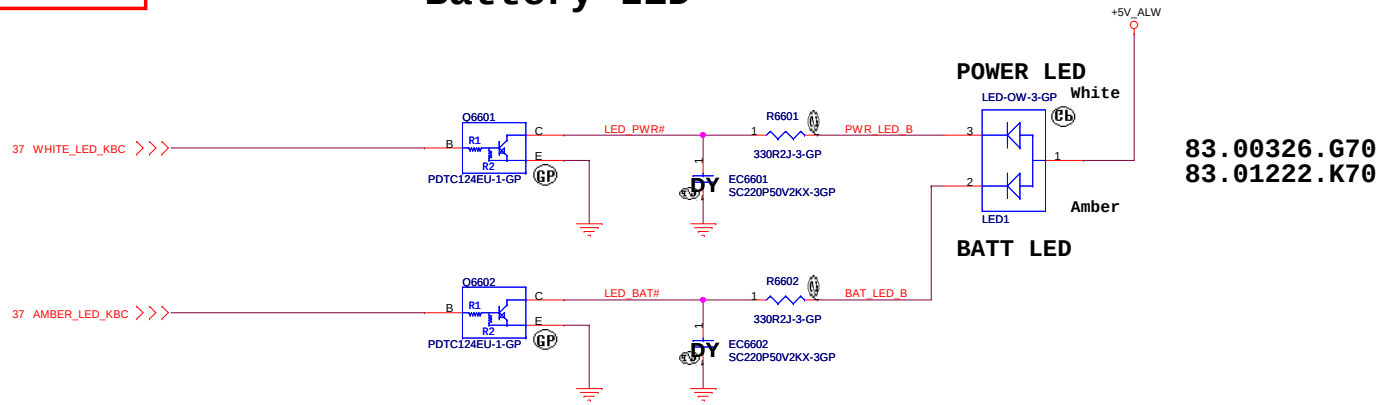
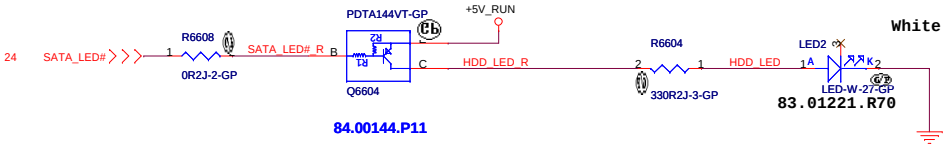
SSID = User.Interface

Battery LED



83.00326.G70
83.01222.K70

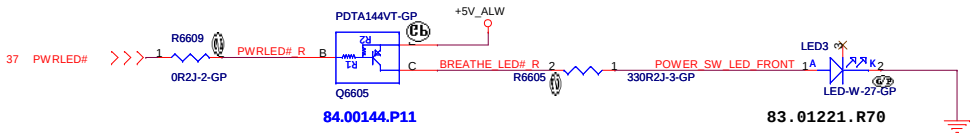
HDD LED



84.00144.P11

83.01221.R70

BREATHE PWR LED (Front)



84.00144.P11

83.01221.R70

<Core Design>

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Title	LED	
Size A3	Document Number DJ1 Calpella UMA	Rev X01
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<Core Design>

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Title: Reserved

Size: A3 | Document Number: DJ1 Calpella UMA | Rev: X01

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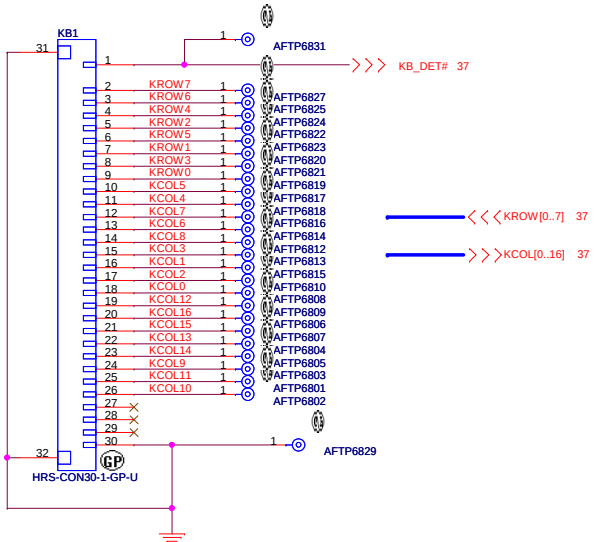
SSID = KBC

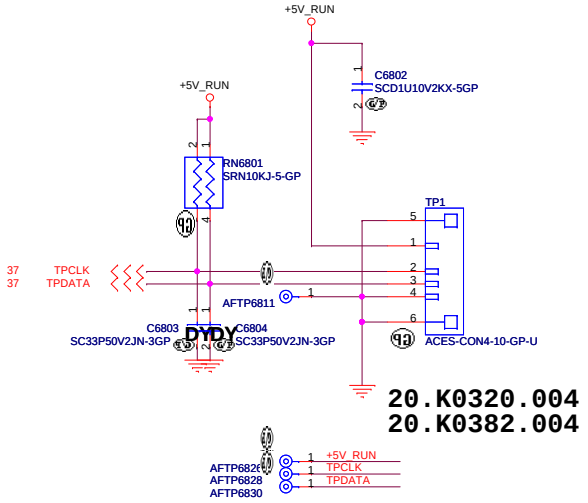
Internal KeyBoard Connector



Main 20.K0259.030
20.K0461.030
20.K0421.030

SSID = Touch.Pad

TouchPad Connector



20.K0320.004
20.K0382.004

<Core Design>

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Title	Key Board/Touch Pad	
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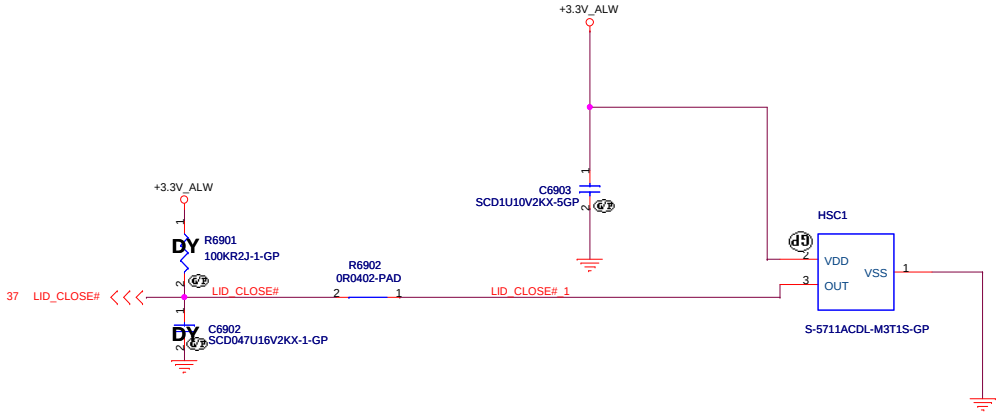

<Core Design>

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Title: Hall Sensor

Size	Document Number	Rev
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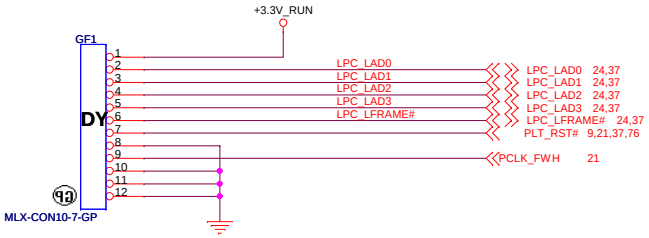

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Title: *Reserved*

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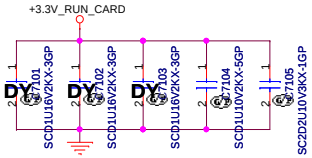
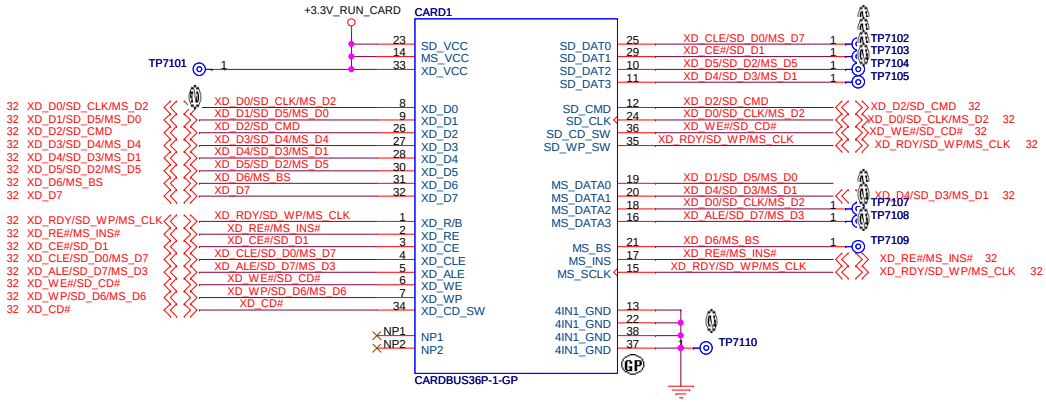
SSID = SDIO

SD/XD/MS Card Reader





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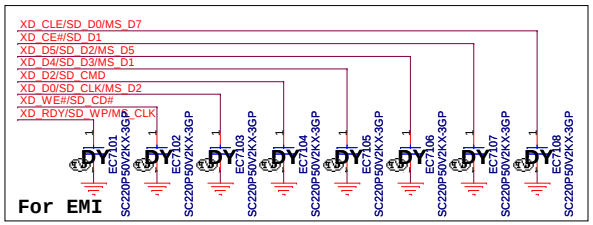

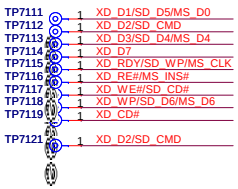

<Core Design>

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Title: CARD Reader CONN

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<Core Design>

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Title: RESERVED

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A3	DJ1 Calpella UMA	X01

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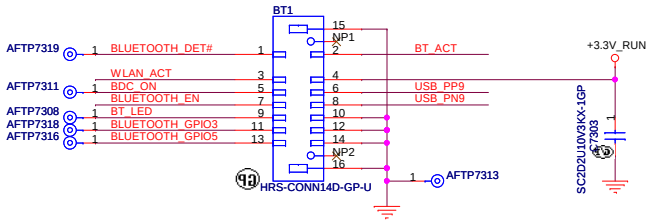
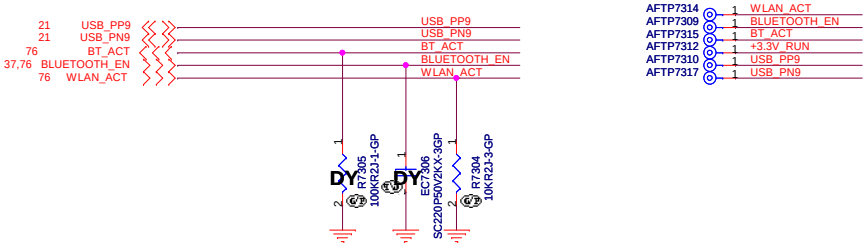
SSID = User.Interface

Bluetooth Module conn.



20.F0987.014



<Core Design>

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Title	Bluetooth	
Size A3	Document Number DJ1 Calpella UMA	Rev X01
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<Core Design>

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Title: Reserved

Size: A3 | Document Number: DJ1 Calpella UMA | Rev: X01

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<Core Design>

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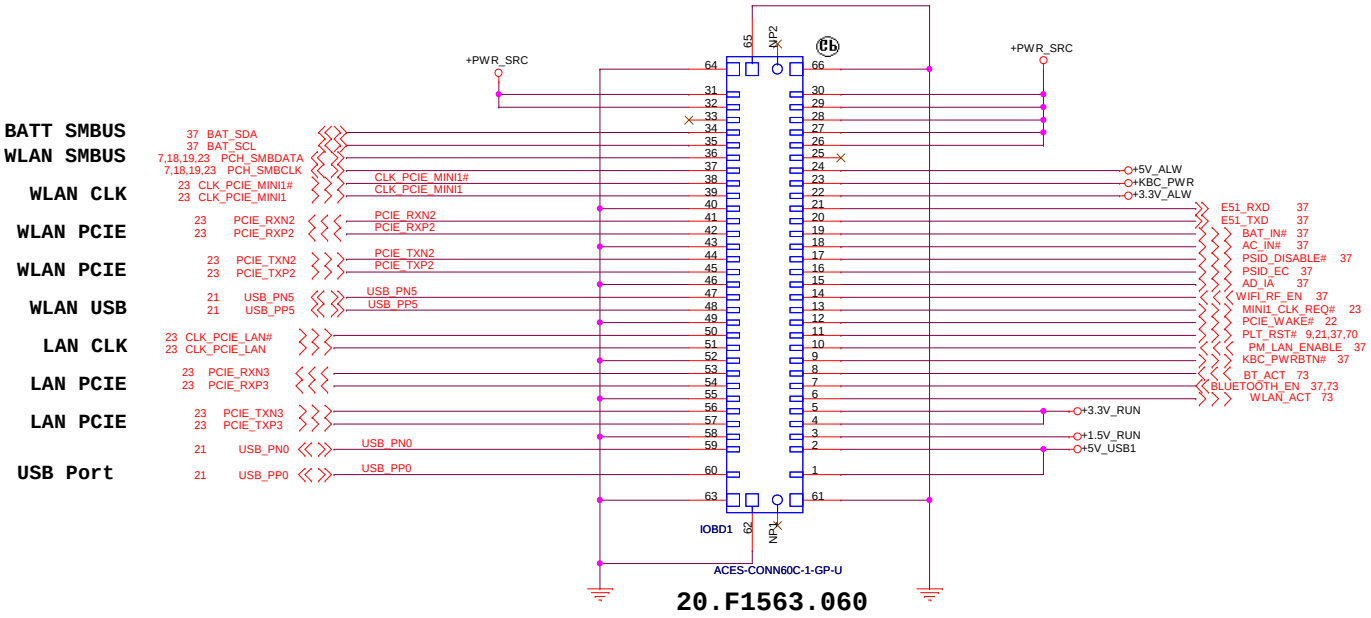
Title: Reserved

Size: A3 | Document Number: DJ1 Calpella UMA | Rev: X01

Date: Friday, April 16, 2010 | Sheet 75 of 90

SSID = PWR.Support



20.F1563.060

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *IO Board Connector*

Size: A3 | Document Number: *DJ1 Calpella UMA* | Rev: *X01*

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<Core Design>

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Title	Reserved	
Size: A3	Document Number: DJ1 Calpella UMA	Rev: X01
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<Core Design>

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SSID = Mechanical

2010/04/20
X01

+PWR_SRC

+3.3V_RUN

+3.3V_ALW

+5V_ALW

+1.8V_RUN

+1.05V_VTT

+1.5V_RUN

For Audio EMI
2010/04/19
X01

H1 HOLE355X355R111-S1-GP

H13 HT85BE95R29-U-5-GP

H4 HT85BE95R29-U-5-GP

H8 HOLE237R95-GP

H21 HOLE197R166-GP

H22 HOLE197R166-GP

H23 HOLE197R166-GP

H18 HOLE237R95-GP

H6 HT85BE95R29-U-5-GP

H7 HOLE355X355R111-S1-GP

H2 HT85BE95R29-U-5-GP

H3 HTE95BE95R29-R-5-GP

H20 HOLET315B236R95-GP

R7904 SCD1U25V2ZY-1GP

R7906 0R2J-2-GP

C7910 SCD1U25V2ZY-1GP

AUD_AGND

2010/04/19
X01

SPR1 SPRING-14-GP

SPR3 SPRING-51-GP

34.4F822.002

+3.3V_ALW

+1.05V_VTT

+PWR_SRC

+3.3V_RUN

+1.05V_VTT

+3.3V_RUN EC7970 +1.05V_VTT

SCD1U10V2KX-4GP

+3.3V_RUN EC7958 +3.3V_ALW

SCD1U10V2KX-4GP

+1.8V_RUN

+5V_ALW

+1.8V_RUN EC7967 +5V_ALW

SCD1U10V2KX-4GP

2010/04/20
X01

+1.8V_RUN EC7963 +1.05V_VTT

SCD1U10V2KX-4GP

+PWR_SRC EC7962 +3.3V_RUN

SCD1U25V2ZY-1GP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: UNUSED PARTS/EMI Capacitors

Size: A3 | Document Number: DJ1 Calpella UMA | Rev: X01

Date: Thursday, April 22, 2010 | Sheet 79 of 90

SSID = VIDEO

<Core Design>

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Title: *Reserved*		
Size: A3	Document Number: *DJ1 Calpella UMA*	Rev: X01
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<Core Design>

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Title: *Reserved*

Size	Document Number	Rev
C	*DJ1 Calpella UMA*	*X01*

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: Reserved

Size	Document Number	Rev
A2	DJ1 Calpella UMA	X01

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title
Reserved

Size	Document Number	Rev
C	*DJ1 Calpella UMA*	*X01*

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: Custom | Document Number: DJ1 Calpella UMA | Rev: X01

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Reserved

Size	Document Number	Rev
Custom	*DJ1 Calpella UMA*	*X01*

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *DJ1 Calpella UMA* | Rev: *X01*

Date: Friday, April 16, 2010 | Sheet 86 of 90

<Core Design>

Wistron Corporation
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Title: Reserved

Size: A3 | Document Number: DJ1 Calpella UMA | Rev: X01

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<Core Design>

Wistron Corporation
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Title: Reserved

Size	Document Number	Rev
C	DJ1 Calpella UMA	X01

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Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
1	46	2010/04/16	Power team	PU4603 (RT8205) shortage risk	Change to TPS51125	X01
2	50	2010/04/16	Power team	PU5002 (RT8207) shortage risk	Change to TPS51116, DY PR5011	X01
3	49	2010/04/16	EE	PM_PWROK to +1.05V_VTT power down sequence out of SPEC	Modify PC4907=0.022U,PR5004, add R4905=1K	X01
4	55	2010/04/16	EE	For SIV CRT test fail item	Modify RN5504=100 Ohm	X01
5	50	2010/04/16	Power team	Cost down	DY PTC5001	X01
6	53/13	2010/04/19	Power team	Power team request	Change PC5321=0.015U, PC5326=0.01U, PR5312 Mount PC5319,PC5312,PC5311,C1325,C1328,C1323	X01
7	47/12	2010/04/19	Power team	Power team request	Modify PR4705=2,8K, PR4727=1.4K Mount C1214=C1236=C1241=C1208=C1231=10U	X01
8	79	2010/04/19	ME	For EMI	Add SPR1	X01
9	79	2010/04/21-22	EMC	For EMI	Add EC7972-EC7981(DY) Mount EC7938,EC7947,EC7954	X01
10	26/37/47 /51/53/	2010/04/21	EE	Cost down	Change 0 Ohm resistance to 0 Ohm pad: R2611,R2603,L3701,PR4706,PR4708,PR4713,PR4718, PR4722,PR4732,PR4738,PR4744,PR4755,PR4764, PR4707,PR4711,PR4776,PR4784,PR4703,PR4704, PR4790,PR5102,PR5310,PR5313,PR5314,PR5317, PR5333	X01
11	60	2010/04/21	EE	for audio vender's segguest	Modify R6009,R6010 to 0 Ohm resistances	X01
12	37	2010/04/21	EE	For version ID	Mount R3722, DY R3725	X01
13	46	2010/04/22	Power team	For power snubber	Mount PR4606=PR4607=2R2, PC4620=330P, PC4621=680P	X01
14	46	2010/04/22	Power team	For OCP	Modify PR4603=140K	X01
15	47	2010/04/23	Power team	For power snubber	Modify PR4717=10K	X01

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Title: Change History

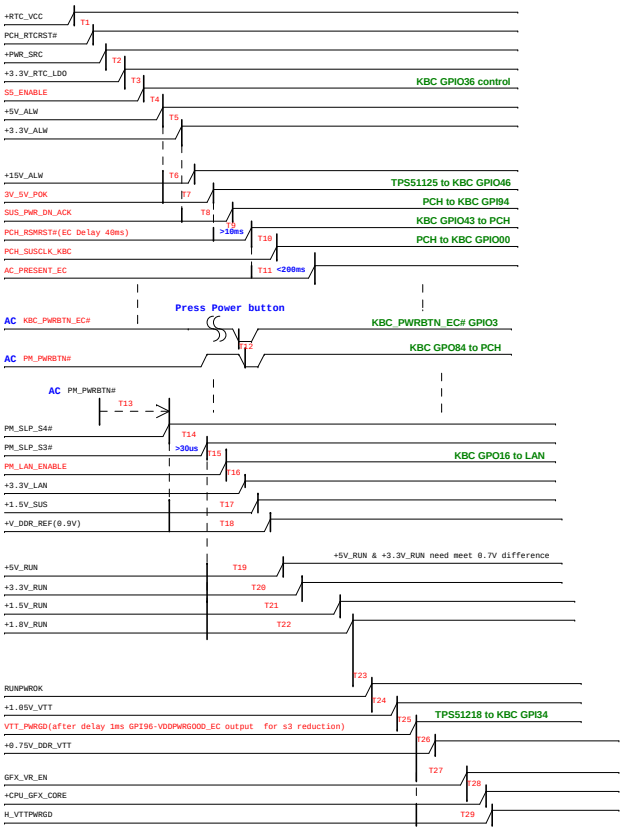
Size: A3 | Document Number: DJ1 Calpella UMA | Rev: X01

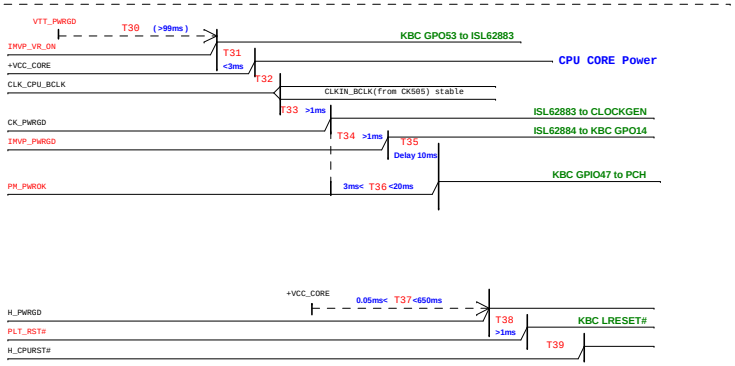
Date: Monday, April 26, 2010 | Sheet 89 of 90

DJ1 Calpella UMA-Power Up Sequence

(AC mode)

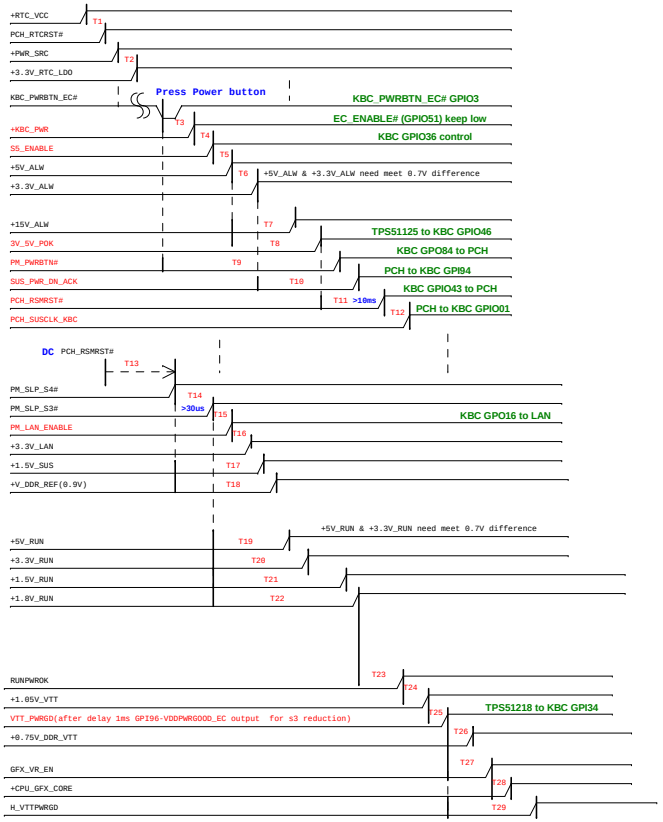
red word: KBC GPIO

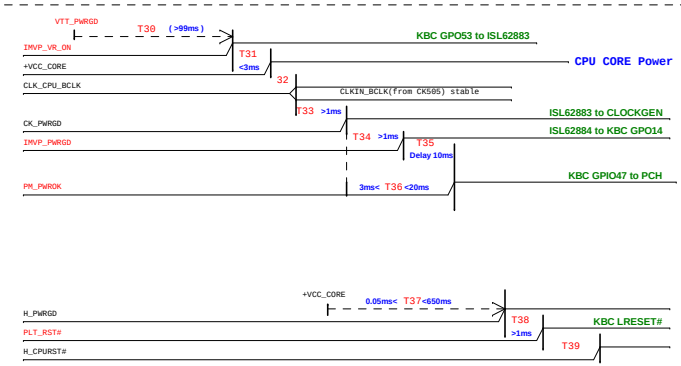




(DC mode)

red word: KBC GPIO





<Core Design>

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Title: Power Sequence

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A1	DJ1 Calpella Discrete	X01

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