

Schematics Page Index (Title / Revision / Change Date)

Page	Title of Schematics Page	Rev.	Date	Page	Title of Schematics Page	Rev.	Date
01	Schematics Page Index	1.0	07/28	36	AUDIO (MUTE)	1.0	07/28
02	Block Diagram	1.0	07/28	37	EXPRESS CARD/MDC	1.0	07/28
03	Yonah(HOST BUS) 1/2	1.0	07/28	38	PCI (PCI BUS)	1.0	07/28
04	Yonah(HOST BUS) 2/3	1.0	07/28	39	PCI (ILINK)	1.0	07/28
05	Yonah(Power/Gnd) 3/3	1.0	07/28	40	PCI (MS-DUO/MDC)	1.0	07/28
06	CALISTOGA (HOST) 1/7	1.0	07/28	41	Button/LID Switch/EMI CAP	1.0	07/28
07	CALISTOG (DMI) 2/7	1.0	07/28	42	USB2.0	1.0	07/28
08	CALIST (GRAPHIC) 3/7	1.0	07/28	43	HOLE	1.0	07/28
09	CALISTOGA (DDR2) 4/7	1.0	07/28	44	Power Design Diagram	1.0	07/28
10	CALIST (POWER,VCC) 5/7	1.0	07/28	45	DCIN&Charger	1.0	07/28
11	CALIST (VCC CORE) 6/7	1.0	07/28	46	SYS Power (+3_3V/+5V)	1.0	07/28
12	CALIST (VSS) 7/7	1.0	07/28	47	SYS Power(+1_5V/+1_05V)	1.0	07/28
13	DDR2(S0-DIMM_0) 1/3	1.0	07/28	48	DDR2 Power(+1_8V/+0_9V)	1.0	07/28
14	DDR2(S0-DIMM_1) 2/3	1.0	07/28	49	CPU_Vcore ---MAX8771	1.0	07/28
15	DDR2(Termination) 3/3	1.0	07/28	50	Others power plan	1.0	07/28
16	LVDS	1.0	07/28	51	OVP protection	1.0	07/28
17	CRT	1.0	07/28	52	History (1)	1.0	07/28
18	LAN CONTROLL	1.0	07/28	53	History (2)	1.0	07/28
19	LAN TRANSFORMER	1.0	07/28	54			
20	CLOCK GEN	1.0	07/28	55			
21	ICH7-M(PCI/USB) 1/5	1.0	07/28	56			
22	ICH7-M(LPC,IDE,SATA)2/5	1.0	07/28	57			
23	ICH7-M(GPIO) 3/5	1.0	07/28	58			
24	ICH7-M(POWER) 4/5	1.0	07/28	59			
25	ICH7-M(GND) 5/5	1.0	07/28	60			
26	SATA HDD/CD-ROM	1.0	07/28				
27	EC+KBC	1.0	07/28				
28	Flash ROM/X-Bus	1.0	07/28				
29	LED/Touch PAD	1.0	07/28				
30	Mini-PCIE Card	1.0	07/28				
31	FAN	1.0	07/28				
32	OIDE	1.0	07/28				
33	AUDIO(CODEC & POWER)	1.0	07/28				
34	AUDIO(AMP & HP & SPK)	1.0	07/28				
35	AUDIO(EXTMIC)	1.0	07/28				

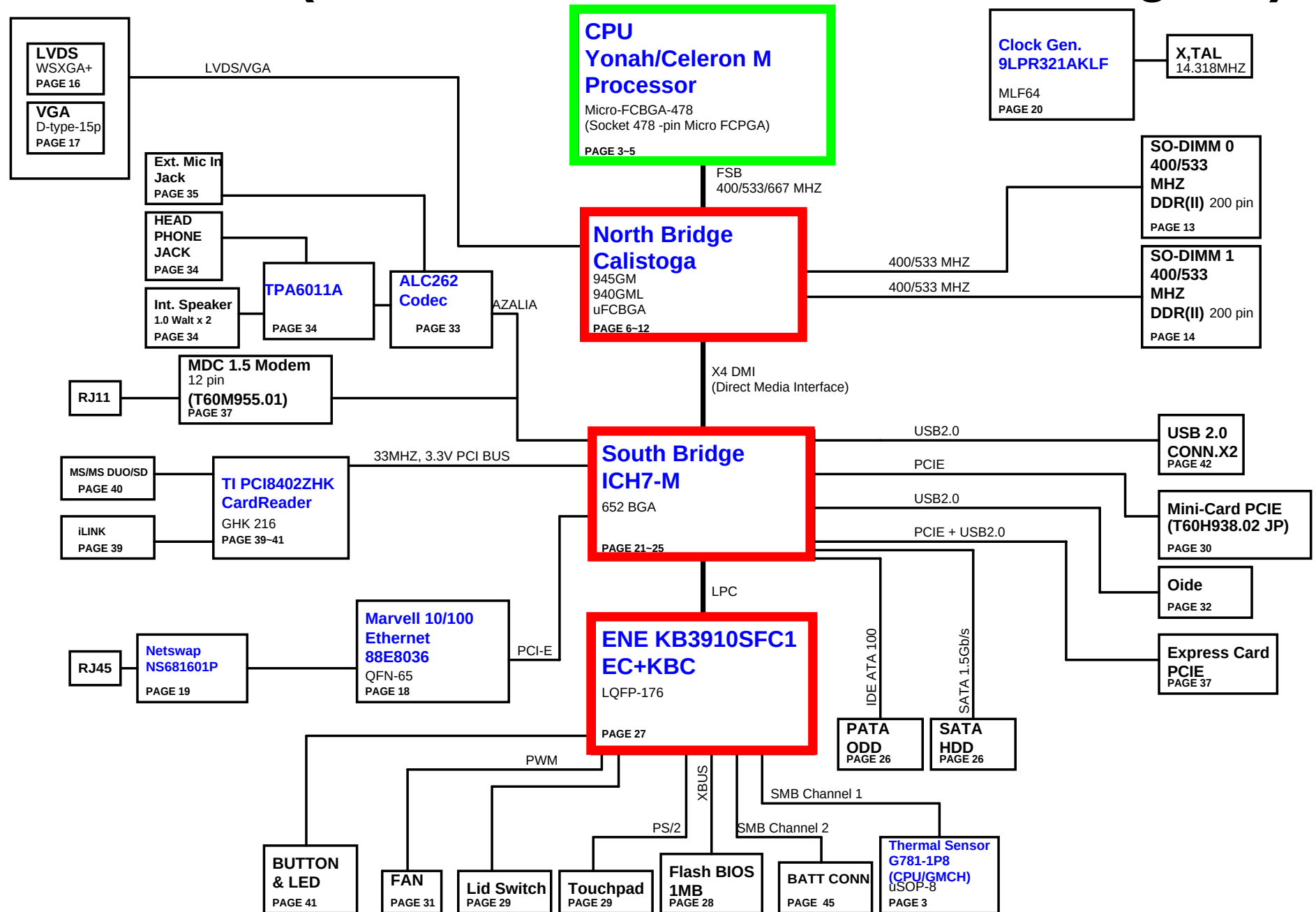
P. Leader	Check by	Design by

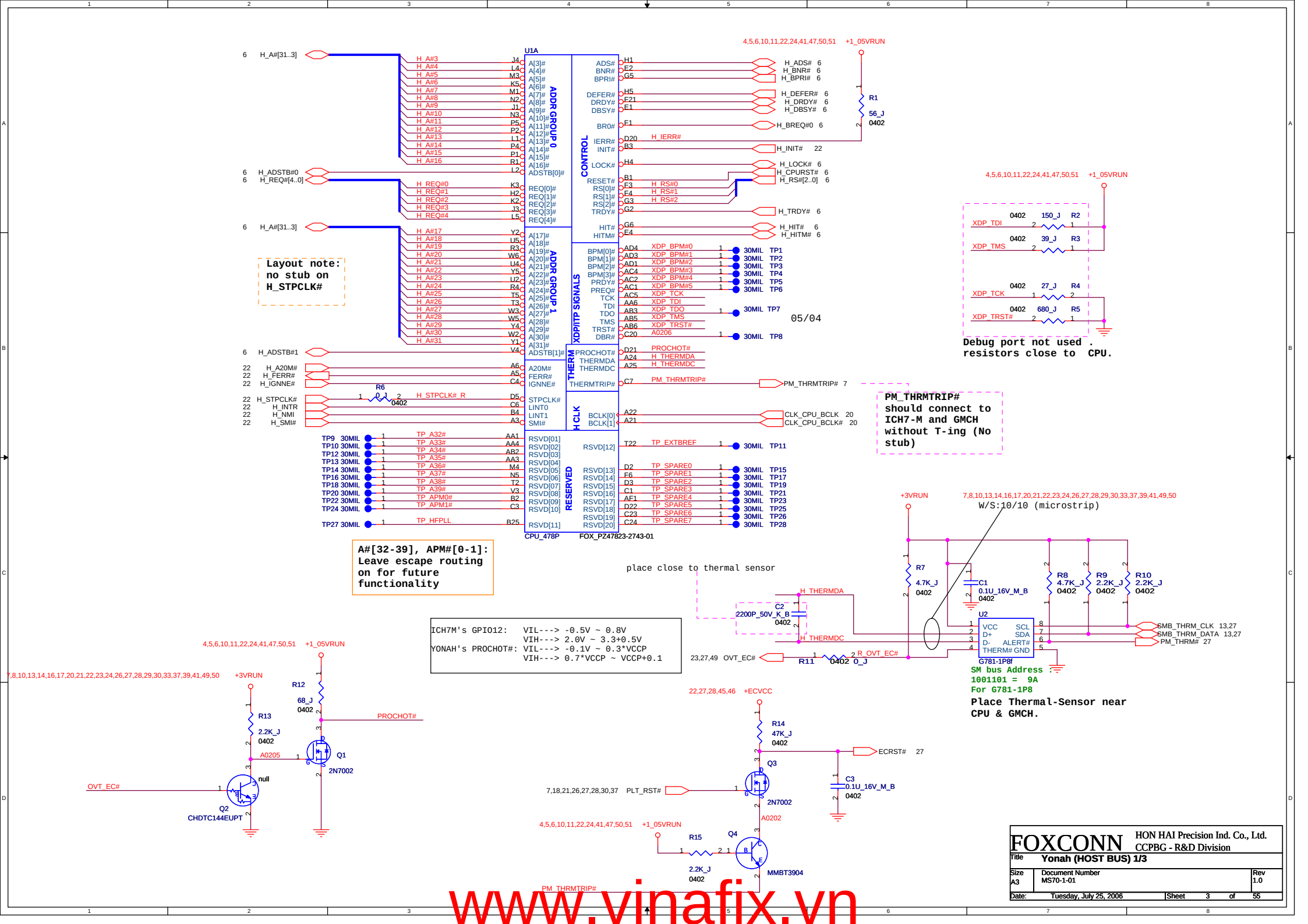
Project Code & Schematics Subject: MS70 Main Board

PCB P/N: (FUBAI) 1P-0067100-6010
(NAN YA) 1P-0067200-6010
(HANSTAR) 1P-0067500-6010

FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title Index Page			
Size A3	Document Number MS70-1-01	Rev 1.0	
Date: Tuesday, July 25, 2006	Sheet 1	of 55	

RAPTOR/MS70(CALISTOGA GM/GML Block Diagram)





Layout note:
no stub on
H_STPCLK#

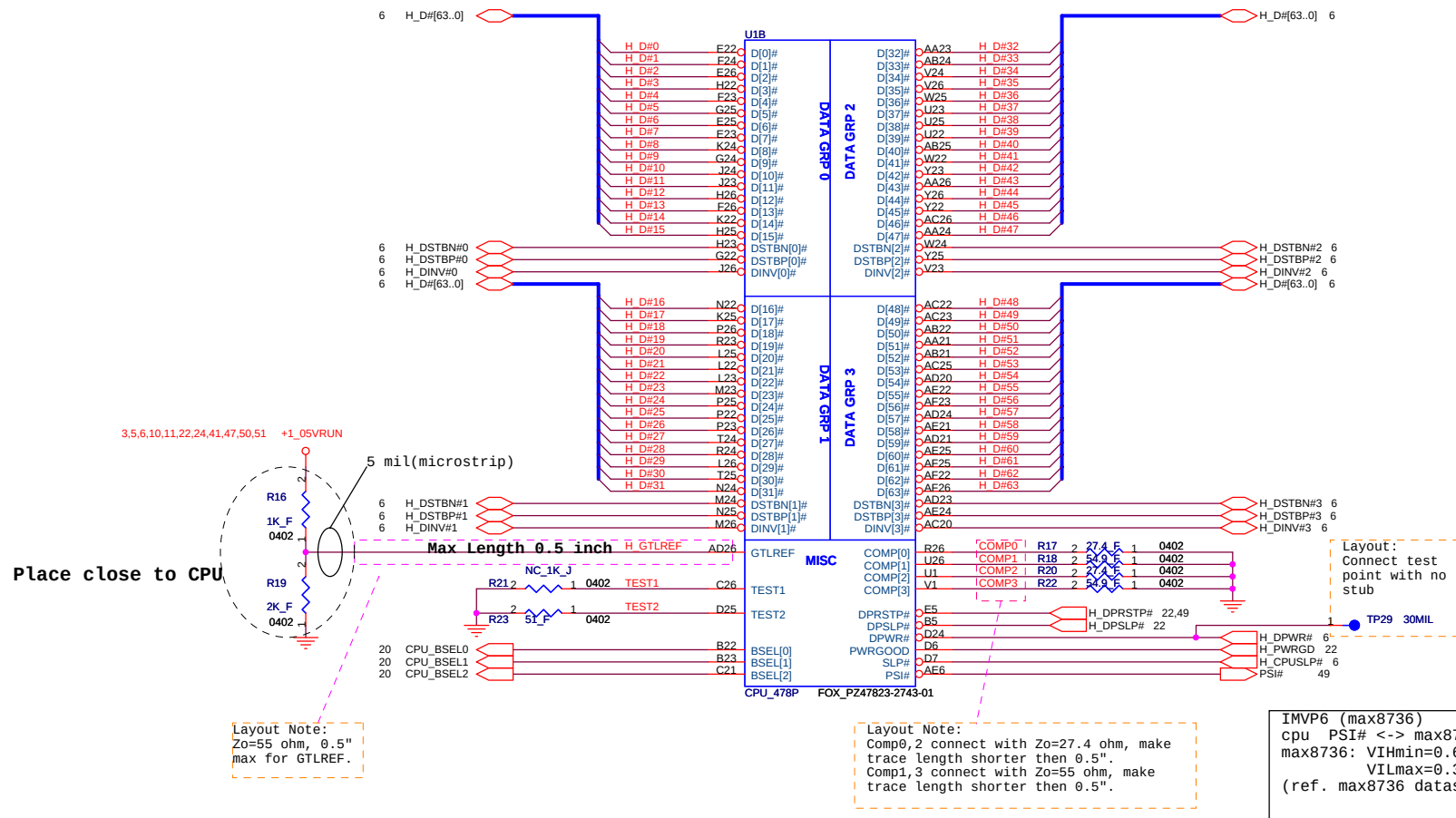
A#[32-39], APM#[0-1]:
Leave escape routing
on for future
functionality

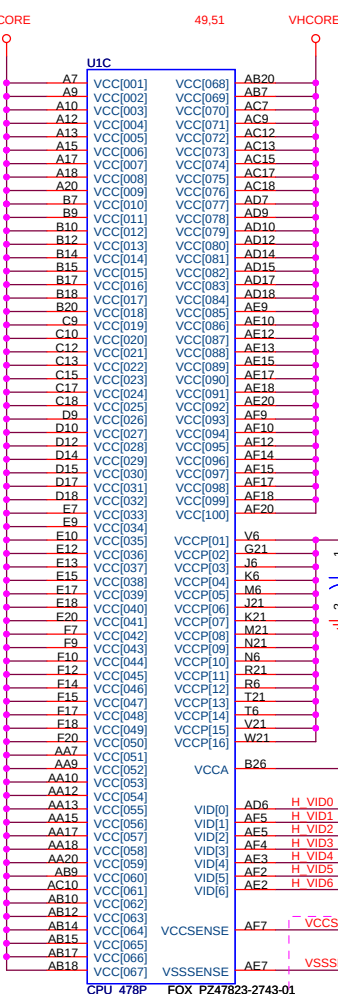
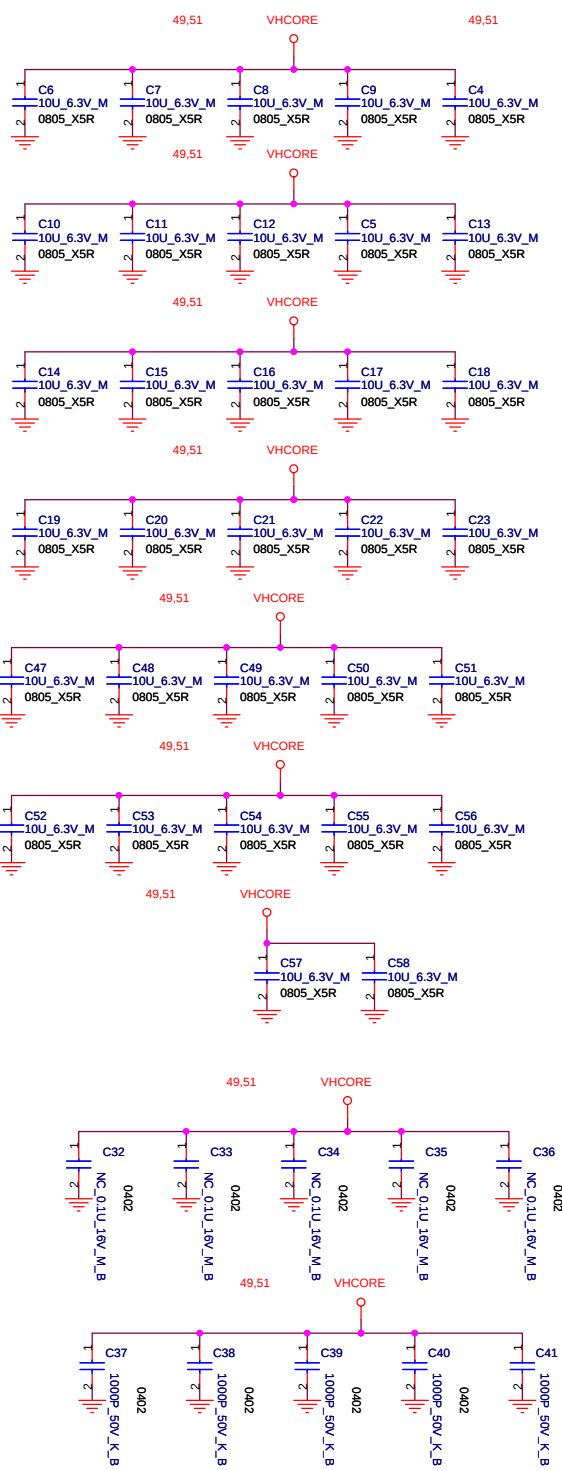
ICH7M's GPIO12:
VIL----> -0.5V ~ -0.8V
VIH----> 2.0V ~ 3.3+0.5V
YONAH's PROCHOT#:
VIL----> -0.1V ~ -0.3*VCCP
VIH----> 0.7*VCCP ~ VCCP+0.1

PM_THRMTRIP#
should connect to
ICH7-M and GMCH
without T-ing (No
stub)

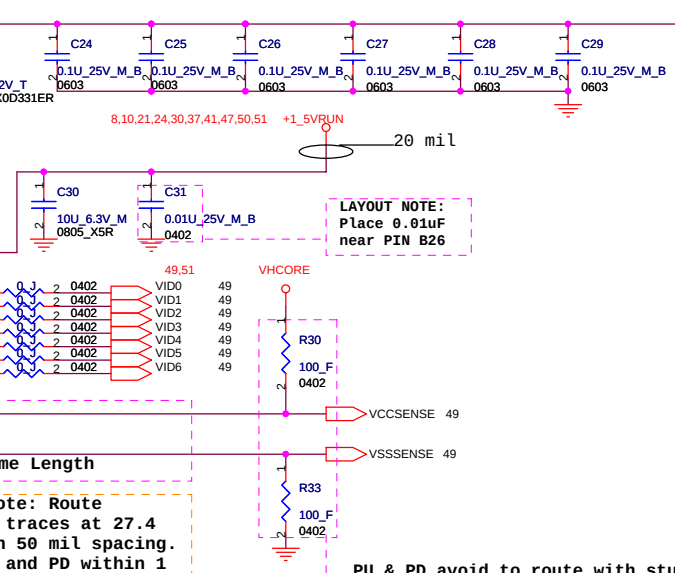
Debug port not used .
resistors close to CPU.

SM bus Address :
1001101 = 9A
For 6781-1P8
Place Thermal-Sensor near
CPU & GMCH.

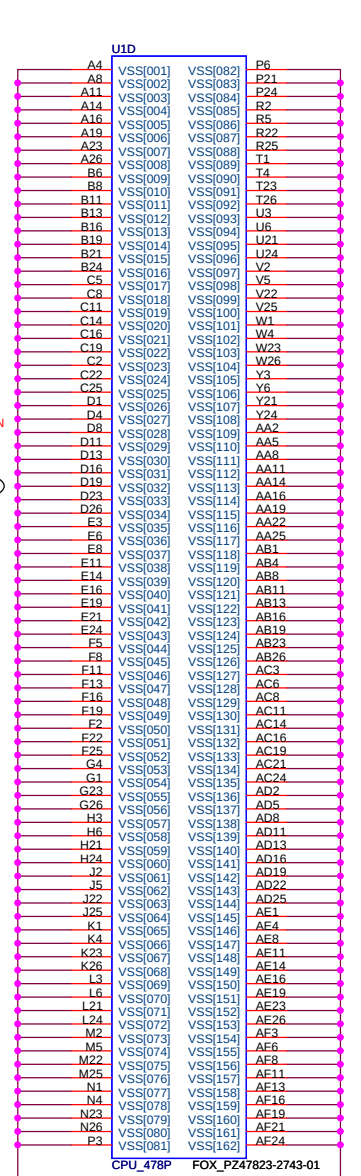


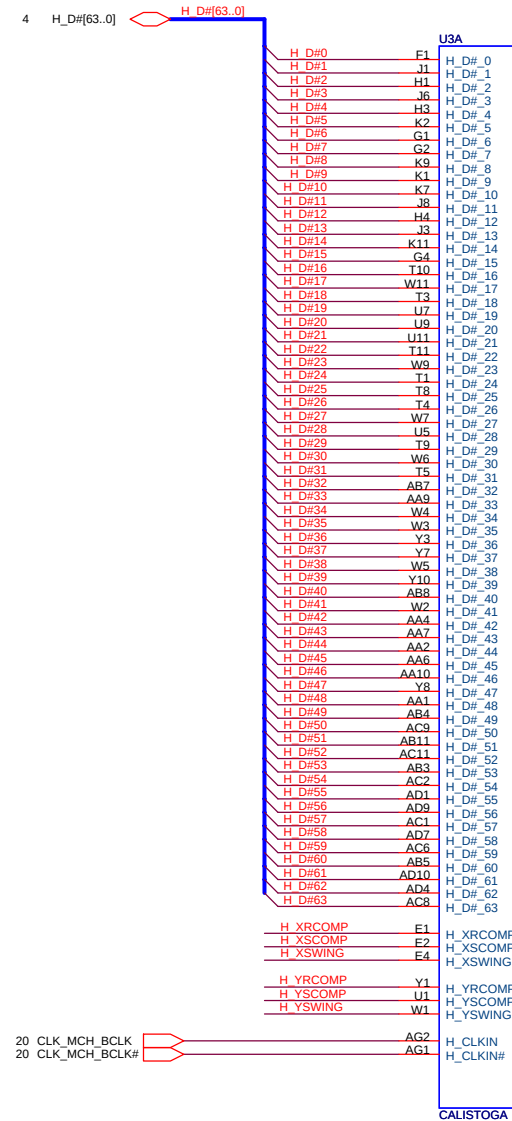
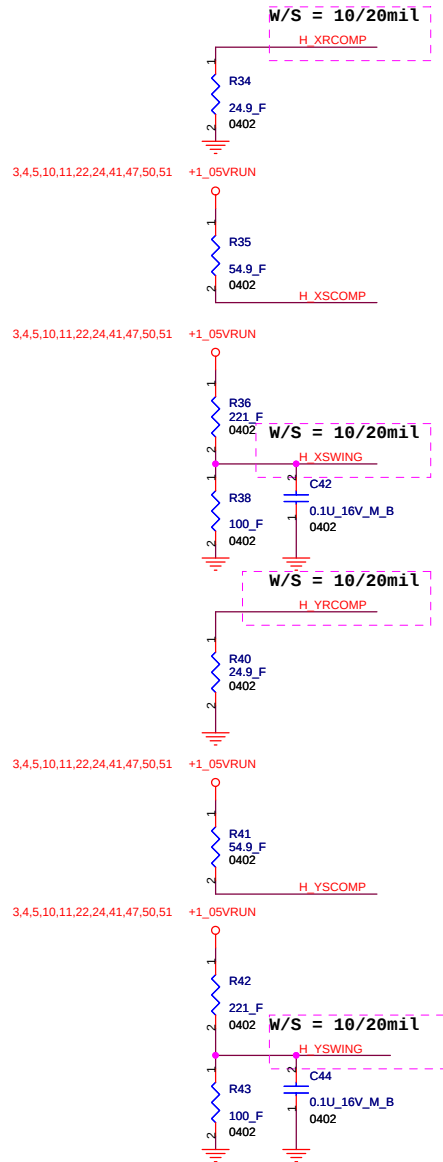


CPU_VCCA---->120mA
CPU_VCCP----->2.5A
CPU_VCC----->36A

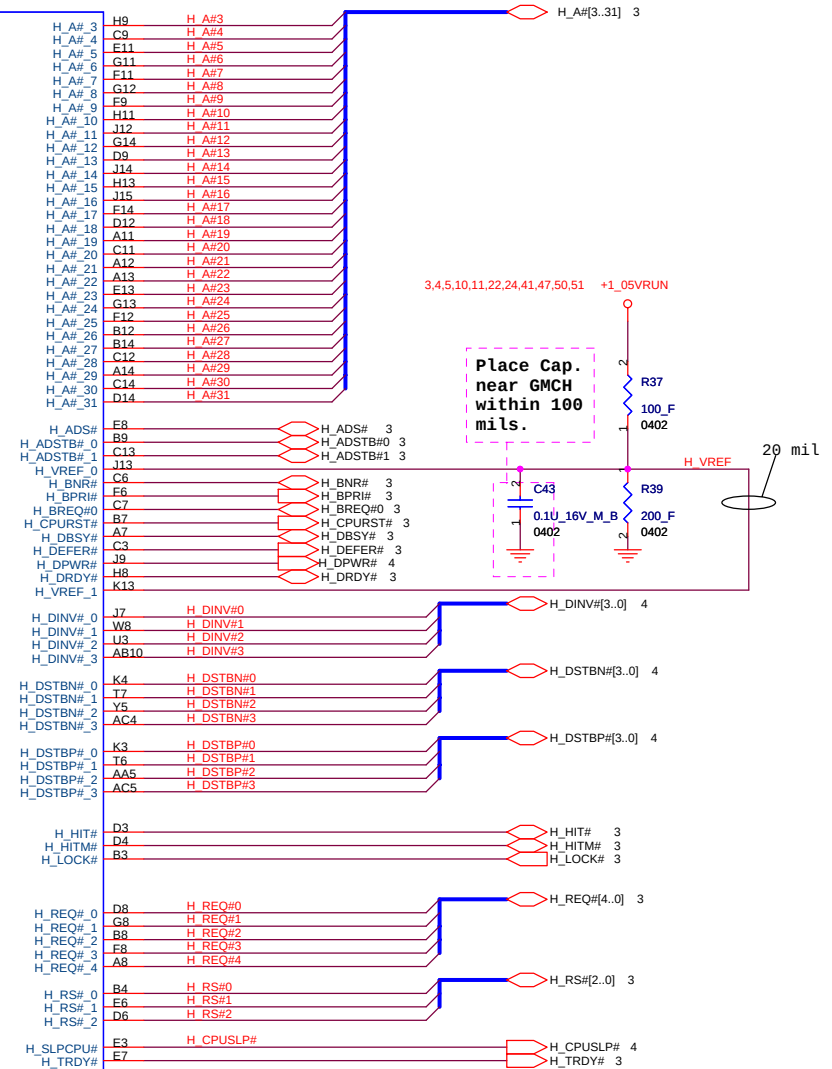


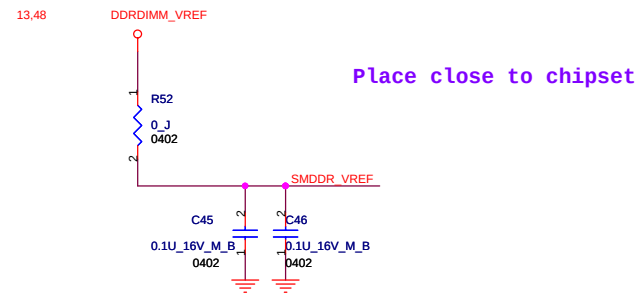
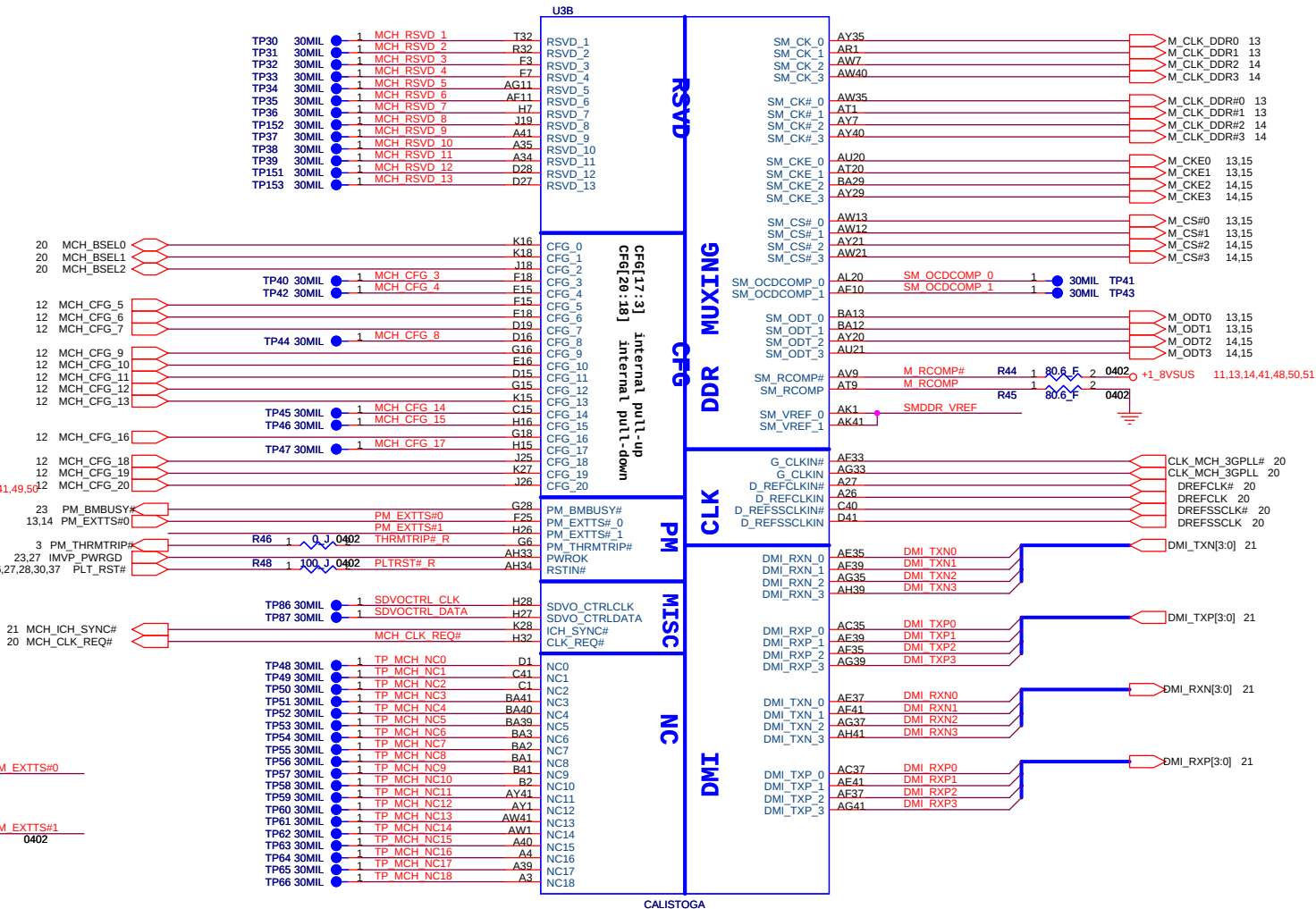
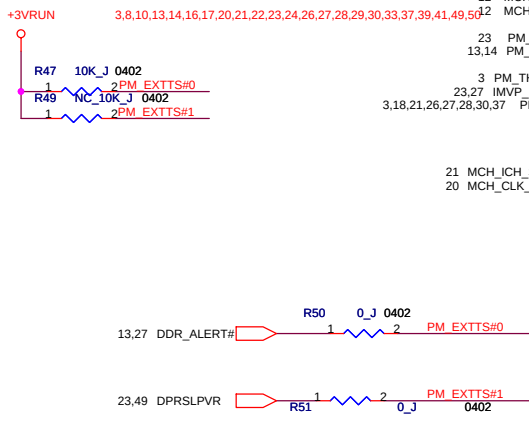
Layout Note: Route VCCSENSE traces at 27.4 Ohms with 50 mil spacing. Place PU and PD within 1 inch of cpu.
width=18 mil
spacing=7 mil

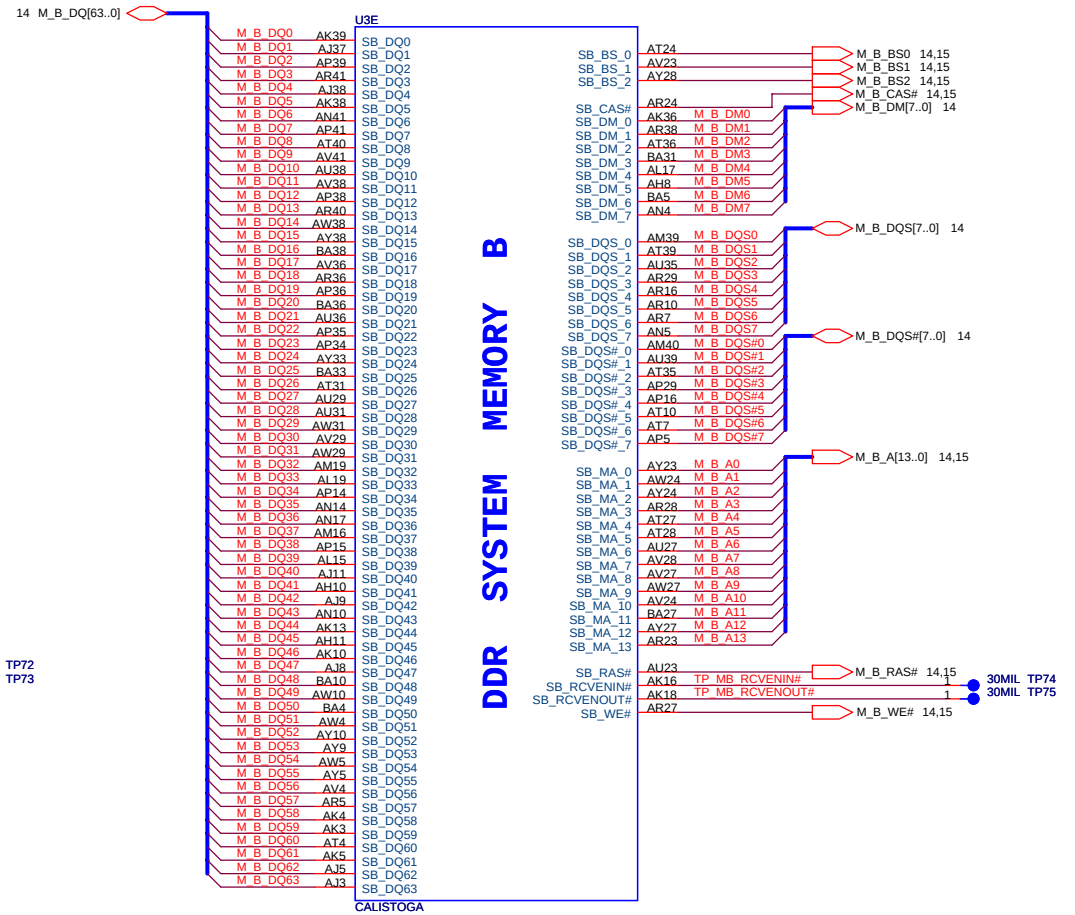
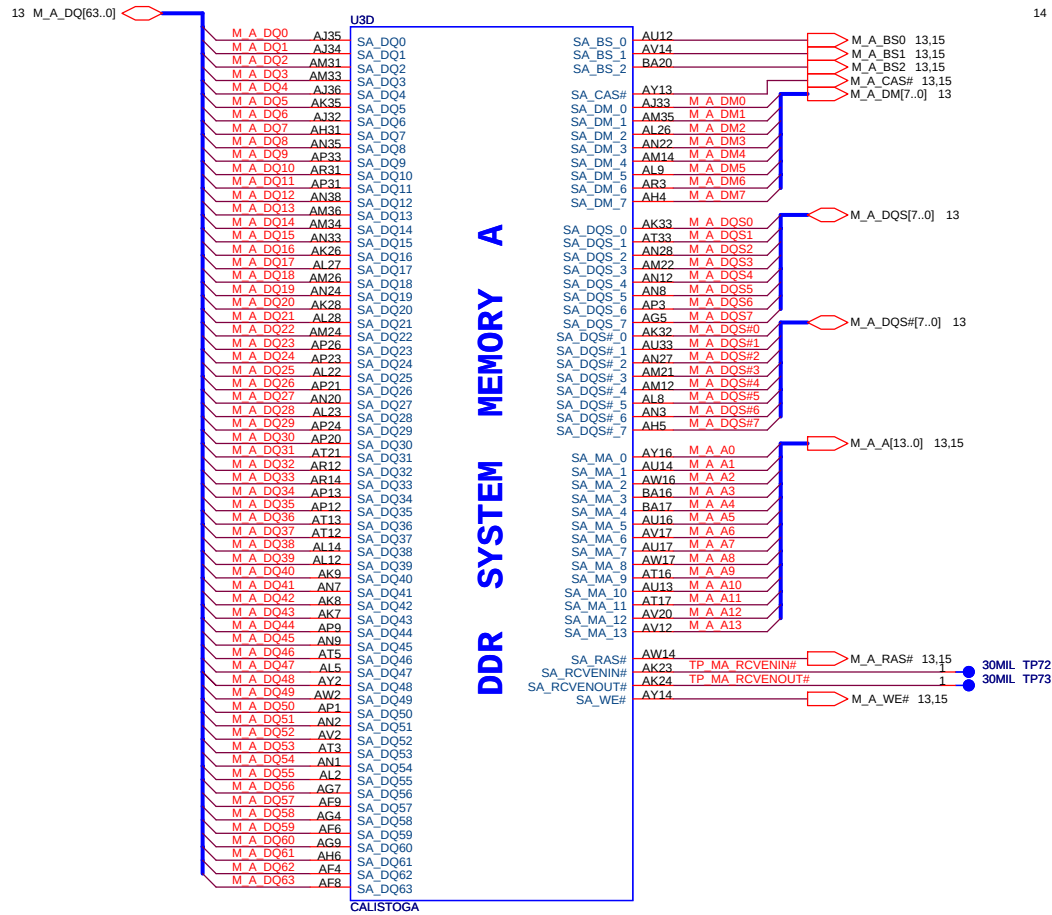


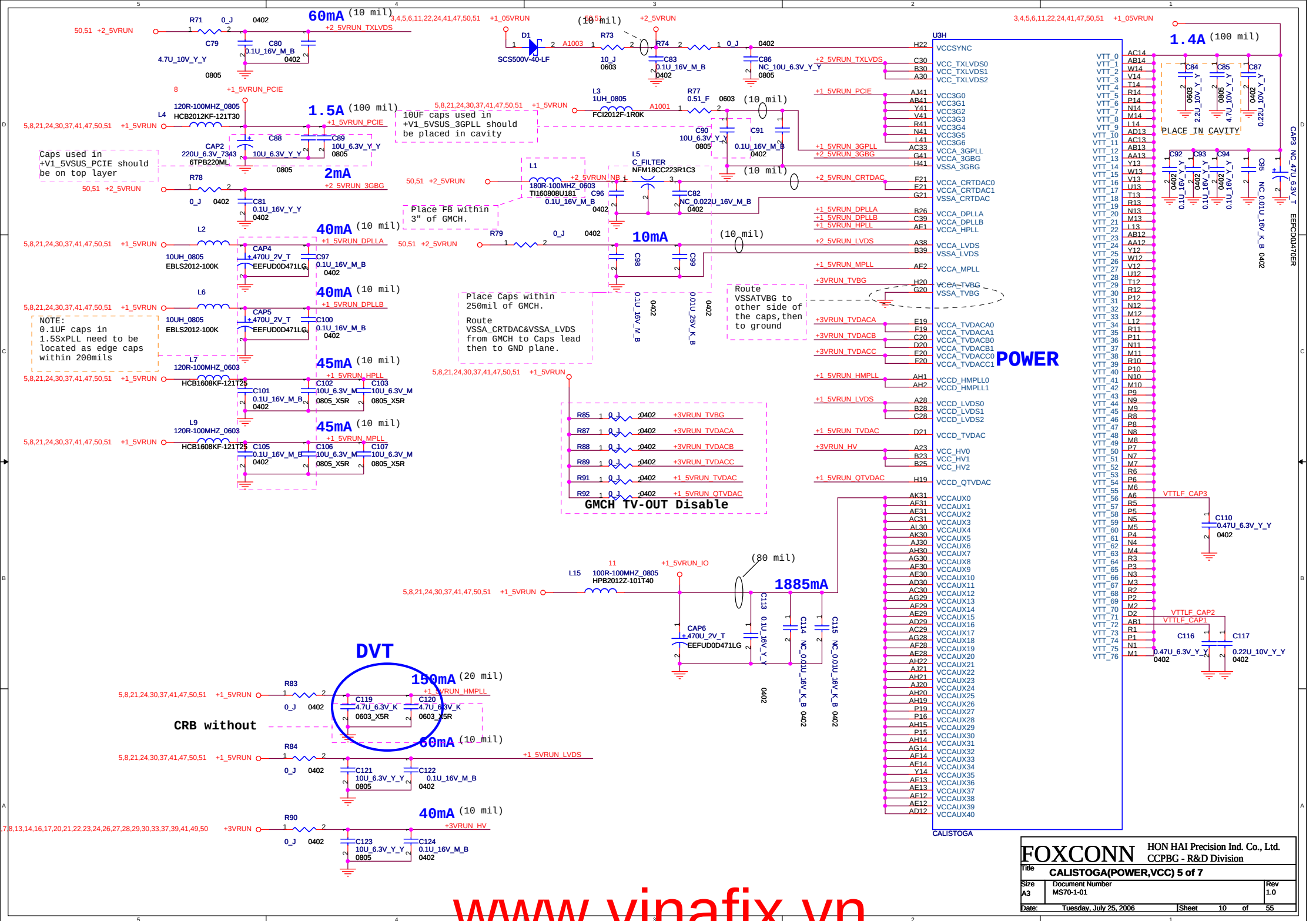


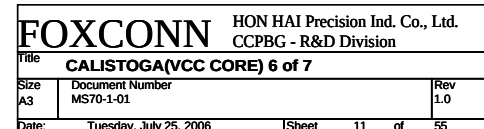
HOST











7 MCH_CFG_5 30MIL TP76

MCH_CFG_5
Low = DMIX2
High = DMIX4

MCH_CFG_18
(VCC_CORE Select)
Low = 1.05V(default)
High = 1.5V

7 MCH_CFG_18 30MIL TP79

7 MCH_CFG_6 30MIL TP77

MCH_CFG_6
Low = Moby Dick
High = Calistoga
DDR2 select (default high)

MCH_CFG_19
(DMI LANE REVERSAL)
Low = Normal(default)
High = LANES REVERSED

7 MCH_CFG_19 30MIL TP80

7 MCH_CFG_7 30MIL TP78

MCH_CFG_7
(CPU Strap)
Low = RSVD
High = Mobile Yonah processor

MCH_CFG_20
(PCIe Backward Interoperability mode)
Low = Only SDVO or PCIe x1 is operational (defaults)
High = SDVO and PCIe x1 are operating simultaneously via the PEG port

7 MCH_CFG_20 30MIL TP83

7 MCH_CFG_9 30MIL TP81

MCH_CFG_9
(PCIe Graphics Lane)
Low = Reverse Lane
High = Normal operation

For layout convenience

7 MCH_CFG_10 30MIL TP82

MCH_CFG_10
(HOST PLL VCC SELECT)
Low = RESERVED
High = MOBILITY

Layout Noe:
Location of all MCH_CFG strap resistors needs to be close to trace to minimize stub

7 MCH_CFG_11 30MIL TP84

MCH_CFG_11
(PSB 4x CLK ENABLE)
Low = Calistoga
High = Reserved

R93
NC_2.2K_Ω
0402

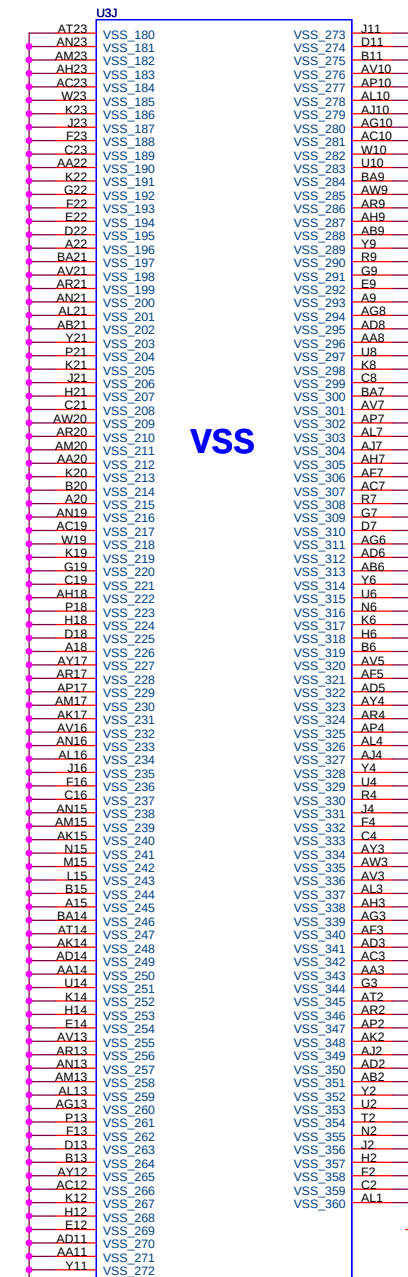
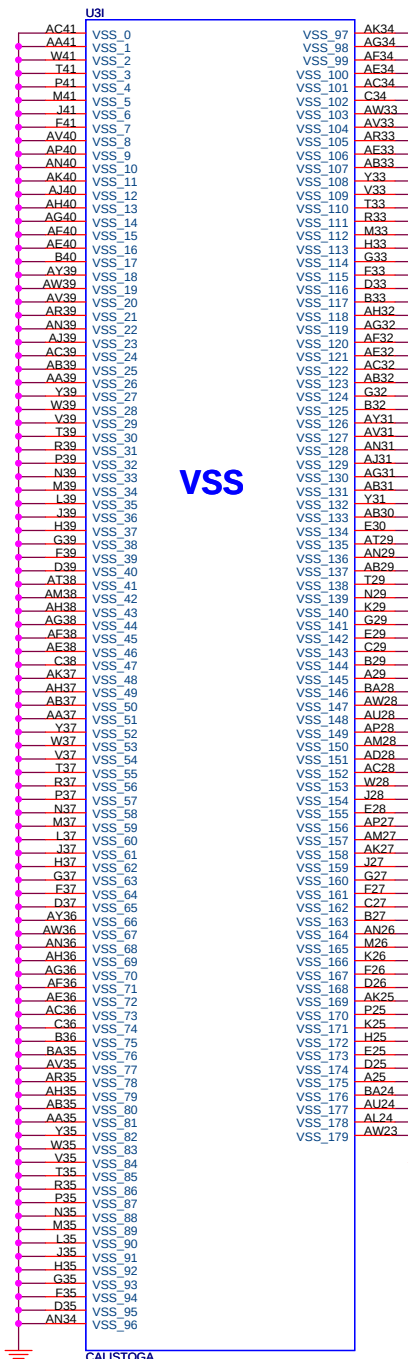
7 MCH_CFG_12 30MIL TP84

7 MCH_CFG_13 30MIL TP85

MCH_CFG [13:12]
(XOR/ALLZ)
00=Partial Clock Gating Disable
01=XOR Mode Enable
10=All-Z Mode Enable
11=Normal Operation(Default)

7 MCH_CFG_16 30MIL TP160

MCH_CFG_16
(FSB Dynamic ODT)
Low = Dynamic ODT Disabled
High = Dynamic ODT Enable

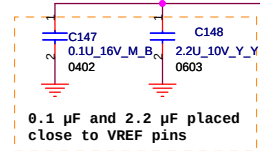


VSS

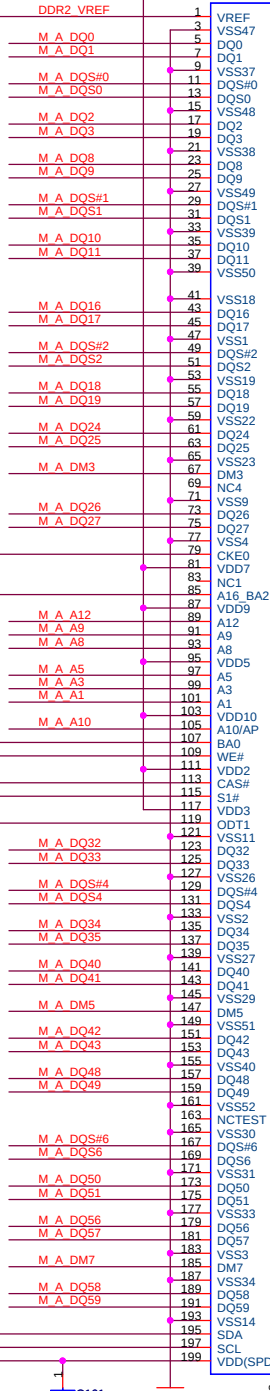
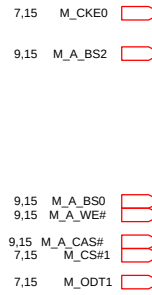
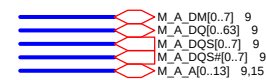
VSS

CALISTOGA

CALISTOGA



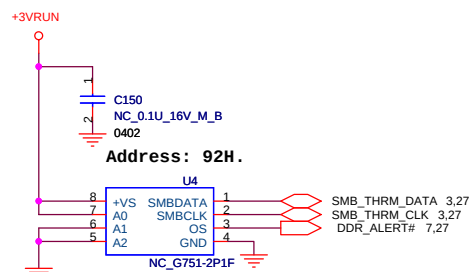
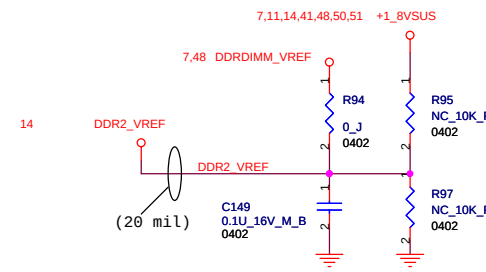
1.8V per DIMM=3.08A



PC-4200/PC2-5300 DDR2 SDRAM SO-DIMM (200P)

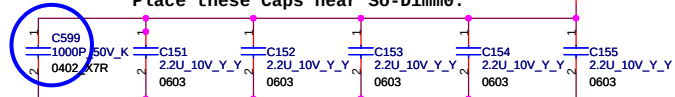
DIMM_0

SMBus Address: A0(W)/A1(R)



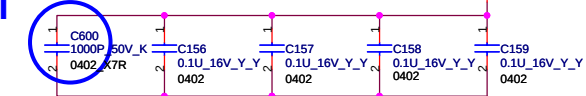
Address: 92H.

DVT



Place these Caps near So-Dimm0.

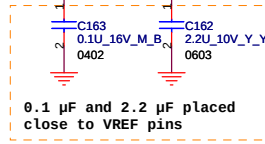
DVT



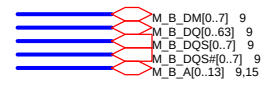
Place these Caps near So-Dimm0.

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title DDR(II)SO-DIMM_0			
Size A3	Document Number MS70-1-01		Rev 1.0
Date: Tuesday, July 25, 2006	Sheet 13	of 55	

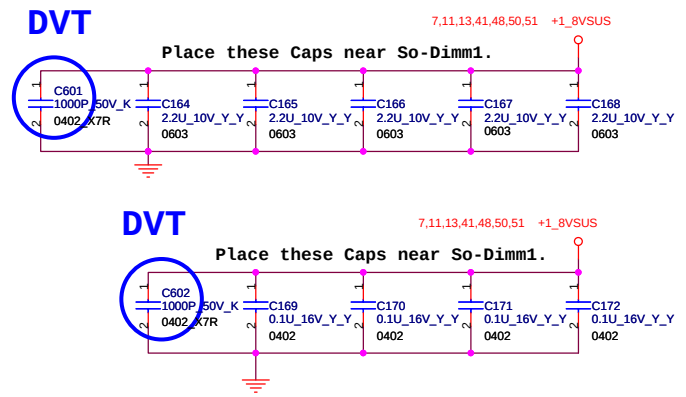
www.vinafix.vn



1.8V per DIMM=3.08A



PC2-4200/PC2-5300 DDR2 SDRAM SO-DIMM (200P)

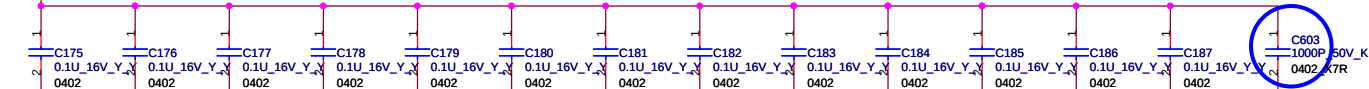


FOXCONN		HON HAI Precision Ind. Co., Ltd.	
File		DDR(I)SO-DIMM_1	
Size	A3	Document Number	MS70-1-01
Date:	Tuesday, July 25, 2006	Sheet	14 of 55

www.vinafix.vn

48,50,51

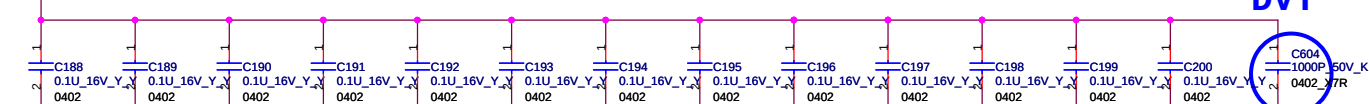
+0_9VSUS



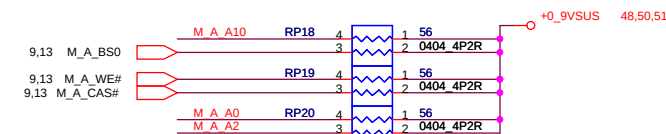
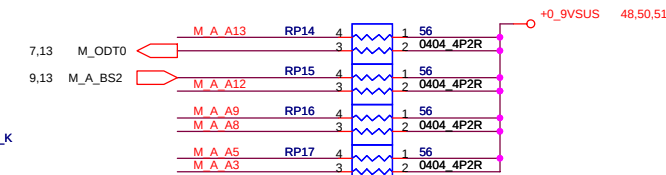
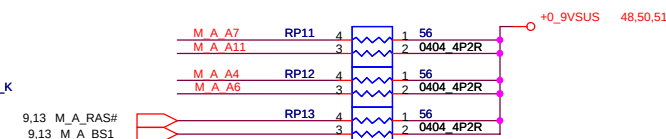
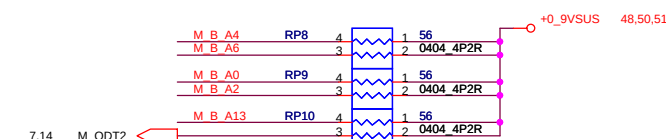
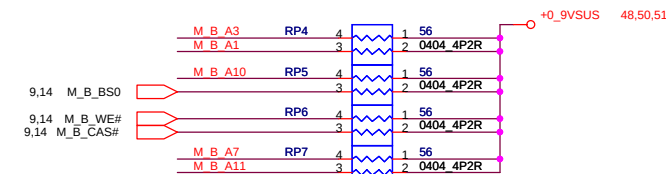
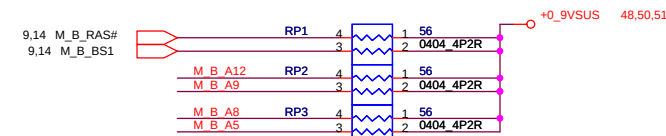
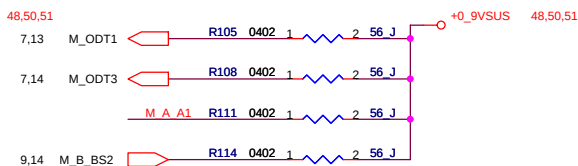
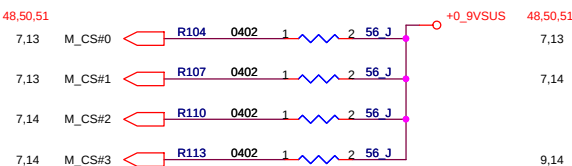
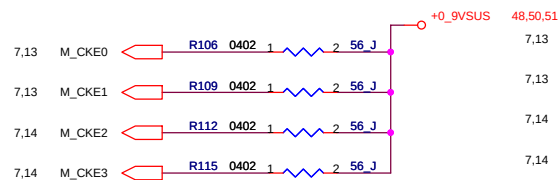
Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9VSUS

48,50,51

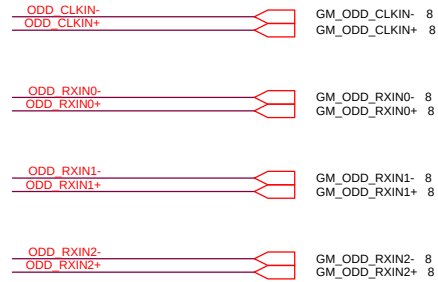
+0_9VSUS



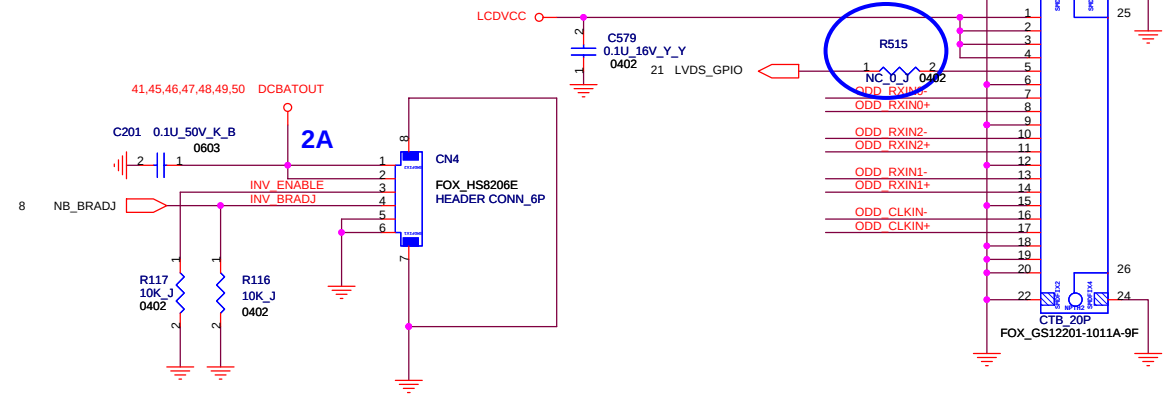
Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9VSUS



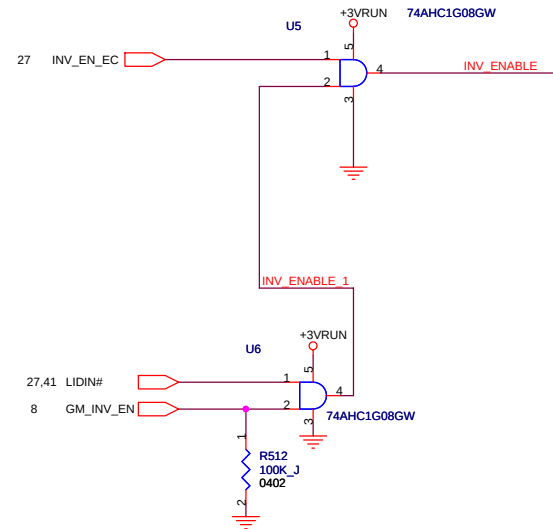
LVDS



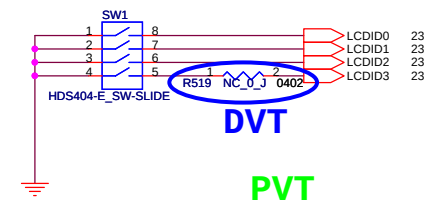
LVDS CONNECTOR DVT



INVERTER CONNECTOR



PANEL ID



PVT

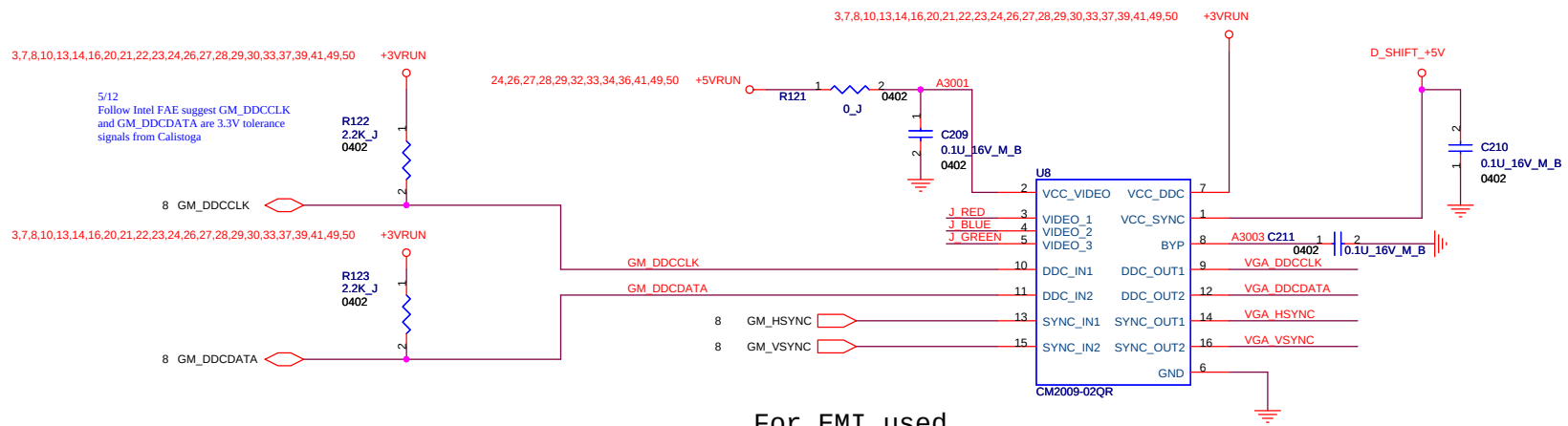
Type	WXGA	WXGA	WSXGA
Size	15.4" wide	15.4" wide	15.4" wide
Vendor	CPT	QDI	InnoLux
Device Name	CLAA154WA05AN	QDI15TL0703	TBD
Panel ID Check[3..0]	1001	1010	1011

ON=0

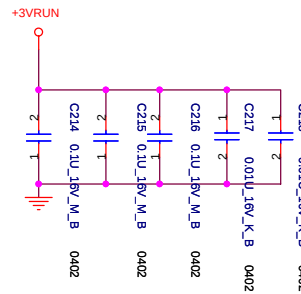
DISCHARGE

The R461 will consume about 0.054 Watt ($3.3 \times 3.3 / 200 = 0.054W$). We changed resistor to 0603 size (1/8 Watt)

FOXCONN			HON HAI Precision Ind. Co., Ltd.
Title			CCPBG - R&D Division
Size	Document Number	Rev	
A3	MS70-1-01	1.0	
Date:	Tuesday, July 25, 2006	Sheet	16 of 55

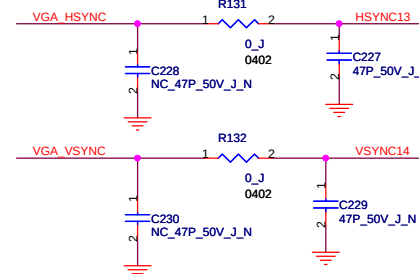
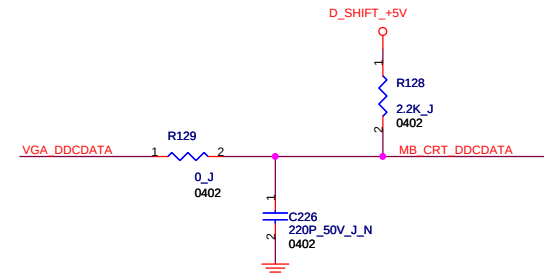
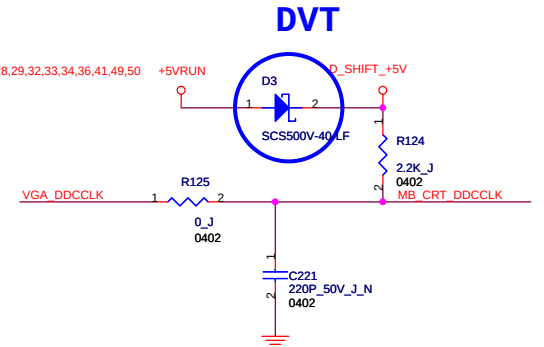
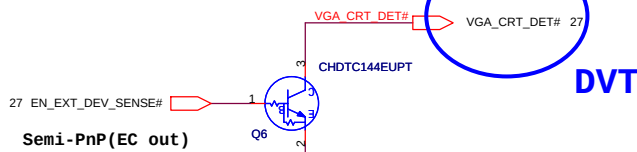
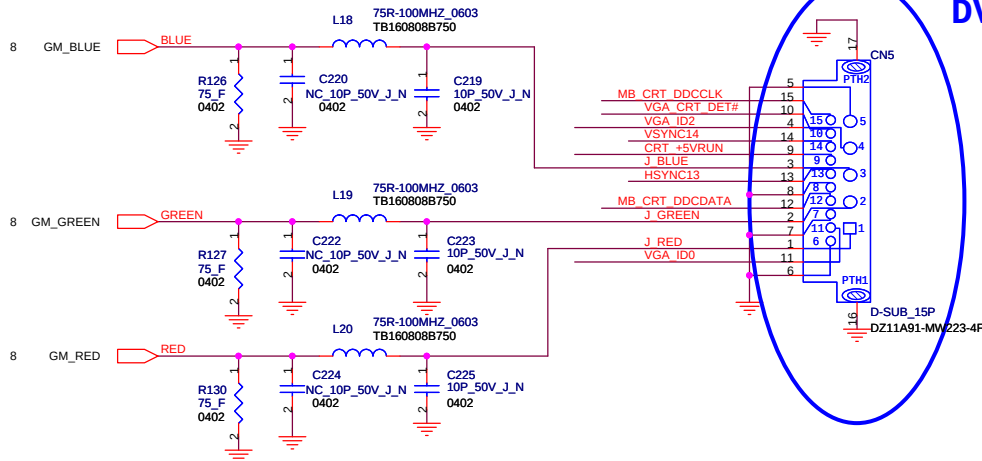


For EMI used

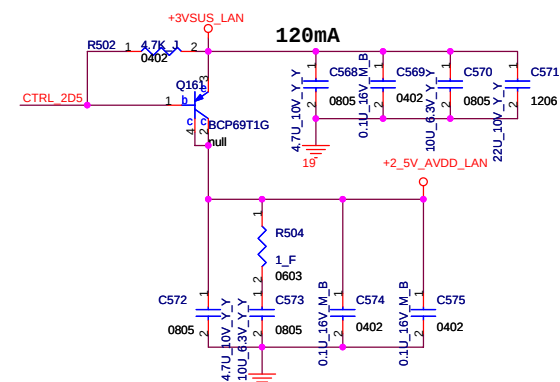
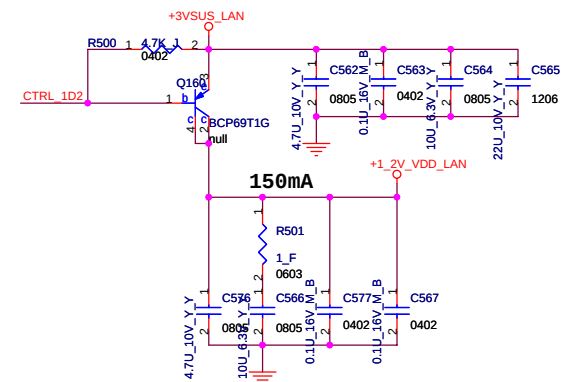
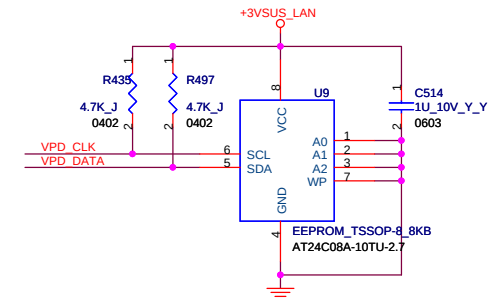
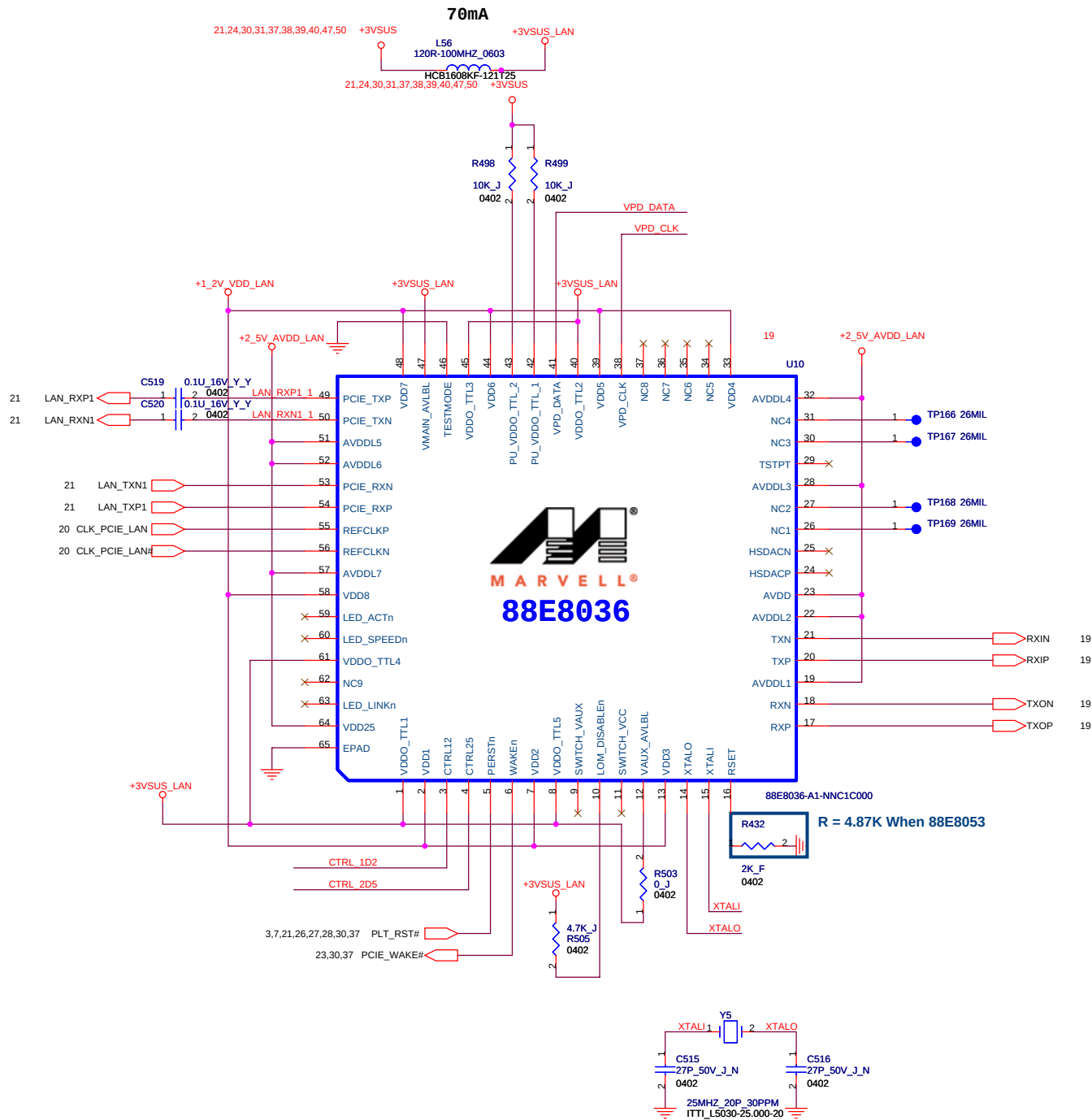


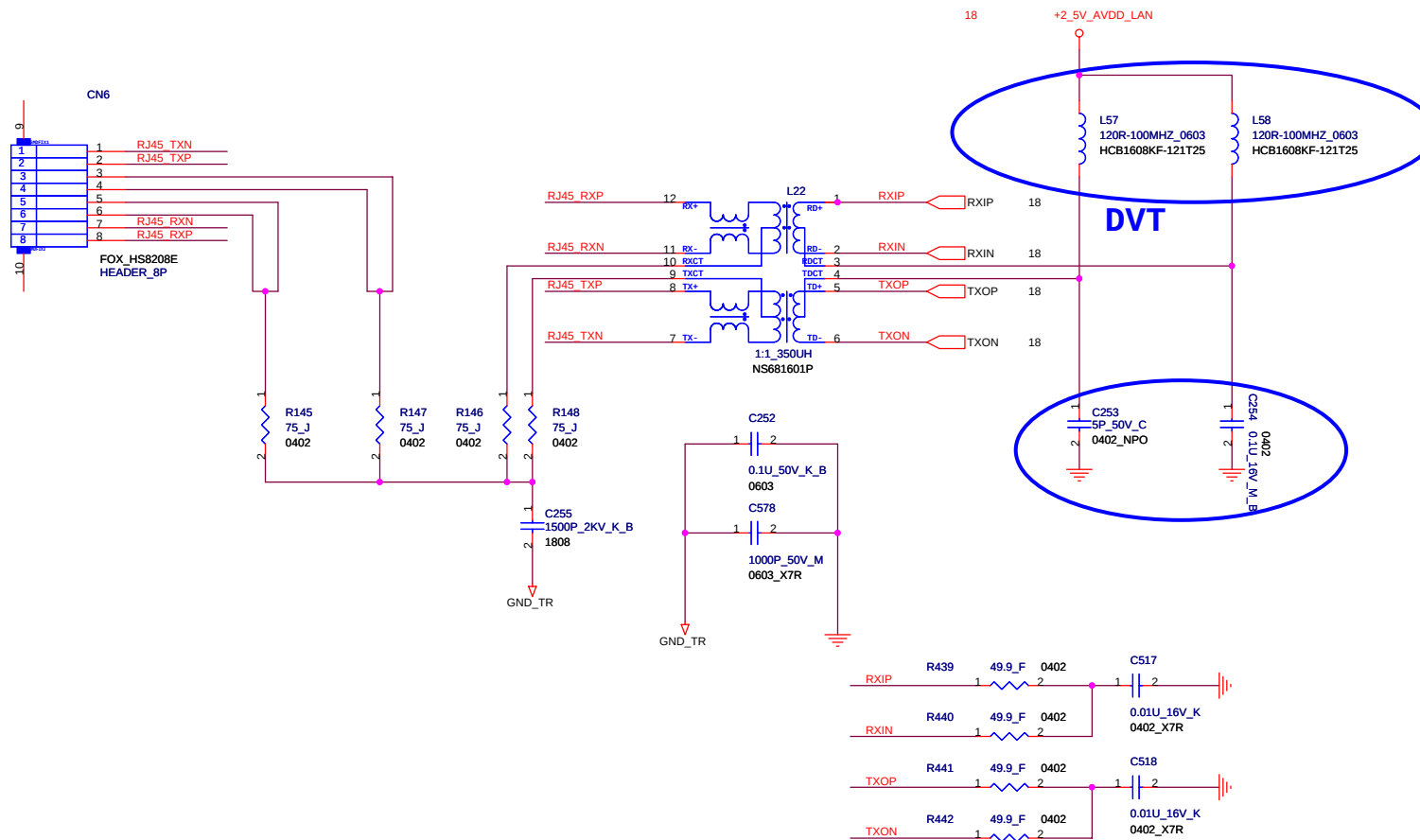
CRT CONNECTOR

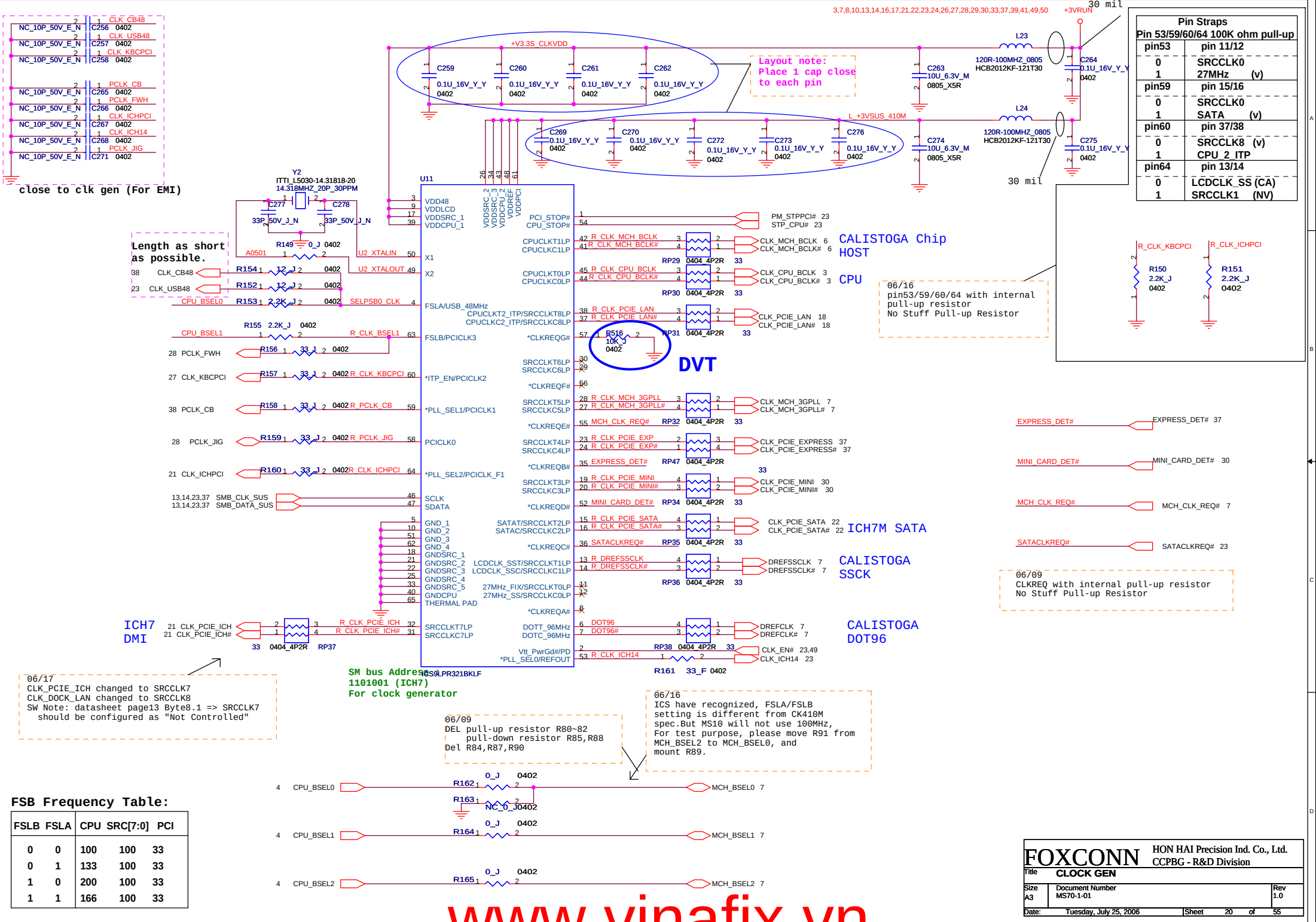
DVT



FOXCONN			HON HAI Precision Ind. Co., Ltd.
Title			CCPBG - R&D Division
Size	Document Number	Rev	
A3	MS70-1-01	1.0	
Date:	Tuesday, Jul 25, 2006	Sheet	17 of 55







NC_10P_50V_E_N	2	1	CLK CB48
NC_10P_50V_E_N	2	1	CLK USB48
NC_10P_50V_E_N	2	1	CLK KBCPCI
NC_10P_50V_E_N	2	1	PCLK CB
NC_10P_50V_E_N	2	1	PCLK FW
NC_10P_50V_E_N	2	1	CLK ICHPCI
NC_10P_50V_E_N	2	1	CLK ICH14
NC_10P_50V_E_N	2	1	PCLK JIG
NC_10P_50V_E_N	2	1	C271 0402

close to clk gen (For EMI)

Length as short as possible.

ICH7 DMI

06/17
CLK_PCIE_ICH changed to SRCCLK7
CLK_DOCK_LAN changed to SRCCLK8
SW Note: datasheet page13 Byte8.1 => SRCCLK7 should be configured as "Not Controlled"

FSB Frequency Table:

FSLB	FSLA	CPU SRC[7:0]	PCI
0	0	100	100 33
0	1	133	100 33
1	0	200	100 33
1	1	166	100 33

Pin Straps	
Pin	Signal
pin53	pin 11/12
0	SRCCLK0
1	27MHz (v)
pin59	pin 15/16
0	SRCCLK0
1	SATA (v)
pin60	pin 37/38
0	SRCCLK8 (v)
1	CPU 2 ITP
pin64	pin 13/14
0	LCDCLK_SS (CA)
1	SRCCLK1 (NV)

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

CLOCK GEN

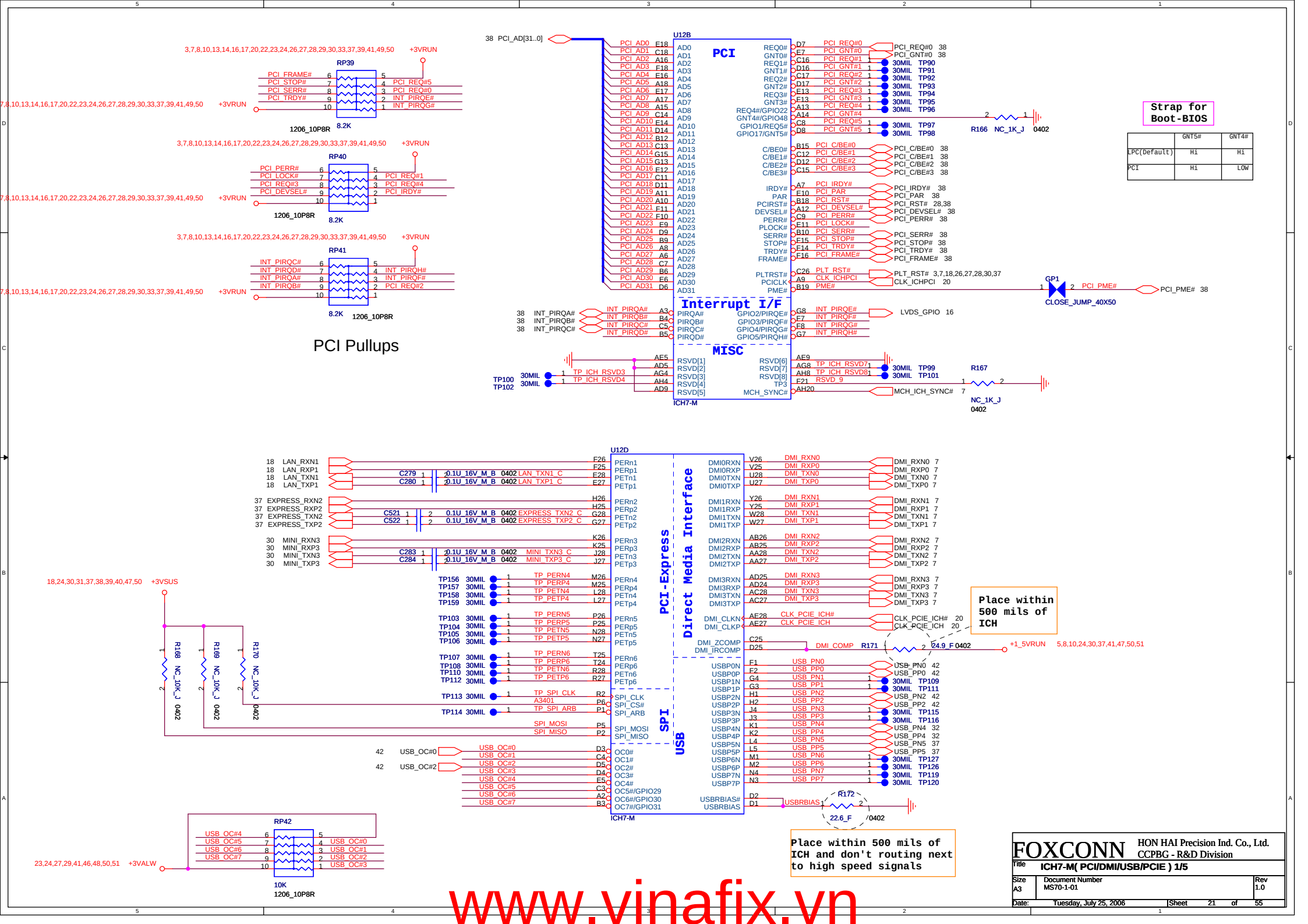
Size A3

Document Number MS70-1-01

Rev 1.0

Date: Tuesday, July 25, 2006

Sheet 20 of 55



Strap for
Boot-BIOS

	GNT5#	GNT4#
LPC(Default)	H1	H1
PCI	H1	LOW

PCI Pullups

Interrupt I/F

MISC

Direct Media Interface

SPI

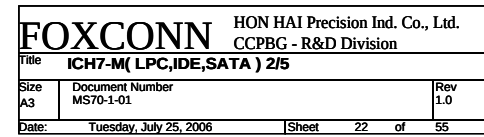
USB

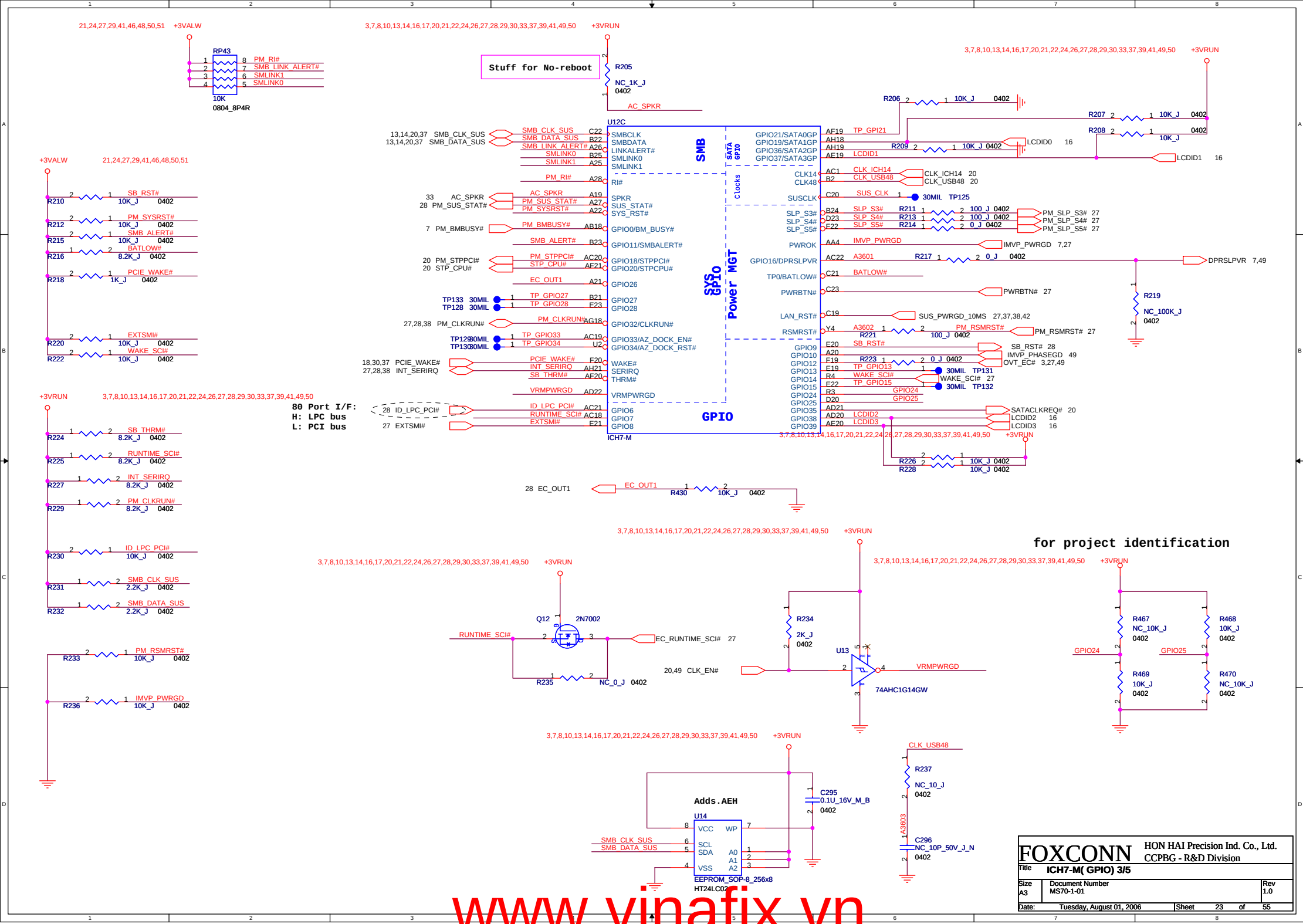
Place within
500 mils of
ICH

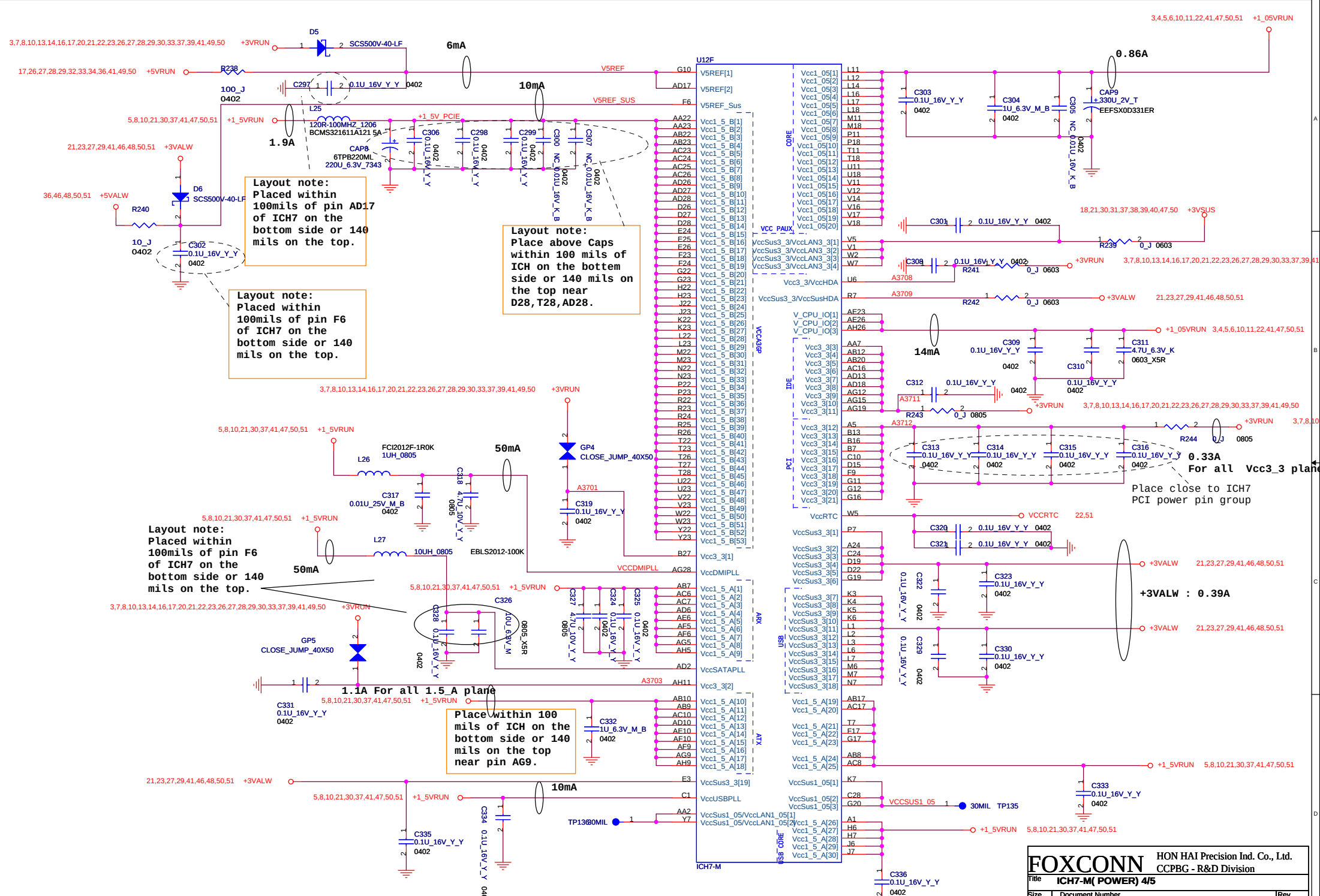
Place within 500 mils of
ICH and don't routing next
to high speed signals

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title ICH7-M (PCI/DMI/USB/PCIE) 1/5		
Size A3	Document Number MS70-1-01	Rev 1.0
Date Tuesday, July 25, 2006	Sheet 21	of 55





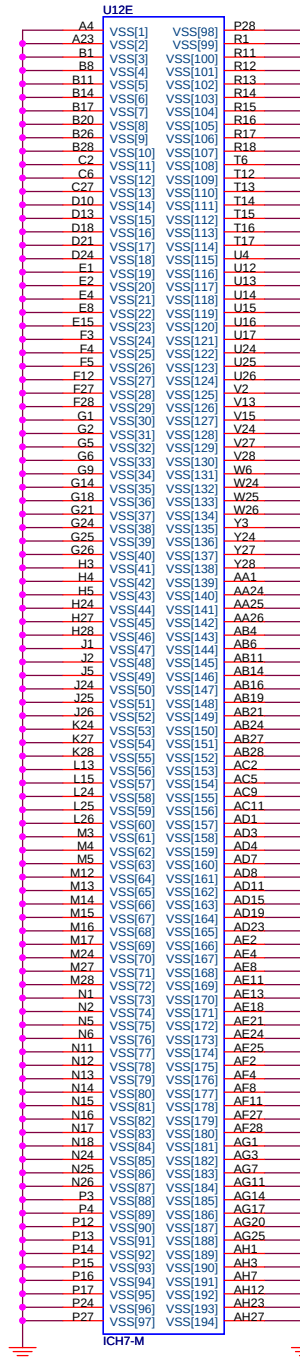


Layout note:
Placed within
100mils of pin AD17
of ICH7 on the
bottom side or 140
mils on the top.

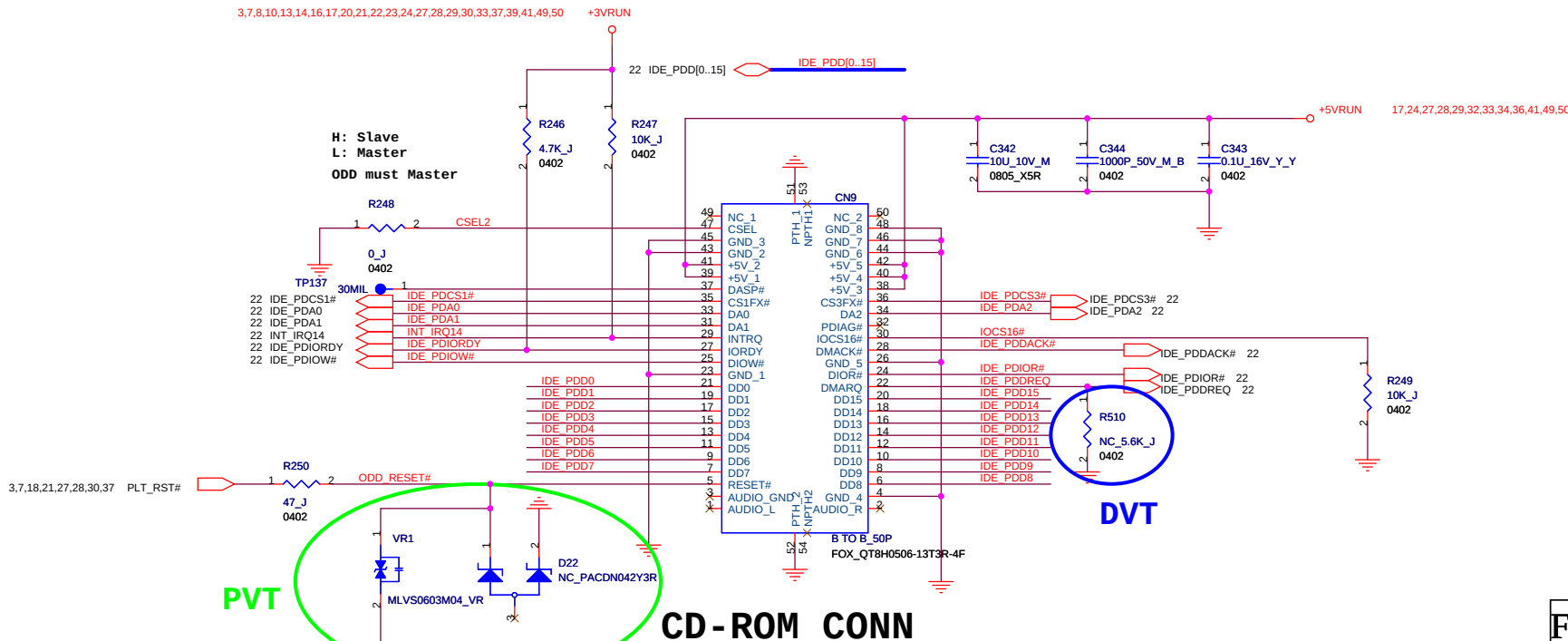
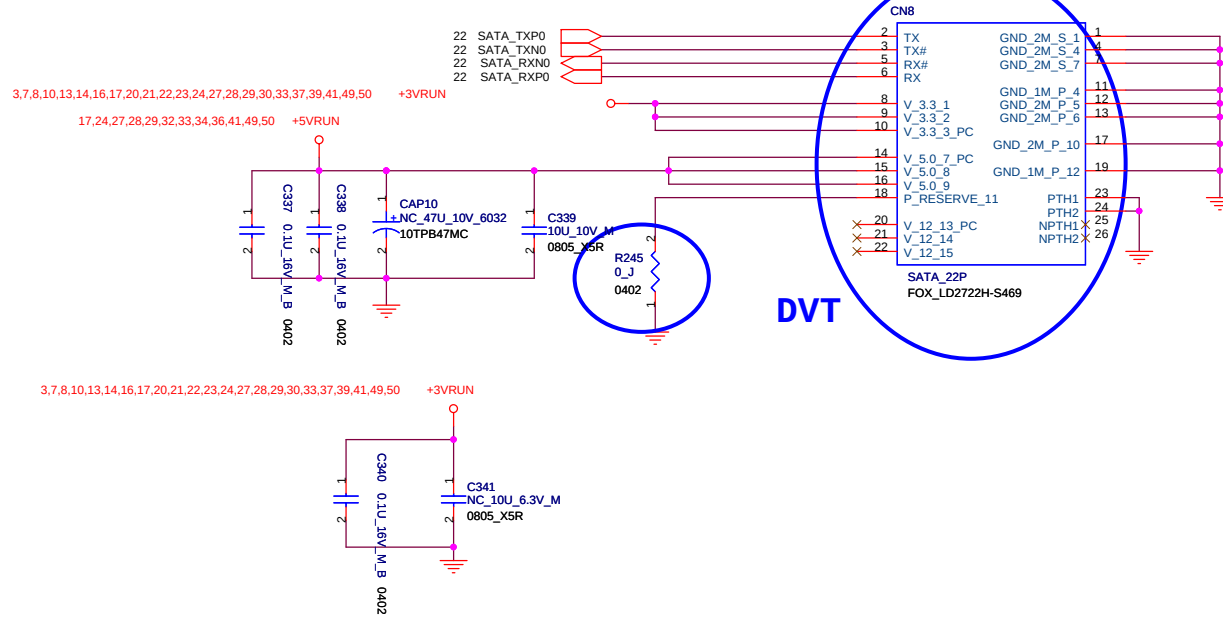
Layout note:
Placed within
100mils of pin F6
of ICH7 on the
bottom side or 140
mils on the top.

Layout note:
Placed within
100mils of pin F6
of ICH7 on the
bottom side or 140
mils on the top.

Place within 100
mils of ICH on the
bottom side or 140
mils on the top
near pin AG9.



SATA HDD CONN



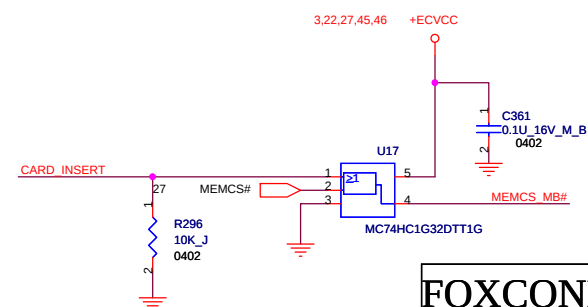
CD-ROM CONN

Follow Adoi san suggest ODD: Master/HDD:Slave

FOXCONN			HON HAI Precision Ind. Co., Ltd.
Title			CCPBG - R&D Division
Size	Document Number	Rev	
A3	MS70-1-01	1.0	
Date:	Tuesday, July 25, 2006	Sheet	26 of 55

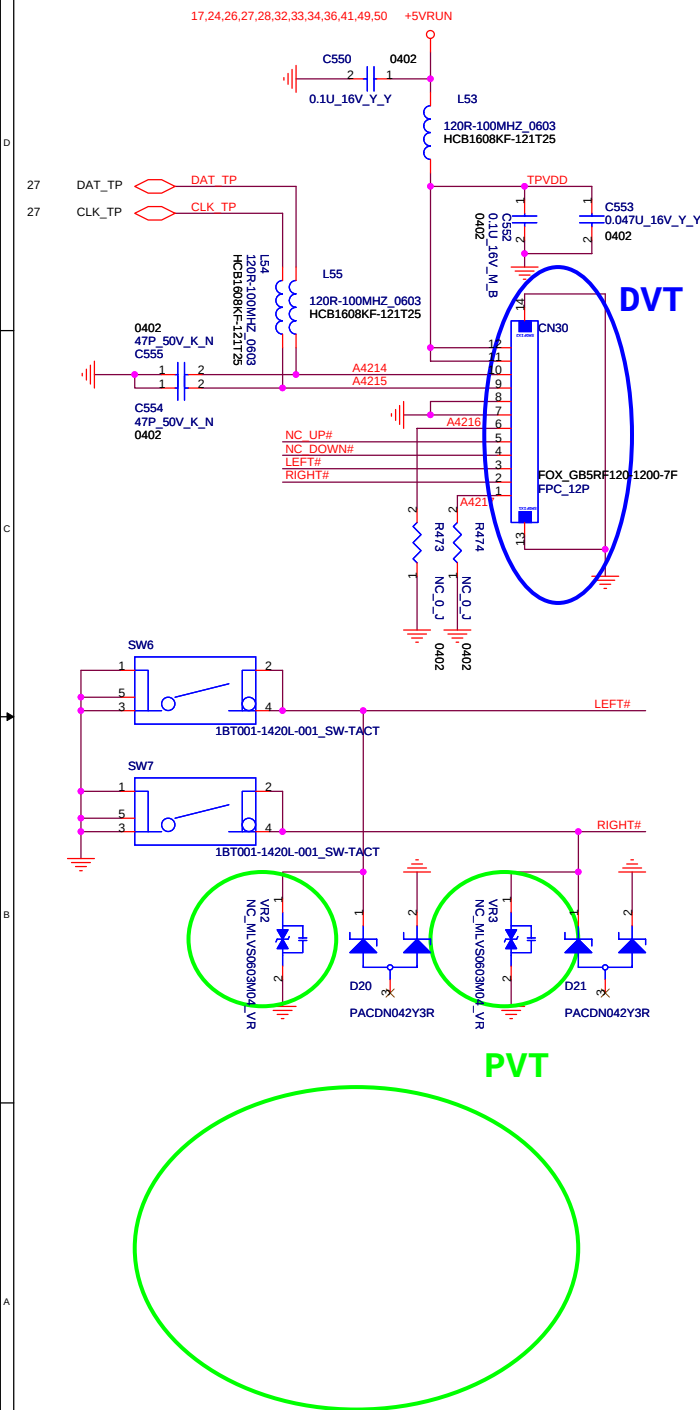
www.vinafix.vn



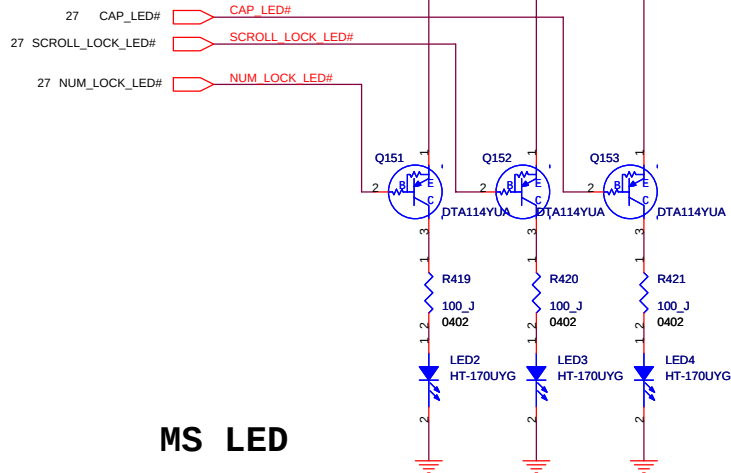


FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title Flash ROM/X-Bus/LID SW#			
Size A3	Document Number MS70-1-01	Rev 1.0	
Date:	Tuesday, July 25, 2006	Sheet	28 of 55

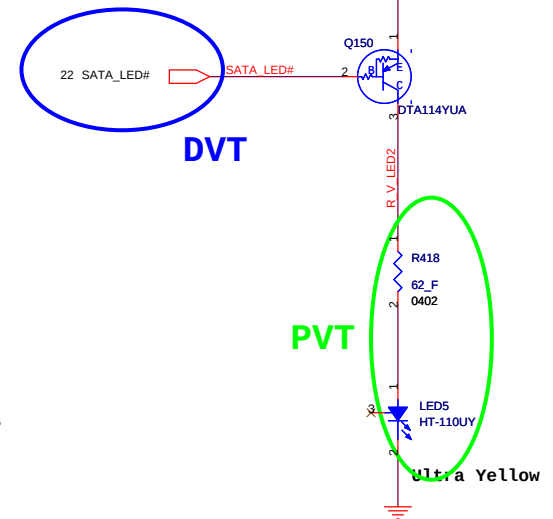
Touch Pad Board



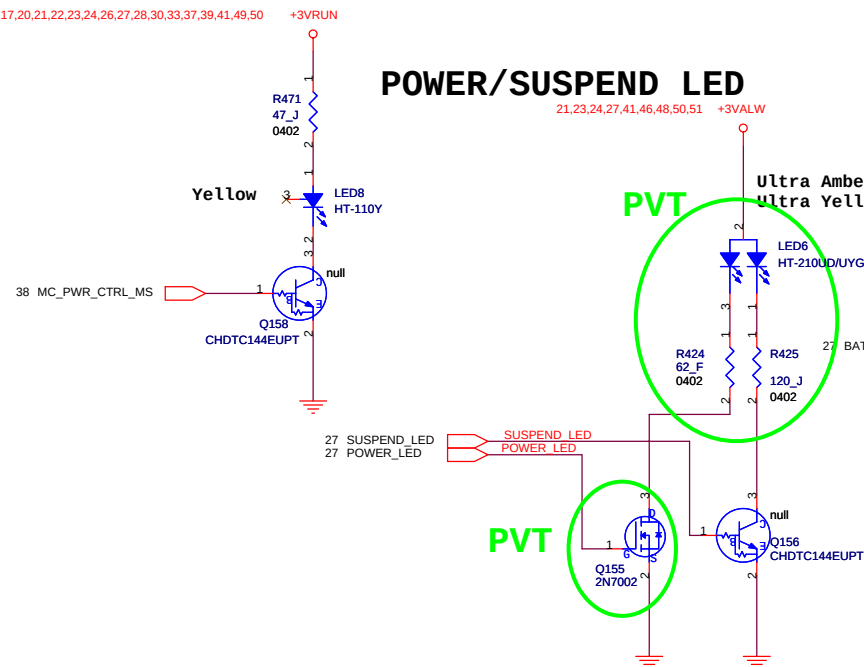
CAP_LED# SCROLL_LOCK_LED# NUM_LOCK_LED#



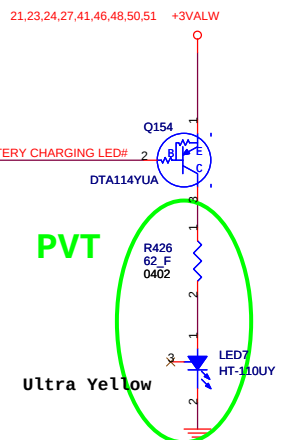
HDD_LED#

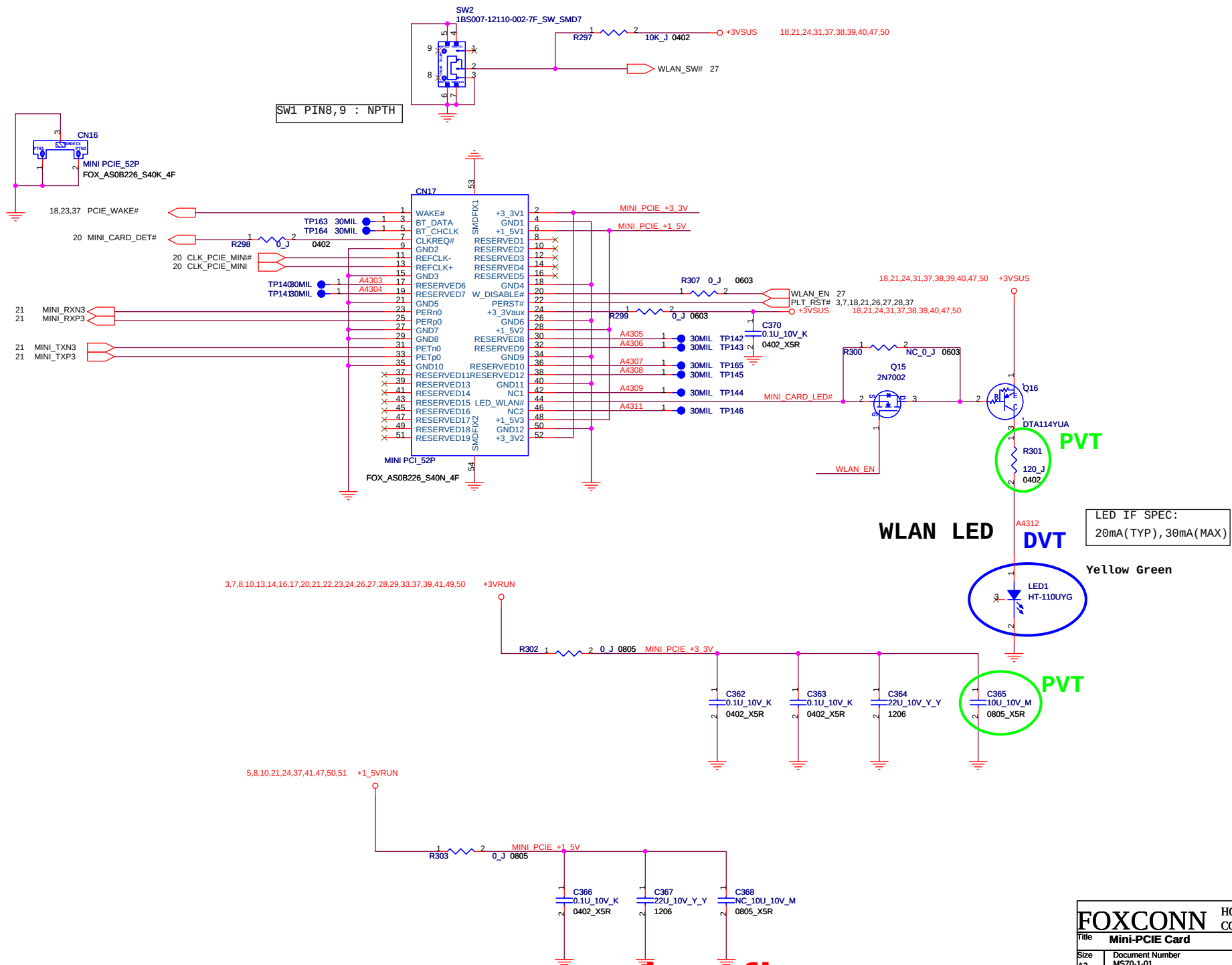


POWER/SUSPEND LED



BATTERY CHARGING LED#





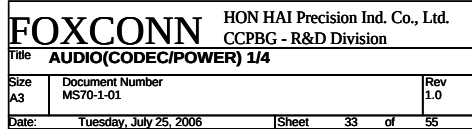
The schematic diagram illustrates the fan control circuit for the ASUS ROG Strix Z690-E motherboard. It features two main sections: the PVT (Pulse Width Modulation) section and the DVT (Digital Voltage Transistor) section.

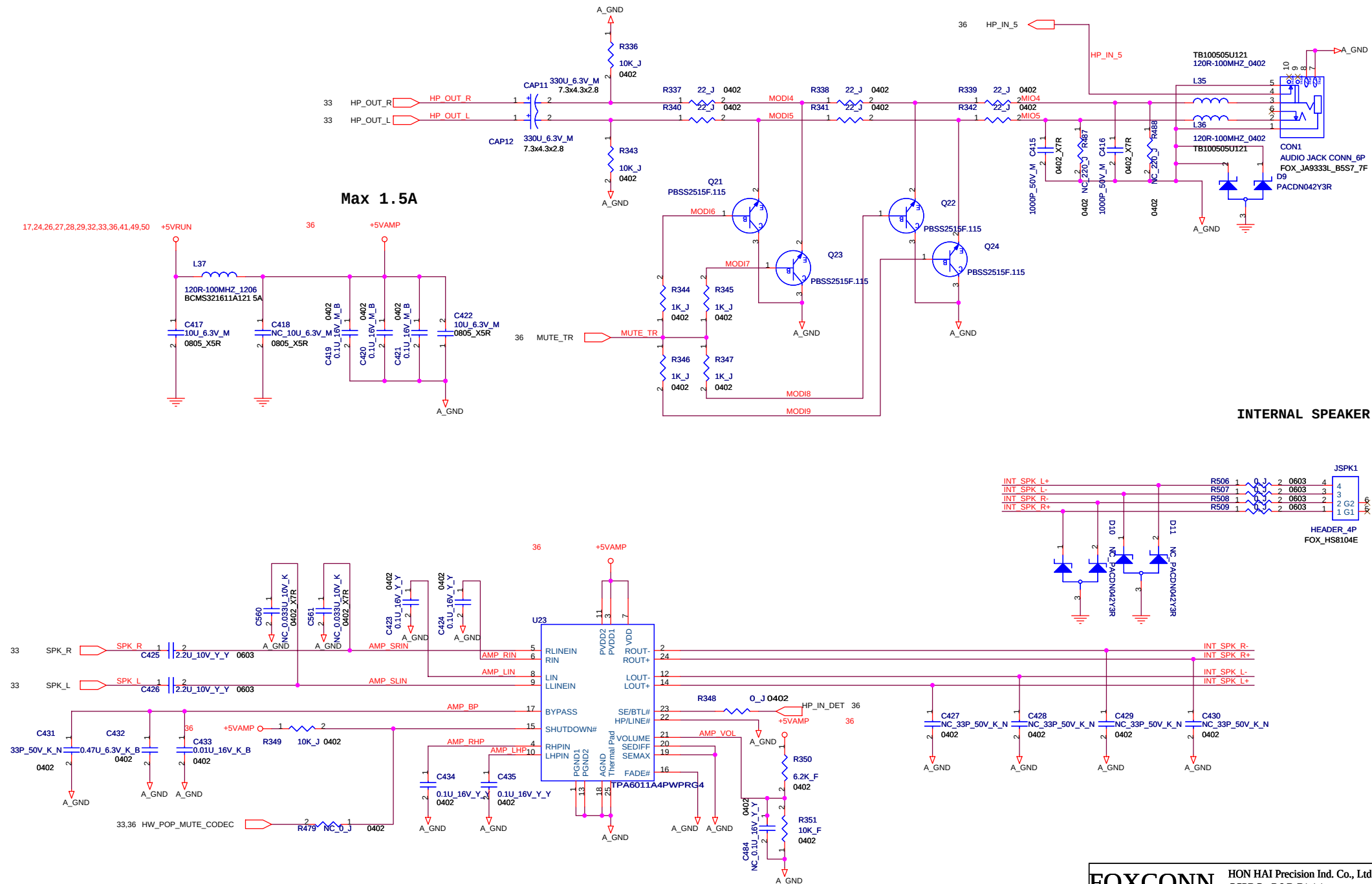
PVT Section: This section is responsible for controlling the fan speed. It includes a MOSFET (Q157) driven by the FAN1_PWM signal. The MOSFET's source is connected to ground, and its drain is connected to the fan's positive terminal. A diode (D18, SSM22LLPT) is connected in parallel with the fan to prevent back EMF. A resistor (R305, 4.7K_J 0402) is connected between the +5VSUS supply and the fan's positive terminal. The fan's negative terminal is connected to ground.

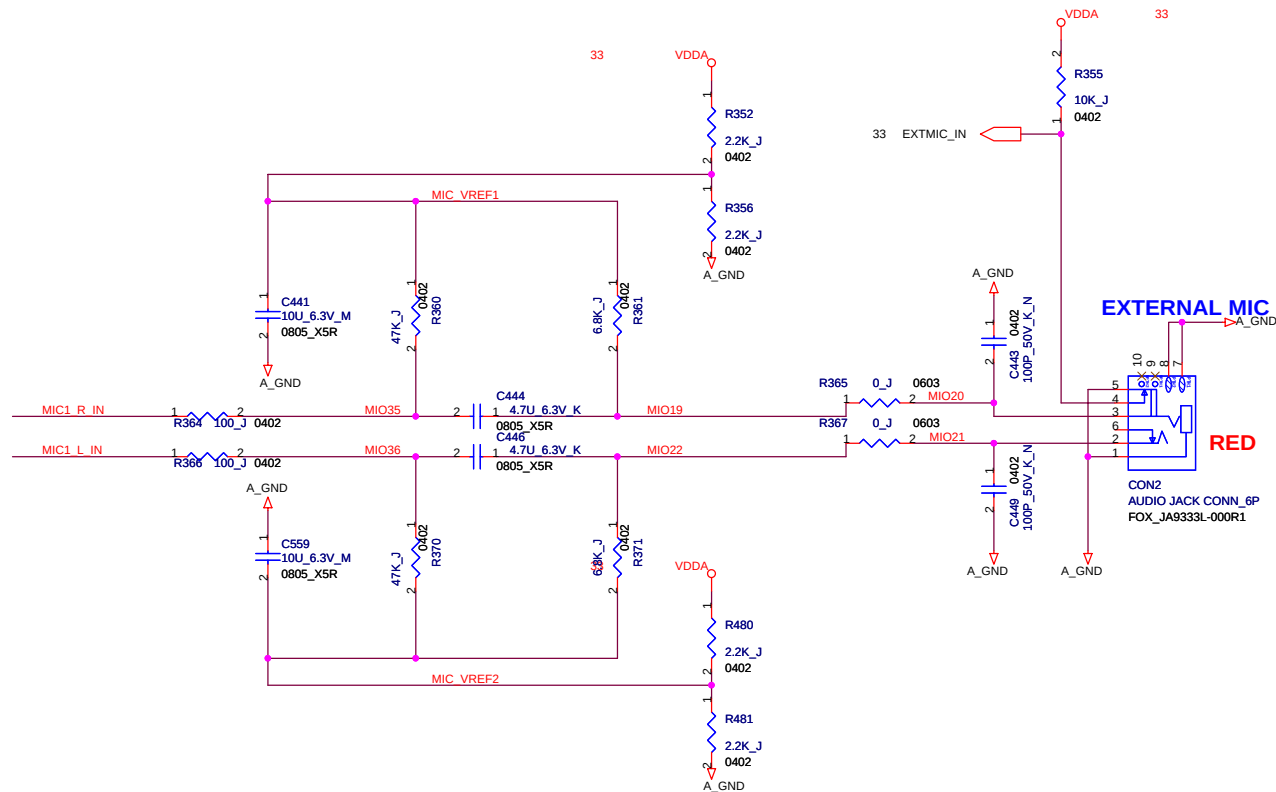
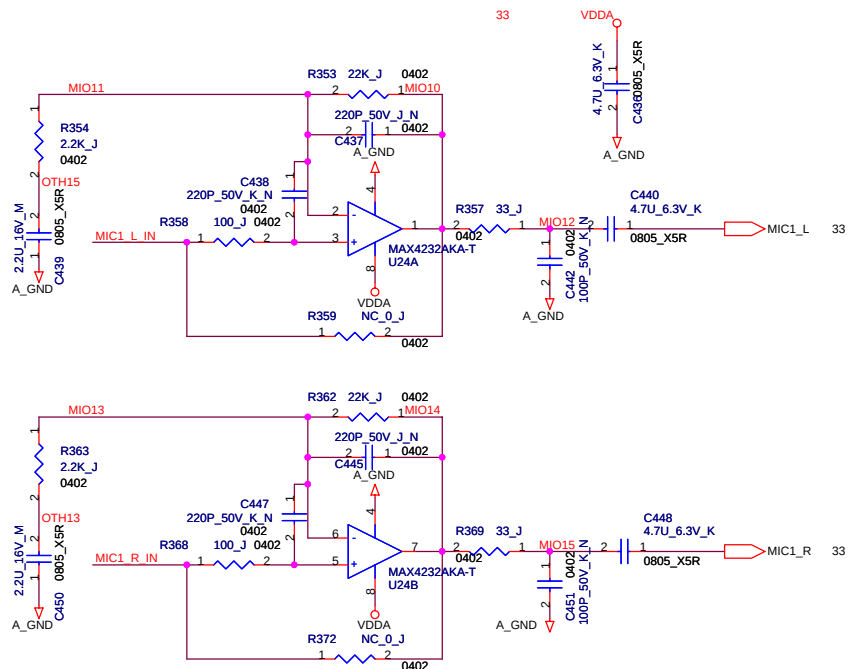
DVT Section: This section is responsible for controlling the fan's voltage. It includes a MOSFET (Q17) driven by the FAN1_TACH signal. The MOSFET's source is connected to ground, and its drain is connected to the fan's positive terminal. A diode (D8, BD4148FPT) is connected in parallel with the fan to prevent back EMF. A resistor (R304, 10K_F 0603) is connected between the +3VSUS supply and the fan's positive terminal. The fan's negative terminal is connected to ground.

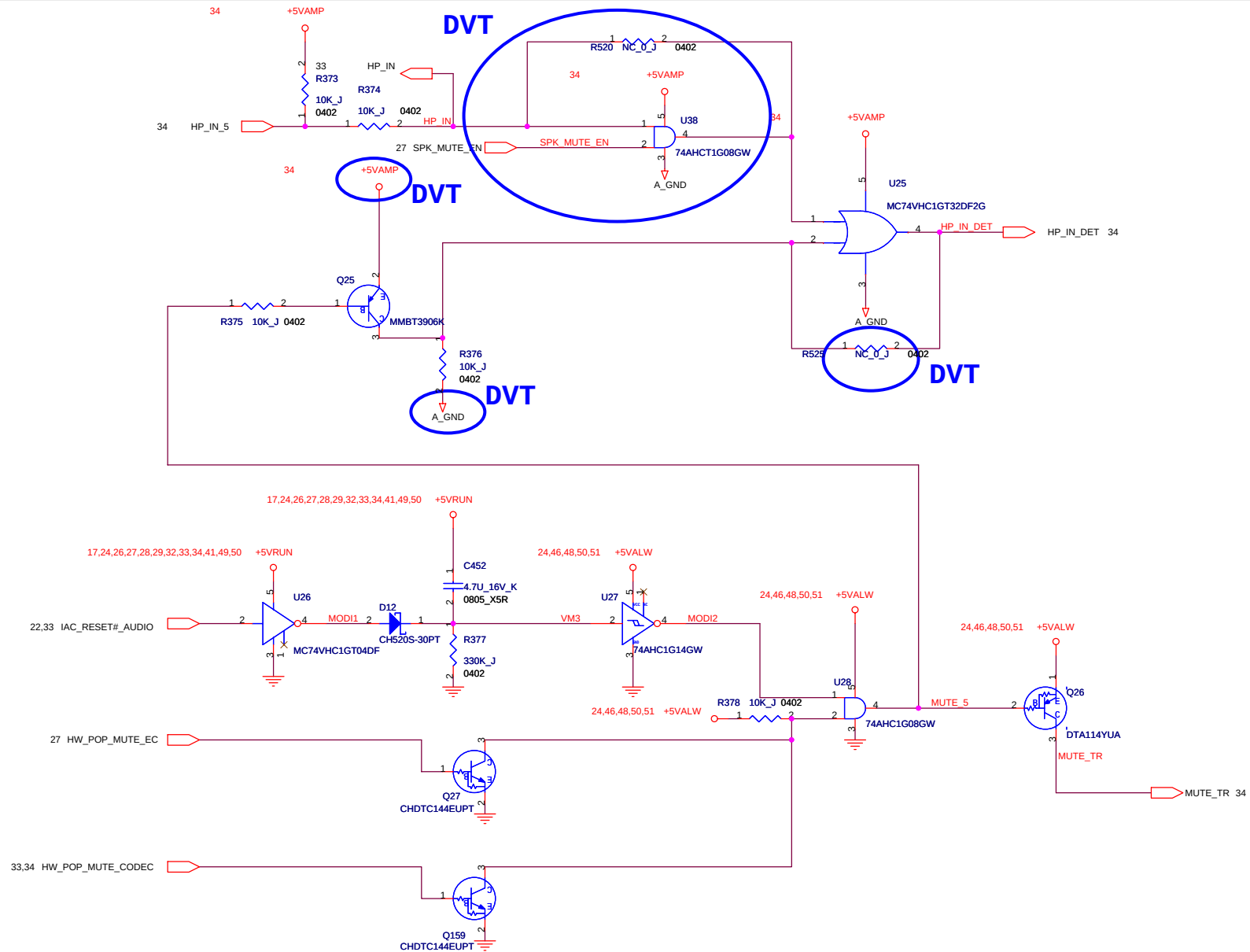
Power Supply: The circuit is powered by +5VSUS and +3VSUS. The +5VSUS supply is connected to the PVT section, and the +3VSUS supply is connected to the DVT section.

Components: The components used in the circuit include MOSFETs (Q157, Q17), diodes (D18, D8), resistors (R305, R306, R304), and capacitors (C369, C4405). The fan is connected to the FAN1 header (CN18) and the FAN1 header is connected to the FAN1 pin (FOX_HS8103E).

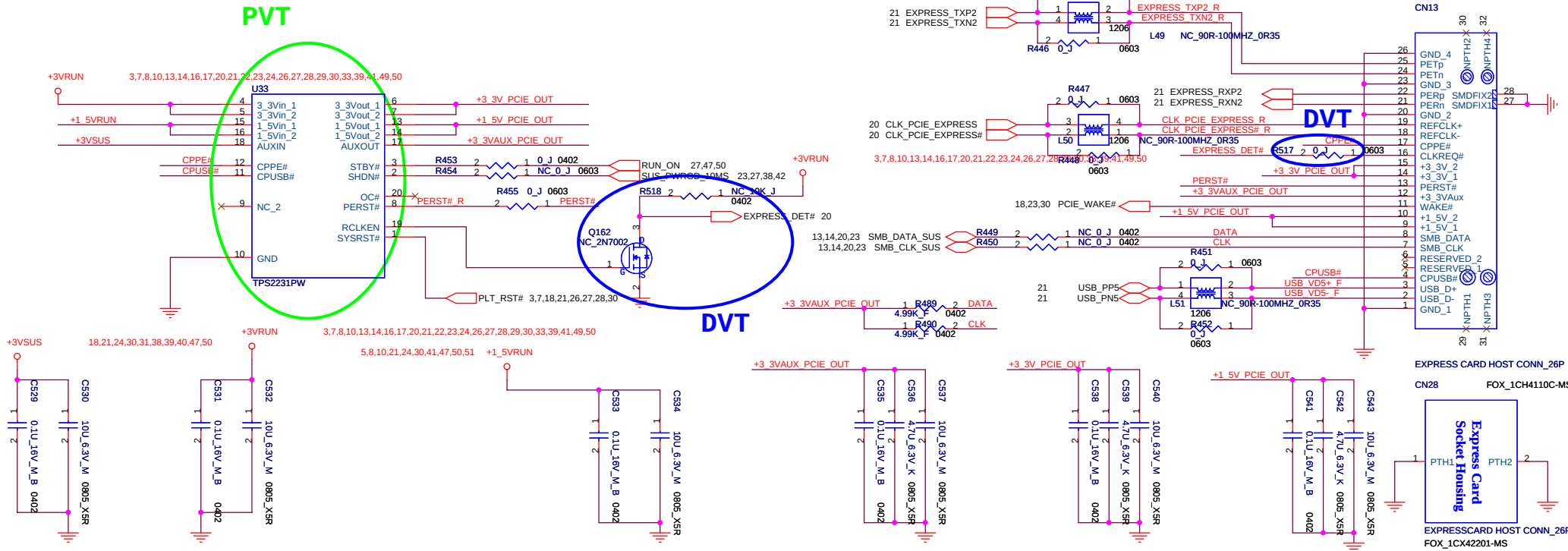




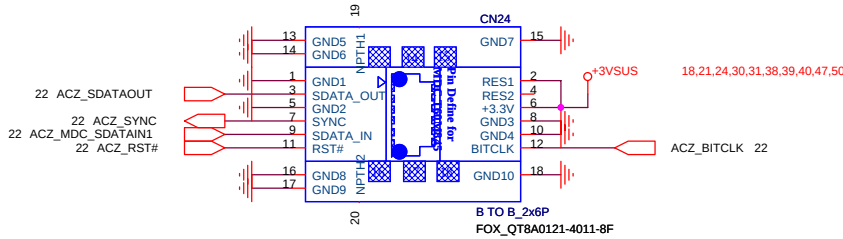


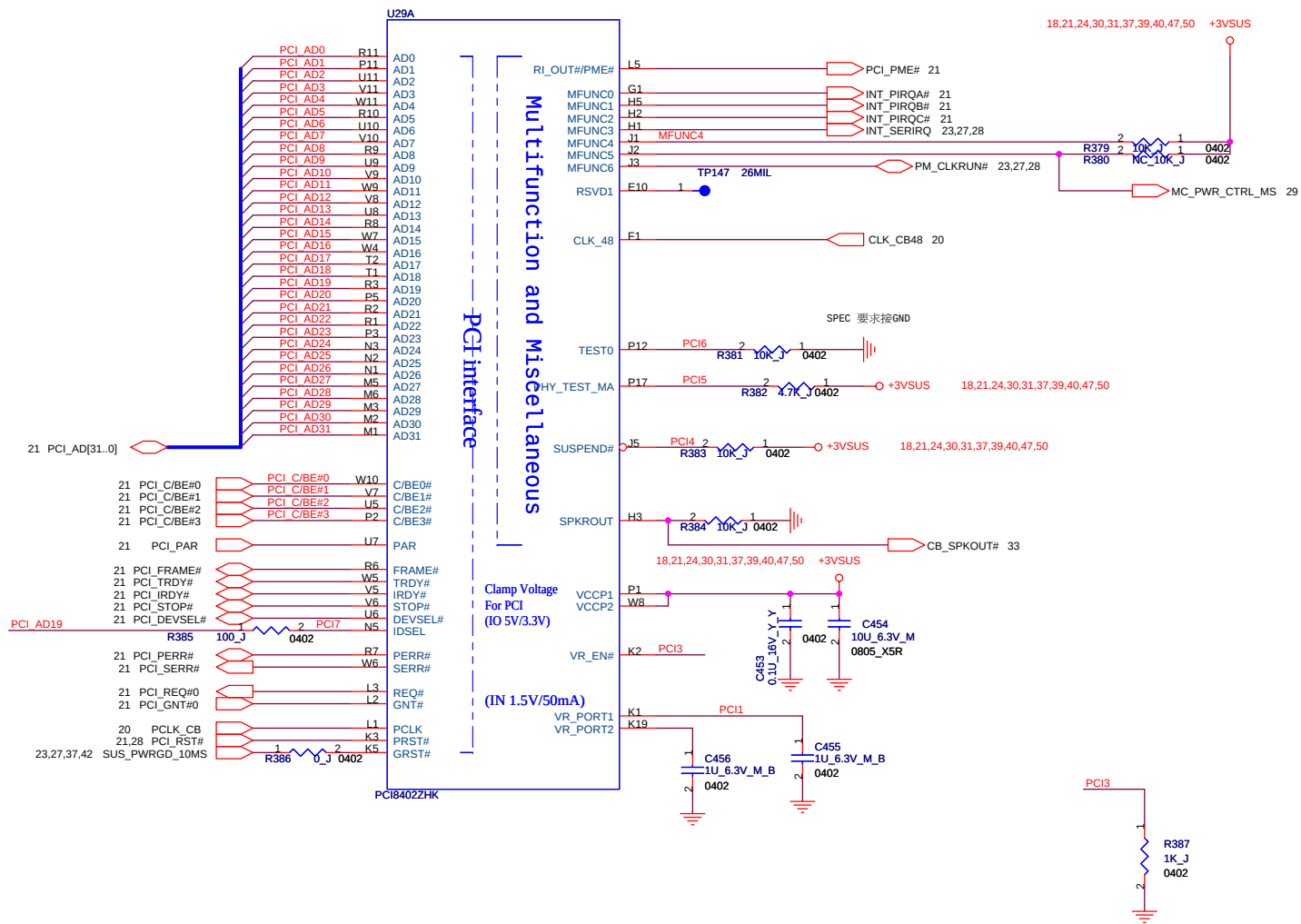


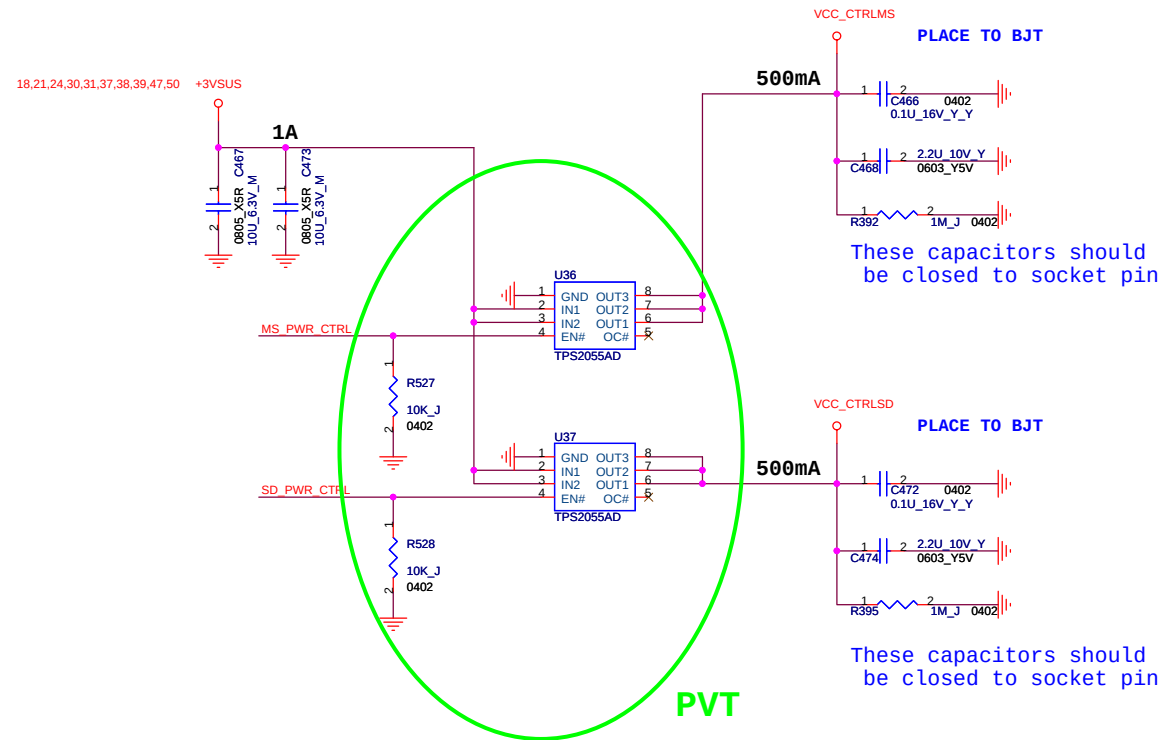
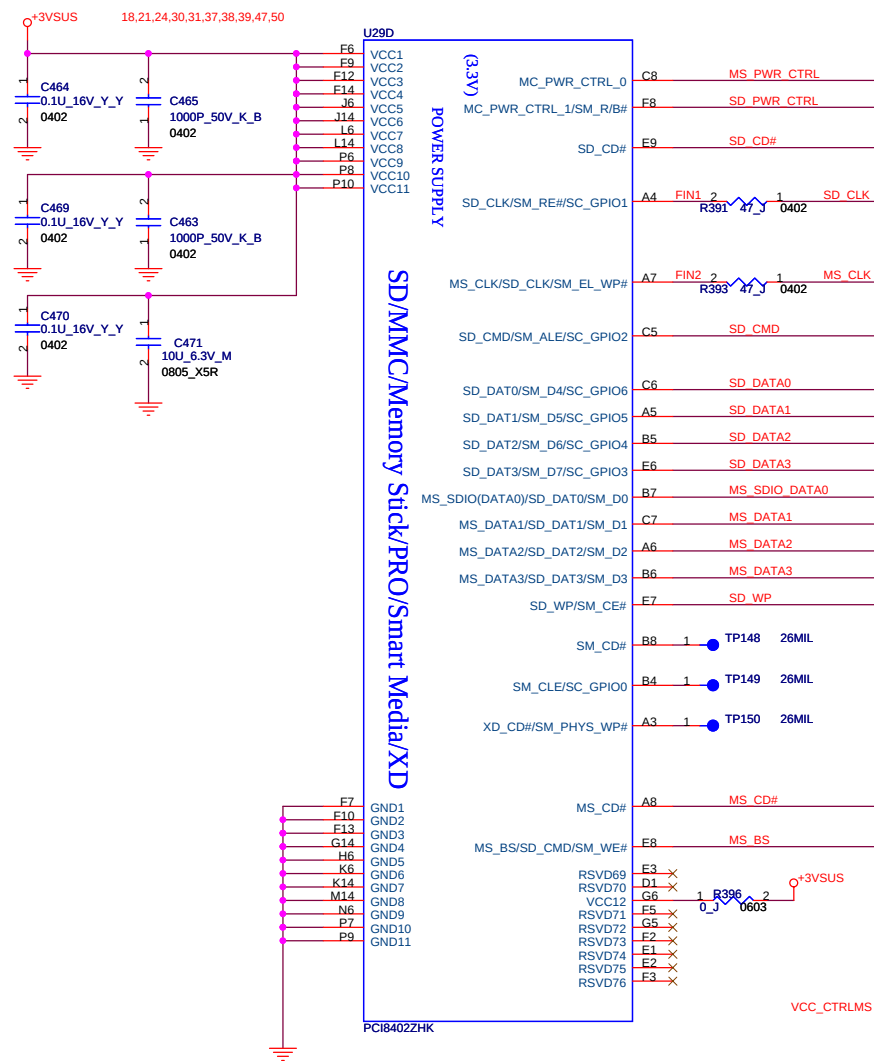
EXPRESS CONN



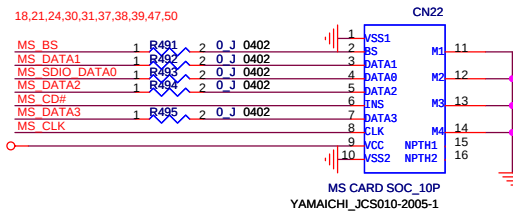
MDC CONN.



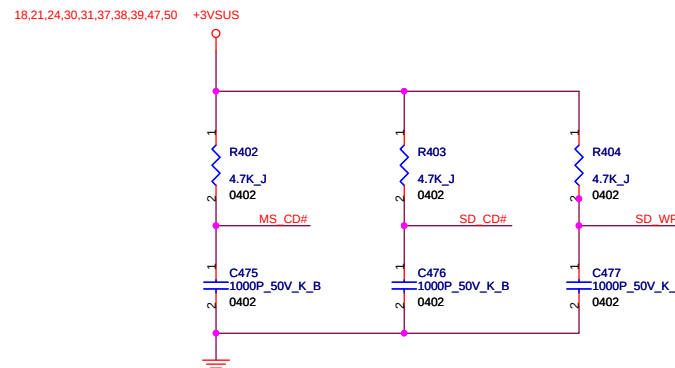
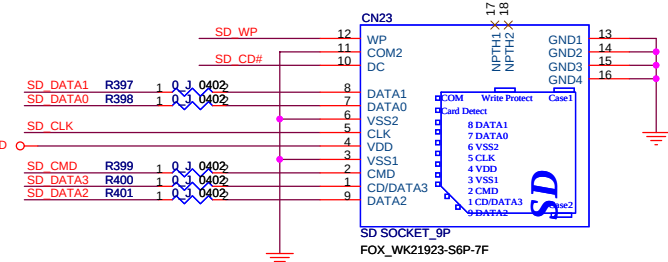




MS STD/DUO CONN.



SD CONN.

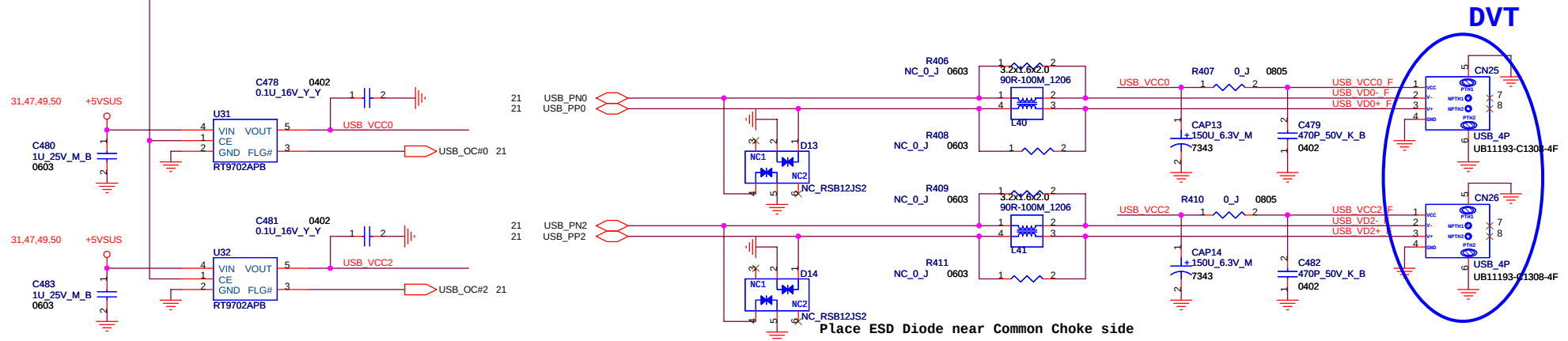


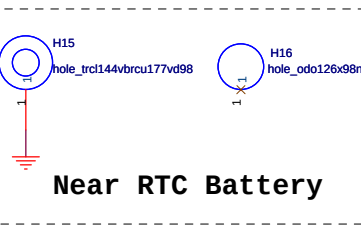
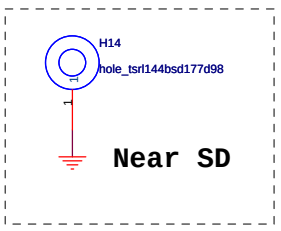
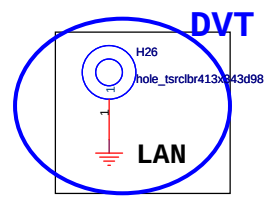
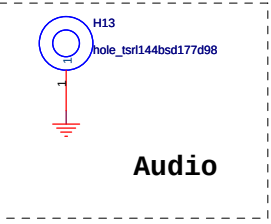
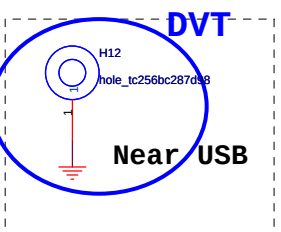
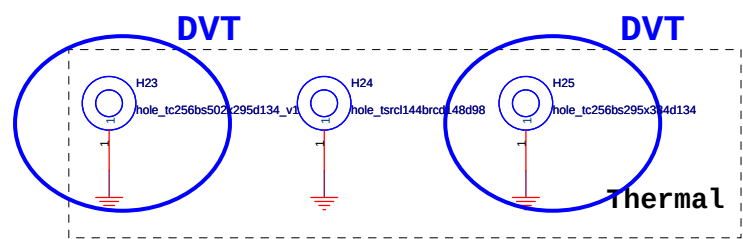
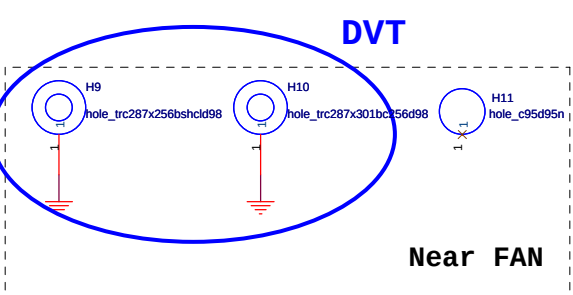
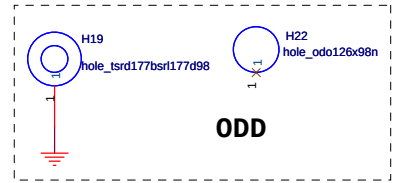
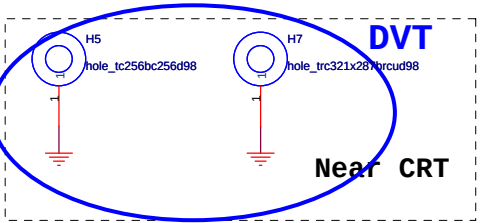
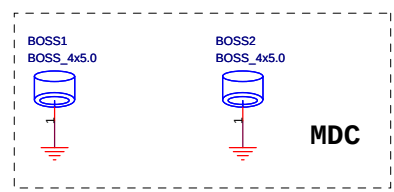
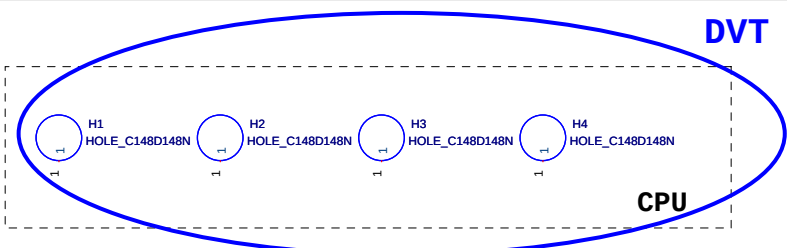
[illegible]

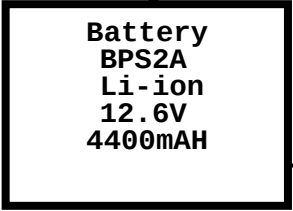
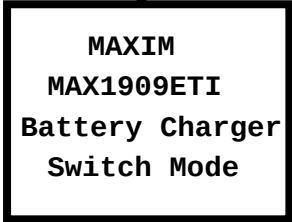
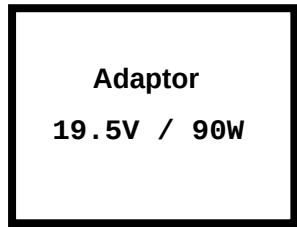
LID Switch

USB CONN X 2

23,27,37,38 SUS_PWRGD_10MS







DCBATOUT

ALW_ON



System

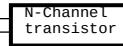
+5VALW/5A

System

+3VALW/5.5A

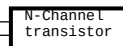
+5VALW_LDO
+ECVCC
ALW_PWRGD

SUS_ON



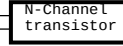
+5VSUS/0.5A

RUN_ON



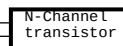
+5VRUN/3A

SUS_ON



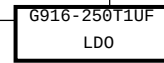
+3VSUS/1.2A

RUN_ON



+3VRUN/4.3A

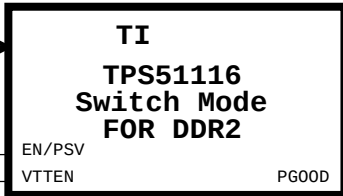
RUN_ON



+2_5VRUN/150mA

DCBATOUT

SUS_ON



+1_8VSUS/8.5A

+0_9VSUS/2A

DDRDIMM_VREF
DDR2_PWRGD

DCBATOUT

RUN_ON

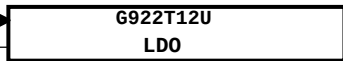


+1_05VRUN/9.5A

+1_5VRUN/6.5A

RUN_PWRGD

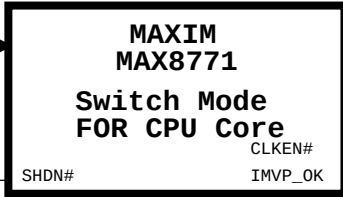
SUS_ON



+8V For Load switch

DCBATOUT

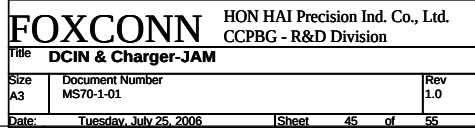
IMVP_VR_ON

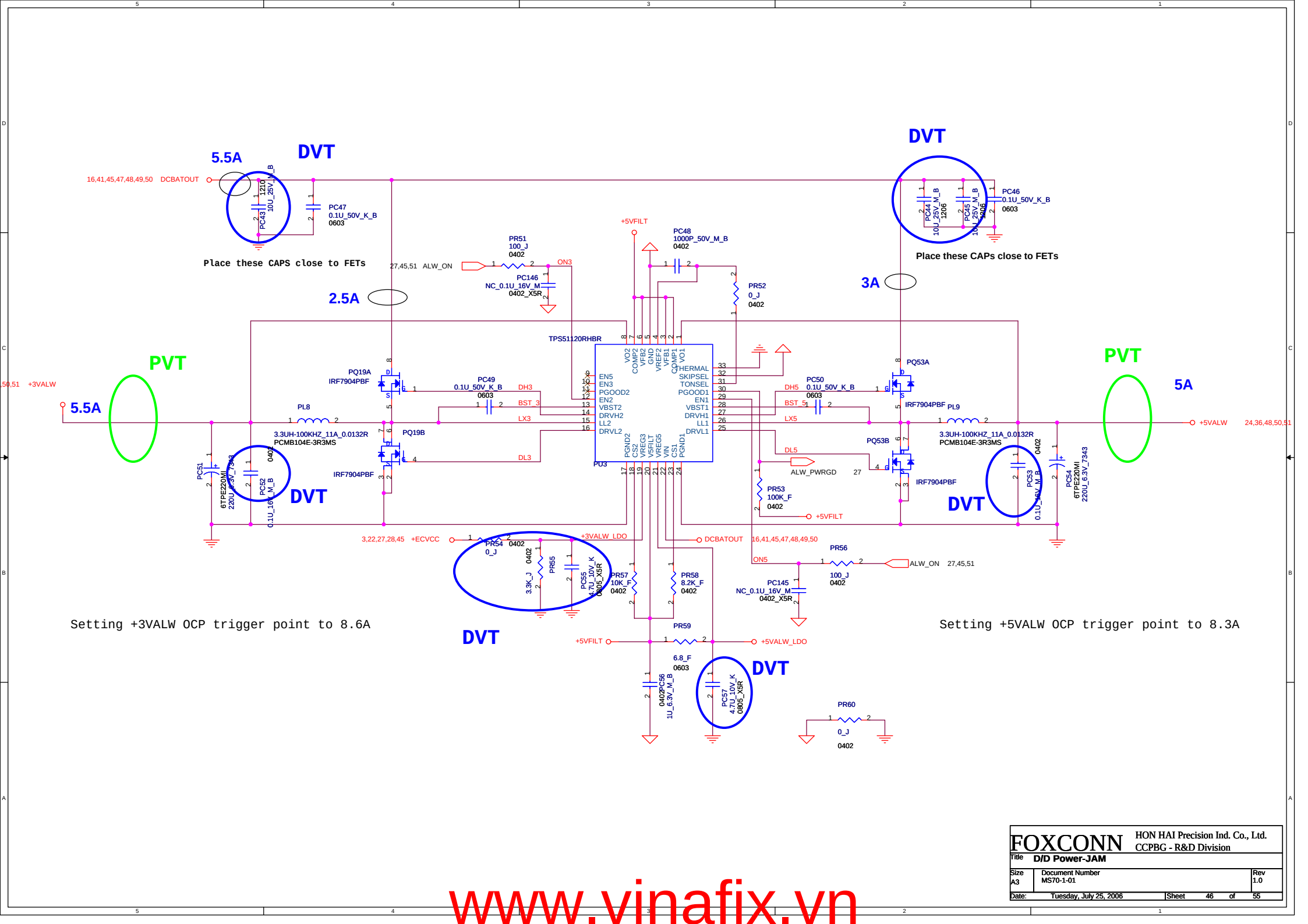


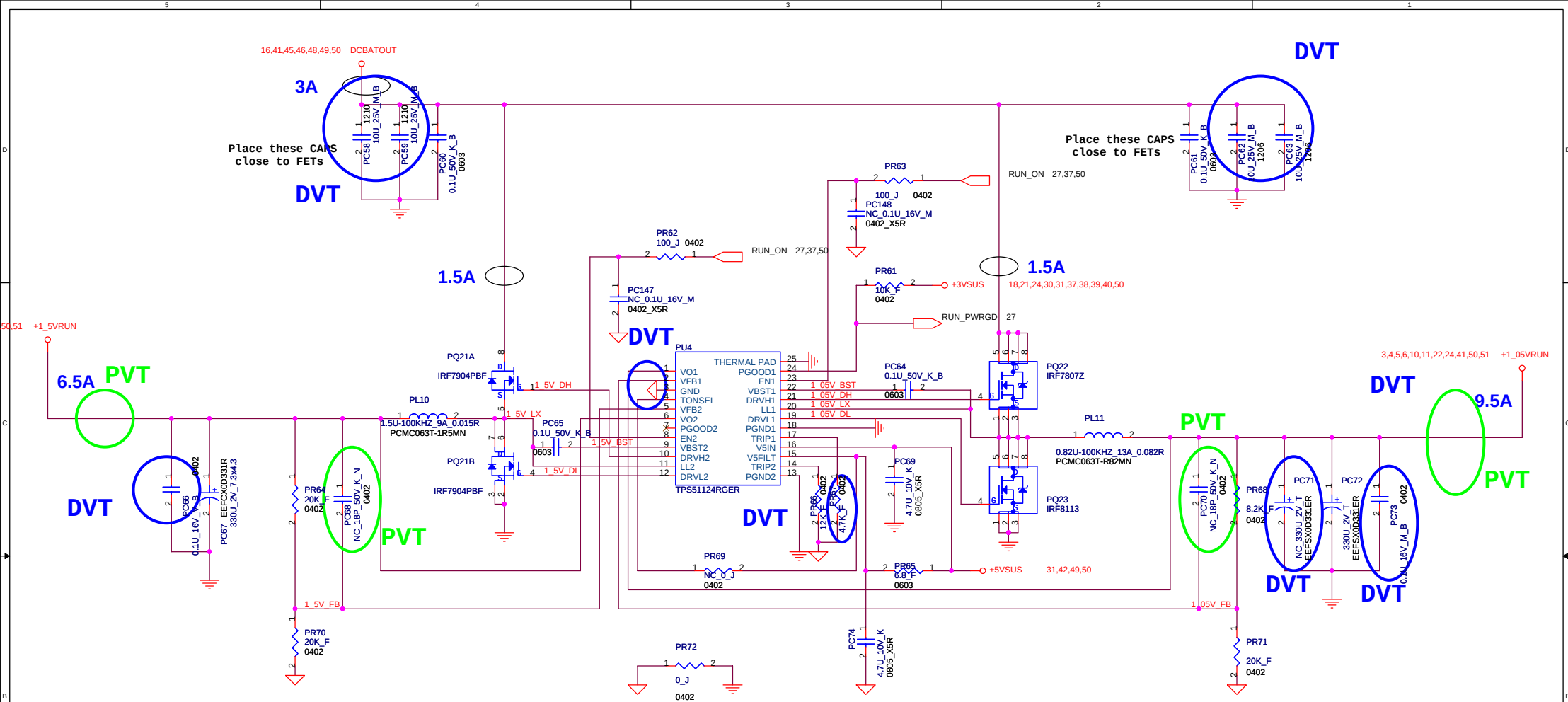
VHCORE/36A

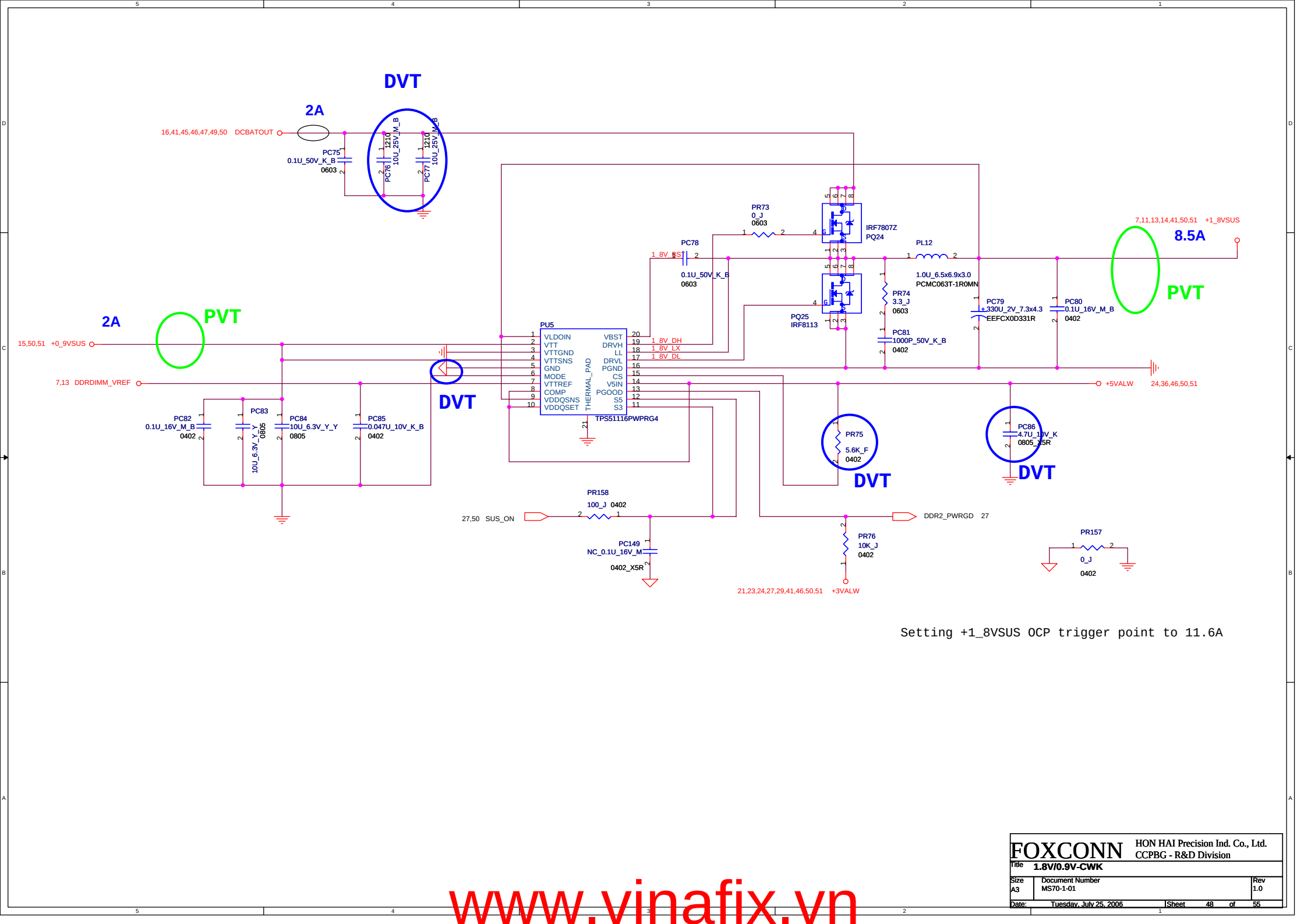
CLK_EN#

IMVP_OK

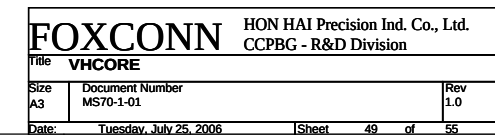


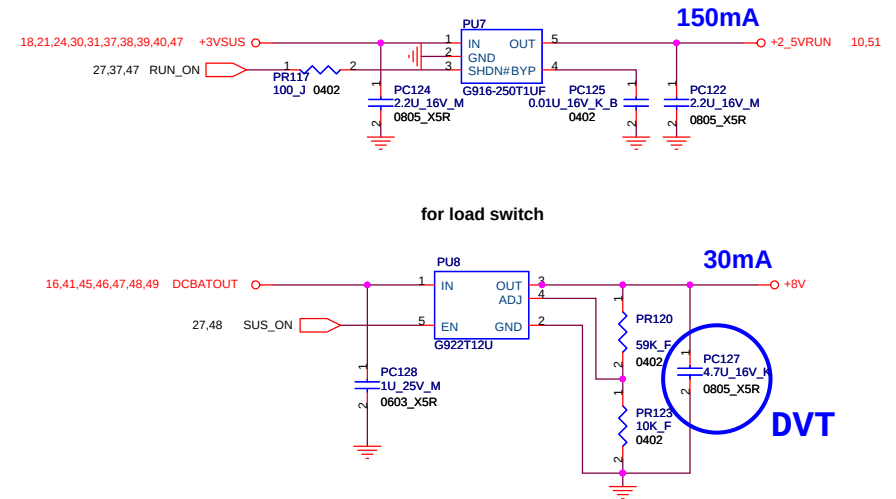
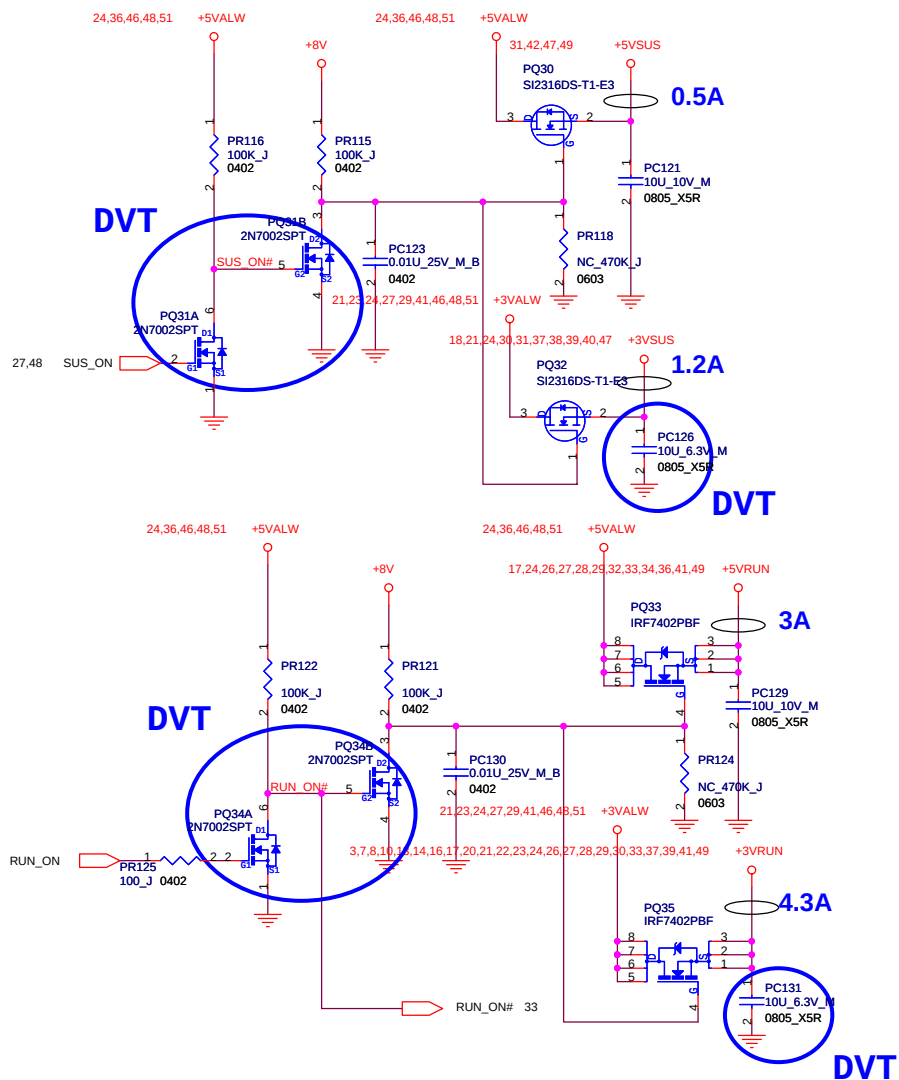




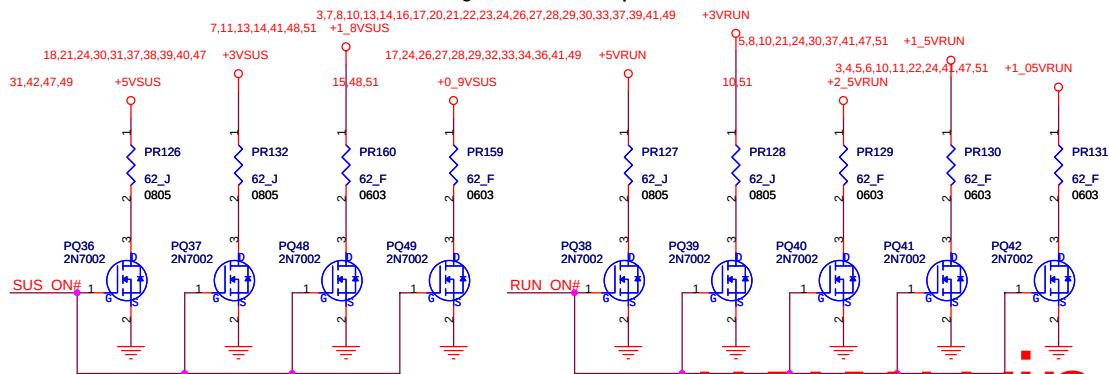


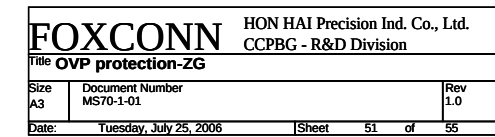
Setting +1_8VSUS OCP trigger point to 11.6A





Discharge circuit for power-off





HISTORY (1)

(2006/04/25)

P.16 CN3 pin5 Add R515 0ohm for QDI LCD Panel doesn't support gamma correction issue.
P.17 Add VGA_CRT_DET# connect to U15 pin29 for Semi-PnP function fail issue.
P.20 U11 pin57 add R516 10Kohm pull down for LAN can't be recognized issue.
P.27 U15 pin29 add R513 10Kohm pull up for Semi-PnP function fail issue.
P.27 U15 pin12 add R514 100Kohm pull down for EC hardware strap pin.
P.27 U15 pin171 add C597 1000pF to ground for FAN can't be controlled issue.
P.31 R304 change from 4.7k to 10k for FAN can't be controlled issue.

(2006/05/03)

P.49 Add netname(IMVP_PHASEGD_1) on the right side of PR119 for application modification.
P.45 PC11, PC21, PC151, PR167 change from DNI to mount for DC_IN spike issue
P.45 PD4 pin1 and pin3 exchange for application modification
P.46 PR54 change from 100 ohm to 0 ohm for PU3 output abnormal issue
P.46 PR55 change from DNI to mount for can't boot up issue
P.47 PU4 pin3 change from GND to GND_SIGNAL_1D5V for application modification
P.48 PU5 pin5 change from GND to GND_SIGNAL_1D8V for application modification
P.49 Add PR169 NC_1M ohm for MAX8771 CCI issue
P.49 PC96, PC97, PC98, PC111, PC112, PC114 change from SANYO 2R5TPL330M9 to Panasonic EEF5X0D331XE for purchase difficult

(2006/05/04)

P.37 Add Q162(NC), R517, R518(NC) for Express card power sequence issue

(2006/05/15)

P.45 PR32 change from 22K_F to 23.2K_F for ACIN Vcls function trigger point correct to 3.4A
P.47 PR67 change from 8.2K_F to 4.7K_F for +1_05VRUN OCP trigger point correct to 12.8A
P.48 PR75 change from 6.8K_F to 5.6K_F for +1_8VSUS OCP trigger point correct to 11.6A
P.51 PR146 change from 51K_F to 46.4K_F for DCBATOUT OCP trigger point correct to 4.2A
P.51 PR150 change from 62K_F to 56K for PWRLIMIT# function trigger point correct to 3.6A
P.46 Delete PJ1, PJ2
P.47 Delete PJ3, PJ4, PJ5, PJ6
P.48 Delete PJ7, PJ8, PJ9

(2006/05/17)

P.45 Add PR41 10K_J_0402 and PQ13 2N7002 for preventing leakage current
P.45 PR17 change from 0.015_J 0805 to 0.015_F 1206 for application modification
P.46 PR55 change from 1K_J to 3.3K_J and PC55, PC57 change from 10u_25V X5R 1206 to 4.7u_10V X5R 0805 for reducing +ECVCC static current
P.47 PC71 change from mount to DNI for application modification
P.49 PR110 change from 20K_J to 0_J and PC102 change from DNI to mount for MAX8771 CCI issue
P.45 Delete PR19, PR28, PR33, PR35, PR37, PR38, PR39, PR40, PC31, PQ7, PQ10, PQ14, PQ16 For +ECVCC needed to work in battery only mode
P.51 Delete PD36, PD37 for +ECVCC needed to work in battery only mode
P.51 The net of VSOURCE (PQ43 pin3) change to DCBATOUT for +ECVCC needed to work in battery only mode
P.51 The net of BATT_EN (PD38 pin2) change to ALW_ON for +ECVCC needed to work in battery only mode

(2006/05/19)

P.13 C155 change from 2.2U_10V_Y_Y to 1000P_16V_K ; C159 change from 0.1U_16V_Y_Y to 1000P_50V_K for EMC DDR2 solution
P.14 C168 change from 2.2U_10V_Y_Y to 1000P_16V_K ; C172 change from 0.1U_16V_Y_Y to 1000P_50V_K for EMC DDR2 solution
P.15 C177,C179,C181,C191,C192,C196 change from 0.1U_16V_Y_Y to 1000P_50V_K for EMC DDR2 solution
P.39 C547,C548 change from 18P_50V_J_N to 22P_50V_J for PCI8402's Crystal issue
P.30 LED1 change from HT-110Y to HT-110UYG for LED color requirement
P.45 PCN1 change from MOLEX_53259-0229 to FOX_GS53020-00580-7F
P.45 PC11 change from 10U_25V_M_1206 to 10U_25V_M_B_1210 for purchase convenient
P.46 PC43,PC44,PC45 change from 10U_25V_M_B_1206 to 10U_25V_M_B_1210 for purchase convenient
P.47 PC58,PC59,PC62,PC63 change from 10U_25V_M_B_1206 to 10U_25V_M_B_1210 for purchase convenient
P.48 PC76,PC77 change from 10U_25V_M_B_1206 to 10U_25V_M_B_1210 for purchase convenient
P.48 PC86 change from 4.7U_10V_K_B_1206 to 4.7U_10V_K_0805 for purchase convenient
P.50 PC126,PC131 change from 10U_10V_M to 10U_6.3V_M for purchase convenient
P.50 PC127 change from 4.7U_25V_K_B_1206 to 4.7U_16V_K_0805 for purchase convenient

(2006/05/22)

P.32 CN21 change from FOXCONN_GB11060_0221_7F to FOXCONN_GB5RF060_1200_7F for ME's requirement
P.29 CN30,CN31 change from foxconn_gb11120_0221_7F to FOXCONN_GB5RF120_1200_7F for ME's requirement
P.29 CN31 change from mount to DNI for ME's requirement
P.50 PQ31,PQ34 change from DIODES,2N7002DW-7-F to CHENMKO,2N7002SPT for purchase convenient
P.51 PQ45 change from DIODES,2N7002DW-7-F to CHENMKO,2N7002SPT for purchase convenient
P.27 Q149 change from DIODES,2N7002DW-7-F to CHENMKO,2N7002SPT for purchase convenient

(2006/05/23)

P.47 PC62,PC63 change from 10U_25V_M_B_1210 to 10U_25V_M_B_1206 for ME limit of height
P.46 PC44,PC45 change from 10U_25V_M_B_1210 to 10U_25V_M_B_1206 for ME limit of height
P.46 Add PJ1,PJ2 for test request
P.47 Add PJ3,PJ4 for test request
P.48 Add PJ7,PJ9 for test request

(2006/05/24)

P.42 CN25,CN26(USB CONN) change from FOX_UB11193_C1301_4F to UB11193-C1308-4F for ME's requirement
P.17 CN5(VGA CONN) change from FOX_DZ11A91_MB221_4F to DZ11A91-MW223-4F for ME's requirement

(2006/05/25)

P.47 Add PJ6 for test request
P.26 CN8 footprint change from FOXCONN_LD2722H_S469 to FOXCONN_LD2722H_S469_MS70 for ME PAD request
P.32 C389 change from 22U_10V_Y_Y_1206 to 10U_10V_M_0805 and add C598 10U_10V_M_0805 for limit of ME
P.43 H1,H2,H3,H4 change from hole_c158d158n to HOLE_C148D148N for ME request
P.43 H7 change from hole_tsru144bsru177d98 to hole_trc321x287brcd98 for ME request
P.43 H26 change from hole_c120d100 to hole_tsrlclbr413x343d98 for ME request
P.43 H23 change from hole_tc256brclD295d98_v1 to hole_tc256bs502x295d134_v1 for ME request
P.43 H25 change from hole_tc256brcu148d98 to hole_tc256bs295x384d134 for ME request
P.43 H5 change from hole_tc256bc315d98 to hole_tc256bc256d98 for ME request
P.43 H10 change from hole_tshrd144bc315d98 to hole_trc287x301bc256d98 for ME request
P.43 H9 change from hole_trcd144brcl177d98 to hole_trc287x321brcd98 for ME request
P.43 H12 change from hole_tc256bsrcu144d98 to hole_tc256bc287d98 for ME request

(2006/05/26)

P.42 CN25,CN26 change from FOXCONN_UB11193_C1308_4F to FOXCONN_UB11193_C1308_4F_HM for solder issue
P.17 D3 change from 16-CH500H4-0P00 to 16-SCS500V-4000 for purchase convenient
P.10 C119 change from 1C-2B30105-K000 to 1C-2B30475-K100 ; C120 change from 1C-2B20103-K001(0402) to 1C-2B30475-K100(0603) for +1_5VRUN_HMPLL noise issue
P.48 Add PJ8 for test request

(2006/06/01)

P.16 Add R519(0ohm 0402) for desinger set "LCDID3" to "0" by mistake.
P.49 PC102 change from mount to NC for application modification
P.46 PC52,PC53 change from 0.1U_16V_Y_Y(Y5V) to 0.1U_16V_M_B(X5R) for application modification
P.47 PC66,PC73 change from 0.1U_16V_Y_Y(Y5V) to 0.1U_16V_M_B(X5R) for application modification
P.49 PC99,PC113 change from 0.1U_16V_Y_Y(Y5V) to 0.1U_16V_M_B(X5R) for application modification
P.36 Q25 pin2 netname change from +5VRUN to +5VAMP
P.36 R376 pin2 netname change from GND to A_GND
P.36 Add U38,R520(NC) for SPK_MUTE_EN for Vista requirement
P.36 Add NET "SPK_MUTE_EN" from U38 pin2 to U15 pin99 for Vista requirement
P.40 Change U36,U37 from RT9702 to RT9703, Add R521-R524.
P.27 Delete Q149.

(2006/06/02)

P.16 R515,R519 change from mount to NC
P.36 Add R525(NC) for Audio mute option
P.49 Add PC152 for application modification
P.26 R510 change from mount to NC for application modification
P.22 R188 change from mount to NC for application modification

(2006/06/05)

P.49 PC92,PC108 change from NC to mount for design rating
P.40 U36,U37 change from RT9703 to RT9702, Del R521-R524 for RT9703 phase out issue
P.49 Add PC153 for solving audible noise
P.19 Add R526 for LAN application modification

(2006/06/06)

P.13 Add C599,C600(1000P_50V_K) ; C155 change from 1000P_16V_K to 2.2U_10V_Y_Y ; C159 change from 1000P_50V_K to 0.1U_16V_Y_Y for EMC solution
P.14 Add C601,C602(1000P_50V_K) ; C168 change from 1000P_16V_K to 2.2U_10V_Y_Y ; C172 change from 1000P_50V_K to 0.1U_16V_Y_Y for EMC solution
P.15 Add C603,C604(1000P_50V_K) ; C177,C179,C181,C191,C192,C196 change from 1000P_50V_K to 0.1U_16V_Y_Y for EMC solution
P.51 Add PD36,PD37 for application modification
P.19 C253 change form 0.1U_16V_M_B to 5P_50V_C ; C254 change from 5P_50V_C to 0.1U_16V_M_B ; Add L58 ; Del R526 for LAN application modification

FOXCONN			HON HAI Precision Ind. Co., Ltd.
History (1)			CCPBG - R&D Division
Size	Document Number	Rev	
C	MS70-1-01	1.0	
Date:	Tuesday, July 25, 2006	Sheet	52 of 55

HISTORY (2)

(2006/06/07)
P.26 R245 change from NC to mount for application modification

(2006/06/13)
P.33 R325 change from mount to NC for acoustic noise.
P.36 U38 change from 74AHC1G08GW to 74AHCT1G08GW for Vih can't meet EC spec.

PVT

(2006/07/12)
P.47 Change PC68, PC70 from mount to NC for TPS51124 OVP issue.
P.27 Add R526 (1K ohm) series on ALW_ON net to prevent EC damage issue.
P.46 Delete PJ1, PJ2
P.47 Delete PJ3, PJ4, PJ6
P.48 Delete PJ7, PJ8, PJ9
P.32 F1,R320,R321,L32,C598,C389,C390,C391,CN21 change from mount to NC for cancel Oide function
P.37 U33 change from 15-TPS2231-0000(24pin) to 15-TPS2231-0002(20pin) for purchase convenient
P.40 U36,U37 change from 15-RT9702A-0000 to 15-TPS2055-0000 ;
Add R527,R528 for MS_PWR_CTRL and SD_PWR_CTRL are recognized to be high level by accident

(2006/07/20)
P.26 CN9 vendor part number change from QT8H0506-13T3R-7F to QT8H0506-13T3R-4F
for packing type change.
P.49 PC153 change from 1C-10X0107-M403 to 1C-1XX0107-M400 for purchase convenient.
P.29 Delete CN31 for touch pad application modification.
P.22 R195 change from 47ohm to 0ohm ; C293 change from NC to mount for EMI solution.
P.29 LED6 change from 16-HT210DY-G000 to 16-HT210UD-UY00 for ME brightness issue.
LED5,LED7 change from 16-HT110Y0-0000 to 16-HT110UY-0000 for ME brightness issue.

(2006/07/21)
P.26 Add D22(NC) for ESD solution
P.30 R301 change from 120ohm to 47ohm for ME brightness issue

(2006/07/25)
P.30 C365 change from NC to mount for WLAN power ripple noise issue
P.26 Add VR1 for ESD solution
P.29 Add VR2,VR3(NC) for ESD solution
P.41 Add VR4,VR5(NC) for ESD solution

(2006/07/28)
P.29 Q155 change from 17-CHDTC14-4E01 to 17-2N70020-0000 for ME brightness issue.

(2006/07/31)
P.30 R301 change from 47ohm to 120ohm (LED1 is 10mA) for ME brightness issue
P.29 R418 change from 47ohm to 62ohm (LED5 is 18.75mA) for ME brightness issue
P.29 R424 change from 47ohm to 62ohm (LED6 is 19.5mA)
R425 change from 47ohm to 120ohm (LED6 is 10mA)for ME brightness issue
P.29 R426 change from 47ohm to 62ohm (LED7 is 18.9mA)

(2006/08/01)
P.31 Q17 change from 17-ME2301T-1000 to 17-S12301B-DS00 for Fan rotational speed issue