Compal Confidential

C5PM2 MB Schematic Document

LA-E361P

Rev:1.0

2016.10.27

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.		
Title: Cover Sheet		
Size: Custom	Document Number: C5PM2_LA-E361P	Rev: 1.0
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HDMI Conn.

HDMI
PS8407A
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HDMI x 4 lanes

eDP

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eDP

DDI

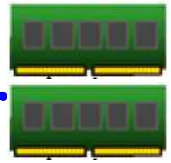
Kabylake H PROCESSOR
BGA1440
(42X28) (SKL-H_4+2)

Processor page 06~13

Memory BUS
Dual Channel

1.2V DDR4 1333/1600

Interleaved Memory



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260pin DDR4-SO-DIMM X1
BANK 4, 5, 6, 7 page 15

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Card Reader
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on SUB/B

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CLK=24MHz

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PS2 / I2C

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Sub Board

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FUN/B page 33

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LED/B page 33

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Title: Block Diagrams

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Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	V_{BID} min	V_{BID} typ	V_{BID} max	EC AD
0	0		0.000 V	0.300 V	0x00 - 0x13
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x14 - 0x1E
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1F - 0x25
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x26 - 0x30
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3A
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B - 0x45
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 - 0x54
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64
8	75K +/- 1%	1.398 V	1.414 V	1.430 V	0x65 - 0x76
9	100K +/- 1%	1.634 V	1.650 V	1.667 V	0x77 - 0x87
10	130K +/- 1%	1.849 V	1.865 V	1.881 V	0x88 - 0x96
11	160K +/- 1%	2.015 V	2.031 V	2.046 V	0x97 - 0xA4
12	200K +/- 1%	2.185 V	2.200 V	2.215 V	0xA5 - 0xAF
13	240K +/- 1%	2.316 V	2.329 V	2.343 V	0xB0 - 0xB7
14	270K +/- 1%	2.395 V	2.408 V	2.421 V	0xB8 - 0xBF
15	330K +/- 1%	2.521 V	2.533 V	2.545 V	0xC0 - 0xC9
16	430K +/- 1%	2.667 V	2.677 V	2.687 V	0xCA - 0xD4
17	560K +/- 1%	2.791 V	2.800 V	2.808 V	0xD5 - 0xDD
18	750K +/- 1%	2.905 V	2.912 V	2.919 V	0xDE - 0xF0
19	NC	3.000 V	3.000 V		0xF1 - 0xFF

Power State

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

I2C Address Table

BUS	Device	Address(7 bit)	Address(8bit) Write	Address(8bit) Read
I2C_0 (+3VS)	Touch Panel	reserved		
I2C_1 (+3VS)	TM-P2969-001 (Touch Pad)			
	SB8787-1200 (Touch Pad)			
PCH_SMBCLK (+3VS)	DIMM1			
	DIMM2			
	LIS3DHTR(G-sensor)	0x30		
PCH_SML1CLK (+3VS)	N17P-GX (VGA)	0x9E		
	EC			
EC_SMB_CK1 (+3VLP)	BQ24780 (Charger IC)	0x12		
	BATTERY PACK	0x16		

BOM Structure Table

BOM Option Table

Item	BOM Structure
Unpop	@
Connector	CONN@
EMC requirement	EMC@
EMC requirement depop	XEMC@
UMA only	UMA@
TPM	TPM@
CMC	CMC@
LPC MODE for EC	LPC@
BA Serial	BA@
dGPU	VGA@
N17P-G0	G0@
N17P-G1	G1@
VRAM BOM Select	X76@
DMIC*1	DMIC@
[illegible]	IOAC@
[illegible]	NIOAC@
FPC	FP@

Voltage Rails

Power Plane	Description	S0	S3	S4	S5
+RTCVCC	RTC Battery Power	ON	ON	ON	ON
+19V_VIN	Adapter power supply	N/A	N/A	N/A	N/A
+12.6V_BATT	Battery power supply	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A	N/A
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON
+5VALW	+5V Always power rail	ON	ON	ON	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON
+3VALW_PCH_PRIM	+3VALW power for PCH power rails	ON	ON	ON	ON*
+3VALW_SPI	+3VALW_PRIM supply for the SPI IO	ON	ON	ON	ON
+1.0VALW	+1.0V Always power rail	ON	ON	ON	ON
+1.2V_VDDQ	DDR4 +1.2V power rail	ON	ON	OFF	OFF
+1.0V_VCCST	Sustain voltage for processor in Standby modes	ON	ON	OFF	OFF
+5VS	System +5V power rail	ON	OFF	OFF	OFF
+3VS	System +3V power rail	ON	OFF	OFF	OFF
+1.0VS_VCCSTG	+1.0VALW_PRIM Gated version of VCCST	ON	OFF	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator .	ON	OFF	OFF	OFF
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF	OFF
+VCCIO	CPU IO power rail	ON	OFF	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF	OFF
+1.8VSDGPU_AON	+1.8VS power rail for GPU(AON rails)	ON	OFF	OFF	OFF
+1.8VSDGPU_MAIN	+1.8VS power rail for GPU GC6	ON	OFF	OFF	OFF
+VGA_CORE	Core voltage for VGA	ON	OFF	OFF	OFF
+1.35VSDGPU	+1.35VS power rail for GPU	ON	OFF	OFF	OFF
+1.0VSDGPU	+1.0VS power rail for GPU	ON	OFF	OFF	OFF
+VGA_CORE_S	Core voltage for VGA				

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

43 level BOM table

43 Level	Description	BOM Structure
431A5HB0L14	SMT MB AE361 C5PM2 I57300 G0 2G HDMI	I573@/NIOAC@/VGA@/G0@/2G@
431A5HB0L15	SMT MB AE361 C5PM2 I57300 G0 4G HDMI	I573@/NIOAC@/VGA@/G0@/4G@
431A5HB0L16	SMT MB AE361 C5PM2 I77700 G0 2G HDMI	I777@/NIOAC@/VGA@/G0@/2G@
431A5HB0L17	SMT MB AE361 C5PM2 I77700 G0 4G HDMI	I777@/NIOAC@/VGA@/G0@/4G@
431A5HB0L18	SMT MB AE361 C5PM2 I57300 G1 2G HDMI	I573@/NIOAC@/VGA@/G1@/2G@
431A5HB0L19	SMT MB AE361 C5PM2 I57300 G1 4G HDMI	I573@/NIOAC@/VGA@/G1@/4G@
431A5HB0L20	SMT MB AE361 C5PM2 I77700 G1 2G HDMI	I777@/NIOAC@/VGA@/G1@/2G@
431A5HB0L21	SMT MB AE361 C5PM2 I77700 G1 4G HDMI	I777@/NIOAC@/VGA@/G1@/4G@

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Title: Notes List

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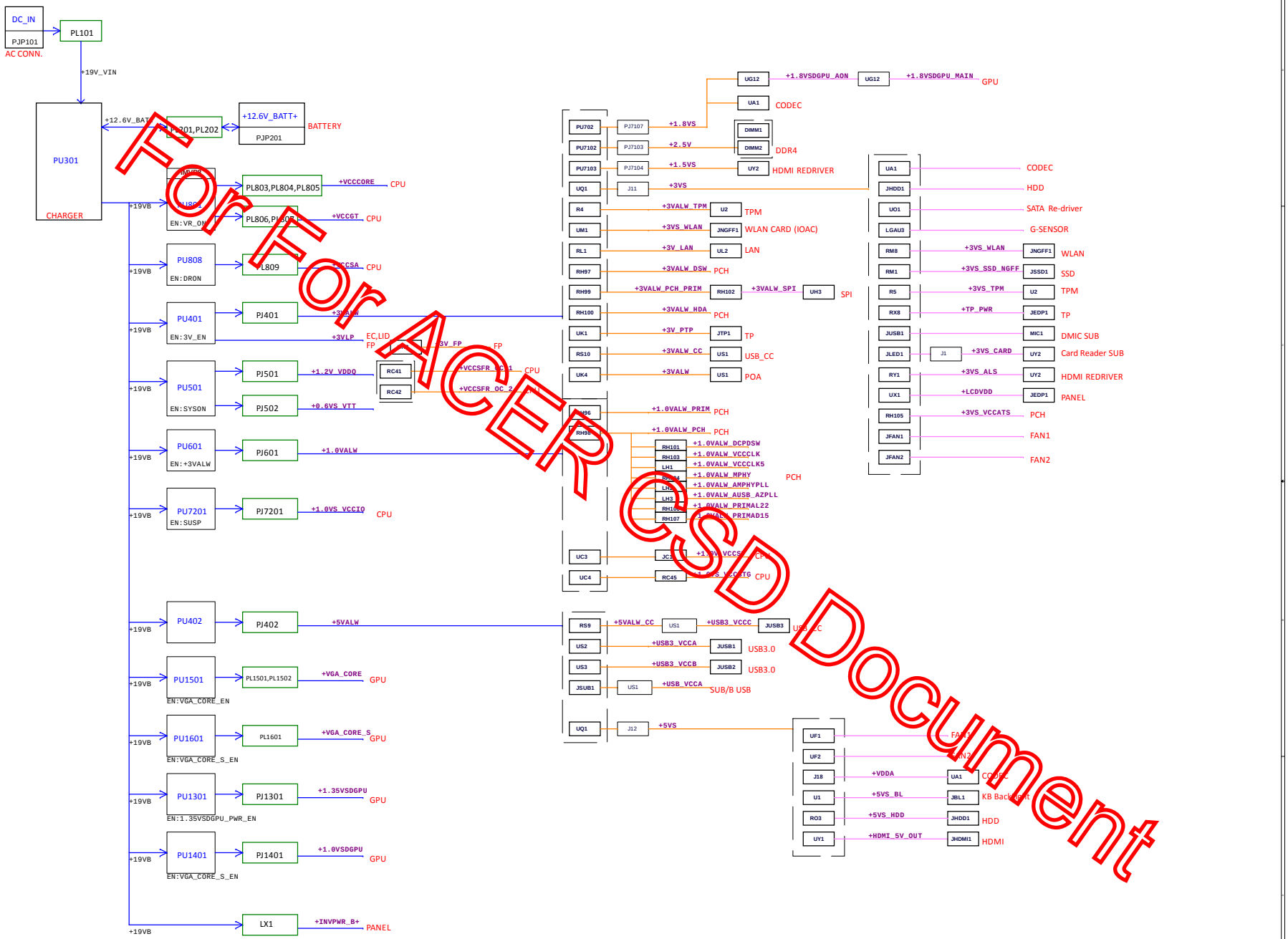

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Power Map

CSPM2 H/B LA-E361P

C5PM2_DIS_EVT Power Sequence AC mode

BIOS ver: V0.01
EC: ver: V0.01

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Compal Electronics, Inc.

Title: Power Sequence

Size	Document Number	Rev
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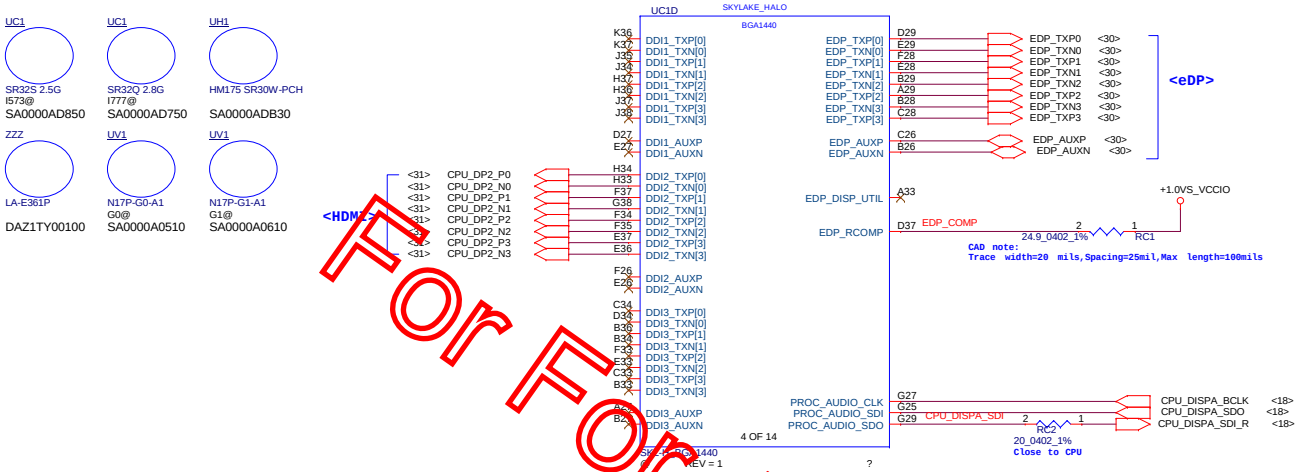

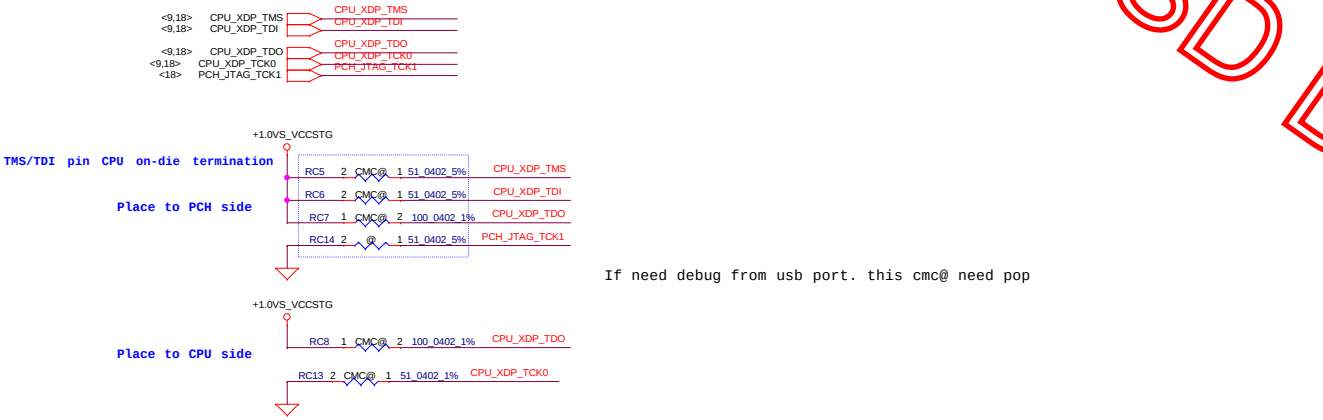

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Compal Electronics, Inc.

Title: SKL-H(1/9)DDI,EDP

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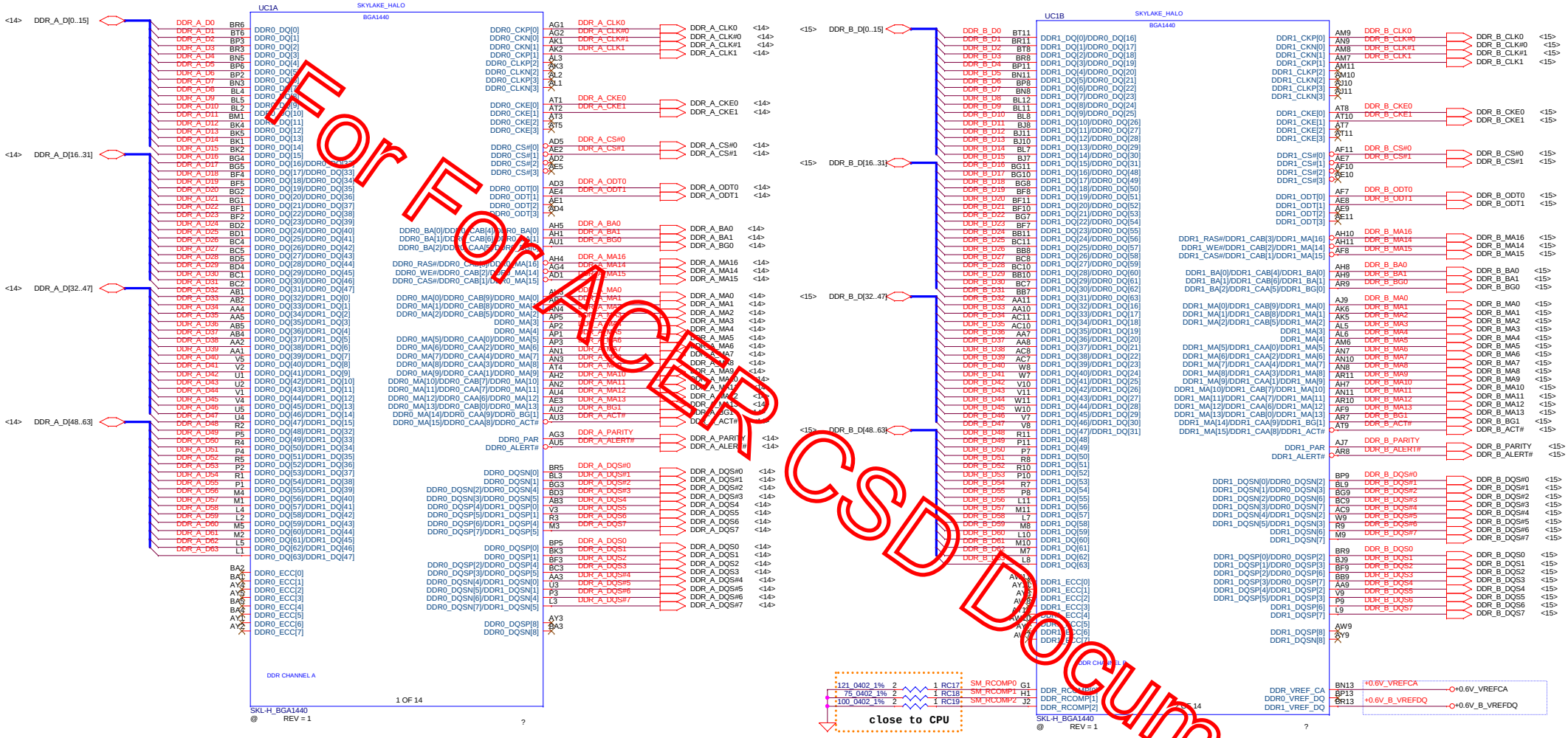
Interleaved Memory



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Compal Electronics, Inc.

Title: SKL-H(2/9)DDRIII

Size	Document Number	Rev
Custom	C5PM2 M/B LA-E361P	1.0

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Compal Electronics, Inc.			
Title: SKL-H(3/9) PEG,DMI			
Size: Custom	Document Number: C5PM2 M/B LA-E361P		Rev: 1.0
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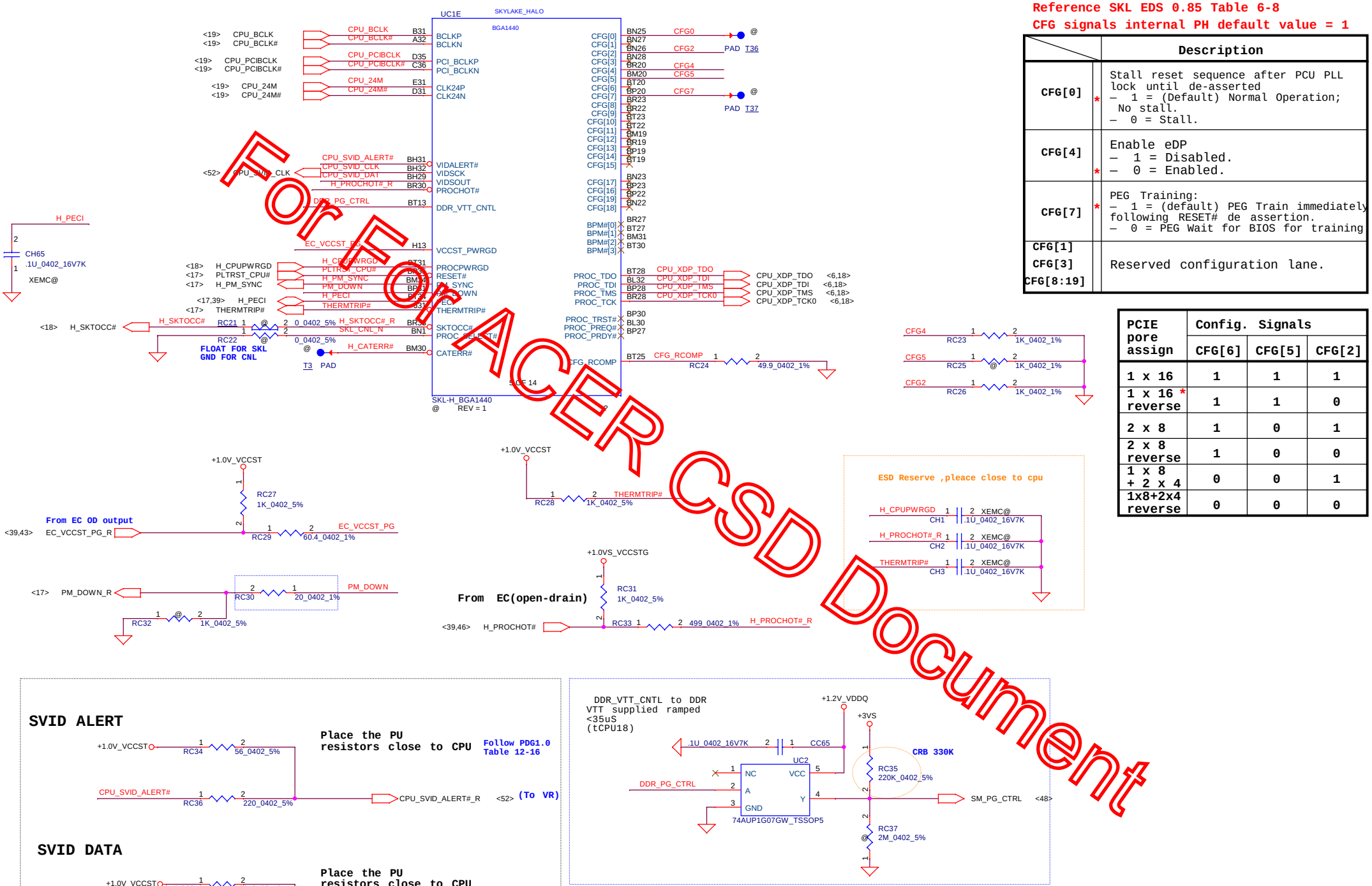

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Compal Electronics, Inc.

Title: SKL-H(4/9)CLK,GPIO

Size: Custom | Document Number: C5PM2 M/B LA-E361P | Rev: 1.0

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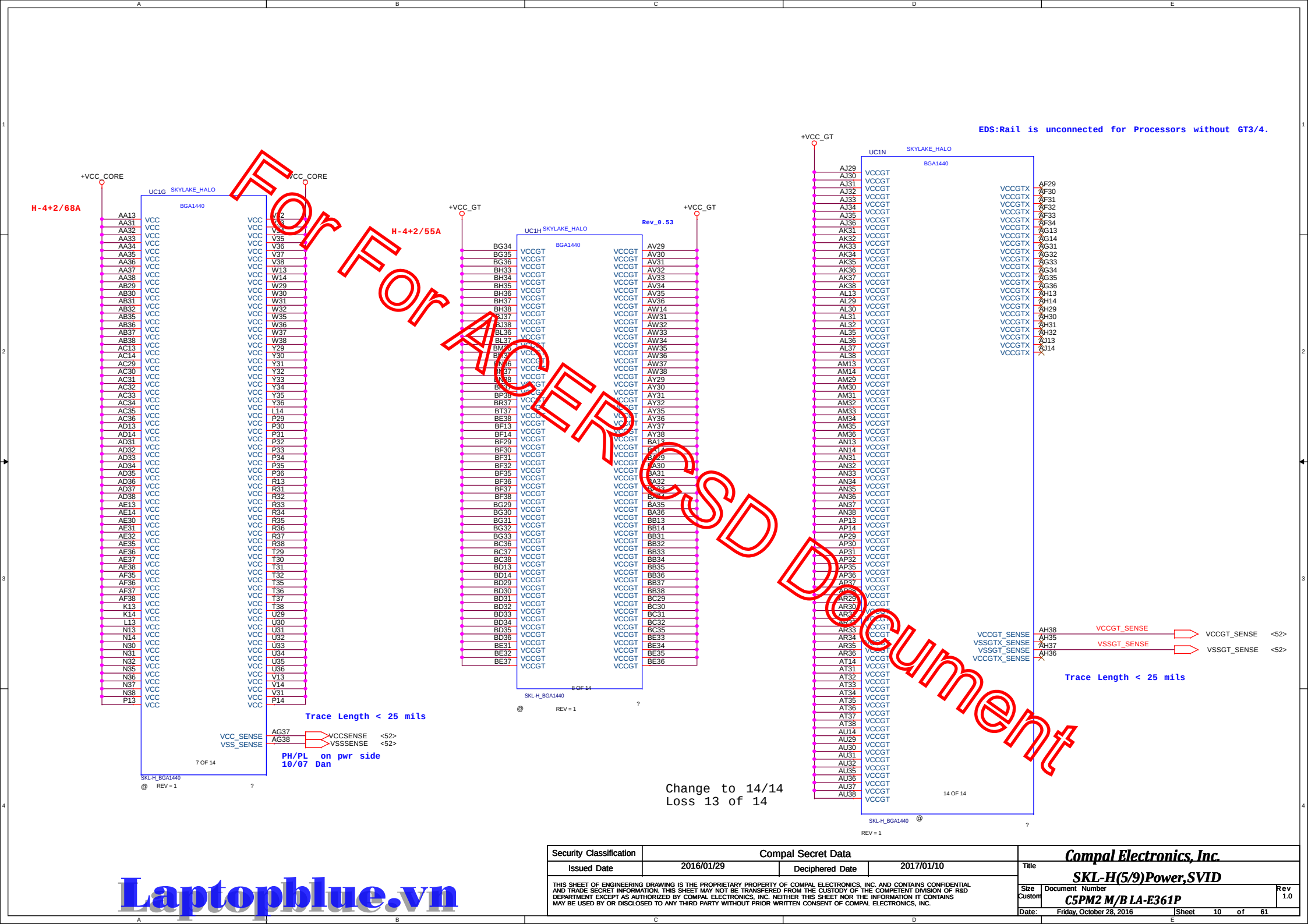

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Compal Electronics, Inc.

Title: SKL-H(5/9)Power,SVID

Size	Document Number	Rev
Custom	C5PM2 M/B LA-E361P	1.0

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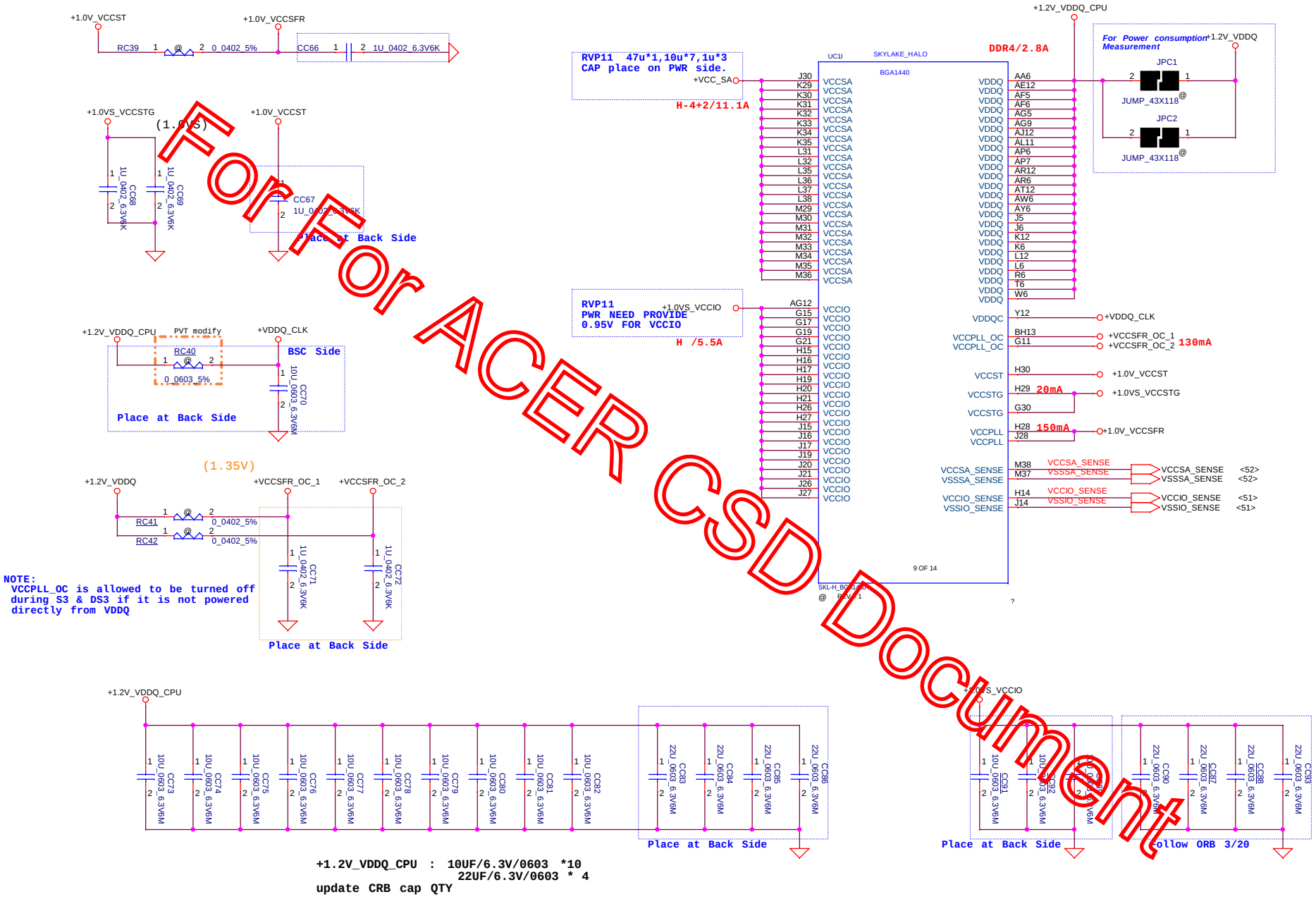

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: SKL-H(6/9)POWER

Size	Document Number	Rev
Custom	C5PM2 M/B LA-E361P	1.0

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Compal Electronics, Inc.

Title: SKL-H(8/9)GND

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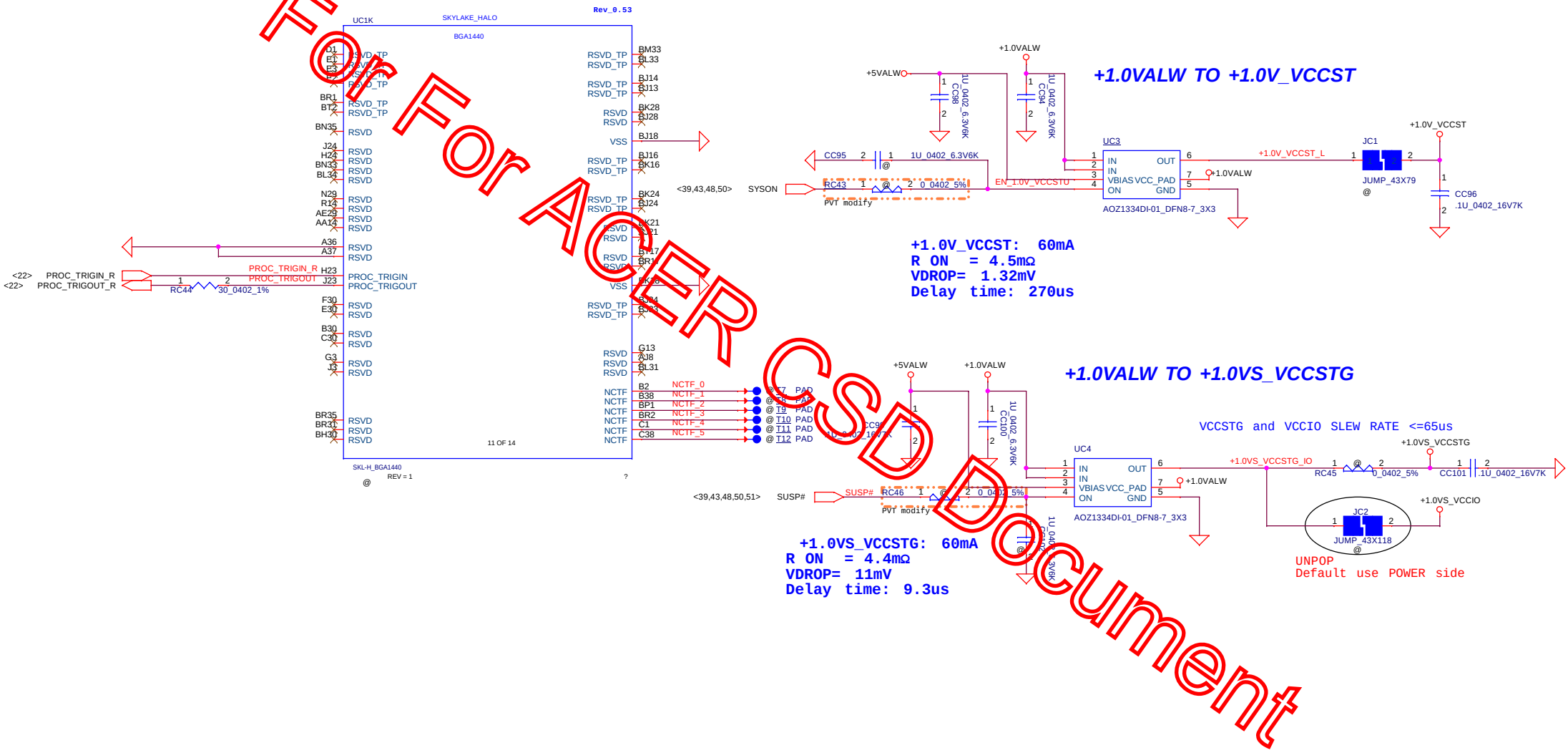

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Title: SKL-H(9/9)RSVD

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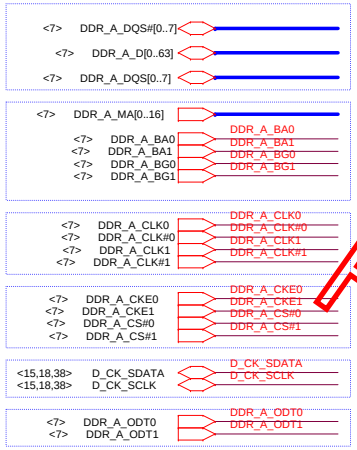
Reverse Type-4H

2-3A to 1 DIMMs/channel



Layout Note:
Place near JDIMM1.164

CPU Side

+0.6V_VREFCA

+1.2V_VDDQ

RD1 1K_0402_1%

CD1 .1U_0402_16V7K

RD2 2_0402_1%

CD2 0.022U_0402_16V7K

RD4 24.9_0402_1%

RD3 1K_0402_1%

CD3 .1U_0402_16V7K

Dimm1 Side

+0.6V_DDRA_VREFCA

+0.6V_DDRA_VREFCA

#543016 PDG 1.0164
20mils wide & spacing

Place near to SO-DIMM connector.

Layout Note:
Place near JDIMM1

Note:
place caps close to DIMM
4 on each side of DIMM

+1.2V_VDDQ

CD4 1U_0402_6.3V6K
CD5 1U_0402_6.3V6K
CD6 1U_0402_6.3V6K
CD7 1U_0402_6.3V6K
CD8 1U_0402_6.3V6K
CD9 1U_0402_6.3V6K
CD10 1U_0402_6.3V6K
CD11 1U_0402_6.3V6K

+1.2V_VDDQ

CD12 .1U_0402_16V7K
CD13 .1U_0402_16V7K

+1.2V_VDDQ

CD18 10U_0603_6.3V6M
CD19 10U_0603_6.3V6M
CD20 10U_0603_6.3V6M
CD21 10U_0603_6.3V6M
CD22 10U_0603_6.3V6M
CD23 10U_0603_6.3V6M
CD24 10U_0603_6.3V6M
CD25

Follow MA51

CD26 330U_D2_2V_Y

SGA00009S00
330U 2V H1.9
9mohm POLY

Layout Note:
Place near JDIMM1.257,259

+2.5V

CD14 1U_0402_6.3V6K
CD15 1U_0402_6.3V6K
CD16 10U_0603_6.3V6M
CD17 10U_0603_6.3V6M

Layout Note:
Place near JDIMM1.258

+0.6VS_VTT

CD28 1U_0402_6.3V6K
CD29 1U_0402_6.3V6K
CD30 1U_0402_6.3V6K
CD31 1U_0402_6.3V6K
CD32 10U_0603_6.3V6M
CD33 10U_0603_6.3V6M

Place Holder

@

+3VS

RD8 0_0402_5%

+3VS_DIMMA

CD35 1U_0402_6.3V6K
CD36 2.2U_0402_6.3V6M

+0.6V_DDRA_VREFCA

CD37 .1U_0402_16V7K
CD38 1U_0402_6.3V6M

Layout Note:
Place near JDIMM1.255

Layout Note:
Place near JDIMM1.164
within 200mils

JDIMM1A

REVERSE

DDR_A_CLK0	137	CK0(T)	DQ0	8	DDR_A_D0
DDR_A_CLK#0	139	CK0#(C)	DQ1	7	DDR_A_D1
DDR_A_CLK1	138	CK1(T)	DQ2	20	DDR_A_D2
DDR_A_CLK#1	140	CK1#(C)	DQ3	21	DDR_A_D3
			DQ4	4	DDR_A_D4
DDR_A_CKE0	109	CKE0	DQ5	3	DDR_A_D5
DDR_A_CKE1	110	CKE1	DQ6	16	DDR_A_D6
			DQ7	17	DDR_A_D7
DDR_A_CS#0	149	S0#	DQS0(T)	13	DDR_A_DQS0
DDR_A_CS#1	157	S1#	DQS0#(C)	11	DDR_A_DQS#0
	162	S2#/C0			
	165	S3#/C1	DQ8	28	DDR_A_D8
DDR_A_ODT0	155		DQ9	29	DDR_A_D9
DDR_A_ODT1	161	ODT0	DQ10	41	DDR_A_D10
		ODT1	DQ11	42	DDR_A_D11
			DQ12	24	DDR_A_D12
DDR_A_BG0	115	BG0	DQ13	25	DDR_A_D13
DDR_A_BG1	113	BG1	DQ14	38	DDR_A_D14
DDR_A_BA0	150	BA0	DQ15	37	DDR_A_D15
DDR_A_BA1	145	BA1	DQS1(T)	34	DDR_A_DQS1
			DQS1#(C)	32	DDR_A_DQS#1
DDR_A_MA0	144	A0			
DDR_A_MA1	133	A1	DQ16	50	DDR_A_D16
DDR_A_MA2	132	A2	DQ17	49	DDR_A_D17
DDR_A_MA3	131	A3	DQ18	62	DDR_A_D18
DDR_A_MA4	128	A4	DQ19	63	DDR_A_D19
DDR_A_MA5	126	A5	DQ20	46	DDR_A_D20
DDR_A_MA6	127	A6	DQ21	45	DDR_A_D21
DDR_A_MA7	122	A7	DQ22	58	DDR_A_D22
DDR_A_MA8	125	A8	DQ23	59	DDR_A_D23
DDR_A_MA9	121	A9	DQS2(T)	55	DDR_A_DQS2
DDR_A_MA10	146	A10_AP	DQS2#(C)	53	DDR_A_DQS#2
DDR_A_MA11	120	A11			
DDR_A_MA12	119	A12	DQ24	70	DDR_A_D24
DDR_A_MA13	158	A13	DQ25	71	DDR_A_D25
DDR_A_MA14	151	A14_WE#	DQ26	83	DDR_A_D26
DDR_A_MA15	156	A15_CAS#	DQ27	84	DDR_A_D27
DDR_A_MA16	152	A16_RAS#	DQ28	66	DDR_A_D28
			DQ29	67	DDR_A_D29
DDR_A_ACT#	114	ACT#	DQ30	79	DDR_A_D30
			DQ31	80	DDR_A_D31
DDR_A_PARITY	143	PARITY	DQS3(T)	76	DDR_A_DQS3
DDR_A_ALERT#	116	ALERT#	DQS3#(C)	74	DDR_A_DQS#3
DDR_A_EVENT#	134	EVENT#			
DDR_DRAMRST#_R	108	RESET#	DQ32	174	DDR_A_D32
			DQ33	173	DDR_A_D33
D_CK_SDATA	254		DQ34	187	DDR_A_D34
D_CK_SCLK	253	SDA	DQ35	186	DDR_A_D35
		SCL	DQ36	170	DDR_A_D36
			DQ37	169	DDR_A_D37
DDR_A_SA2	166		DQ38	183	DDR_A_D38
DDR_A_SA1	260	SA2	DQ39	182	DDR_A_D39
DDR_A_SA0	256	SA1	DQS4(T)	179	DDR_A_DQS4
		SA0	DQS4#(C)	177	DDR_A_DQS#4
	92				
	91	CB0_NC	DQ40	195	DDR_A_D40
	101	CB1_NC	DQ41	194	DDR_A_D41
	105	CB2_NC	DQ42	207	DDR_A_D42
	88	CB3_NC	DQ43	208	DDR_A_D43
	87	CB4_NC	DQ44	191	DDR_A_D44
	100	CB5_NC	DQ45	190	DDR_A_D45
	104	CB6_NC	DQ46	203	DDR_A_D46
	97	CB7_NC	DQ47	204	DDR_A_D47
	95	DQS8(T)	DQS5(T)	200	DDR_A_DQS5
		DQS8#(C)	DQS5#(C)	198	DDR_A_DQS#5
	12				
	33	DM0#/DBI0#	DQ48	216	DDR_A_D48
	51	DM1#/DBI1#	DQ49	215	DDR_A_D49
	69	DM2#/DBI2#	DQ50	228	DDR_A_D50
	86	DM3#/DBI3#	DQ51	229	DDR_A_D51
	119	DM4#/DBI4#	DQ52	211	DDR_A_D52
	139	DM5#/DBI5#	DQ53	212	DDR_A_D53
	220	DM6#/DBI6#	DQ54	224	DDR_A_D54
	241	DM7#/DBI7#	DQ55	225	DDR_A_D55
			DQS6(T)	221	DDR_A_DQS6
			DQS6#(C)	219	DDR_A_DQS#6
			DQ56	237	DDR_A_D56
			DQ57	236	DDR_A_D57
			DQ58	248	DDR_A_D58
				250	DDR_A_D59
				232	DDR_A_D60
			DQ61	233	DDR_A_D61
			DQ62	245	
			DQ63	246	
			DQS7(T)	242	
			DQS7#(C)	240	DDR_A_DQS#7

LOTES_ADDR0206-P001A

<7> DDR_A_ACT#

+1.2V_VDDQ <7> DDR_A_PARITY

<7> DDR_A_ALERT#

RD5 240_0402_1%

SPD Address for CHANNEL0
Write Address 0xA0
Read Address 0xA1
SA0=0;SA1=0;SA2=0

+1.2V_VDDQ

<18> DDR_DRAMRST#

RD7 0_0402_5%

DDR_DRAMRST#_R <15>

XEMC@ CD24 100P_0402_50V8J

RD6 470_0402_5%

CD27 .1U_0402_16V7K @

Layout NOTE
PLACE THE CAP within 200mil from Pin108

*2015MOW02, Can't install Cap on DRAMRST

JDIMM1B

REVERSE

+1.2V_VDDQ

+1.2V_VDDQ

+0.6V_DDRA_VREFCA

+3VS_DIMMA

+0.6VS_VTT

+2.5V

	111	VDD1	VDD11	141	
	112	VDD2	VDD12	142	
	117	VDD3	VDD13	147	
	118	VDD4	VDD14	148	
	123	VDD5	VDD15	153	
	124	VDD6	VDD16	154	
	129	VDD7	VDD17	159	
	130	VDD8	VDD18	160	
	135	VDD9	VDD19	163	
	136	VDD10			
					+0.6VS_VTT
	255	VDDSPD	VTT	258	+2.5V
	164	VREFCA	VPP1	257	
			VPP2	259	
	1			99	
	2	VSS	VSS	102	
	5	VSS	VSS	103	
	6	VSS	VSS	106	
	9	VSS	VSS	107	
	10	VSS	VSS	167	
	14	VSS	VSS	168	
	15	VSS	VSS	171	
	18	VSS	VSS	172	
	19	VSS	VSS	175	
	22	VSS	VSS	176	
	23	VSS	VSS	180	
	26	VSS	VSS	181	
	27	VSS	VSS	184	
	30	VSS	VSS	185	
	31	VSS	VSS	188	
	35	VSS	VSS	189	
	36	VSS	VSS	192	
	39	VSS	VSS	193	
	40	VSS	VSS	196	
	43	VSS	VSS	197	
	44	VSS	VSS	201	
	47	VSS	VSS	202	
	48	VSS	VSS	205	
	51	VSS	VSS	206	
	52	VSS	VSS	209	
	56	VSS	VSS	210	
	57	VSS	VSS	213	
	60	VSS	VSS	214	
	61	VSS	VSS	217	
	64	VSS	VSS	218	
	65	VSS	VSS	222	
	68	VSS	VSS	223	
	69	VSS	VSS	226	
	72	VSS	VSS	227	
	73	VSS	VSS	230	
	77	VSS	VSS	231	
	78	VSS	VSS	234	
	81	VSS	VSS	235	
	82	VSS	VSS	238	
	85	VSS	VSS	239	
	86	VSS	VSS	243	
	89	VSS	VSS	244	
	90	VSS	VSS	247	
	93	VSS	VSS	248	
	94	VSS	VSS	251	
	98	VSS	VSS	252	
		VSS	VSS		
	262	GND	GND	261	

LOTES_ADDR0206-P001A

Interleaved Memory

Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.

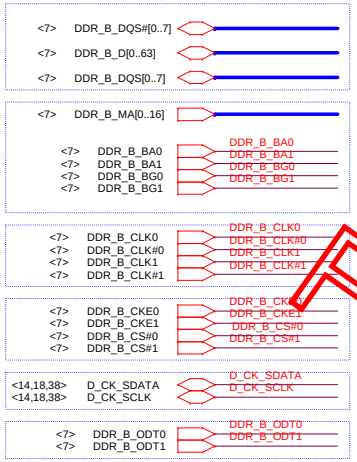
Title: DDR4 DIMMA

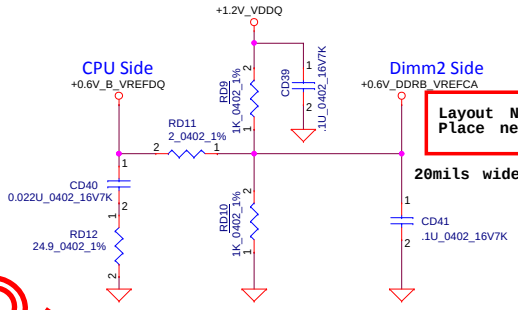
Size: Custom | Document Number: C5PM2 M/B LA-E361P | Rev: 1.0

Date: Friday, October 28, 2016 | Sheet 14 of 61

Reverse Type-8H

2-3A to 1 DIMMs/channel





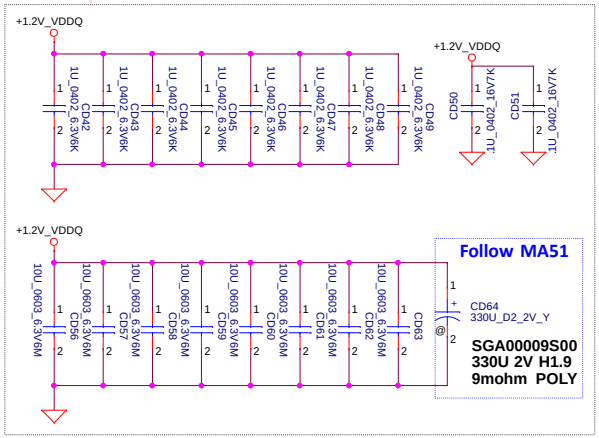
Layout Note:
Place near JDIMM2.164

20mils wide & spacing

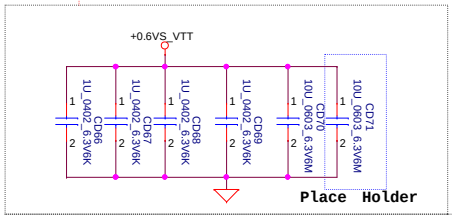
Place near to SO-DIMM connector.

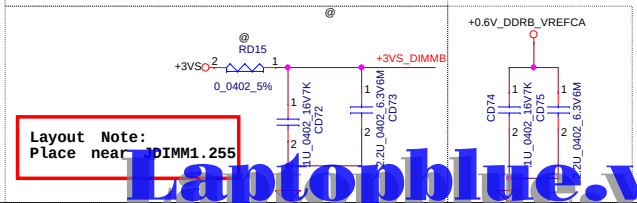
Layout Note:
Place near JDIMM2

Note:
place caps close to DIMM
4 on each side of DIMM



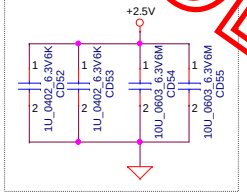
Layout Note:
Place near JDIMM2.258



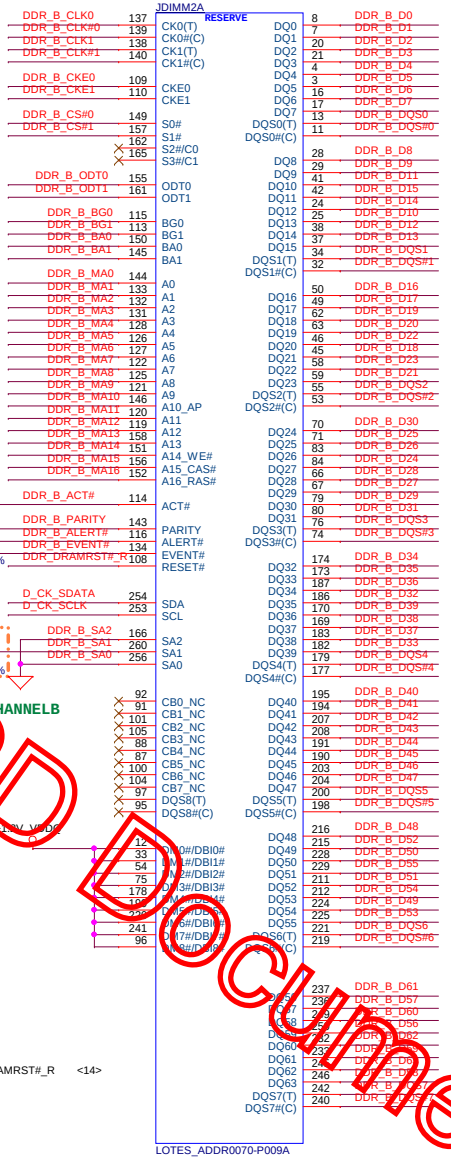


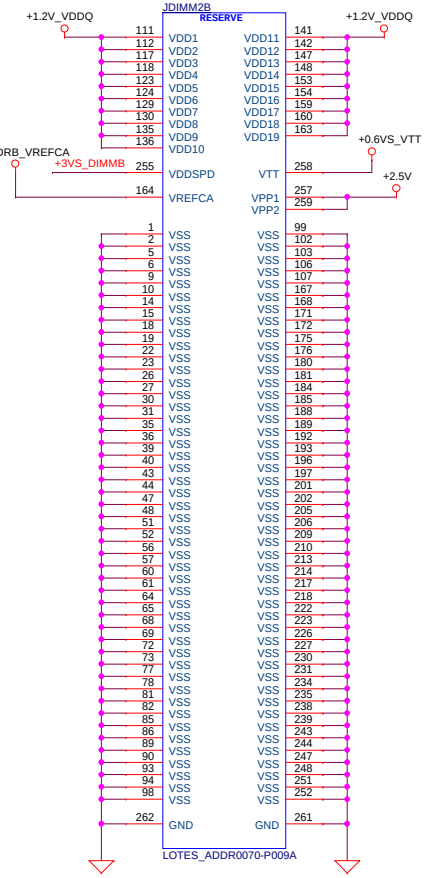
Layout Note:
Place near JDIMM1.255

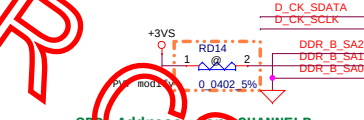
Layout Note:
Place near JDIMM1.164
within 200mils

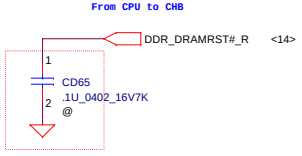


Layout Note:
Place near JDIMM2.257,259









Layout NOTE
PLACE THE CAP within 200mil from Pin108

*2015MOW02, Can't install Cap on DRAMRST

Interleaved Memory

Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: DDR4 DIMMB

Size: Custom | Document Number: C5PM2 M/B LA-E361P | Rev: 1.0

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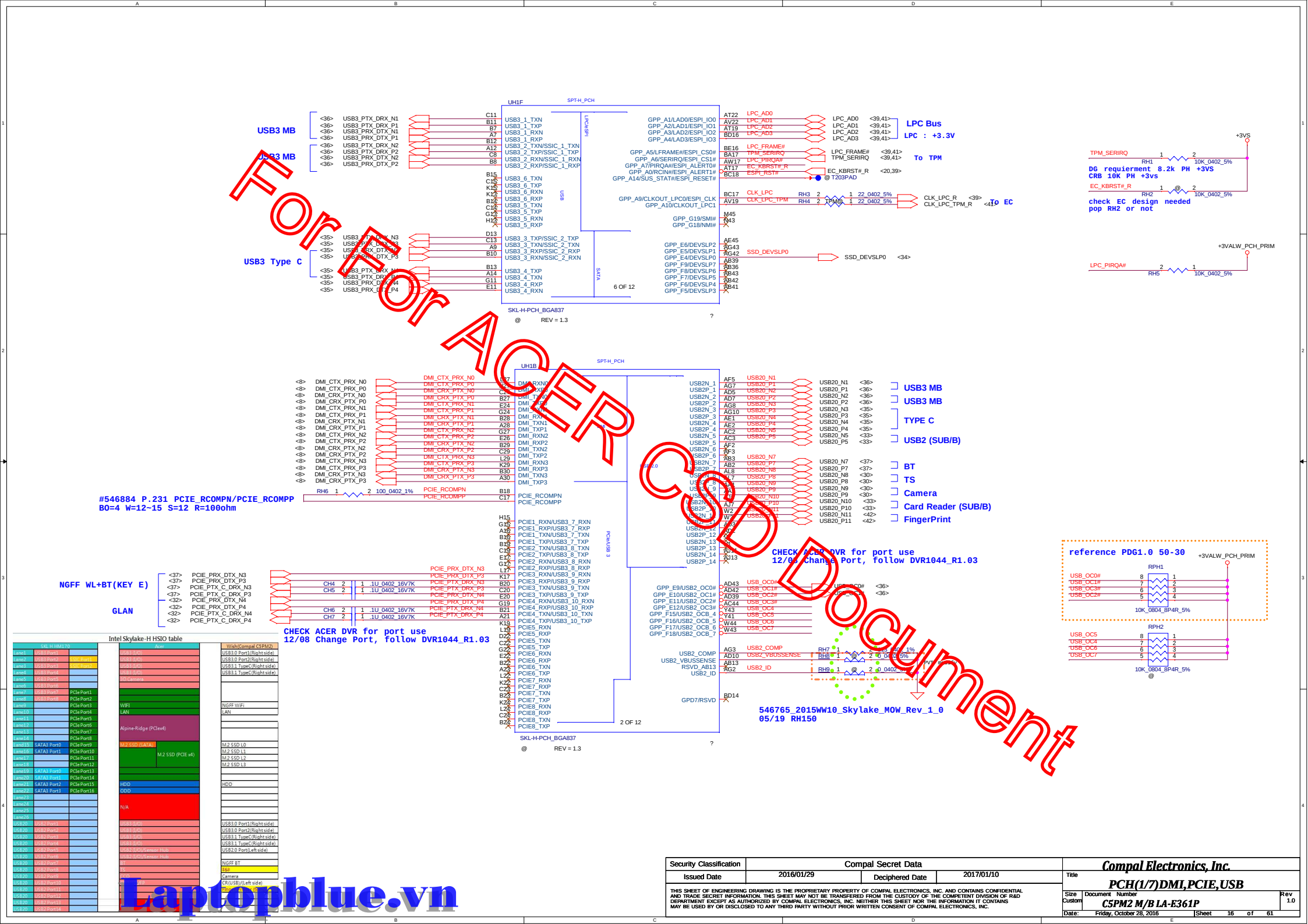

Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

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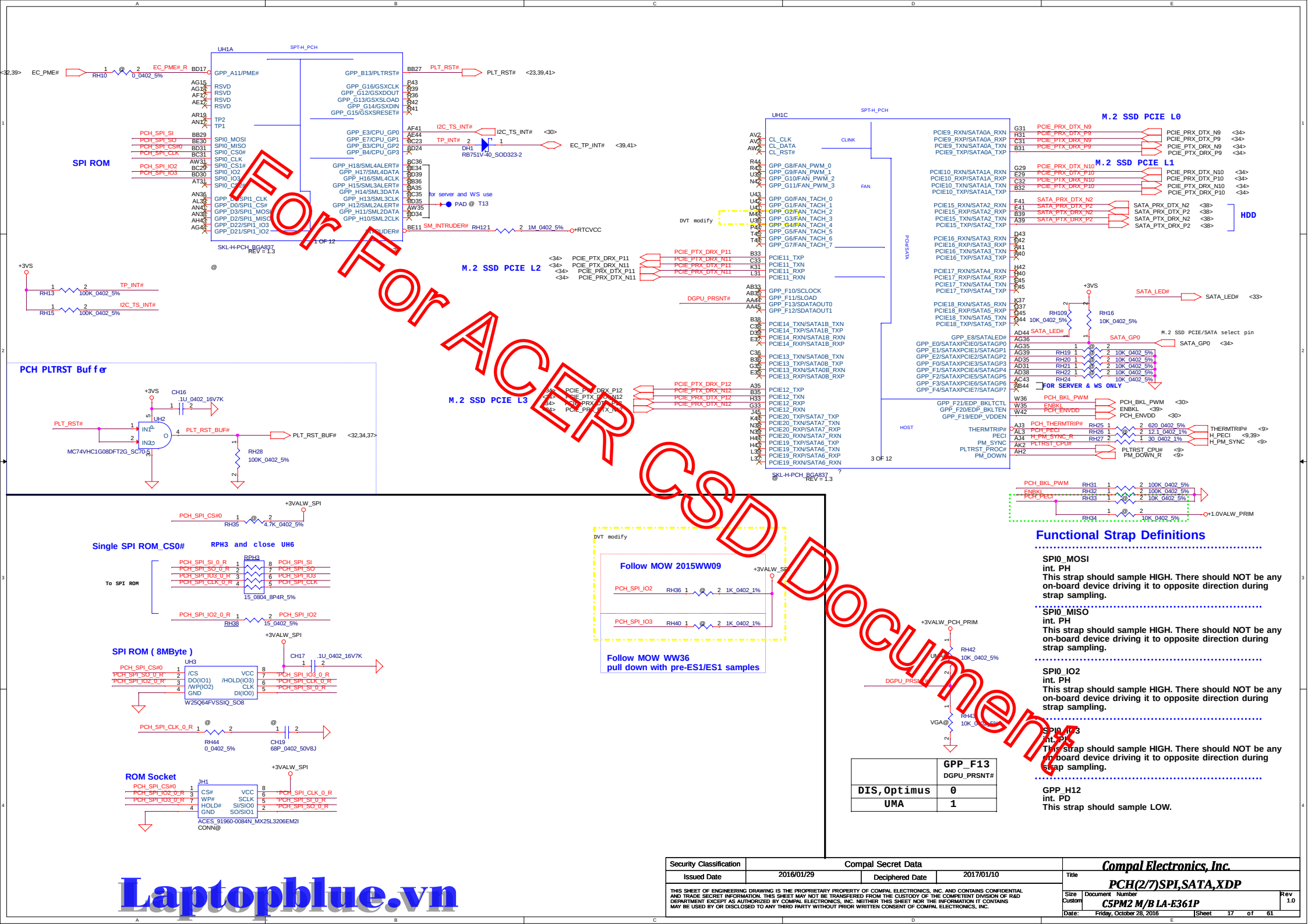
Compal Electronics, Inc.

Title: PCH(1/7)DMI,PCIE,USB

Size	Document Number	Rev
Custom	C5PM2 M/B LA-E361P	1.0

Date: Friday, October 28, 2016 Sheet 16 of 61



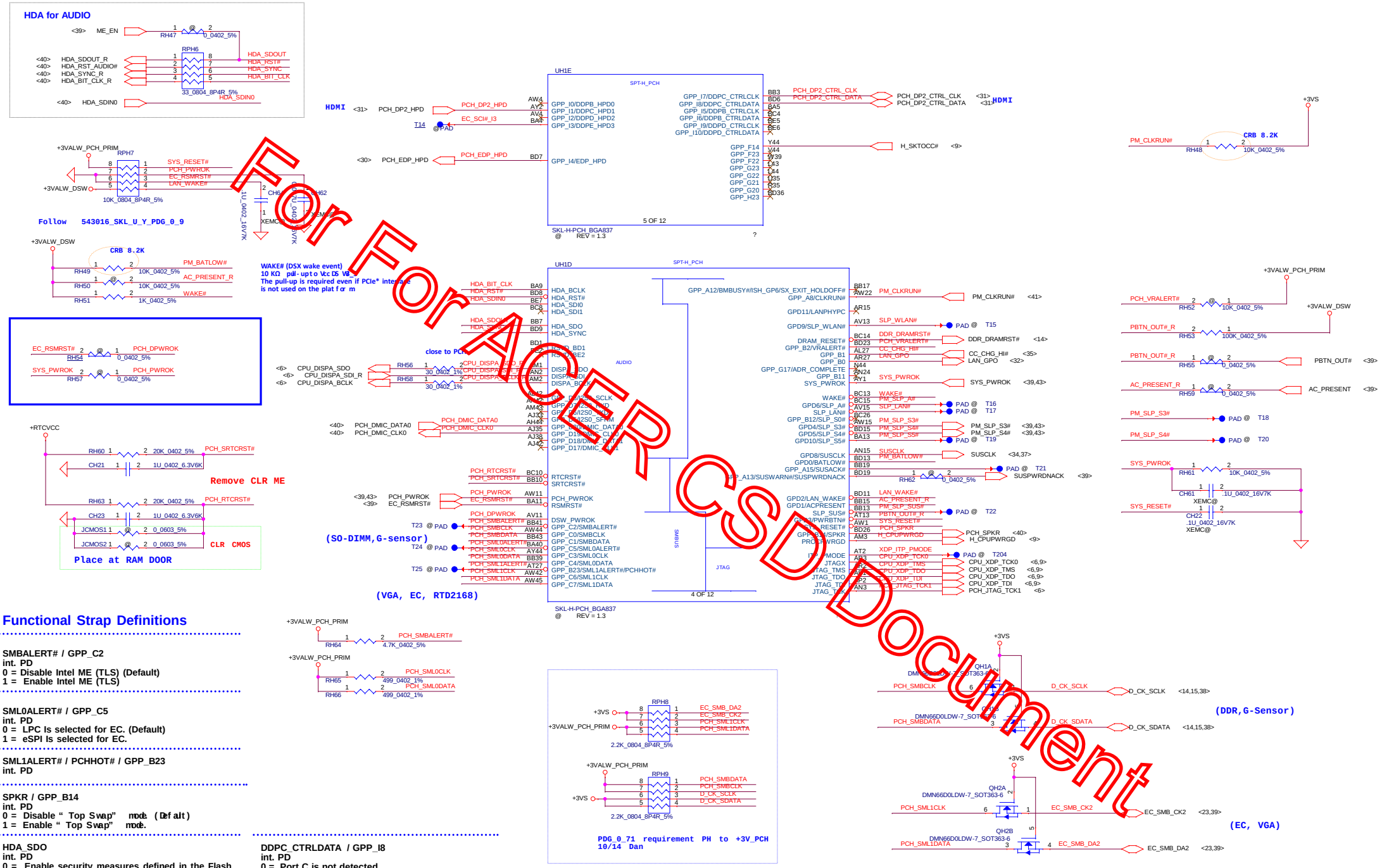
Security Classification	Compal Secret Data
Issued Date	2016/01/29
Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: PCH(2/7)SPI,SATA,XDP

Size: Custom | Document Number: C5PM2 M/B LA-E361P | Rev: 1.0

Date: Friday, October 28, 2016 | Sheet 17 of 61



Functional Strap Definitions

SMBALERT# / GPP_C2
int. PD
0 = Disable Intel ME (TLS) (Default)
1 = Enable Intel ME (TLS)

SML0ALERT# / GPP_C5
int. PD
0 = LPC Is selected for EC. (Default)
1 = eSPI Is selected for EC.

SML1ALERT# / PCHHOT# / GPP_B23
int. PD

SPKR / GPP_B14
int. PD
0 = Disable “ Top Swap” mode. (Default)
1 = Enable “ Top Swap” mode.

HDA_SDO
int. PD
0 = Enable security measures defined in the Flash Descriptor. (Default)
1 = Disable Flash Descriptor Security (override).

DDPB_CTRLDATA / GPP_I6
int. PD
0 = Port B is not detected.
1 = Port B is detected. (Default)

DDPC_CTRLDATA / GPP_I8
int. PD
0 = Port C is not detected.
1 = Port C is detected. (Default)

DDPD_CTRLDATA / GPP_I10
int. PD
0 = Port D is not detected. (Default)
1 = Port D is detected.

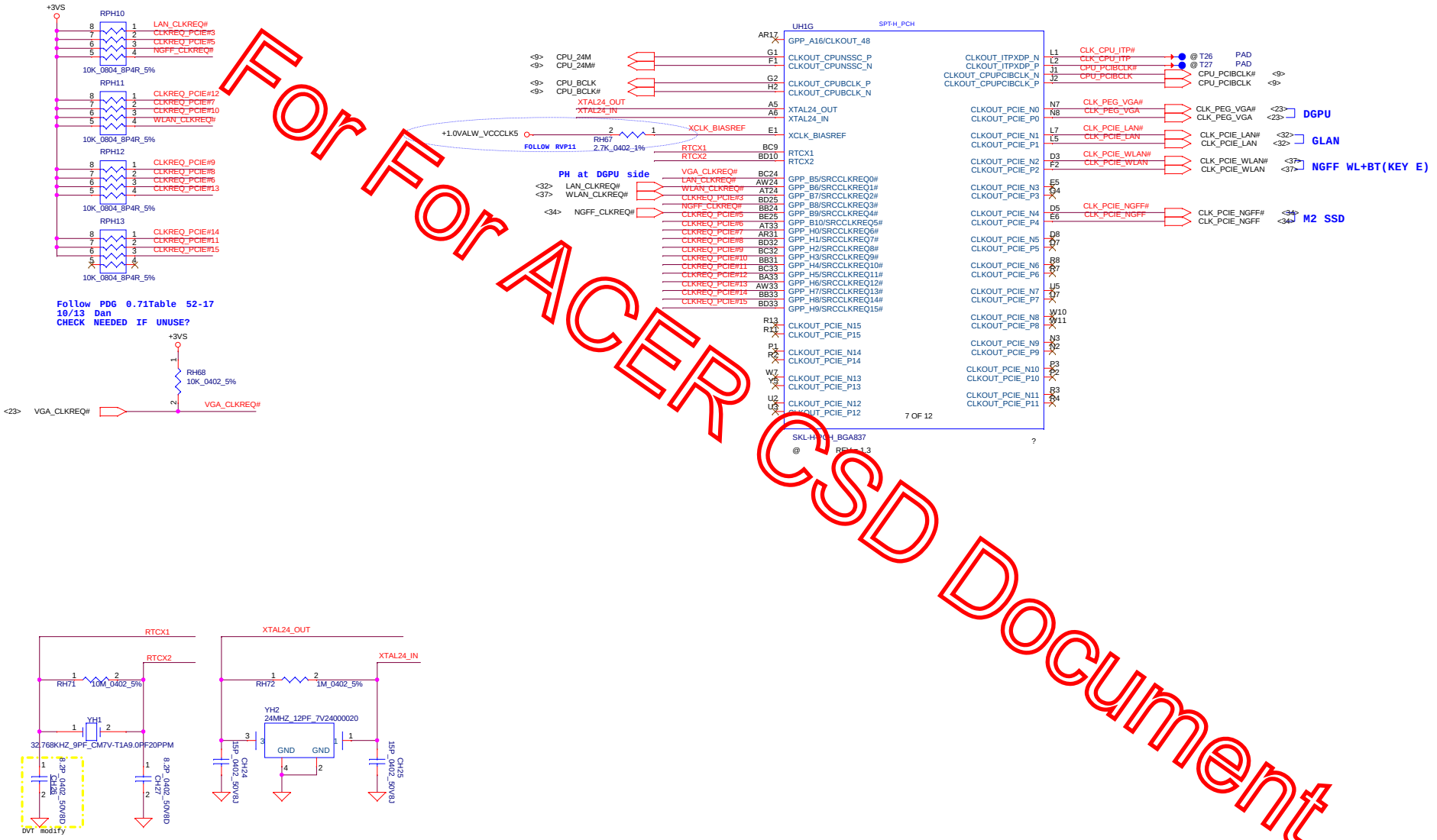
Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: PCH(3/7)GPIO,SMBUS

Size	Document Number	Rev
Custom	C5PM2 M/B LA-E361P	1.0

Date: Friday, October 28, 2016 Sheet 18 of 61



Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: PCH(4/7)CLK

Size	Document Number	Rev
Custom	C5PM2 M/B LA-E361P	1.0

Date: Friday, October 28, 2016 Sheet 19 of 61

Functional Strap Definitions

GSPI1_MOSI / GPP_B22
int. PD
Boot BIOS Destination
0 = SPI (Default)
1 = LPC

GSPI0_MOSI / GPP_B18
int. PD
0 = Disable "No Reboot" mode. (Default)
1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature).

VGA_ID	GPP_D9
G0	0
G1	1

RANK_ID	GPP_D10
DR	0
SR	1

Project ID	Project_ID1 GPP_D12	Project_ID0 GPP_D11
*C5PM2	0	0
Reserved	0	1
Reserved	1	0
Reserved	1	1

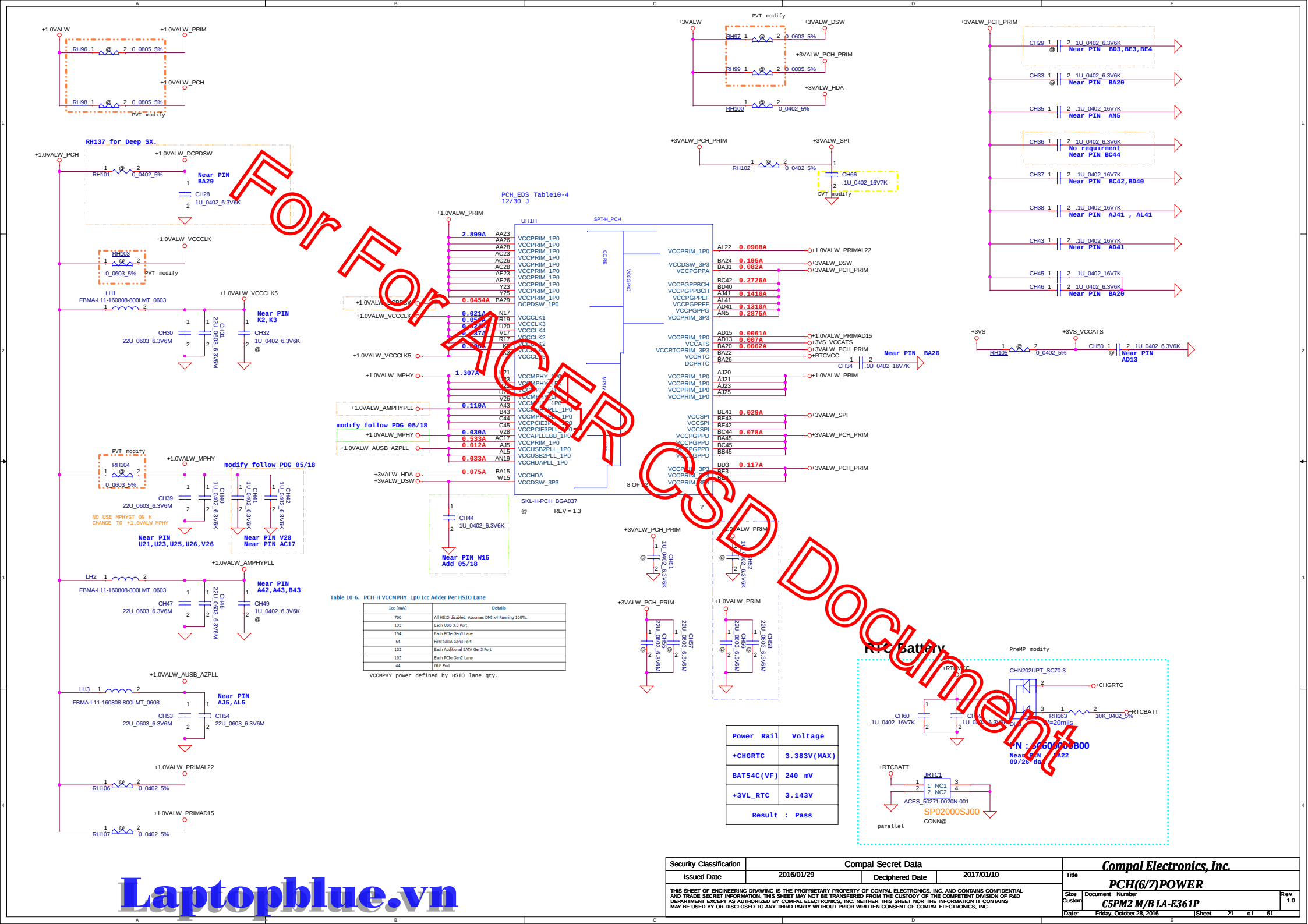
Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: PCH(5/7)UART,I2C,GPIO

Size: Custom | Document Number: C5PM2 M/B LA-E361P | Rev: 1.0

Date: Friday, October 28, 2016 | Sheet 20 of 61



Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: PCH(6/7)POWER

Size	Document Number	Rev
Custom	C5PM2 M/B LA-E361P	1.0

Date: Friday, October 28, 2016 Sheet 21 of 61

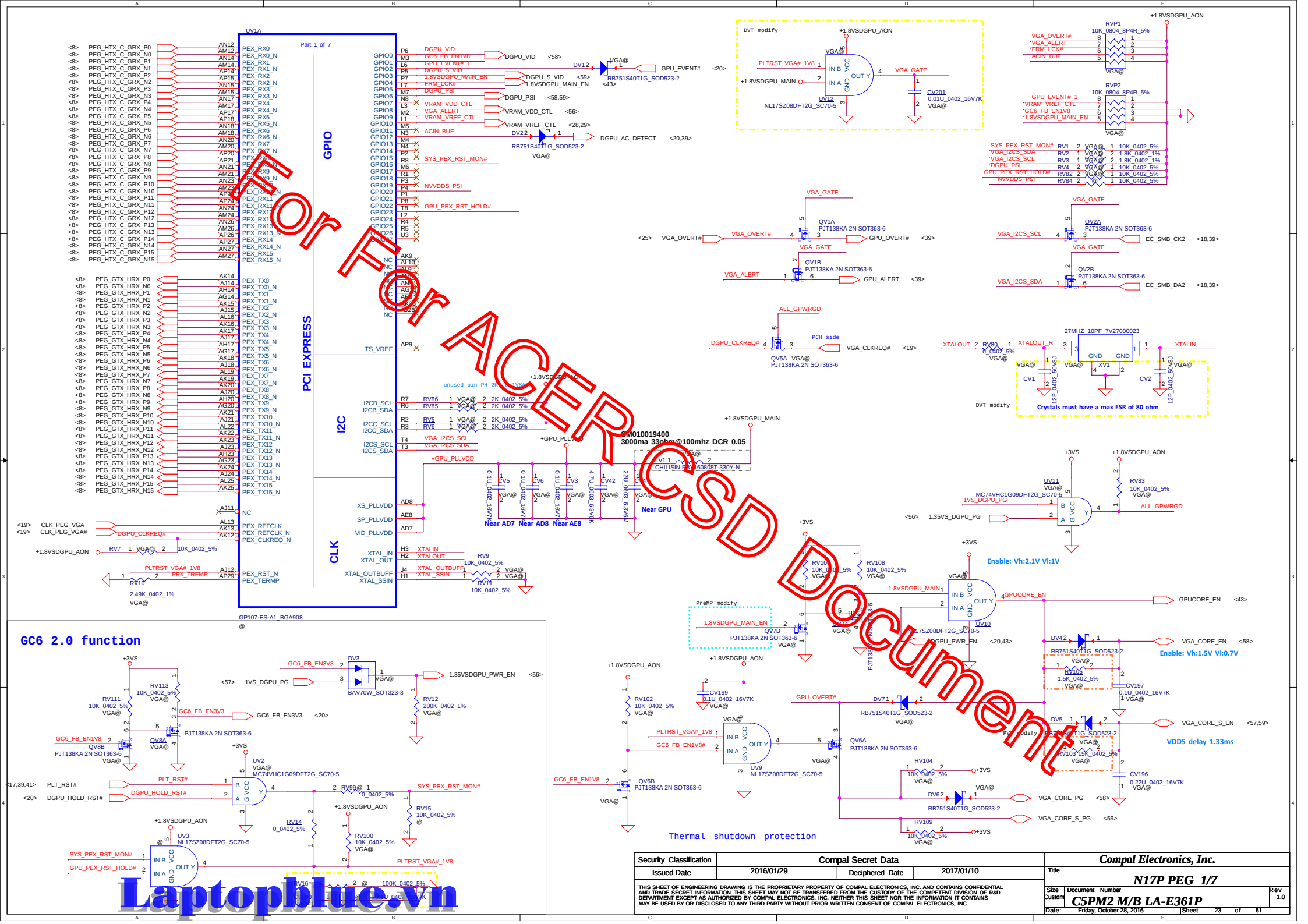
Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: PCH(7/7)GND

Size	Document Number	Rev
Custom	C5PM2 M/B LA-E361P	1.0

Date: Friday, October 28, 2016 Sheet 22 of 61



GDDR5 Mode H Mapping

<29>	DATA Bus	
Address	0..31	32..63
CMD0	CS#	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE#	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI#	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS#	
CMD13	RST#	
CMD14	CKE#	
CMD15	CAS#	
CMD16		CS#
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE#
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI#
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS#
CMD29		RST#
CMD30		CKE#
CMD31		CAS#

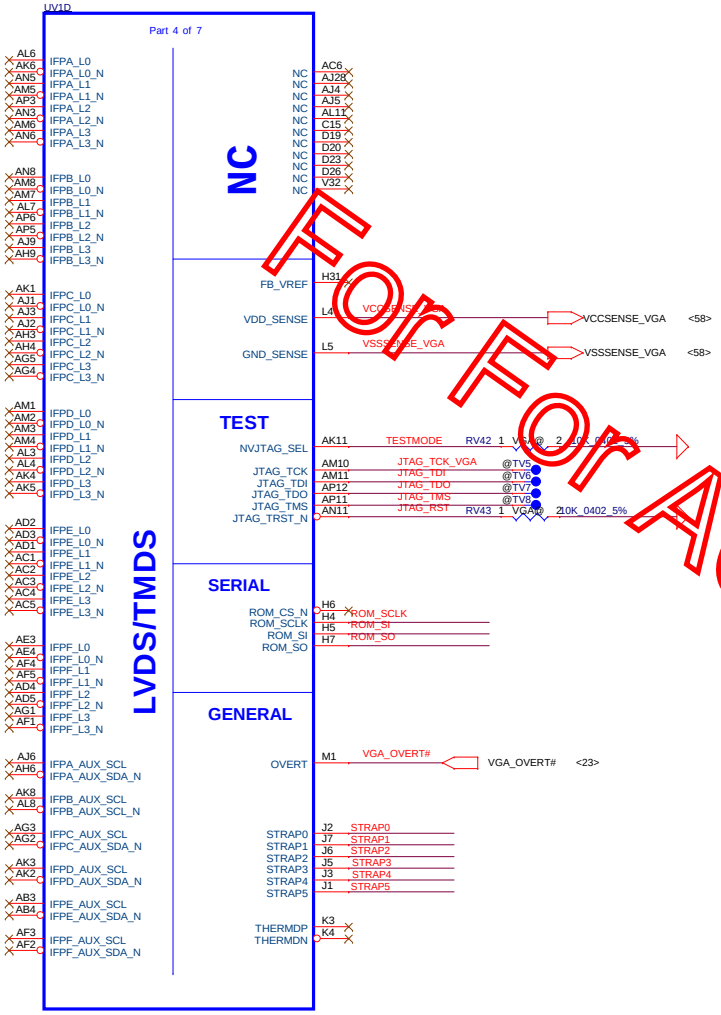
Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: *N17P VRAM 2/7*

Size: Custom | Document Number: *C5PM2 M/B LA-E361P* | Rev: 1.0

Date: Friday, October 28, 2016 | Sheet 24 of 61

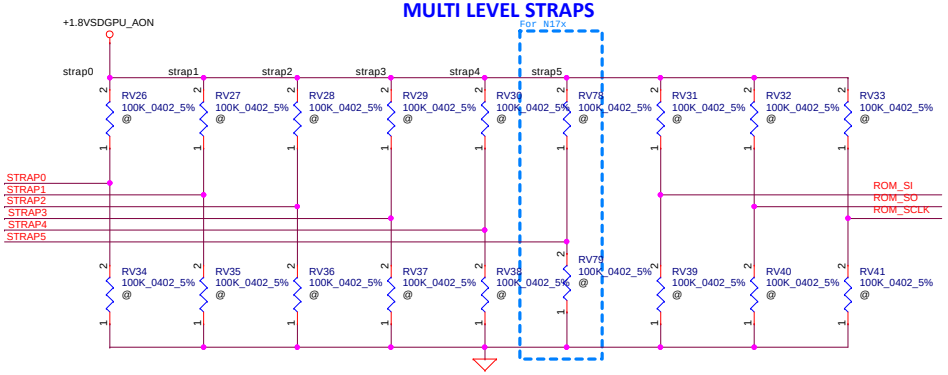


@

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0
M	H	H	1	1	1	1

SMB_ATL_ADDR	
LOW	Single GPU
High	Dual GPU
DEVID_SEL	
LOW	Orig. Device ID
High	Support G-Sync GPUID
VGA_DEVICE	
LOW	3D Device
High	VGA Device
PCIE_CFG	
LOW	Normal signal swing
High	Reduce the signal amplitude

MULTI LEVEL STRAPS



Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V and 1.5V[2]	Samsung	K4G80325FB-HC28	B-die	0x0	7 Gbps	N/A	Full	Production candidate
			Micron	MT51J256M32HF-70:A	A-die	0x1	7 Gbps	N/A	Full	Production candidate
			Hynix	H5GC8H24MJR-R0C	M-die	0x2	7 Gbps	N/A	Full	Post production candidate
4 Gb	128Mx32	1.35V and 1.5V[2]	Samsung	K4G41325FE-HC28	E-die	0x7	7 Gbps	N/A	Full	Production candidate
		1.35V and 1.5V[2]	Hynix	H5GC4H24AJR-R0C	A-die	0x6	7 Gbps	N/A	Full	Production candidate
		1.35V and 1.5V[2]	Micron	EDW4032BABG-70-F	A-die	0x8	7 Gbps	N/A	Full	Post production candidate

Table 5.2 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Table 5.4 SORx_EXPOSED Strap Enablement for Down Designs

Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_ EXPOSED	SOR2_ EXPOSED	SOR1_ EXPOSED	SOR0_ EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
11	H	L	L	ENABLED	disabled	ENABLED	ENABLED
10	H	L	H	ENABLED	disabled	ENABLED	disabled
9	H	H	L	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
	All other strap configurations			(Reserved)			

Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.			
Title	N17P STRAP 3/7		
Size	Document Number		Rev
Custom	C5PM2 M/B LA-E361P		1.0
Date:	Friday, October 28, 2016	Sheet	25 of 61

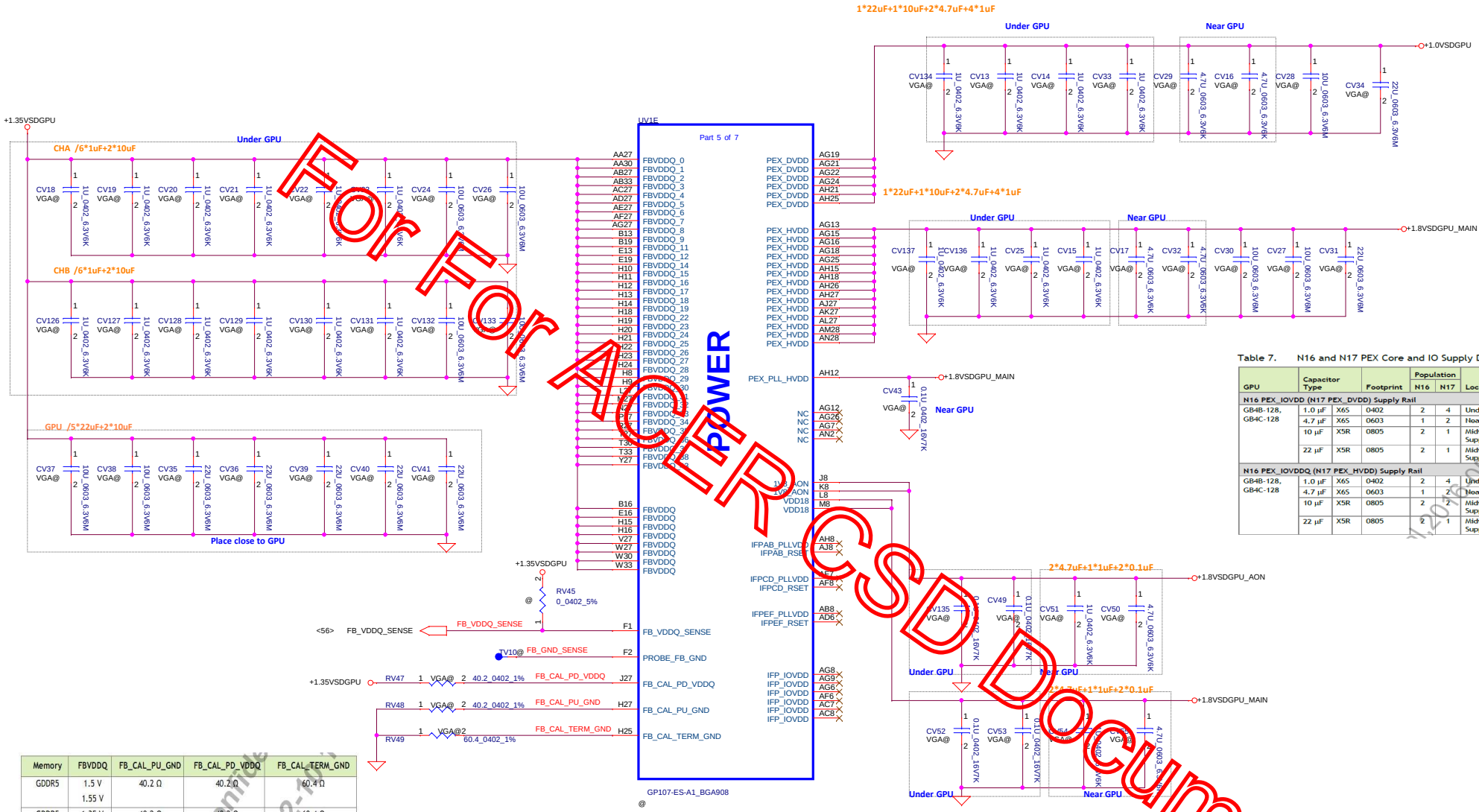


Table 7. N16 and N17 PEX Core and IO Supply Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
N16 PEX_IOVDD (N17 PEX_DVDD) Supply Rail					
GB4B-128, GB4C-128	1.0 µF	X6S	0402	2	4	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X5R	0805	2	1	Midway between GPU and Power Supply
	22 µF	X5R	0805	2	1	Midway between GPU and Power Supply
N16 PEX_IOVDDQ (N17 PEX_HVDD) Supply Rail					
GB4B-128, GB4C-128	1.0 µF	X6S	0402	2	4	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X5R	0805	2	2	Midway between GPU and Power Supply
	22 µF	X5R	0805	2	1	Midway between GPU and Power Supply

Memory	FBVDDQ	FB_CAL_PU_GND	FB_CAL_PD_VDDQ	FB_CAL_TERM_GND
GDDR5	1.5 V	40.2 Ω	40.2 Ω	60.4 Ω
	1.55 V			
GDDR5	1.35 V	40.2 Ω	40.2 Ω	60.4 Ω

For N17x GPU Package: GB4C-128 (preliminary)			
1.0 uF	X6S [0402]	12	Under GPU FBVDDQ ball
10 uF	X6S [0603]	4	
10 uF	X6S [0603]	2	Near GPU device
22 uF	X6S [0603]	5	

Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.	
Title	N17P POWER 4/7
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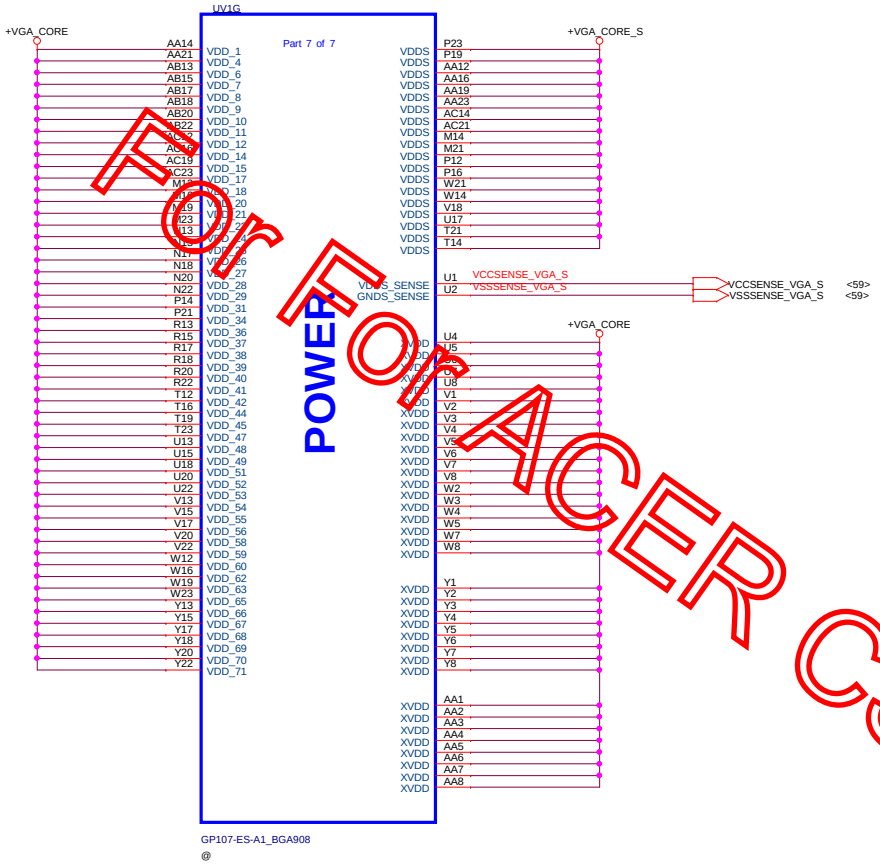
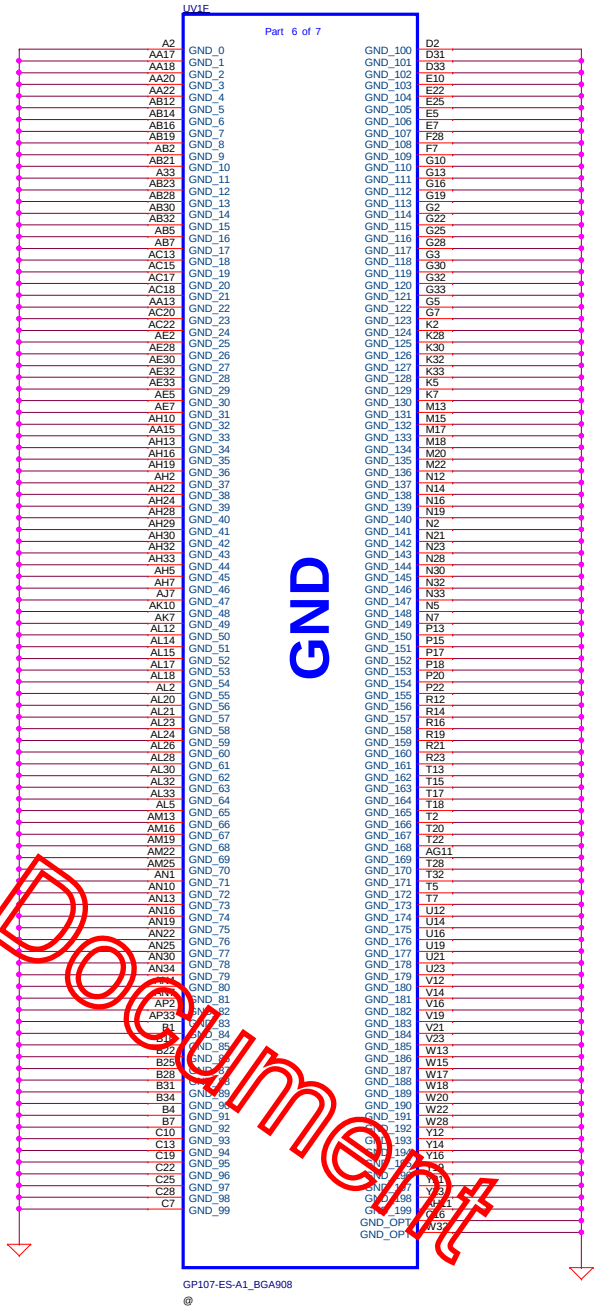
N17P VDDS
1uF*5/4.7uF*5 (under GPU)
330uF*1/22uF*3/10uF*2/4.7uF*2





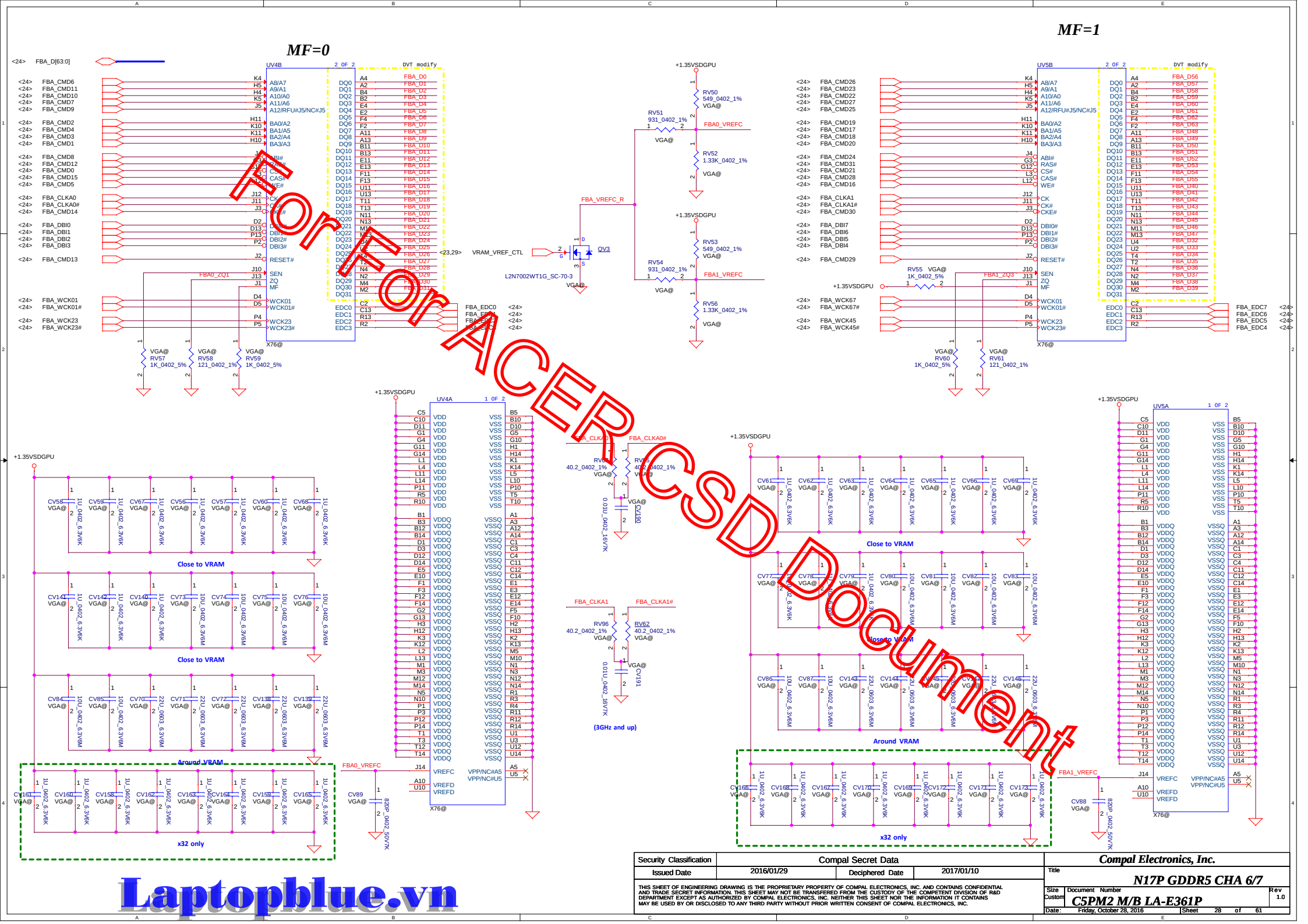
Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: N17P POWER & GND 5/7

Size: Custom | Document Number: C5PM2 M/B LA-E361P | Rev: 1.0

Date: Friday, October 28, 2016 | Sheet 27 of 61



Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.	
Title	N17P GDDR5 CHA 6/7
Size: Custom	Document Number: C5PM2 M/B LA-E361P
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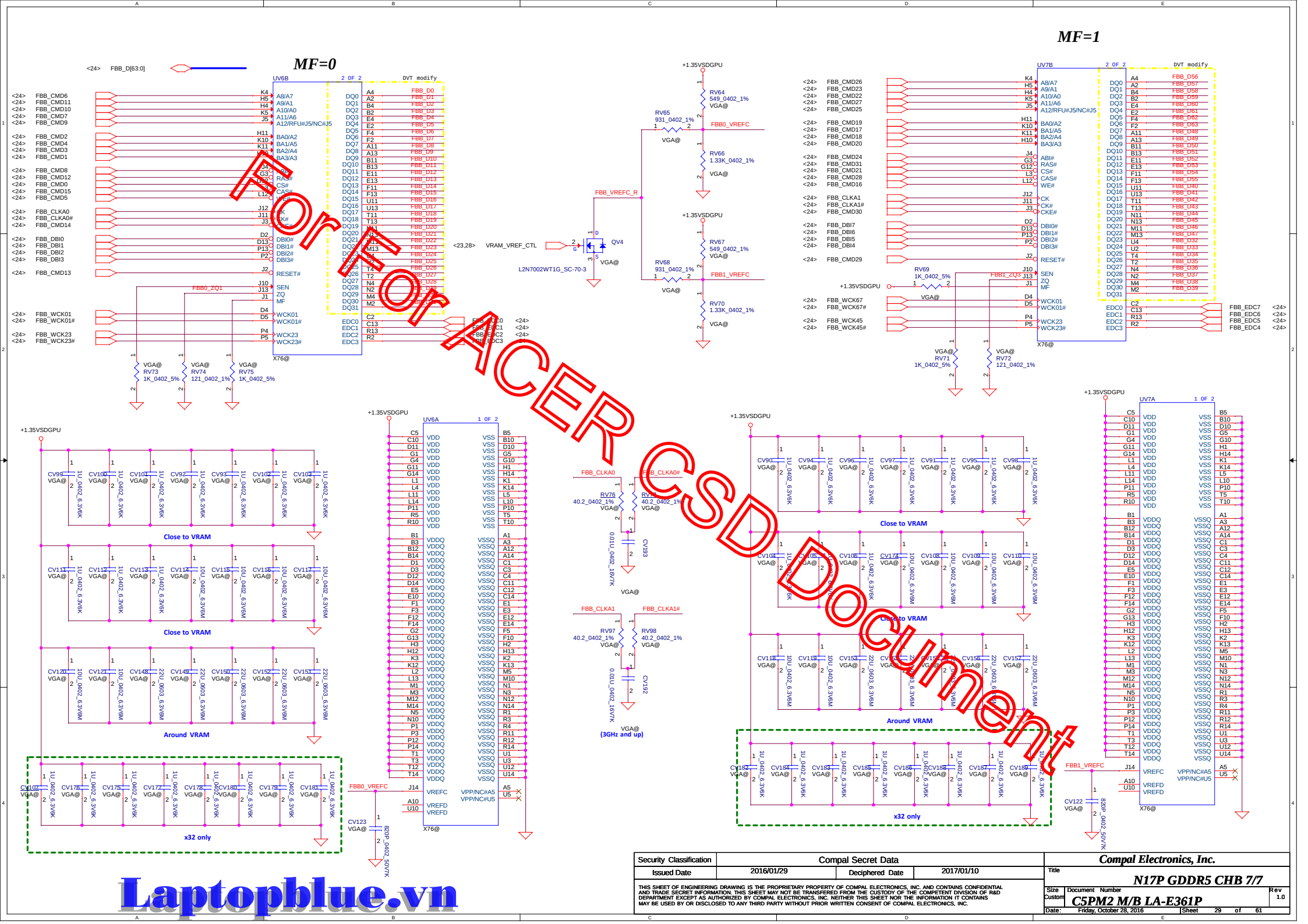
Date: Friday, October 28, 2016	Sheet 28 of 61



Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

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Compal Electronics, Inc.

Title: **N17P GDDR5 CHB 7/7**

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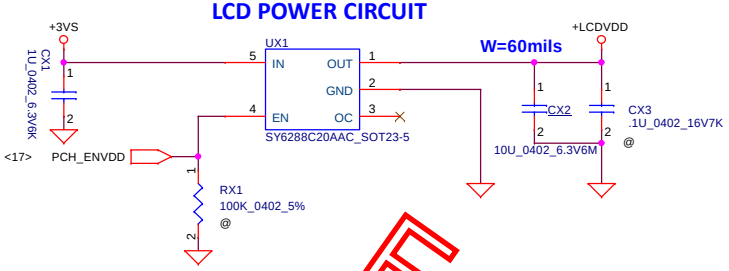
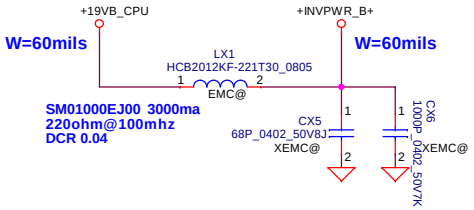
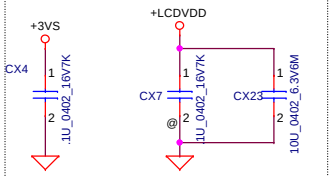
LCD POWER CIRCUIT

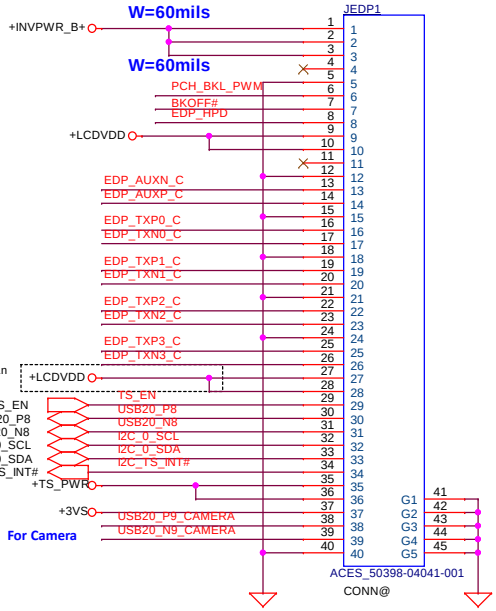


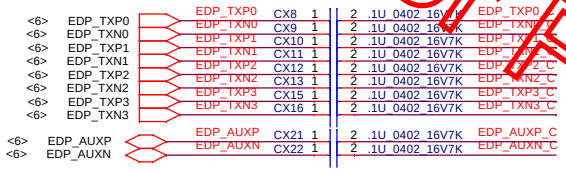


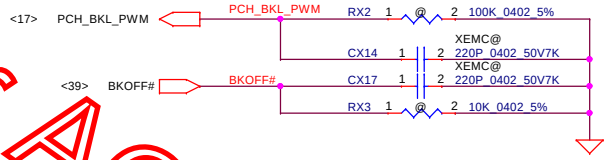
Place closed to JEDP1

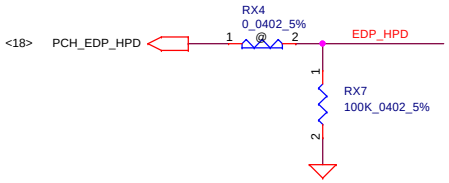


LED PANEL Conn.

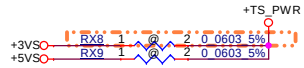






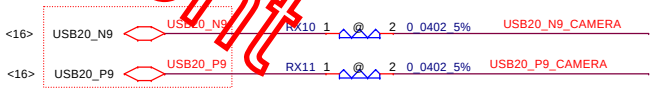


I2C Touch Screen



SPI touch RST follow CRB #544669 P.8

Camera



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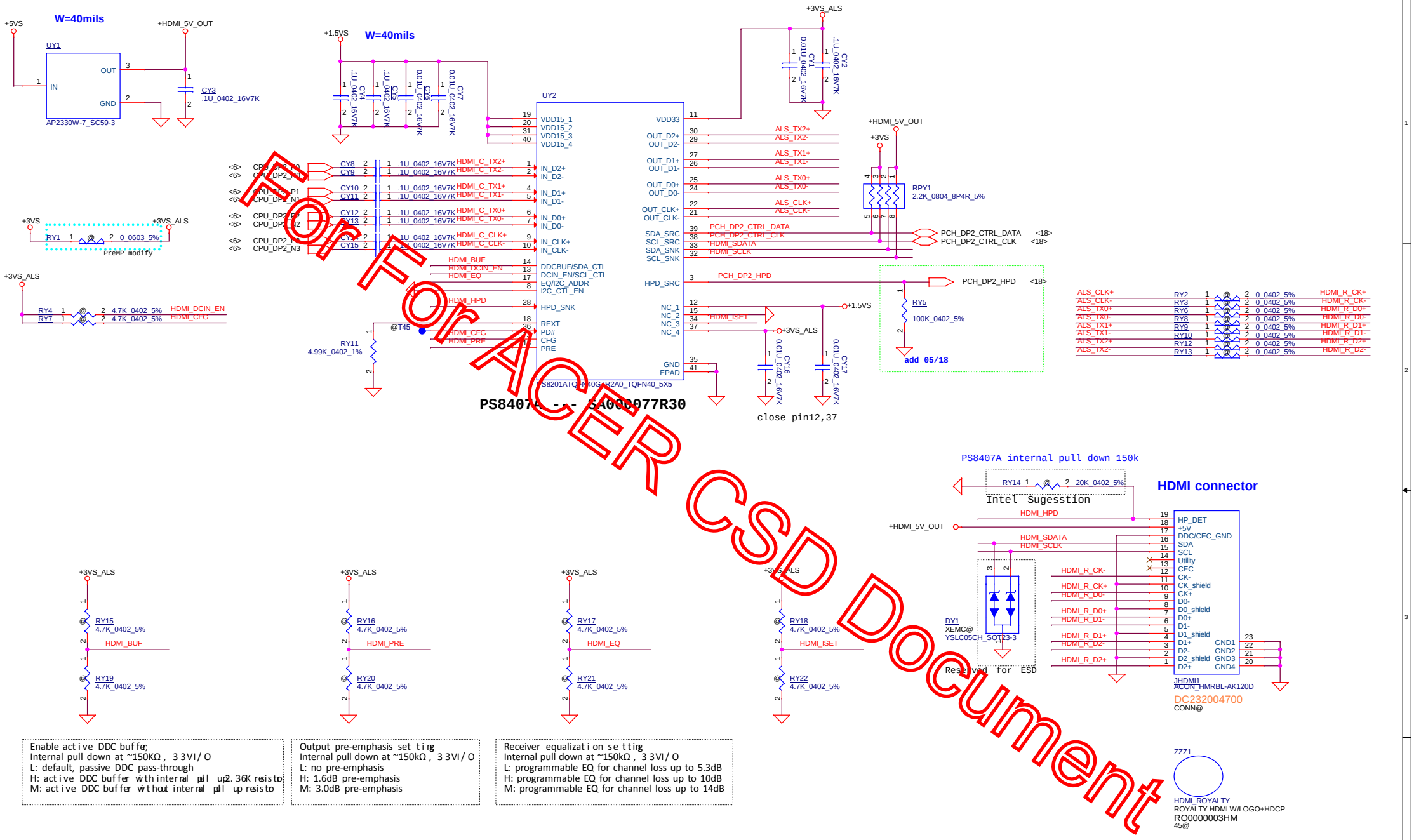
Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.			
Title: eDP CONN.			
Size: Custom	Document Number: C5PM2 M/B LA-E361P		Rev: 1.0
Date: Friday, October 28, 2016	Sheet 30 of 61		



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Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.	
Title	HDMI PS8407 CONN.
Size: Custom	Document Number: C5PM2 M/B LA-E361P
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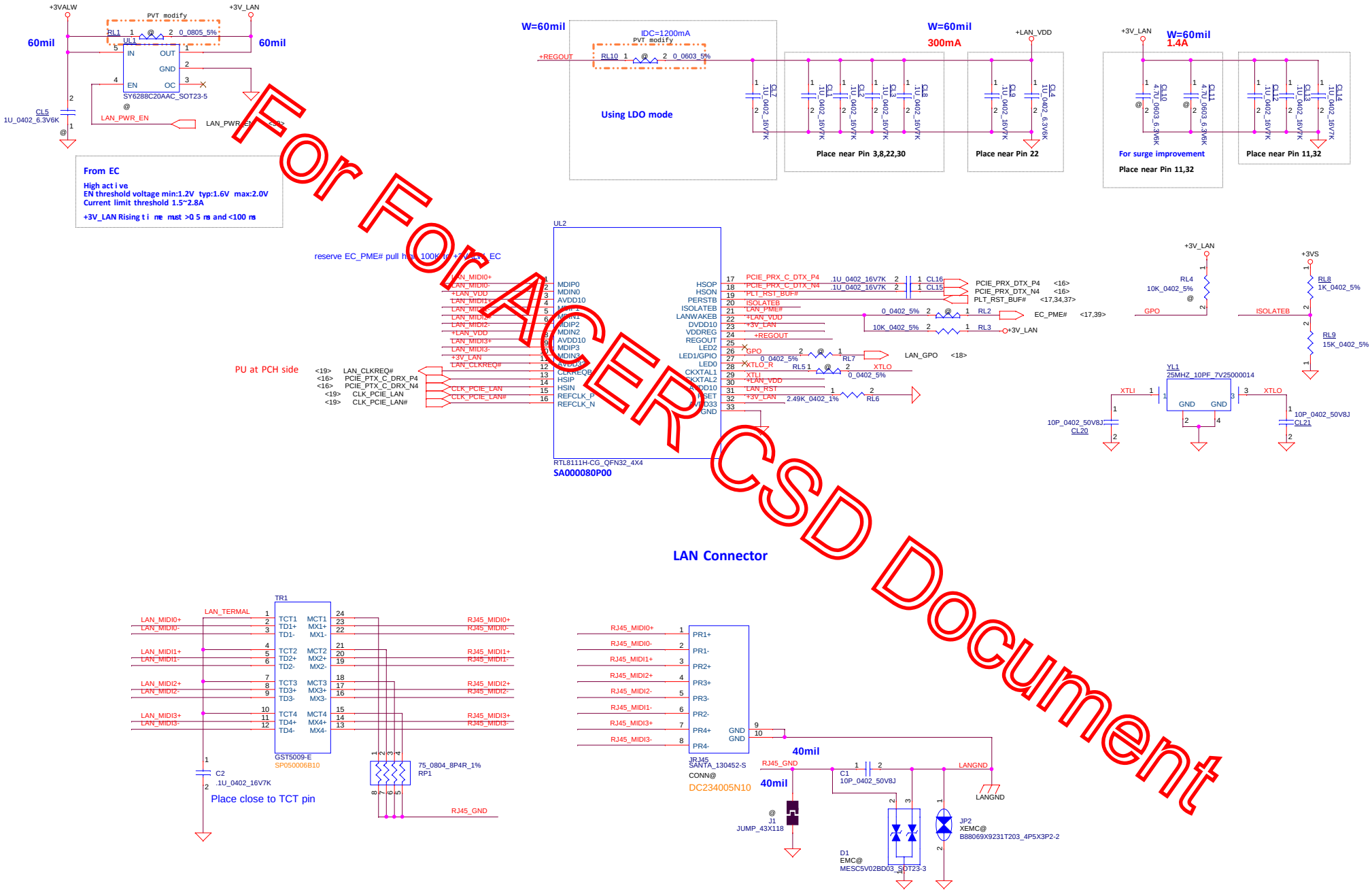
LAN-RTL8111H



Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.	
Title	LAN RTL8411H
Size: Custom	Document Number: C5PM2 M/B LA-E361P
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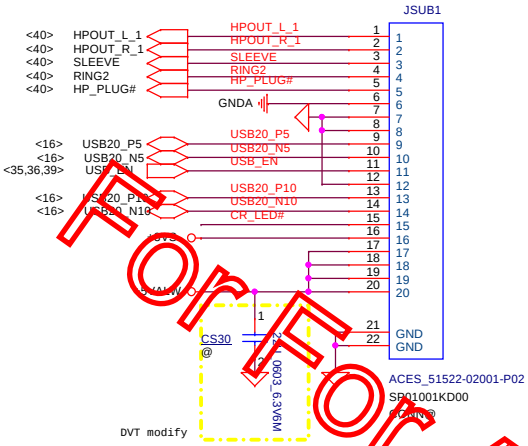
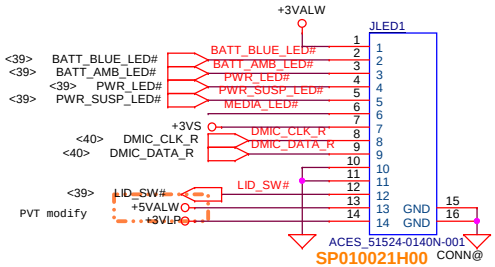
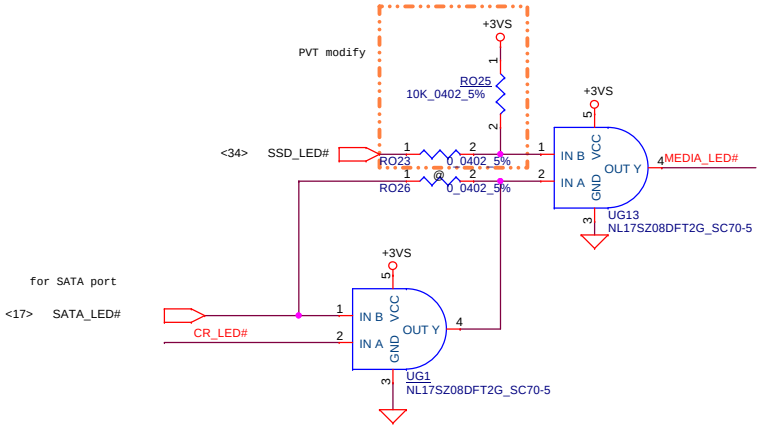
To Fun/B (USB Port 5, + AUDIO)



To LED/B





Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.		
Title: FUN/B & LED/B		
Size: Custom	Document Number: C5PM2 M/B LA-E361P	Rev: 1.0
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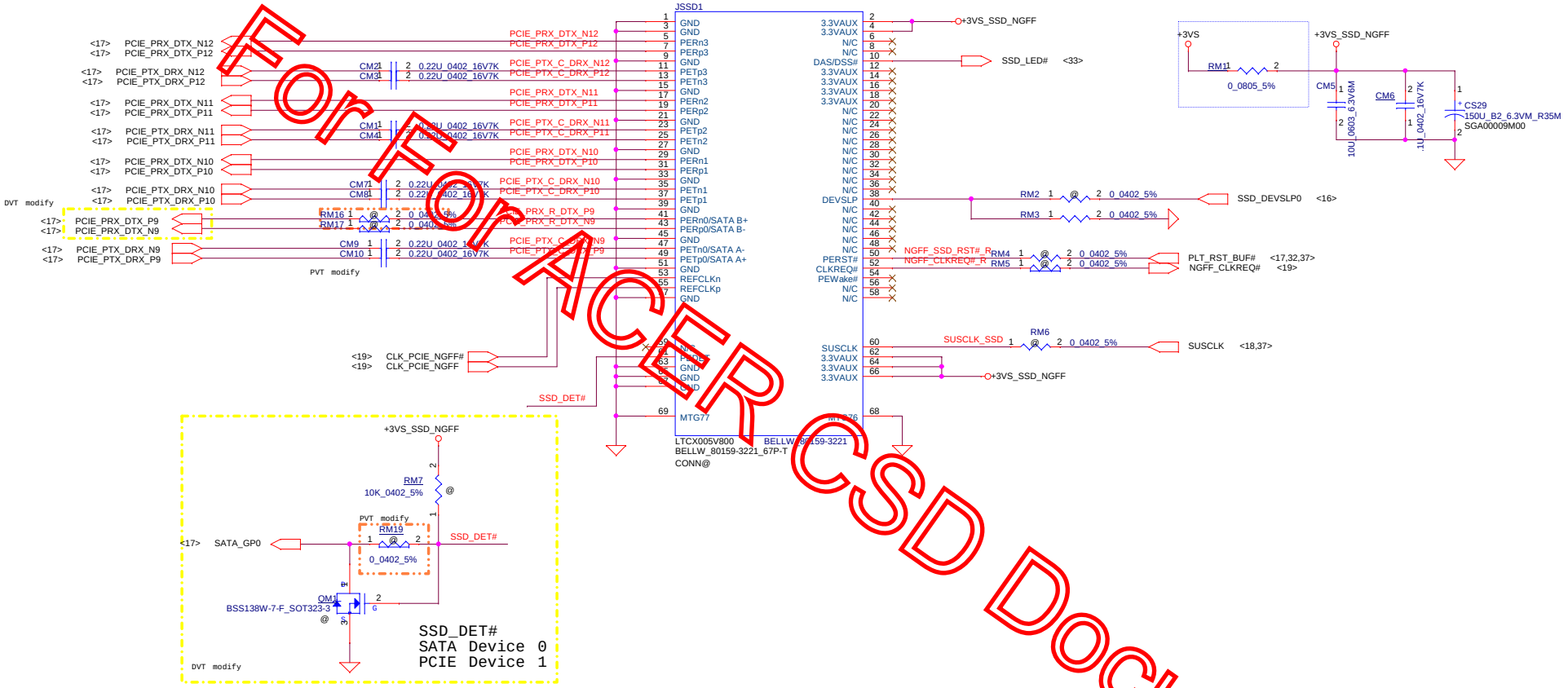

Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.	
Title	mSATA-SSD
Size: Custom	Document Number: C5PM2 M/B LA-E361P
Rev	1.0
Date:	Friday, October 28, 2016
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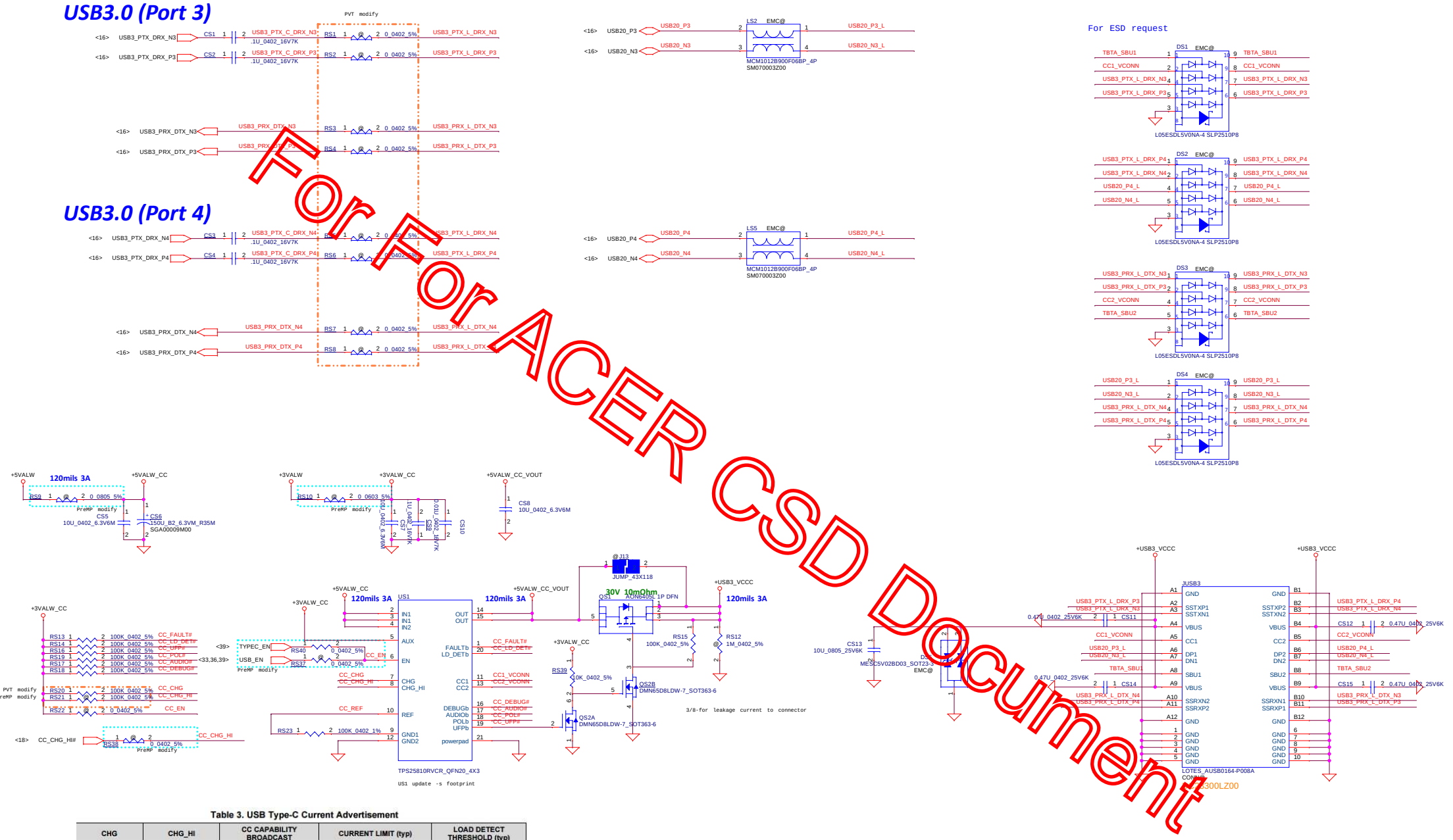

Table 3. USB Type-C Current Advertisement

CHG	CHG_HI	CC CAPABILITY BROADCAST	CURRENT LIMIT (typ)	LOAD DETECT THRESHOLD (typ)
0	0	STD	1.7 A	NA
0	1	STD	1.7 A	NA
1	0	1.5 A	1.7 A	NA
1	1	3 A	3.4 A	1.95 A

Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: CC+USB TYPE C

Size	Document Number	Rev
Custom	C5PM2 M/B LA-E361P	1.0

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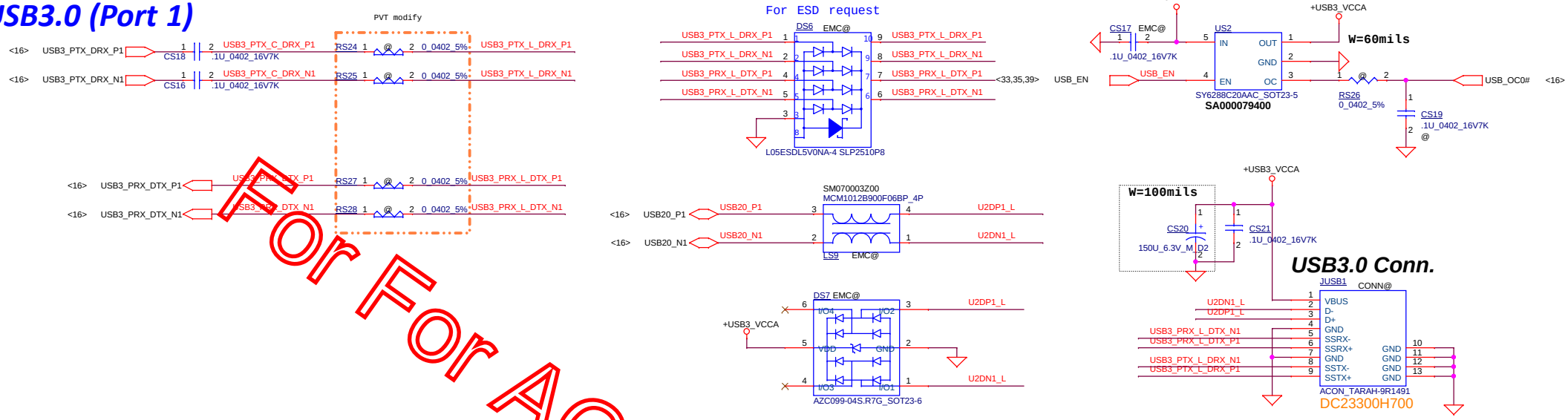
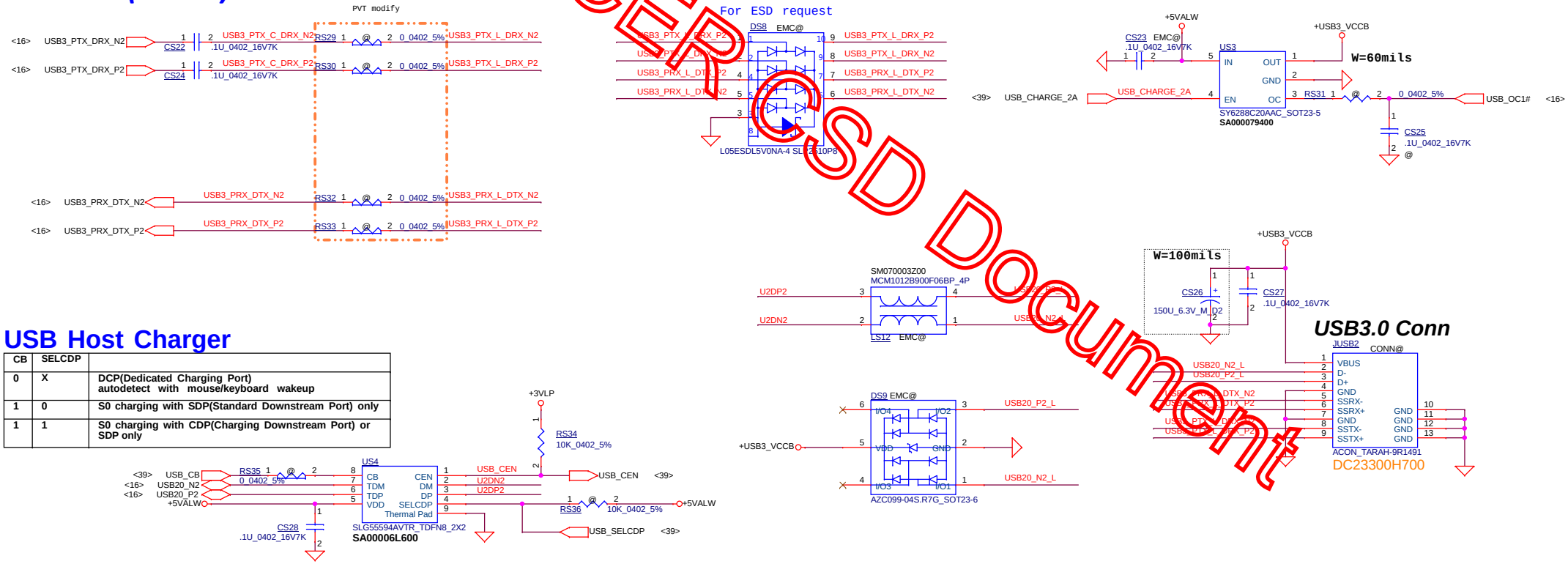
USB3.0 (Port 1)



USB3.0 (Port 2)



USB Host Charger

CB	SELCDP	
0	X	DCP(Dedicated Charging Port) autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP(Standard Downstream Port) only
1	1	S0 charging with CDP(Charging Downstream Port) or SDP only

Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: USB3.0 Conn/USB Charger

Size	Document Number	Rev
Custom	C5PM2 M/B LA-E361P	1.0

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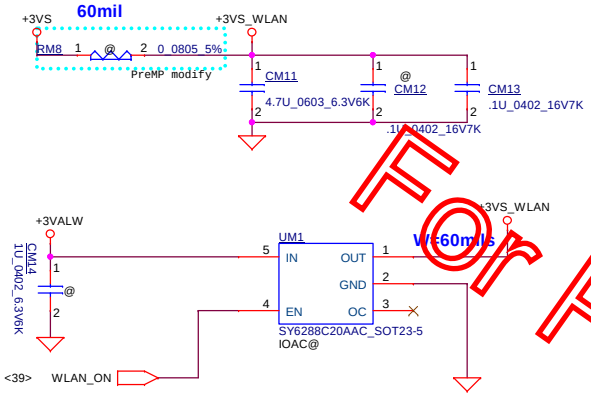
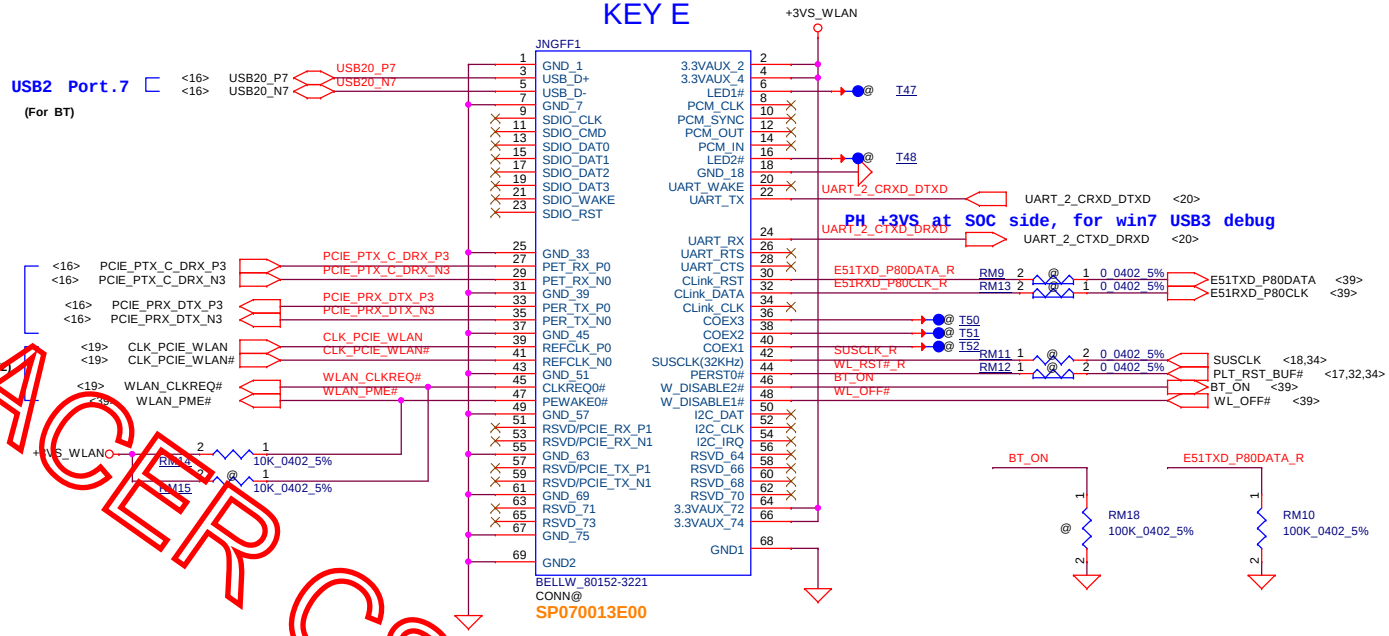
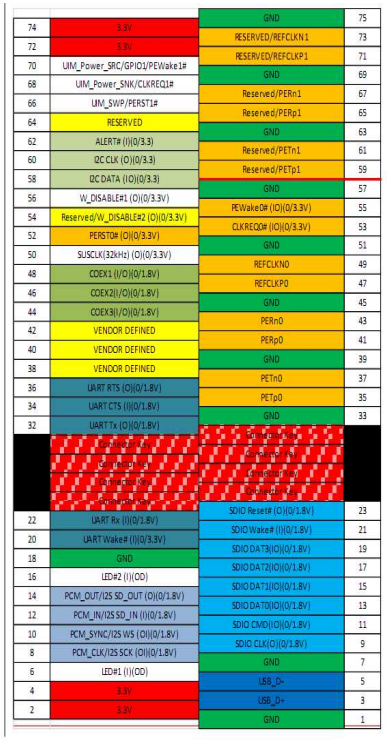
Wireless LAN



KEY E



NGFF WL+BT (KEY E)



3.1.8.4.3.1.7.1. UART Wakeup

The UART power management protocol supports the following 4-wire and 5-wire interfaces:

- ~~BT~~ UART RXD (Input): Receive Data
- ~~BT~~ UART TXD (Output): Transmit Data
- UART RTS (Output): Request to Send (Host Flow Control)
- UART CTS (Output): Clear to Send (Device Flow Control)
- ~~Host Wake Up~~UART Wake (Output): Host wake-up line is optional in case the host support in band wake-up

Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: **M.2 Key E (WLAN)**

Size	Document Number	Rev
Custom	C5PM2 M/B LA-E361P	1.0

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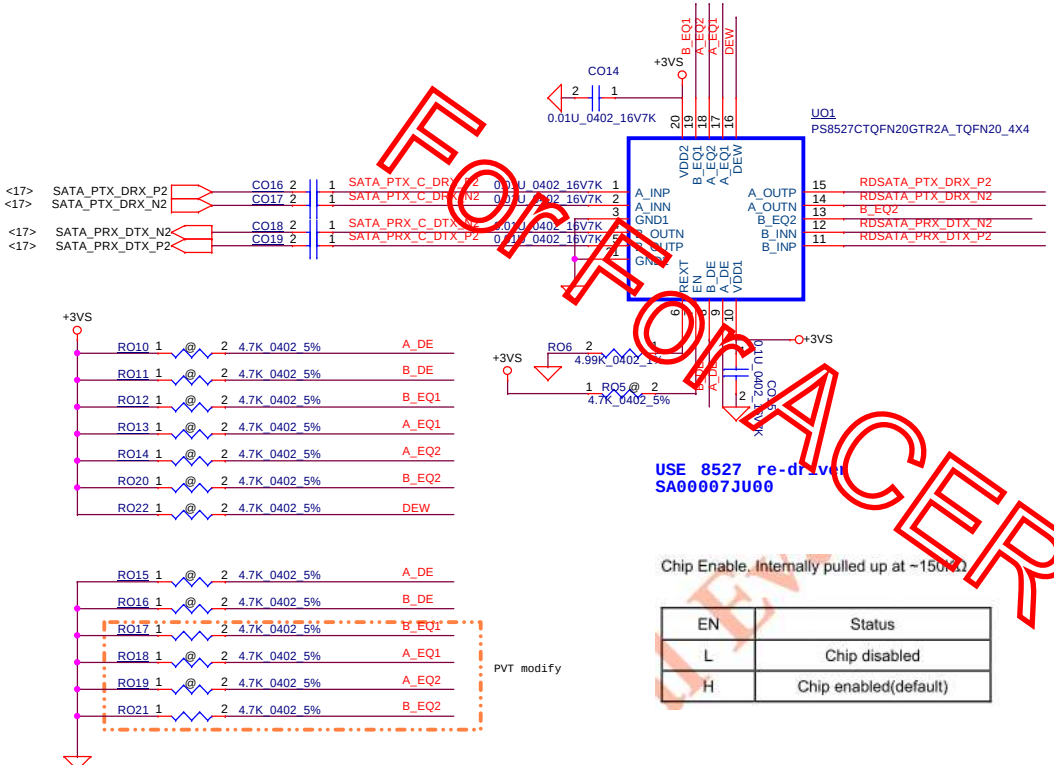
SATA Re-Driver and cable HDD Conn.



USE 8527 re-driver
SA00007JU00

Chip Enable. Internally pulled up at ~150KΩ

EN	Status
L	Chip disabled
H	Chip enabled(default)

Programmable output de-emphasis level setting for channel A.

Internally tied to VDD/2(M status).

A_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-6dB

Programmable output de-emphasis level setting for channel B.

Internally tied to VDD/2(M status).

B_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-6dB

Equalizer control and program for channel A.

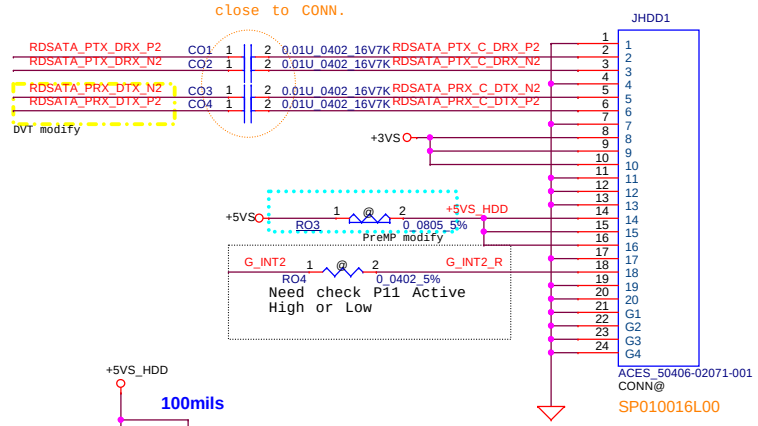
Internally tied to VDD/2 (M status).

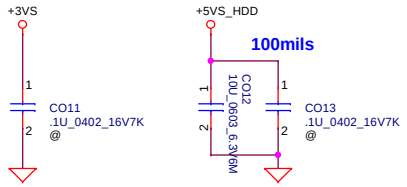
A_EQ2	A_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

Equalizer control and program for channel B.

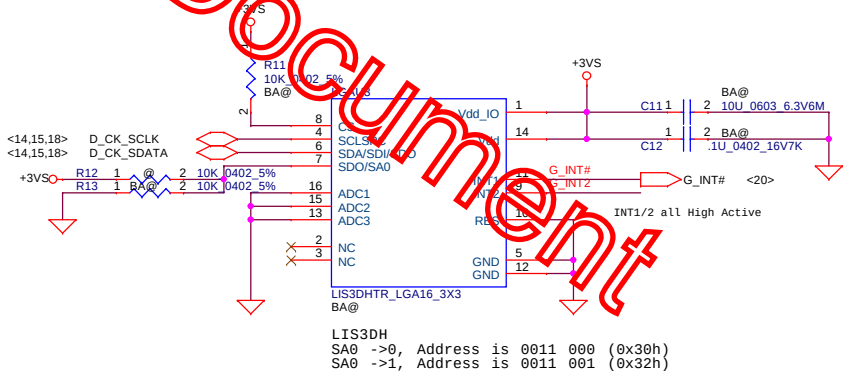
Internally tied to VDD/2(M status).

B_EQ2	B_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB





G-sensor reserved for BA serial



LIS3DH
SA0 ->0, Address is 0011 000 (0x30h)
SA0 ->1, Address is 0011 001 (0x32h)

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Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: HDD/ Re-Driver/ G-sensor

Size	Document Number	Rev
Custom	C5PM2 M/B LA-E361P	1.0

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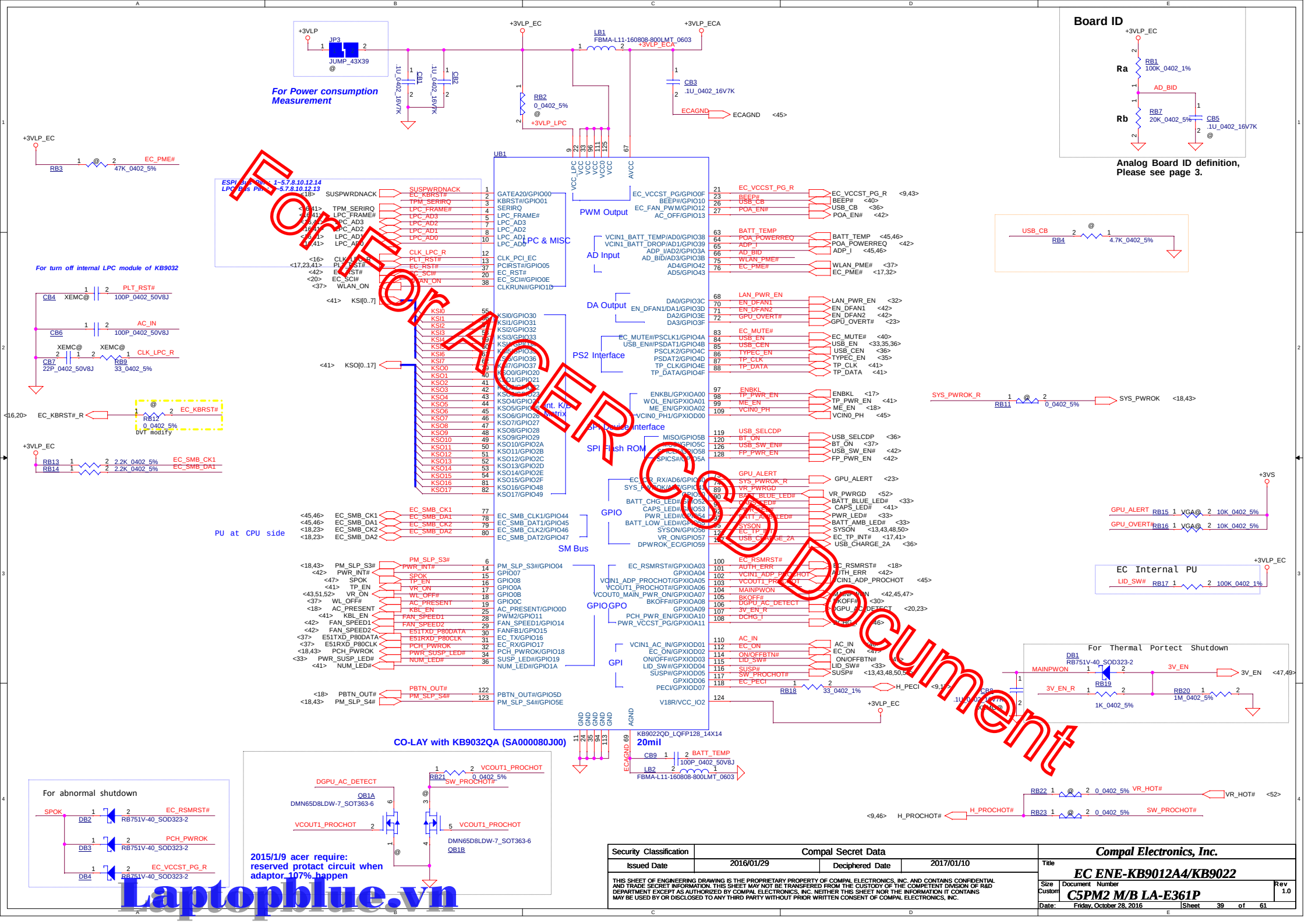

Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: EC ENE-KB9012A4/KB9022

Size: Custom | Document Number: C5PM2 M/B LA-E361P | Rev: 1.0

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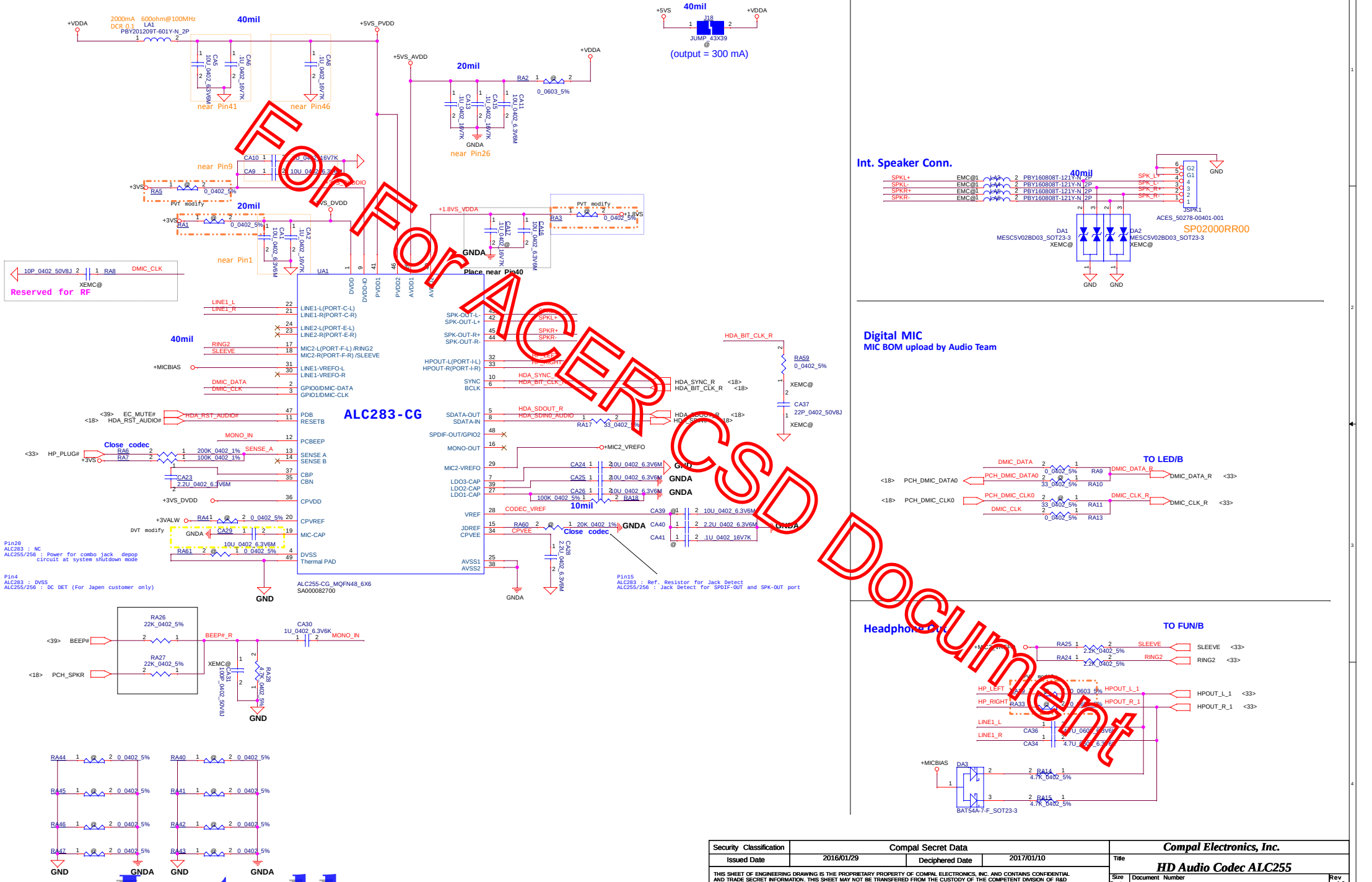
HD Audio Codec



Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.			
Title: HD Audio Codec ALC255			
Size: Custom	Document Number: C5PM2 M/B LA-E361P		Rev: 1.0
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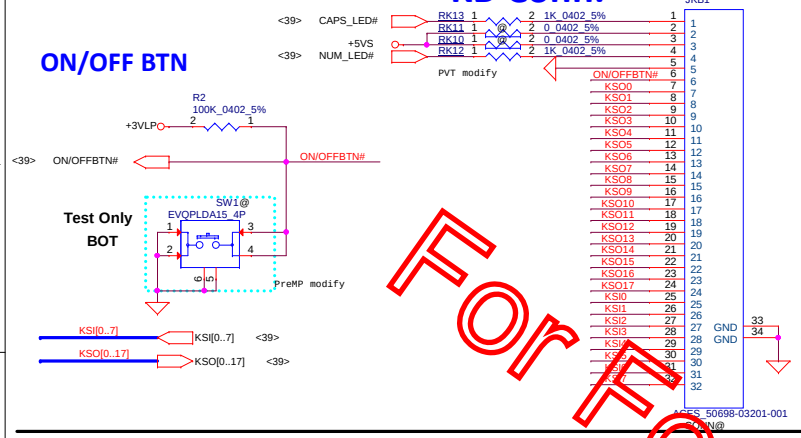
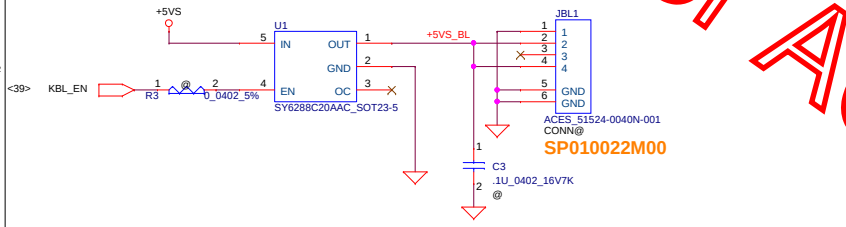
KB Conn.

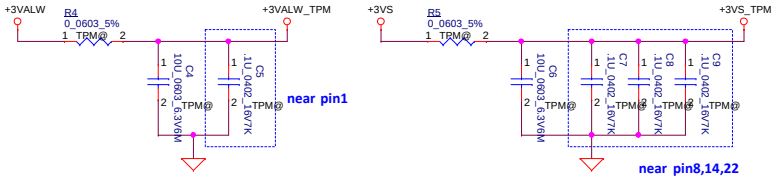
ON/OFF BTN



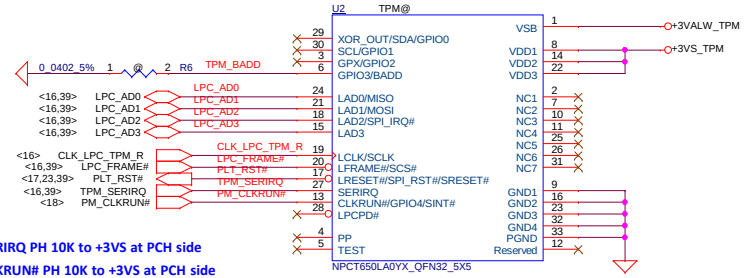
KB BackLight



TPM



BADD	SELECTION
* 1	AEh(write), AFh(read)



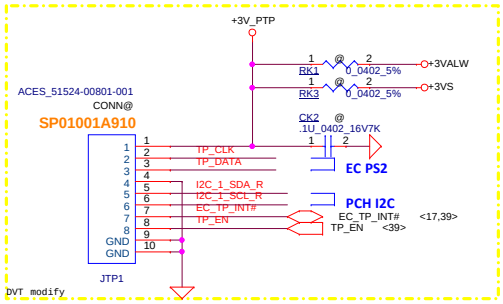
SERIRQ PH 10K to +3VS at PCH side

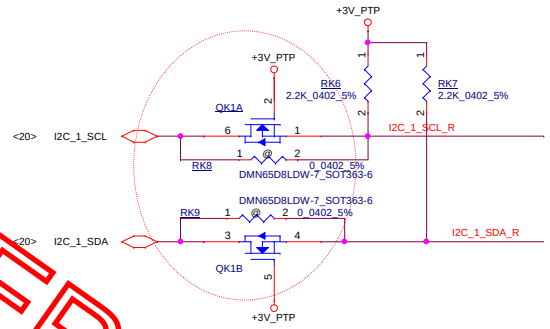
CLKRUN# PH 10K to +3VS at PCH side

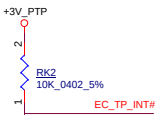
LPCPD# had internal PH

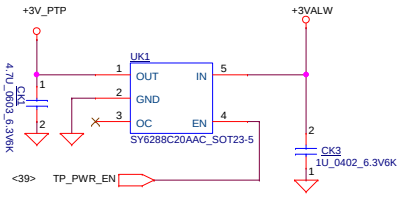
CLK_LPC_TPM_R R7 33_0402_5% C10 22P_0402_50V8J XEMC@

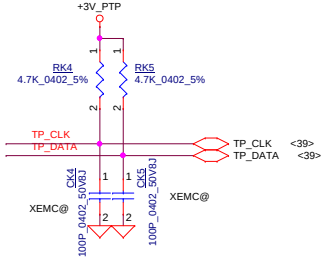
TP/B Conn.











Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: KB & TP & TPM Connector

Size	Document Number	Rev
Custom	C5PM2 M/B LA-E361P	1.0

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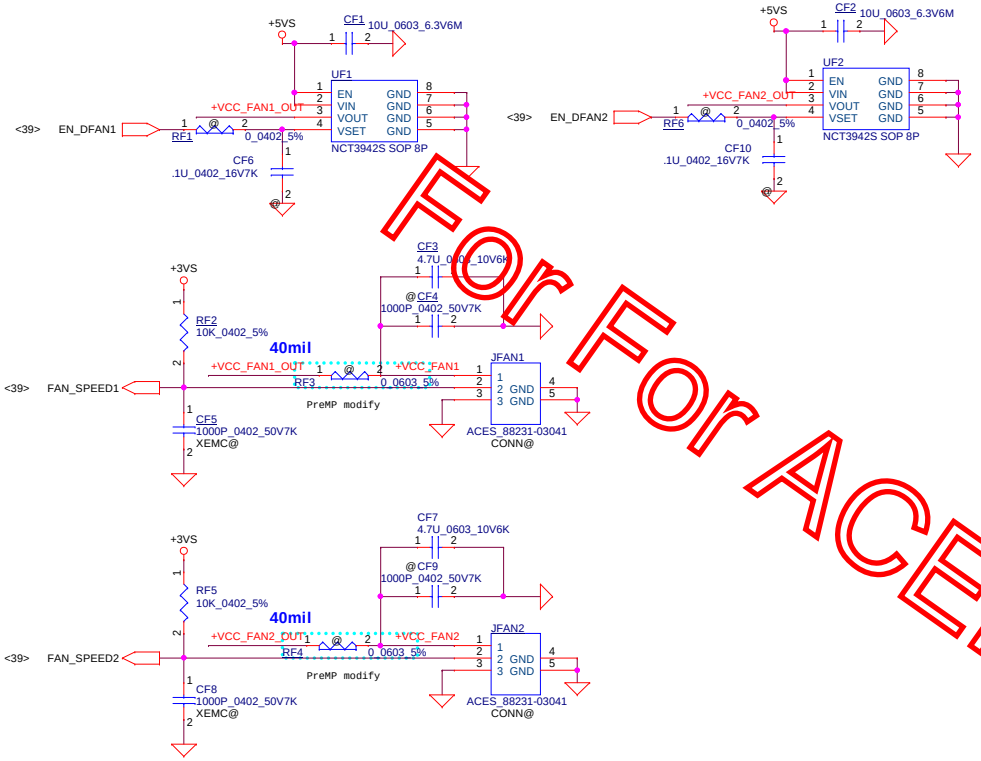
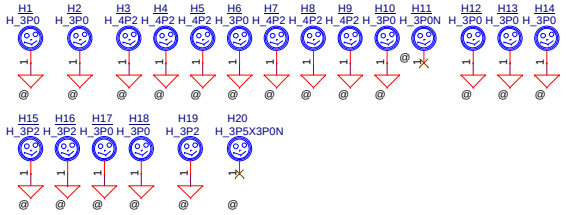
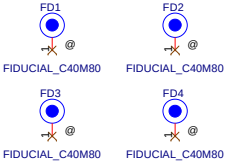
FAN Conn

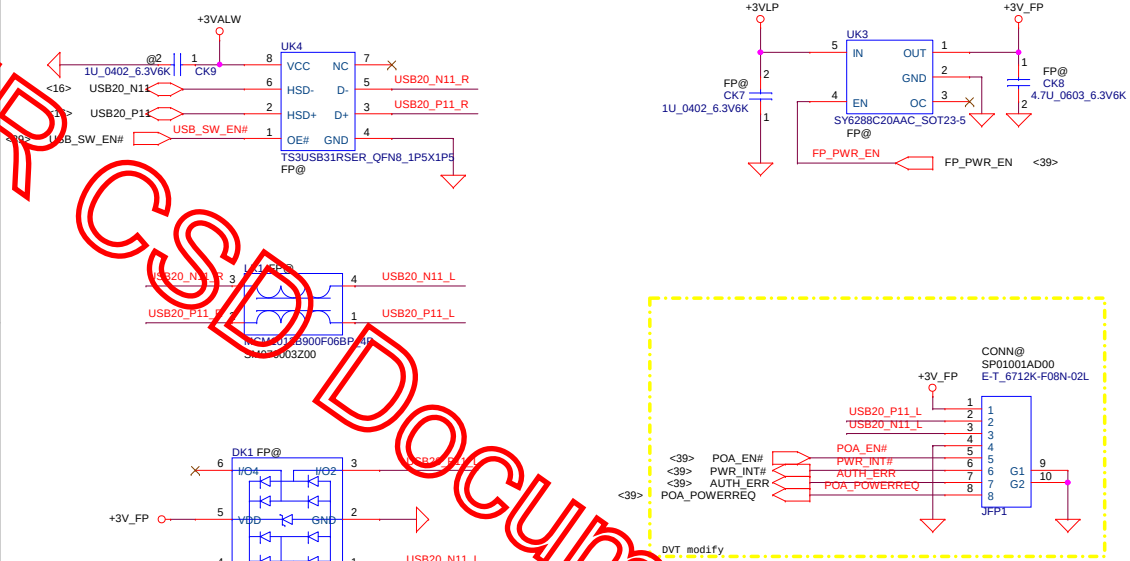


Screw Hole



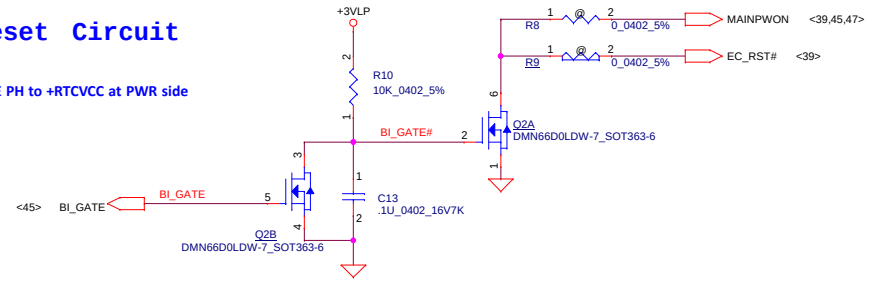


Finger Print POA



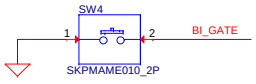
Reset Circuit

BI_GATE PH to +RTCVCC at PWR side

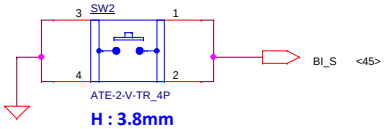


Reset Button

Reset Button



BI SW



H : 3.8mm

Release : Battery Of
Push : Battery ON

Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: FAN & FP & Screw Hole

Size	Document Number	Rev
Custom	C5PM2 M/B LA-E361P	1.0

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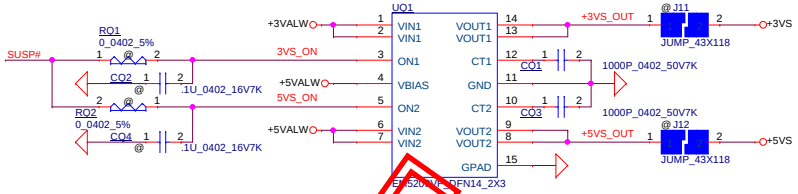
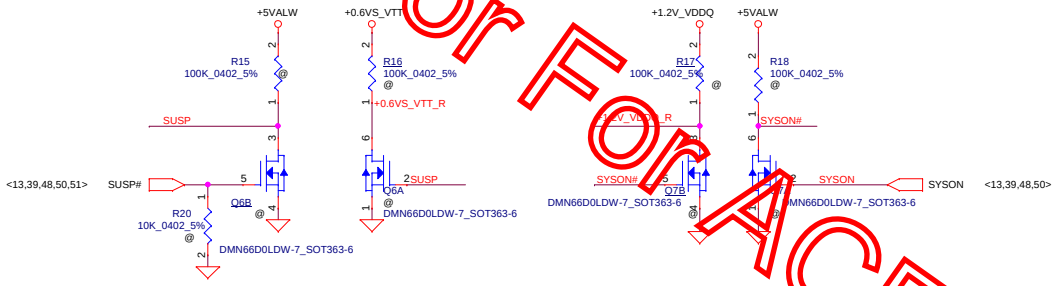
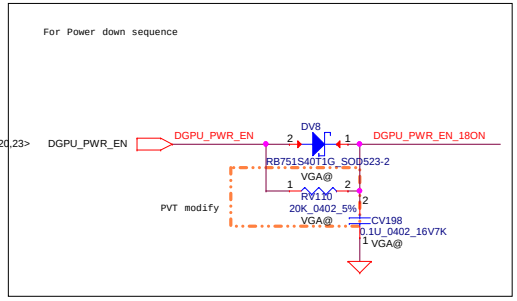
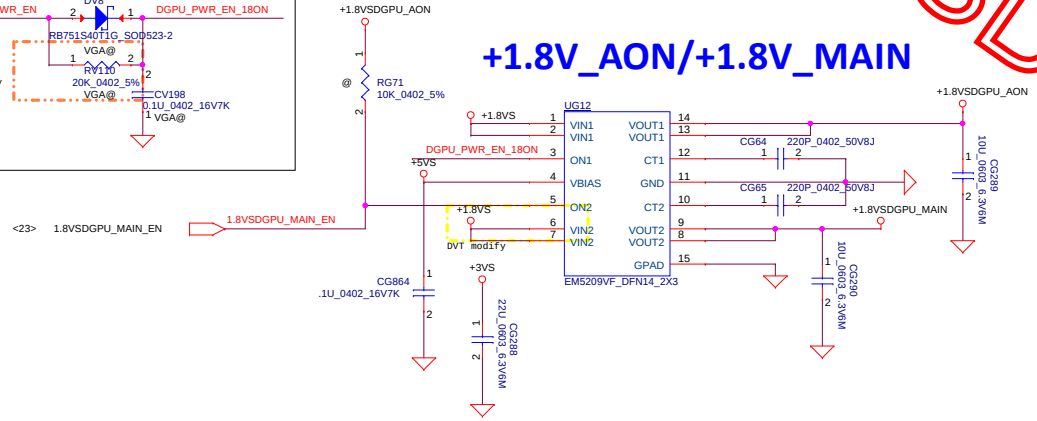
DC & VGA Interface



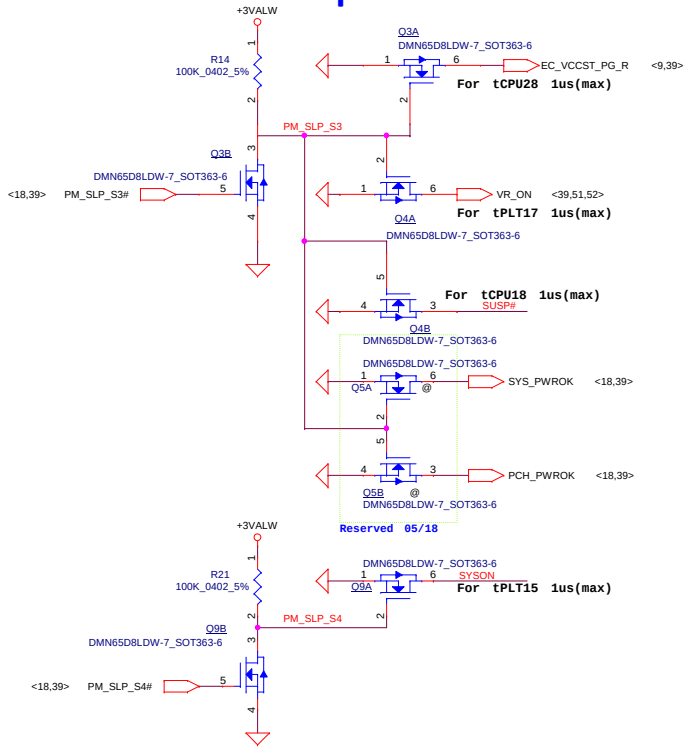


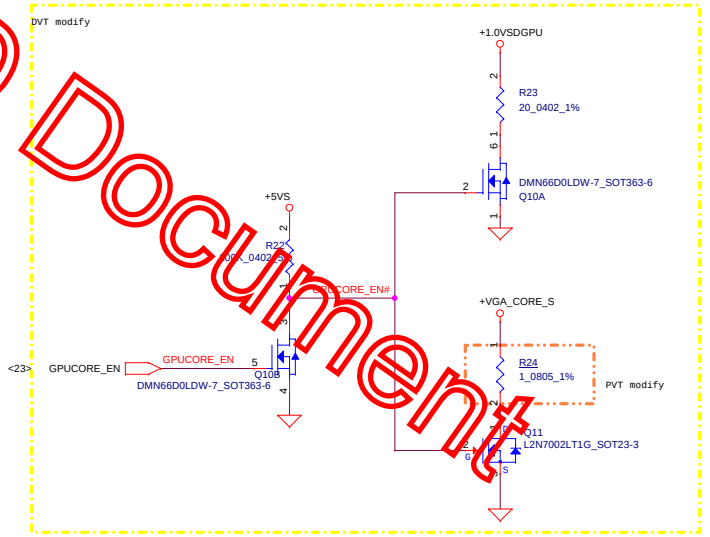


+1.8V_AON/+1.8V_MAIN



For Power Of f Sequence





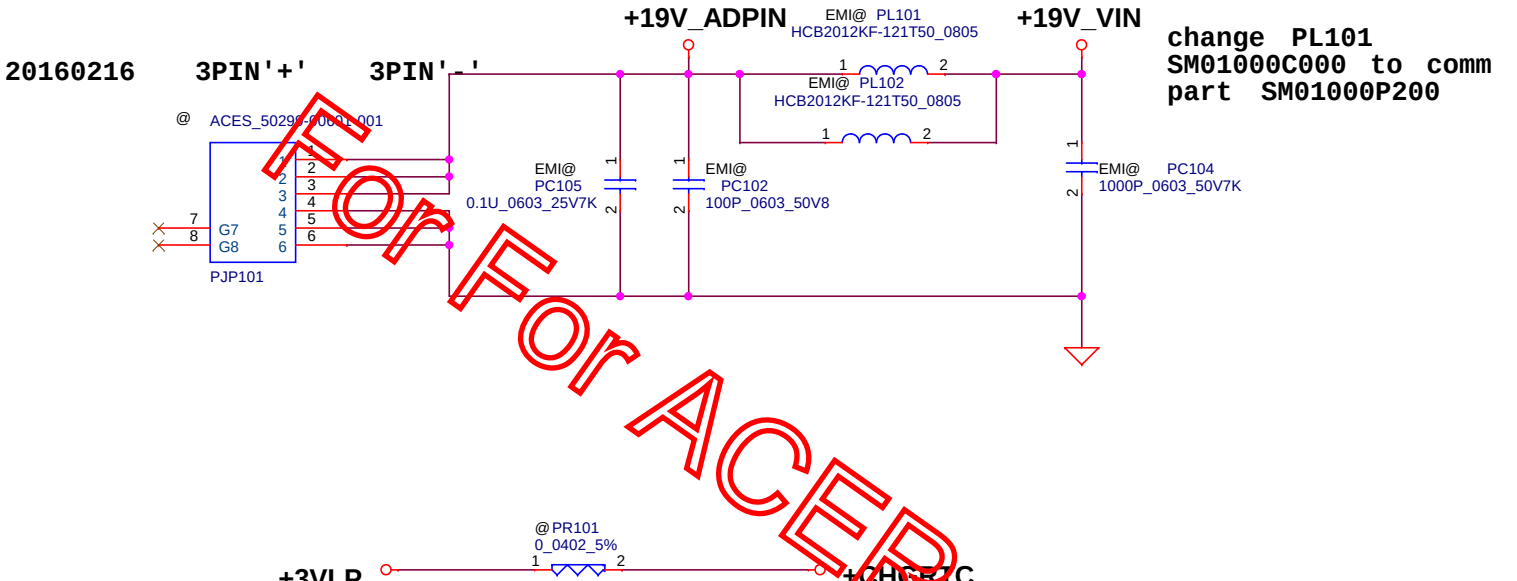
Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
Custom	C5PM2 M/B LA-E361P	1.0

Date: Friday, October 28, 2016 Sheet 43 of 61



Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: DCIN

Size: Custom | Document Number: C5PM2 M/B LA-E361P | Rev: 1.0

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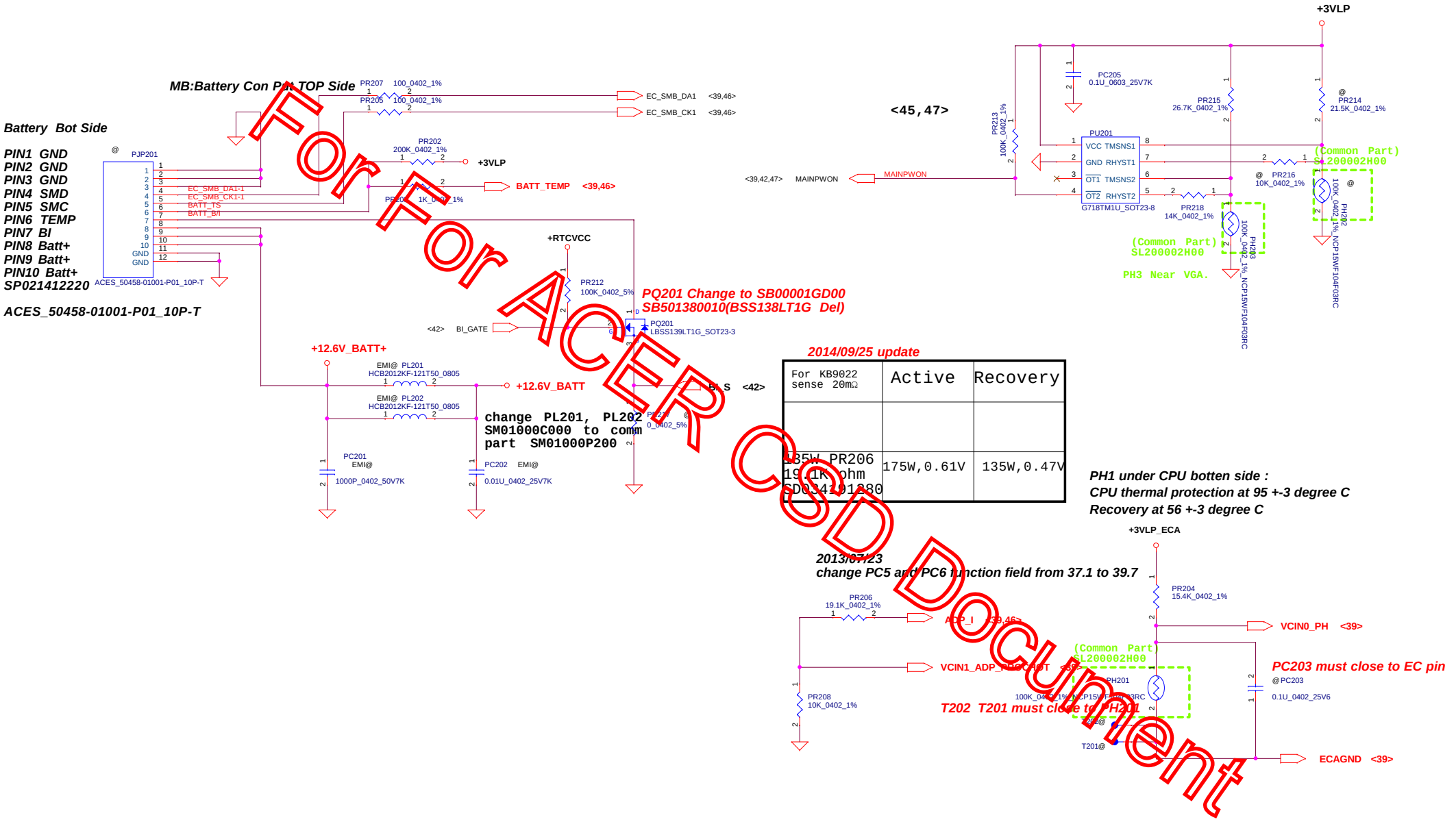


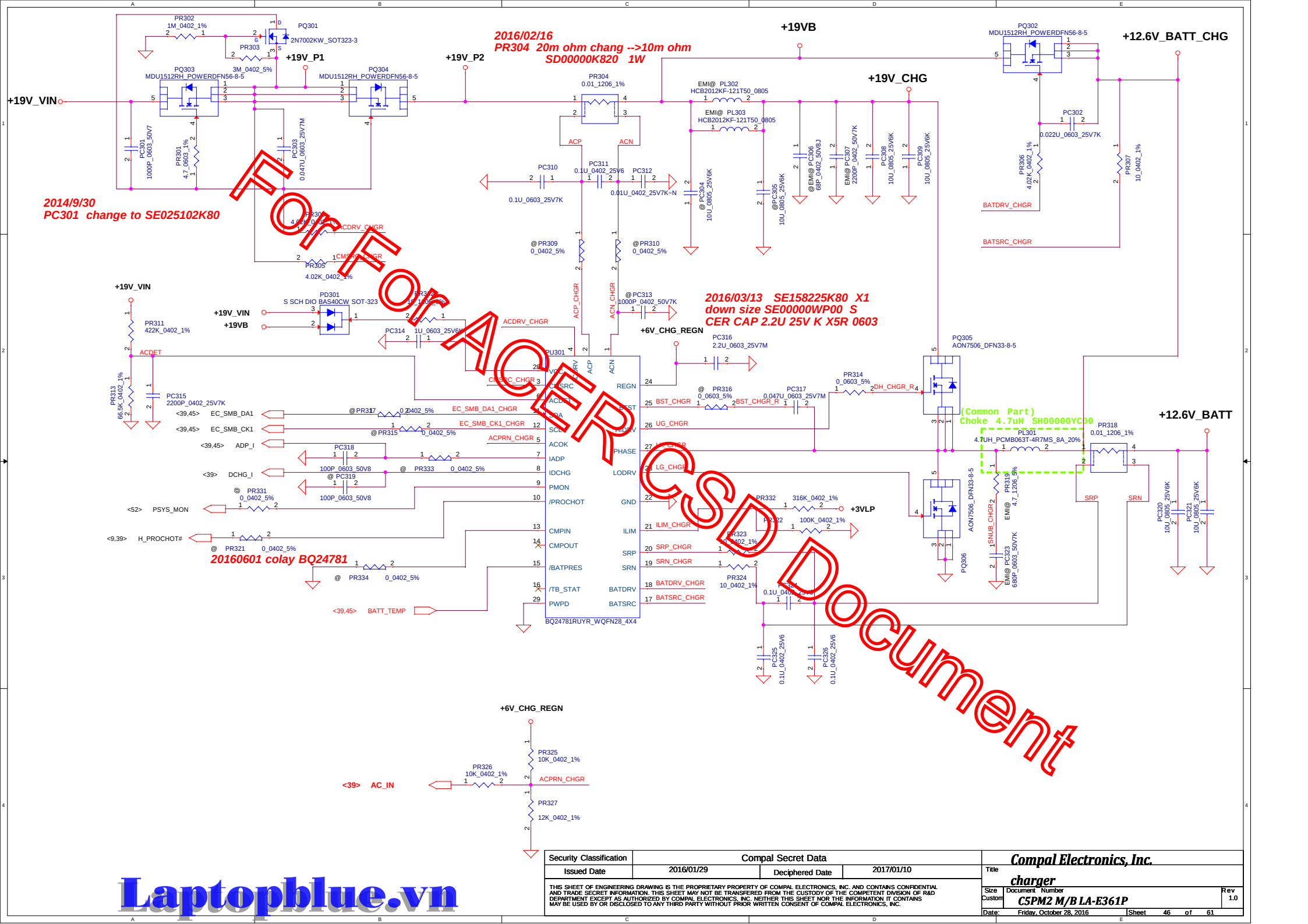
Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: BATTERY CONN/OTP

Size: Custom | Document Number: C5PM2 M/B LA-E361P | Rev: 1.0

Date: Friday, October 28, 2016 | Sheet 45 of 61



Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

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Compal Electronics, Inc.

Title: charger

Size	Document Number	Rev
Custom	C5PM2 M/B LA-E361P	1.0

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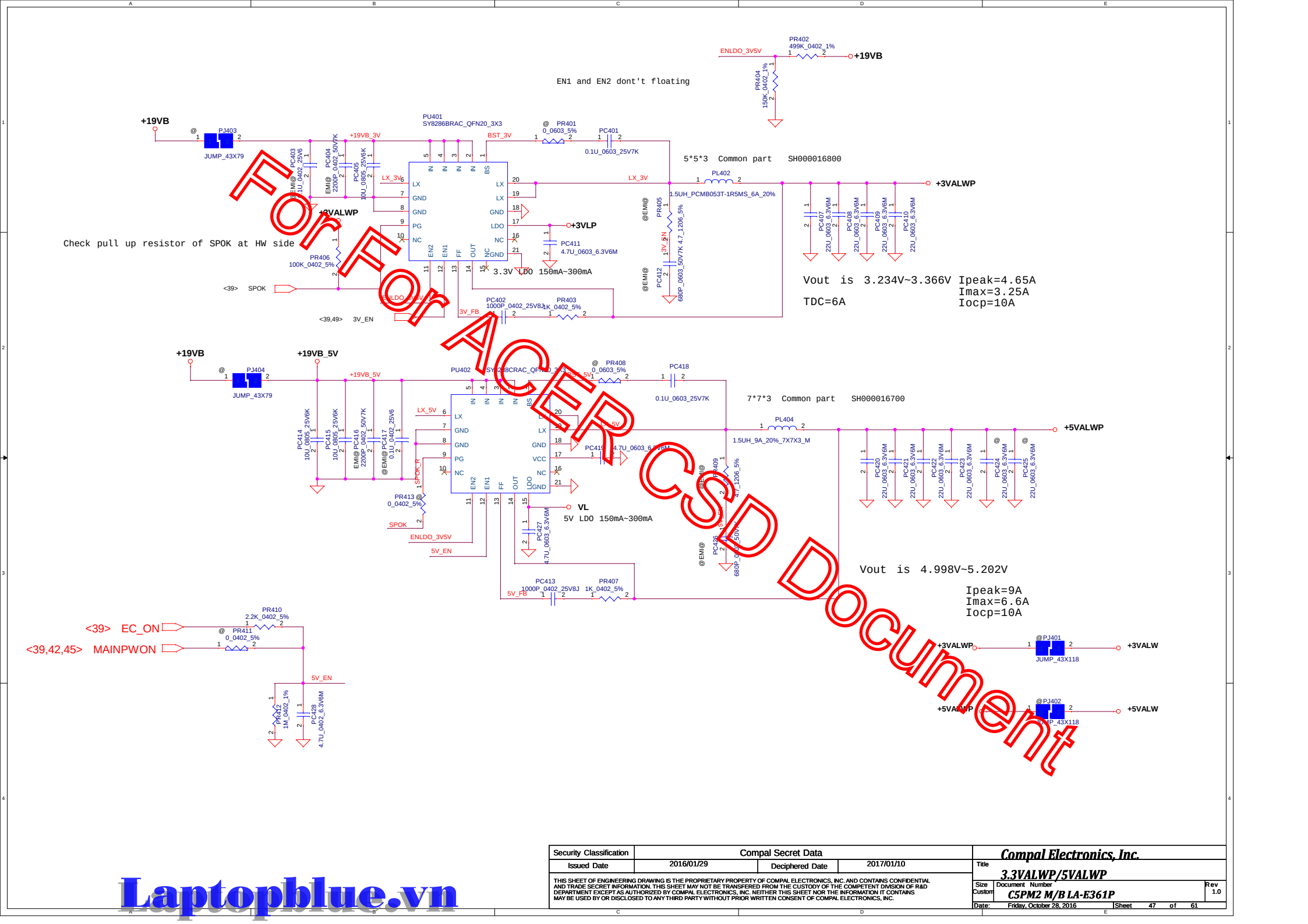


Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.

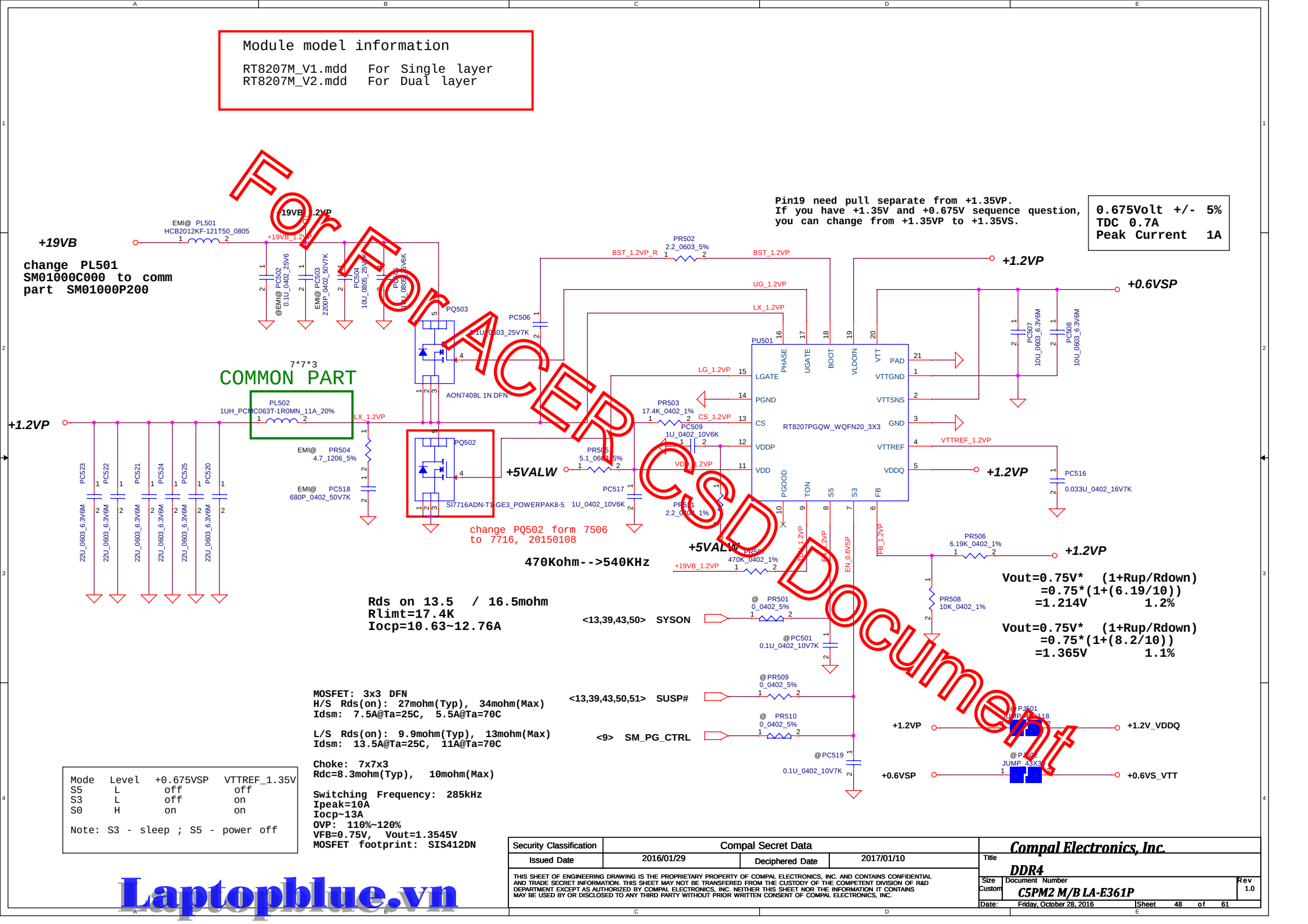
Title: 3.3VALWP/5VALWP

Size: Custom | Document Number: C5PM2 M/B LA-E361P | Rev: 1.0

Date: Friday, October 28, 2016 | Sheet 47 of 61

Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer



Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.

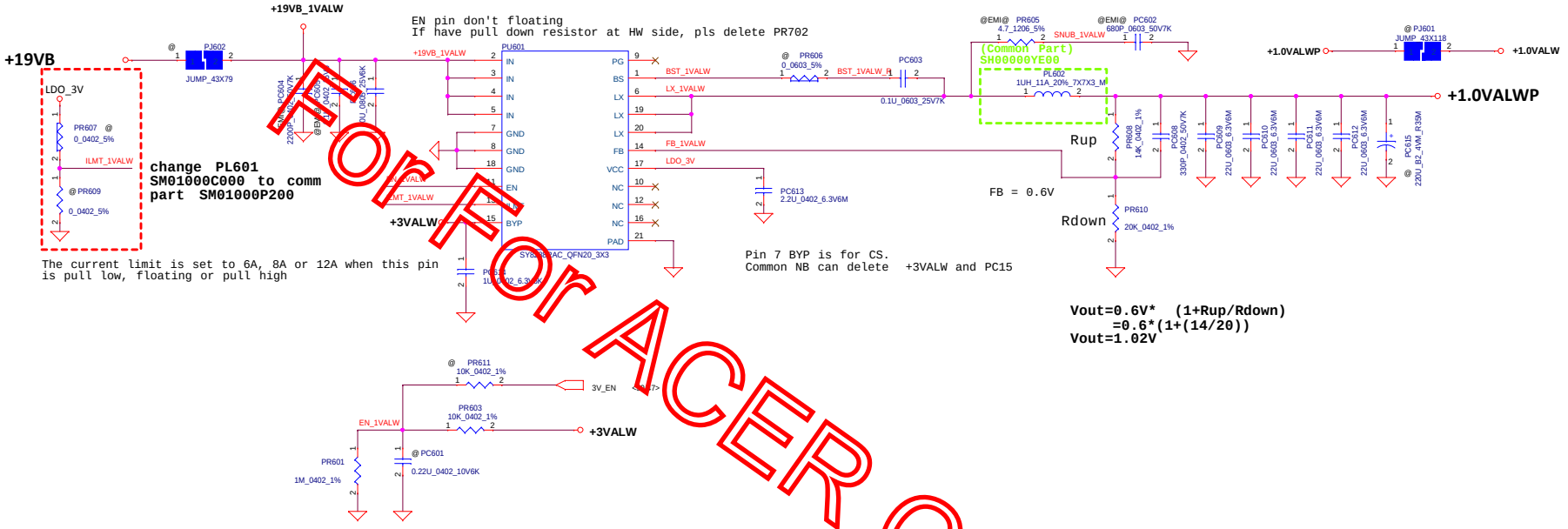
Title: DDR4

Size: Custom | Document Number: C5PM2 M/B LA-E361P | Rev: 1.0

Date: Friday, October 28, 2016 | Sheet 48 of 61

Module model information

SYX196D_V3.mdd



Function Field :
VCCEDPIO : IC-35.21 , others - 35.22
VCCEDRAM : IC-35.25 , others - 35.26

Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: 1V

Size: C | Document Number: C5PM2 M/B LA-E361P | Rev: 1.0

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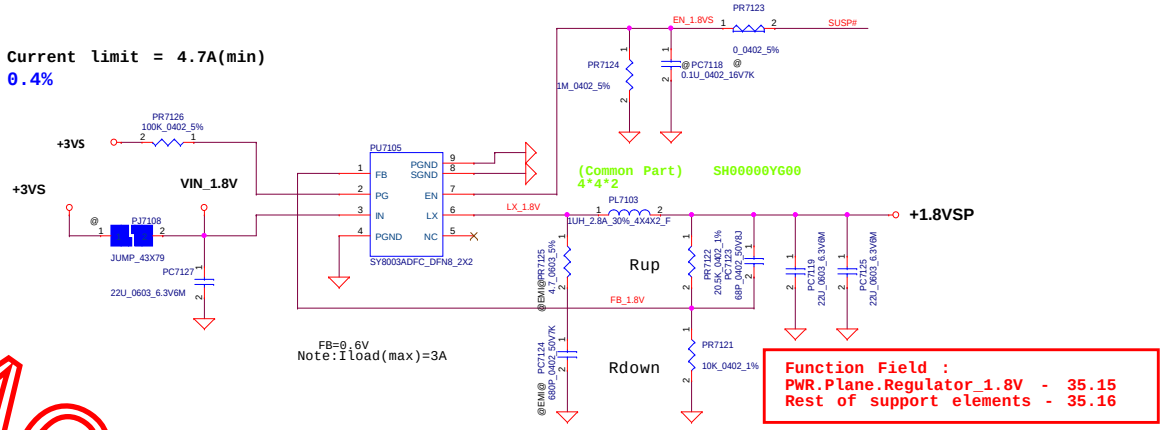
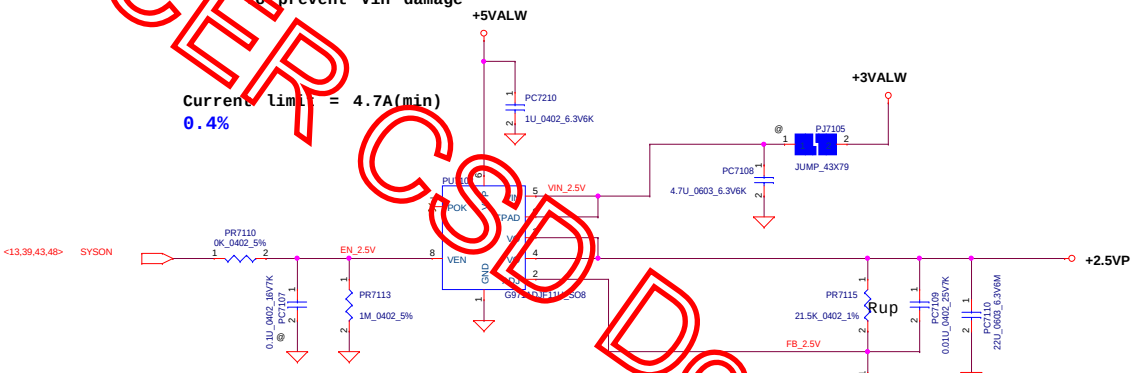
Current limit = 4.7A(min)
0.4%



Function Field :
PWR.Plane.Regulator_1.8V - 35.15
Rest of support elements - 35.16

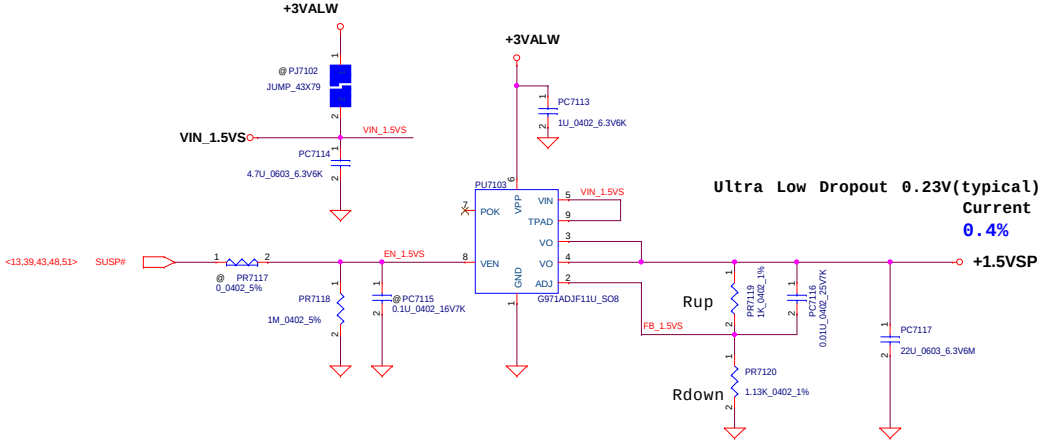
Note:
When design Vin=5V, please stuff snubber
to prevent Vin damage

Current limit = 4.7A(min)
0.4%



Function Field :
PWR.Plane.Regulator_2.5V - 35.13
Rest of support elements - 35.14

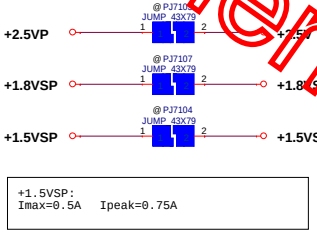
Vout=0.8V* (1+(12.7/10)) = 1.816V



Ultra Low Dropout 0.23V(typical) at 3A Output Current
Current limit = 4.7A(min)
0.4%

Vout=0.8V* (1+Rup/Rdown)
Vout=0.8V* (1+(1/1.13)) = 1.507V

Vout=0.8V* (1+(21.5/10)) = 2.52V 0.8%



+1.5VSP:
Imax=0.5A Ipeak=0.75A

Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: 1.5VS/2.5V

Size: C | Document Number: C5PM2 M/B LA-E361P | Rev: 1.0

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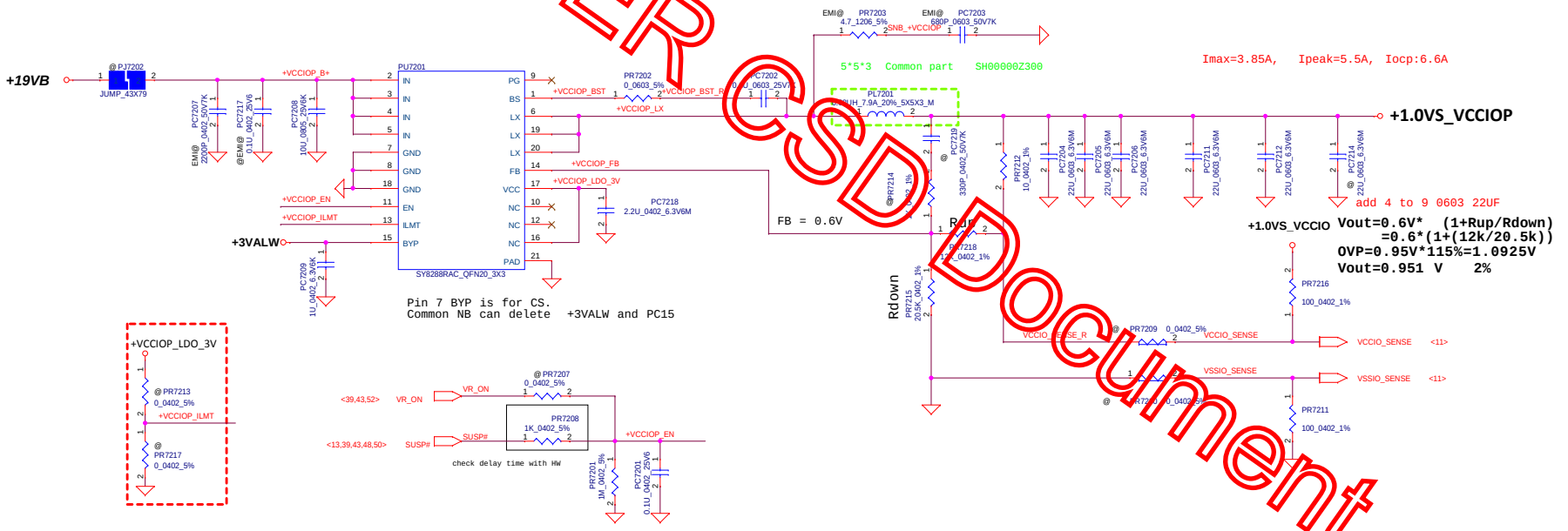
Note:Iload(max)=5.5A

IOCP=7A~8A(typ)

+1.0VS_VCCIOP — @ PJ7201 JUMP_43X118 — +1.0VS_VCCIO



Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: C5PM2 M/B LA-E361P

Size: C | Document Number: 1.0VS_VCCIO | Rev: 1.0

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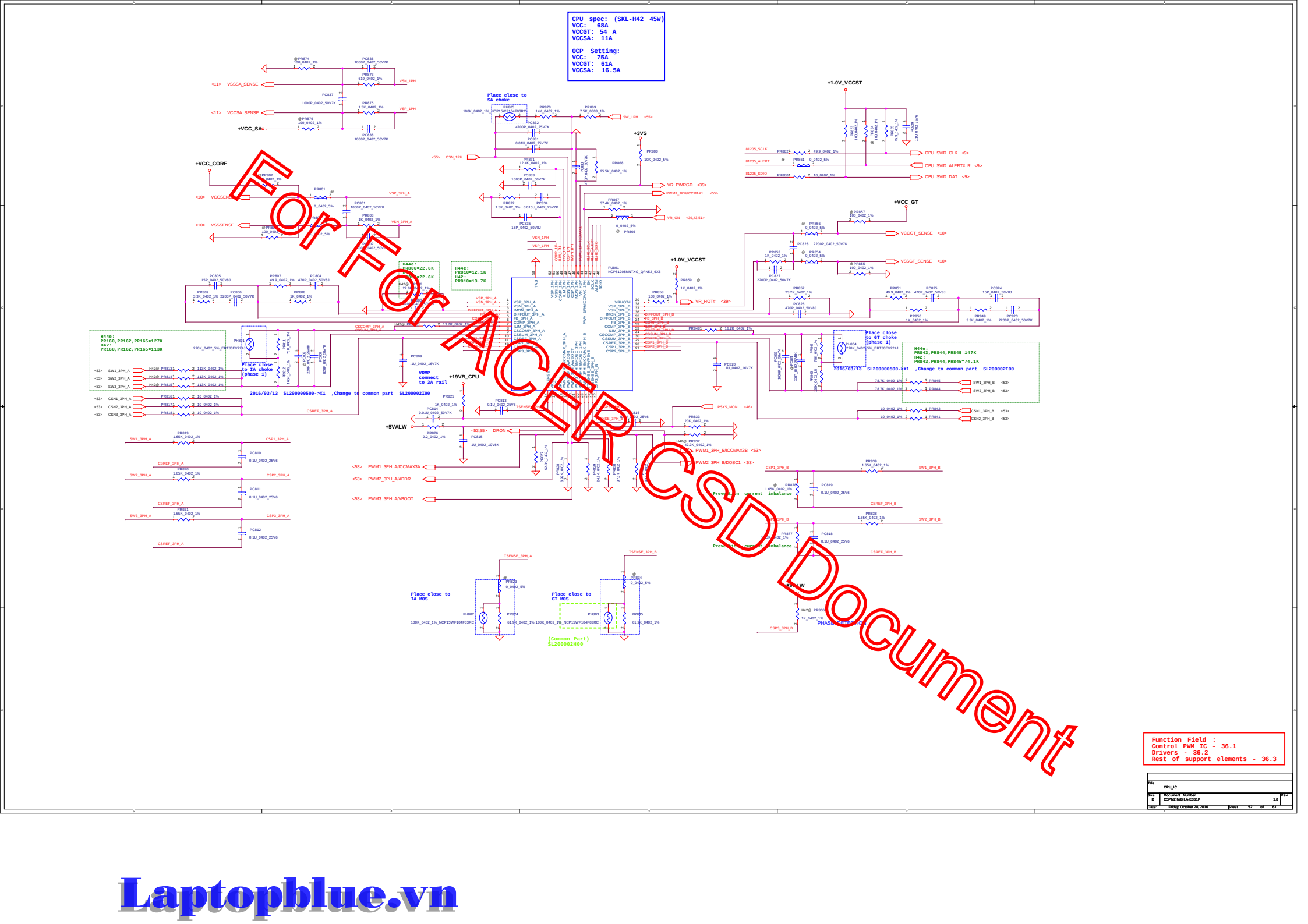
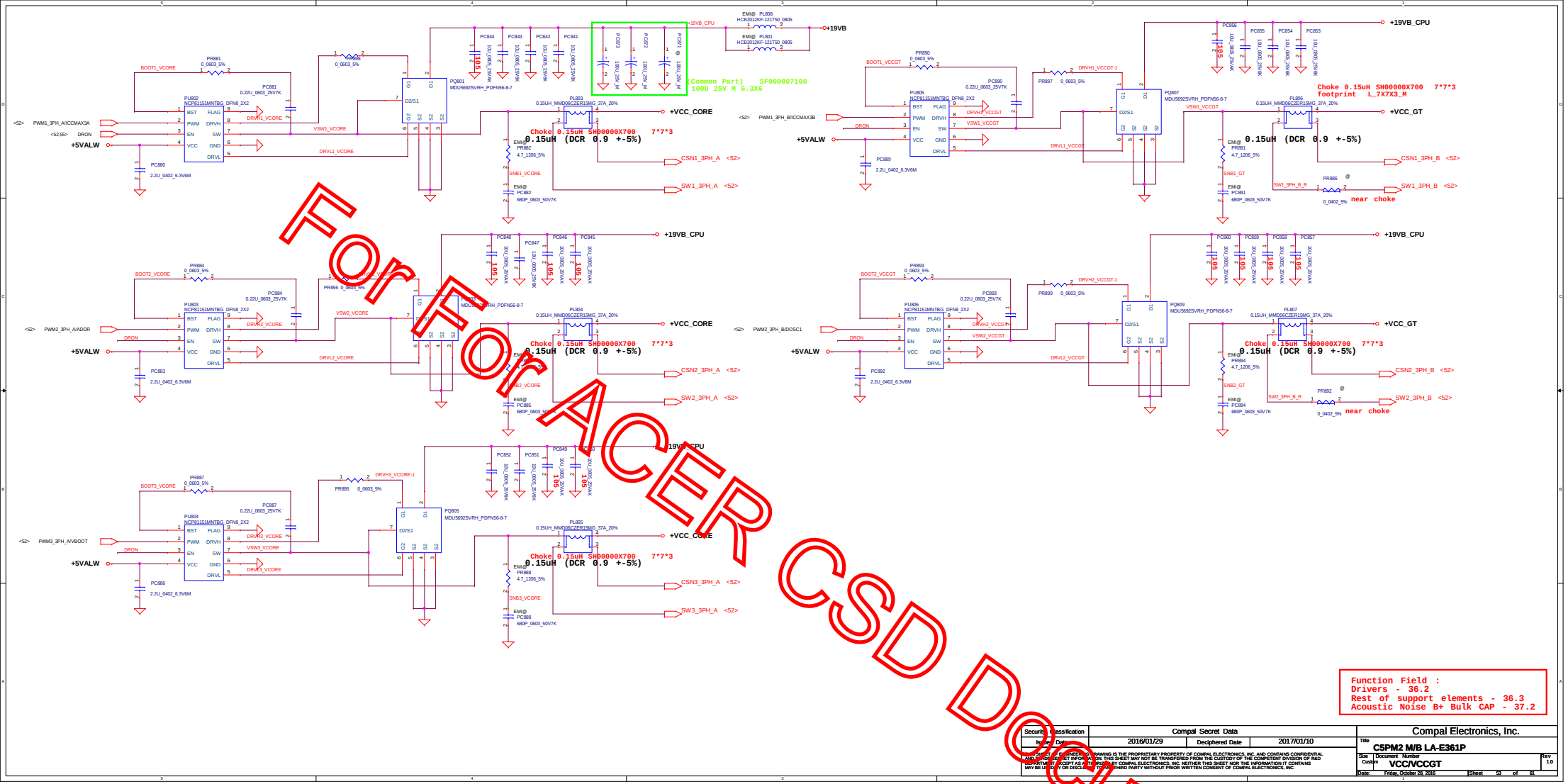
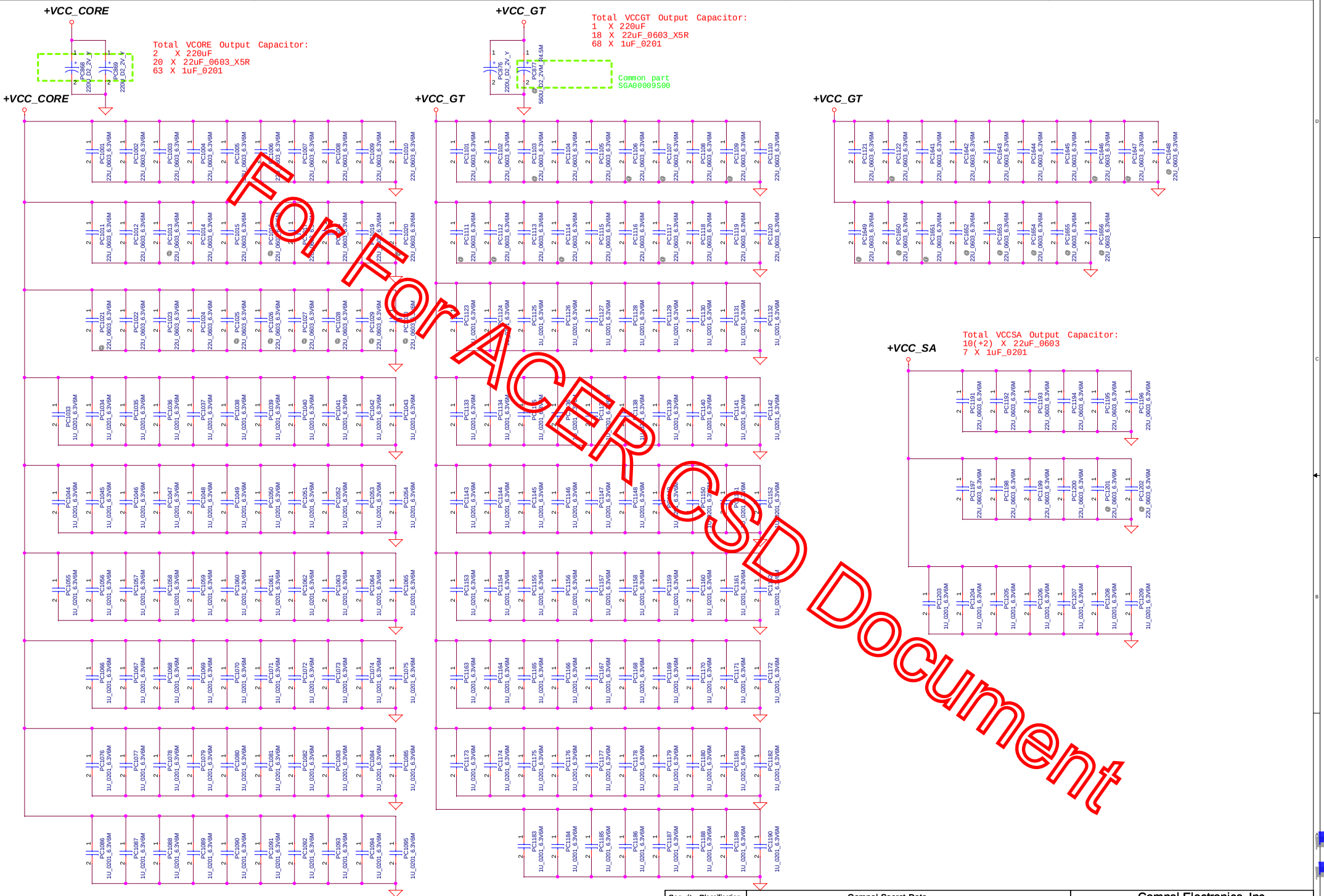

CPU spec: (SKL-H42 45W)
VCC: 68A
VCCGT: 54 A
VCCSA: 11A
OCP Setting:
VCC: 75A
VCCGT: 61A
VCCSA: 16.5A
+VCC_CORE
+VCC_SA
+1.0V_VCCST
+VCC_GT
+3VS
+19VB_CPU
+5VALW
+1.0V_VCCST
Place close to SA choke
Place close to IA choke (phase 1)
Place close to GT choke (phase 1)
Place close to IA MOS
Place close to GT MOS
VRMP connect to 3A rail
2016/03/13 SL20000500->X1 ,Change to common part SL20002I00
H44e: PR160,PR162,PR165=113K
H42: PR160,PR162,PR165=127K
H44e: PR806=22.6K
H42: PR806=22.6K
H44e: PR810=12.1K
H42: PR810=13.7K
H44e: PR843,PR844,PR845=147K
H42: PR843,PR844,PR845=74.1K
Prevent from current imbalance
(Common Part) SL20002H00
Function Field :
Control PWM IC - 36.1
Drivers - 36.2
Rest of support elements - 36.3
FOR TACER CSD Document
Laptopblue.vn



Function Field :
Drivers - 36.2
Rest of support elements - 36.3
Acoustic Noise B+ Bulk CAP - 37.2

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/01/29	Deciphered Date 2017/01/10	Title: C5PM2 M/B LA-E361P
			Size: Custom; Document Number: VCC/VCCGT; Rev: 1.0
			Date: Friday, October 28, 2016; Sheet 53 of 61



Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: C5PM2 M/B LA-E361P

Size: Custom | Document Number: CPU CAP | Rev: 1.0

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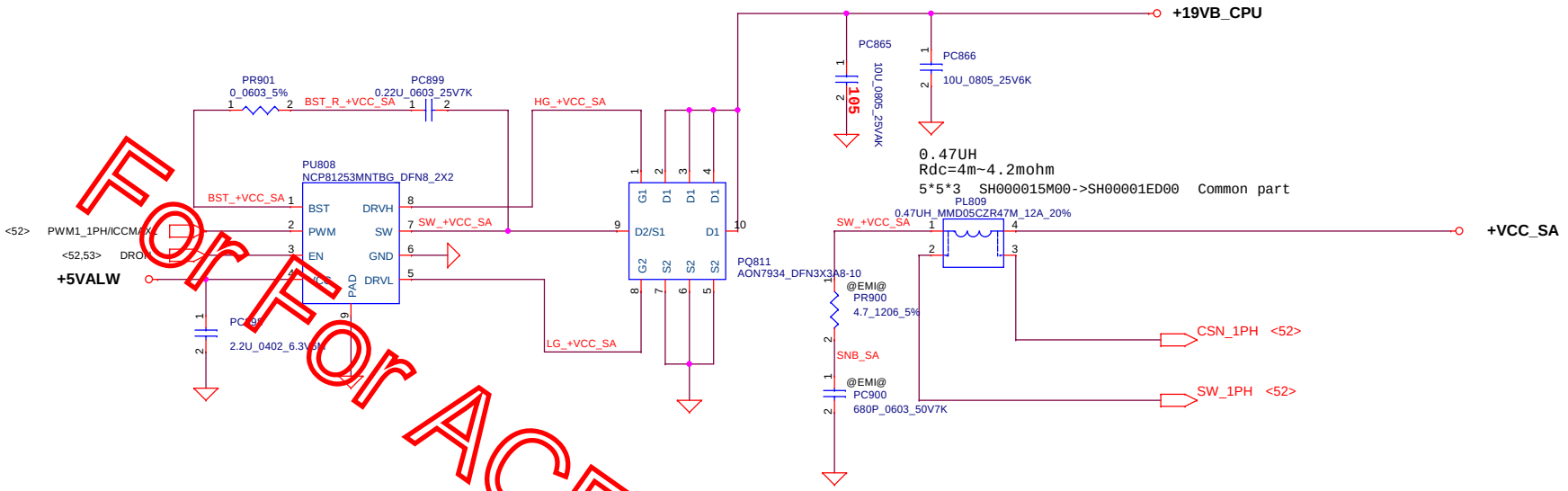


Function Field :
Drivers - 36.2
Rest of support elements - 36.3

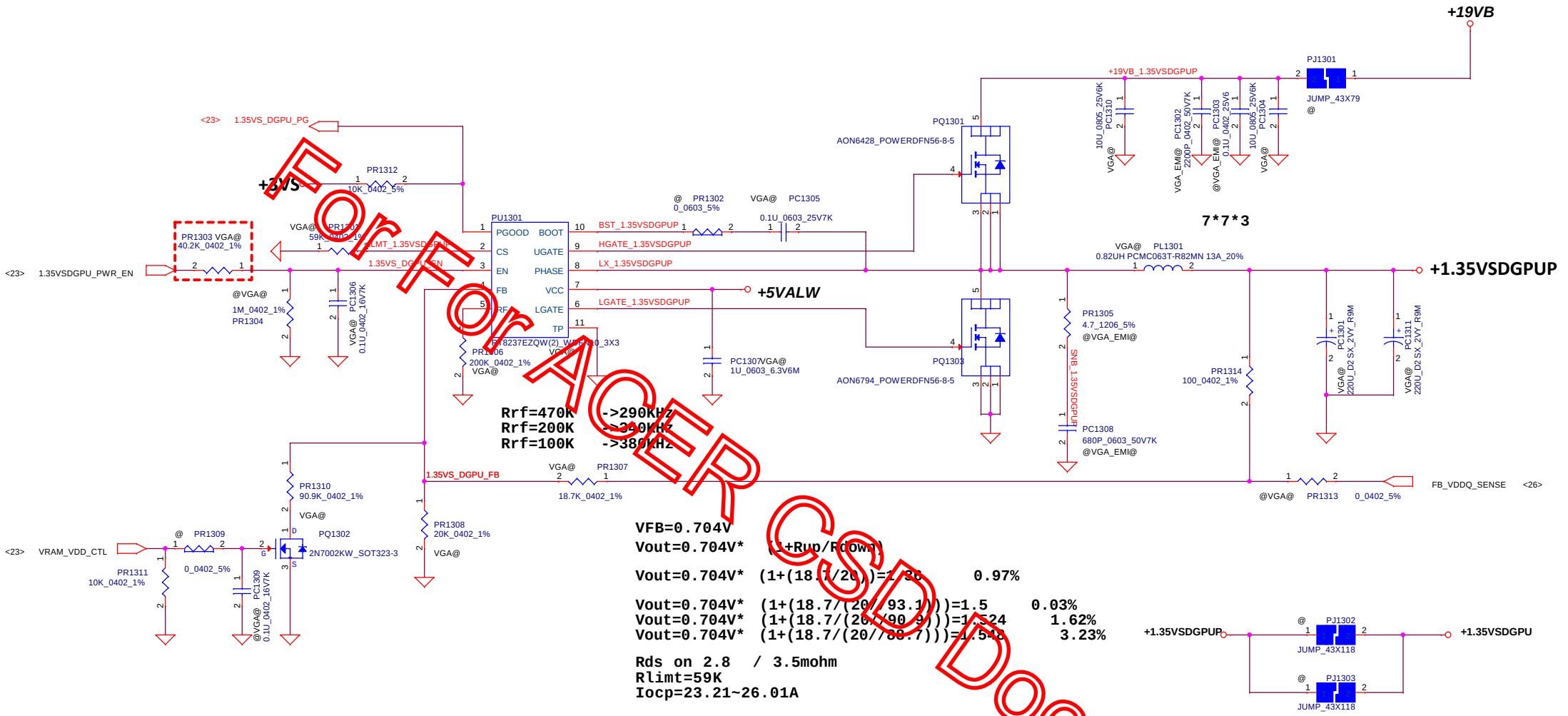
Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: C5PM2 M/B LA-E361P

Size: Custom | Document Number: VCCSA | Rev: 1.0

Date: Friday, October 28, 2016 | Sheet 55 of 61



Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: VRAM

Size	Document Number	Rev
A3	C5PM2 M/B LA-E361P	1.0

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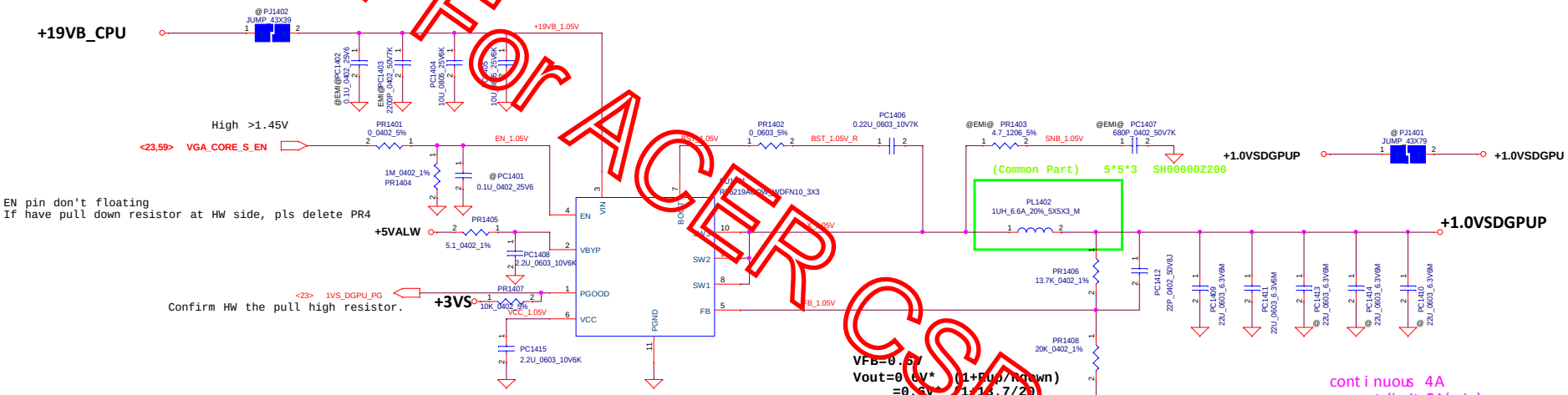
Function Field :
PWR.Plane.Regulator_1.05VDGPU - 43.7
Rest of support elements - 43.8



Switching frequency is 500KHz.

PR7(Rup) + PR8(Rdown) < 8Kohm, if you project has output voltage leakage concern when EN is low.

Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: 1.05VSDGPU

Size	Document Number	Rev
C	C5PM2 M/B LA-E361P	1.0

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Module model information

NCP81278_NVVDD_V1A.mdd for IC portion.
NCP81278_NVVDD_V1B.mdd for SW portion.

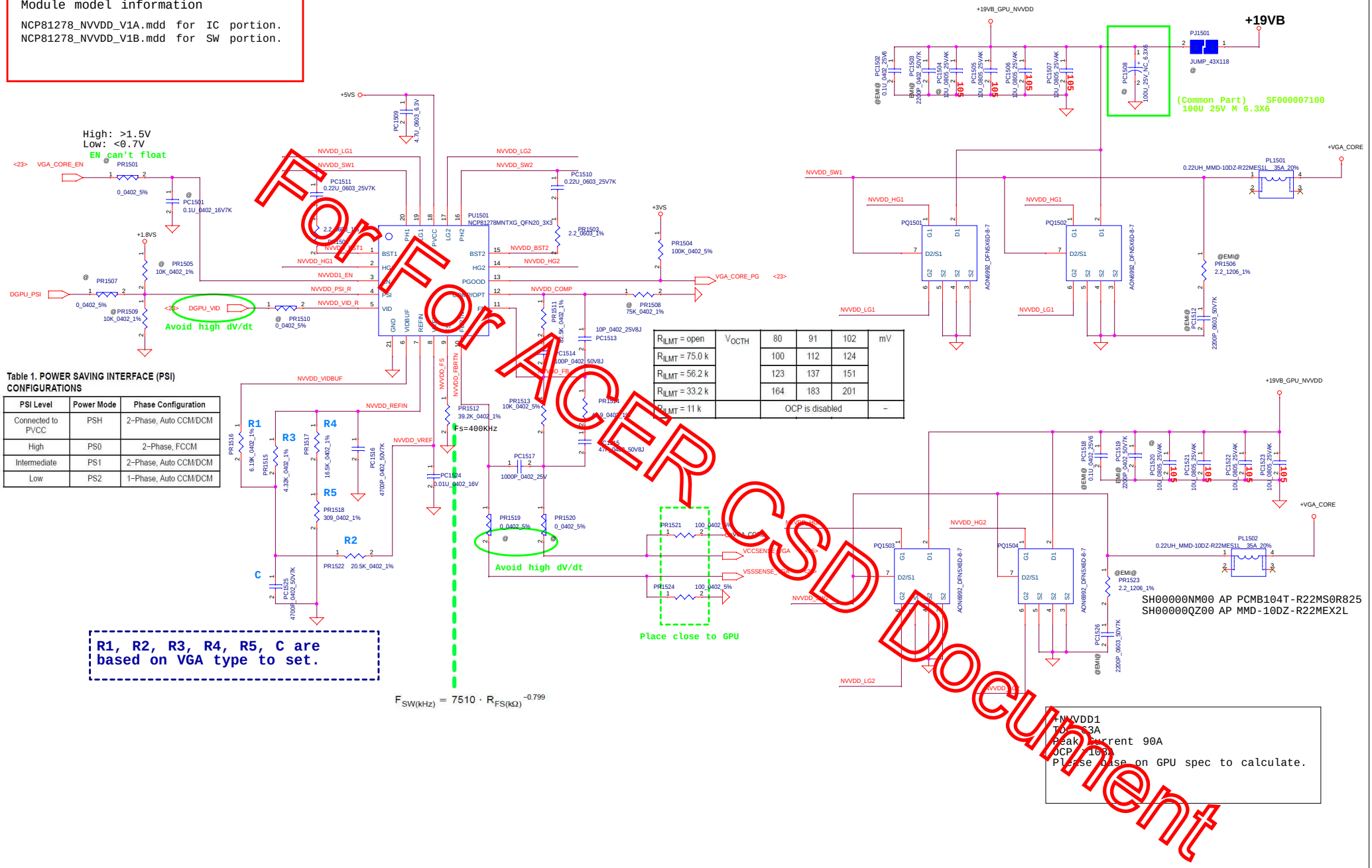


Table 1. POWER SAVING INTERFACE (PSI) CONFIGURATIONS

PSI Level	Power Mode	Phase Configuration
Connected to PVCC	PSH	2-Phase, Auto CCM/DCM
High	PS0	2-Phase, FCCM
Intermediate	PS1	2-Phase, Auto CCM/DCM
Low	PS2	1-Phase, Auto CCM/DCM

R_{ILMT} = open	V_{OCTH}	80	91	102	mV
R_{ILMT} = 75.0 k		100	112	124	
R_{ILMT} = 56.2 k		123	137	151	
R_{ILMT} = 33.2 k		164	183	201	
R_{ILMT} = 11 k		OCP is disabled			-

$$F_{SW(kHz)} = 7510 \cdot R_{FS(k\Omega)}^{-0.799}$$

Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.

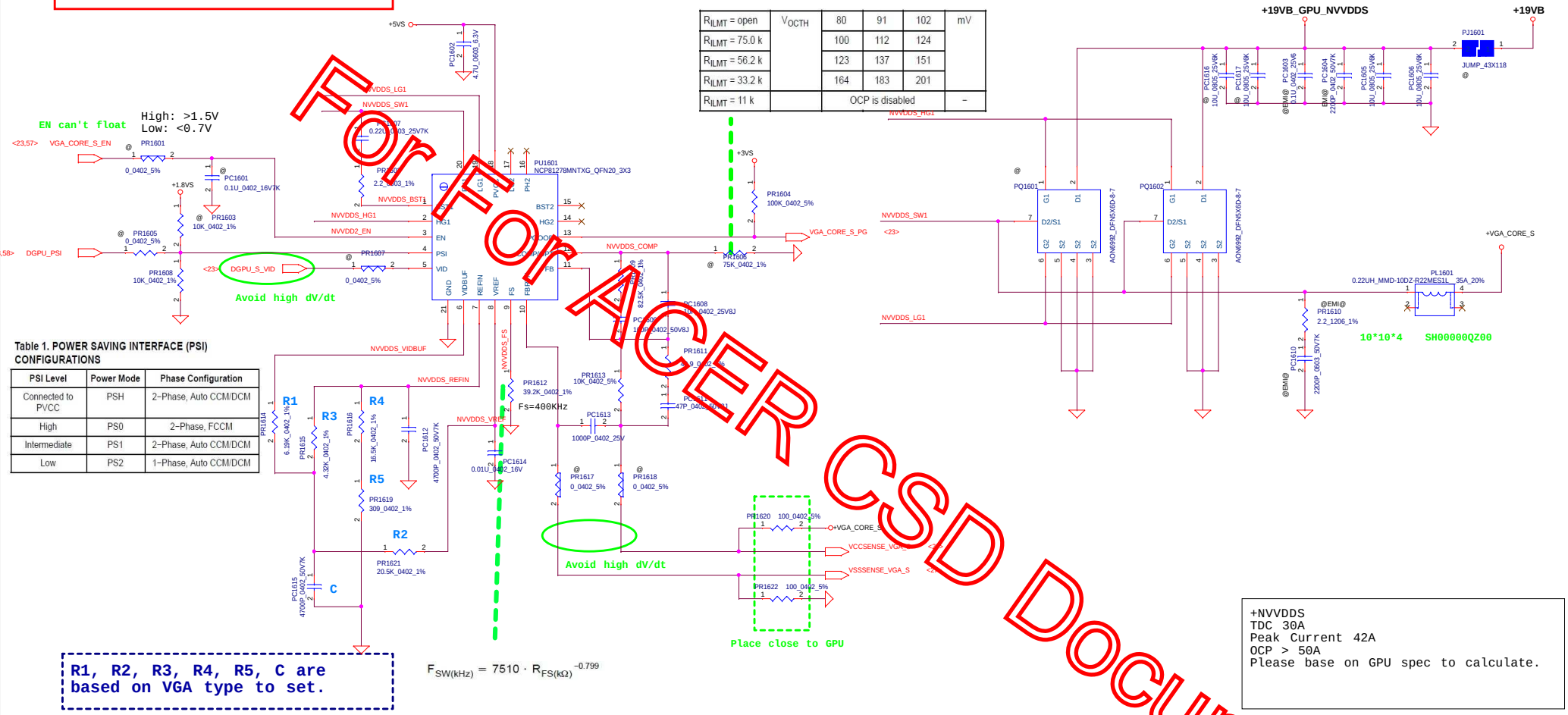
Title: VGA_CORE

Size | Document Number: C5PM2 M/B LA-E361P | Rev: 1.0

Date: Friday, October 28, 2016 | Sheet 58 of 61

Module model information

NCP81278_NVVDDS_V1A.mdd for IC portion.
NCP81278_NVVDDS_V1B.mdd for SW portion.



R_{ILMT} = open	V_{OCTH}	80	91	102	mV
R_{ILMT} = 75.0 k		100	112	124	
R_{ILMT} = 56.2 k		123	137	151	
R_{ILMT} = 33.2 k		164	183	201	
R_{ILMT} = 11 k		OCP is disabled			-

Table 1. POWER SAVING INTERFACE (PSI) CONFIGURATIONS

PSI Level	Power Mode	Phase Configuration
Connected to PVCC	PSH	2-Phase, Auto CCM/DCM
High	PS0	2-Phase, FCCM
Intermediate	PS1	2-Phase, Auto CCM/DCM
Low	PS2	1-Phase, Auto CCM/DCM

+NVVDDS
TDC 30A
Peak Current 42A
OCP > 50A
Please base on GPU spec to calculate.

Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: VGA_CORE_S

Size | Document Number: C5PM2 M/B LA-E361P | Rev: 1.0

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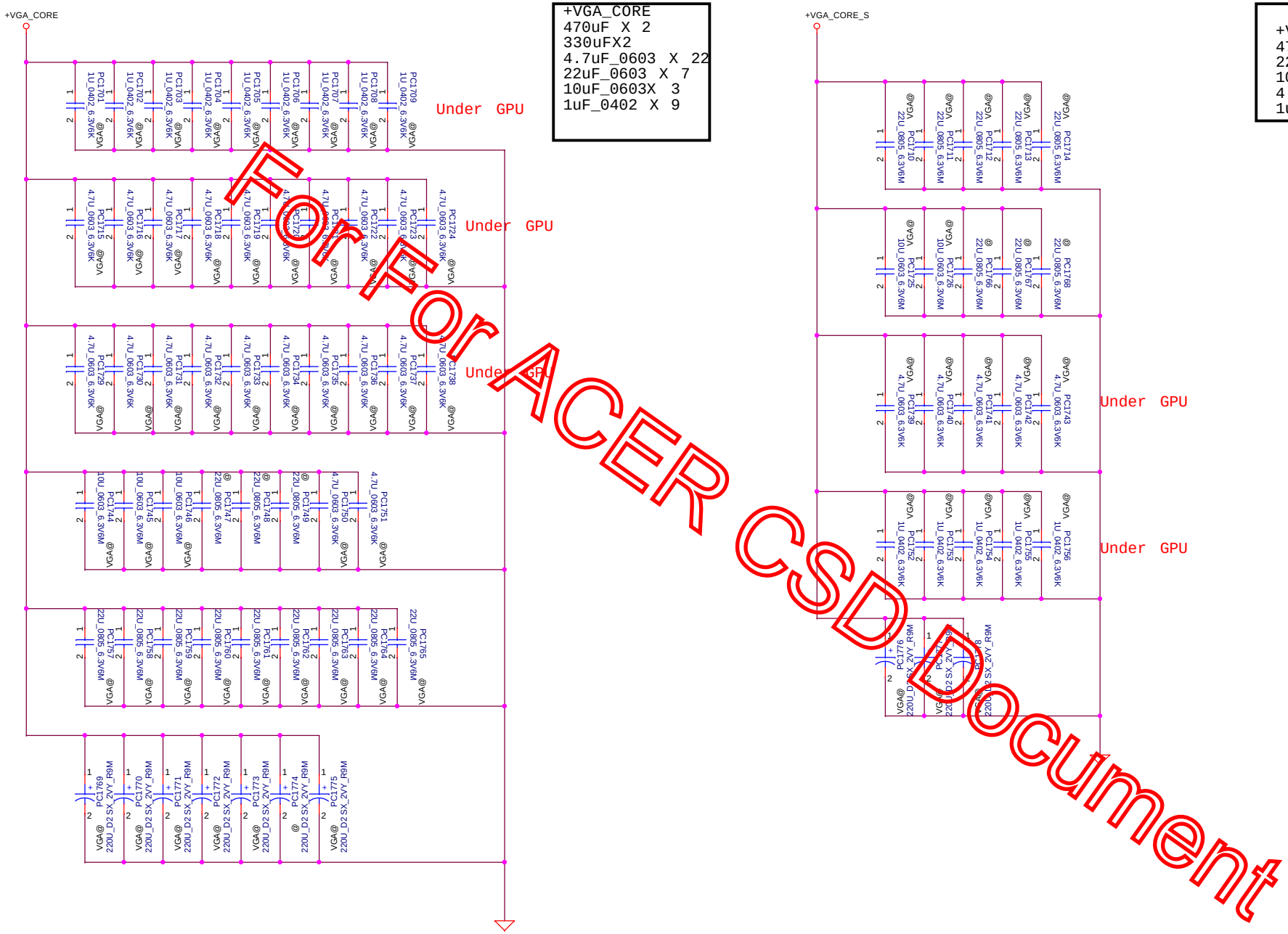

Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: VGA DECOUPLING

Size | Document Number: C5PM2 M/B LA-E361P | Rev: 1.0

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01		SPEC current down so change IC	0.1	P50	change: PC7108 SE00000M000 -> SE107475K80 S CER CAP 4.7U 6.3V K X5R 0603 PC7109 SE071680J80 -> SE075103K80 S CER CAP .01U 25V K X7R 0402 PC7202 SE000006880 -> SE042104K80 S CER CAP 1U 25V K X7R 0603 PC7207 SE000006880 -> SE074222K80 S CER CAP 2200P 50V K X7R 0402 PC7208 SE00000X200 -> SE00000QK00 S CER CAP 10U 25V K X5R 0805 H1.25 PR7115 SD034324280 -> SD034215280 S RES 1/16W 32.4K +-1% 0402 PR7118 SD028470280 -> SD028100480 S RES 1/16W 47K +-5% 0402 PR7201 SD034100480 -> SD028100480 S RES 1/16W 1M +-5% 0402 PR7202 SD000001J80 -> SD013000080 S RES 1/10W 0 +-5% 0603 PR7208 SD028000080 -> SD028100180 S RES 1/16W 1K +-5% 0402 PU7102 SA000007QP00 -> SA00001HW80 S IC G971AB2F11U SO 8P PU7201 SA000085D00 -> SA00001400 S IC SY8288RAC QFN 20P PWM Del: PC7111 SE00000M000 S CER CAP 22U 6.3V M X5R 0603 PL7102 SH00000Y600 S COIL 1UH +-30% 2.8A 4X4X2 FERRITE PR7109 SD028000080 S RES 1/16W 0 +-5% 0402 PR7112 SD028100380 S RES 1/16W 100K +-5% 0402 PR7204 SD028000080 S RES 1/16W 0 +-5% 0402 PR7205 SD034200280 S RES 1/16W 20K +-1% 0402 PR7206 SD034200280 S RES 1/16W 20K +-1% 0402 Add: PC7201 SE000006880 S CER CAP 0.1U 25V K X5R 0402 PC7203 SE025681K80 S CER CAP 680P 50V K X7R 0603 PC7210 SE00000K80 S CER CAP 1U 6.3V K X5R 0402 PC7211 SE00000M000 S CER CAP 22U 6.3V M X5R 0603 PC7212 SE00000M000 S CER CAP 22U 6.3V M X5R 0603 PC7218 SE000008880 S CER CAP 2.2U 6.3V M X5R 0402 PR7211 SD034100080 S RES 1/16W 100 +-1% 0402 PR7212 SD034100A80 S RES 1/16W 10 +-1% 0402 PR7215 SD034205280 S RES 1/16W 20.5K +-1% 0402 PR7216 SD034100080 S RES 1/16W 100 +-1% 0402 PR7218 SD034120280 S RES 1/16W 12K +-1% 0402	0727	EVT
		change common part.	0.1	P47 P58	change: PL1501 SH00001EA00 -> SH00000QZ00 S COIL 22UH +-20% MMD-10DZ-R22MES1L 35A PL1502 SH00001EA00 -> SH00000QZ00 S COIL 22UH +-20% MMD-10DZ-R22MES1L 35A PL1601 SH00001EA00 -> SH00000QZ00 S COIL 22UH +-20% MMD-10DZ-R22MES1L 35A PL404 SH000016800 -> SH000016700 S COIL 1.5UH +-20% 9A 7X7X3 MOLDING	0727	EVT
		CPU Transient Test improve.	0.1	P52 P54	PR844 SD034750280-> SD034787280 S RES 1/16W 78.7K +-1% 0402 PR845 SD034750280-> SD034787280 S RES 1/16W 78.7K +-1% 0402 PR852 SD034226280-> SD034232280 S RES 1/16W 23.2K +-1% 0402 PR867 SD034348280-> SD034374280 S RES 1/16W 37.4K +-1% 0402 PR868 SD000003580-> SD034255280 S RES 1/16W 25.5K +-1% 0402 PR871 SD034137280-> SD00000A180 S RES 1/16W 12.4K +-1% 0402 PR875 SD034100180-> SD034150180 S RES 1/16W 1.5K +-1% 0402 PC807 SE074102K80-> SE00003W00 S CER CAP 820P 50V K X7R 0402 PC809 SE074103K80-> SE074104K80 S CER CAP 0.1U 50V K X7R 0402 PC820 SE074103K80-> SE074104K80 S CER CAP 0.1U 50V K X7R 0402 PC868 SGA20331E10-> SGA20221D40 S POLY C 330U 2V Y D2 LESR9M EEFSX H1.9 PC876 SGA20331E10-> SGA20221D40 S POLY C 220U 2V Y D2 SX LESR9M H1.9 PL809 SH000015M00-> SH00001ED00 S COIL 47UH 20% MMD-05CZ-R47MEV1L 12.2A PQ801 PQ803 PQ805 PQ807 PQ809 SB000017L00-> SB000017400 S TR MDU5692SVRH 2N DUAL PDFN56-8 Del: PC1013 PC1016 PC1020 PC1021 PC1025 PC1026 PC1027 PC1028 PC1029 PC1030 PC1103 PC1106 PC1107 PC1109 PC1111 PC1112 PC1114 PC1117 PC1122 PC1646 PC1647 PC1649 PC1651 SE00000M000 S CER CAP 22U 6.3V M X5R 0603 Add: PC869 SGA20221D40 S POLY C 220U 2V Y D2 SX LESR9M H1.9	0727	EVT
		VRAM 1.05VSDGPU Transient Test improve.	0.1	P56 P57	change: PC1301SF000004J00 SGA20221D40 S POLY C 220U 2V Y D2 SX LESR9M H1.9 PR1306 SD034470380 SD034200380 S RES 1/16W 200K +-1% 0402 Del: PC1410 SE00000M000 S CER CAP 22U 6.3V M X5R 0603 PC1413 SE00000M000 S CER CAP 22U 6.3V M X5R 0603 PC1[illegible] SE00000M000 S CER CAP 22U 6.3V M X5R 0603 Add: PC1411 SGA20221D40 S POLY C 220U 2V Y D2 SX LESR9M H1.9	0727	EVT
		VGA Transient Test improve & SPEC CURRENT down.	0.1	P59 P60	Del: PQ1601 SB000017J00 S MOS AON6992 2N DFN5X6D PR1603 SD034100280 S RES 1/16W 10K +-1% 0402 PR1605 SD034750280 S RES 1/16W 75K +-1% 0402 PC1609 SE000007100 S E-CAP CAP 100U 25V M 6.3X6 PC1616 SE00000QK00 S CER CAP 10U 25V K X5R 0805 H0.85 PC1617 SE00000QK00 S CER CAP 10U 25V K X5R 0805 H0.85 Add: PC1769 PC1770 PC1773 PC1775 PC1776 PC1778 SGA20221D40 S POLY C 220U 2V Y D2 SX LESR9M H1.9 PR1608 SD034100280 S RES 1/16W 10K +-1% 0402	0727	EVT
		EMI request	0.1		Add: PC323 PC518 PC882 PC885 PC887 PC888 PC891 PC894 SE025681K80 S CER CAP 680P 50V K X7R 0603 PL302 PL303 PL501 PL801 PL808 SM01000P200 S SUPPRE TAI-TECH SMD2012KF200150 0402 PR319 PR504 PR7203 PR882 PR885 PR888 PR891 PR894 SD001470880 S RES 1/4W 4.7 +-5% 1206		
		CPU NVVDD NVVDDS input Cap 85度->105度 0ohm-->R-SHORT Add thermal PH2 PH3 EMI request	0.2		PU301_SA00008OM00_BQ24780S -> SA0000A6B00_BQ24701 PC809 PC820 SE074104K80_0.1uF_0402_50V -> SE076104K80_0.1uF_0402_16V	09/14	DVT
		Remove thermal PH2 Setting PH1 95度P H3 85度	0.2		Del: PH202_100K_0402_NTC_SL200002H00 PR214_21.5K_0402_SD034215280 PR216_10K_0402_SD034100280 change: PQ201_BSS138LT1G_SB00000QO00 -> L8SS139LT1G_SB00001GD00 PR204_18.7K_0402_SD034187280 -->15.4K_0402_SD034154280 PR218_10K_0402_SD034100280 -->14K_0402_SD034140280 PR215_21.5K_0402_SD034215280 -->26.7K_SD034267280	09/23	DVT

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