Compal Confidential

EH78F MB Schematic Document

LA-G161P

Rev:1C

2019.01.16

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Title: Cover Sheet			
Size: Custom	Document Number: EH78F M/B LA-G161PR01		Rev: 0.1
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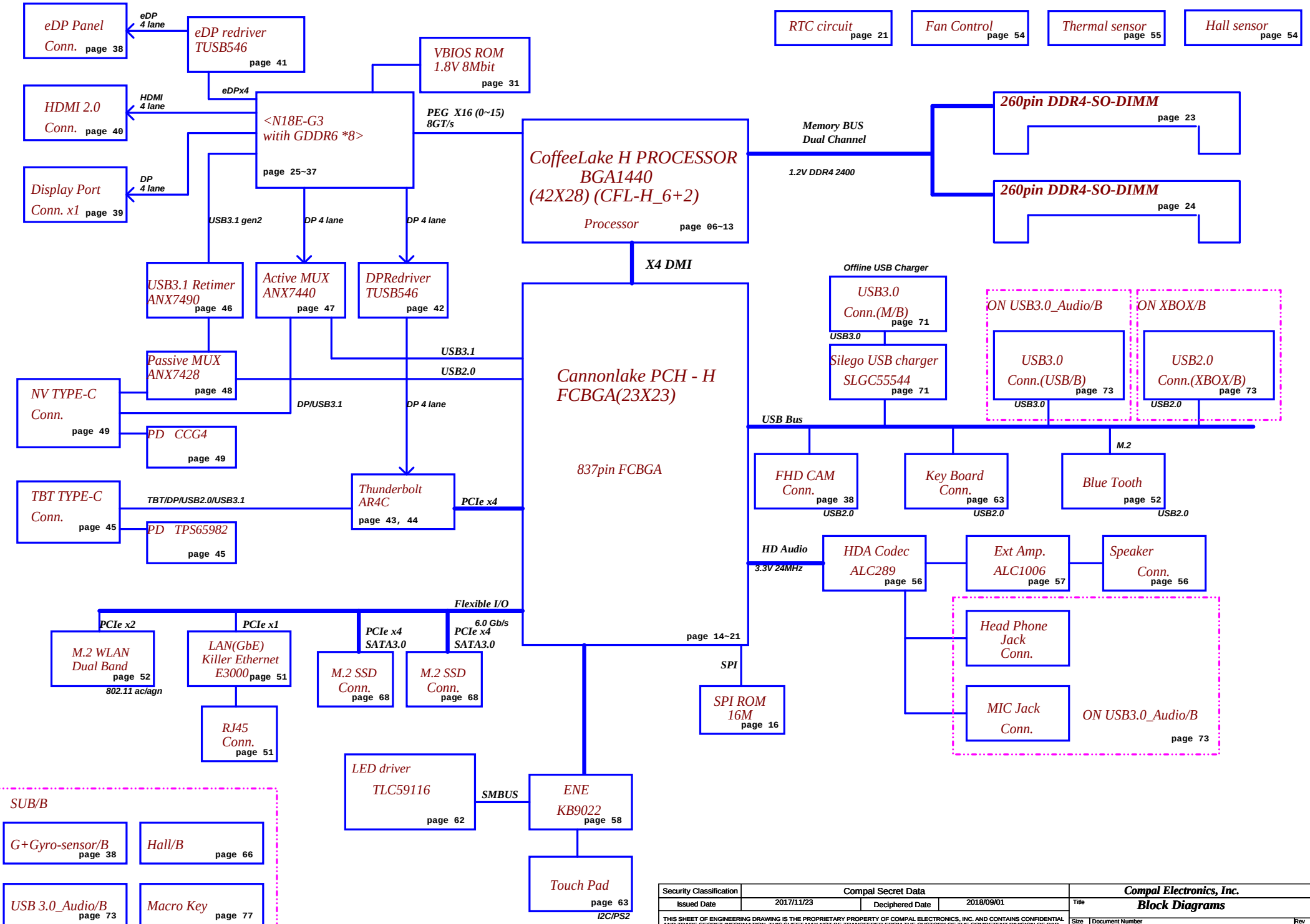

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Title	Block Diagrams		
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Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	V_{BID} min	V_{BID} typ	V_{BID} max	EC AD
0	0		0.000 V	0.300 V	0x00 - 0x13
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x14 - 0x1E
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1F - 0x25
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x26 - 0x30
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3A
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B - 0x45
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 - 0x54
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64
8	75K +/- 1%	1.398 V	1.414 V	1.430 V	0x65 - 0x76
9	100K +/- 1%	1.634 V	1.650 V	1.667 V	0x77 - 0x87
10	130K +/- 1%	1.849 V	1.865 V	1.881 V	0x88 - 0x96
11	160K +/- 1%	2.015 V	2.031 V	2.046 V	0x97 - 0xA4
12	200K +/- 1%	2.185 V	2.200 V	2.215 V	0xA5 - 0xAF
13	240K +/- 1%	2.316 V	2.329 V	2.343 V	0xB0 - 0xB7
14	270K +/- 1%	2.395 V	2.408 V	2.421 V	0xB8 - 0xBF
15	330K +/- 1%	2.521 V	2.533 V	2.544 V	0xC0 - 0xC9
16	430K +/- 1%	2.667 V	2.677 V	2.687 V	0xCA - 0xD4
17	560K +/- 1%	2.791 V	2.800 V	2.808 V	0xD5 - 0xDD
18	750K +/- 1%	2.905 V	2.912 V	2.919 V	0xDE - 0xF0
19	NC	3.000 V	3.000 V		0xF1 - 0xFF

I2C Address Table

BUS	Device	Address(7 bit)	Address(8bit) Write	Address(8bit) Read
I2C_0 (+3VS)	LIS2DH12TR (G-sensor)			
I2C_1 (+3VS)	TM-03461-001 (Touch Pad)			
PCH_SMBCLK (+3VALW)	DIMM1			
	DIMM2			
PCH_SML1CLK EC_SMB_CK2 (+3VALW)	N18E-G3 (VGA)	0x9E		
	TMS(NCT7718W)hot	0x98		
	TMS(W83L771AWG-2)cool	0x9A		
	LIS2DH12TR(M/B)			
	LIS2DH12TR(SUB/B)			
EC_SMB_CK1 (+3VLP)	ISL88739 (Charger IC)	0x11		
	BATTERY PACK	0x16		
EC_SMB_CK3 (+3VALW)	PD(TPS65982)	0x70		
	LED driver	0xC0		
EC_SMB_CK4 (+3VALW)				

BOM Structure Table

BOM Option Table	
Item	BOM Structure
Unpop	@
Connector	CONN@
HDMI royalty	45@
i5 CPU	I5@
i7 CPU	I7@
PCH	PCH@
CMC	CMC@
dGPU circuit	VGA@
OVRM-Onsemi	onsemi@
OVRM-Onsemi	upi@
FGC6	FGC6@
NON FGC6	NFGC6@
Intel CNVi (reserve)	CNVI@
USB charger	CHG@
GSYNC	GSYNC@
NON GSYNC	NGSYNC@
Thunderbolt	TBT@
Thermal sensor	TMS@
for SW debug board	UART@
EMI/ESD requirement	EMC@
EMI/ESD require reserve	XEMC@
DIS sequency control	NGPK@
M/B GSENSOR	MBGSEN@
GSENSOR ISH path	ISHGSEN@
GSENSOR EC path	ECGSEN@

Power State

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Voltage Rails

Power Plane	Description	S0	S3	S4	S5
+RTCVCC	RTC Battery Power	ON	ON	ON	ON
+19V_VIN	Adapter power supply	N/A	N/A	N/A	N/A
+12.6V_BATT	Battery power supply	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A	N/A
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON
+5VALW	+5V Always power rail	ON	ON	ON	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON
+3VALW_PCH_PRIM	+3VALW power for PCH power rails	ON	ON	ON	ON*
+3VALW_SPI	+3VALW_PRIM supply for the SPI IO	ON	ON	ON	ON
+1.05VALW	+1.05V Always power rail	ON	ON	ON	ON
+1.2V_VDDQ	DDR4 +1.2V power rail	ON	ON	OFF	OFF
+1.05V_VCCST	Sustain voltage for processor in Standby modes	ON	ON	OFF	OFF
+5VS	System +5V power rail	ON	OFF	OFF	OFF
+3VS	System +3V power rail	ON	OFF	OFF	OFF
+1.05VS_VCCSTG	+1.05VALW_PRIM Gated version of VCCST	ON	OFF	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator .	ON	OFF	OFF	OFF
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF	OFF
+VCCIO	CPU IO +0.95VS power rail	ON	OFF	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF	OFF
+1.8VSDGPU_AON	+1.8VS power rail for GPU(AON rails)	ON	OFF	OFF	OFF
+1.8VSDGPU_MAIN	+1.8VS power rail for GPU GC6	ON	OFF	OFF	OFF
+VGA_CORE	Core voltage for VGA (merge core & core_s)	ON	OFF	OFF	OFF
+1.35VSDGPU	+1.35VS power rail for GPU	ON	OFF	OFF	OFF
+1.0VSDGPU	+1.0VS power rail for GPU	ON	OFF	OFF	OFF
+1.8VALW	System +1.8VALW always on power rail	ON	ON	ON	ON*

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

43 level BOM table

43 Level	Description	BOM Structure
43	EH78F 1180	I7@/QNDQ@/CMC@/VGA@/NGPK@/CNVI@/CHG@/XBOX@/TBT@/EMC@

BOARD ID Table

Board ID	PCB Revision	Board ID	PCB Revision
0	0.1	10	
1	1.0	11	1.0 w/ EC gensor
2	1A	12	
3	1B	13	
4	1C	14	
5		15	
6		16	
7		17	
8		18	
9		19	

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Title: Notes List

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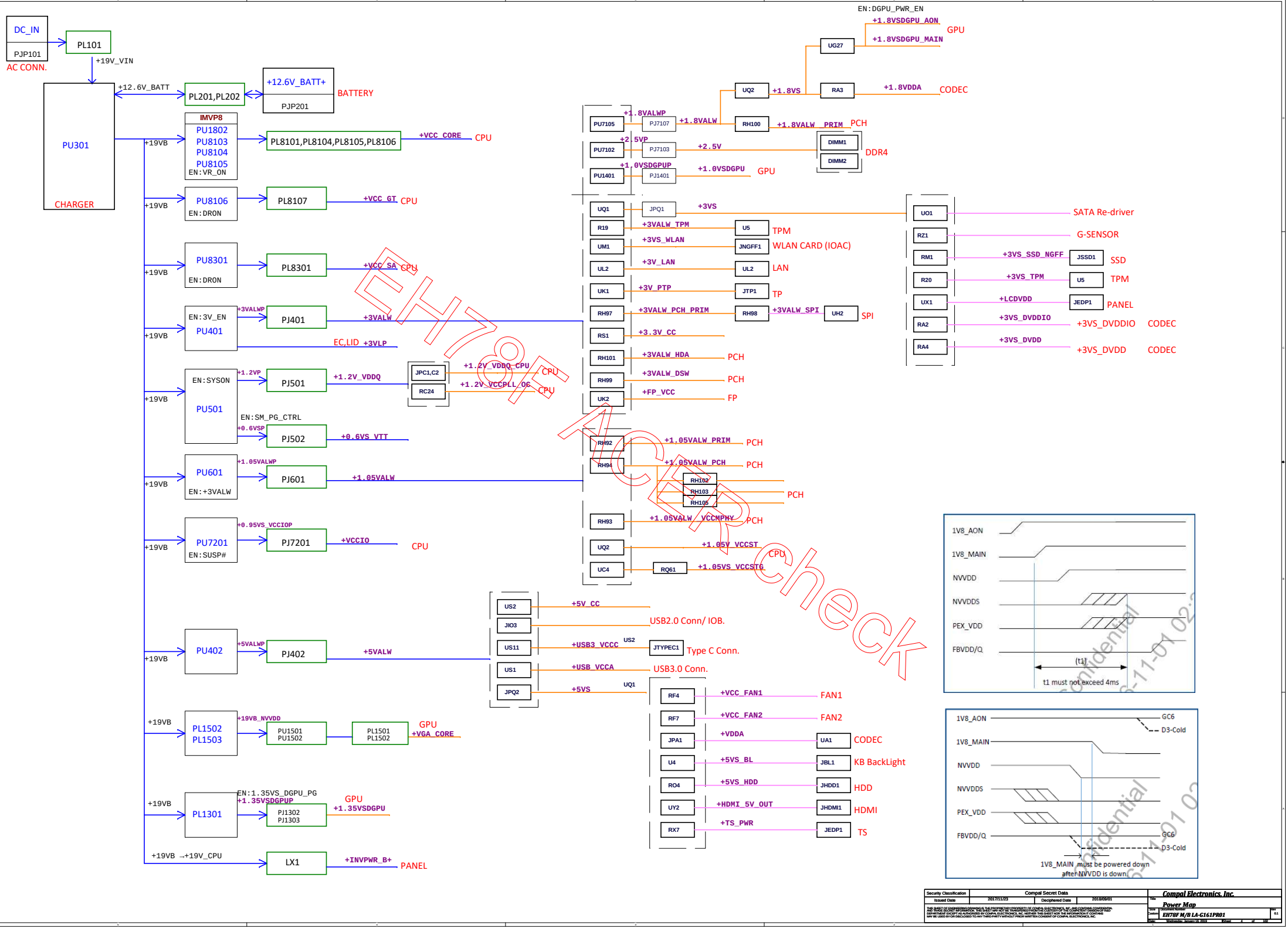

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Issued Date	2017/11/23	Deciphered Date	2018/09/01
			Power Map
			EH70F M/B LA-G161PR01

EH78F_EVT Power Sequence
BIOS : 0.05
EC : 0.05

AC mode

Plug in

EH78F ACES check

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Compal Electronics, Inc.

Title: Power Sequence

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PCB DAZ

ZZZ

PCB@ DAZ2HB00100

PCB EH78F LA-G161P LS-G161P/G162P/G163P/G164P/G165P/G168P

Coffee Lake-H CPU SKU

UC1

CFL-H_BGA1440

S IC CL8068403359524 SR3YY U0 2.2G ABO!

SA0000BPZ40

i7@

Cannon Lake PCH SKU

UH1

CFL-H_BGA1440

S IC FH82HM370 SR40B B0 BGA 874P PCH-H ABO!

SA0000BVP10

PCH@

NV N18E-G3

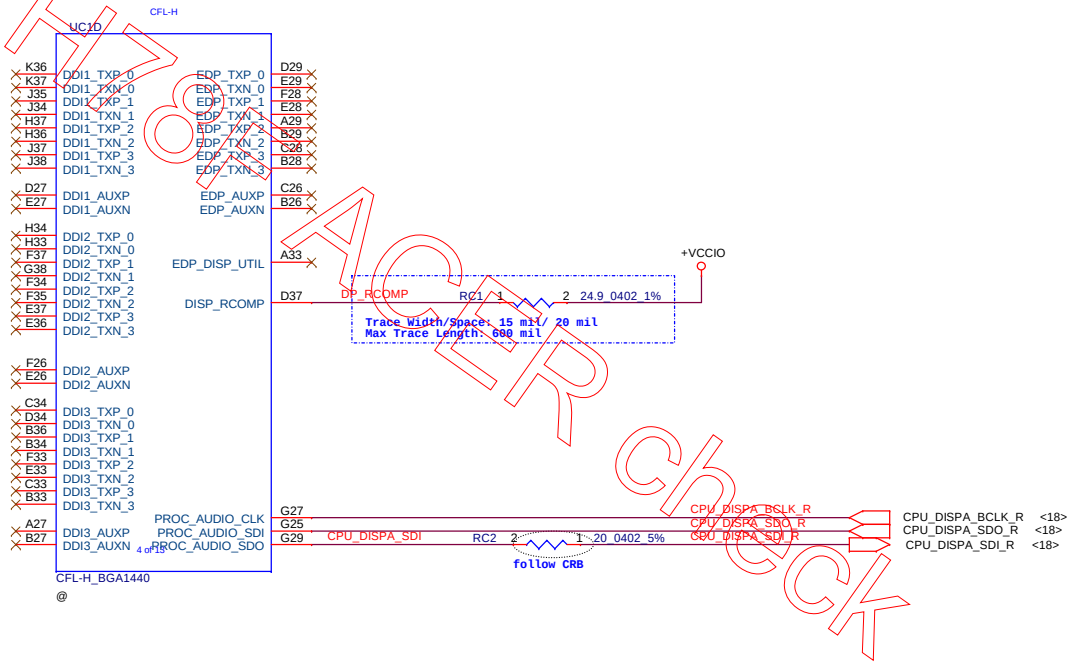
UG9

VGA@

S IC TU104-750-A1 FCBGA 2228 GPU ABO !

SA0000CD510

Need check USE QS PN



ETV acer check

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Title: CFL-H(1/8)DDI/eDP

Size: Custom | Document Number: EH78F M/B LA-G161PR01 | Rev: 0.1

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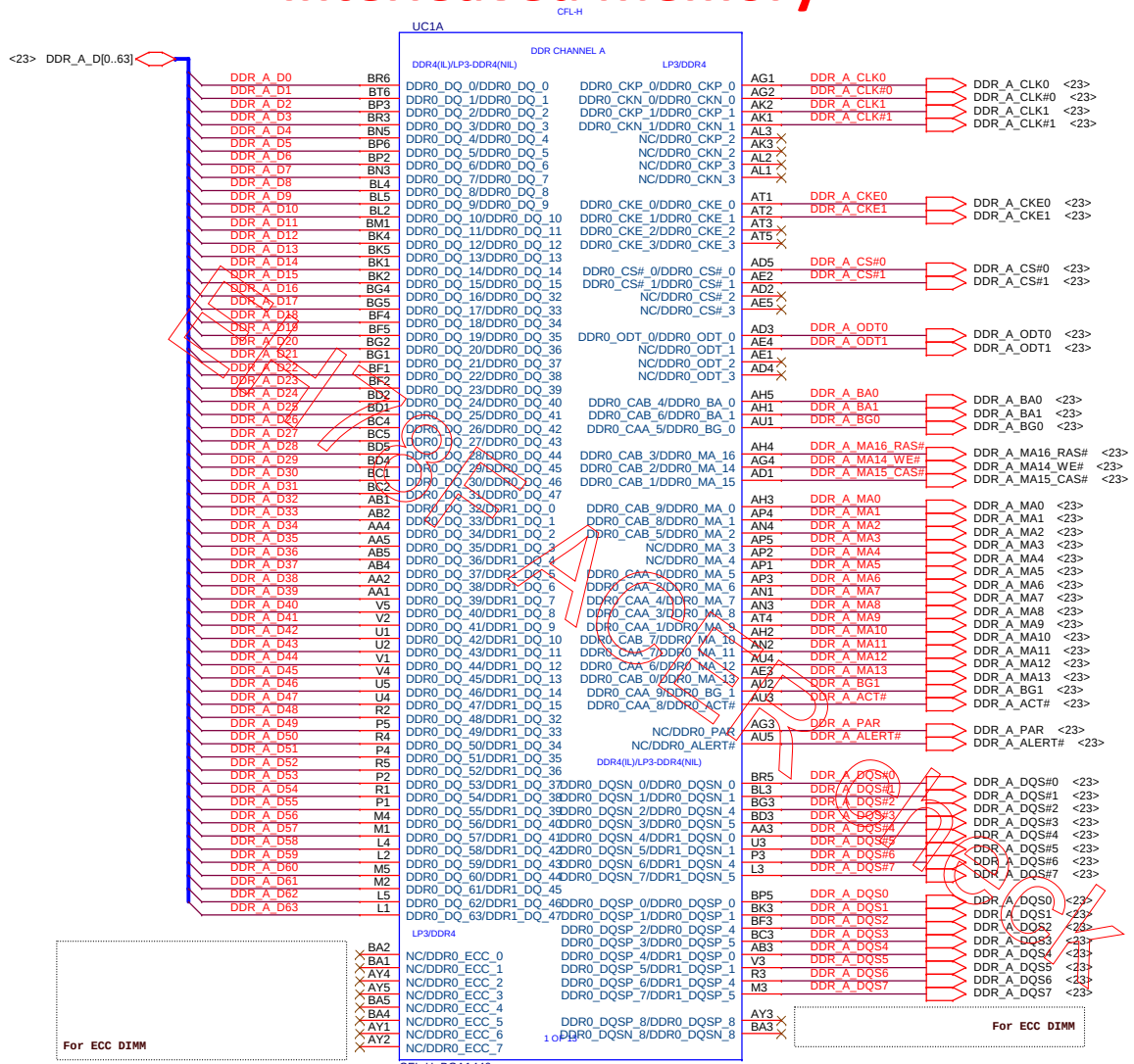
CHANNEL - A

Interleaved Memory



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Compal Electronics, Inc.

Title: CFL-H(2/8)DIMMA

Size: Custom | Document Number: EH78F M/B LA-G161PR01 | Rev: 0.1

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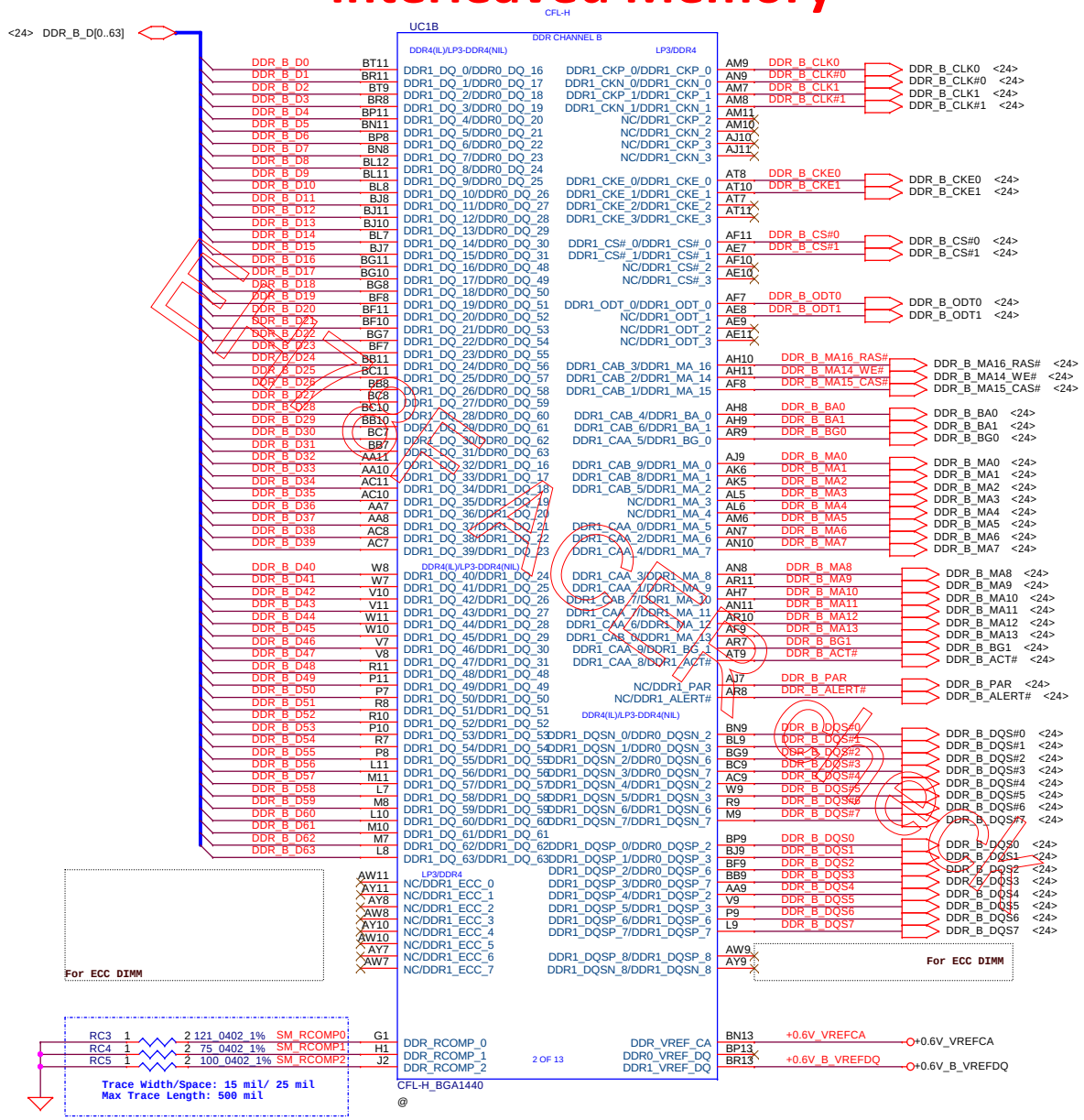
CHANNEL - B

Interleaved Memory



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Compal Electronics, Inc.

Title: CFL-H(3/8)DIMMB

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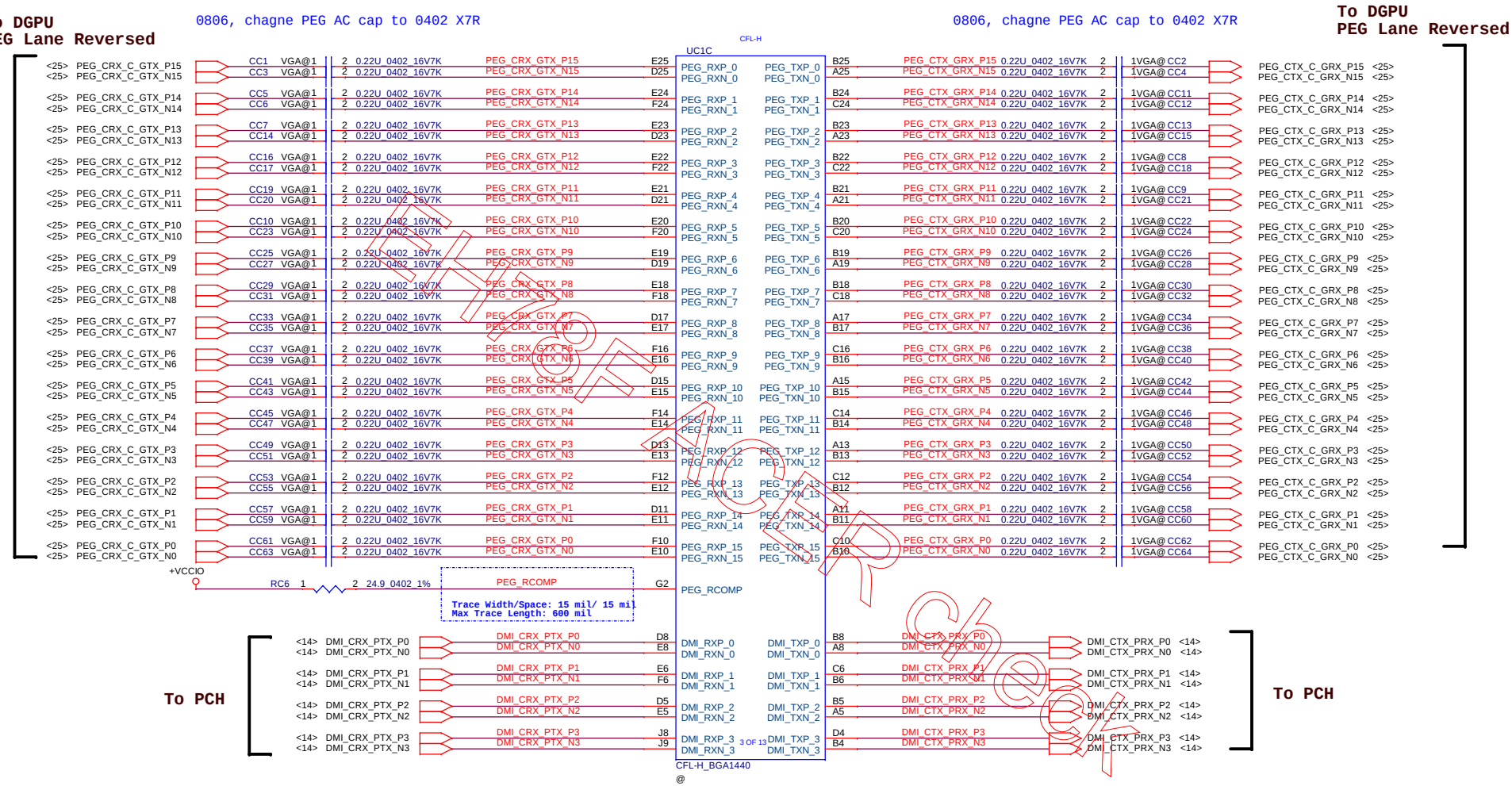
PEG&DMI



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571391_CFL_H_PDG_Rev0p5
1. The total Length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).
2. Route the Alert signal between the Clock and the Data signals.
3. Place those resistors close CPU side.

UC1E
CFL-H
5 OF 13
CFL-H_BGA1440

PCH_CPU_BCLK_P BCLKP
PCH_CPU_BCLK_N BCLKN
PCH_CPU_PCIBCLK_P PCI_BCLKP
PCH_CPU_PCIBCLK_N PCI_BCLKN
PCH_CPU_24M_CLK_P CLK24P
PCH_CPU_24M_CLK_N CLK24N
CPU_SVID_ALERT# VIDALERT#
CPU_SVID_CLK VIDSCK
CPU_SVID_DAT VIDSOUT
H_PROCHOT#_R PROCHOT#
DDR_PG_CTRL DDR_VTT_CNTL
EC_VCCST_PG VCCST_PWRGD
H_CPUPWRGD PROCPWRGD
H_PLTRST_CPU# RESET#
H_PM_SYNC_R PM_SYNC
H_PM_DOWN PM_DOWN
H_PECI PECI
H_THERMTRIP# THERMTRIP#
SKTOCC# SKTOCC#
PROC_SELECT# PROC_SELECT#
CATERR# CATERR#
ZVM#
MSM#
RSVD1
RSVD2
CFG_0 … CFG_19
BPM#_0 … BPM#_3
PROC_TDO
PROC_TDI
PROC_TMS
PROC_TCK
PROC_TRST#
PROC_PREQ#
PROC_PRDY#
CFG_RCOMP

Sensitive
Sensitive

CFG0 CFG2 CFG3 CFG4 CFG5 CFG6 CFG7 → TC22 TP@
RC7 RC8 RC9 RC10 RC11 RC12 1 K 0402 5%

The CFG signals have a default value of '1' if not terminated on the board.
disable eDP

CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted
* 1 = (Default) Normal Operation;
0 = Stall.

CFG[2]: PCI Express* Static x16 Lane Numbering Reversal.
1 = Normal operation
* 0 = Lane numbers reversed.

CFG[4]: eDP enable:
* 1 = Disabled.
0 = Enabled.

CFG[6:5]: PCI Express* Bifurcation:
00 = 1 x8, 2 x4 PCI Express*
01 = reserved
10 = 2 x8 PCI Express*
* 11 = 1 x16 PCI Express*

CFG[7]: PEG Training:
* 1 = (default) PEG Train immediately following RESET# de assertion.
0 = PEG Wait for BIOS for training.

*CFG Pin Use CMC debug on DDX03 R02 Schematic.

XDP_BPM#0 XDP_BPM#1 XDP_BPM#2 XDP_BPM#3 → TC1 TP@ TC2 TP@ TC3 TP@ TC4 TP@

CPU_XDP_TDO CPU_XDP_TDI CPU_XDP_TMS CPU_XDP_TCK0 CPU_XDP_TRST# XDP_PREQ# XDP_PRDY#
CPU_XDP_TDO <18>
CPU_XDP_TDI <18>
CPU_XDP_TMS <18>
CPU_XDP_TCK0 <18>
CPU_XDP_TRST# <21>
TC19 TP@ TC20 TP@
To be confirm

CFG_RCOMP 1 RC18 2 49.9 0402 1%
Trace Width/Space: 4 mil/ 12 mil
Max Trace Length: 600 mil

XDP_PREQ# <21>
XDP_PRDY# <21>

<18> H_CPUPWRGD
<17> H_PLTRST_CPU#
<17> H_PM_SYNC_R
<17,58> H_PECI
<17> PCH_THERMTRIP#_R
RC17 1 @ 2 0 0402 5%
TP@ TC5
TP@ TC6

PROC_SELECT#
should be unconnected on CFL processor
EDS1.2 8/21

XEMC@ .1U_0402_16V7K CC65 H_CPUPWRGD
EMC@ 1000P_0402_50V7K CC66 H_PROCHOT#_R
XEMC@ .1U_0402_16V7K CC67 H_THERMTRIP#
EMC@ 1000P_0402_50V7K CC68 EC_VCCST_PG

Near CPU side
follow 1050 Request
8/21

+1.05V_VCCST
RH1 1 2 1K_0402_5% H_THERMTRIP#

+1.2V_VDDQ
UC3
NC VCC A GND Y
74AUP1G07GW_TSSOP5
DDR_PG_CTRL
CC69 .1U_0402_16V7K
SM_PG_CTRL
+3VS
RC23 330K_0402_5%
SM_PG_CTRL <85>
PU 330K follow CRB
8/21

+1.05VS_VCCSTG
RC76 RC77 RC78 2 CMC@ 1 51 0402 5% CPU_XDP_TMS / CPU_XDP_TDI / CPU_XDP_TDO
Place to CPU side
RC79 2 CMC@ 1 51 0402 5% CPU_XDP_TCK0
RC81 2 @ 1 51 0402 5% CPU_XDP_TRST#
RC80 2 @ 1 51 0402 5% PCH_JTAG_TCK1
PCH_JTAG_TCK1 <18>
Place to PCH side

SVID

+1.05VS_VCCSTG
RC21 1K_0402_5%
<58,82,83> H_PROCHOT#
RC14 1 2 499_0402_1% H_PROCHOT#_R
+1.05V_VCCST
RC22 1K_0402_5%
<58,78> EC_VCCST_PG_R
RC151 2 60.4_0402_1% EC_VCCST_PG
<17> H_PM_DOWN_R
RC16 1 2 20_0402_5% H_PM_DOWN
RH2 @ 13_0402_5%

+1.05V_VCCST
RC19 56_0402_1%
RC20 100_0402_1%
<89> CPU_SVID_ALERT#_R
RC13 1 2 220_0402_5% CPU_SVID_ALERT#
<89> CPU_SVID_DAT
CPU_SVID_DAT

<89> CPU_SVID_CLK

<15> PCH_CPU_BCLK_P
<15> PCH_CPU_BCLK_N
<15> PCH_CPU_PCIBCLK_P
<15> PCH_CPU_PCIBCLK_N
<15> PCH_CPU_24M_CLK_P
<15> PCH_CPU_24M_CLK_N

INTEL CONFIDENTIAL Check

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Compal Electronics, Inc.
Title: CFL-H(5/8)CFG,SVID
Size: Custom
Document Number: EH78F M/B LA-G161PR01
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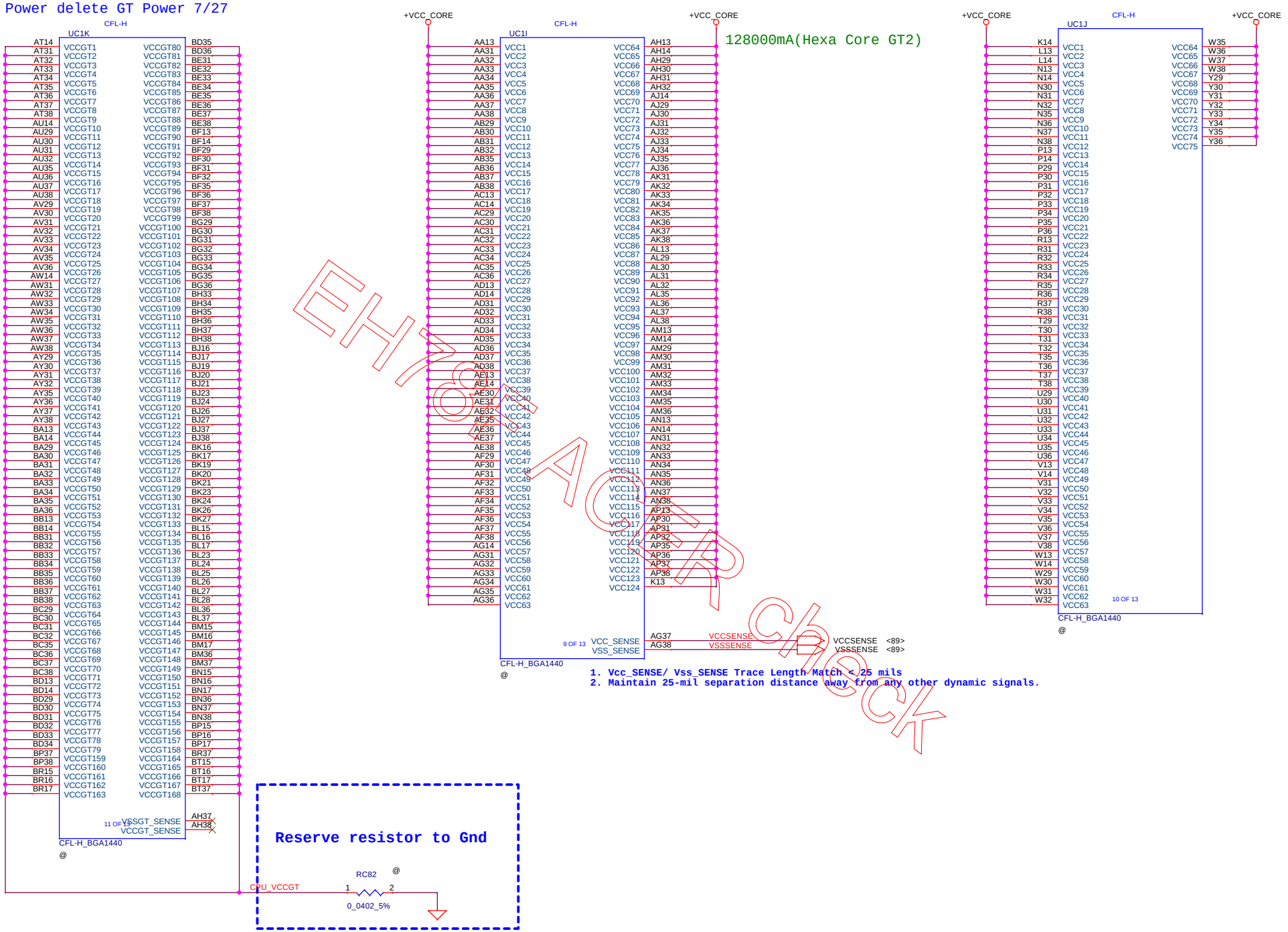
Power delete GT Power 7/27



EH78F ACAD Check

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Compal Electronics, Inc.

Title: CFL-H(6/8)VCC CORE/GT

Size: Custom | Document Number: EH78F M/B LA-G161PR01 | Rev: 0.1

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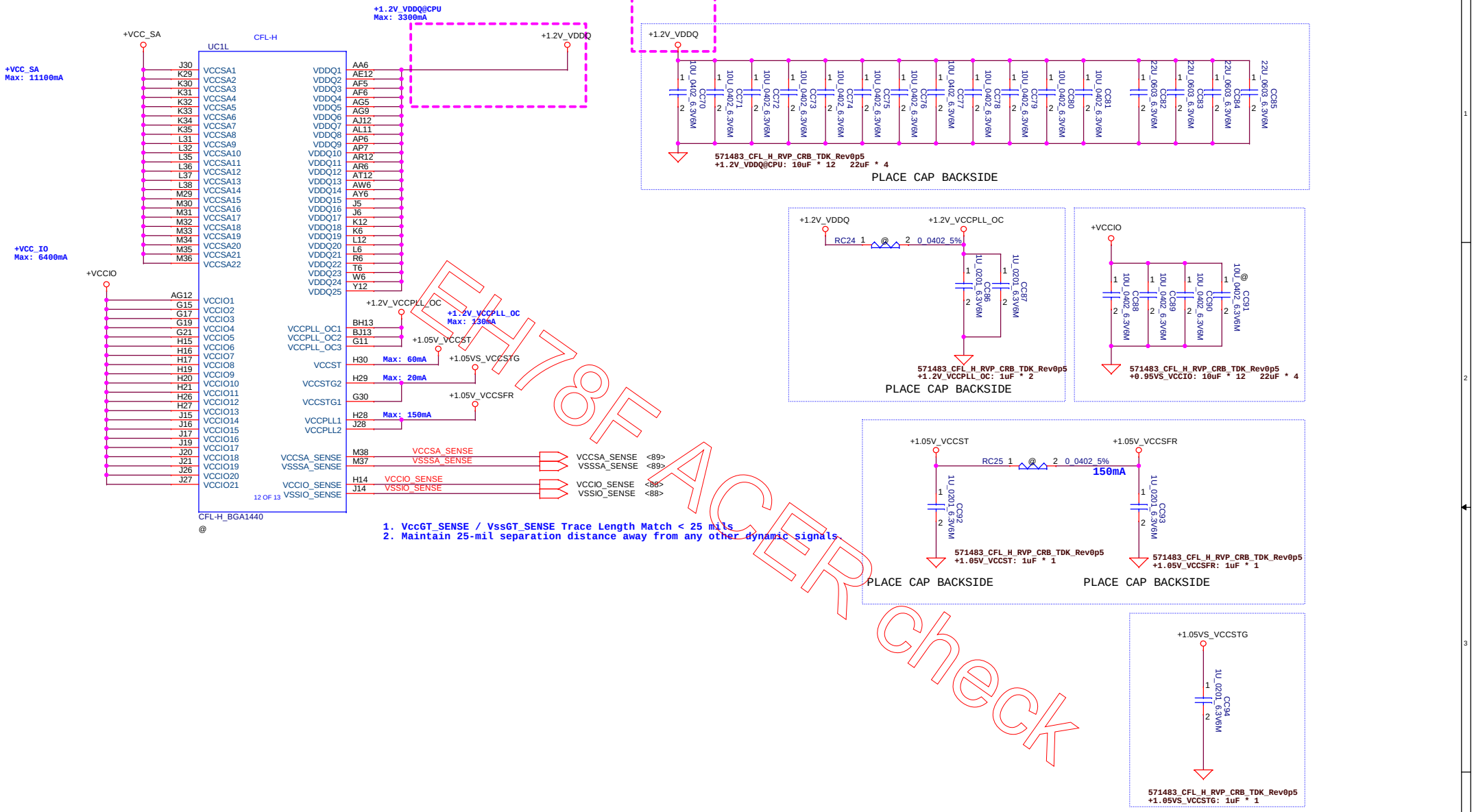

EH78F ACER check

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2018/09/01

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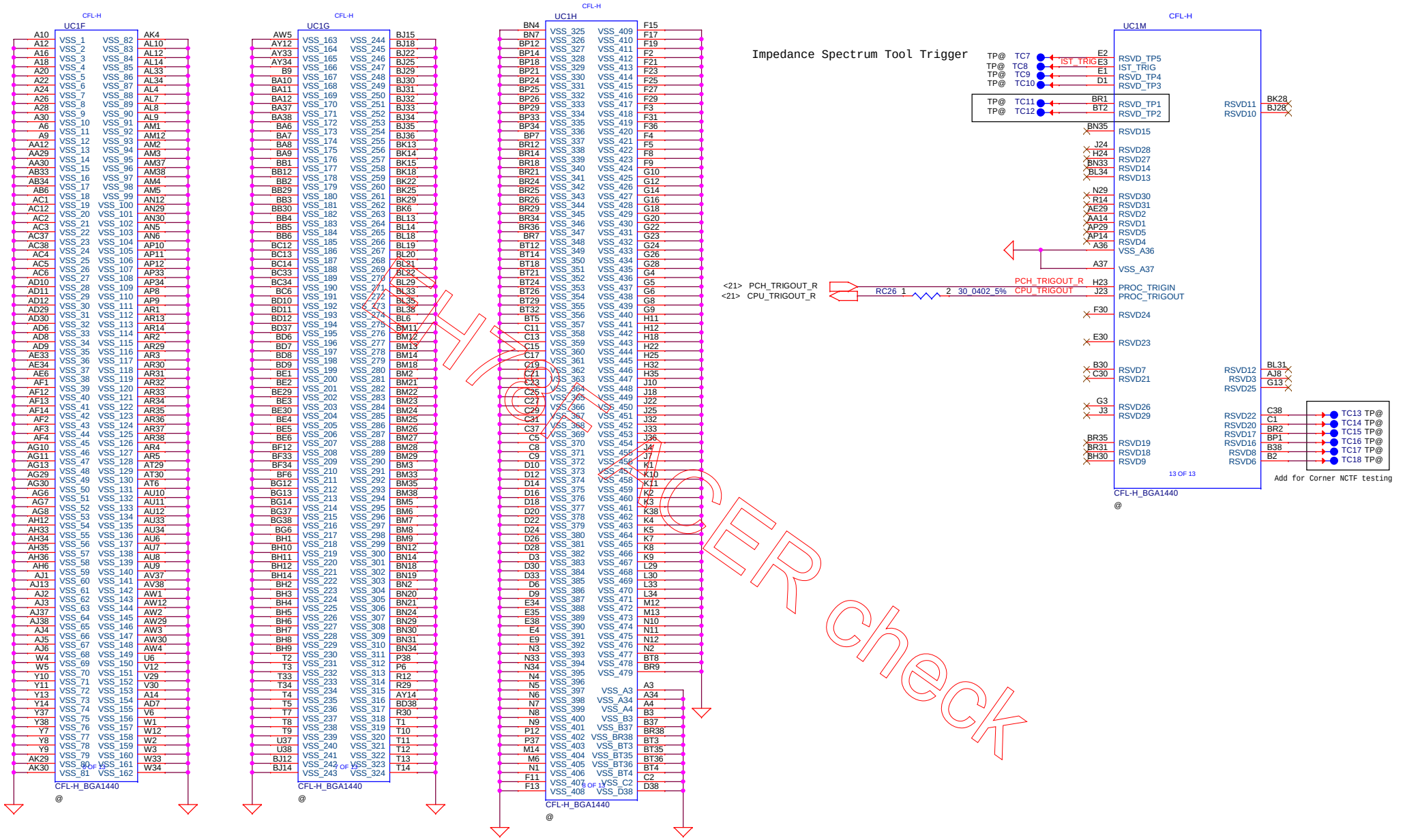
Compal Electronics, Inc.

Title: CFL-H(7/8)VCCSA/VCCIO/VDDQ

Size	Document Number	Rev
Custom	EH78F M/B LA-G161PR01	0.1

Date: Wednesday, January 16, 2019 Sheet 12 of 102



Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2018/09/01

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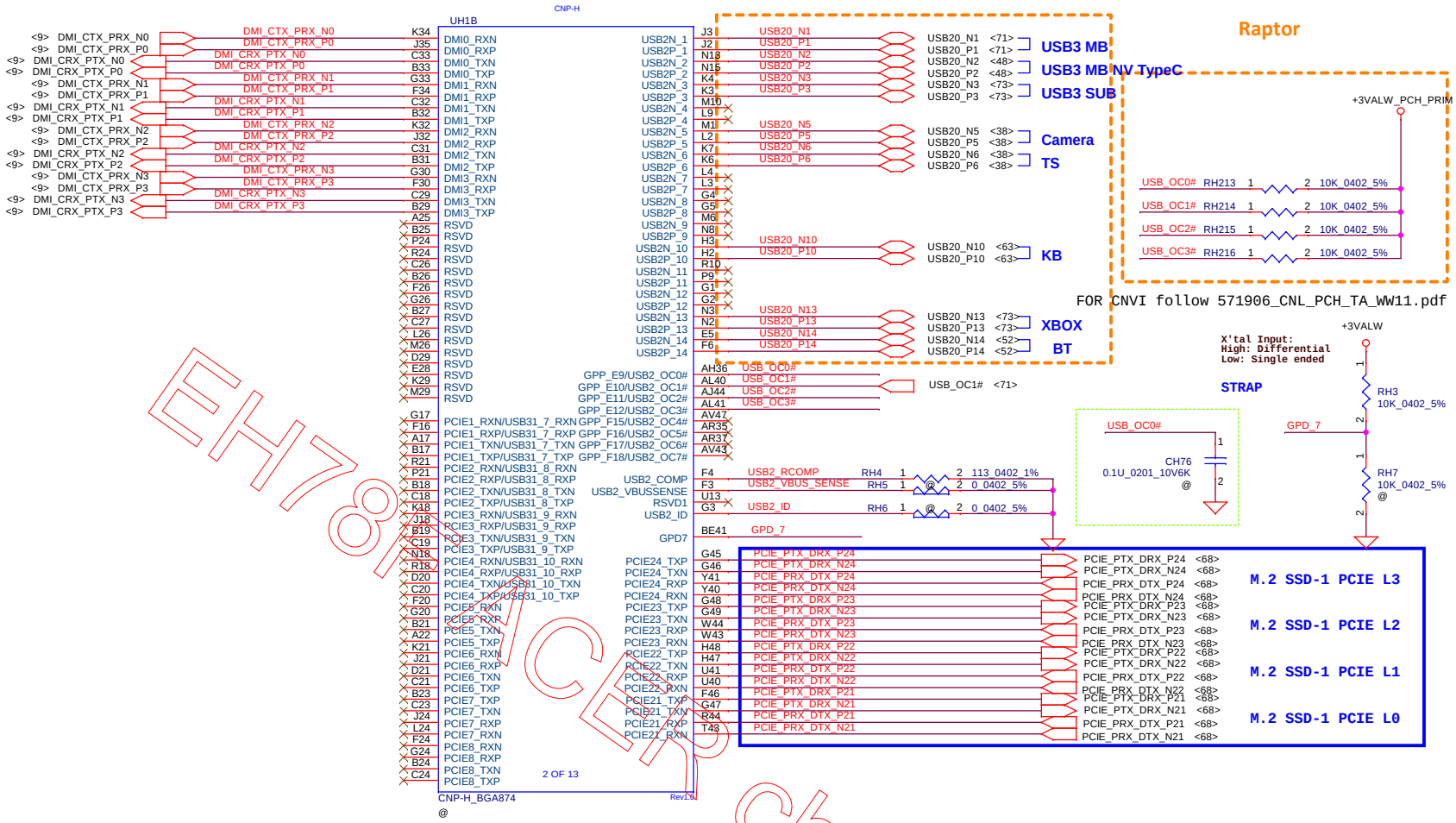
Compal Electronics, Inc.

Title: **CFL-H(8/8)GND/RSVD**

Size	Document Number	Rev
Custom	EH78F M/B LA-G161PR01	0.1

Date: Wednesday, January 16, 2019 Sheet 13 of 102



EH78F MB ECR check

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
High Speed I/O (HSIO) Type and Lane	USB3.1 #1	USB3.1 #2	USB3.1 #3	USB3.1 #4	USB3.1 #5	USB3.1 #6	USB3.1 #7 / PCIe* #1	USB3.1 #8 / PCIe* #2	USB3.1 #9 / PCIe* #3	USB3.1 #10 / PCIe* #4	PCIe* #5 / GbE	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9 / GbE	PCIe* #10 / SATA 0a	PCIe* #11 / GbE	PCIe* #12 / SATA 1a	PCIe* #13 / SATA 0b / GbE	PCIe* #14 / SATA 1b	PCIe* #15 / SATA 2	PCIe* #16 / SATA 3	PCIe* #17 / SATA 4	PCIe* #18 / SATA 5	PCIe* #19	PCIe* #20	PCIe* #21	PCIe* #22	PCIe* #23	PCIe* #24
Intel® RST Support							No Support				No Support				Yes				No Support				Yes				Yes			

The 30 HSIO lanes on PCH-H supports the following configurations:
1. Up to 24 PCIe* Lanes
—A maximum of 16 PCIe* Ports (or devices) can be enabled
- When a GbE Port is enabled, the maximum number of PCIe* Ports (or devices) that can be enabled reduces based off the following:
Max PCIe* Ports (or devices) = 16 - GbE (0 or 1)
— PCIe* Lanes 1-4 (PCIe* Controller #1), 5-8 (PCIe* Controller #2), 9-12 (PCIe* Controller #3), 13-16 (PCIe* Controller #4), 17-20 (PCIe* Controller #5), and 21-24 (PCIe* Controller #6) can be individually configured
2. Up to 6 SATA Lanes
— A maximum of 6 SATA Ports (or devices) can be enabled
— SATA Lane 0 has the flexibility to be mapped to Flex I/O Lane 16 or 18
— SATA Lane 1 has the flexibility to be mapped to Flex I/O Lane 17 or 19
3. Up to 10 USB 3.1 Lanes
— A maximum of 10 USB 3.1 Ports (or devices) can be enabled
4. Up to 4 GbE Lanes
— A maximum of 1 GbE Port (or device) can be enabled
5. Supports up to 3 Remapped (IntelR Rapid Storage Technology) PCIe* storage devices
— x2 and x4 PCIe* NVMe SSD
— x2 IntelR Optane? Memory Device
— See the "PCI Express* (PCIe*)" chapter for the PCH PCIe* Controllers,configurations , and lanes that can be used for IntelR Rapid Storage Technology PCIe* storage support

6. For unused SATA/PCIe* Combo Lanes, Flex I/O Lanes that can be configured as PCIe* or SATA, the lanes must be statically assigned to SATA or PCIe* via the SATA/PCIe Combo Port Soft Straps discussed in the SPI Programming Guide and through the IntelR Flash Image Tool (FIT) tool.

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2018/09/01

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Compal Electronics, Inc.

Title: PCH(1/8)DMI/PCIE/USB2

Size	Document Number	Rev
Custom	EH78F M/B LA-G161PR01	0.1

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PCH-H XTAL_IN/OUT POR is 24MHz for 571697_CNL_MOW_WW16_2017.pdf

XTAL_24M_PCH_OUT — RH11 EMC@ 33_0402_1% — XTAL_24M_PCH_OUT_R

XTAL_24M_PCH_IN — RH8 1M_0402_5% — RH9 EMC@ 33_0402_1% — XTAL_24M_PCH_IN_R

YH1 24MHZ_18PF_XRCGB24M000F2P51R0

NC NC

CH5 18P_0402_50V8J — CH6 18P_0402_50V8J

PCH_RTCX1 — RH12 10M_0402_5% — PCH_RTCX2

YH2 32.768KHZ_9PF_X1A000141000200

CH7 10P_0402_50V8J — CH8 10P_0402_50V8J

Trace Space: 15 mil
Max Trace Length: 1000 mil

use same part w C5MMH

remove TP as C5PRH

UH1G — CNP-H — CNP-H_BGA874 — 7 OF 13 — Rev1.0

GPP_A16/CLKOUT_48 — BE33

<10> PCH_CPU_24M_CLK_P — PCH_CPU_24M_CLK_P — D7
<10> PCH_CPU_24M_CLK_N — PCH_CPU_24M_CLK_N — C6

CLKOUT_CPUNSSC_P — CLKOUT_ITPXDP# — Y3 — TP@ TH2
CLKOUT_CPUNSSC# — CLKOUT_ITPXDP_P — Y4 — TP@ TH3

<10> PCH_CPU_BCLK_P — PCH_CPU_BCLK_P — B8
<10> PCH_CPU_BCLK_N — PCH_CPU_BCLK_N — C8

CLKOUT_CPUBCLK_P CLKOUT_CPUPCIBCLK# — B6 PCH_CPU_PCIBCLK_N — PCH_CPU_PCIBCLK_N <10>
CLKOUT_CPUBCLK# CLKOUT_CPUPCIBCLK_P — A6 PCH_CPU_PCIBCLK_P — PCH_CPU_PCIBCLK_P <10>

XTAL_24M_PCH_OUT_R — U9
XTAL_24M_PCH_IN_R — U10

XTAL_OUT — CLKOUT_PCIE_N0 — AJ6 CLK_PEG_VGA# — CLK_PEG_VGA# <25>
XTAL_IN — CLKOUT_PCIE_P0 — AJ7 CLK_PEG_VGA — CLK_PEG_VGA <25> — DGPU

RH10 2_60.4_0402_1% — XCLK_BIASREF — T3

XCLK_BIASREF — CLKOUT_PCIE_N1 — AH9 CLK_PCIE_LAN# — CLK_PCIE_LAN# <51>
CLKOUT_PCIE_P1 — AH10 CLK_PCIE_LAN — CLK_PCIE_LAN <51> — GLAN

XCLK_BIASREF (PDG)
Trace Width/Space: 15mil /15 mil
Max Trace Length: 1000 mil
8/24

PCH_RTCX1 — BA49
PCH_RTCX2 — BA48

RTCX1 — CLKOUT_PCIE_N2 — AE14 CLK_PCIE_WLAN# — CLK_PCIE_WLAN# <52>
RTCX2 — CLKOUT_PCIE_P2 — AE15 CLK_PCIE_WLAN — CLK_PCIE_WLAN <52> — NGFF WL+BT(KEY E)

<25> VGA_CLKREQ# — VGA_CLKREQ# — BF31
<51> LAN_CLKREQ# — LAN_CLKREQ# — BE31
<52> WLAN_CLKREQ# — WLAN_CLKREQ# — AR32
<68> SSD1_CLKREQ# — SSD1_CLKREQ# — BB30
<43> TBT_CLKREQ# — TBT_CLKREQ# — BA30
<68> SSD2_CLKREQ# — SSD2_CLKREQ# — AN29

GPP_B5/SRCCLKREQ0# — CLKOUT_PCIE_N3 — AE6 CLK_PCIE_NGFF1# — CLK_PCIE_NGFF1# <68>
GPP_B6/SRCCLKREQ1# — CLKOUT_PCIE_P3 — AE7 CLK_PCIE_NGFF1 — CLK_PCIE_NGFF1 <68> — M2-1 SSD
GPP_B7/SRCCLKREQ2# — AC2 CLK_PCIE_TBT# — CLK_PCIE_TBT# <43>
GPP_B8/SRCCLKREQ3# — CLKOUT_PCIE_N4 — AC3 CLK_PCIE_TBT — CLK_PCIE_TBT <43> — TBT
GPP_B9/SRCCLKREQ4# — CLKOUT_PCIE_P4 — AB2 CLK_PCIE_NGFF2# — CLK_PCIE_NGFF2# <68>
GPP_B10/SRCCLKREQ5# — AB3 CLK_PCIE_NGFF2 — CLK_PCIE_NGFF2 <68> — M2-2 SSD
GPP_H0/SRCCLKREQ6# — CLKOUT_PCIE_N5 — W4
GPP_H1/SRCCLKREQ7# — CLKOUT_PCIE_P5 — W3
GPP_H2/SRCCLKREQ8# — CLKOUT_PCIE_N6 — W7
GPP_H3/SRCCLKREQ9# — CLKOUT_PCIE_P6 — W6
GPP_H4/SRCCLKREQ10# — CLKOUT_PCIE_N7 — AC14
GPP_H5/SRCCLKREQ11# — CLKOUT_PCIE_P7 — AC15
GPP_H6/SRCCLKREQ12# — CLKOUT_PCIE_N8 — U2
GPP_H7/SRCCLKREQ13# — CLKOUT_PCIE_P8 — U3
GPP_H8/SRCCLKREQ14# — CLKOUT_PCIE_N9 — AC9
GPP_H9/SRCCLKREQ15# — CLKOUT_PCIE_P9 — AC11
CLKOUT_PCIE_N10 — AE9
CLKOUT_PCIE_N15 — CLKOUT_PCIE_P10 — AE11
CLKOUT_PCIE_P15
CLKOUT_PCIE_N11
CLKOUT_PCIE_N14 — CLKOUT_PCIE_P11
CLKOUT_PCIE_P14
CLKOUT_PCIE_N12
CLKOUT_PCIE_N13 — CLKOUT_PCIE_P12
CLKOUT_PCIE_P13
CLKIN_XTAL — R6 — REFCLK_CNV — REFCLK_CNV <52>

Raptor

RH14 10K_0402_5%

+3VS

RH217 LAN_CLKREQ# — RH218 VGA_CLKREQ# — RH219 WLAN_CLKREQ# — RH220 SSD1_CLKREQ# — 10K_0402_5%

RH221 SSD2_CLKREQ# — RH222 TBT_CLKREQ# — 10K_0402_5%

Raptor

EH78F ACED ckt

remove SD signal from PCH

remove CPU_C10_GATE#

UH1M — CNP-H — CNP-H_BGA874 — 13 OF 13 — Rev1.0

GPP_G0/SD_CMD — AW13
GPP_G1/SD_DATA0 — BE9
GPP_G2/SD_DATA1 — BF8
GPP_G3/SD_DATA2 — BF9
GPP_G4/SD_DATA3 — BG8
GPP_G5/SD_CD# — BE8
GPP_G6/SD_CLK — BD8
GPP_G7/SD_WP — AV13

CNV_WR_CLKN — BD4 CLK_CNV_PRX_DTX_N — CLK_CNV_PRX_DTX_N <52>
CNV_WR_CLKP — BE3 CLK_CNV_PRX_DTX_P — CLK_CNV_PRX_DTX_P <52>

CNV_WR_D0N — BB3 CNV_PRX_DTX_N0 — CNV_PRX_DTX_N0 <52>
CNV_WR_D0P — BB4 CNV_PRX_DTX_P0 — CNV_PRX_DTX_P0 <52>
CNV_WR_D1N — BA3 CNV_PRX_DTX_N1 — CNV_PRX_DTX_N1 <52>
CNV_WR_D1P — BA2 CNV_PRX_DTX_P1 — CNV_PRX_DTX_P1 <52>

CNV_WT_CLKN — BC5 CLK_CNV_PTX_DRX_N — CLK_CNV_PTX_DRX_N <52>
CNV_WT_CLKP — BB6 CLK_CNV_PTX_DRX_P — CLK_CNV_PTX_DRX_P <52>

CNV_WT_D0N — BE6 CNV_PTX_DRX_N0 — CNV_PTX_DRX_N0 <52>
CNV_WT_D0P — BD7 CNV_PTX_DRX_P0 — CNV_PTX_DRX_P0 <52>
CNV_WT_D1N — BG6 CNV_PTX_DRX_N1 — CNV_PTX_DRX_N1 <52>
CNV_WT_D1P — BF6 CNV_PTX_DRX_P1 — CNV_PTX_DRX_P1 <52>
CNV_WT_RCOMP — BA1 CNV_WT_RCOMP — RH16 150_0402_1%

PCIE_RCOMPN — B12 PCIE_RCOMPN — RH17 100_0402_1%
PCIE_RCOMPP — A13 PCIE_RCOMPP

SD_1P8_RCOMP — BE5 SD_RCOMP_1P8 — RH18 200_0402_1%
SD_3P3_RCOMP — BE4 SD_RCOMP_3P3 — RH19 200_0402_1%

GPPJ_RCOMP_1P81 — BD1
GPPJ_RCOMP_1P82 — BE1 GPPJ_RCOMP_1P8 — RH20 200_0402_1%
GPPJ_RCOMP_1P83 — BE2

RSVD2 — Y35
RSVD3 — Y36
RSVD1 — BC1
TP — AL35 — TP@ TH4

#571483_CFL_H_RVP_CRB_TDK_Rev0p5
Recommend external test point

checked CRB

3.3V

1.8V

<52> CNV_BRI_PTX_DRX — CNV_BRI_PTX_DRX — AV4
<52> CNV_BRI_PRX_DTX — CNV_BRI_PRX_DTX — AY2
<52> CNV_RGI_PTX_DRX — CNV_RGI_PTX_DRX — BA4
<52> CNV_RGI_PRX_DTX — CNV_RGI_PRX_DTX — AV3
GPP_J9 — AW2 — AU9

GPP_J_2
GPP_J_3
GPP_J4/CNV_BRI_DT/UART0B_RTS#
GPP_J5/CNV_BRI_RSP/UART0B_RXD
GPP_J6/CNV_RGI_DT/UART0B_TXD
GPP_J7/CNV_RGI_RSP/UART0B_CTS#
GPP_J8/CNV_MFUART2_RXD
GPP_J9/CNV_MFUART2_TXD

For DDX03 R02

XTAL Frequency Select

+1.8VALW_PRIM — RH15 4.7K_0402_5% — CNV_BRI_PTX_DRX — STRAP

This signal has a weak internal pull-down 20K.
0 = 38.4/19.2MHz XTAL frequency selected.
1 = 24MHz XTAL frequency selected. (DDX03)
Notes:
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

VCCPSPI Select

+1.8VALW_PRIM — RH21 @ 4.7K_0402_5% — GPP_J9 — STRAP

The signal has a weak internal pull-down 20K
0 = VCCPSPI is connected to 3.3V rail
1 = VCCPSPI is connected to 1.8V rail
Note: If VCCPSPI is connected to 1.8V rail, this pin strap must be a '1' for the proper functionality of the SPI (Flash) I/Os

M.2 CNV Mode Select

+1.8VALW_PRIM — RH22 10K_0402_5% — CNV_RGI_PTX_DRX — STRAP
RH23 @ 10K_0402_5%

An external pull-up or pull-down is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.
Pulled down by CRF CNVi RGI_DT pin

+1.8VALW_PRIM
RH1811 CNVI@ 20K_0402_1% — CNV_BRI_PRX_DTX
RH1821 CNVI@ 20K_0402_1% — CNV_RGI_PRX_DTX

571391_CFL_H_PDG_Rev0p71
To avoid floating input at the I/O pin BRI_RSP and RGI_RSP it is recommended to add a weak pull up resistor to the SoC pin with a recommended value of 20K ohm.

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Compal Electronics, Inc.

Title: PCH(2/8)CLK/CNVI/SD

Size: Custom | Document Number: EH78F M/B LA-G161PR01 | Rev: 0.1

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Raptor: for GC 3.0

<39> DP0_HPD_PCH
<40> HDMI_HPD_PCH
<49> CCG4_HOTPLUG_DET_3V3
<42,43> TBT_DP4_HPD

DP0_HPD_PCH — RT881 1 @ 2 0_0402_5% — AT6
HDMI_HPD_PCH — AN10
CCG4_HOTPLUG_DET_3V3 — RT880 1 @ 2 0_0402_5% — AP9
TBT_DP4_HPD — RT879 1 @ 2 0_0402_5% — AL15

CPU_EDP_HPD_R — AN6

UH1E
CNP-H
GPP_I0/DDPB_HPD0/DISP_MISC0
GPP_I1/DDPC_HPD1/DISP_MISC1
GPP_I2/DDPD_HPD2/DISP_MISC2
GPP_I3/DDPF_HPD3/DISP_MISC3
GPP_I4/EDP_HPD/DISP_MISC4
GPP_I5/DDPB_CTRLCLK — AL13
GPP_I6/DDPB_CTRLDATA — AR8
GPP_I7/DDPC_CTRLCLK — AN13
GPP_I8/DDPC_CTRLDATA — AL10
GPP_I9/DDPD_CTRLCLK — AL9
GPP_I10/DDPD_CTRLDATA — AR3
GPP_F23/DDPF_CTRLDATA — AN40
GPP_F22/DDPF_CTRLCLK — AT49
GPP_F14/PS_ON# — AP41
GPP_K23/IMGCLKOUT1 — M45
GPP_K22/IMGCLKOUT0 — L48
GPP_K21 — T45
GPP_K20 — T46
GPP_H23/TIME_SYNC0 — AJ47
5 OF 13
CNP-H_BGA874
Rev1.0
@

TBT_CIO_PLUG_EVENT# <43>

Raptor

RX3 0_0402_5% — CPU_EDP_HPD_R — EDP_HPD_R — EDP_HPD_R <38>
RX4 100K_0402_5%

Raptor TBT

intel critical net recommend

RH1981 2 100K_0201_5%
PLT_RST# — CH9 1 2 100P_0402_50V8J — XEMC@

can remove if no use DP
08/18

remove PCH DP SCLK/SDATA

DDP[B..F]CTRLDATA
This signal has a weak internal Pull-down.
0 = Port B~D is not detected.
1 = Port B,C,D is detected. (Default)
Notes:
1. The internal Pull-down is disabled after PCH_PWROK de-asserts.
2. This signal is in the primary well.

<51,58> EC_PME# — RH24 1 @ 2 0_0402_5% — EC_PME#_R — BE36

UH1A
CNP-H
GPP_A11/PME#/SD_VDD2_PWR_EN#
RSVD2 — R15
RSVD1 — R13
VSS — AL37
TP — AN35
SPI0_MOSI — AU41
SPI0_MISO — BA45
SPI0_CS0# — AY47
SPI0_CLK — AW47
SPI0_CS1# — AW48
SPI0_IO2 — AY48
SPI0_IO3 — BA46
SPI0_CS2# — AT40
GPP_D1/SPI1_CLK/SBK1_BK1 — BE19
GPP_D0/SPI1_CS#/SBK0_BK0 — BF19
GPP_D3/SPI1_MOSI/SBK3_BK3 — BF18
GPP_D2/SPI1_MISO/SBK2_BK2 — BE18
GPP_D22/SPI1_IO3 — BC17
GPP_D21/SPI1_IO2 — BD17
1 OF 13
CNP-H_BGA874
Rev1.0
@

GPP_B13/PLTRST# — AV29 — PLT_RST# — PLT_RST# <58>
GPP_K16/GSXCLK — Y47
GPP_K12/GSXDOUT — Y46
GPP_K13/GSXSLOAD — Y48
GPP_K14/GSXDIN — W46
GPP_K15/GSXSRESET# — AA45

GPIO Serial Expander (GSX) is the capability provided by the PCH to expand the GPIOs on a platform that needs more GPIOs than the ones provided by the PCH.

GPP_E3/CPU_GP0 — AL47
GPP_E7/CPU_GP1 — AM45
GPP_B3/CPU_GP2 — BF32 — TP_INT# 2 1 — TYPEC_1P5A DH1 — RB751V-40_SOD323-2 — TYPEC_1P5A <45,49> — EC_TP_INT# <58,63>
GPP_B4/CPU_GP3 — BC33

+3VS
TP_INT# — RH28 2 1 100K_0402_5%

GPP_H18/SML4ALERT# — AE44
GPP_H17/SML4DATA — AJ46 — iTBT_FORCE_PWR — TBT_FORCE_PWR <43>
GPP_H16/SML4CLK — AE43 — RTD3_CIO_PWR_EN — RTD3_CIO_PWR_EN <43>
GPP_H15/SML3ALERT# — AC47 — GPP_H15
GPP_H14/SML3DATA — AD48
GPP_H13/SML3CLK — AF47
GPP_H12/SML2ALERT# — AB47 — GPP_H12 — GPP_H12 <19>
GPP_H11/SML2DATA — AD47
GPP_H10/SML2CLK — AE48
INTRUDER# — BB44 — SM_INTRUDER# — 1M_0402_5% 2 1 RH30 — +RTCVCC

RVP: 330K
A 1 M pull-up is used on the customer reference board (CRB). This is needed to reduce leakage from Coin Cell Battery in G3 state.

Raptor TBT

* wait confirm CG7
PDG P348 quad mode support PH1K
CRB PU 20k
#571182_CFL_PCH_EDS_Rev1.0 recommend 100k

CRB connect GND

+3VALW_SPI
#571391_CFL_H_PDG_Rev0p71

RH25 2 1 1K_0402_5% — PCH_SPI_IO2
RH26 2 1 1K_0402_5% — PCH_SPI_IO3
RH27 2 1 1K_0402_5% — PCH_SPI_SI

+3VALW_PCH_PRIM
RH29 2 1 100K_0402_5% — GPP_H15 — STRAP

#571182_CNL_PCH_H_EDS_V1_Rev0.7
External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
571007_CFL_MOW_Archive_WW22_2017
STUFF R on GPP_H15

TH6 TP@ — RH1861 @ 2 0_0402_5% — AL37
TH50 TP@ — PCH_HDD_PWRGT

Raptor

PCH_SPI_CLK — RH1951 @ 2 100K_0201_5%

intel critical net recommend

SPI ROM (16MByte)

+3VALW_SPI
CH10 1 2 0.1U_0201_10V6K

UH2
PCH_SPI_CS#0 — 1 /CS — VCC 8
PCH_SPI_SO_0_R — 2 DO(IO1) — /HOLD(IO3) 7 — PCH_SPI_IO3_0_R
PCH_SPI_IO2_0_R — 3 /WP(IO2) — CLK 6 — PCH_SPI_CLK_0_R
4 GND — DI(IO0) 5 — PCH_SPI_SI_0_R
W25Q128FVSIQ_SO8
P/N: SA00005VV20

+3VALW_SPI
PCH_SPI_CS#0 — RH31 1 @ 2 4.7K_0402_5%

PCH_SPI_CLK_0_R — RH33 @ 1 0_0402_5% — CH12 @ 2 68P_0402_50V8J

PCH_SPI_SI_0_R — RH107 — PCH_SPI_SI
PCH_SPI_SO_0_R — RH108 — PCH_SPI_SO
PCH_SPI_IO3_0_R — RH109 — PCH_SPI_IO3
PCH_SPI_CLK_0_R — RH110 — PCH_SPI_CLK
PCH_SPI_IO2_0_R — RH111 — PCH_SPI_IO2
1 — 2 33_0402_1%

intel PDG 1.8
33 ohm for 3.3V for singel load
place 500 mil from PCH

note : 1050 Use 8M rom

PCH PLTRST Buffer

RH32 1 @ 2 0_0402_5% — PLT_RST# — PLT_RST_BUF# <25,43,49,51,52,68>
+3VS
CH11 2 .1U_0402_16V7K
UH3 TC7SH08FU_SSOP5

ENGINEER check

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2018/09/01

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Compal Electronics, Inc.
Title: PCH(3/8)DDC/SPI
Size: Custom
Document Number: EH78F M/B LA-G161PR01
Rev: 0.1
Date: Wednesday, January 16, 2019
Sheet 16 of 102

#571391_CFL_H_PDG_Rev0p5
- eSPI clock and eSPI data mismatched: <500 mils.
- eSPI clock and eSPI chip select mismatched: <500 mils.
- eSPI signal maximum 9 Vias

* If DATA signals are entirely routed on MS, stuff the resistor with 15 Ohm.

USB3 MB

USB3 NV TypeC

USB3 SUB

CNP-H

UH1F

CNP-H_BGA874

6 OF 13

Rev1.0

LPC Bus check straps

LPC : +3.3V

Raptor

CONFIRM WITH SW

CONFIRM WITH SW

For Intel CLINK

M.2 SSD-1 PCIE L3

M.2 SSD-1 PCIE L2

NGFF
WL+BT(KEY E)

M.2 SSD-1 PCIE L1

TBT PCIE L0

TBT PCIE L1

GLAN

M.2 SSD-1 PCIE L0

TBT PCIE L3

TBT PCIE L2

M.2 SSD PCIE/SATA select pin

CONFIRM WITH SW

DIS only

3 OF 13

Vinafix.com

	GPP_F13
	DGPU_PRSNT#
DIS,Optimus	0
UMA	1

Raptor

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2018/09/01

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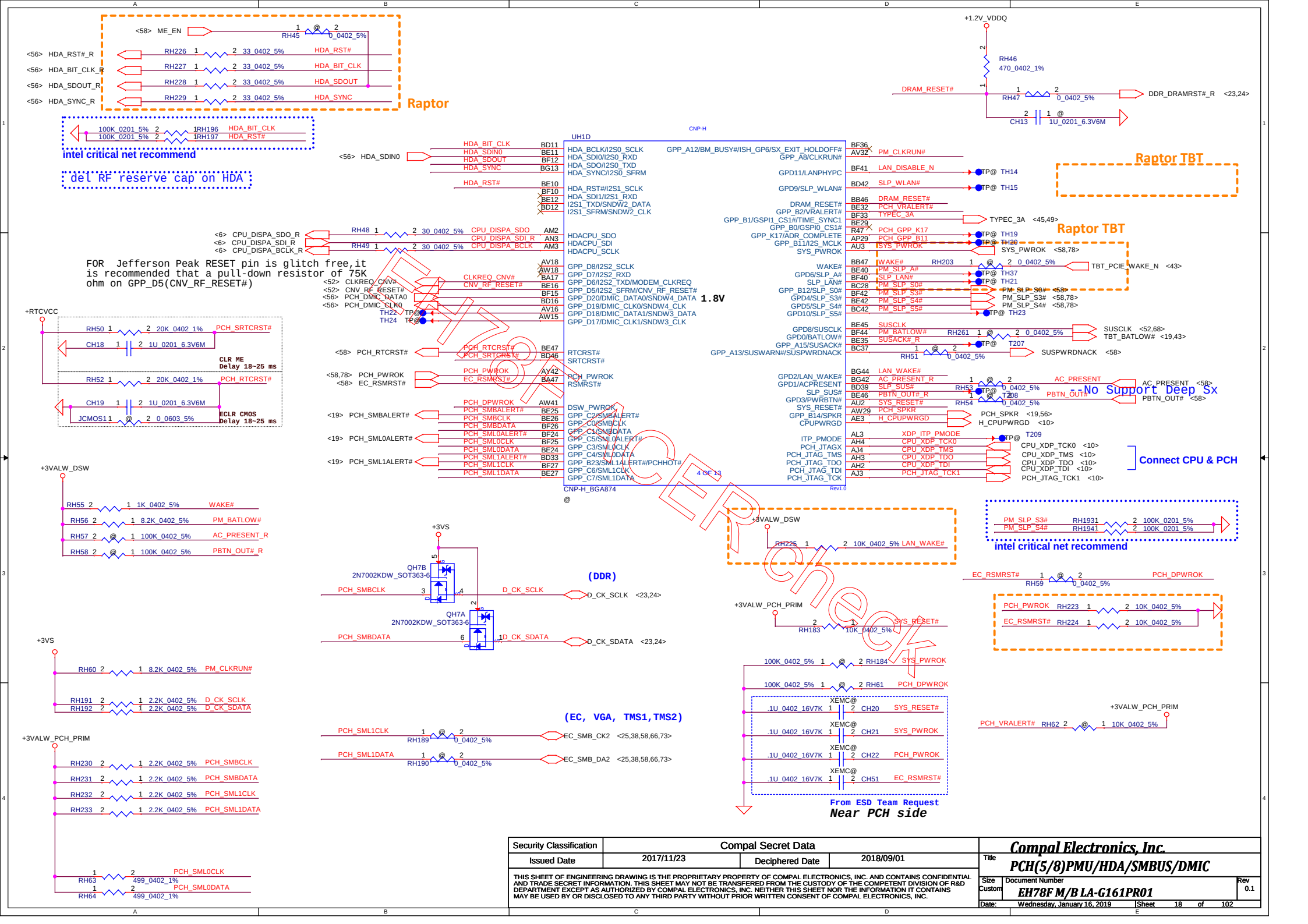
Compal Electronics, Inc.

Title: PCIE/SATA/USB3/eSPI

Size: Custom | Document Number: EH78F M/B LA-G161PR01 | Rev: 0.1

Date: Wednesday, January 16, 2019 | Sheet 17 of 102



Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2018/09/01

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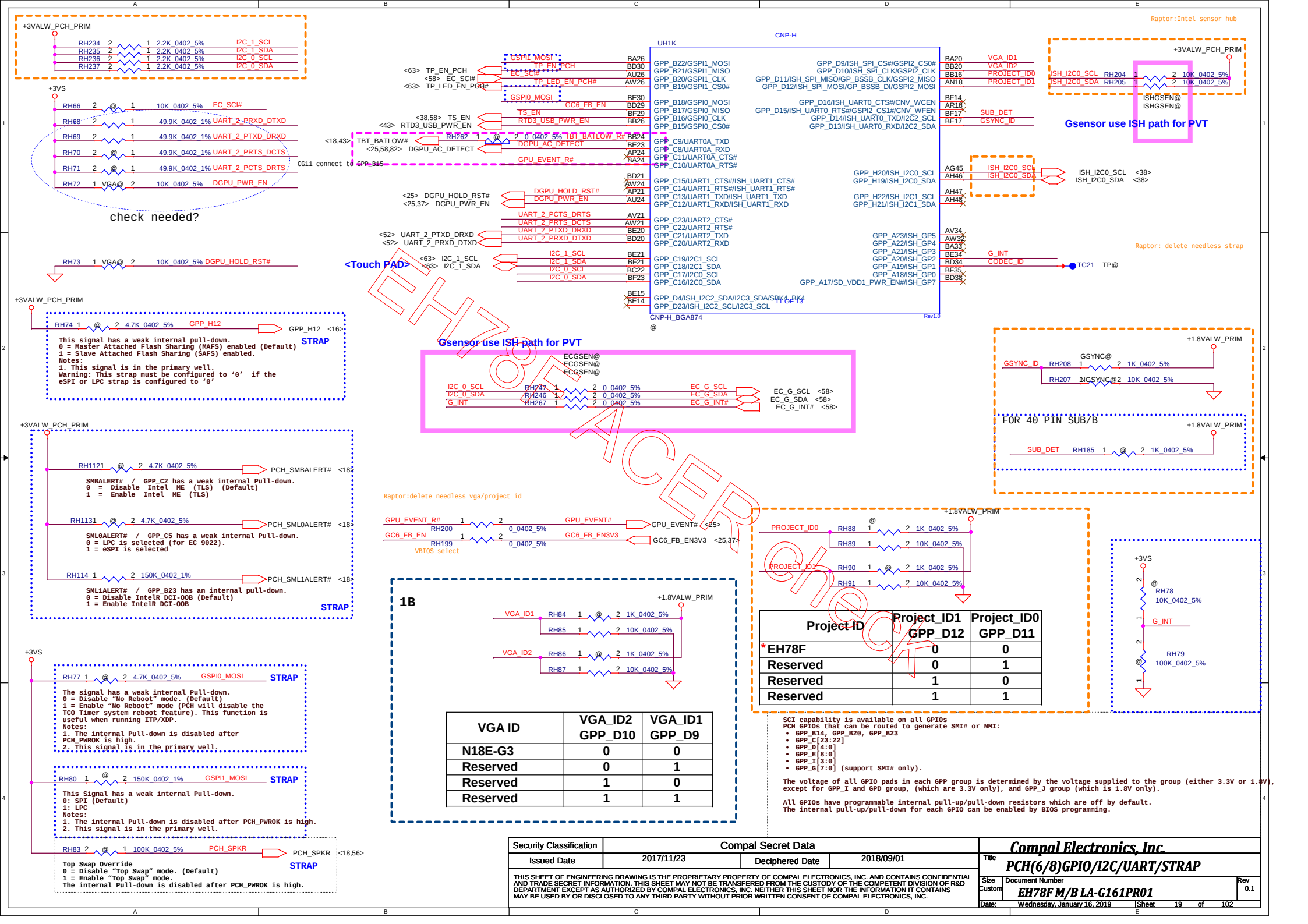
Compal Electronics, Inc.			
Title	PCH(5/8)PMU/HDA/SMBUS/DMIC		
Size	Document Number		Rev
Custom	EH78F M/B LA-G161PR01		0.1
Date:	Wednesday, January 16, 2019	Sheet 18 of 102	



VGA ID	VGA_ID2 GPP_D10	VGA_ID1 GPP_D9
N18E-G3	0	0
Reserved	0	1
Reserved	1	0
Reserved	1	1

Project ID	Project_ID1 GPP_D12	Project_ID0 GPP_D11
*EH78F	0	0
Reserved	0	1
Reserved	1	0
Reserved	1	1

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2018/09/01

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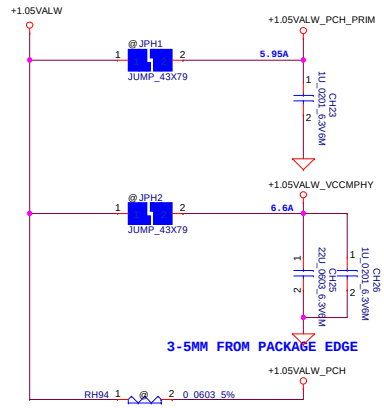
Compal Electronics, Inc.

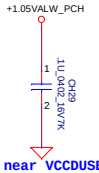
Title: PCH(6/8)GPIO/I2C/UART/STRAP

Size: Custom | Document Number: EH78F M/B LA-G161PR01 | Rev: 0.1

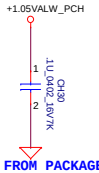
Date: Wednesday, January 16, 2019 | Sheet 19 of 102

GPIO Group	Voltage
GPPA	3.3V
GPPB GPPC	3.3V
GPPD	3.3V * 1.8V
GPPE GPPF	3.3V
GPPG	3.3V
GPPH GPPK	3.3V
GPPI	3.3V Only
GPPJ	1.8V Only
GPD	3.3V Only

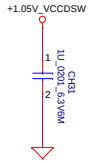




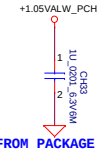
place near VCCDUSB
FOR W22/W23



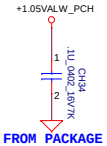
1-3MM FROM PACKAGE
VCCPRIM_MPHY W31



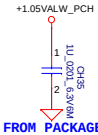
1-3MM FROM PACKAGE EDGE



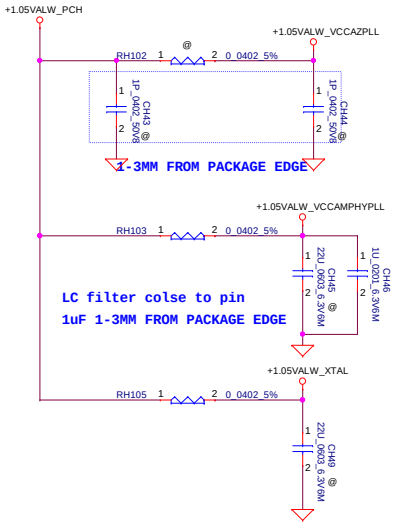
1-5MM FROM PACKAGE EDGE
FOR VCCAPLL C1/C2

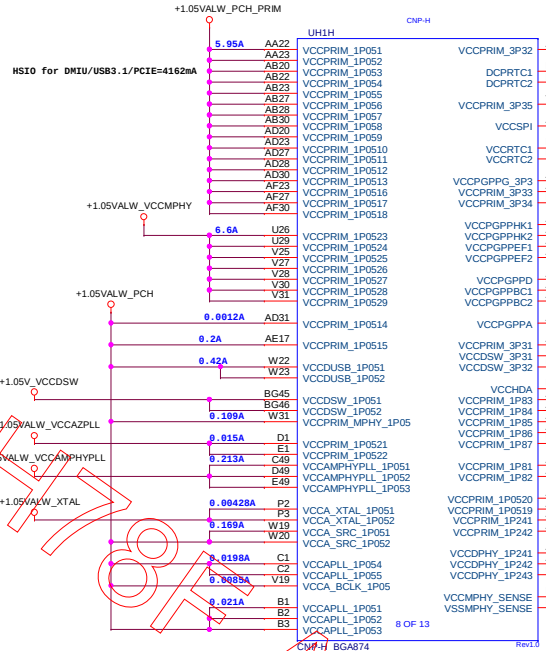


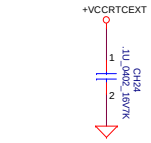
1-3MM FROM PACKAGE EDGE
FOR VCCA_BCLK V19

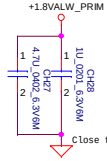


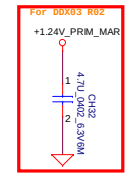
1-5MM FROM PACKAGE EDGE
FOR VCCAPLL B1/B2/B3

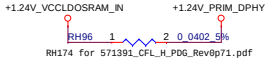


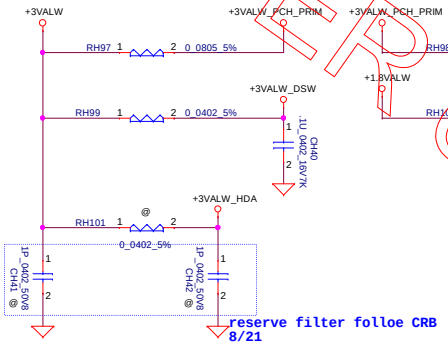


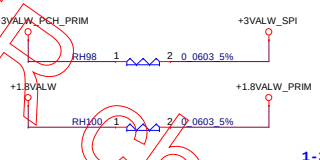


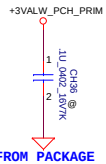




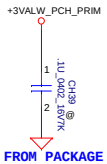




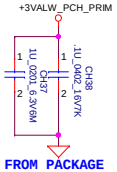




1-3MM FROM PACKAGE
FOR PGPPEF AE35/AE37

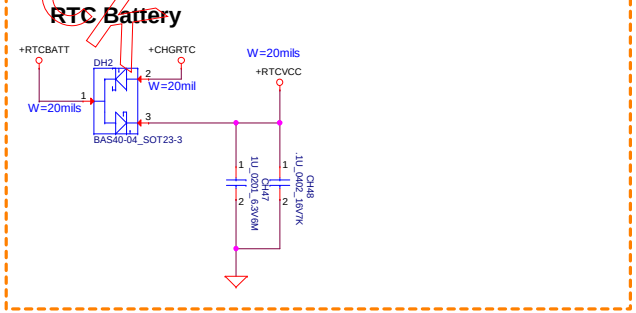


1-3MM FROM PACKAGE
FOR PGPPHK AC35/AC36



1-3MM FROM PACKAGE
FOR VCCPRIM AY8/BB7

Raptor:use chargeable RTC, JRTC on POWER side



ETV for AVCFD check

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2018/09/01

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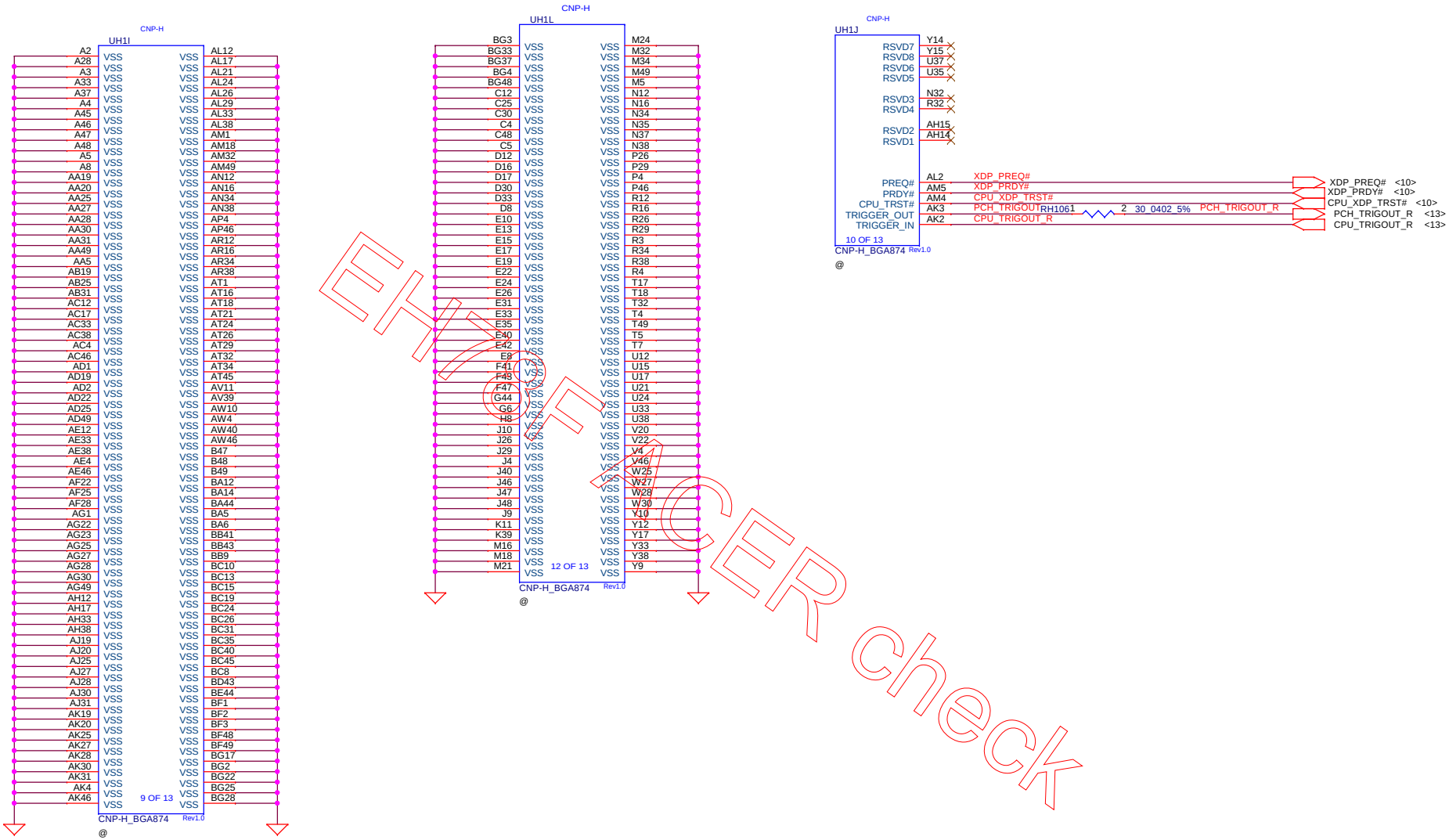
Compal Electronics, Inc.

Title: PCH(7/8)Power

Size	Document Number	Rev
Custom	EH78F M/B LA-G161PR01	0.1

Date: Wednesday, January 16, 2019 | Sheet 20 of 102



ENGINEER check

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Issued Date	2017/11/23	Deciphered Date	2018/09/01

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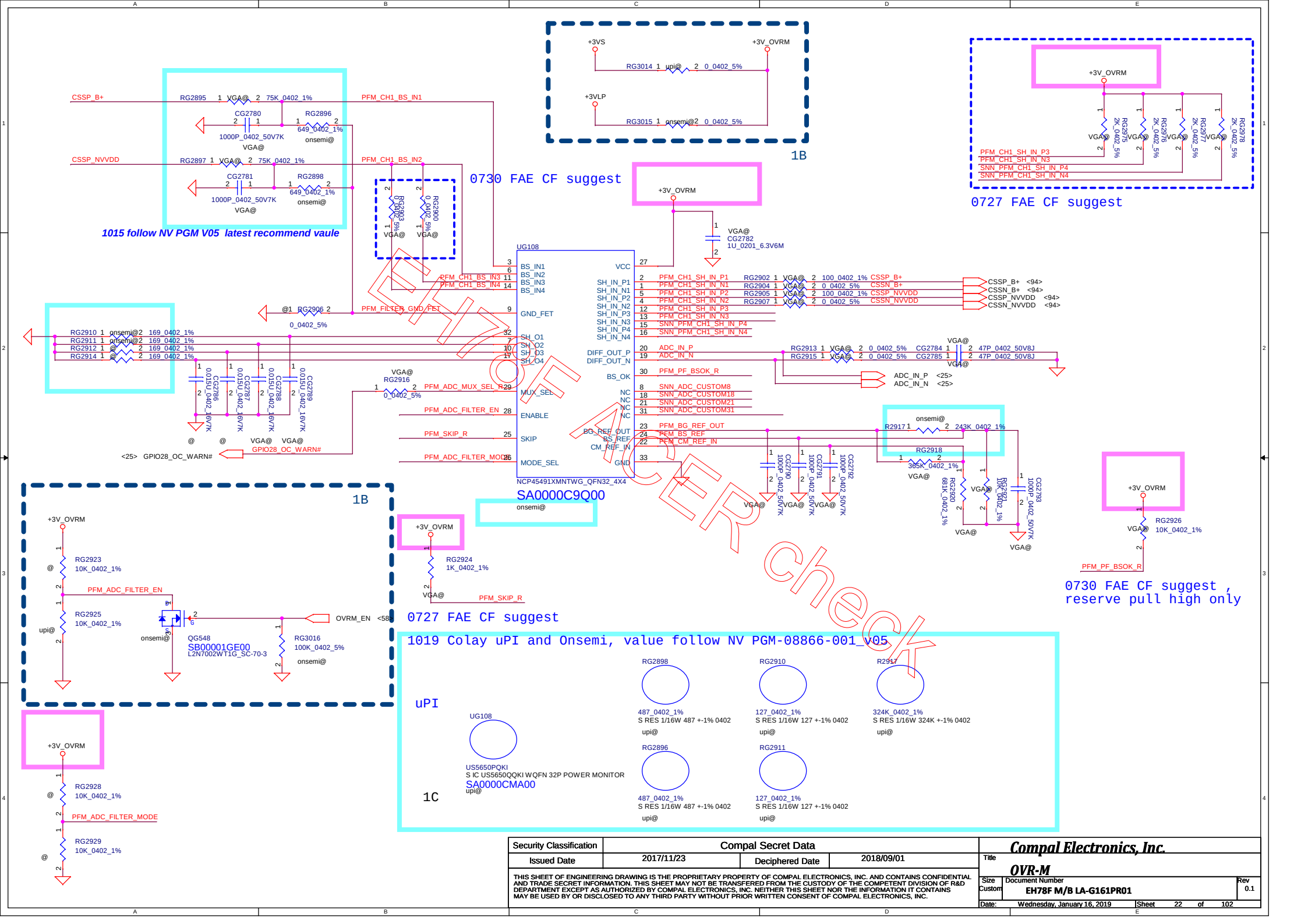
Compal Electronics, Inc.			
Title: PCH(8/8)GND/RSVD			
Size: Custom	Document Number: EH78F M/B LA-G161PR01		Rev: 0.1
Date: Wednesday, January 16, 2019	Sheet 21 of 102		



Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2018/09/01

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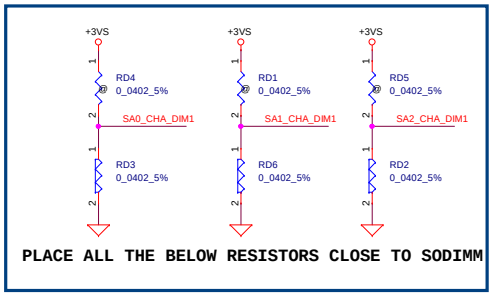
Compal Electronics, Inc.			
Title: OVR-M			
Size: Custom	Document Number: EH78F M/B LA-G161PR01		Rev: 0.1
Date: Wednesday, January 16, 2019	Sheet 22 of 102		

CHANNEL-A

TOP REVERSE (4mm)

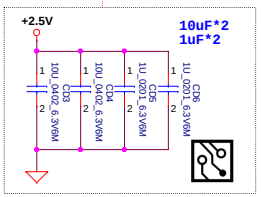
Interleaved Memory

TOP: JDIMM1 CONN Non-ECC DIMM

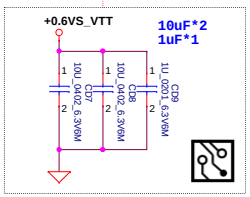


SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS: 0XA0
READ ADDRESS: 0XA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

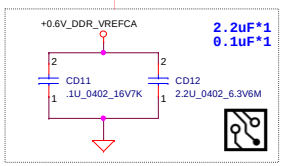
Layout Note:
Place near JDIMM1.257,259



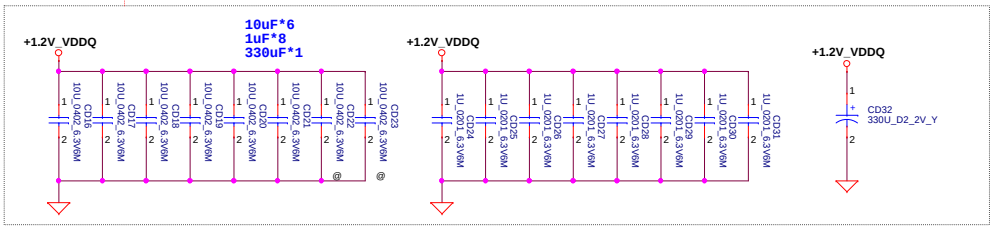
Layout Note:
Place near JDIMM1.258

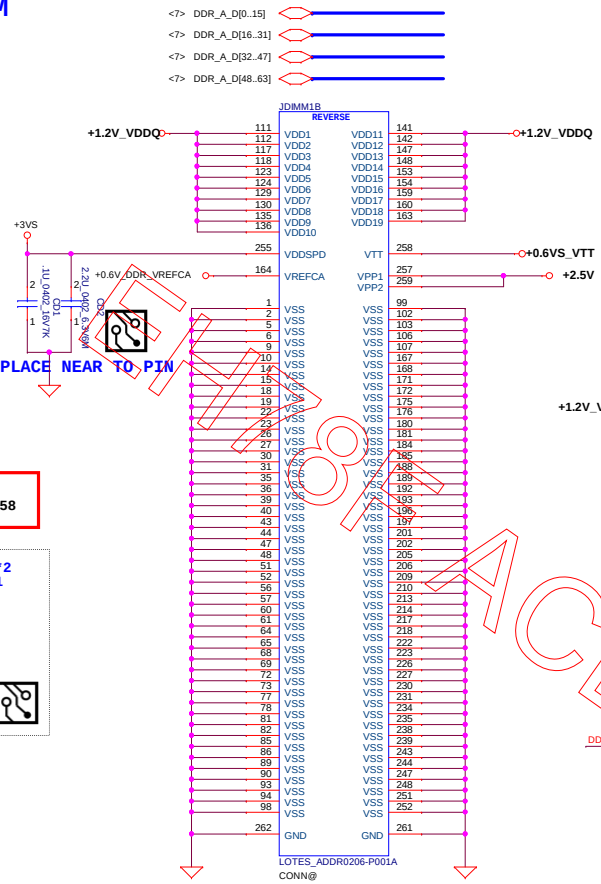


Layout Note:
PLACE THE CAP near JDIMM1. 164



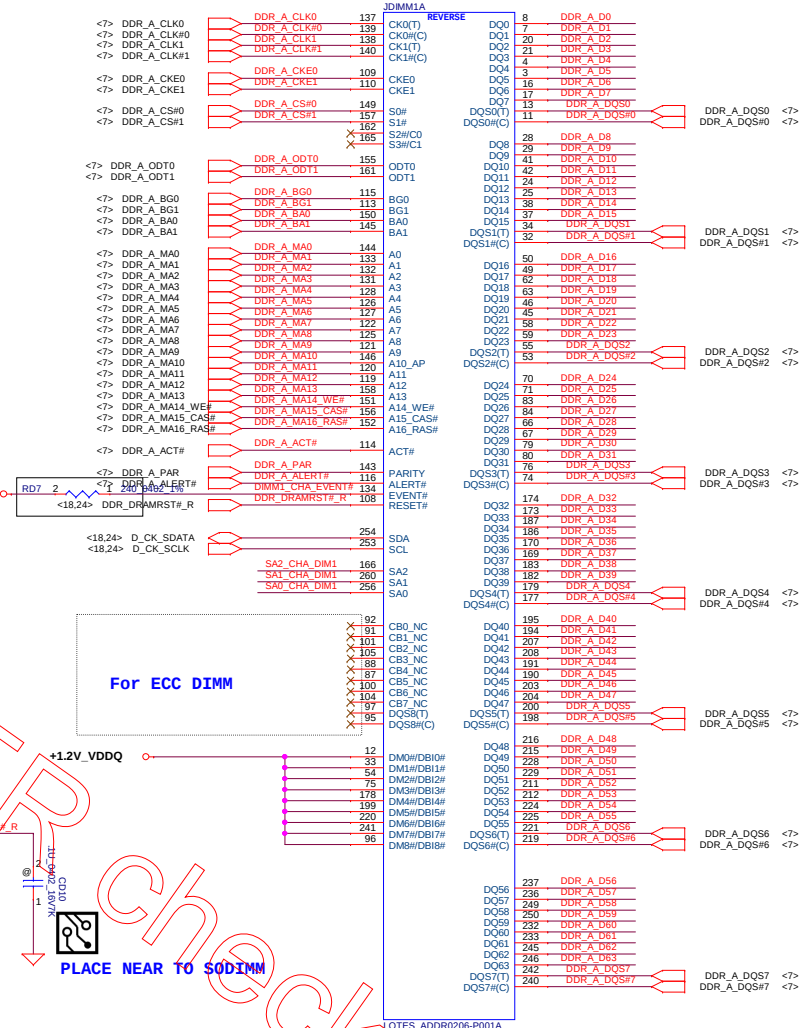
Layout Note:
Place near JDIMM1

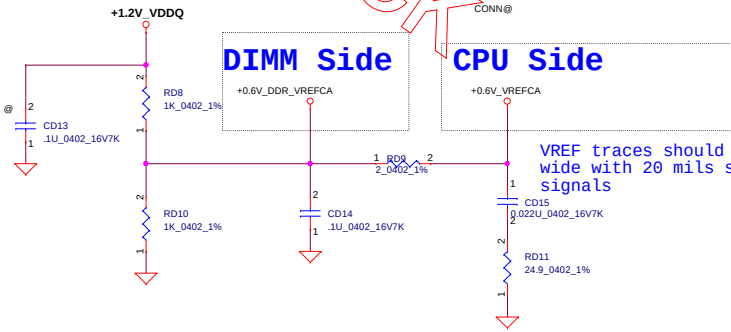




Part Number:SP07001CY00
Part Value:S SOCKET LOTES ADDR0206-P001A 260P DDR4

Connector follow 2018V-VX





VREF traces should be at least 20 mils wide with 20 mils spacing to other signals

Top ACCEPT check

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2018/09/01

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Compal Electronics, Inc.	
Title	DDRIV_CHA: DIMM0
Size	Document Number: EH78F M/B LA-G161PR01
Rev	0.1
Date:	Wednesday, January 16, 2019
Sheet	23 of 102

CHANNEL-B

TOP: JDIMM2 CONN Non-ECC DIMM

TOP REV (8mm)

Interleaved Memory

PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

Layout Note:
Place near JDIMM2.257,259

Layout Note:
Place near JDIMM2.258

Layout Note:
PLACE THE CAP WITHIN 200 MILS
FROM THE JDIMM2

Layout Note:
Place near JDIMM2

PLACE NEAR TO PIN

PLACE NEAR TO JDIMM2

Raptor

For ECC DIMM

Connector follow 2018V-VX

DIMM Side

CPU Side

VREF traces should be at least 20 mils wide with 20 mils spacing to other signals

EH78P Tester check

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2018/09/01

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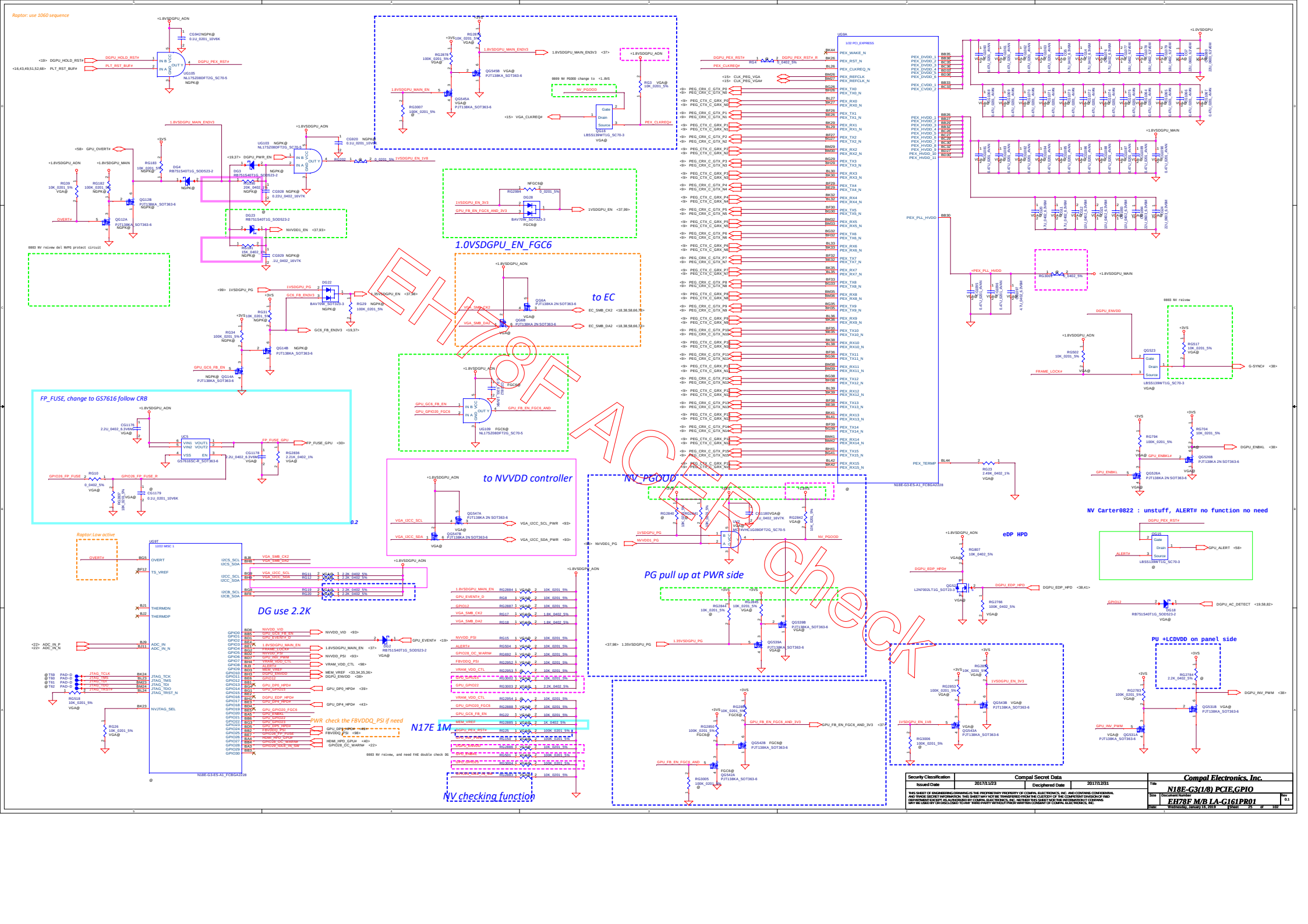
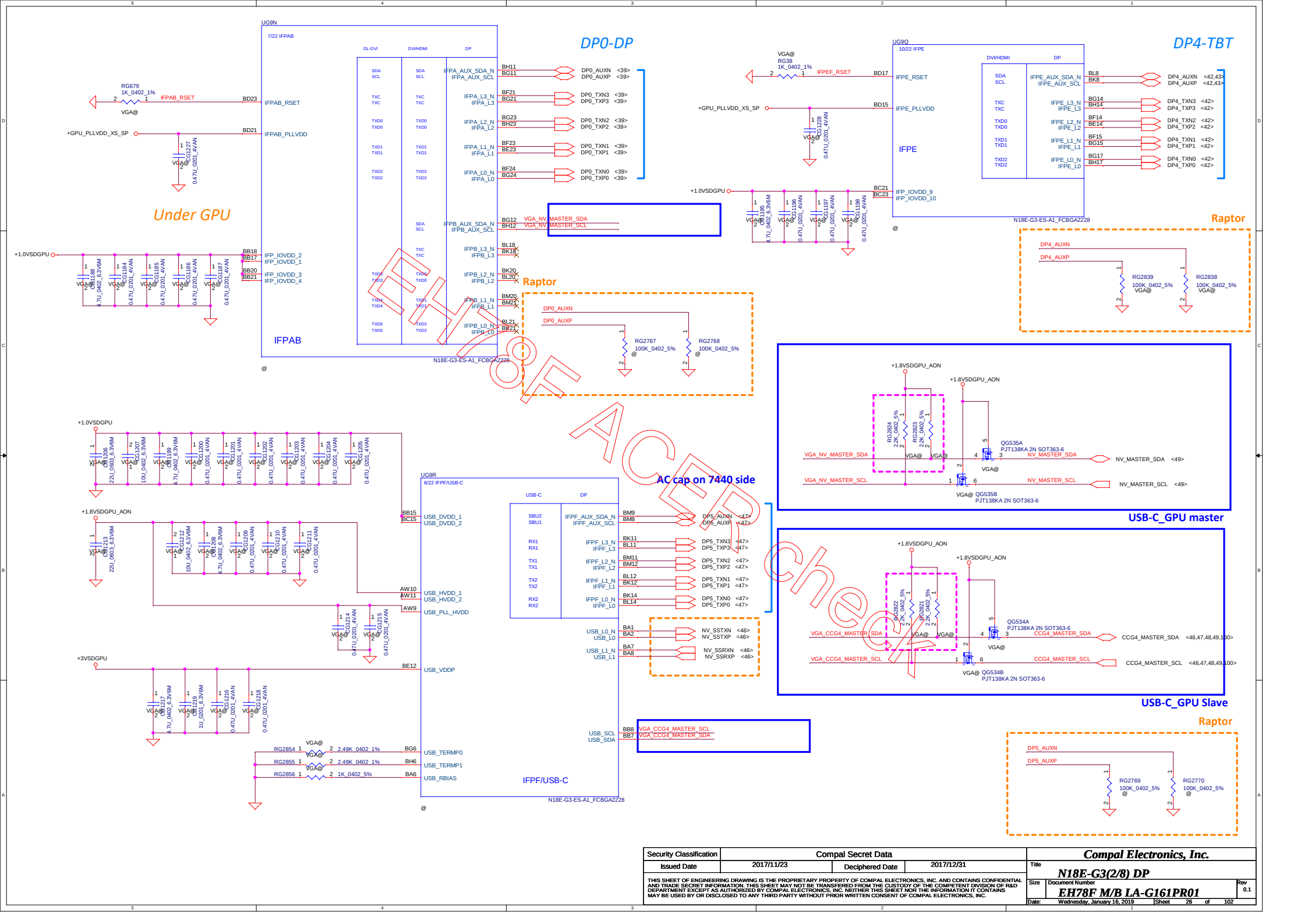
Compal Electronics, Inc.

Title: DDRIV_CHB: DIMM0

Size | Document Number: EH78F M/B LA-G161PR01 | Rev: 0.1

Date: Wednesday, January 16, 2019 | Sheet 24 of 102


Raptor: use 1060 sequence
1.0VSDGPU_EN_FGC6
to EC
FP_FUSE, change to GS7616 follow CRB
to NVVDD controller
NV_PGOOD
PG pull up at PWR side
eDP HPD
NV Carter0822 : unstuff, ALERT# no function need
DG use 2.2K
PU +LCDVDD on panel side
N17E 1M
NV checking function
PWR check the FBVDDQ_PSI if need
NV checking function
Raptor:Low active
0.2
Compal Secret Data
Compal Electronics, Inc.
N18E-G3(1/8) PCIE,GPIO
FH78F M/B LA-G161PR01
0.1
Wednesday, January 16, 2019
25
102



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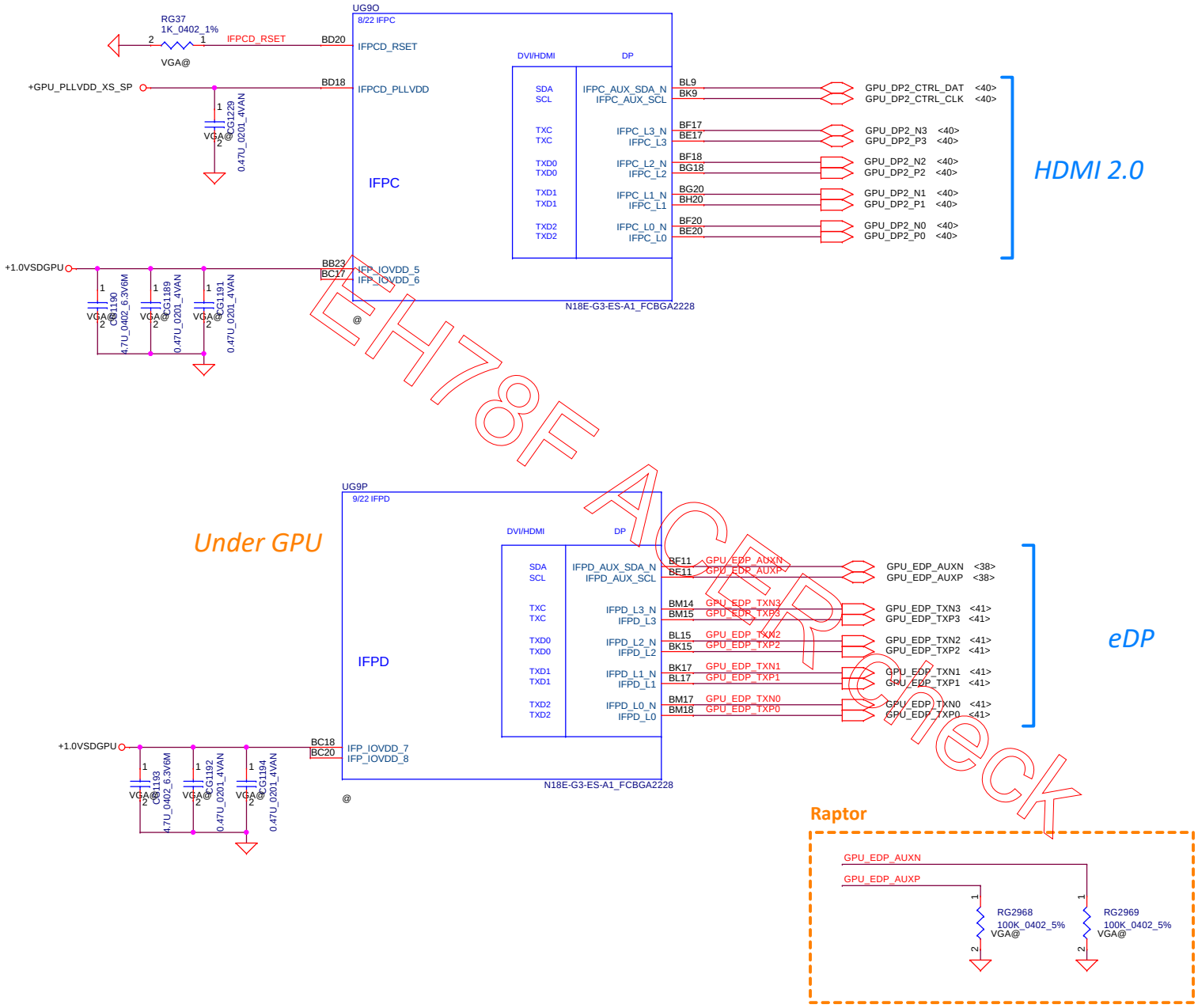
Compal Electronics, Inc.	
Title	N18E-G3(2/8) DP
Size	Document Number: EH78F M/B LA-G161PR01
Rev	0.1
Date:	Wednesday, January 16, 2019
Sheet	26 of 102



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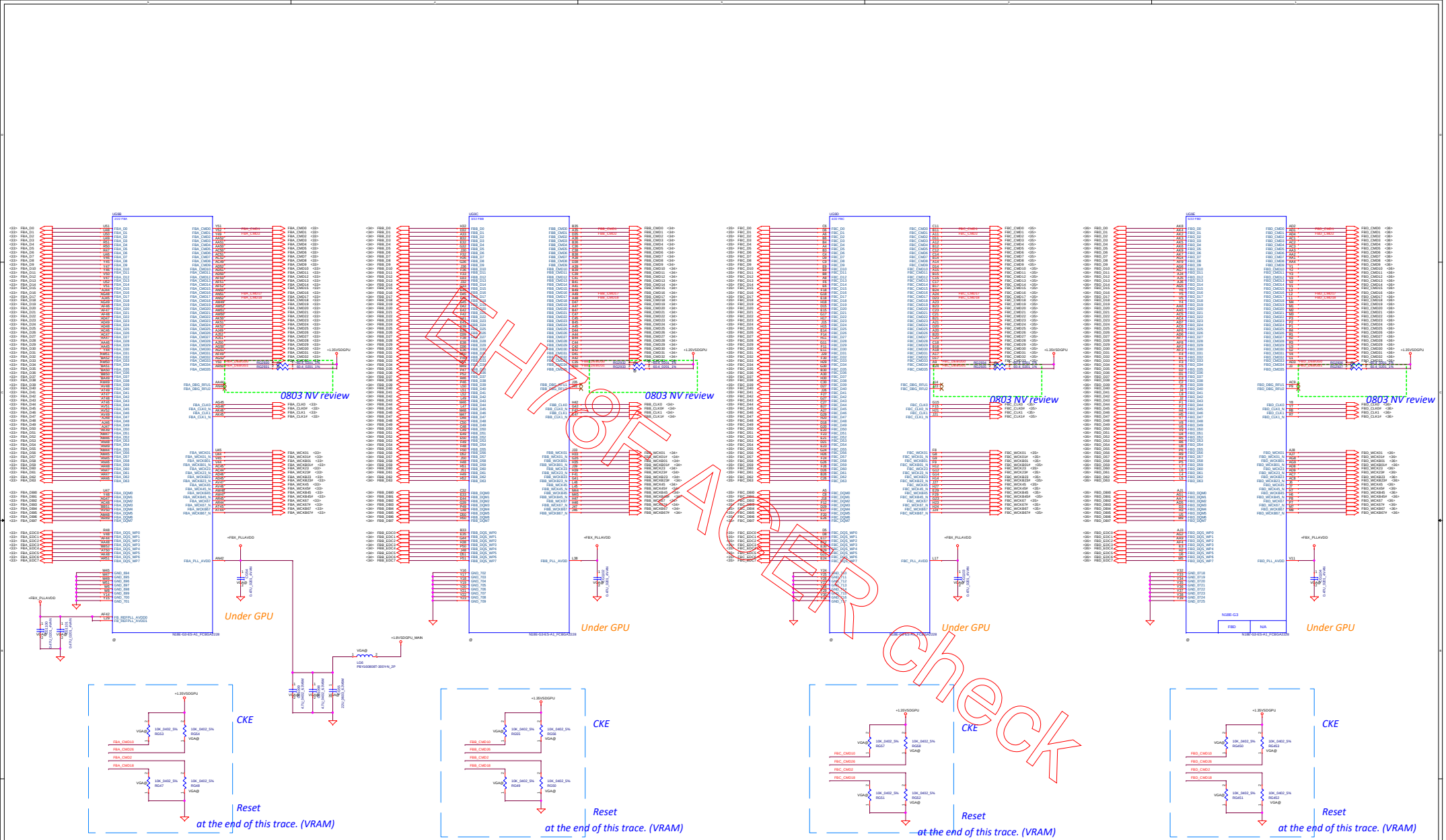
Compal Electronics, Inc.			
Title: N18E-G3(3/8) eDP,HDMI			
Size	Document Number: EH78F M/B LA-G161PR01		Rev: 0.1
Date: Wednesday, January 16, 2019	Sheet 27 of 102		



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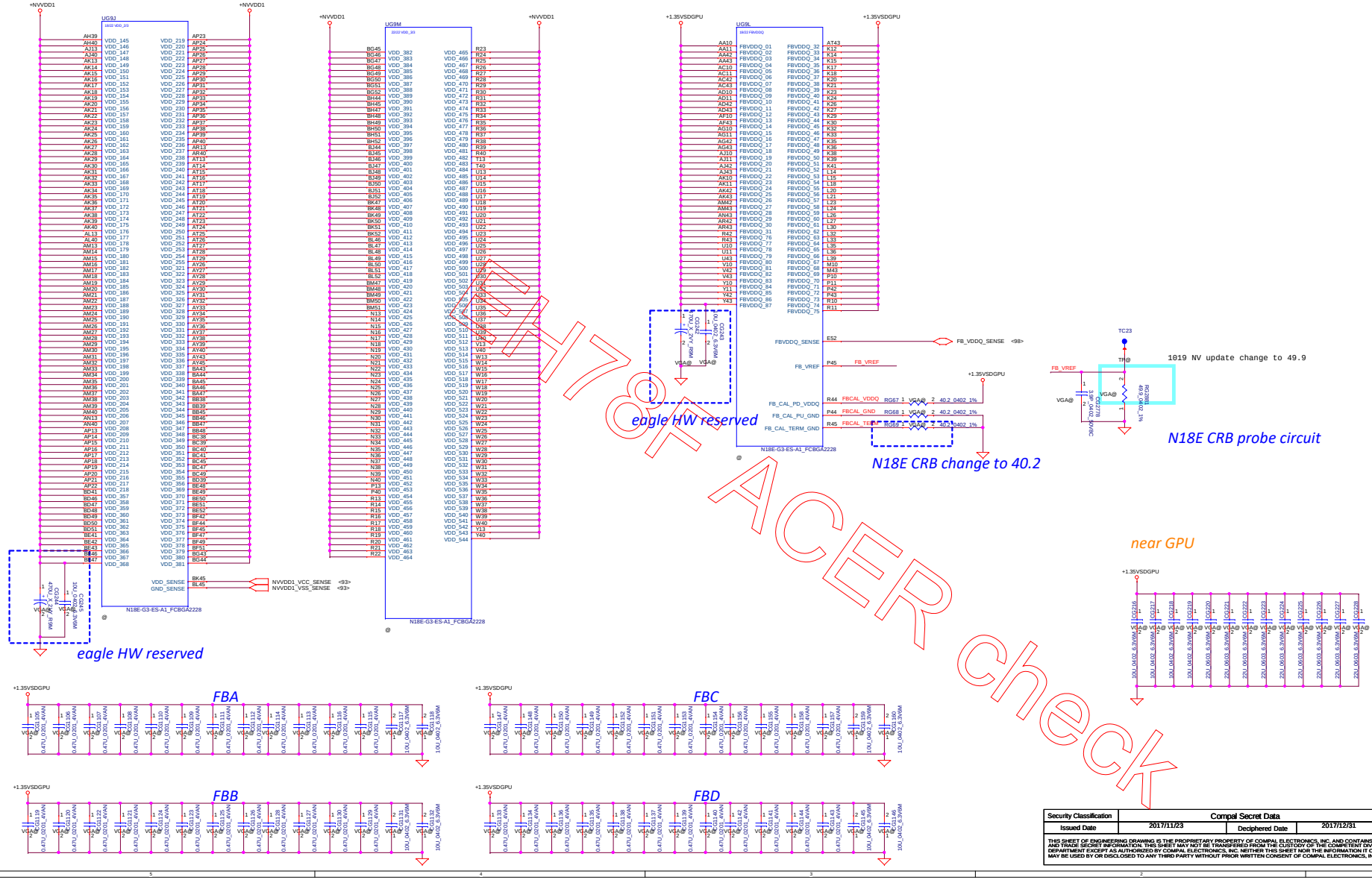
Compal Electronics, Inc.

Title: N18E-G34(48) MEM

Size: Document Number: FH78F M/B LA-G161PR01 Rev: 0.1

Date: Wednesday, January 24, 2018 Sheet 39 of 100



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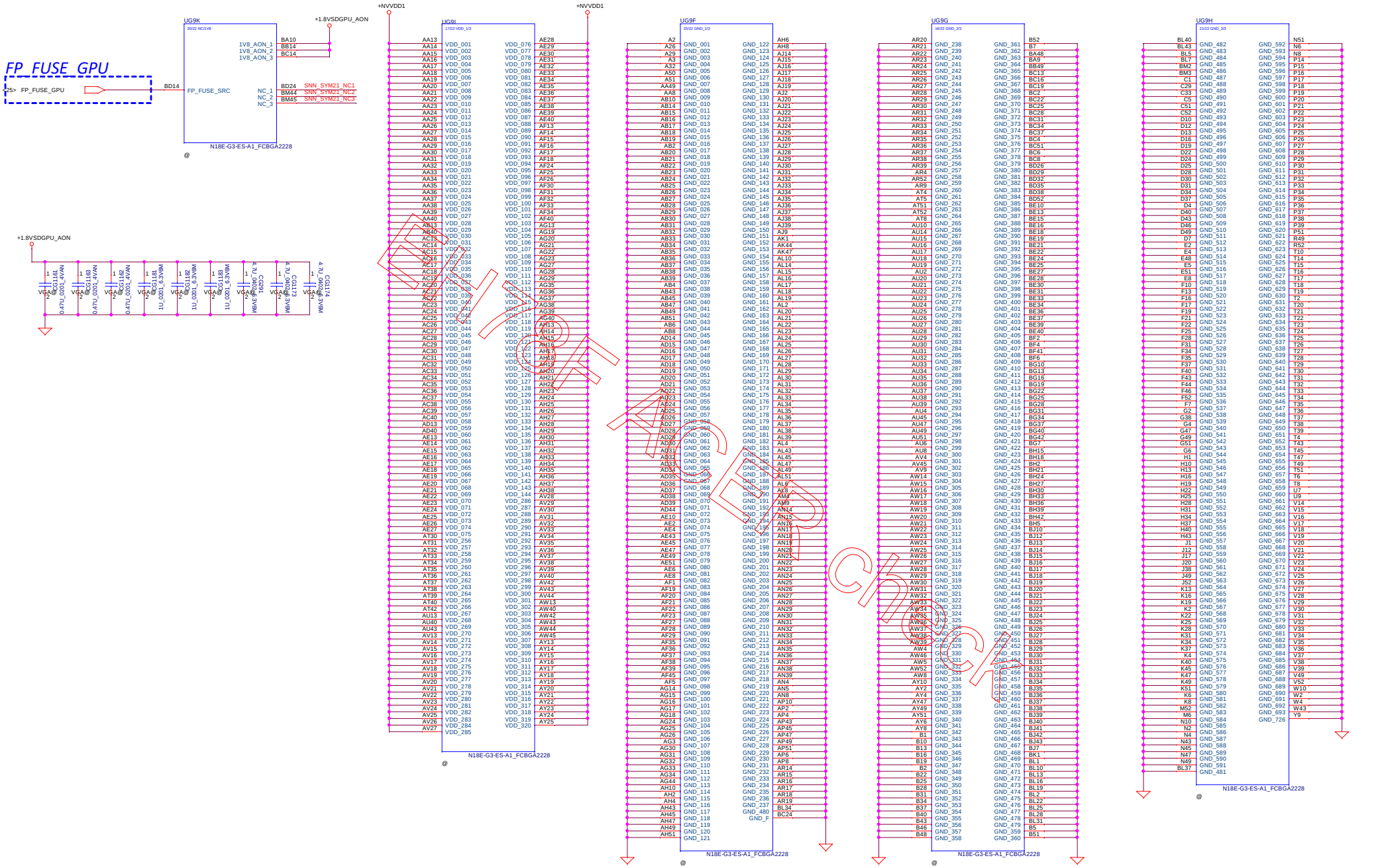
Compal Electronics, Inc.	
Title	N18E-G3(5/8) Power
Size	Document Number: EH78F M/B LA-G161PR01
Rev	0.1
Date:	Wednesday, January 16, 2019
Sheet	29 of 102



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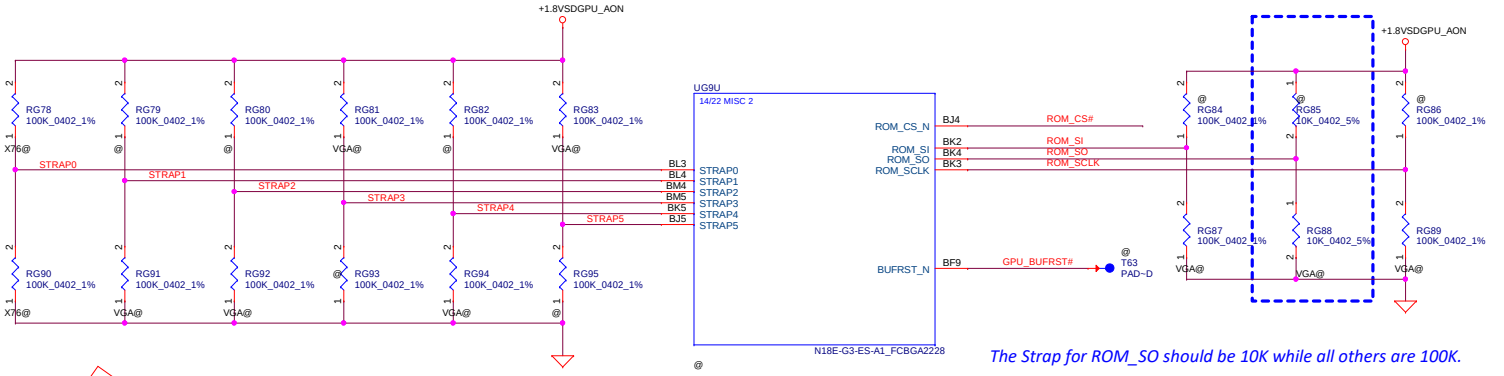


The Strap for ROM_SO should be 10K while all others are 100K.

G-sync with VGA device	Strap0 (LSB)	Strap1	Strap2	Strap3 (LSB)	Strap4	Strap5 (MSB)	ROM_SO (MSB)	ROM_SI	ROM_SCLK (LSB)
MICRON MT61K256M32JE-14:A	PU 100kOhm	PD 100kOhm	PD 100kOhm	PU 100kOhm	PD 100kOhm	PU 100kOhm	PD 10kOhm	PD 100kOhm	PD 100kOhm
Samsung K4Z80325BC-HC14	PD 100kOhm	PD 100kOhm	PD 100kOhm	PU 100kOhm	PD 100kOhm	PU 100kOhm	PD 10kOhm	PD 100kOhm	PD 100kOhm

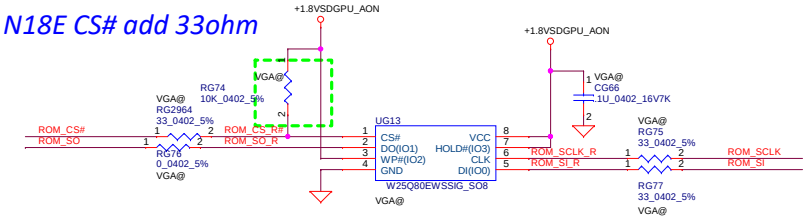
Table 1. N18E-G3 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.25V and 1.35V[2]	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	N/A	Full	Production candidate
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	N/A	Full	Production candidate

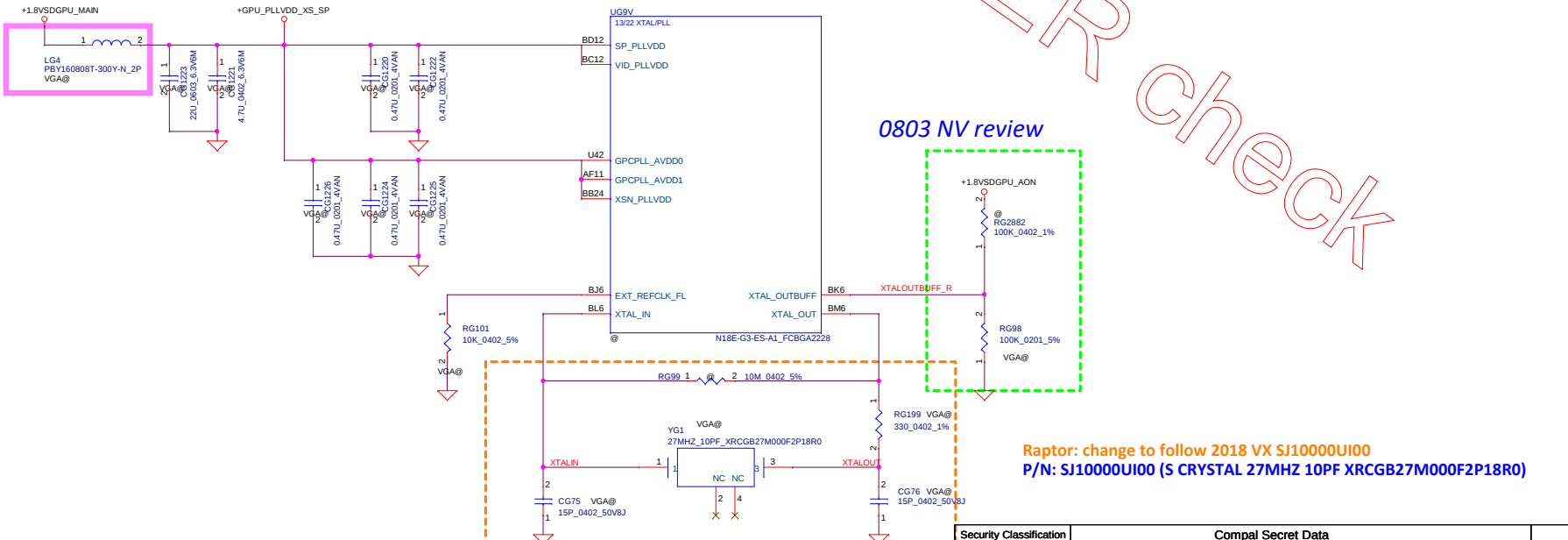
Notes:
1. For N18E-G3, the maximum allowable memory case temperature is 95 °C.
2. DVS is required. WCK: TBD

NVIDIA Confidential
2018-07-1 18:31:
ECN OF ACER check

N18E CS# add 33ohm



DGPU VBIOS ROM 8Mb



0803 NV review

Raptor: change to follow 2018 VX SJ10000UI00
P/N: SJ10000UI00 (S CRYSTAL 27MHZ 10PF XRCGB27M000F2P18R0)

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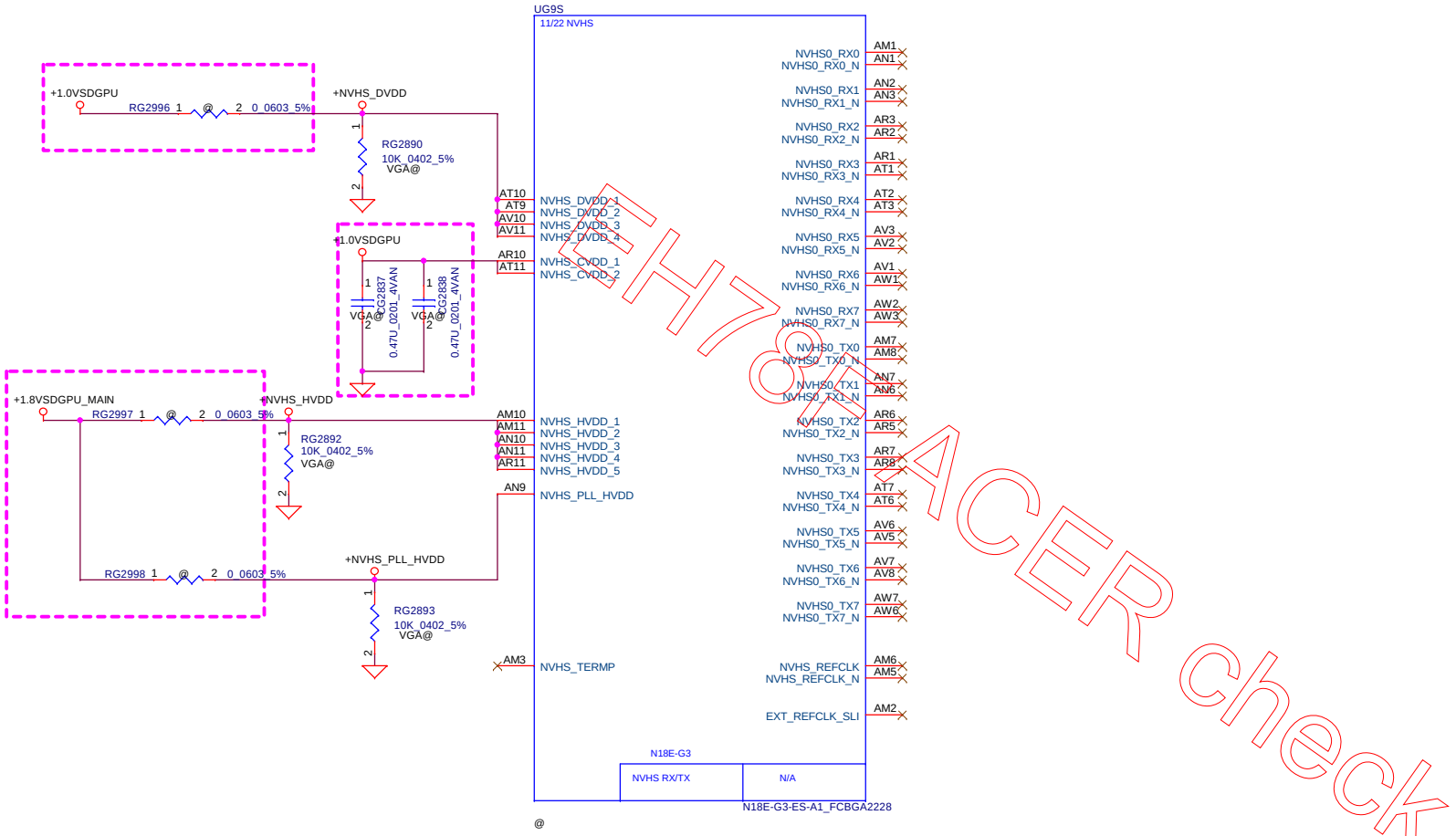
Compal Electronics, Inc.

Title: **N18E-G3(7/8) Strap,ROM**

Size | Document Number: **EH78F M/B LA-G161PR01** | Rev: 0.1

Date: Wednesday, January 16, 2019 | Sheet 31 of 102

Pull down NVHS_DVDD, NVHS_CVDD, NVHS_HVDD, NVHS_PLL_HVDD rails to GND with 10K Resistor



EH78 M/B ACER check

Security Classification	Compal Secret Data		
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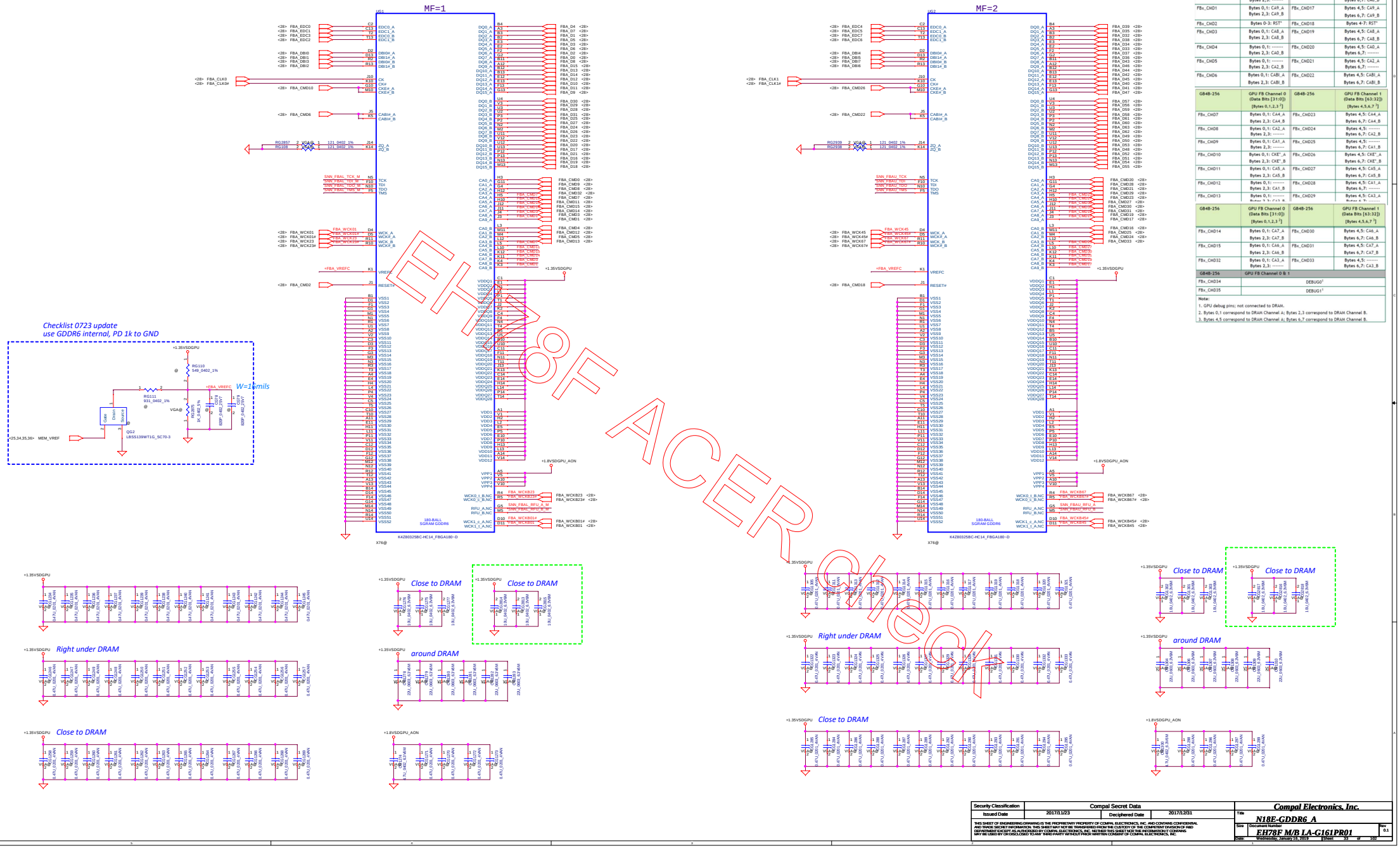
Compal Electronics, Inc.

Title: **N18E-G3(8/8) NVLINK**

Size | Document Number: **EH78F M/B LA-G161PR01** | Rev: 0.1

Date: Wednesday, January 16, 2019 | Sheet 32 of 102



GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [2]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [2]]
FBx_CMD0	Bytes 0, 1: CA0_A Bytes 2, 3: -------	FBx_CMD16	Bytes 4, 5: ------- Bytes 6, 7: CA0_B
FBx_CMD1	Bytes 0, 1: CA9_A Bytes 2, 3: CA9_B	FBx_CMD17	Bytes 4, 5: CA9_A Bytes 6, 7: CA9_B
FBx_CMD2	Byte 0-3: RST*	FBx_CMD18	Bytes 4-7: RST*
FBx_CMD3	Bytes 0, 1: CA8_A Bytes 2, 3: CA8_B	FBx_CMD19	Bytes 4, 5: CA8_A Bytes 6, 7: CA8_B
FBx_CMD4	Bytes 0, 1: ------- Bytes 2, 3: CA0_B	FBx_CMD20	Bytes 4, 5: CA0_A Bytes 6, 7: -------
FBx_CMD5	Bytes 0, 1: ------- Bytes 2, 3: CA2_B	FBx_CMD21	Bytes 4, 5: CA2_A Bytes 6, 7: -------
FBx_CMD6	Bytes 0, 1: CABI_A Bytes 2, 3: CABI_B	FBx_CMD22	Bytes 4, 5: CABI_A Bytes 6, 7: CABI_B

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [2]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [2]]
FBx_CMD7	Bytes 0, 1: CA4_A Bytes 2, 3: CA4_B	FBx_CMD23	Bytes 4, 5: CA4_A Bytes 6, 7: CA4_B
FBx_CMD8	Bytes 0, 1: CA2_A Bytes 2, 3: -------	FBx_CMD24	Bytes 4, 5: ------- Bytes 6, 7: CA2_B
FBx_CMD9	Bytes 0, 1: CA1_A Bytes 2, 3: -------	FBx_CMD25	Bytes 4, 5: ------- Bytes 6, 7: CA1_B
FBx_CMD10	Bytes 0, 1: CKE*_A Bytes 2, 3: CKE*_B	FBx_CMD26	Bytes 4, 5: CKE*_A Bytes 6, 7: CKE*_B
FBx_CMD11	Bytes 0, 1: CA5_A Bytes 2, 3: CA5_B	FBx_CMD27	Bytes 4, 5: CA5_A Bytes 6, 7: CA5_B
FBx_CMD12	Bytes 0, 1: ------- Bytes 2, 3: CA1_B	FBx_CMD28	Bytes 4, 5: CA1_A Bytes 6, 7: -------
FBx_CMD13	Bytes 0, 1: ------- Bytes 2, 3: CA3_B	FBx_CMD29	Bytes 4, 5: CA3_A Bytes 6, 7: -------

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [2]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [2]]
FBx_CMD14	Bytes 0, 1: CA7_A Bytes 2, 3: CA7_B	FBx_CMD30	Bytes 4, 5: CA6_A Bytes 6, 7: CA6_B
FBx_CMD15	Bytes 0, 1: CA6_A Bytes 2, 3: CA6_B	FBx_CMD31	Bytes 4, 5: CA7_A Bytes 6, 7: CA7_B
FBx_CMD32	Bytes 0, 1: CA3_A Bytes 2, 3: -------	FBx_CMD33	Bytes 4, 5: ------- Bytes 6, 7: CA3_B

GB4B-256	GPU FB Channel 0 B 1
FBx_CMD34	DEBUG0 [1]
FBx_CMD35	DEBUG1 [1]

Note:
1. GPU debug pins; not connected to DRAM.
2. Bytes 0,1 correspond to DRAM Channel A; Bytes 2,3 correspond to DRAM Channel B.
3. Bytes 4,5 correspond to DRAM Channel A; Bytes 6,7 correspond to DRAM Channel B.

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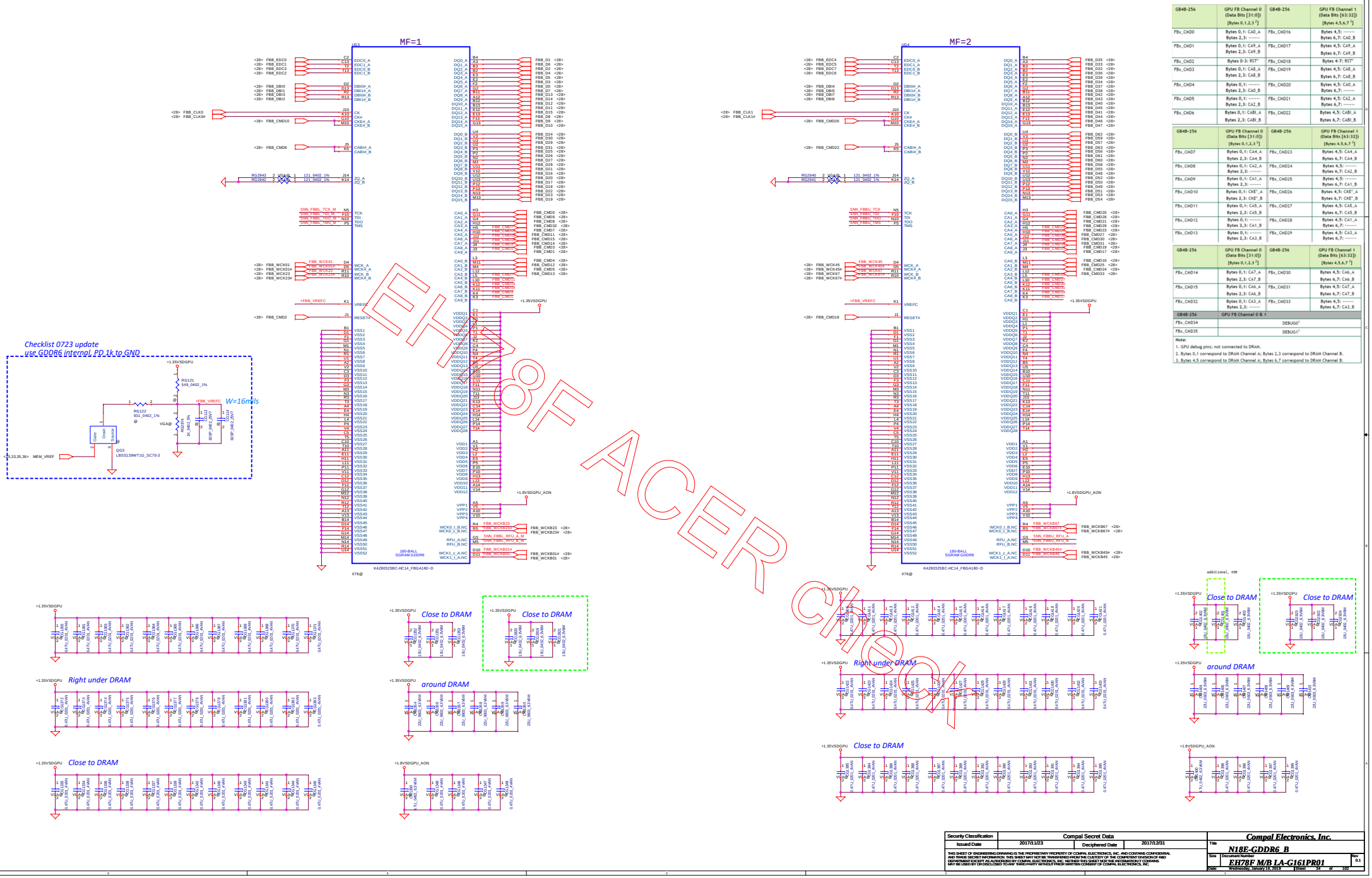
Compal Electronics, Inc.

Title: N18E-GDDR6_A

Size: Document Number: EH78F M/B LA-G161PR01 Rev: 0.1

Date: Wednesday, January 10, 2018 Sheet 33 of 102



GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [2]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [3]]
FBx_CMD0	Bytes 0, 1: CA0_A Bytes 2, 3: -------	FBx_CMD16	Bytes 4, 5: ------- Bytes 6, 7: CA0_B
FBx_CMD1	Bytes 0, 1: CA9_A Bytes 2, 3: CA9_B	FBx_CMD17	Bytes 4, 5: CA9_A Bytes 6, 7: CA9_B
FBx_CMD2	Bytes 0-3: RST*	FBx_CMD18	Bytes 4-7: RST*
FBx_CMD3	Bytes 0, 1: CA8_A Bytes 2, 3: CA8_B	FBx_CMD19	Bytes 4, 5: CA8_A Bytes 6, 7: CA8_B
FBx_CMD4	Bytes 0, 1: ------- Bytes 2, 3: CA0_B	FBx_CMD20	Bytes 4, 5: CA0_A Bytes 6, 7: -------
FBx_CMD5	Bytes 0, 1: ------- Bytes 2, 3: CA2_B	FBx_CMD21	Bytes 4, 5: CA2_A Bytes 6, 7: -------
FBx_CMD6	Bytes 0, 1: CABI_A Bytes 2, 3: CABI_B	FBx_CMD22	Bytes 4, 5: CABI_A Bytes 6, 7: CABI_B

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [2]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [3]]
FBx_CMD7	Bytes 0, 1: CA4_A Bytes 2, 3: CA4_B	FBx_CMD23	Bytes 4, 5: CA4_A Bytes 6, 7: CA4_B
FBx_CMD8	Bytes 0, 1: CA2_A Bytes 2, 3: -------	FBx_CMD24	Bytes 4, 5: ------- Bytes 6, 7: CA2_B
FBx_CMD9	Bytes 0, 1: CA1_A Bytes 2, 3: -------	FBx_CMD25	Bytes 4, 5: ------- Bytes 6, 7: CA1_B
FBx_CMD10	Bytes 0, 1: CKE*_A Bytes 2, 3: CKE*_B	FBx_CMD26	Bytes 4, 5: CKE*_A Bytes 6, 7: CKE*_B
FBx_CMD11	Bytes 0, 1: CA5_A Bytes 2, 3: CA5_B	FBx_CMD27	Bytes 4, 5: CA5_A Bytes 6, 7: CA5_B
FBx_CMD12	Bytes 0, 1: ------- Bytes 2, 3: CA1_B	FBx_CMD28	Bytes 4, 5: CA1_A Bytes 6, 7: -------
FBx_CMD13	Bytes 0, 1: ------- Bytes 2, 3: CA3_B	FBx_CMD29	Bytes 4, 5: CA3_A Bytes 6, 7: -------

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [2]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [3]]
FBx_CMD14	Bytes 0, 1: CA7_A Bytes 2, 3: CA7_B	FBx_CMD30	Bytes 4, 5: CA6_A Bytes 6, 7: CA6_B
FBx_CMD15	Bytes 0, 1: CA6_A Bytes 2, 3: CA6_B	FBx_CMD31	Bytes 4, 5: CA7_A Bytes 6, 7: CA7_B
FBx_CMD32	Bytes 0, 1: CA3_A Bytes 2, 3: -------	FBx_CMD33	Bytes 4, 5: ------- Bytes 6, 7: CA3_B

GB4B-256	GPU FB Channel 0 B 1
FBx_CMD34	DEBUG0[1]
FBx_CMD35	DEBUG1[1]

Note:
1. GPU debug pins; not connected to DRAM.
2. Bytes 0,1 correspond to DRAM Channel A; Bytes 2,3 correspond to DRAM Channel B.
3. Bytes 4,5 correspond to DRAM Channel A; Bytes 6,7 correspond to DRAM Channel B.

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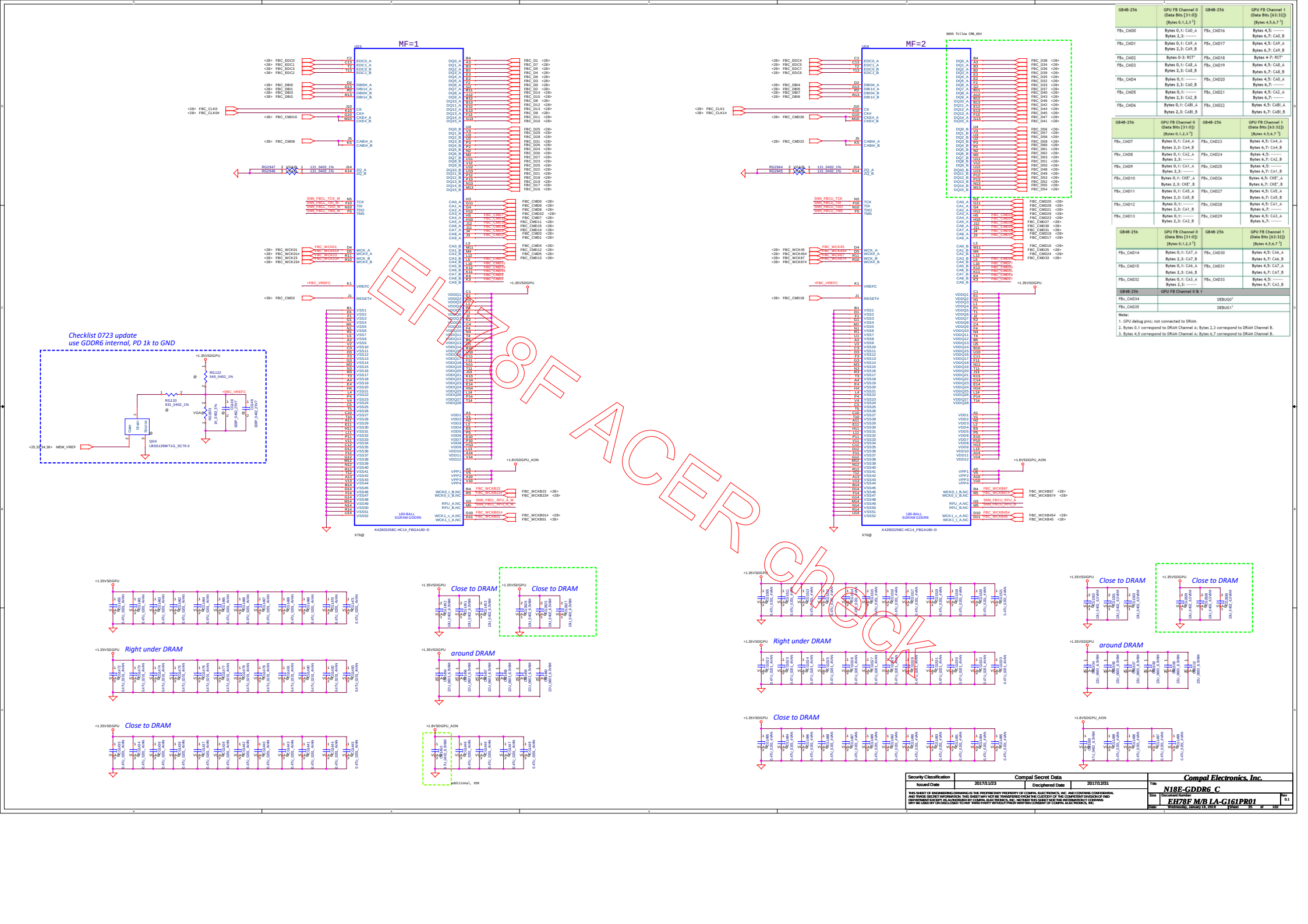
Title: N18E-GDDR6_B

Size: Document Number: EH78F M/B LA-G161PR01 Rev: 0.1

Date: Wednesday, January 16, 2019 Sheet 34 of 102



GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [7]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [7]]
FBx_CMD0	Bytes 0,1: CA0_A Bytes 2,3: -------	FBx_CMD16	Bytes 4,5: ------- Bytes 6,7: CA0_B
FBx_CMD1	Bytes 0,1: CA9_A Bytes 2,3: CA9_B	FBx_CMD17	Bytes 4,5: CA9_A Bytes 6,7: CA9_B
FBx_CMD2	Bytes 0-3: RST#	FBx_CMD18	Bytes 4-7: RST#
FBx_CMD3	Bytes 0,1: CA8_A Bytes 2,3: CA8_B	FBx_CMD19	Bytes 4,5: CA8_A Bytes 6,7: CA8_B
FBx_CMD4	Bytes 0,1: ------- Bytes 2,3: CA0_B	FBx_CMD20	Bytes 4,5: CA0_A Bytes 6,7: -------
FBx_CMD5	Bytes 0,1: ------- Bytes 2,3: CA2_B	FBx_CMD21	Bytes 4,5: CA2_A Bytes 6,7: -------
FBx_CMD6	Bytes 0,1: CABI_A Bytes 2,3: CABI_B	FBx_CMD22	Bytes 4,5: CABI_A Bytes 6,7: CABI_B

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [7]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [7]]
FBx_CMD7	Bytes 0,1: CA4_A Bytes 2,3: CA4_B	FBx_CMD23	Bytes 4,5: CA4_A Bytes 6,7: CA4_B
FBx_CMD8	Bytes 0,1: CA2_A Bytes 2,3: -------	FBx_CMD24	Bytes 4,5: ------- Bytes 6,7: CA2_B
FBx_CMD9	Bytes 0,1: CA1_A Bytes 2,3: -------	FBx_CMD25	Bytes 4,5: ------- Bytes 6,7: CA1_B
FBx_CMD10	Bytes 0,1: CKE#_A Bytes 2,3: CKE#_B	FBx_CMD26	Bytes 4,5: CKE#_A Bytes 6,7: CKE#_B
FBx_CMD11	Bytes 0,1: CA5_A Bytes 2,3: CA5_B	FBx_CMD27	Bytes 4,5: CA5_A Bytes 6,7: CA5_B
FBx_CMD12	Bytes 0,1: ------- Bytes 2,3: CA1_B	FBx_CMD28	Bytes 4,5: CA1_A Bytes 6,7: -------
FBx_CMD13	Bytes 0,1: ------- Bytes 2,3: CA3_B	FBx_CMD29	Bytes 4,5: CA3_A Bytes 6,7: -------

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [7]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [7]]
FBx_CMD14	Bytes 0,1: CA7_A Bytes 2,3: CA7_B	FBx_CMD30	Bytes 4,5: CA6_A Bytes 6,7: CA6_B
FBx_CMD15	Bytes 0,1: CA6_A Bytes 2,3: CA6_B	FBx_CMD31	Bytes 4,5: CA7_A Bytes 6,7: CA7_B
FBx_CMD32	Bytes 0,1: CA3_A Bytes 2,3: -------	FBx_CMD33	Bytes 4,5: ------- Bytes 6,7: CA3_B

GB4B-256	GPU FB Channel 0 B 1
FBx_CMD34	DEBUG0[1]
FBx_CMD35	DEBUG1[1]

Note:
1. GPU debug pins; not connected to DRAM.
2. Bytes 0,1 correspond to DRAM Channel A; Bytes 2,3 correspond to DRAM Channel B.
3. Bytes 4,5 correspond to DRAM Channel A; Bytes 6,7 correspond to DRAM Channel B.

ITEM 8F ACER Confidential

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

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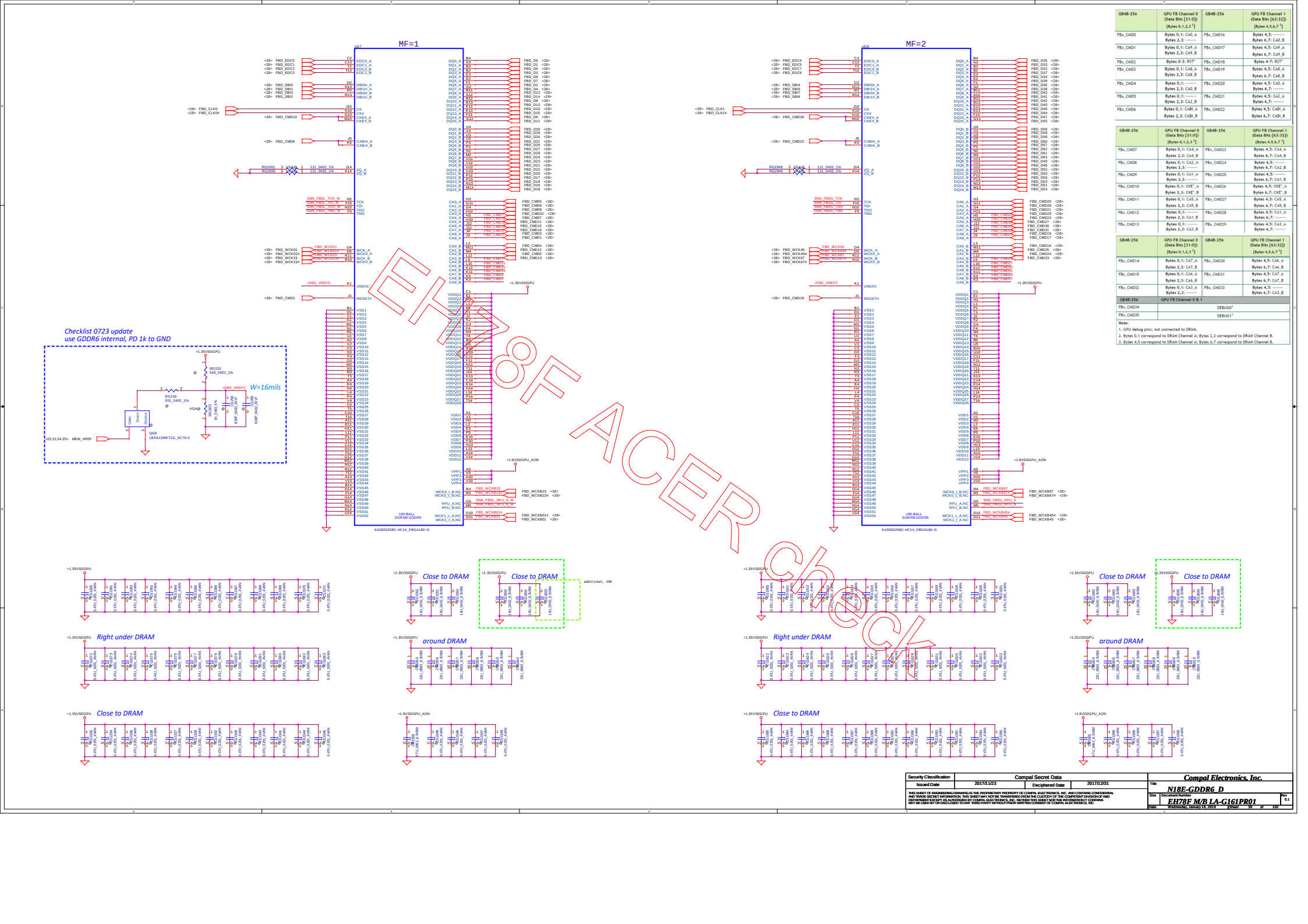
Compal Electronics, Inc.			
Title	N18E-GDDR6_C		
Size	Document Number		Rev
	EH78F M/B LA-G161PR01		0.1
Date: Wednesday, January 10, 2019	Sheet 35 of 102		



GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [2]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [2]]
FBx_CMD0	Bytes 0, 1: CA0_A Bytes 2, 3: ------	FBx_CMD16	Bytes 4, 5: ------ Bytes 6, 7: CA0_B
FBx_CMD1	Bytes 0, 1: CA9_A Bytes 2, 3: CA9_B	FBx_CMD17	Bytes 4, 5: CA9_A Bytes 6, 7: CA9_B
FBx_CMD2	Bytes 0-3: RST*	FBx_CMD18	Bytes 4-7: RST*
FBx_CMD3	Bytes 0, 1: CA8_A Bytes 2, 3: CA8_B	FBx_CMD19	Bytes 4, 5: CA8_A Bytes 6, 7: CA8_B
FBx_CMD4	Bytes 0, 1: ------ Bytes 2, 3: CA0_B	FBx_CMD20	Bytes 4, 5: CA0_A Bytes 6, 7: ------
FBx_CMD5	Bytes 0, 1: ------ Bytes 2, 3: CA2_B	FBx_CMD21	Bytes 4, 5: CA2_A Bytes 6, 7: ------
FBx_CMD6	Bytes 0, 1: CABI_A Bytes 2, 3: CABI_B	FBx_CMD22	Bytes 4, 5: CABI_A Bytes 6, 7: CABI_B

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [2]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [2]]
FBx_CMD7	Bytes 0, 1: CA4_A Bytes 2, 3: CA4_B	FBx_CMD23	Bytes 4, 5: CA4_A Bytes 6, 7: CA4_B
FBx_CMD8	Bytes 0, 1: CA2_A Bytes 2, 3: ------	FBx_CMD24	Bytes 4, 5: ------ Bytes 6, 7: CA2_B
FBx_CMD9	Bytes 0, 1: CA1_A Bytes 2, 3: ------	FBx_CMD25	Bytes 4, 5: ------ Bytes 6, 7: CA1_B
FBx_CMD10	Bytes 0, 1: CKE*_A Bytes 2, 3: CKE*_B	FBx_CMD26	Bytes 4, 5: CKE*_A Bytes 6, 7: CKE*_B
FBx_CMD11	Bytes 0, 1: CA5_A Bytes 2, 3: CA5_B	FBx_CMD27	Bytes 4, 5: CA5_A Bytes 6, 7: CA5_B
FBx_CMD12	Bytes 0, 1: ------ Bytes 2, 3: CA1_B	FBx_CMD28	Bytes 4, 5: CA1_A Bytes 6, 7: ------
FBx_CMD13	Bytes 0, 1: ------ Bytes 2, 3: CA3_B	FBx_CMD29	Bytes 4, 5: CA3_A Bytes 6, 7: ------

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [2]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [2]]
FBx_CMD14	Bytes 0, 1: CA7_A Bytes 2, 3: CA7_B	FBx_CMD30	Bytes 4, 5: CA6_A Bytes 6, 7: CA6_B
FBx_CMD15	Bytes 0, 1: CA6_A Bytes 2, 3: CA6_B	FBx_CMD31	Bytes 4, 5: CA7_A Bytes 6, 7: CA7_B
FBx_CMD32	Bytes 0, 1: CA3_A Bytes 2, 3: ------	FBx_CMD33	Bytes 4, 5: ------ Bytes 6, 7: CA3_B

GB4B-256	GPU FB Channel 0 & 1
FBx_CMD34	DEBUG0[1]
FBx_CMD35	DEBUG1[1]

Note:
1. GPU debug pins; not connected to DRAM.
2. Bytes 0,1 correspond to DRAM Channel A; Bytes 2,3 correspond to DRAM Channel B.
3. Bytes 4,5 correspond to DRAM Channel A; Bytes 6,7 correspond to DRAM Channel B.

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

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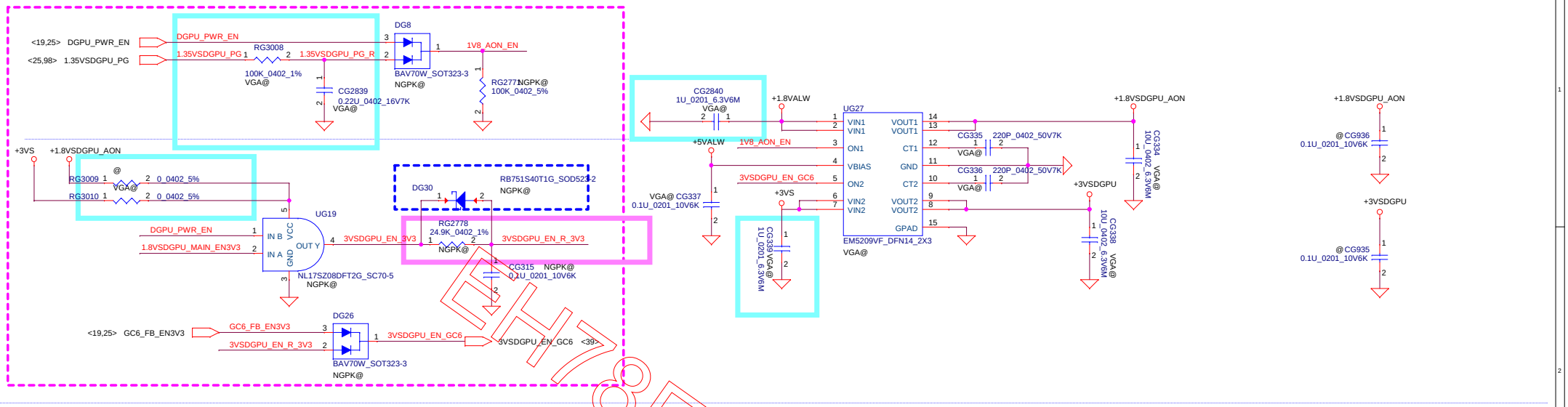
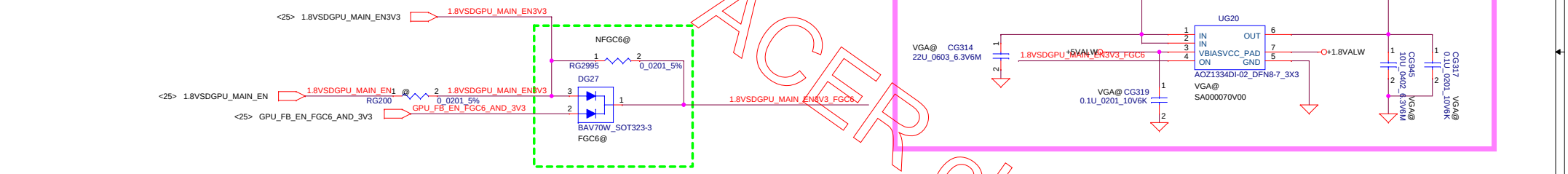
Compal Electronics, Inc.	
Title	N18E-GDDR6_D
Size	Document Number: EH78F M/B LA-G161PR01
Rev	0.1
Date: Wednesday, January 10, 2019	Sheet 35 of 102

+1.8VALW to +1.8VSDGPU_AON & +3VS to +3VSDGPU

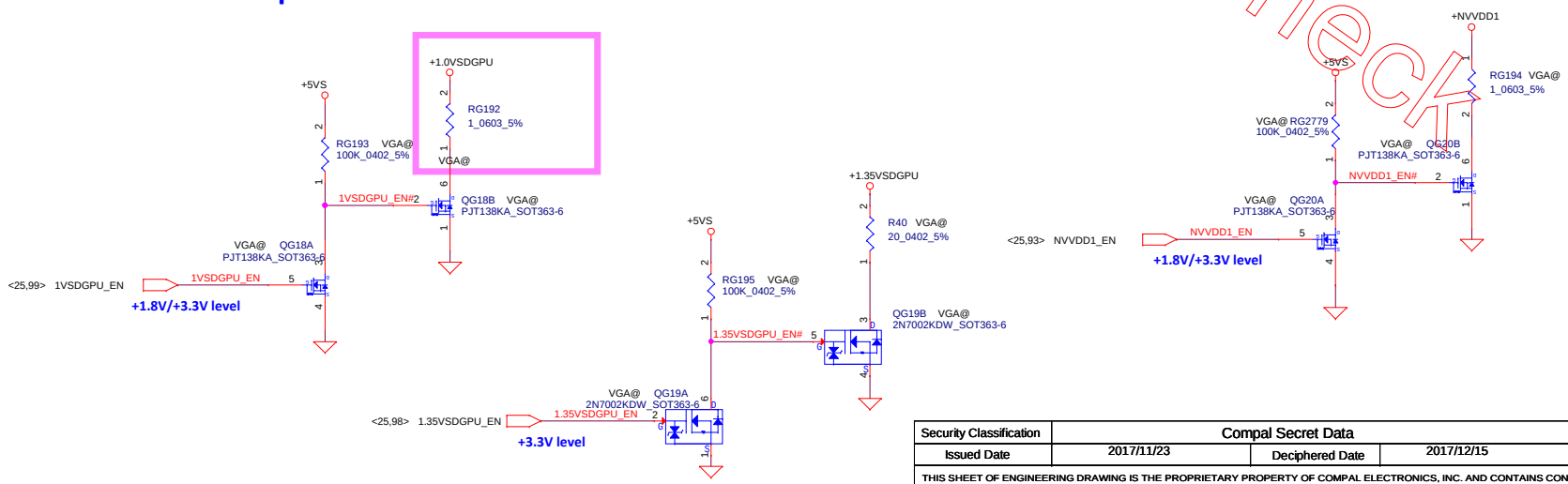
<0.2 modify>



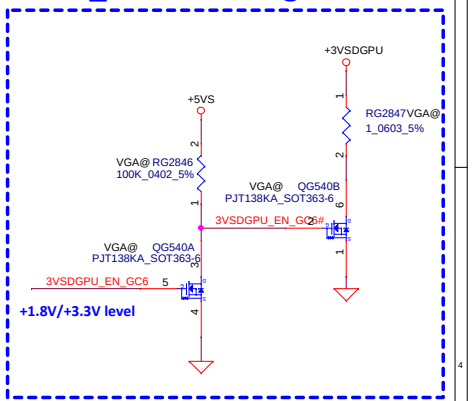
+1.8VALW to +1.8VSDGPU_MAIN



For Power down sequence



+3VSD_GPU discharge if need



EH78F ACER check

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/15

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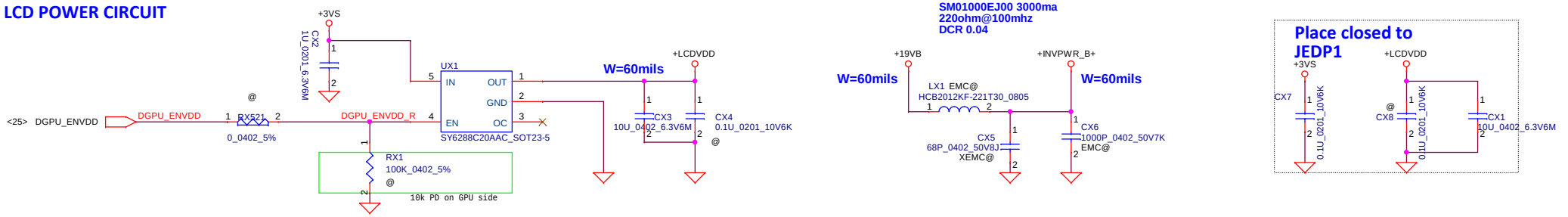
Compal Electronics, Inc.

Title: N18E-GPU Power control

Size | Document Number: EH78F M/B LA-G161PR01 | Rev: 0.1

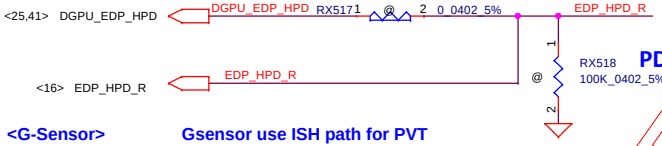
Date: Wednesday, January 16, 2019 | Sheet 37 of 102

LCD POWER CIRCUIT

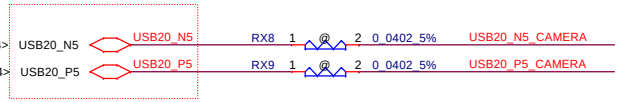


SM01000EJ00 3000ma
220ohm@100mhz
DCR 0.04

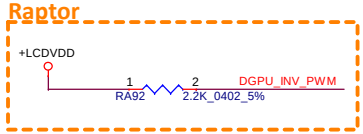
Place closed to JEDP1



Camera

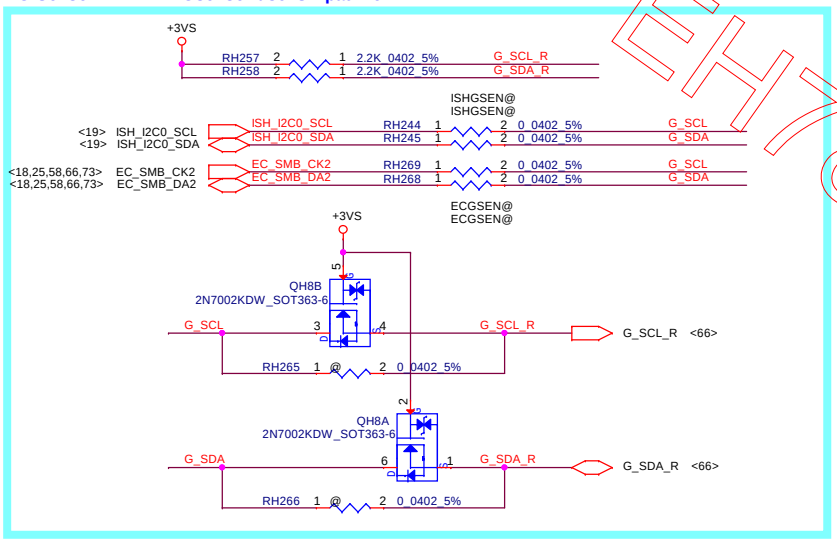


Raptor

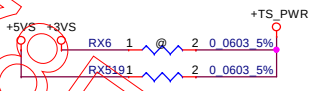


<G-Sensor>

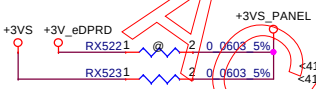
Gsensor use ISH path for PVT



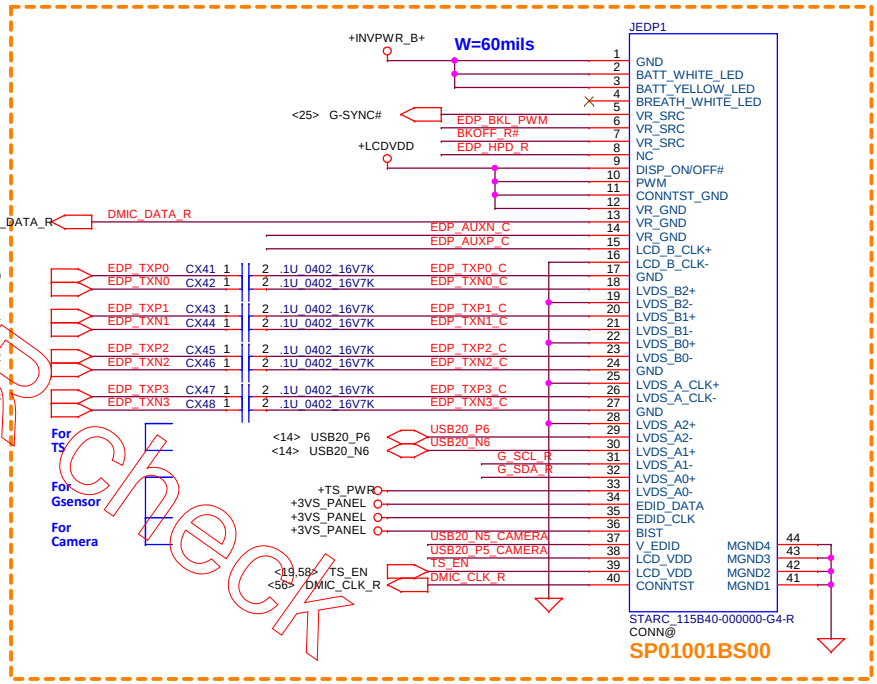
USB Touch Screen



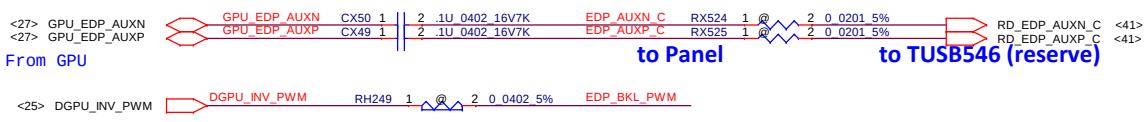
eDP RD SUB, Camera



Raptor



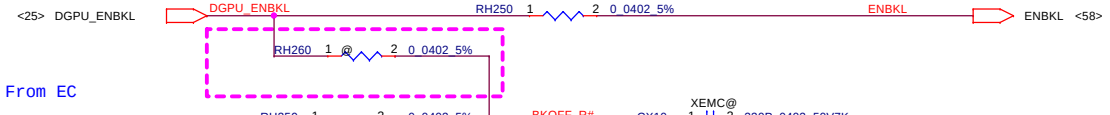
From GPU



From GPU

0809, NV suggest to use dGPU directly control,default use EC

To EC



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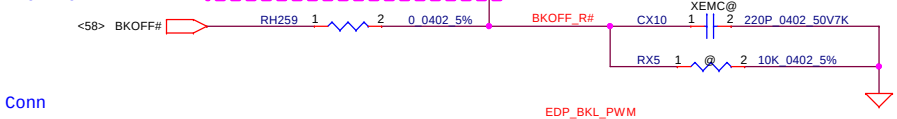
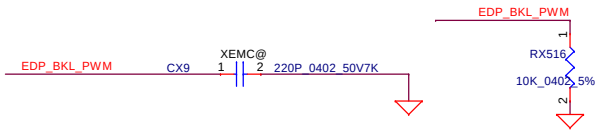
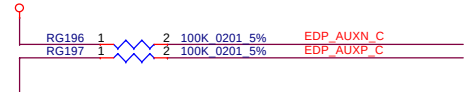
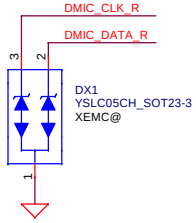


Conn



FOR VGA OUTPUT





EH78F_ACER_Check

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2018/09/01

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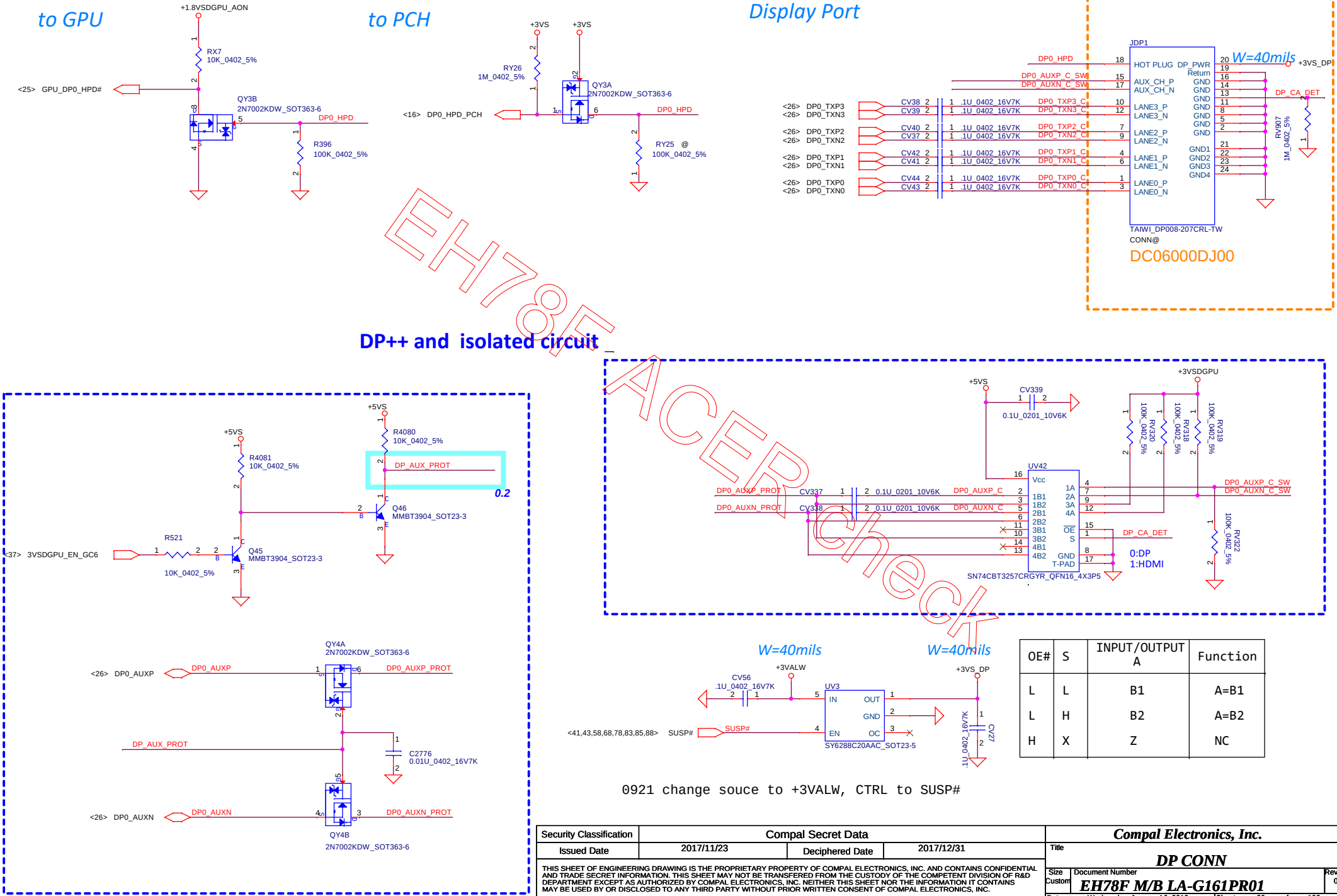
Compal Electronics, Inc.

Title: **eDP CONN.**

Size	Document Number	Rev
Custom	EH78F M/B LA-G161PR01	0.1

Date: Wednesday, January 16, 2019 Sheet 38 of 102



OE#	S	INPUT/OUTPUT A	Function
L	L	B1	A=B1
L	H	B2	A=B2
H	X	Z	NC

0921 change souce to +3VALW, CTRL to SUSP#

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

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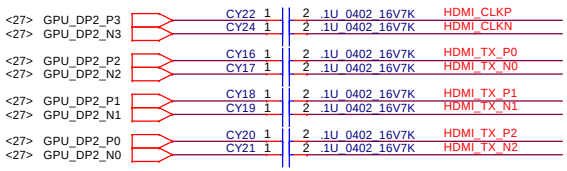
Compal Electronics, Inc.

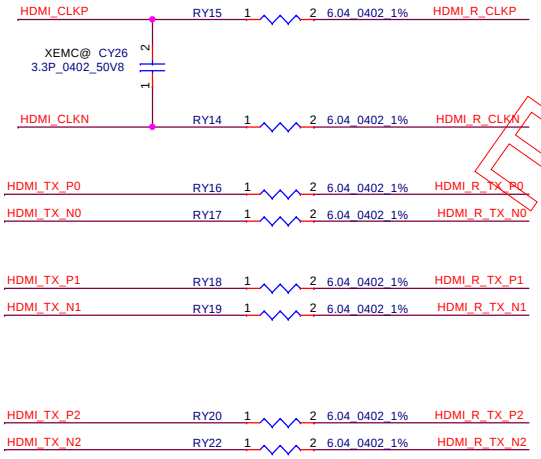
Title: DP CONN

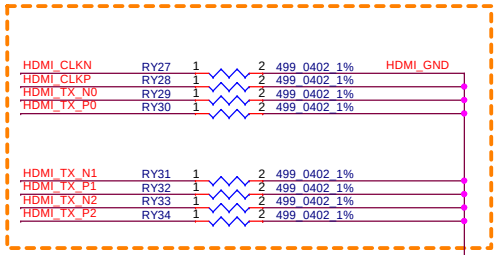
Size: Custom | Document Number: EH78F M/B LA-G161PR01 | Rev: 0.1

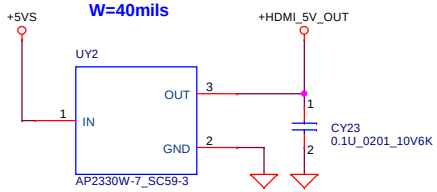
Date: Wednesday, January 16, 2019 | Sheet 39 of 102

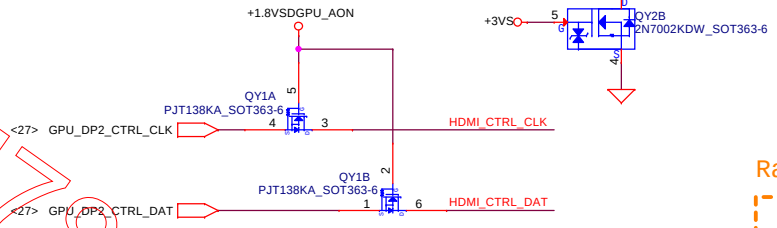
Raptor



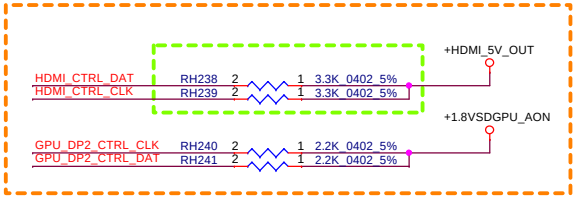


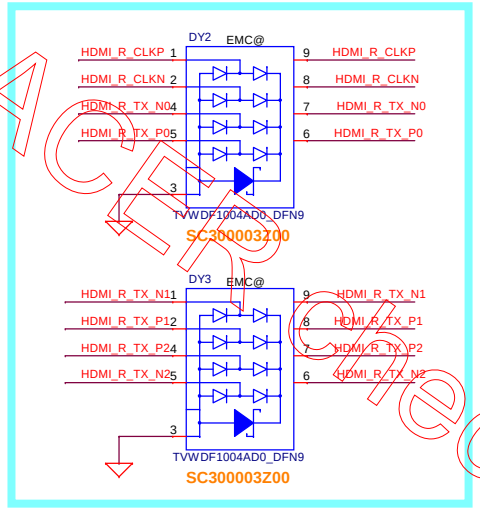




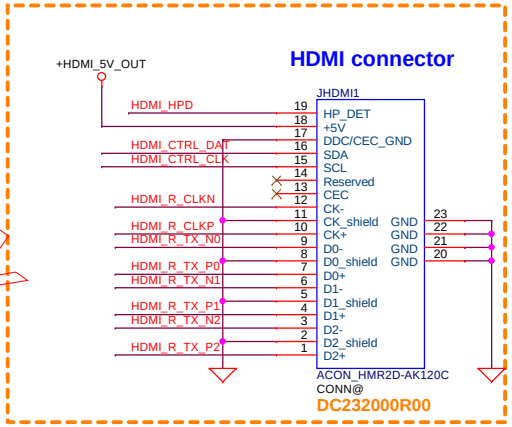


Raptor, follow eagle and 1060 MP 2.2K

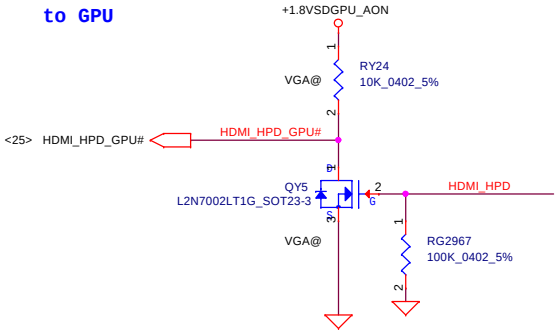




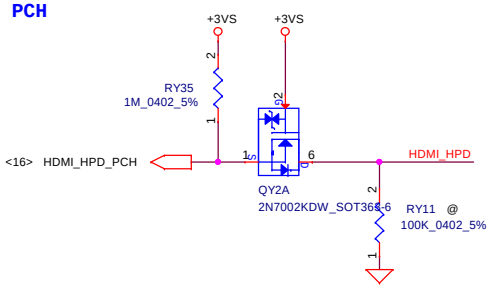
change PN follow USB3

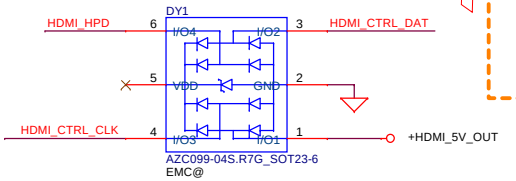


to GPU



to PCH





P/N: SC300002900, S DIO(BR) AZC199-04S.R7G SOT23-6 ESD

ZZZ2

HDMI_ROYALTY
ROYALTY HDMI W/LOGO+HDCP
RO0000003HM
45@

EH78F ACES check

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2018/09/01

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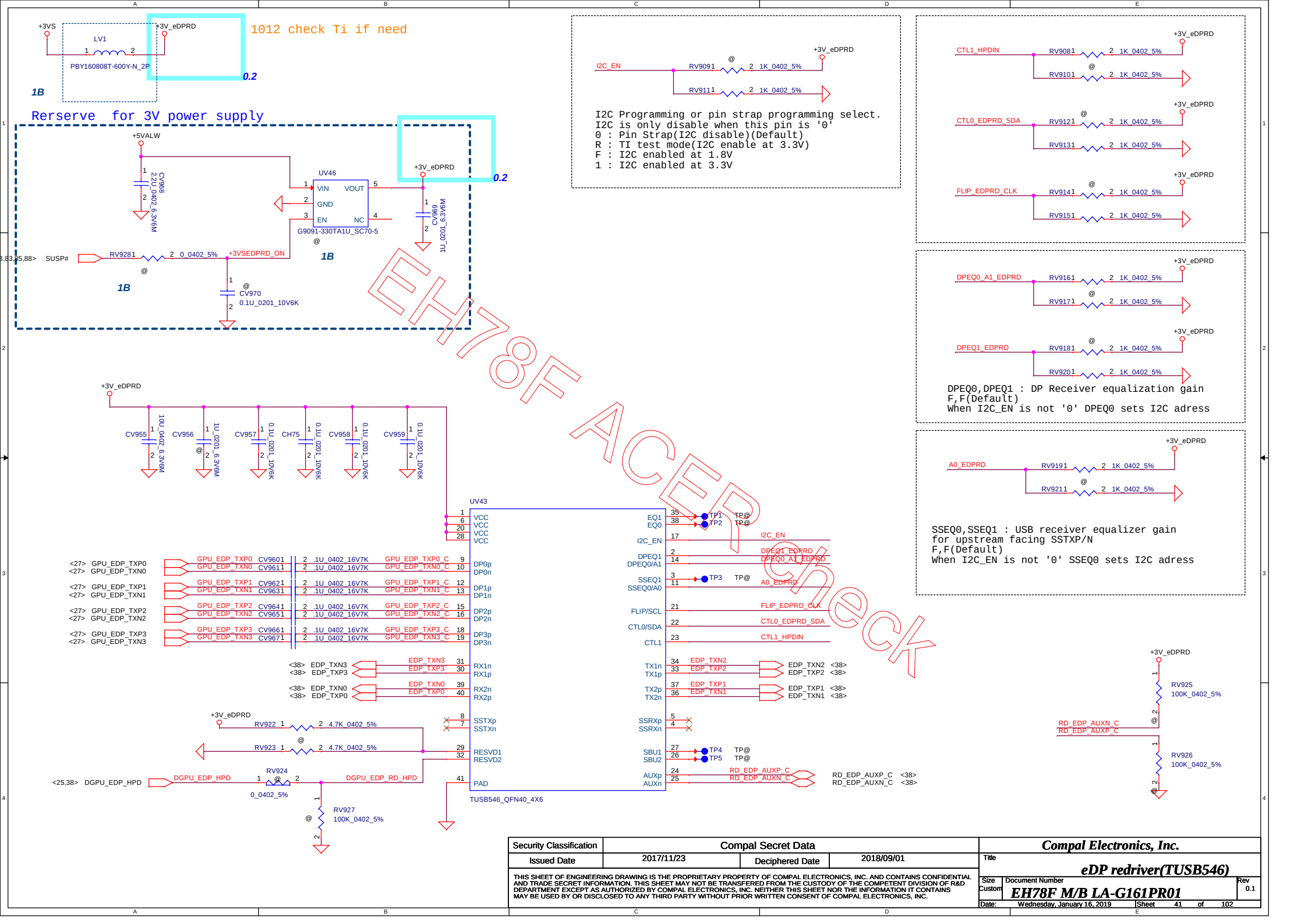
Compal Electronics, Inc.			
Title: HDMI CONN.			
Size: Custom	Document Number: EH78F M/B LA-G161PR01		Rev: 0.1
Date: Wednesday, January 16, 2019	Sheet 40 of 102		



Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2018/09/01

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Compal Electronics, Inc.			
Title	eDP redriver(TUSB546)		
Size	Document Number		Rev
Custom	EH78F M/B LA-G161PR01		0.1
Date:	Wednesday, January 16, 2019	Sheet	41 of 102

1012 check Ti if need

+3VS — LT39 — +3V_TYPEC_DP

PBY160808T-600Y-N_2P

TBT@

I2C_EN_TBT — RT8441 @ 2 1K_0402_5% — +3V_TYPEC_DP

RT8461 2 1K_0402_5% TBT@

I2C Programming or pin strap programming select.
I2C is only disable when this pin is '0'
0 : Pin Strap(I2C disable)(Default)
R : TI test mode(I2C enable at 3.3V)
F : I2C enabled at 1.8V
1 : I2C enabled at 3.3V

CTL1_TBT_HPDIN — RT8431 TBT@ 2 1K_0402_5% — +3V_TYPEC_DP

RT8451 @ 2 1K_0402_5%

CTL0_TBT_SDA — RT9001 @ 2 1K_0402_5% — +3V_TYPEC_DP

RT8471 2 1K_0402_5% TBT@

FLIP_TBT_CLK — RT8481 @ 2 1K_0402_5% — +3V_TYPEC_DP

RT8491 TBT@ 2 1K_0402_5%

DPEQ0_A1_TBT — RT8501 TBT@ 2 1K_0402_5% — +3V_TYPEC_DP

RT8511 @ 2 1K_0402_5%

DPEQ1_TBT — RT8521 @ 2 1K_0402_5% — +3V_TYPEC_DP

RT8531 TBT@ 2 1K_0402_5%

DPEQ0,DPEQ1 : DP Receiver equalization gain
F,F(Default)
When I2C_EN is not '0' DPEQ0 sets I2C adress

A0_TBT — RT8541 TBT@ 2 1K_0402_5% — +3V_TYPEC_DP

RT8551 @ 2 1K_0402_5%

SSEQ0,SSEQ1 : USB receiver equalizer gain
for upstream facing SSTXP/N
F,F(Default)
When I2C_EN is not '0' SSEQ0 sets I2C adress

+3V_TYPEC_DP

CT305 1 10U_0402_6.3V6M 2 TBT@
CT306 1 @ 1U_0201_6.3V6M 2
CT307 1 0.1U_0201_10V6K 2 TBT@
CH74 1 0.1U_0201_10V6K 2 TBT@
CT308 1 0.1U_0201_10V6K 2 TBT@
CT309 1 0.1U_0201_10V6K 2 TBT@

UT11

VCC 1, 6, 20, 28

<26> DP4_TXP0 — CT310 1 TBT@ 2 0.1U_0201_10V6K DP4_TXP0_C — 9 DP0p
<26> DP4_TXN0 — CT311 1 TBT@ 2 0.1U_0201_10V6K DP4_TXN0_C — 10 DP0n
<26> DP4_TXP1 — CT312 1 TBT@ 2 0.1U_0201_10V6K DP4_TXP1_C — 12 DP1p
<26> DP4_TXN1 — CT313 1 TBT@ 2 0.1U_0201_10V6K DP4_TXN1_C — 13 DP1n
<26> DP4_TXP2 — CT314 1 TBT@ 2 0.1U_0201_10V6K DP4_TXP2_C — 15 DP2p
<26> DP4_TXN2 — CT315 1 TBT@ 2 0.1U_0201_10V6K DP4_TXN2_C — 16 DP2n
<26> DP4_TXP3 — CT316 1 TBT@ 2 0.1U_0201_10V6K DP4_TXP3_C — 18 DP3p
<26> DP4_TXN3 — CT317 1 TBT@ 2 0.1U_0201_10V6K DP4_TXN3_C — 19 DP3n

<43> TBT_DP4_N3 — TBT_DP4_N3 — 31 RX1n
<43> TBT_DP4_P3 — TBT_DP4_P3 — 30 RX1p
<43> TBT_DP4_N0 — TBT_DP4_N0 — 39 RX2n
<43> TBT_DP4_P0 — TBT_DP4_P0 — 40 RX2p

+3V_TYPEC_DP — RT856 TBT@ 1 2 4.7K_0402_5% — 8 SSTXp, 7 SSTXn
RT857 @ 1 2 4.7K_0402_5% — 29 RESVD1, 32 RESVD2

<16,43> TBT_DP4_HPD — TBT_DP4_HPD RT858 1 @ 2 0_0402_5% TBT_DP4_HPD_R — 41 PAD

TUSB546_QFN40_4X6
TBT@

EQ1 35 — TH41 TP@
EQ0 38 — TH40 TP@
I2C_EN 17 — I2C_EN_TBT
DPEQ1 2 — DPEQ1_TBT
DPEQ0/A1 14 — DPEQ0_A1_TBT
SSEQ1 3 — TH42 TP@
SSEQ0/A0 11 — A0_TBT
FLIP/SCL 21 — FLIP_TBT_CLK
CTL0/SDA 22 — CTL0_TBT_SDA
CTL1 23 — CTL1_TBT_HPDIN

TX1n 34 — TBT_DP4_N2 — TBT_DP4_N2 <43>
TX1p 33 — TBT_DP4_P2 — TBT_DP4_P2 <43>
TX2p 37 — TBT_DP4_P1 — TBT_DP4_P1 <43>
TX2n 36 — TBT_DP4_N1 — TBT_DP4_N1 <43>

SSRXp 5
SSRXn 4

SBU1 27 — TH43 TP@
SBU2 26 — TH44 TP@

AUXp 24 — RD_DP4_AUXP_C — 0.1U_0201_10V6K 2 1 CT318 DP4_AUXP — DP4_AUXP <26,43>
AUXn 25 — RD_DP4_AUXN_C — 0.1U_0201_10V6K 2 1 CT319 DP4_AUXN — DP4_AUXN <26,43>
TBT@ TBT@

+3V_TYPEC_DP
RT859 1 100K_0402_5% 2 TBT@
RD_DP4_AUXN_C
RD_DP4_AUXP_C
RT860 1 100K_0402_5% 2 TBT@

EH78F ACES Check

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Compal Electronics, Inc.

Title: TBT DP redriver

Size: Custom | Document Number: EH78F M/B LA-G161PR01 | Rev: 0.1

Date: Wednesday, January 16, 2019 | Sheet 42 of 102

Raptor: CAP change to 0201

Raptor: CAP change to 0201

PU at PCH side.

PCIE_X4 Bus
(Link to PCH Port 21~24)

DDC:3.3V
PU @ SOC side

Raptor

PCIE_CLK
(From PCH CLKOUT6)

POC_GPIO_0	interrupt from port power switch
POC_GPIO_1	interrupt from port power switch
POC_GPIO_2	rtd3 power enable for USB mode
POC_GPIO_3	force full power on
POC_GPIO_4	battery low indication
POC_GPIO_5	slp_s3 system indication
POC_GPIO_6	rtd3 power enable for cio mode

Raptor: change to xtal vendor suggest
P/N: SJ10000UH00 (S CRYSTAL 25MHZ 20PF XRCGB25M000F2P18R0)

Follow Intel recommend, 5/4.

Follow Intel recommend, 4/28.

Raptor: intel AR SP refe to 1M

SNK0_DDC_connect 2k PU only if SRC0 is connected HDMI otherrise can be 100k PD

EH78F_MB_LA-G161PR01_Schematic_Check

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Compal Electronics, Inc.

Title: TBT AR(1/2)

Size: Custom | Document Number: EH78F M/B LA-G161PR01 | Rev: 0.1

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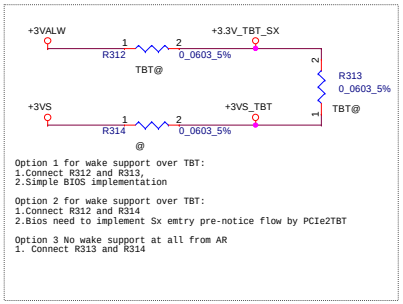


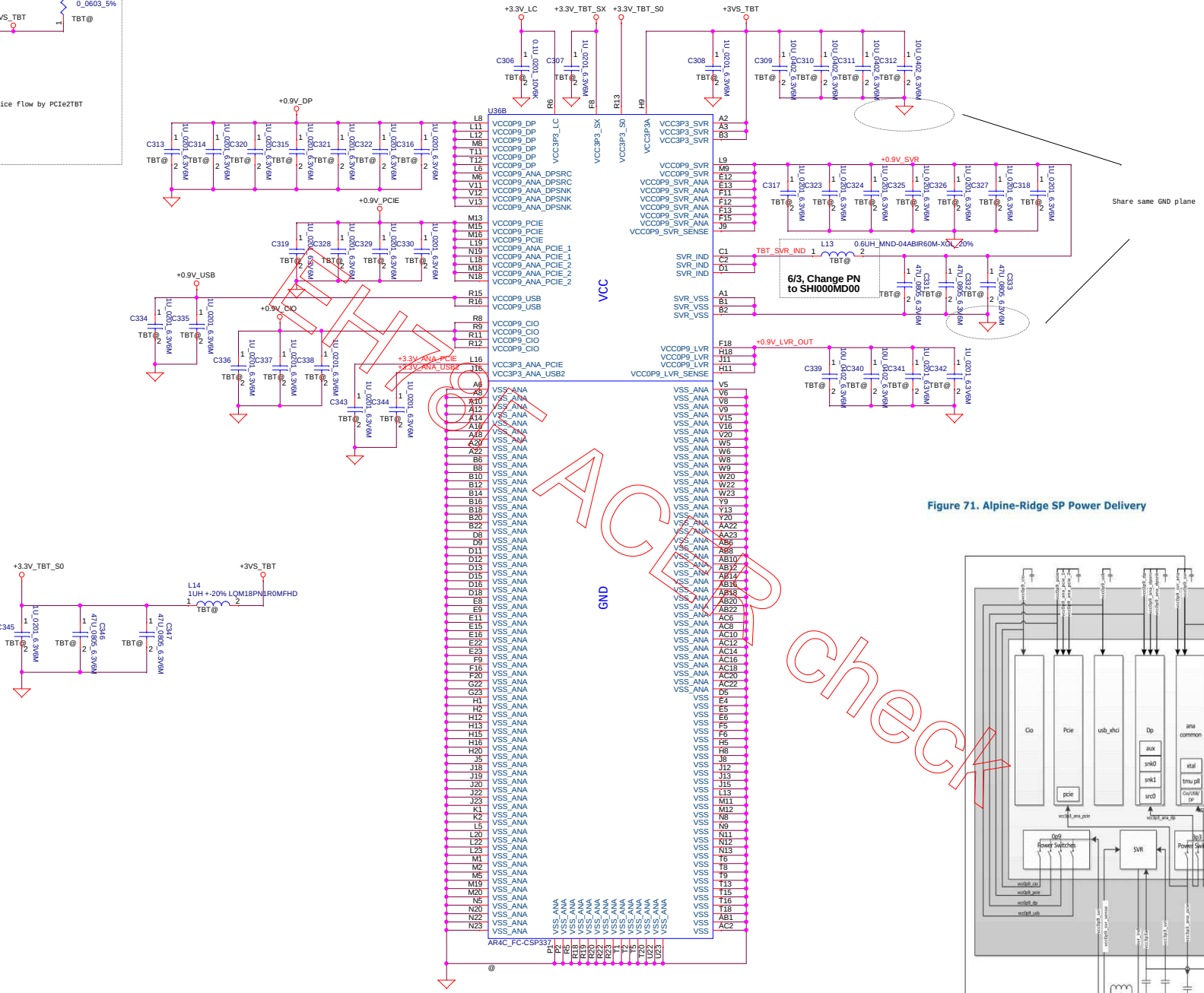
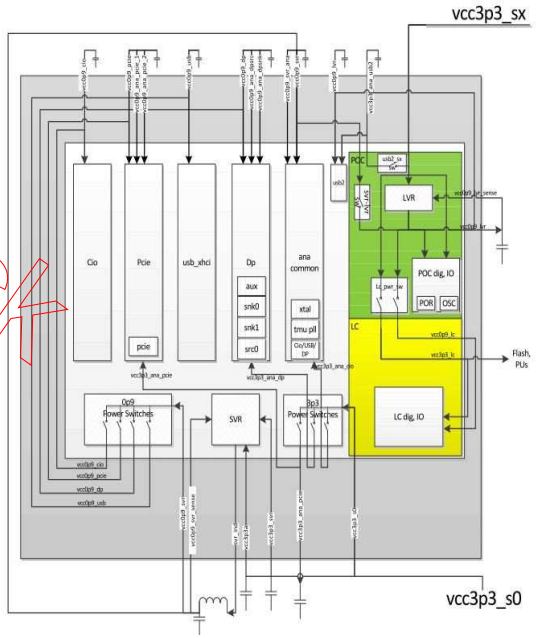


Figure 71. Alpine-Ridge SP Power Delivery



Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

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Compal Electronics, Inc.			
Title: TBT AR(2/2)			
Size: Custom	Document Number: EH78F M/B LA-G161PR01		Rev: 0.1
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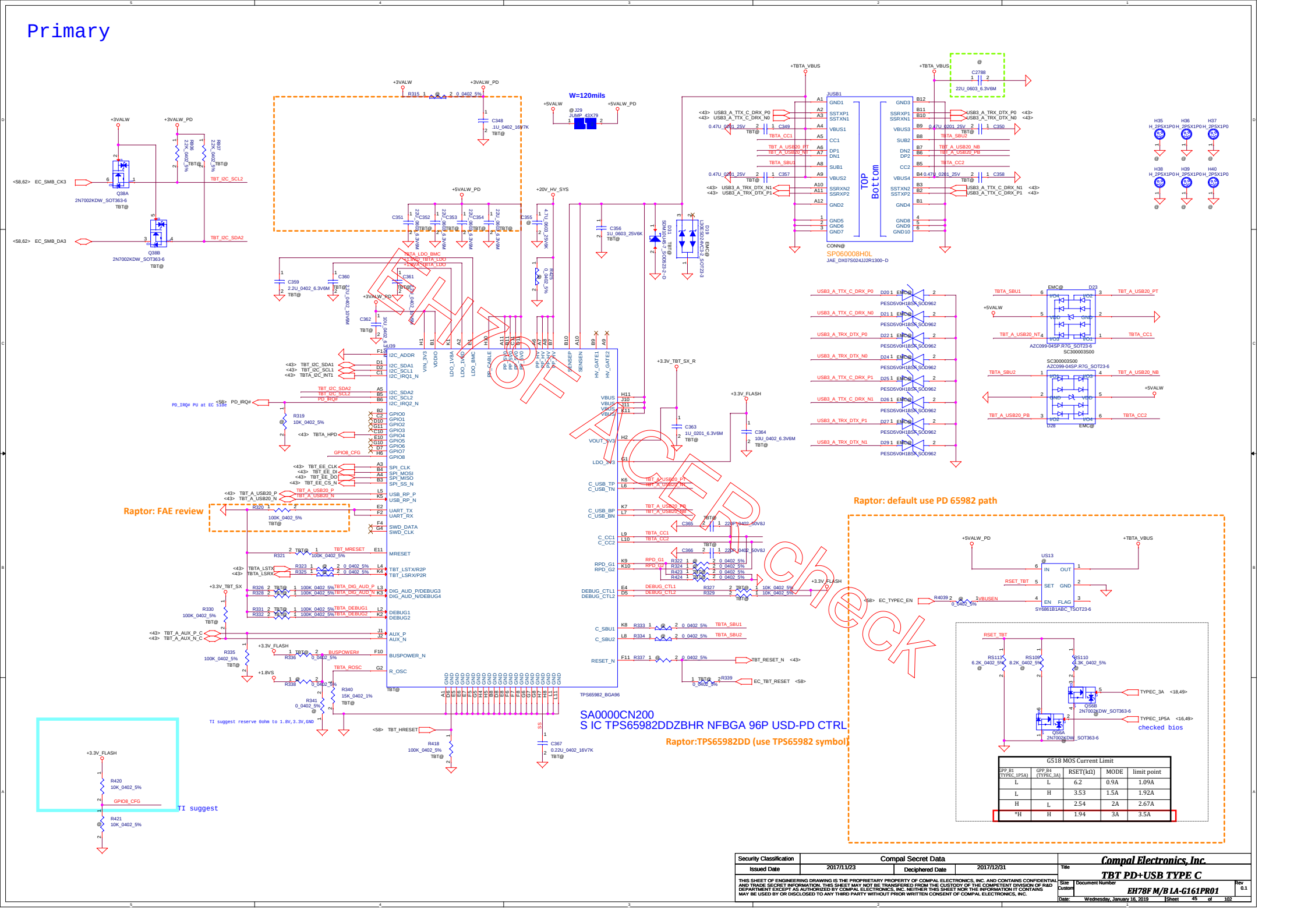
Primary



G518 MOS Current Limit				
GPP_B1 (TYPEC_1P5A)	GPP_B4 (TYPEC_3A)	RSET(kΩ)	MODE	limit point
L	L	6.2	0.9A	1.09A
L	H	3.53	1.5A	1.92A
H	L	2.54	2A	2.67A
*H	H	1.94	3A	3.5A

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Issued Date	2017/11/23	Deciphered Date	2017/12/31

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Title	Compal Electronics, Inc.
	TBT PD+USB TYPE C
Size: Custom	Document Number: EH78F M/B LA-G161PR01
Rev	0.1
Date:	Wednesday, January 16, 2019
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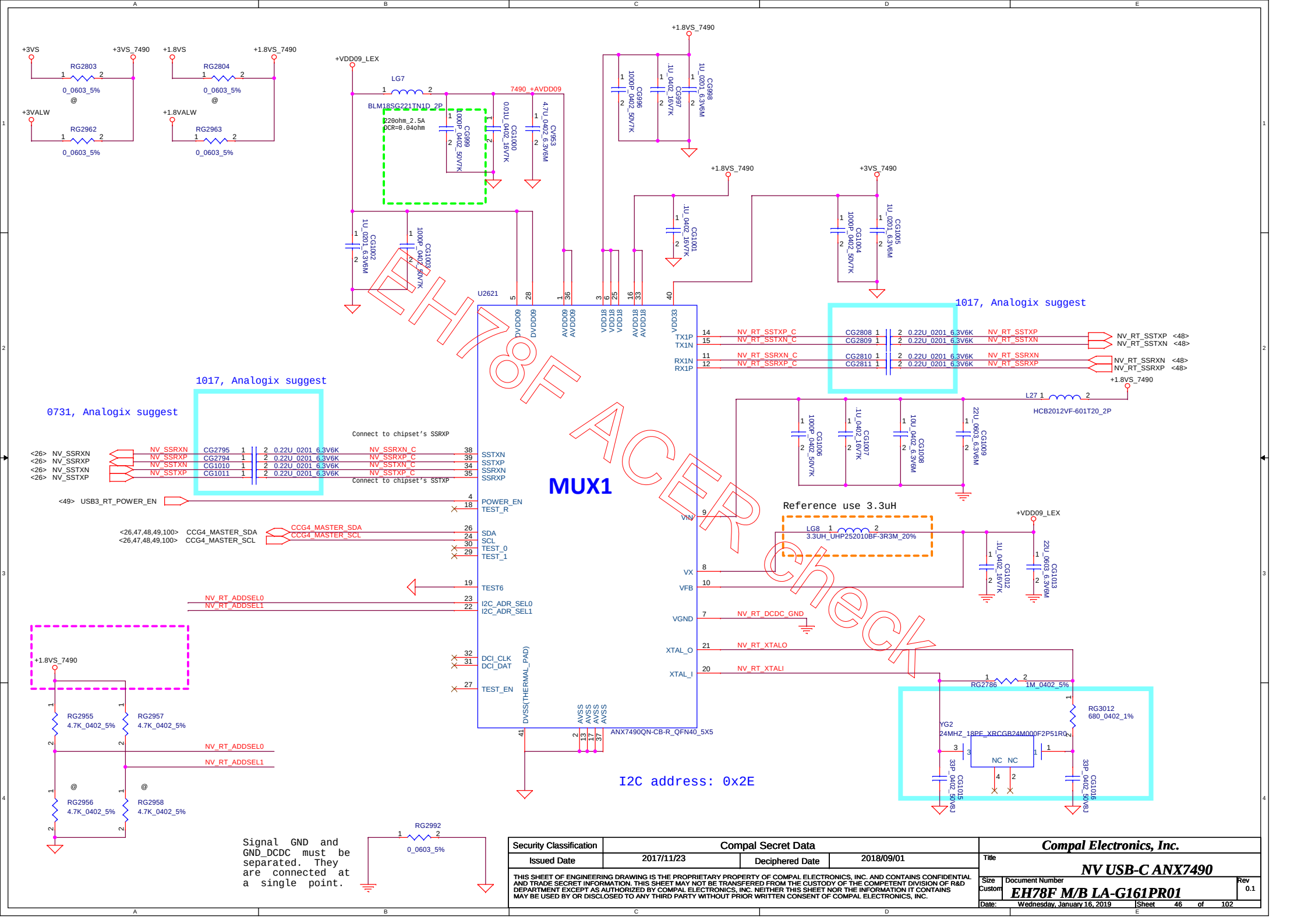

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2018/09/01

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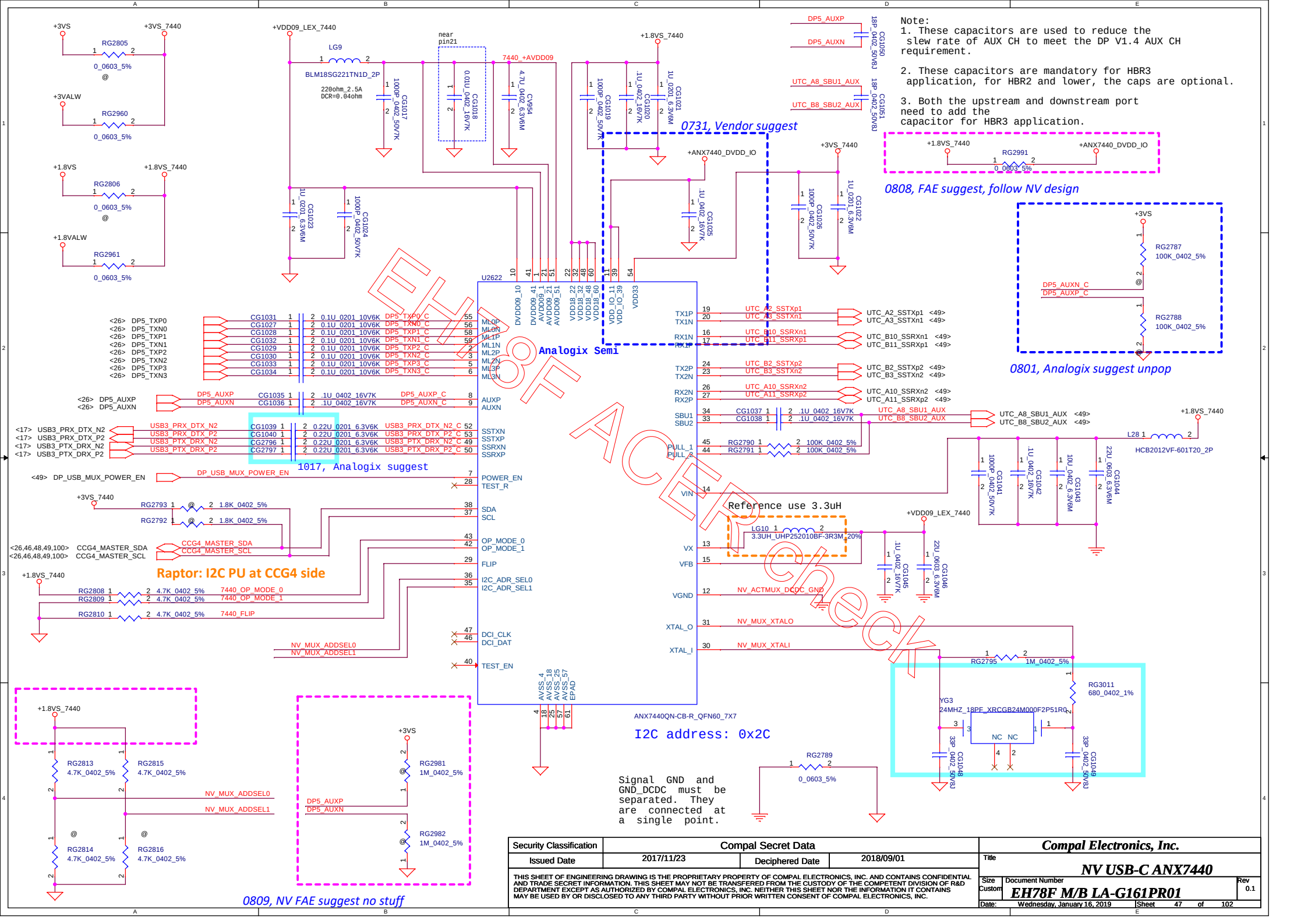
Compal Electronics, Inc.

Title: NV USB-C ANX7490

Size: Custom | Document Number: EH78F M/B LA-G161PR01 | Rev: 0.1

Date: Wednesday, January 16, 2019 | Sheet 46 of 102


Note:
1. These capacitors are used to reduce the slew rate of AUX CH to meet the DP V1.4 AUX CH requirement.
2. These capacitors are mandatory for HBR3 application, for HBR2 and lower, the caps are optional.
3. Both the upstream and downstream port need to add the capacitor for HBR3 application.
0731, Vendor suggest
0808, FAE suggest, follow NV design
0801, Analogix suggest unpop
1017, Analogix suggest
Analogix Semi
U2622
ANX7440QN-CB-R_QFN60_7X7
Reference use 3.3uH
Raptor: I2C PU at CCG4 side
I2C address: 0x2C
Signal GND and GND_DCDC must be separated. They are connected at a single point.
0809, NV FAE suggest no stuff
ENGINEERING SAMPLE
NOT FOR PRODUCTION
Compal Electronics, Inc.
NV USB-C ANX7440
EH78F M/B LA-G161PR01
Security Classification: Compal Secret Data
Issued Date: 2017/11/23
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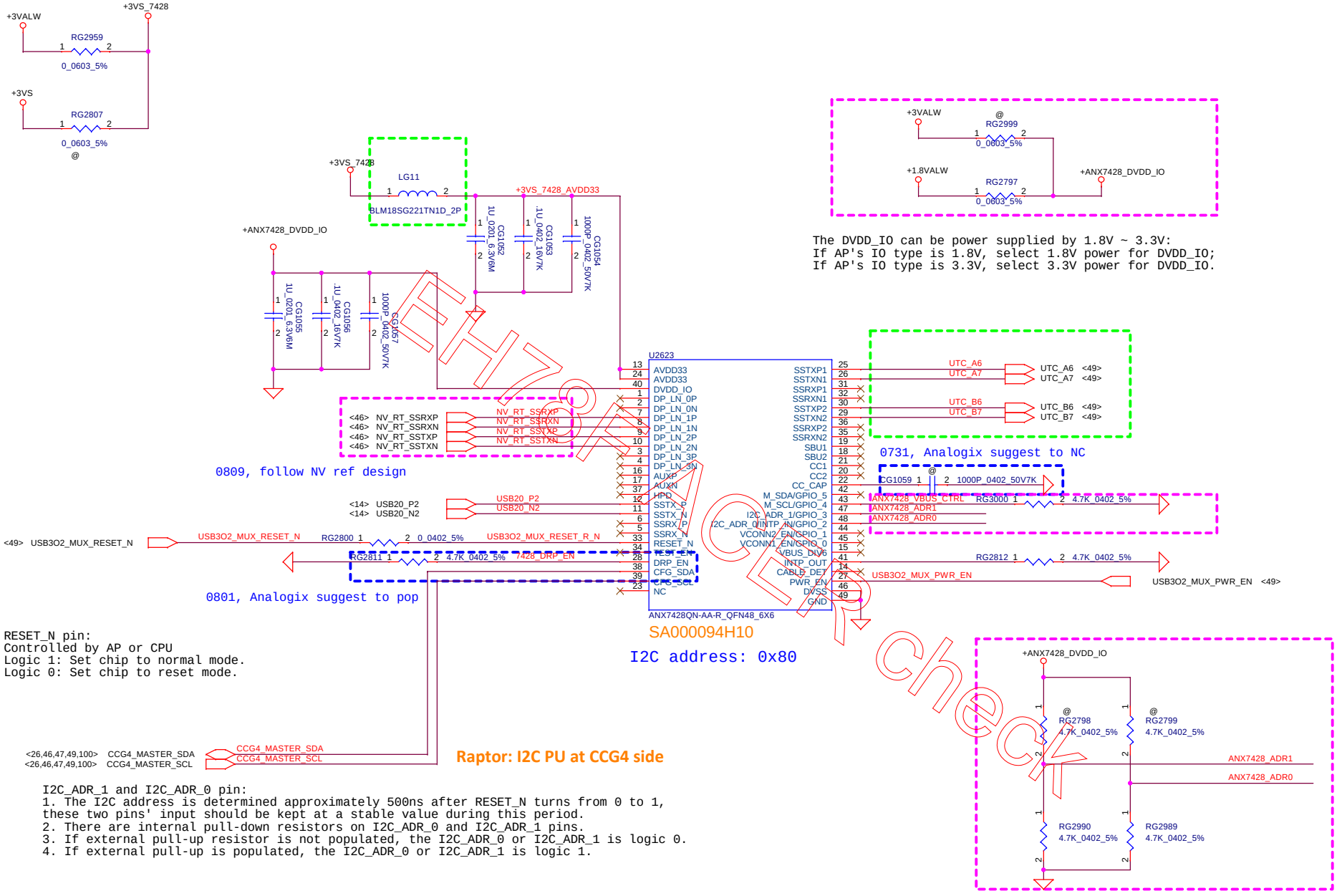

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Compal Electronics, Inc.			
Title: NV USB-C ANX7428			
Size: Custom	Document Number: EH78F M/B LA-G161PR01		Rev: 0.1
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TypeC NV

CCG4 Master, to 7440, 7428, NV GPU,

to NV GPU

HPD

SA0000C9C00
S IC CYPD4136-24LQXQT QFN 24P USB TYPE-C CTRL

use CYPD4136 P/N, Symbol/Footprint use CYPD4126

default use NV design

Raptor: for HV protect

checked bios

G51B MOS Current Limit				
GPP_B1 (TYPEC_1P5A)	GPP_B4 (TYPEC_3A)	RSET(kΩ)	MODE	limit point
L	L	6.2	0.9A	1.09A
L	H	3.53	1.5A	1.92A
H	L	2.54	2A	2.67A
*H	H	1.94	3A	3.5A

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Compal Electronics, Inc.

Title: NV USB-C CCG4+USB TYPE C

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Compal Electronics, Inc.		
Title: Reserve Page		
Size: Custom	Document Number: EH78F M/B LA-G161PR01	Rev: 0.1
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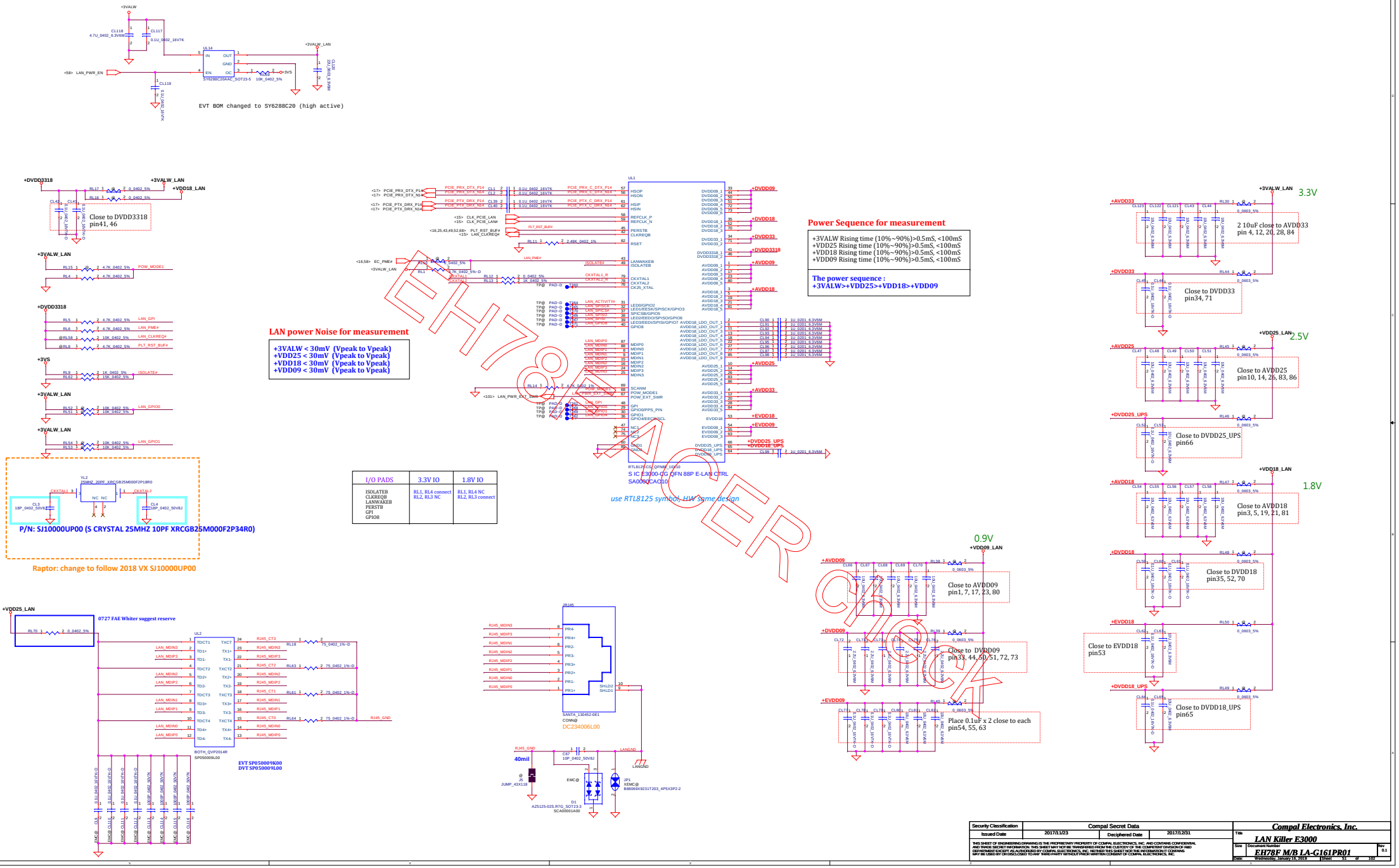
EVT BOM changed to SY6288C20 (high active)
Close to DVDD3318 pin41, 46
LAN power Noise for measurement
+3VALW < 30mV (Vpeak to Vpeak)
+VDD25 < 30mV (Vpeak to Vpeak)
+VDD18 < 30mV (Vpeak to Vpeak)
+VDD09 < 30mV (Vpeak to Vpeak)
Power Sequence for measurement
+3VALW Rising time (10%~90%)>0.5mS, <100mS
+VDD25 Rising time (10%~90%)>0.5mS, <100mS
+VDD18 Rising time (10%~90%)>0.5mS, <100mS
+VDD09 Rising time (10%~90%)>0.5mS, <100mS
The power sequence :
+3VALW>+VDD25>+VDD18>+VDD09
I/O PADS
3.3V IO
1.8V IO
ISOLATEB
CLKREQB
LANWAKEB
PERSTB
GPI
GPIO8
RL1, RL4 connect
RL2, RL3 NC
RL1, RL4 NC
RL2, RL3 connect
S IC E3000-CG QFN 88P E-LAN CTRL
SA000ACAC10
use RTL8125 symbol, HW same design
P/N: SJ10000UP00 (S CRYSTAL 25MHZ 10PF XRCGB25M000F2P34R0)
Raptor: change to follow 2018 VX SJ10000UP00
0727 FAE Whiter suggest reserve
EVT SP050009K00
DVT SP050009L00
Close to AVDD33 pin 4, 12, 20, 28, 84
2 10uF close to AVDD33 pin 4, 12, 20, 28, 84
Close to DVDD33 pin34, 71
Close to AVDD25 pin10, 14, 26, 83, 86
Close to DVDD25_UPS pin66
Close to AVDD18 pin3, 5, 19, 21, 81
Close to DVDD18 pin35, 52, 70
Close to EVDD18 pin53
Close to DVDD18_UPS pin65
Close to AVDD09 pin1, 7, 17, 23, 80
Close to DVDD09 pin33, 44, 50, 51, 72, 73
Place 0.1uF x 2 close to each pin54, 55, 63
3.3V
2.5V
1.8V
0.9V
EH78F M/B LA-G161PR01
Compal Electronics, Inc.
LAN Killer E3000
Security Classification
Compal Secret Data
Issued Date
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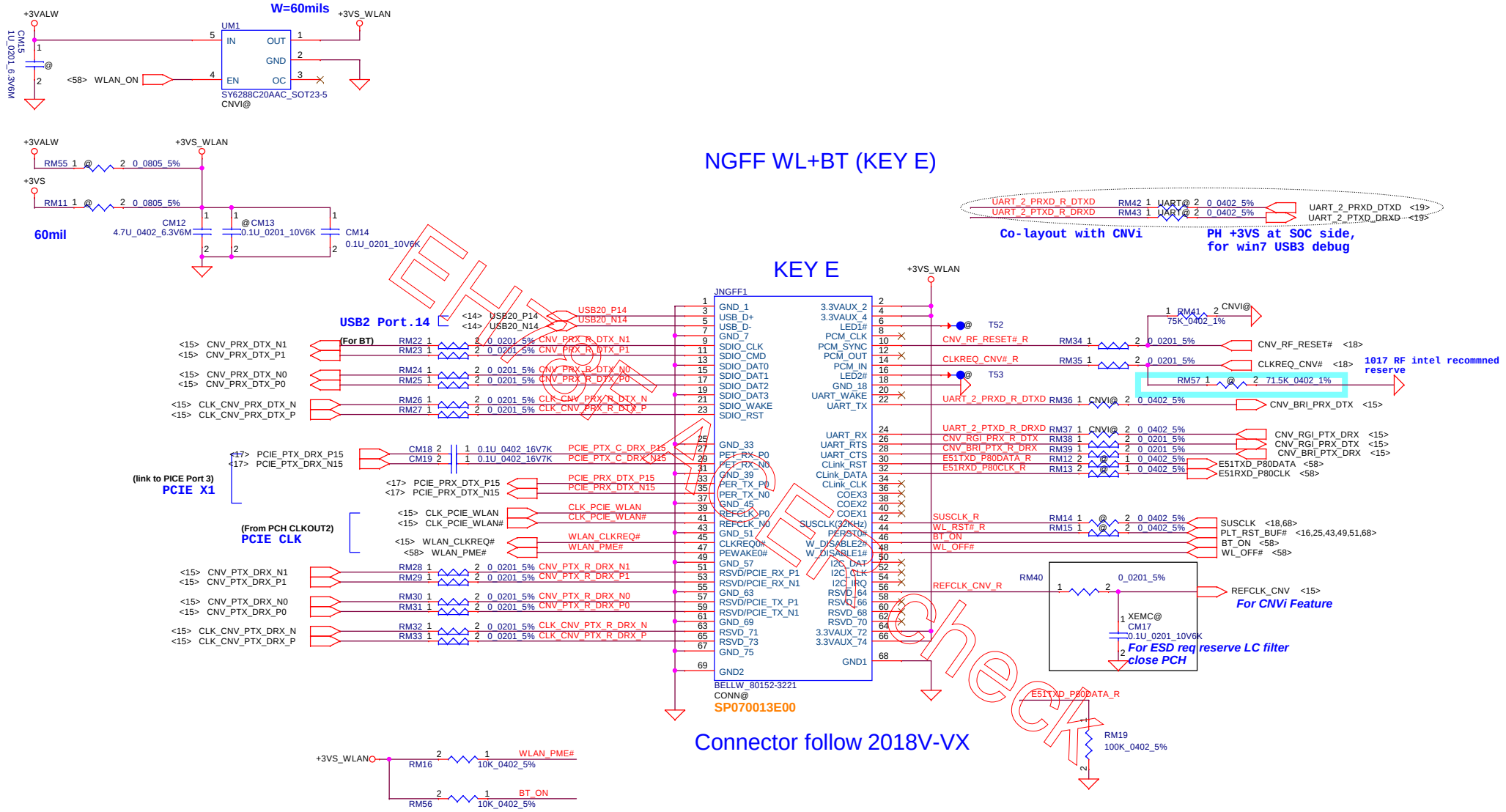
Wireless LAN



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Compal Electronics, Inc.

Title: WLAN M.2

Size: Custom | Document Number: EH78F M/B LA-G161PR01 | Rev: 0.1

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Compal Electronics, Inc.		
Title: Reserve Page		
Size: Custom	Document Number: EH78F M/B LA-G161PR01	Rev: 0.1
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Compal Electronics, Inc.		
Title: Reserve Page		
Size: Custom	Document Number: EH78F M/B LA-G161PR01	Rev: 0.1
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Compal Electronics, Inc.

Title: **Reserve Page**

Size: Custom	Document Number: EH78F M/B LA-G161PR01	Rev: 0.1
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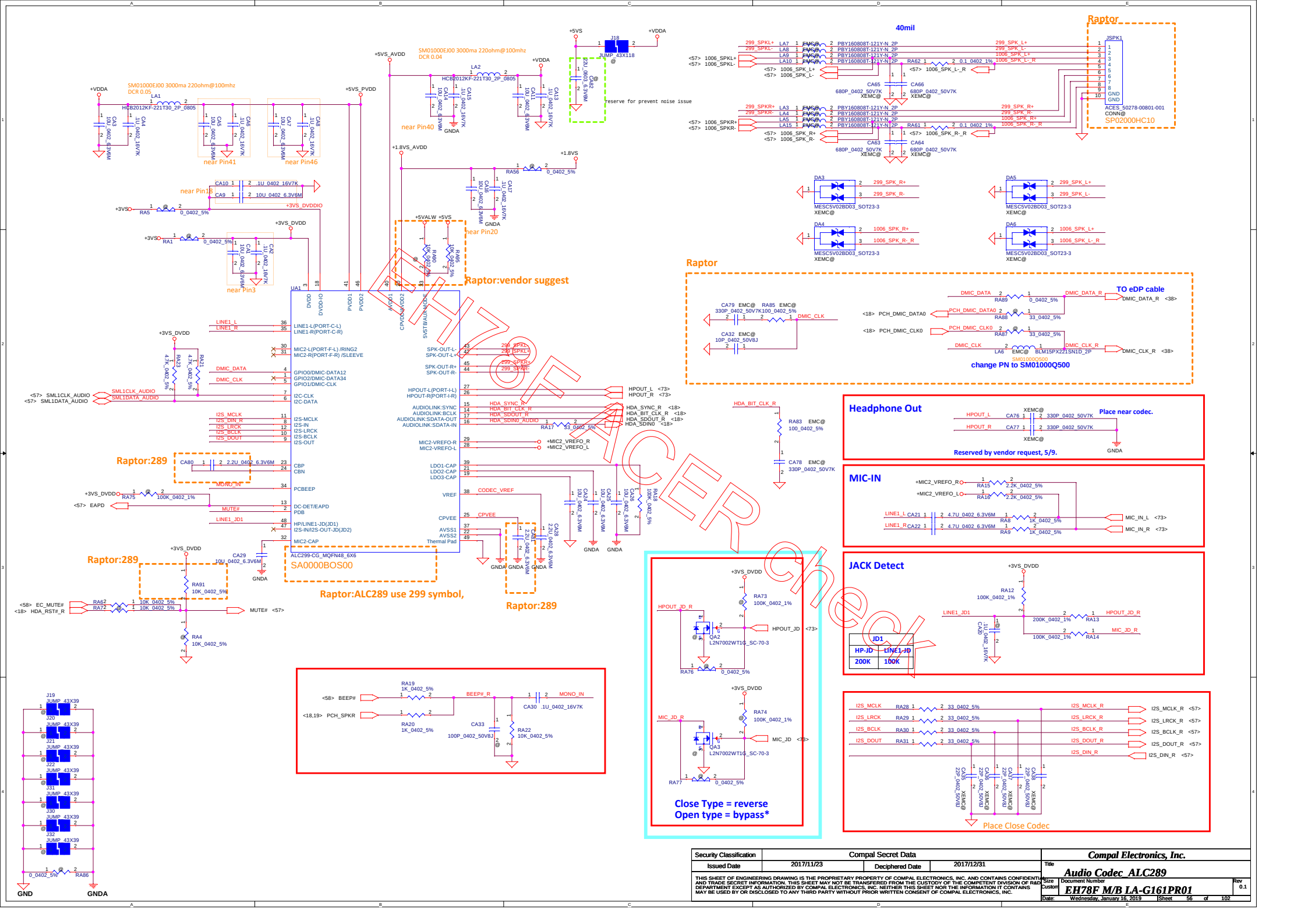

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Compal Electronics, Inc.

Title: Audio Codec_ALC289

Size: Custom | Document Number: EH78F M/B LA-G161PR01 | Rev: 0.1

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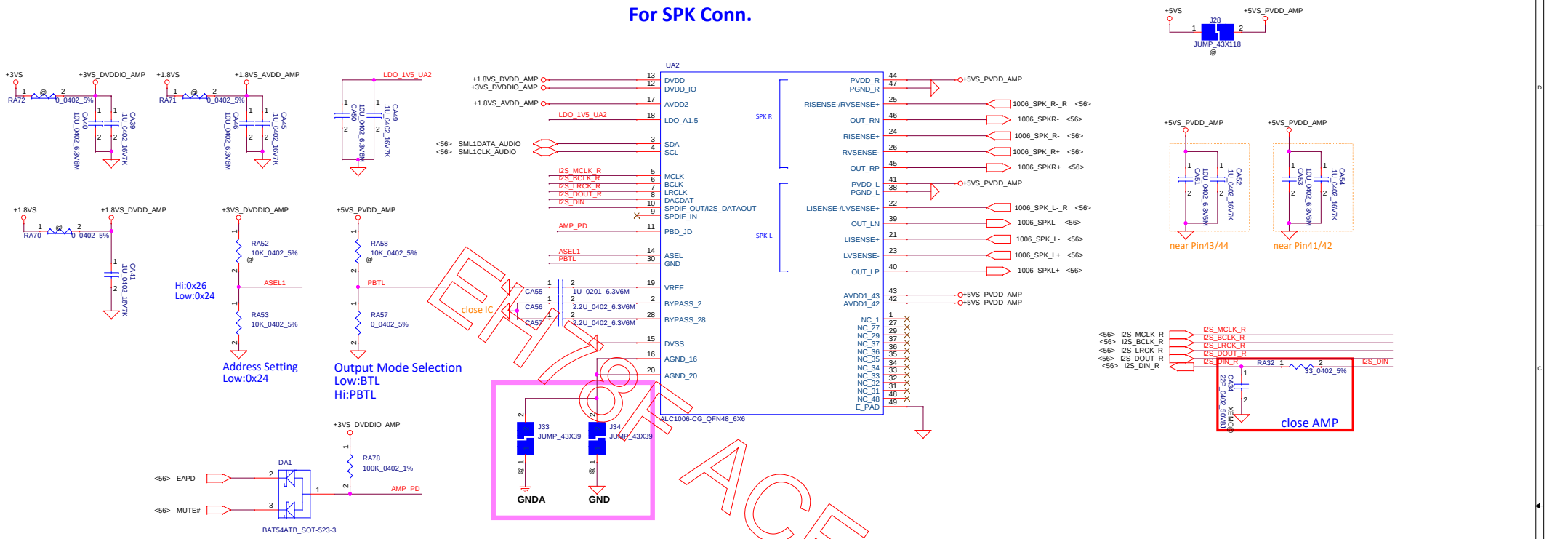
For SPK Conn.



ACER check

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Issued Date	2017/11/23	Deciphered Date	2017/12/31

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Compal Electronics, Inc.	
Title	Audio Amplifier ALC1006
Size: Custom	Document Number: EH78F M/B LA-G161PR01
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Board ID

Analog Board ID definition,
Please see page 3.

1C

near SOC

For Thermal Portect Shutdown

EC Internal PU

Prevent EC CLK test mode issue

0.2

For turn off internal LPC module of KB9032

For Power consumption Measurement

ESPI Bus Pin : 1~5,7,8,10,12,14
LPC Bus Pin : 3~5,7,8,10,12,13

PWM Output

LPC & MISC

AD Input

DA Output

PS2 Interface

Int. K/B Matrix

SPI Device Interface

SPI Flash ROM

GPIO

SM Bus

GPIO

GPI

PU at CPU side

For abnormal shutdown

for marco key 3810

CO-LAY with KB9032QA (SA000080J00)

20mil

2015/1/9 acer require:
reserved protact circuit when
adaptor 107% happen

check VR_PWRGD IS
AND BY CORE_PWRGD & SA_PWRGD

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2018/09/01

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Title: **Reserve Page**

Size	Document Number	Rev
Custom	EH78F M/B LA-G161PR01	0.1

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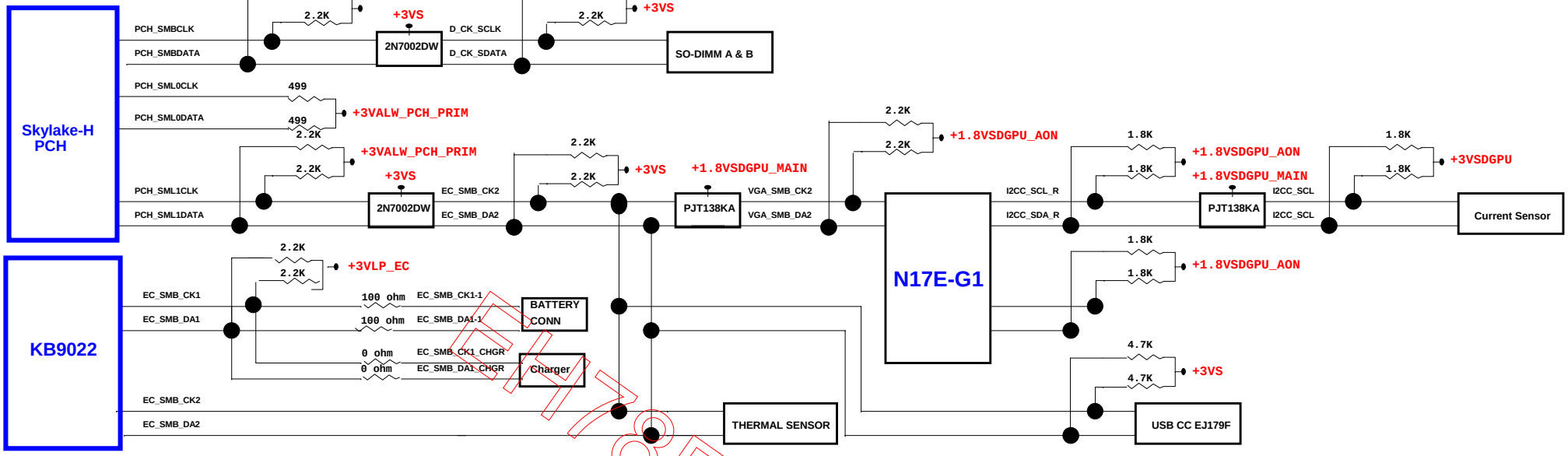

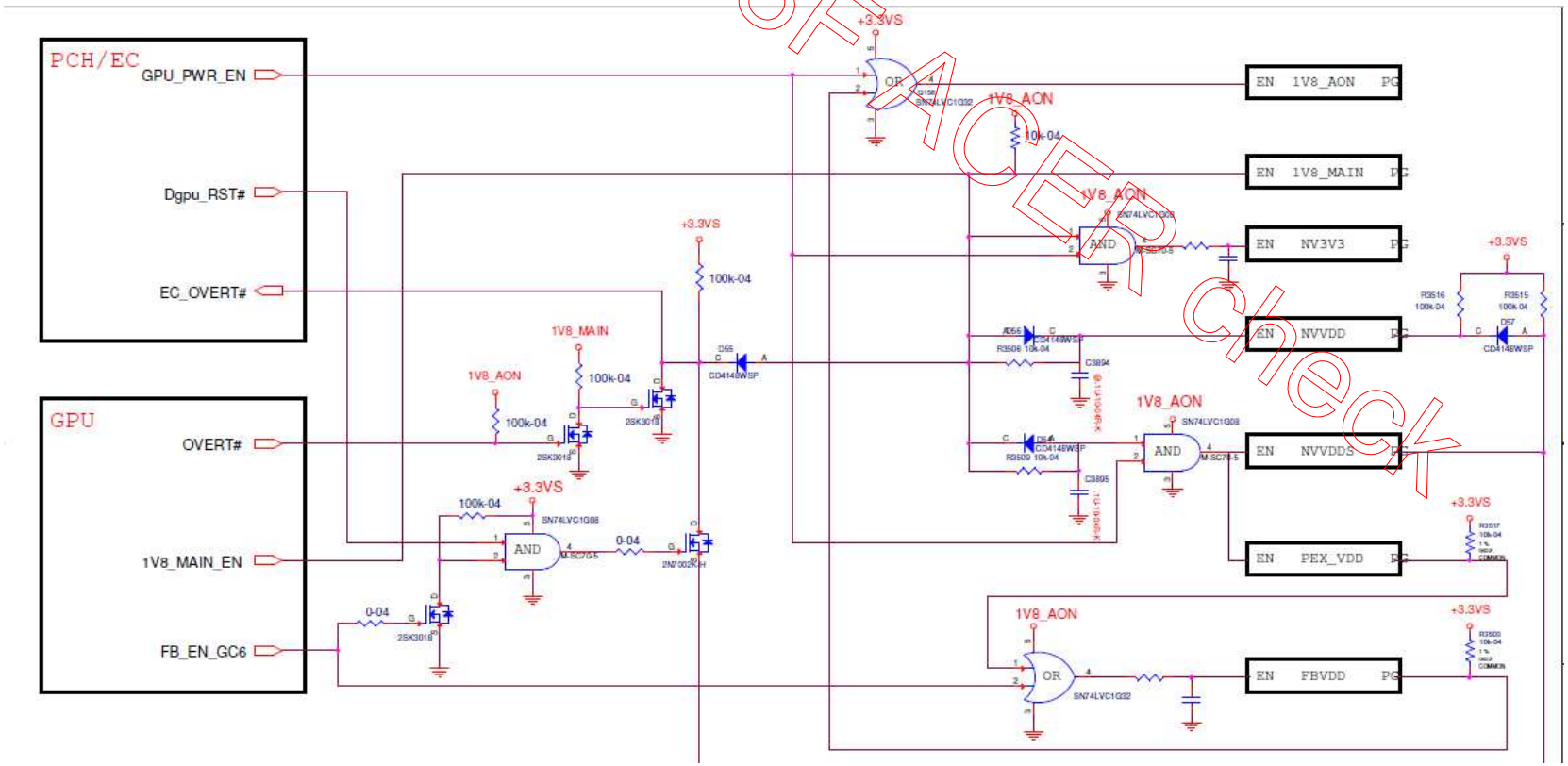

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Size	Document Number		Rev
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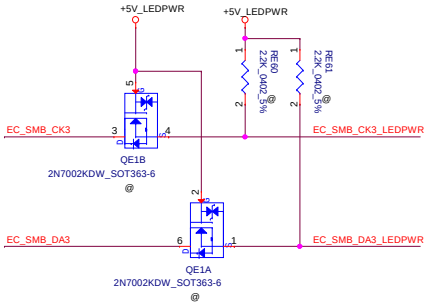
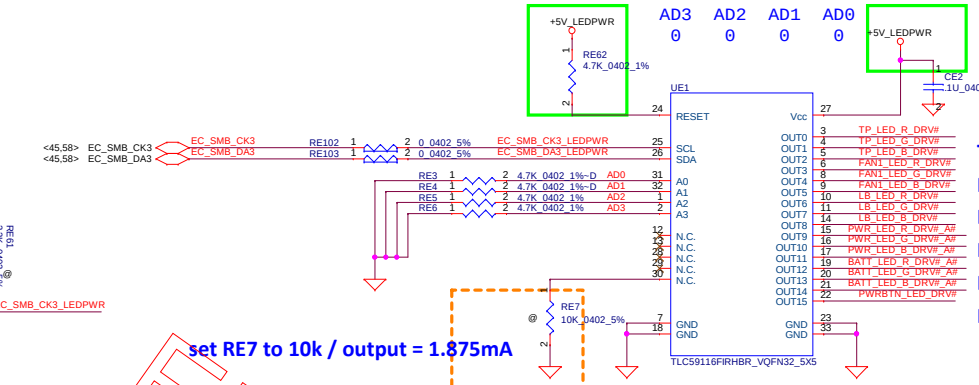
LED driver

Reserve, default bypass





set RE7 to 10k / output = 1.875mA

Raptor: NC for 59116F

T/P

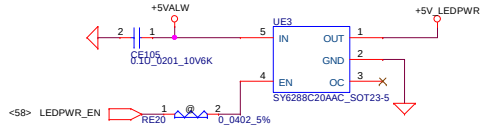
FAN-CPU

LED/B

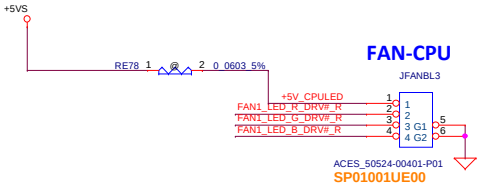
PWR LED

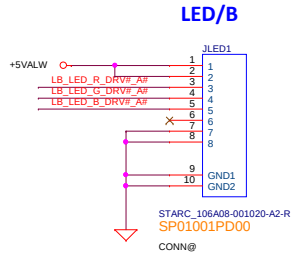
BATT LED

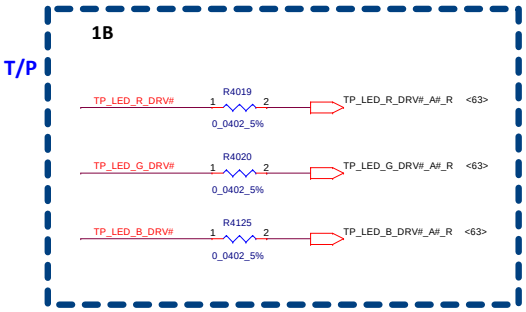
PWRBTN LED

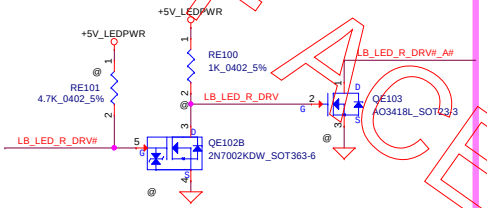


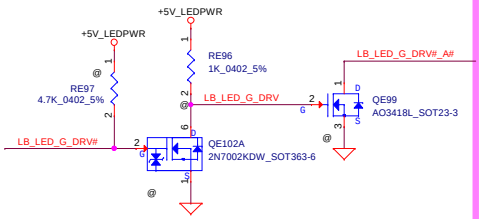
follow ECON

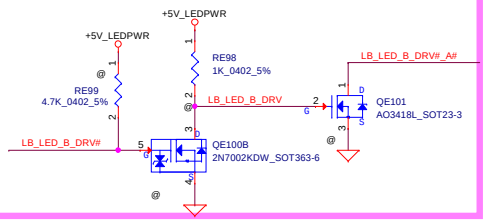


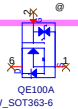








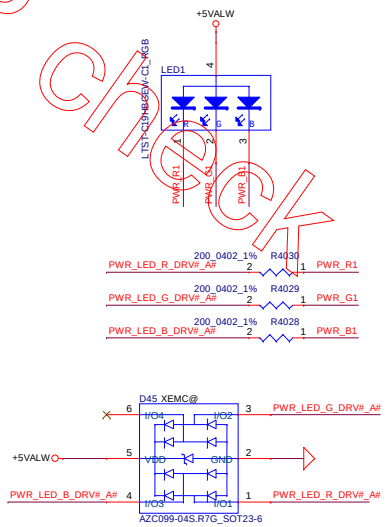




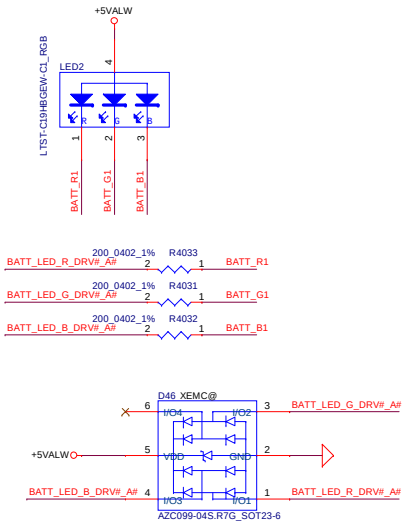
FAN-CPU

PWRBTN LED

PWR LED



BATT LED



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Title: LEDs(TLC59116F)

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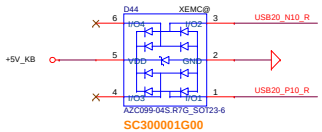
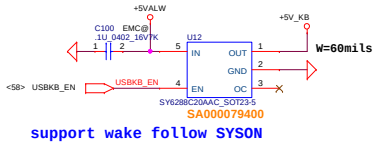
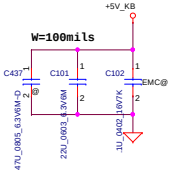
KB Conn.

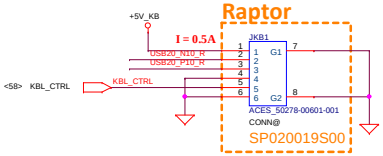




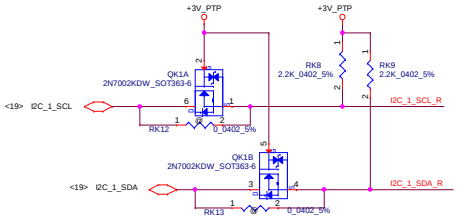
support wake follow SYSON

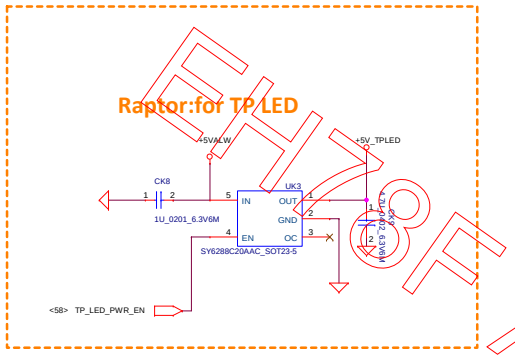


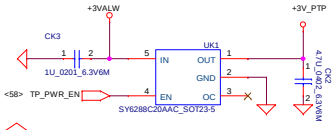
When RGB are WHITE input current <500mA



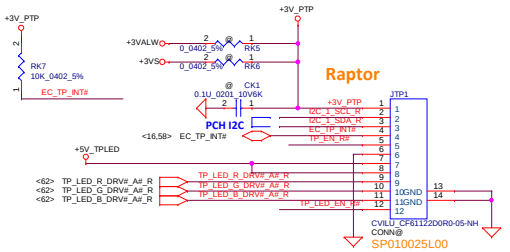
Touch Pad



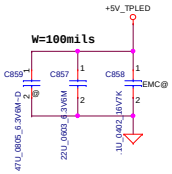


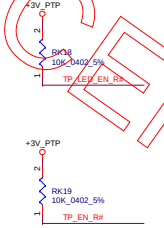


TP_PWR_EN follow SYSON behavior

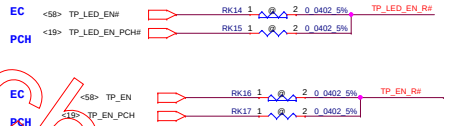


Raptor:waiting more spec for check





Default use EC control



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ACER
Check

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Title: KB/TP

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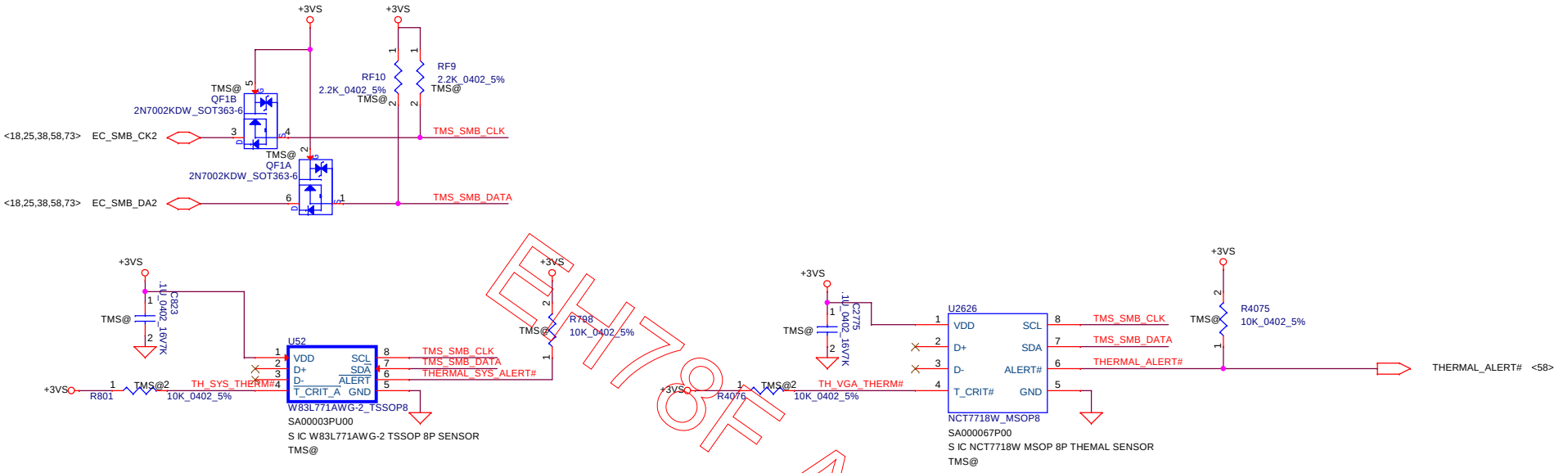
THERMAL SENSOR

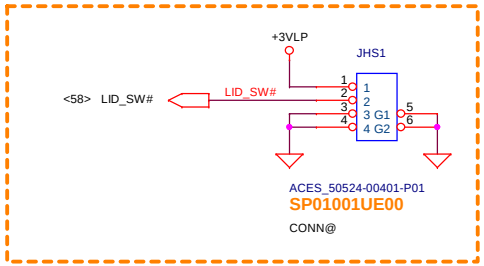


Part Number	SMBUS ADDRESS
NCT7718W	1001_1000b
W83L771AWG-2	1001_1010b

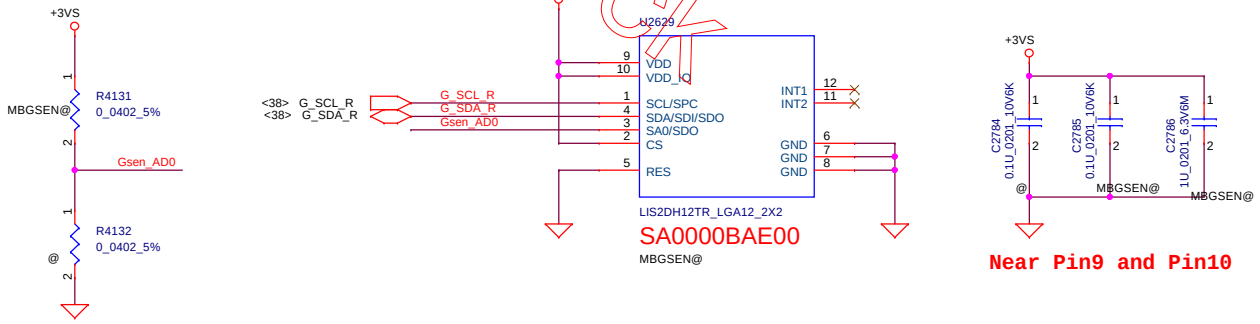
EH78 ACER check

To Hall sensor/B

Raptor



M/B Gsensor



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Compal Electronics, Inc.

Title: Sensors

Size: Custom | Document Number: EH78F M/B LA-G161PR01 | Rev: 0.1

Date: Wednesday, January 16, 2019 | Sheet 66 of 102

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Title: Reserve Page			
Size: Custom	Document Number: EH78F M/B LA-G161PR01		Rev: 0.1
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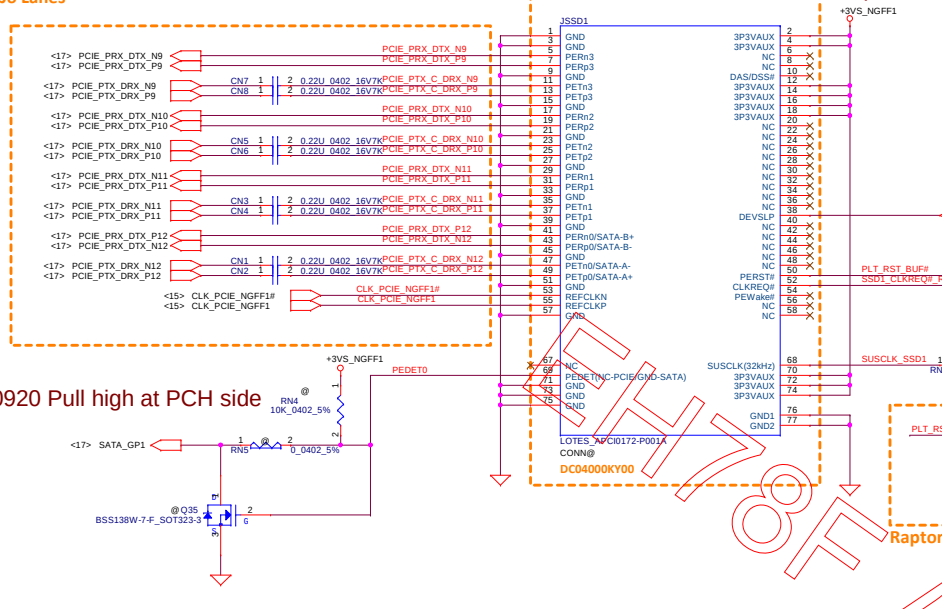
Raptor

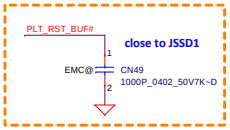
Raptor:LANE REVERSAL for SATA/PCIe Combo Lanes

SSD NGFF Slot_1 Key M

(left side)

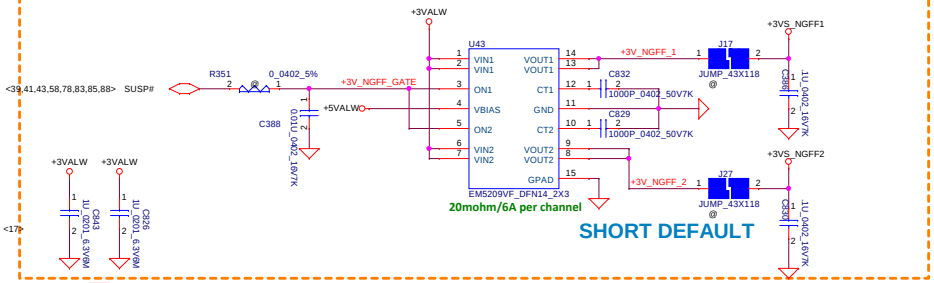


0920 Pull high at PCH side



Raptor:reserve for ESD

+3VS_NGFF PWR

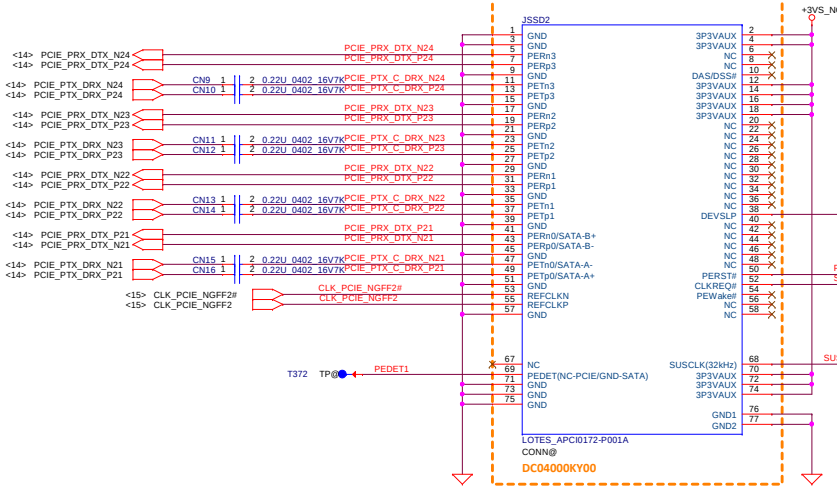


Raptor:Use +3VS

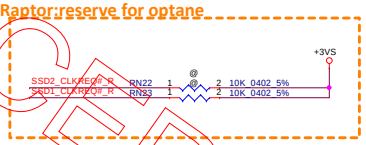
Raptor

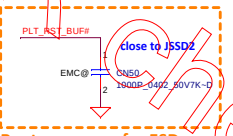
SSD NGFF Slot_2 Key M

(left side)

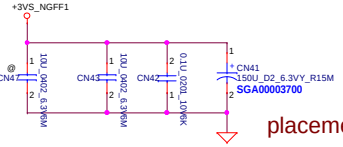


Raptor:reserve for optane





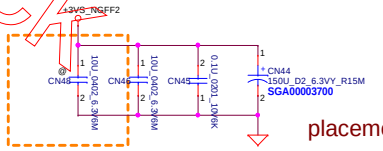
Raptor:reserve for ESD



placement close PCIE SSD side

Raptor:reserve

PEDET	Module Type
0	SATA
1	PCIE



placement close PCIE SSD side

Raptor:reserve

PEDET	Module Type
0	SATA
1	PCIE

ACTIVE CHECK

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: M.2 SSD_PCIe/SATA

Size | Document Number: EH78F M/B LA-G161PR01 | Rev: 0.1

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Size: Custom	Document Number: EH78F M/B LA-G161PR01	Rev: 0.1
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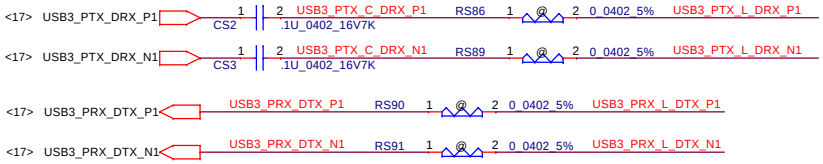
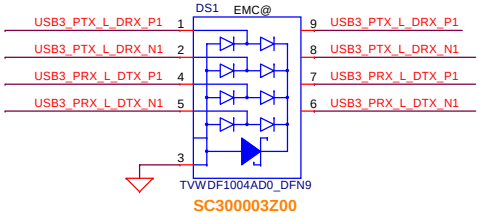
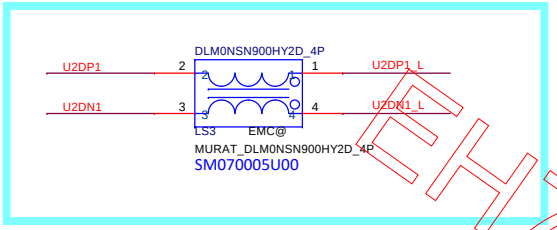
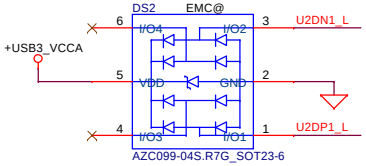
USB3.0 /2.0 CMC



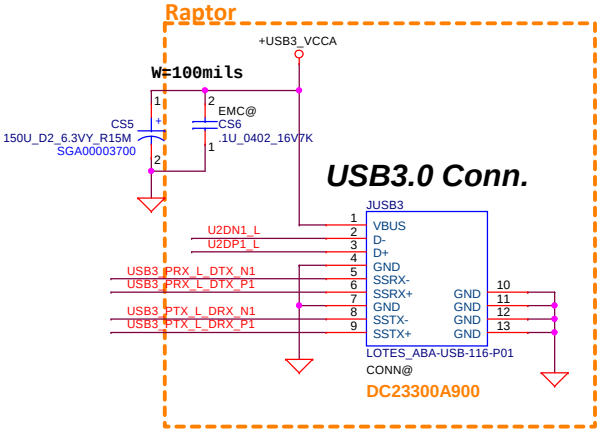




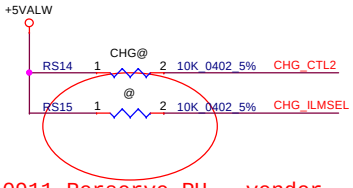
correct footprint to MURAT_DLM0NSN900HY2D_4P



Charger Port

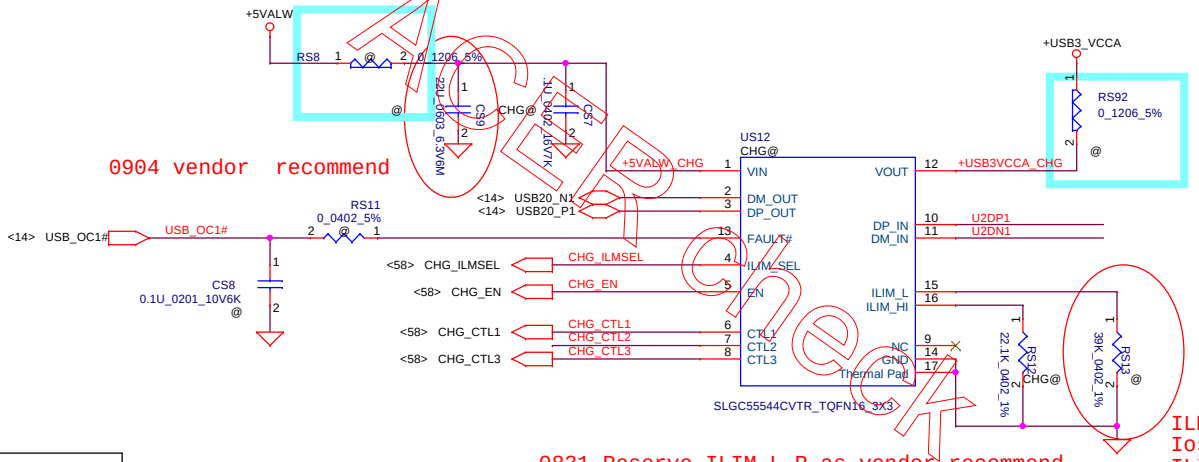


USB Host Charger



0911 Rerserve PU, vendor suggest to EC control if future need support SDP2

0904 vendor recommend



0831 Reserve ILIM_L R as vendor recommend

ILM R vaule
Ios(mA)=50250/R(Kohm)
ILIM_Hi=2273mA
ILIM_L=1288mA(reserve)

USB Host Charger Truth Table

CHG_EN	CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	Note
0	0	1	0	1	SDP1-OFF	ILIM_H	Port power off
1	0	1	0	1	SDP1	ILIM_H	Data Lines Connected
1	0	1	1	1	DCP Auto	ILIM_H	Data Lines Disconnected
1	1	1	1	1	CDP	ILIM_H	Data Lines Connected

EH78F Active

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Title: USB TYPEA with Charger

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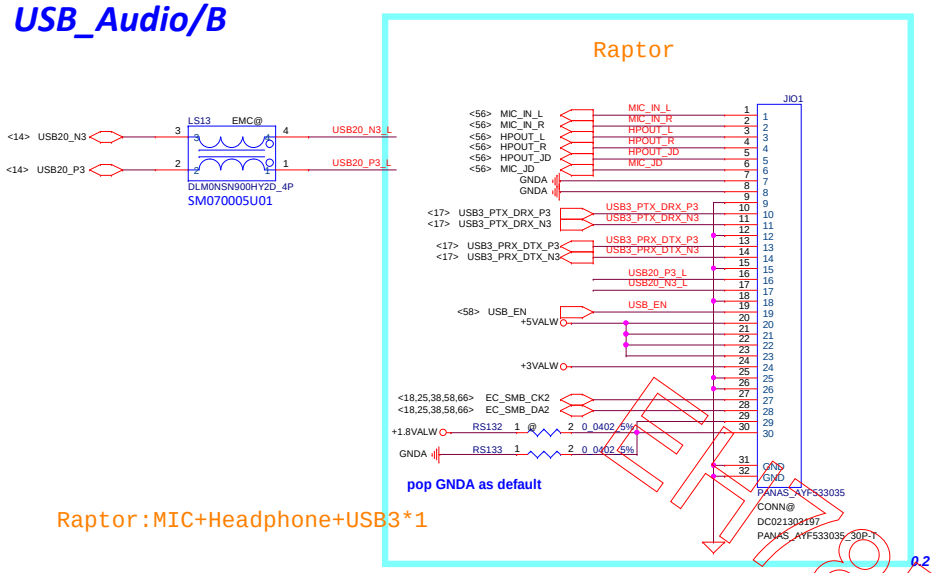
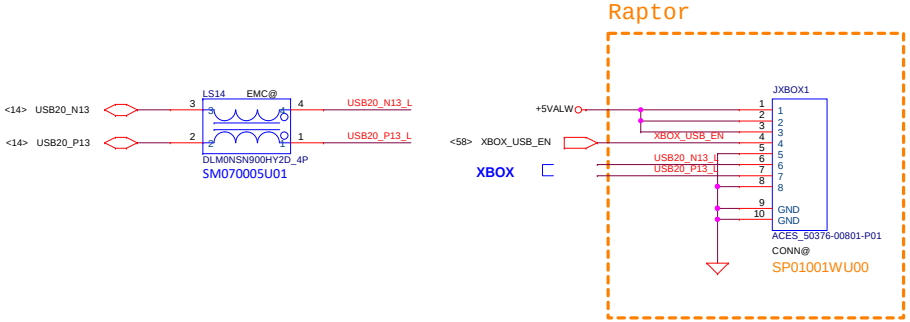
USB_Audio/B



Raptor:MIC+Headphone+USB3*1

XBOX/B



Raptor: 1*USB2.0

0.2

IP of ACER check

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Issued Date	2017/11/23	Deciphered Date 2018/09/01	Title: IO/XBOX DB
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Compal Electronics, Inc.		
Title: *eDP MUX*		
Size: C	Document Number: *EH78F M/B LA-G161PR01*	Rev: 0.1
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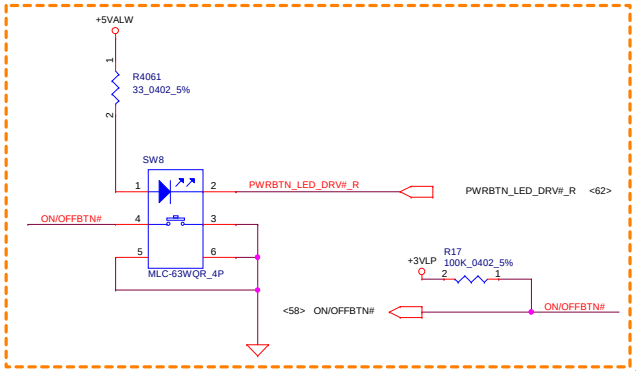
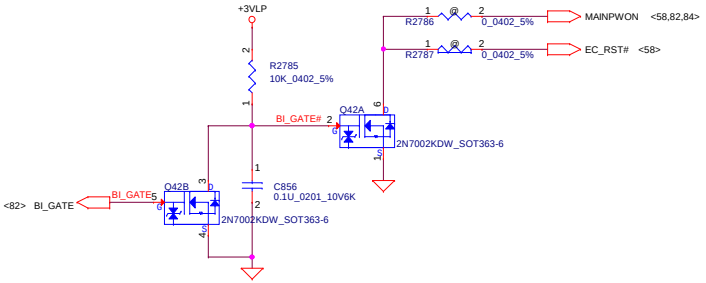
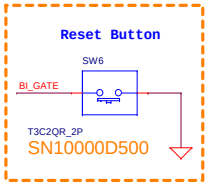
Power BTN Raptor:use MLC-63



Reset Circuit



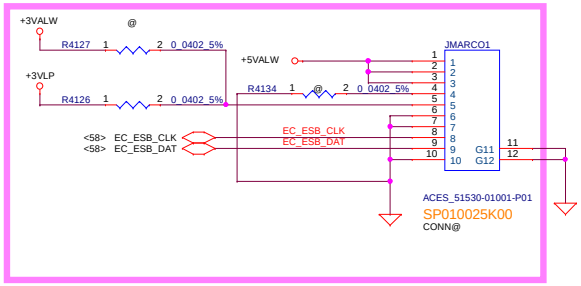
BI_GATE PH to +RTCVCC at PWR side



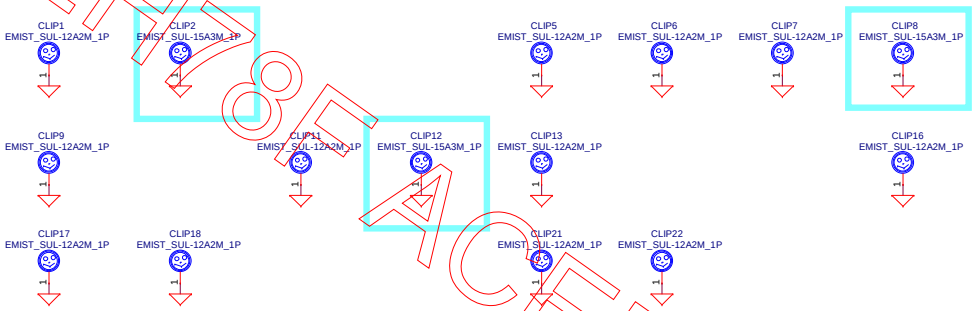
Raptor:use thin type

Macro Key

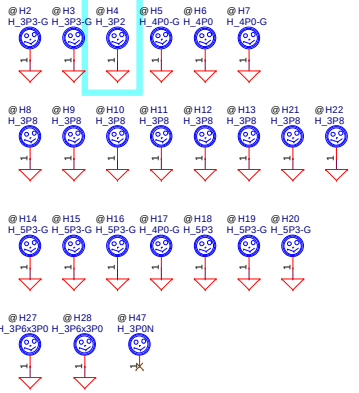
Raptor: use +3VLP as default



Clips

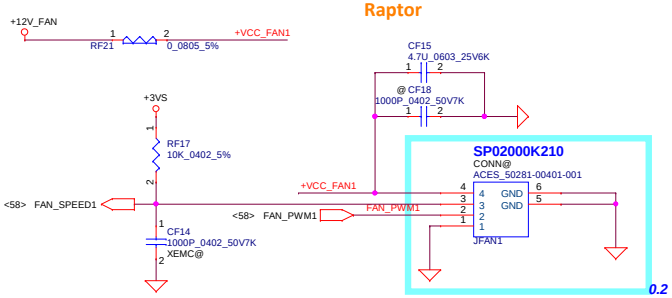


SCREW



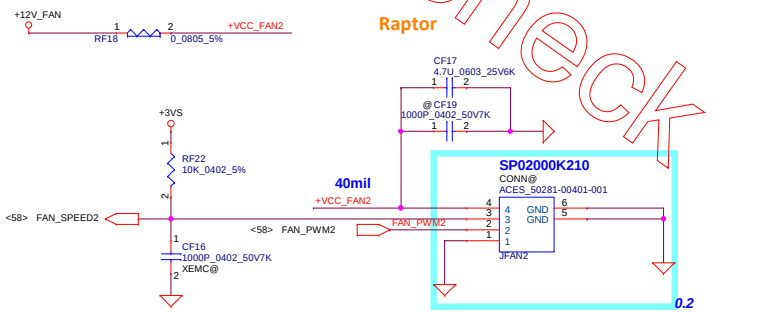
PCB P/N

CPU FAN Conn



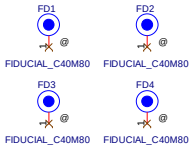
10/12 Thermal want reverse pin for common

GPU FAN Conn



10/12 Thermal want reverse pin for common

FD



ETHAN-ACER check

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Title	PWRBTN/PCB PN//SCREW/FAN
Size: Custom	Document Number: EH78F M/B LA-G161PR01
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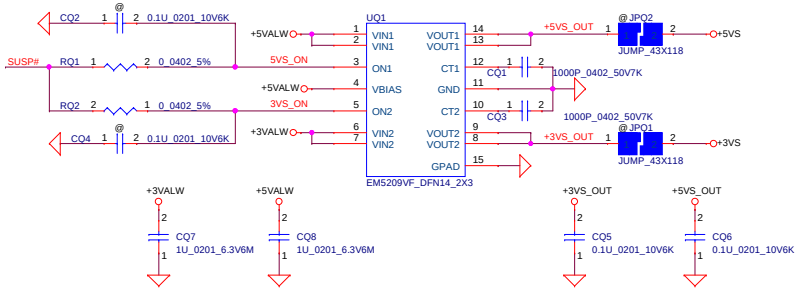
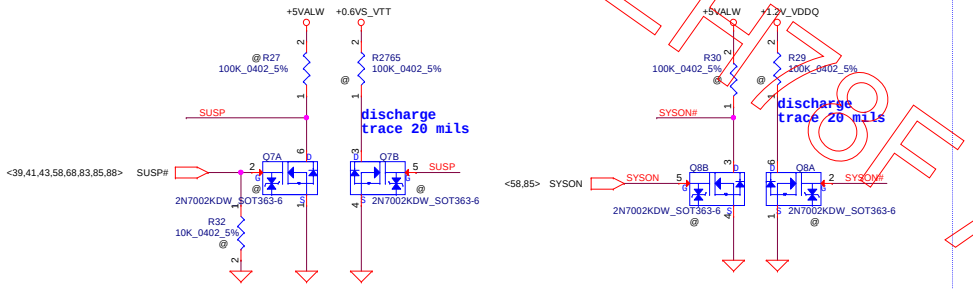
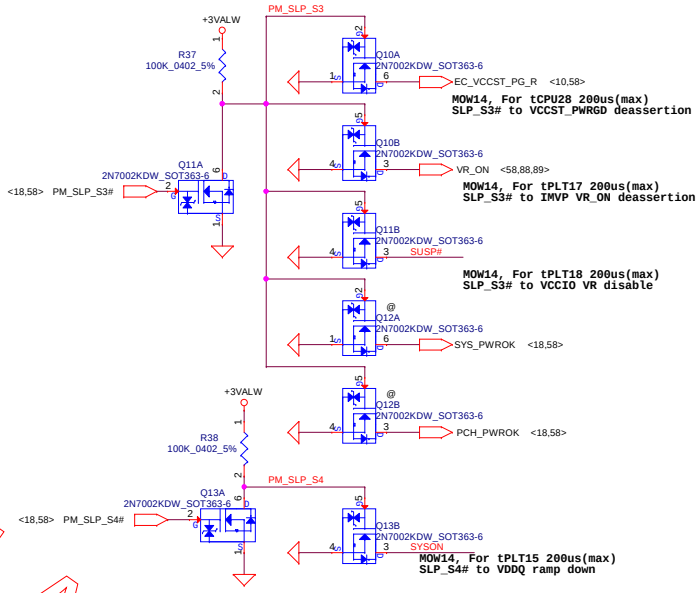
System DC inferface



Place CQ7 close UQ1 pin 1&2
Place CQ8 close UQ1 pin 6&7

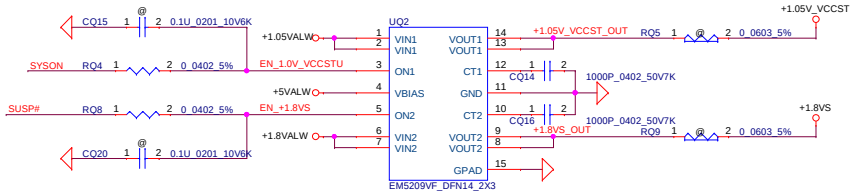


For Power ON/Off Sequence



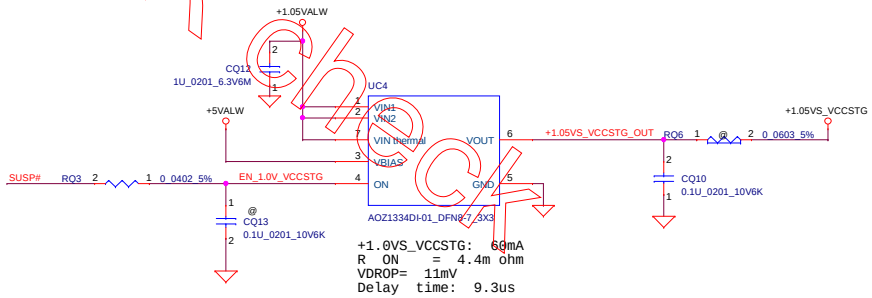
P/N: SB00000E000 footprint use SB00000ZU00

+1.05VALW TO +1.05V_VCCST /+1.8VALW TO +1.8VS



Place CQ11 close UQ2 pin 1&2
Place CQ24 close UQ2 pin 6&7

+1.05VALW TO +1.05VS_VCCSTG



+1.0VS_VCCSTG: 60mA
R ON = 4.4m ohm
VDROP= 11mV
Delay time: 9.3us

ETM SAMPLE

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Issued Date	2017/11/23	Deciphered Date 2018/09/01	Title: DC INTERFACE
			Size: Custom; Document Number: EH78F M/B LA-G161PR01; Rev: 0.1
			Date: Wednesday, January 16, 2019; Sheet 78 of 102

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Title: Reserve Page		
Size: Custom	Document Number: EH78F M/B LA-G161PR01	Rev: 0.1
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Compal Electronics, Inc.		
Title: Reserve Page		
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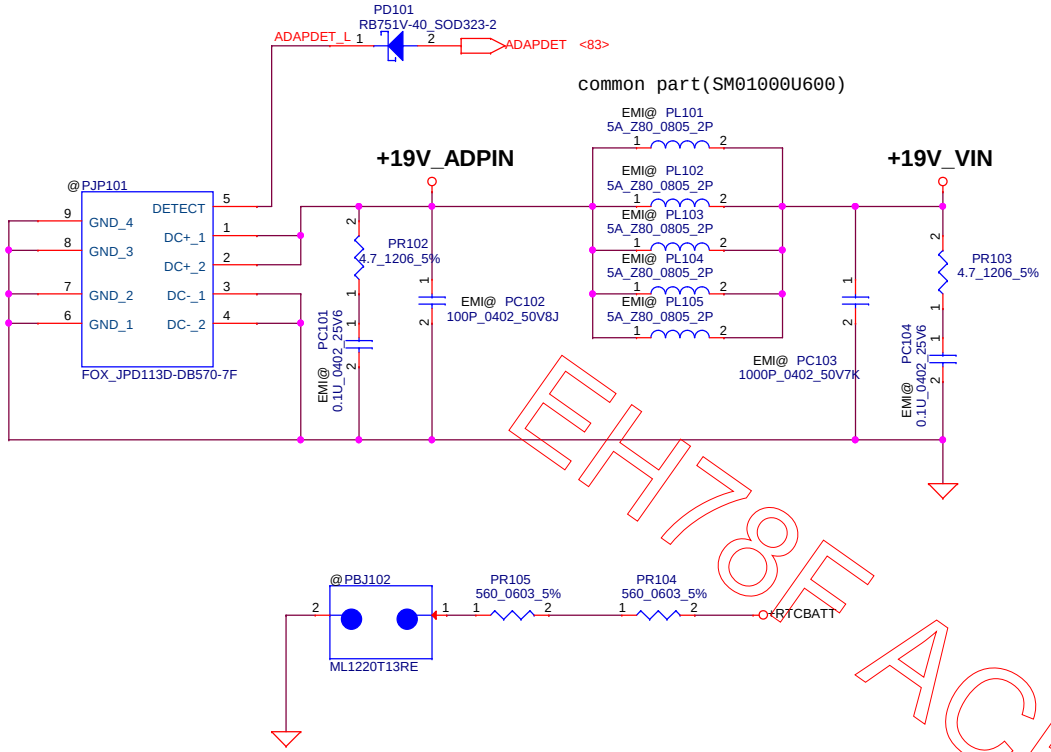

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Compal Electronics, Inc.

Title: ***PWR DCIN / RTC battery***

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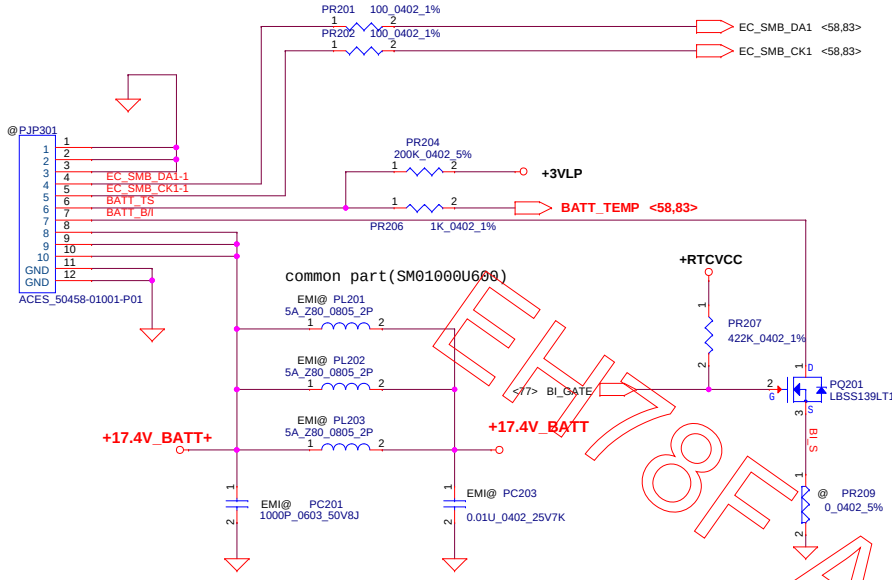
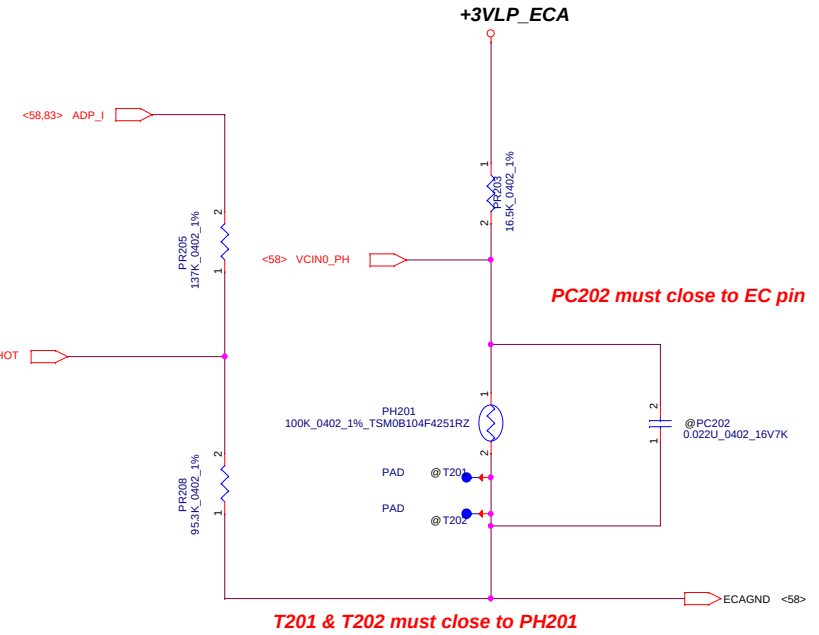


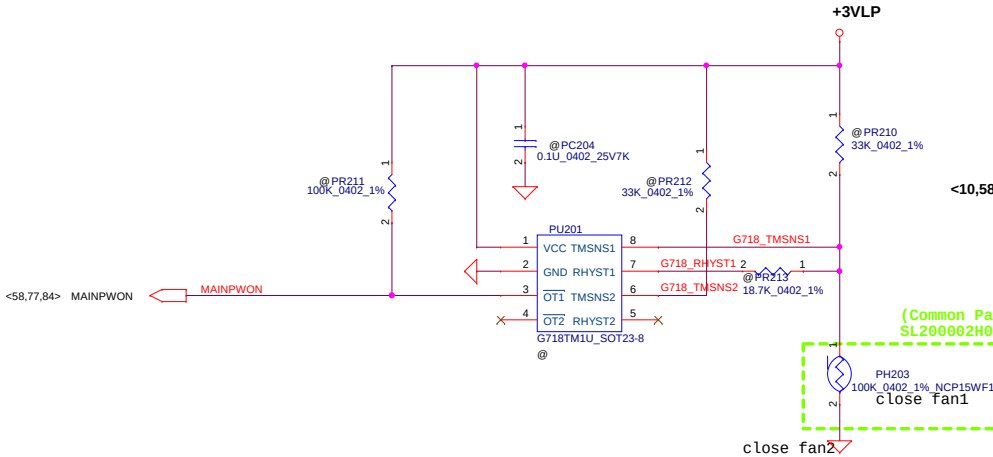


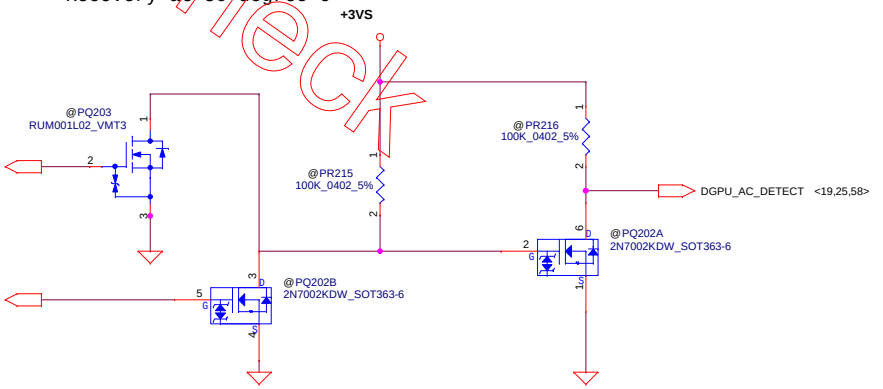

```
---Battery_pin define---
PIN1  GND
PIN2  GND
PIN3  GND
PIN4  SMD
PIN5  SMC
PIN6  TS
PIN7  B/I
PIN8  BATT+
PIN9  BATT+
PIN10 BATT+

---Battery Con_pin define---
PIN10  Batt+
PIN9   Batt+
PIN8   Batt+
PIN7   B/I
PIN6   TS
PIN5   SMC
PIN4   SMD
PIN3   GND
PIN2   GND
PIN1   GND
```

For KB9022 OTP	Active	Recovery
VCIN0_PH(V)	92C, 1V	56C, 2V
PH201(ohm)	7.3K	26.11K

For KB9022 sense 5mΩ	Active	Recovery
330W PR208=95.3Kohm	0.855V(495W)	0.855V(495W)

PH201 under CPU botten side :
CPU thermal protection at 92 degree C (shutdown)
Recovery at 56 degree C





IT178F ACER check

Security Classification	Compal Secret Data		
Issued Date	2016/02/01	Deciphered Date	2017/12/31

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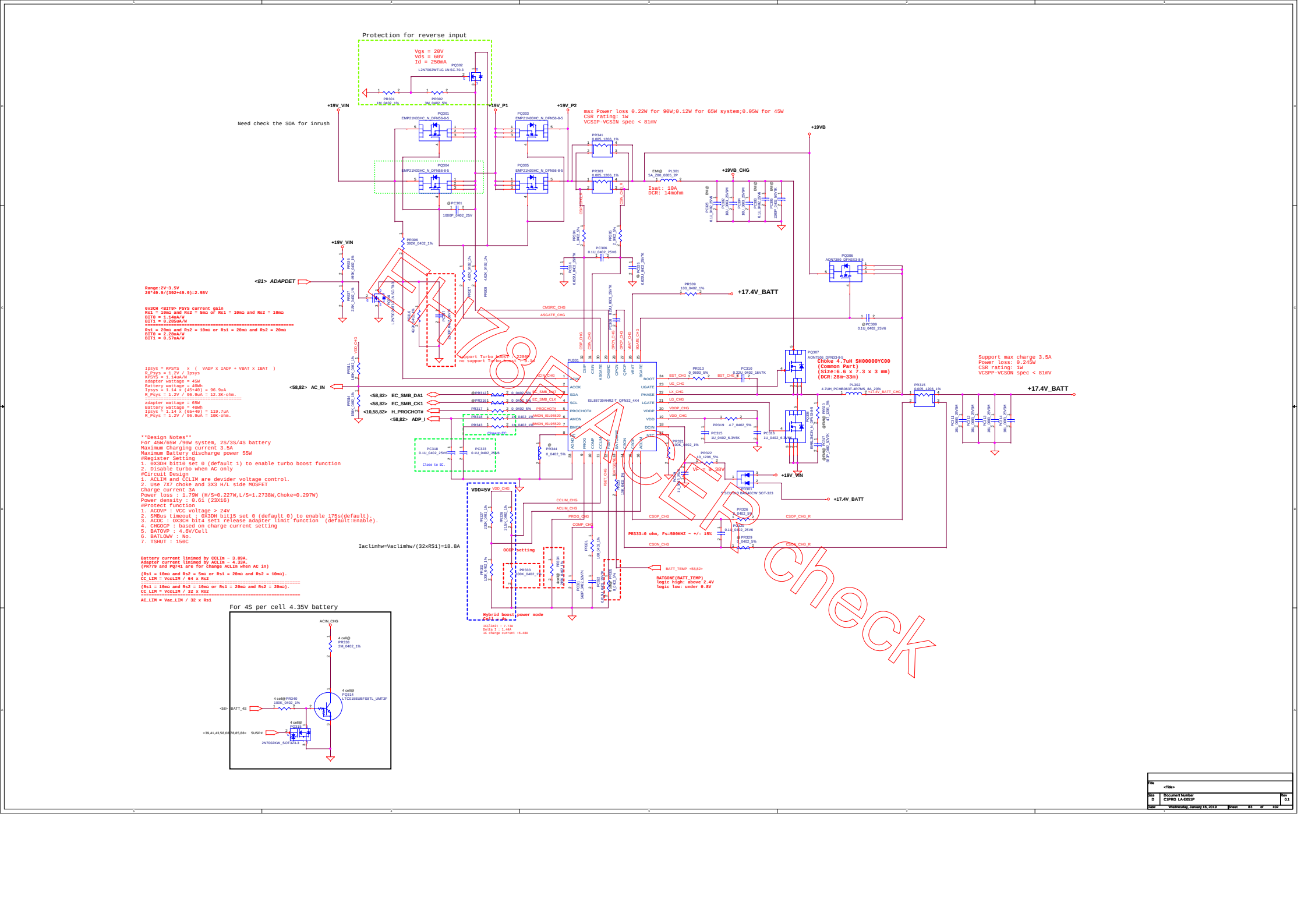
Compal Electronics, Inc.

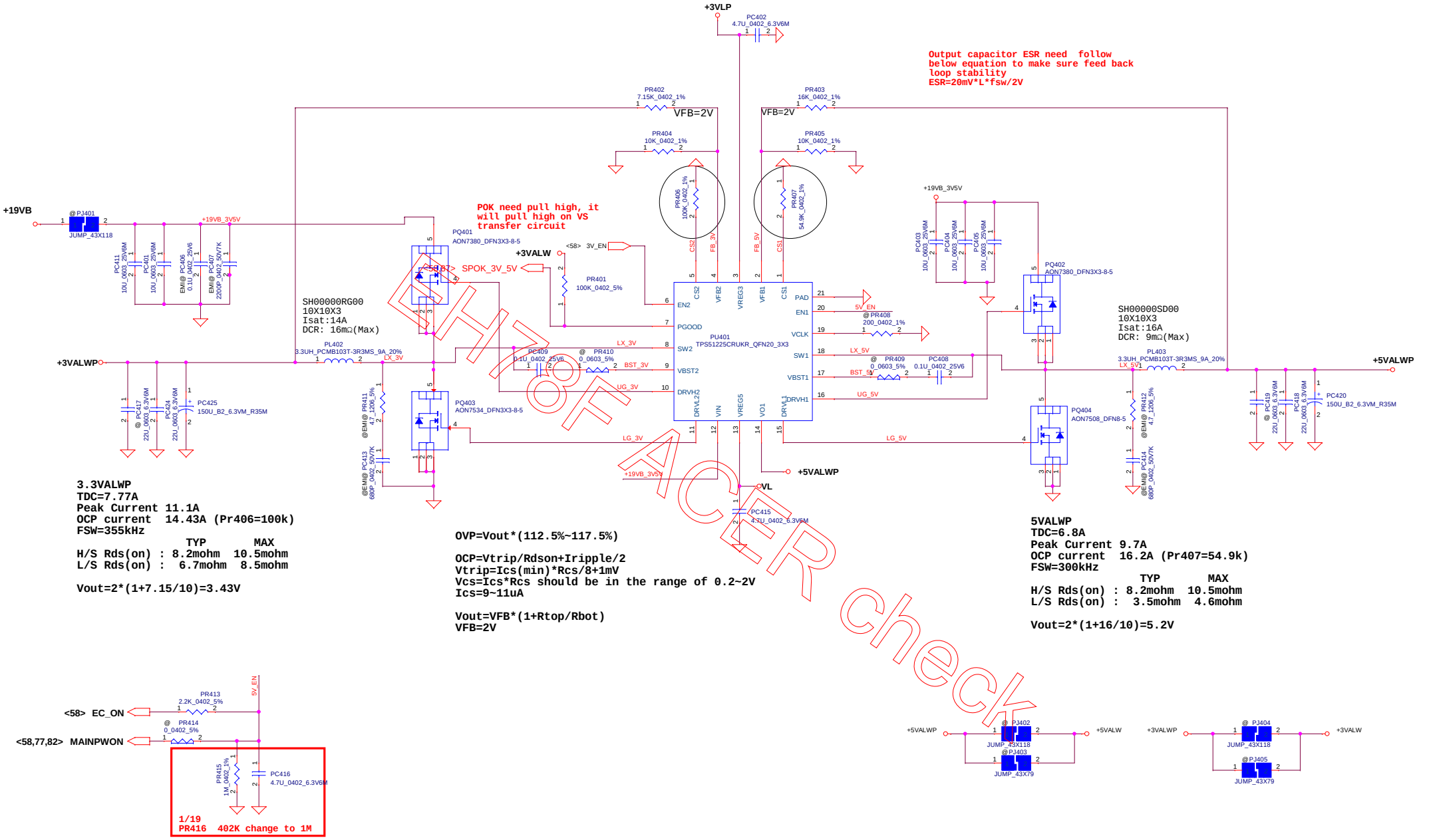
Title: PWR-BATTERY CONN/OTP

Size: Custom | Document Number: SKL_H 42 | Rev: 0.1

Date: Wednesday, January 16, 2019 | Sheet 82 of 102



Title	<Title>		
Size: D	Document Number: C1PRG LA-E051P		Rev: 0.1
Date: Wednesday, January 16, 2019	Sheet 83 of 102		



Security Classification	Compal Secret Data		
Issued Date	2016/02/01	Deciphered Date	2017/12/31

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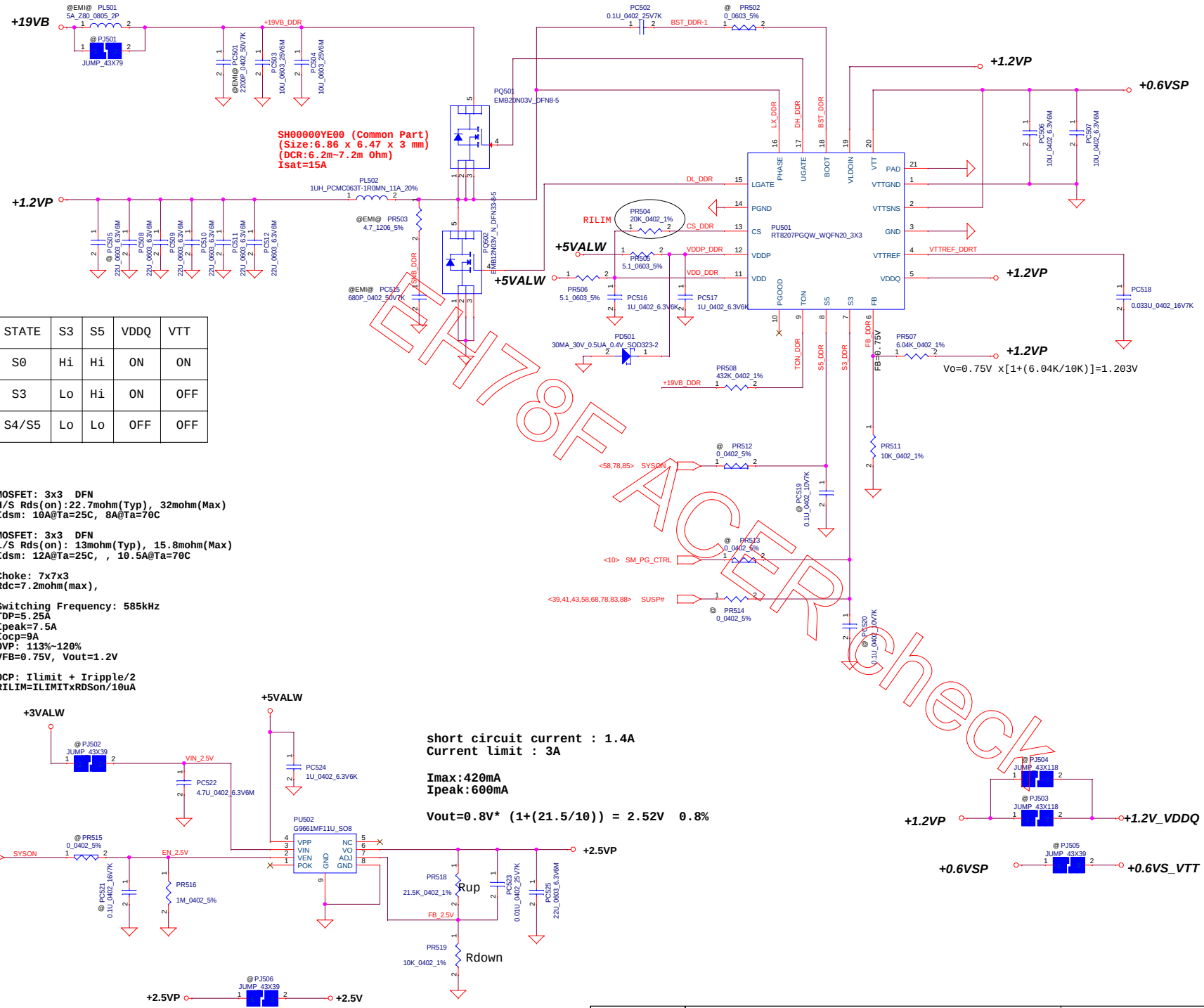
Compal Electronics, Inc.

Title: PWR_3V & 5VALWP

Size	Document Number	Rev
Custom		0.1

Date: Wednesday, January 16, 2019 Sheet 84 of 102



STATE	S3	S5	VDDQ	VTT
S0	Hi	Hi	ON	ON
S3	Lo	Hi	ON	OFF
S4/S5	Lo	Lo	OFF	OFF

MOSFET: 3x3 DFN
H/S Rds(on):22.7mohm(Typ), 32mohm(Max)
Idsm: 10A@Ta=25C, 8A@Ta=70C

MOSFET: 3x3 DFN
L/S Rds(on): 13mohm(Typ), 15.8mohm(Max)
Idsm: 12A@Ta=25C, , 10.5A@Ta=70C

Choke: 7x7x3
Rdc=7.2mohm(max),

Switching Frequency: 585kHz
TDP=5.25A
Ipeak=7.5A
Iocp=9A
OVP: 113%~120%
VFB=0.75V, Vout=1.2V

OCP: Ilimit + Iripple/2
RILIM=ILIMITxRDSon/10uA

short circuit current : 1.4A
Current limit : 3A

Imax:420mA
Ipeak:600mA

Vout=0.8V* (1+(21.5/10)) = 2.52V 0.8%

ER178F ACER check

Security Classification	Compal Secret Data		
Issued Date	2016/02/01	Deciphered Date	2017/12/31

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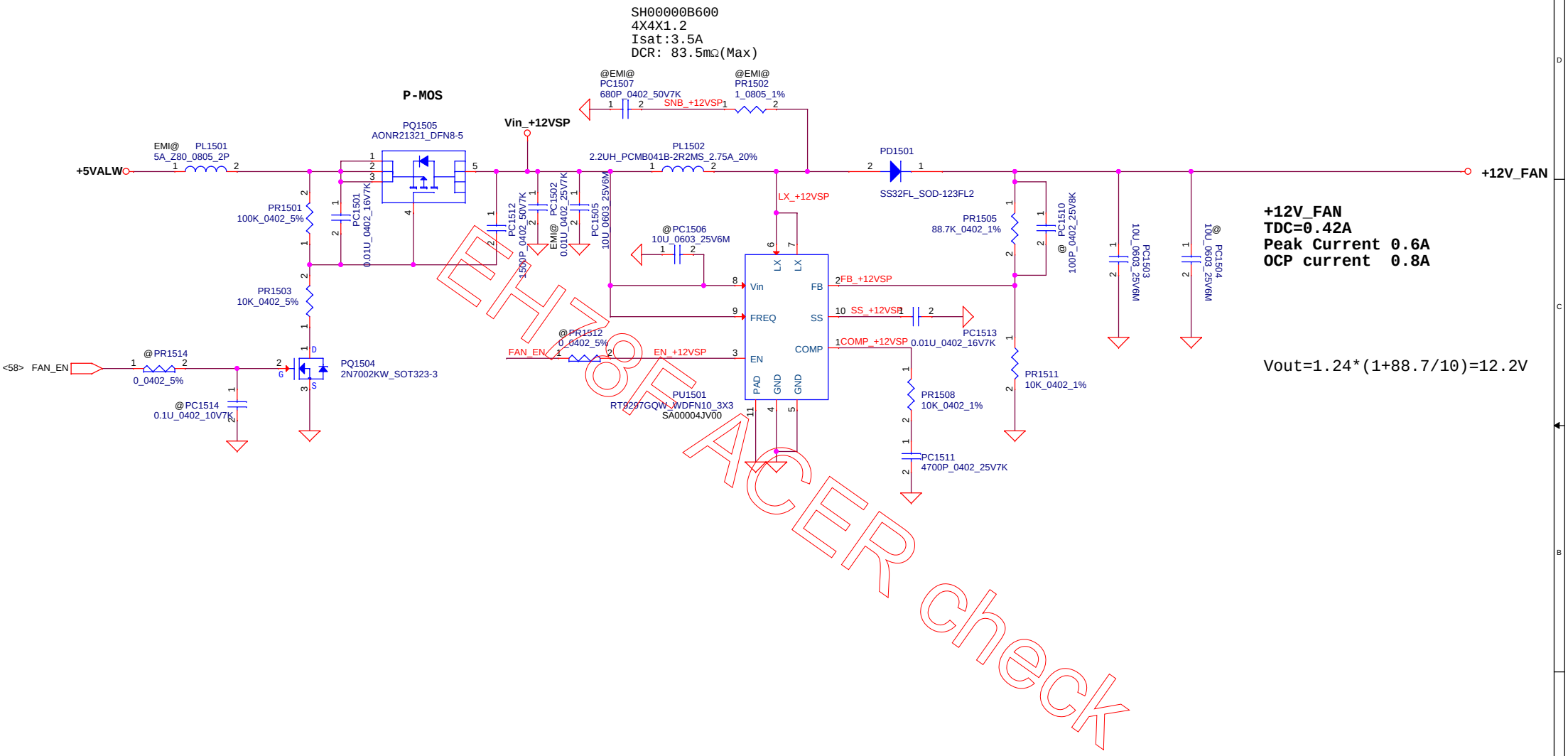
Title: **DDR RT8207P**

Size	Document Number	Rev
Custom		0.1

Date: Wednesday, January 16, 2019 Sheet 85 of 102



ETHOS ACER check

Security Classification	Compal Secret Data		
Issued Date	2016/02/01	Deciphered Date	2017/12/31

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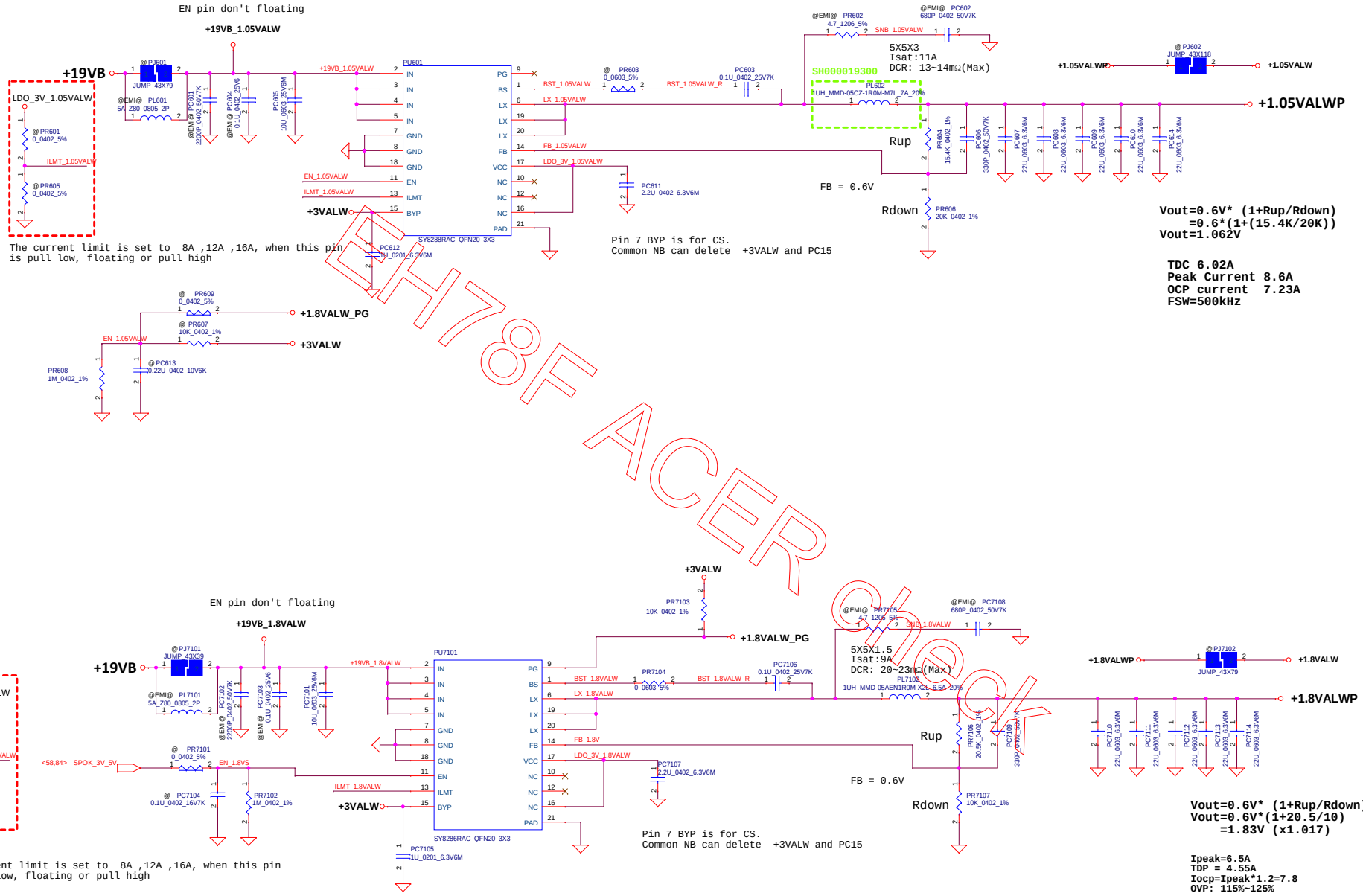
Title	2.5V / FAN 12V		
Size B	Document Number		Rev 0.1
Date: Wednesday, January 16, 2019	Sheet 86 of 102		



EH78F ACER OK

Security Classification	Compal Secret Data		
Issued Date	2016/02/01	Deciphered Date	2017/12/31

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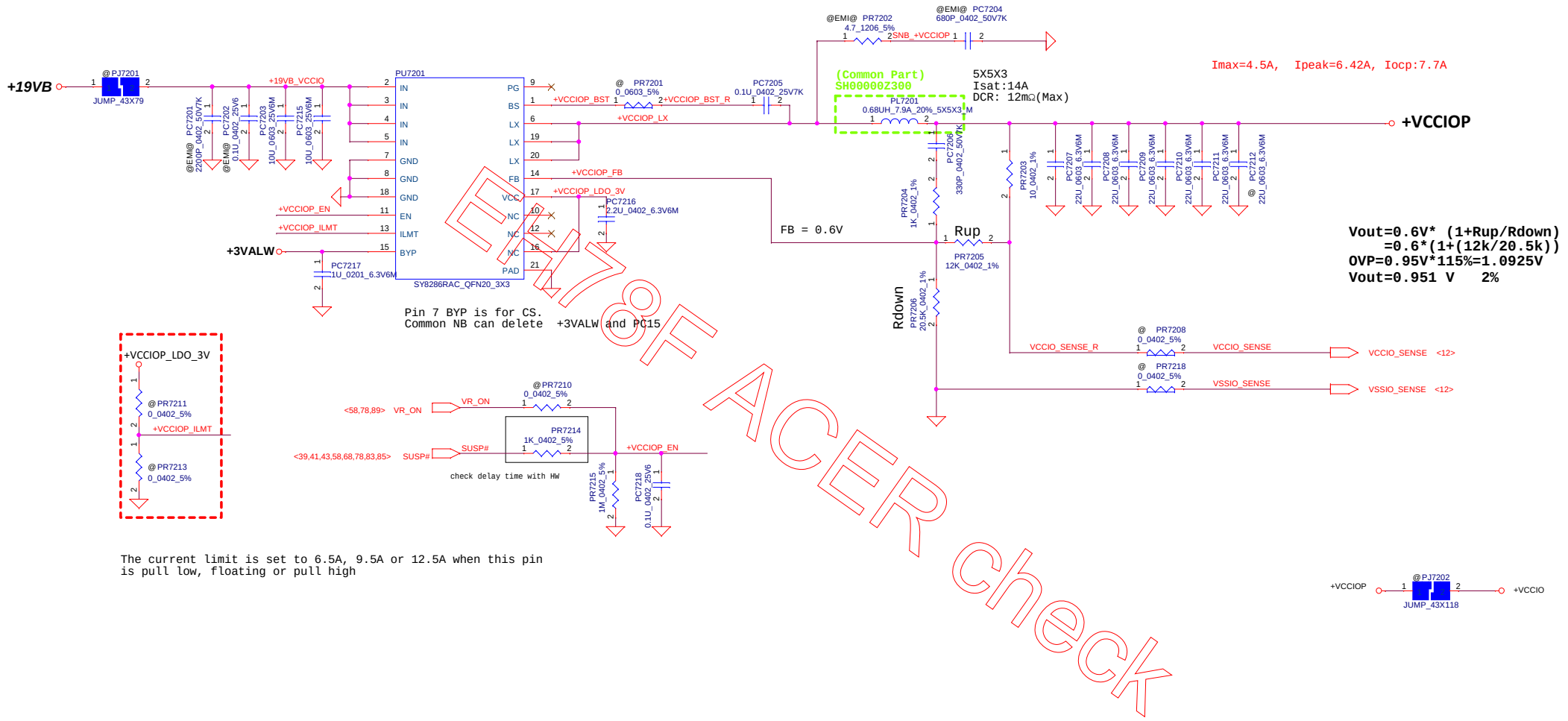
Compal Electronics, Inc.

Title: +1.0VALWP / +1.8VSP

Size	Document Number	Rev
C	C1PRG LA-E051P	0.1

Date: Wednesday, January 16, 2019 Sheet 87 of 102



ENTRY OF ACER check

Security Classification	Compal Secret Data		
Issued Date	2016/02/01	Deciphered Date	2017/12/31

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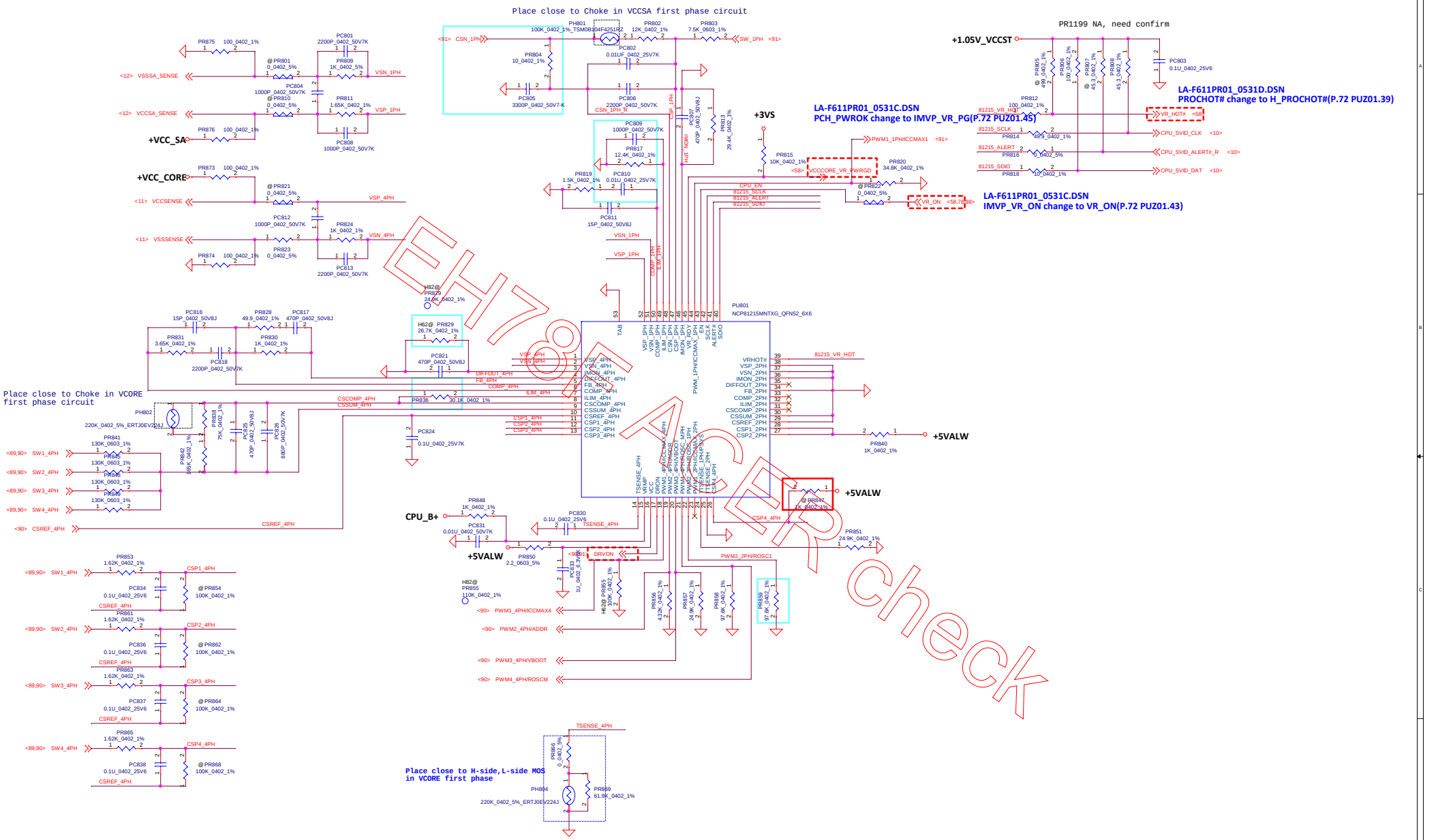
Title	0.95VS		
Size: Custom	Document Number		Rev: 0.1
Date: Wednesday, January 16, 2019	Sheet 88 of 102		



Security Classification	Compal Secret Data		
Issued Date	2016/02/01	Deciphered Date	2017/12/31

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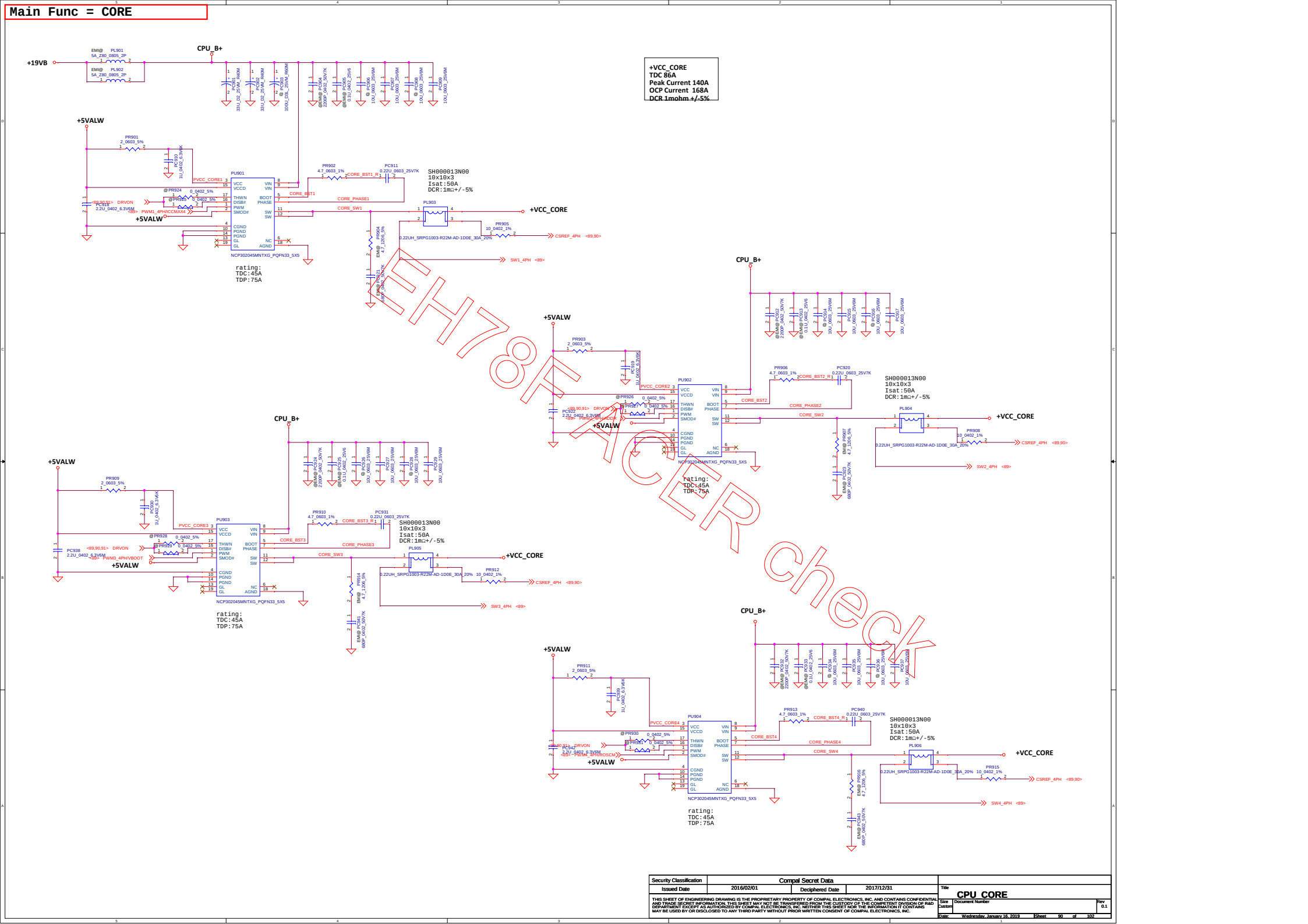
Compal Electronics, Inc.

Size	Document Number	Rev
Custom	CPU IC SKL_H 42	0.1

Date: Wednesday, January 16, 2019 Sheet 89 of 102

Main Func = CORE



WITH78ACTR check

Security Classification	Compal Secret Data		
Issued Date	2016/02/01	Deciphered Date	2017/12/31

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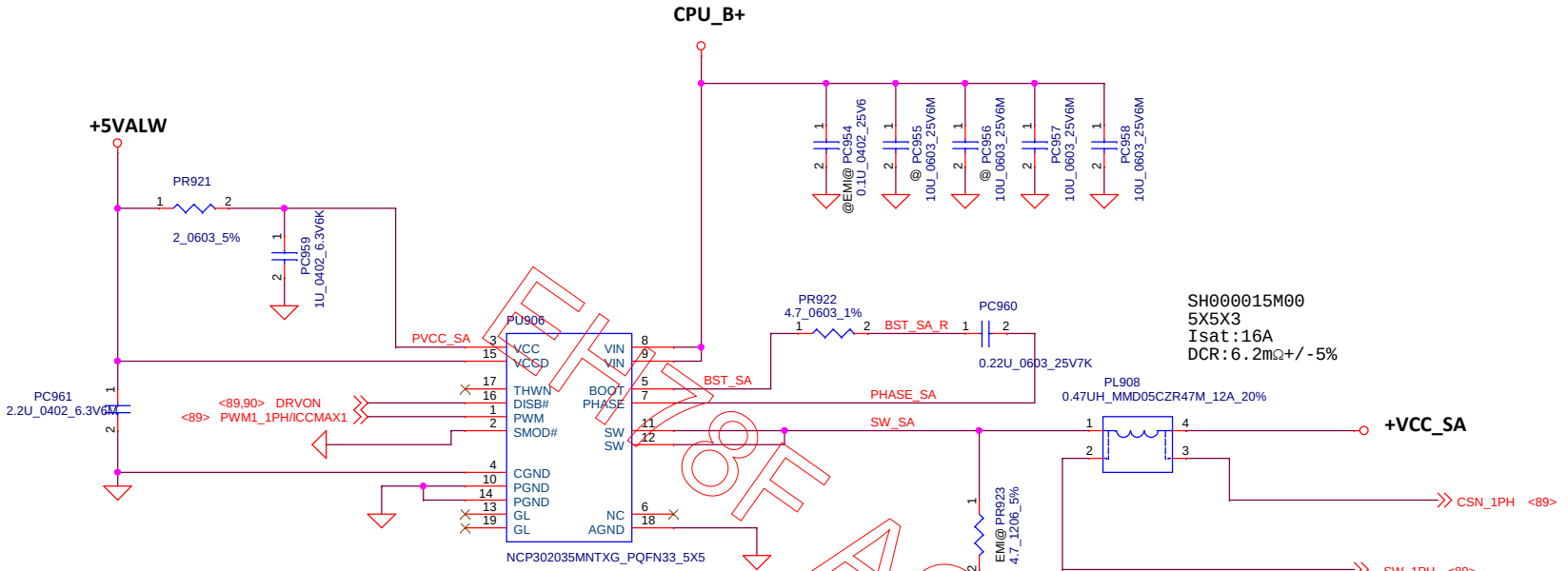
Title: CPU_CORE

Size: Custom | Document Number | Rev: 0.1

Date: Wednesday, January 16, 2019 | Sheet 90 of 102

Main Func = VCCGT/+VCCSA



SH000015M00
5X5X3
Isat:16A
DCR:6.2mΩ+/-5%

+VCCSA
TDC PL2 :10A
Peak Current 11A
OCP Current 13A
DCR 6.2mohm +/-5%
Load Line 10.3mV/A

ETS of ACER check

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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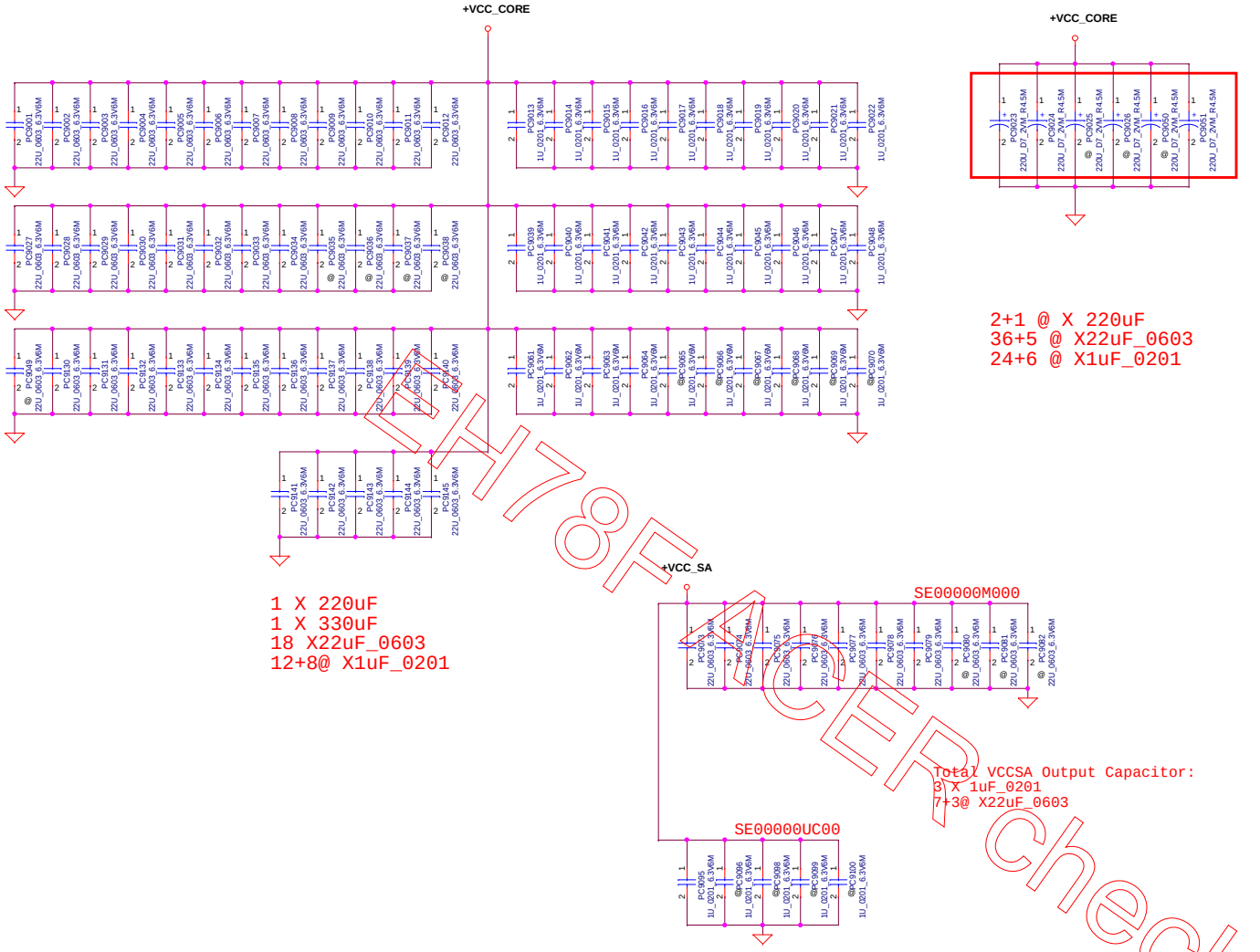
Compal Electronics, Inc.

Title: **+VCC_GT/+VCC_SA**

Size | Document Number: **C1PRG LA-E051P** | Rev: 0.1

Date: Wednesday, January 16, 2019 | Sheet 91 of 102



KL78F ACER check

Security Classification	Compal Secret Data		
Issued Date	2016/02/01	Deciphered Date	2017/12/31

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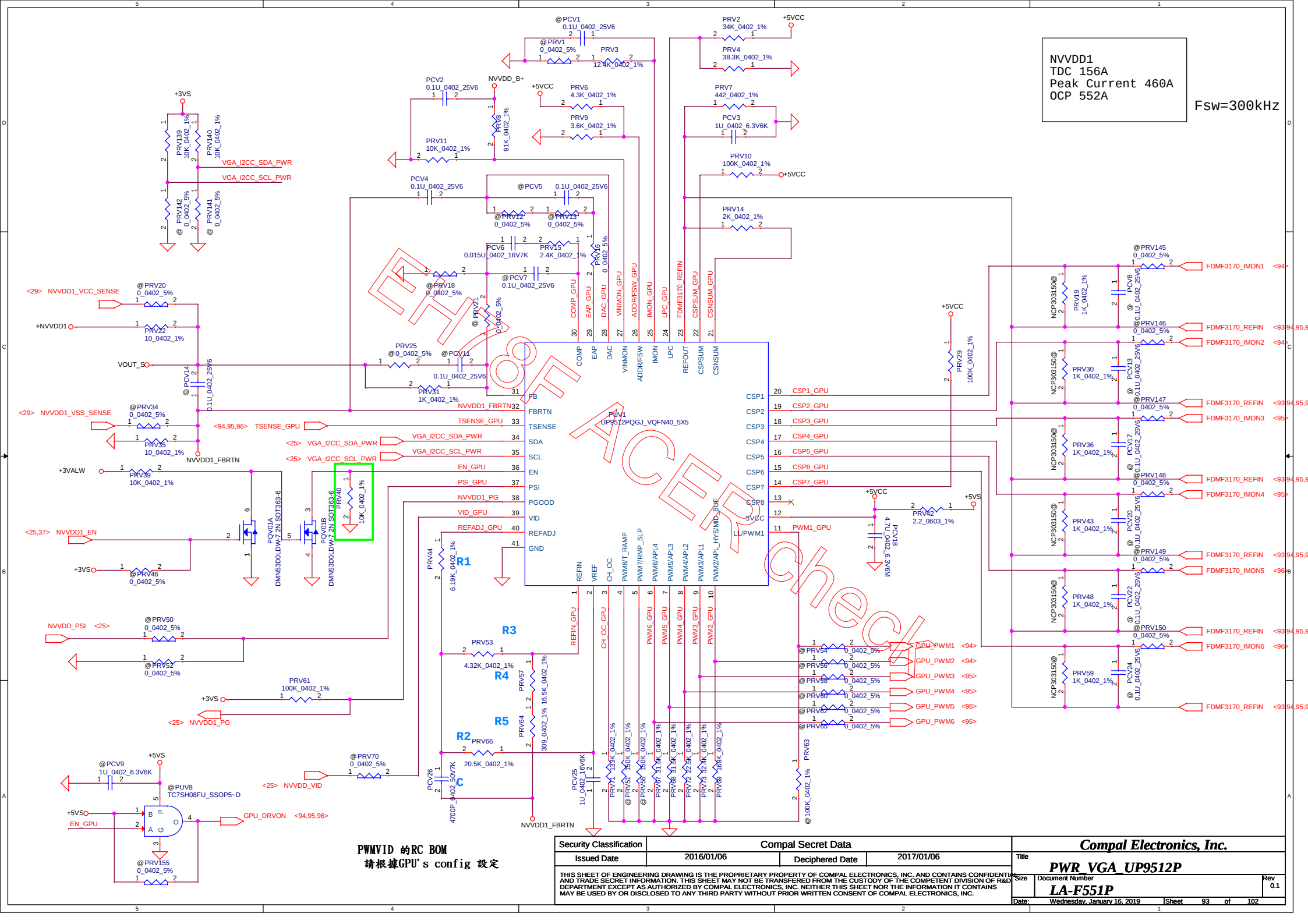
Title: **Processor decoupling**

Size	Document Number	Rev
Custom		SKL_H 42

Date: Wednesday, January 16, 2019 | Sheet 92 of 102



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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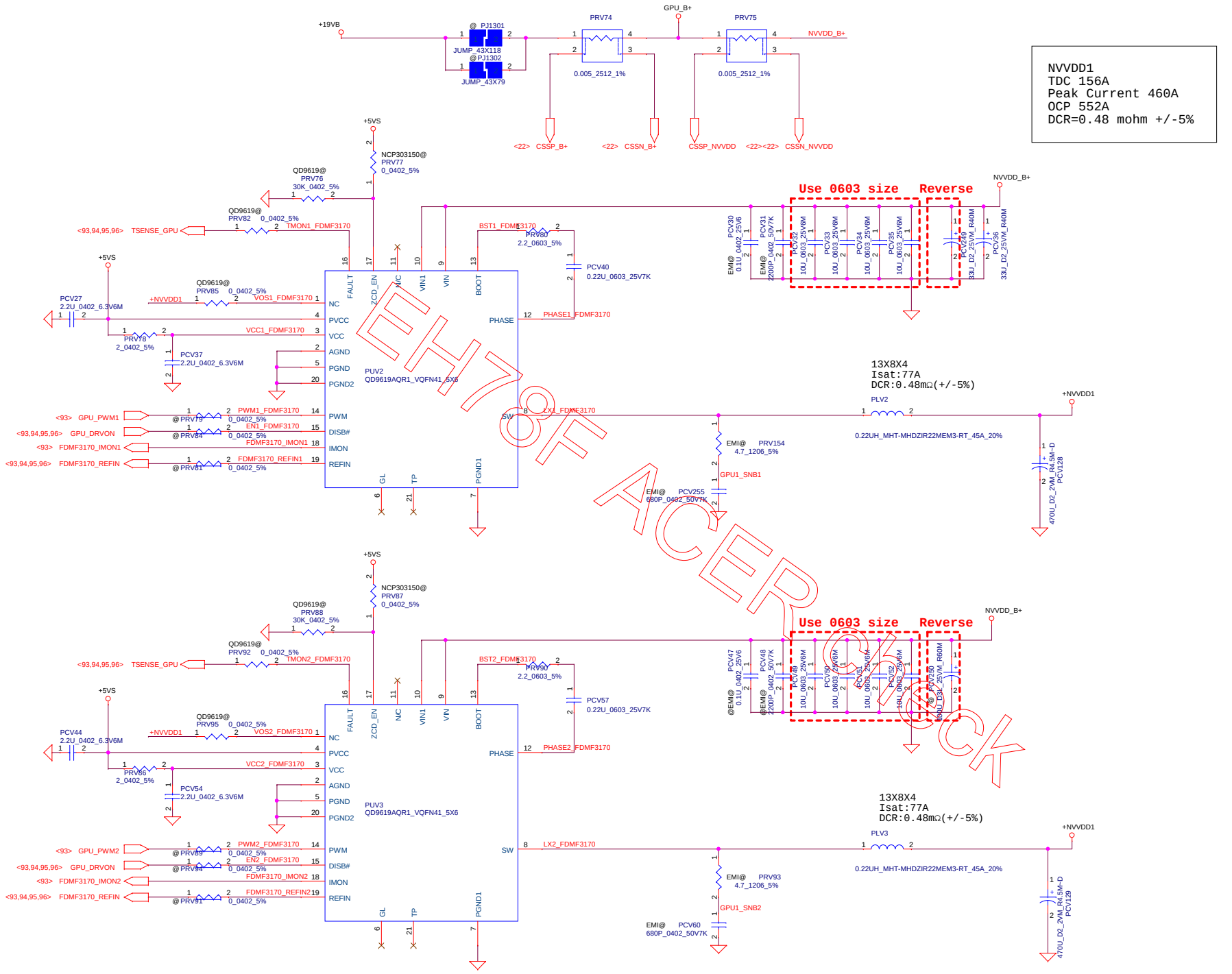
Compal Electronics, Inc.

Title: **PWR_VGA_UP9512P**

Size: | Document Number: **LA-F551P** | Rev: 0.1

Date: Wednesday, January 16, 2019 | Sheet 93 of 102



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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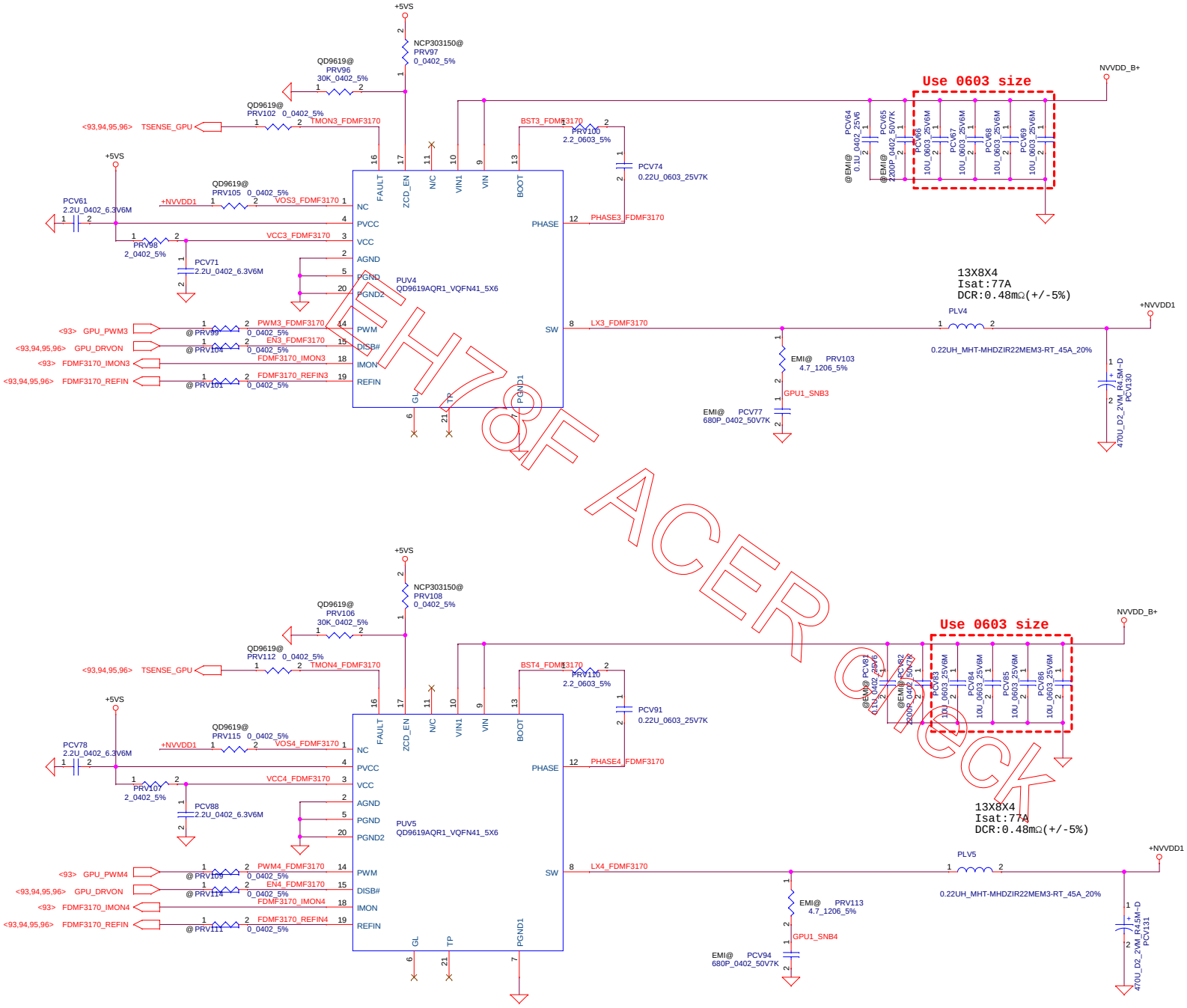
Compal Electronics, Inc.

Title: **PWR_+NVVDD1**

Size	Document Number	Rev
	LA-F551P	0.1

Date: Wednesday, January 16, 2019 | Sheet 94 of 102



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Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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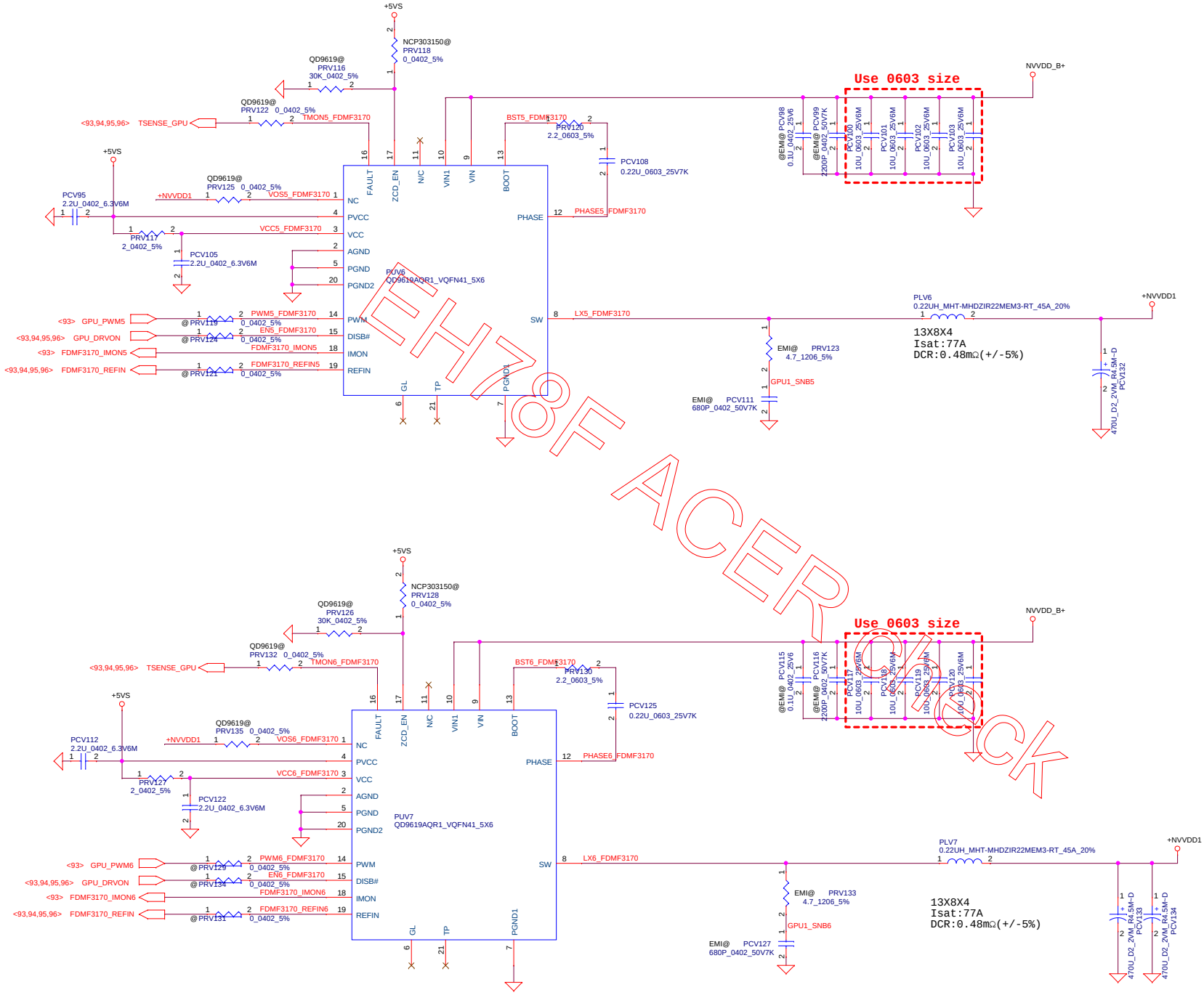
Compal Electronics, Inc.	
Title	PWR_+NVVDD1
Size	Document Number: LA-F551P
Rev	0.1
Date:	Wednesday, January 16, 2019
Sheet	95 of 102



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Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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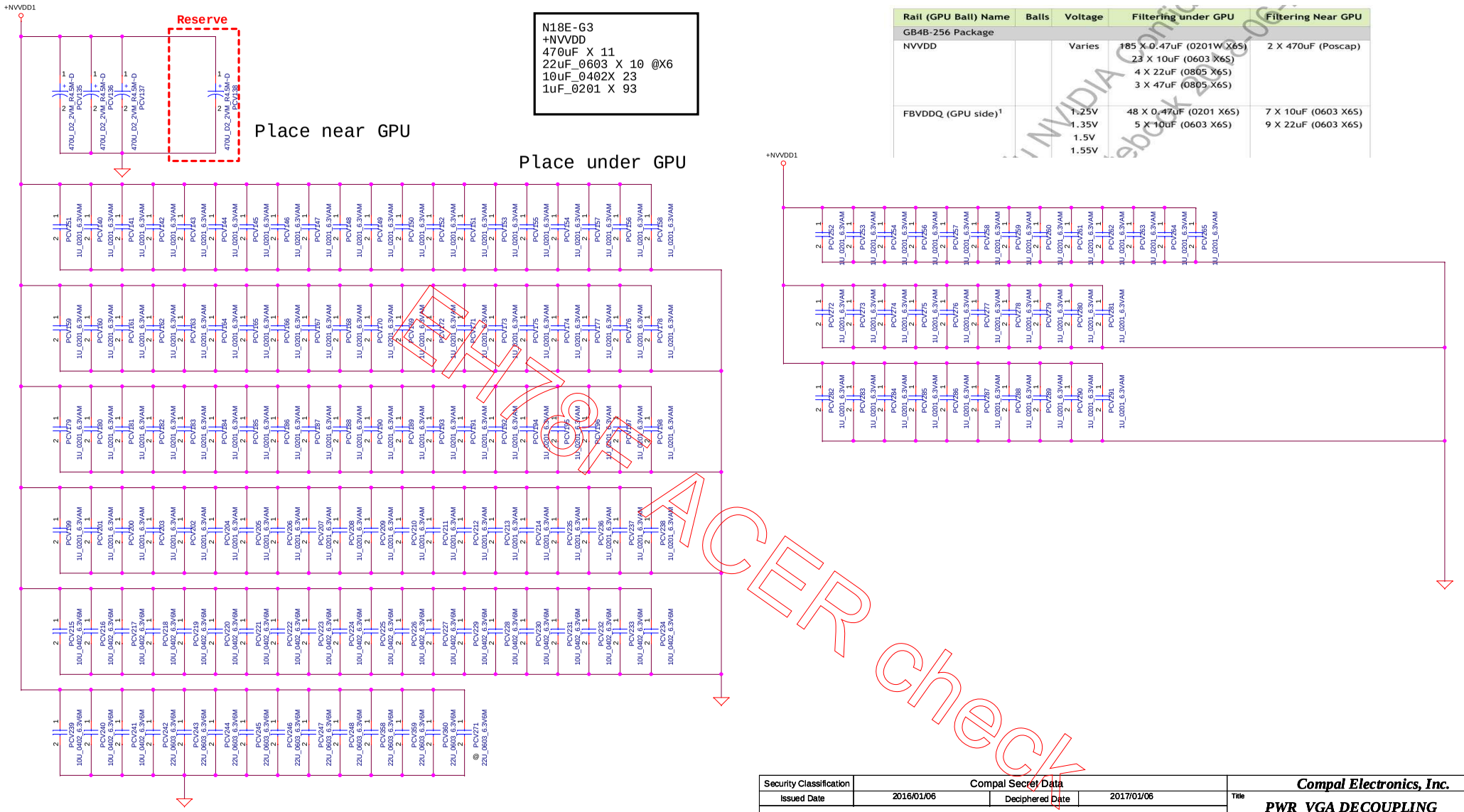
Compal Electronics, Inc.

Title: **PWR_+NVVDD1**

Size	Document Number	Rev
	LA-F551P	0.1

Date: Wednesday, January 16, 2019 | Sheet 96 of 102



Rail (GPU Ball) Name	Balls	Voltage	Filtering under GPU	Filtering Near GPU
GB4B-256 Package				
NVVDD		Varies	185 X 0.47uF (0201W X6S) 23 X 10uF (0603 X6S) 4 X 22uF (0805 X6S) 3 X 47uF (0805 X6S)	2 X 470uF (Poscap)
FBVDDQ (GPU side)[1]		1.25V 1.35V 1.5V 1.55V	48 X 0.47uF (0201 X6S) 5 X 10uF (0603 X6S)	7 X 10uF (0603 X6S) 9 X 22uF (0603 X6S)

NVIDIA Confidential
Feedback 2018-08-06
ACER check

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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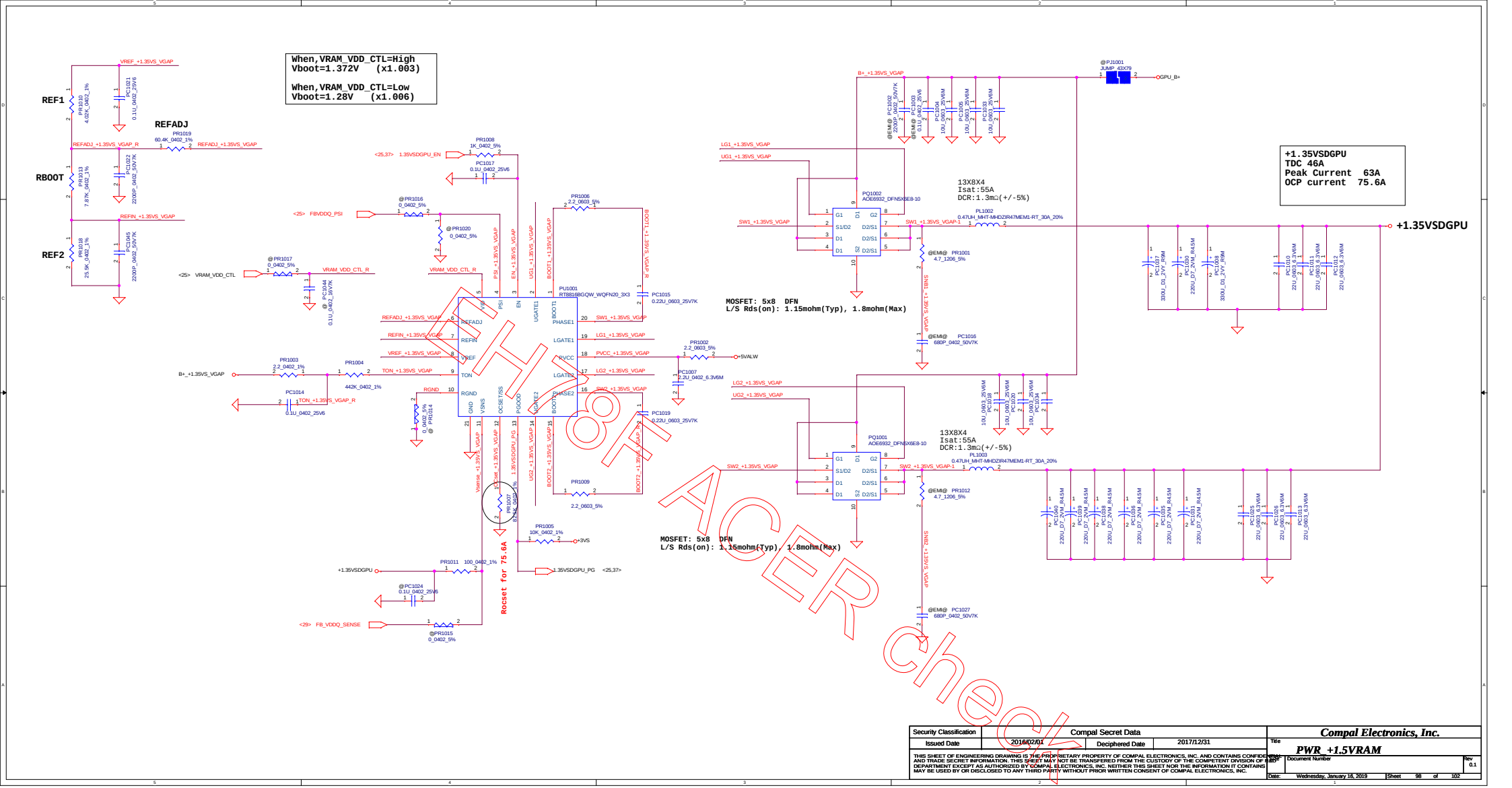
Compal Electronics, Inc.

Title: **PWR_VGA DECOUPLING**

Size | Document Number: **LA-F551P** | Rev: 0.1

Date: Wednesday, January 16, 2019 | Sheet 97 of 102



Security Classification	Compal Secret Data		
Issued Date	2016/02/01	Deciphered Date	2017/12/31

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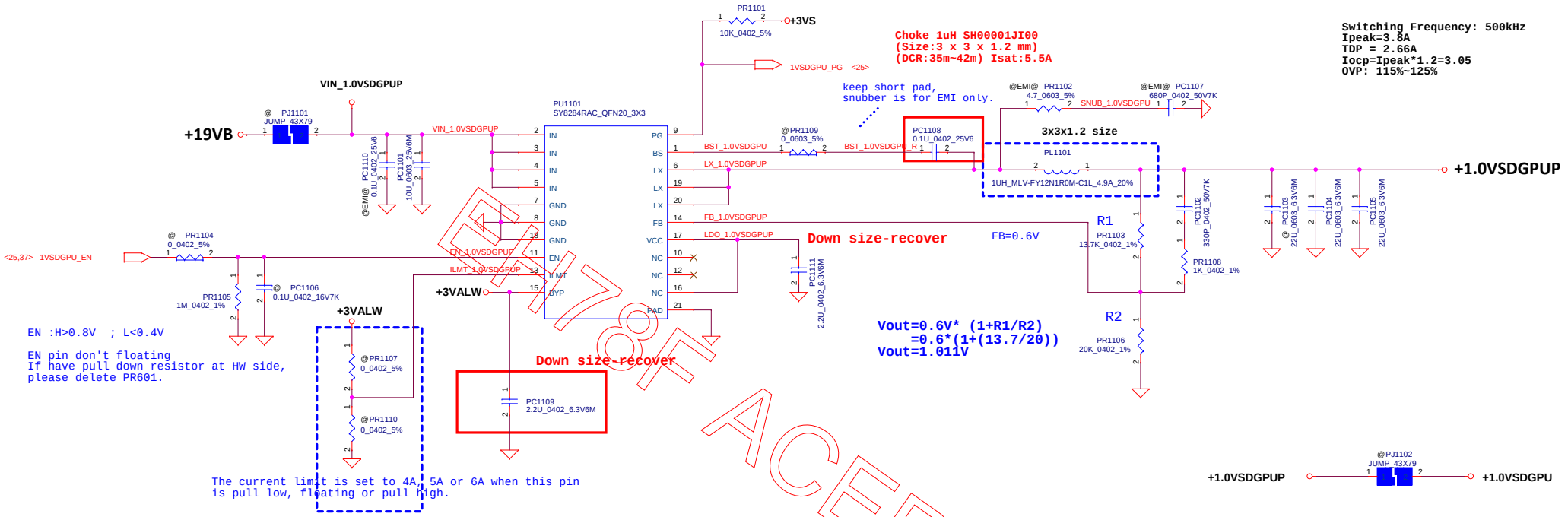
Compal Electronics, Inc.

Title: **PWR_+1.5VRAM**

Size: B | Document Number | Rev: 0.1

Date: Wednesday, January 16, 2019 | Sheet 98 of 102

SKL_H 42



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Security Classification	Compal Secret Data		
Issued Date	2016/02/01	Deciphered Date	2017/12/31

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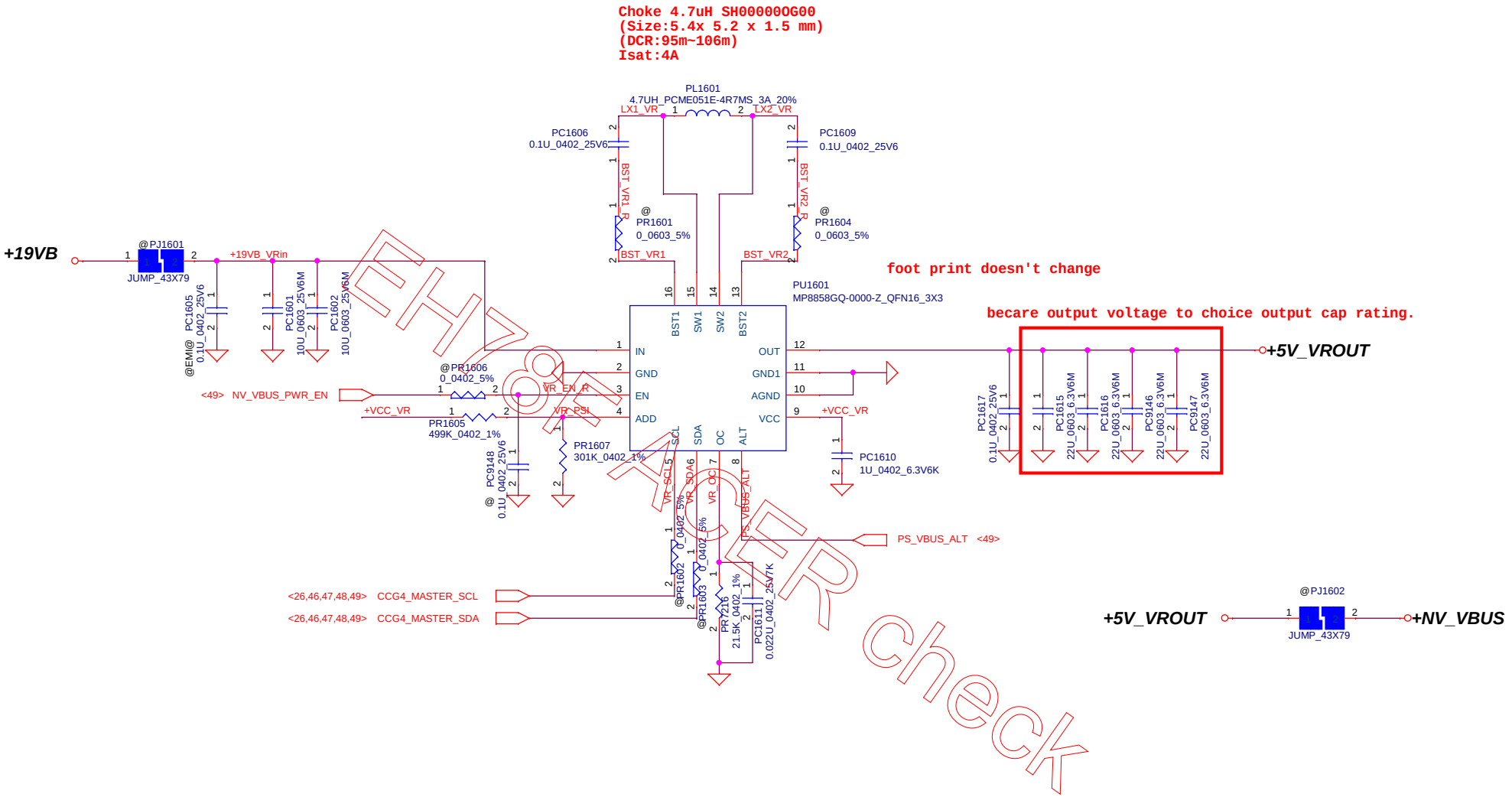
Compal Electronics, Inc.

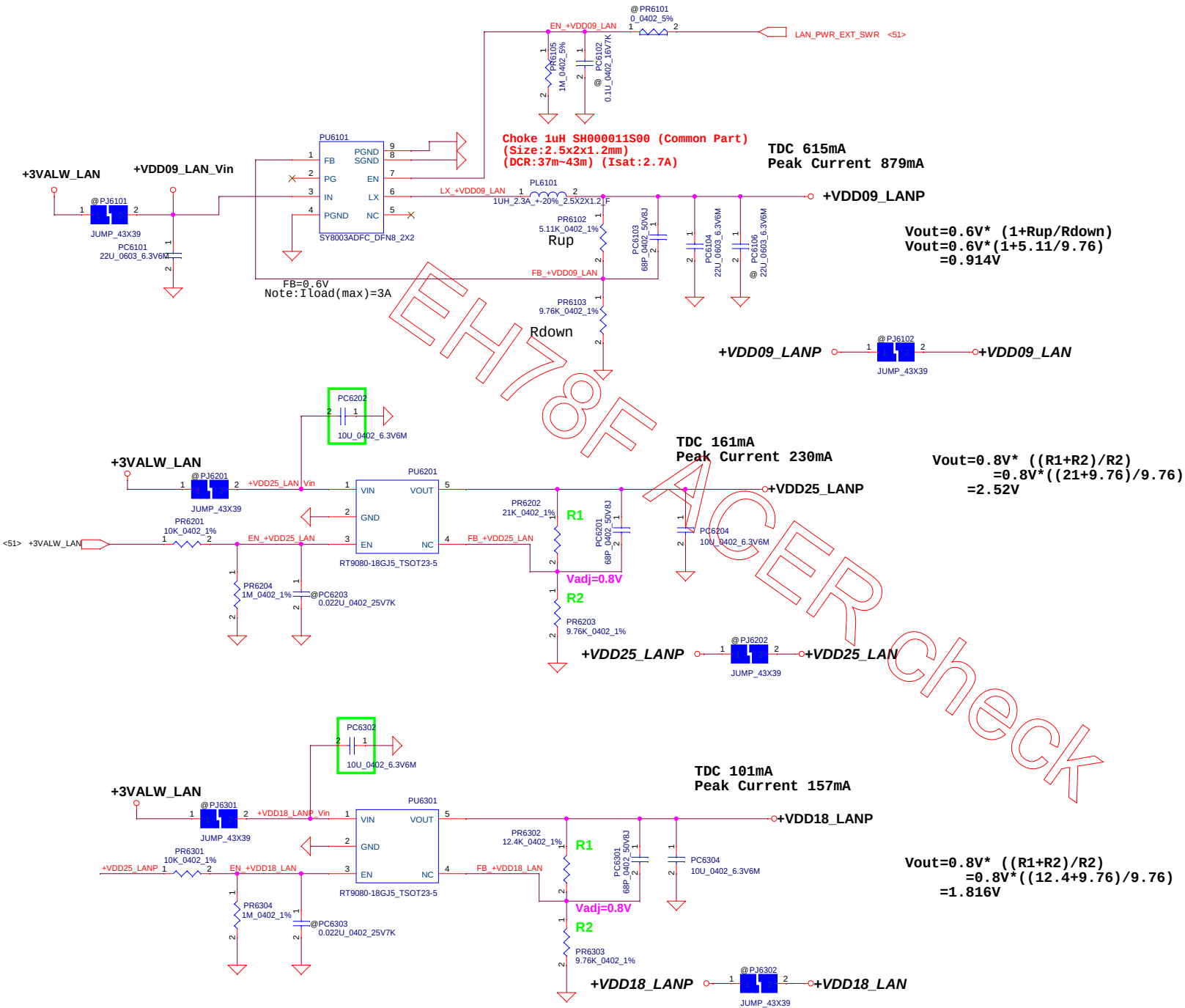
Title: **PWR_+1.0VS_VGA**

Size	Document Number	Rev
		0.1

Date: Wednesday, January 16, 2019 | Sheet 99 of 102



Title	PWR_+5V_VRout	
Size B	Document Number <Doc>	Rev 0.1
Date: Wednesday, January 16, 2019	Sheet 100 of 102	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LAN_PWR_EXT_SWR <51>
PR6105
1M_0402_5%
PC6102
@ 0.1U_0402_16V7K
Choke 1uH SH000011S00 (Common Part)
(Size:2.5x2x1.2mm)
(DCR:37m~43m) (Isat:2.7A)
TDC 615mA
Peak Current 879mA
PU6101
FB
PGND
SGND
PG
EN
IN
LX
PGND
NC
SY8003ADFC_DFN8_2X2
+3VALW_LAN
+VDD09_LAN_Vin
@PJ6101
JUMP_43X39
PC6101
22U_0603_6.3V6M
LX_+VDD09_LAN
PL6101
1UH_2.3A_+-20%_2.5X2X1.2_F
+VDD09_LANP
PR6102
5.11K_0402_1%
Rup
PC6103
68P_0402_50V8J
PC6104
22U_0603_6.3V6M
PC6106
@ 22U_0603_6.3V6M
Vout=0.6V* (1+Rup/Rdown)
Vout=0.6V*(1+5.11/9.76)
=0.914V
FB_+VDD09_LAN
FB=0.6V
Note:Iload(max)=3A
PR6103
9.76K_0402_1%
Rdown
+VDD09_LANP
@PJ6102
JUMP_43X39
+VDD09_LAN
PC6202
10U_0402_6.3V6M
TDC 161mA
Peak Current 230mA
+3VALW_LAN
@PJ6201
JUMP_43X39
+VDD25_LAN_Vin
PU6201
VIN
VOUT
GND
EN
NC
RT9080-18GJ5_TSOT23-5
+VDD25_LANP
Vout=0.8V* ((R1+R2)/R2)
=0.8V*((21+9.76)/9.76)
=2.52V
PR6202
21K_0402_1%
R1
PC6201
68P_0402_50V8J
PC6204
10U_0402_6.3V6M
<51> +3VALW_LAN
PR6201
10K_0402_1%
EN_+VDD25_LAN
FB_+VDD25_LAN
PR6204
1M_0402_1%
@PC6203
0.022U_0402_25V7K
Vadj=0.8V
R2
PR6203
9.76K_0402_1%
+VDD25_LANP
@PJ6202
JUMP_43X39
+VDD25_LAN
PC6302
10U_0402_6.3V6M
TDC 101mA
Peak Current 157mA
+3VALW_LAN
@PJ6301
JUMP_43X39
+VDD18_LANP_Vin
PU6301
VIN
VOUT
GND
EN
NC
RT9080-18GJ5_TSOT23-5
+VDD18_LANP
Vout=0.8V* ((R1+R2)/R2)
=0.8V*((12.4+9.76)/9.76)
=1.816V
PR6302
12.4K_0402_1%
R1
PC6301
68P_0402_50V8J
PC6304
10U_0402_6.3V6M
+VDD25_LANP
PR6301
10K_0402_1%
EN_+VDD18_LAN
FB_+VDD18_LAN
PR6304
1M_0402_1%
@PC6303
0.022U_0402_25V7K
Vadj=0.8V
R2
PR6303
9.76K_0402_1%
+VDD18_LANP
@PJ6302
JUMP_43X39
+VDD18_LAN
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Item	Page	Title	Date	Request Owner	Solution Description	Rev.
1	P82	design change	10/8		pu201 G718_SA00003K300 change to unpop	0B
2	P86	design change	10/8		PD1501 change from SS1P4_SCS00006P00 to SS3P4_SCS00005H00 Add PR1512 0ohm_SD028000080	
3	P83		10/8		PQ307 & PQ308 change footprint	
4	P85		10/8		Add PD501_SCS00009P00	
5	P101		10/8		PR6102 change from 1.33k_SD00000RF00 to 5.11k_SD034511180	
6	P93		10/8		PRV139 & PRV140 change from unpop to SMT 10k_SD034100280	
7	P98		10/8		PR1017 change from R_short to 0_SD028000080 PQ1003 change from 2n7002_SB00000ST00 to DMN53_2N_SB00001DD00	
8	P101		10/12		PU6301 & PU6201 change from RT9041E_SA00006K300 to RT9080N_SA0000C0600, because x1 code.	
9	P83		10/12		PQ302 change from L2N7002_SB00000ST00 to 2N7002_SB000009Q80 for 2nd source	
10	P98		10/15		Add PC1035 PC1036 220u_D7_SGA0000AM00	
11	P100		10/15		PR1608 change from 15k_SD034150280 to 21.5k_SD034215280	
12	P89	design change	10/17		PC825 change from 100p_0402_SE071101J80 to 470p_0402_SE071471J80 PR841,PR845,PR846,PR849 change from 115k_0603_SD014115380 to 130k_0603_SD014130380 PR811 change from 1.78k_0402_SD00000WY80 to 1.65k_0402_SD034165180 PR813 change from 31.6k_0402_SD034316280 to 29.4k_0402_SD034294280	
13	P92		10/17		PC9025,PC9026,PC9050 220u_D7_SGA0000AM00 change to unpop	
14	P98		10/19		1.35Vsdgpu add PC1037 560u_D2_SGA00006J00 PC1030, PC1031 change from 560u_D2_SGA00006J00 to 220u_D7_SGA0000AM00 add PC1038, PC1039, PC1040 220u_D7_SGA0000AM00	
15	P97		10/19		add 1u_0201_PC272~PC291, total 20pcs.	
16	P83		10/22		PR328 change from 200k_SD034200380 to 21.5k_SD034215280	
17	P97		10/22		remove @ 22u_0603_SE00000M000, PCV266,PCV267,PCV268,PCV269, PCV270	
18	P98		10/22		PR1004 change from 383k_0402_SD034383380 to 442k_0402_SD034442300	
19	P98		10/25		PR1010 change form 4.64k_SD00000K980 to 4.02k_SD034402180 PC1008 & PC1037 change form 560u_D2_SGA00006J00 to 330u_D1_SGA00009S00	
20	P84	HW request	11/5		PR402 change from 6.65k_0402_SD034665180 to 7.15k_0402_SD034715180	
21	P99	HW request	11/27		PC1106 change to unpop, for sequence	
22	P93		11/30		add PRV155 0ohm_0402 PCV9 PUV8 change to un-pop	0C
23	P83	EMI request	11/30		add PC326 0.1u_0402, PC303, PC305 change to SMT PR102, PC101, PR103, PC104 change to SMT	
24	P83		12/03		PQ308,PQ502 change from aon7506_SB000010A00 to EMB12N03_SB00001HV00	
25		design change	12/03		update PQ306,PQ307,PQ308,PQ401,PQ402,PQ403,PQ404,PQ501,PQ502 footprint to Q_N_DFN33-8-5	
26		design change	12/03		PR312,PR316,PR344,PR329,PR1512,PR801,PR810,PR821,PR822,PR925,PR929,PR927,PR931, PRV20,PRV34,PRV50,PRV155,PRV70,PRV54,PRV56,PRV58,PRV60,PRV62,PRV65,PRV145, PRV146,PRV147,PRV148,PRV149,PRV150,PRV1,PRV12,PRV13,PRV18,PRV79,PRV84,PRV81, PRV89,PRV94,PRV91,PRV99,PRV104,PRV101,PRV109,PRV114,PRV111,PRV119,PRV124,PRV121, PRV129,PRV134,PRV131,PR1016,PR1017,Pr1606,PR1602,PR1603,PR6101 change to 0402_R-short	
27		design change	12/03		PR409,PR410,PR502,PR603,Pr7201,PR1109,Pr1601,PR1604 change to 0603_R-short	
28	P98	design change	12/03		PC1022,PC1045 change from 4700p_SE074472K80 to 2200p_SE074222K80	
29	P86	design change	12/04		PD1501 change from SS3P4_SCS00005H00 to SS32FL_SCS0000FD00	

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