Compal Confidential

ZIVY2/ZIVY3 M/B Schematics Document

Intel Shark Bay + N15P-GX
(Crescent Bay + N15P-GX)

LA-B111P

2014-02-25

REV:1.0

Security Classification	Compal Secret Data		
Issued Date	2014/02/25	Deciphered Date	2015/02/25

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Title: *Cover Sheet*

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Date: Tuesday, February 25, 2014 | Sheet 1 of 59

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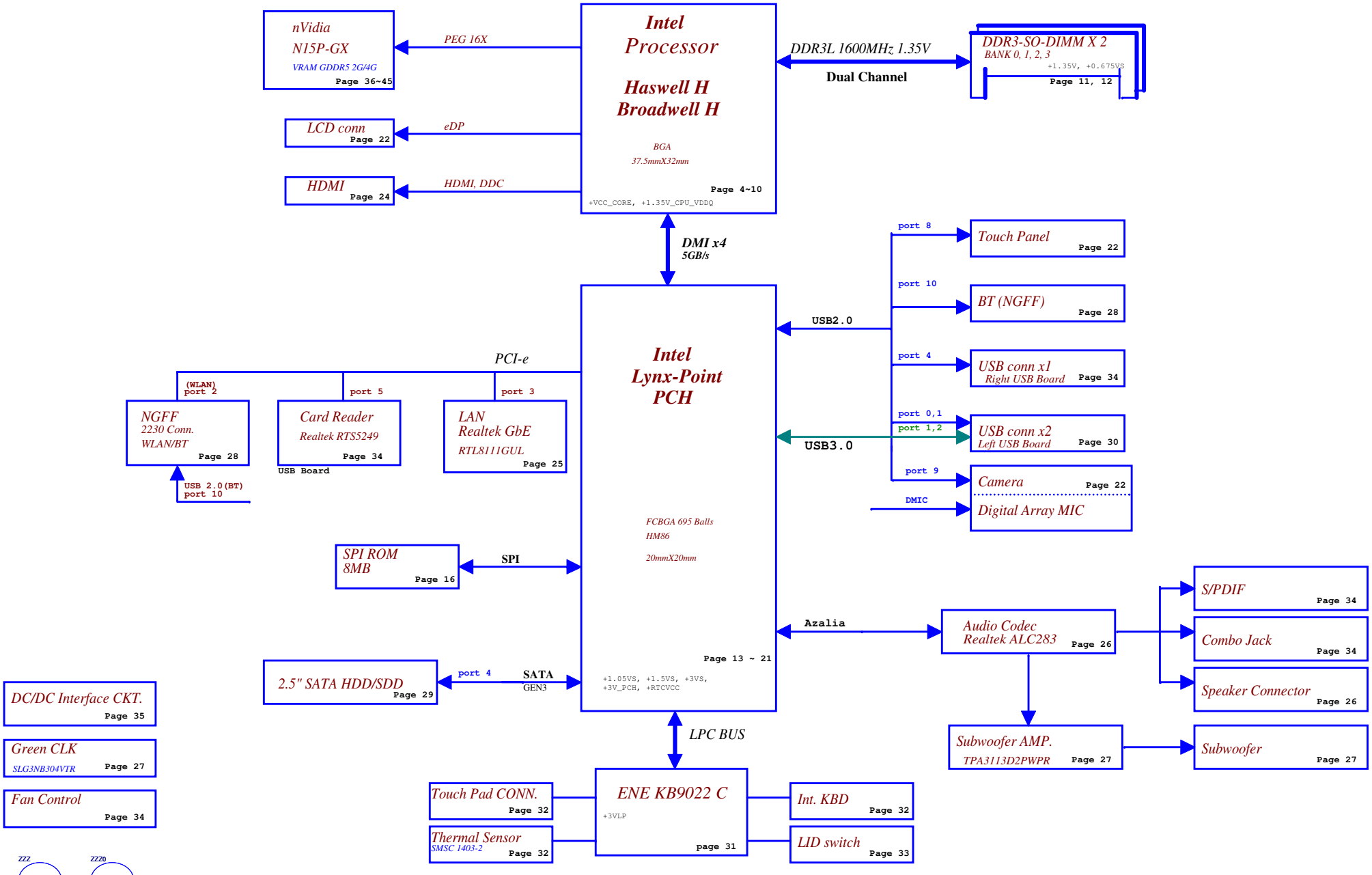
Shark Bay/Crescent Bay



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Title: **Block Diagram**

Size	Document Number	Rev
Custom	LA-B111P	1.0

Date: Tuesday, February 25, 2014 | Sheet 2 of 59

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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane / State	B+	+5VALW +3VALW +12VS_PANEL	+3V_PCH	+1.35V	+5VS +3VS +1.5VS +1.05VS +VCC_CORE +0.675VS +12VS
S0	O	O	O	O	O
S3	O	O	O	O	X
DeepS3	O	O	X	O	X
S5 S4/AC	O	O	X	X	X
S5 S4/ Battery only	O	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X	X

USB Port Table

	USB 2.0	Port	USB 3.0	Port	5 External USB Port
EHCI1	UHCI0	0	XHCI	1	Left USB3.0
		1	XHCI	2	Left USB3.0
	UHCI1	2			
		3			
	UHCI2	4			Right USB2.0
		5			
	UHCI3	6			
		7			
EHCI2	UHCI4	8			Touch screen
		9			Camera
	UHCI5	10			WLAN
		11			
	UHCI6	12			
		13			

BOM Structure Table

BTO Item	BOM Structure
45 LEVEL	45@
Connector	CONN@
KB ZIVY2 (15")	KB15@
KB ZIVY3 (17")	KB17@
ZIVY2 (15")	15@
ZIVY3 (17")	17@
Subwoofer	WF@
DIS SKU	DIS@
Nvidia GC6 state	SW@
Haswell	HW@
Broadwell	BW@
Deep S3	DS3@
NO Deep S3	NODS3@
Green clk support	GCLK@
No Green clk support	NOGCLK@
Unpop	CMOS@/NCMOS@
Unpop	@
EMI Pop	EMI@
EMI unpop	@EMI@
ESD Pop	ESD@
ESD unpop	@ESD@
SATA re-driver	TI@/Parade@

Board ID Table for AD channel

Vcc	3.3V
Ra / Rc	100K +/- 1%

Board ID	Rb / Rd	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	12K +/- 1%	0.347 V	0.354 V	0.360 V
2	15K +/- 1%	0.423 V	0.430 V	0.438 V
3	20K +/- 1%	0.541 V	0.550 V	0.559 V
4	27K +/- 1%	0.691 V	0.702 V	0.713 V
5	33K +/- 1%	0.807 V	0.819 V	0.831 V
6	43K +/- 1%	0.978 V	0.992 V	1.006 V
7				

EC SM Bus1 address

Device	Address
Smart Battery Charger	0b 0001 0010 (0x12H)

EC SM Bus2 address

Device	Address
Thermal Sensor EMC1403-2-AIZL-TR	1001_101xb
PCH SML1 Bus address	
nVidia N15P-GX	0x9E

Symbol Note :

: means Digital Ground

: means Analog Ground

Install below 43 level BOM structure for ver. 0.1

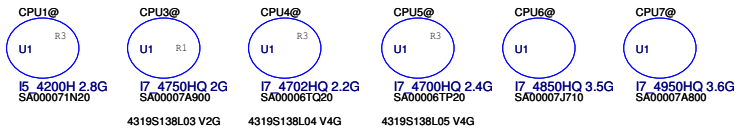
PCH SM Bus address

Device	Address
DDR DIMM0	1010 000x A0h
DDR DIMM1	1010 010x A4h
Click Pad	

PCH SML0 Bus address

Device	Address

CPU part



SMBUS Control Table

	SOURCE	BATT	KB9022	SODIMM	Touch Pad	Thermal sensor	VGA
SMB_EC_CK1 SMB_EC_DA1	KB9022 +3VLP_EC	V	X	X	X	X	X
SMBCLK SMBDATA	PCH +3V_PCH	X	X	V +3VS	V +3VS	X	X
SML0CLK SML0DATA	PCH +3V_PCH	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3V_PCH	X	V +3VS	X	X	V +3VS	V +3VS_DGPU

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Title: **Notes List**

Size: Custom | Document Number: LA-B111P | Rev: 1.0

Date: Tuesday, February 25, 2014 | Sheet 3 of 59

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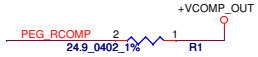
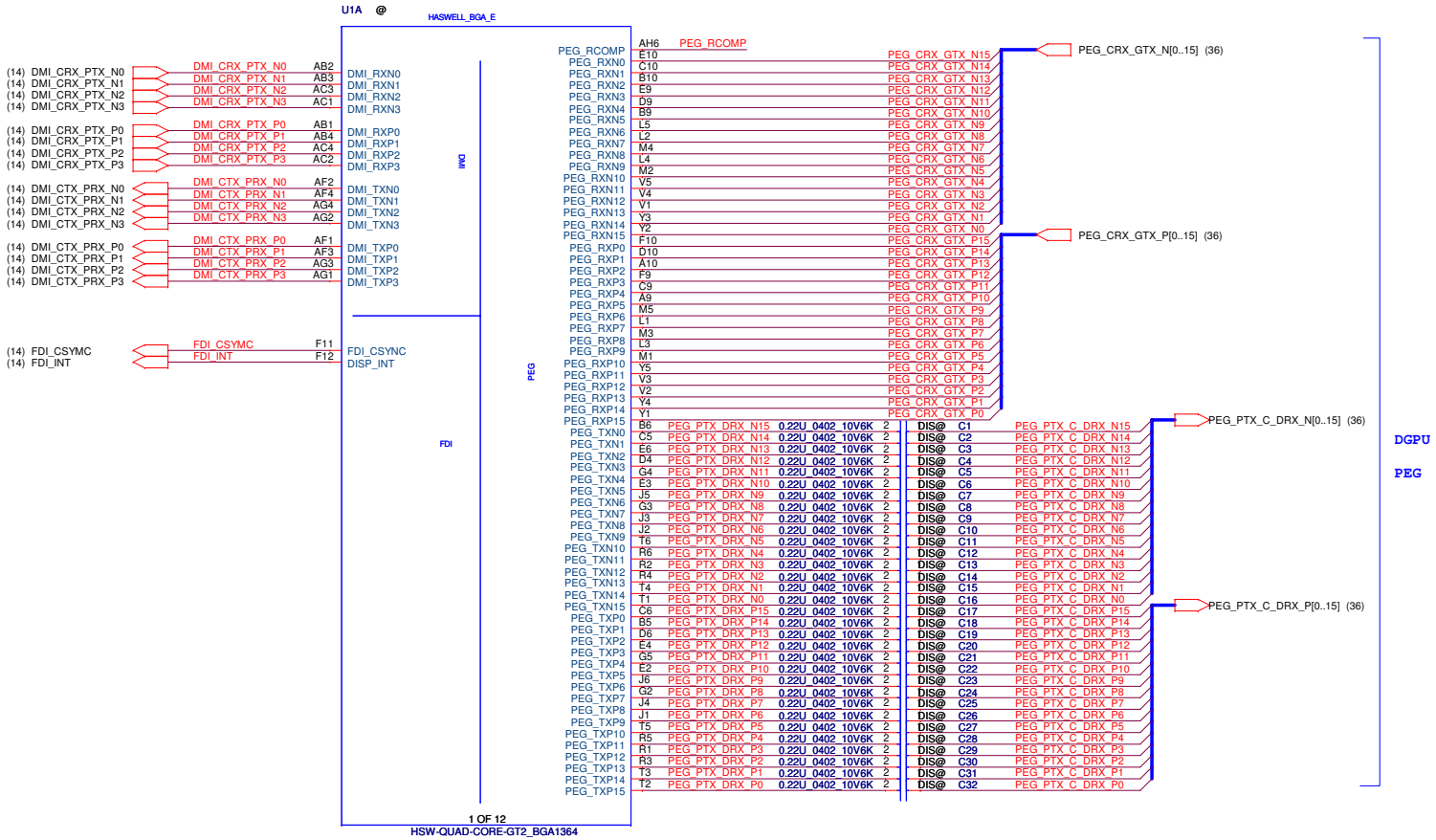


Note:
Trace width=12 mils ,Spacing=15mils
Max length= 400 mils.



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Title: ***PROCESSOR(1/7) DMI,FDI,PEG***

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Date: Tuesday, February 25, 2014 | Sheet 4 of 59

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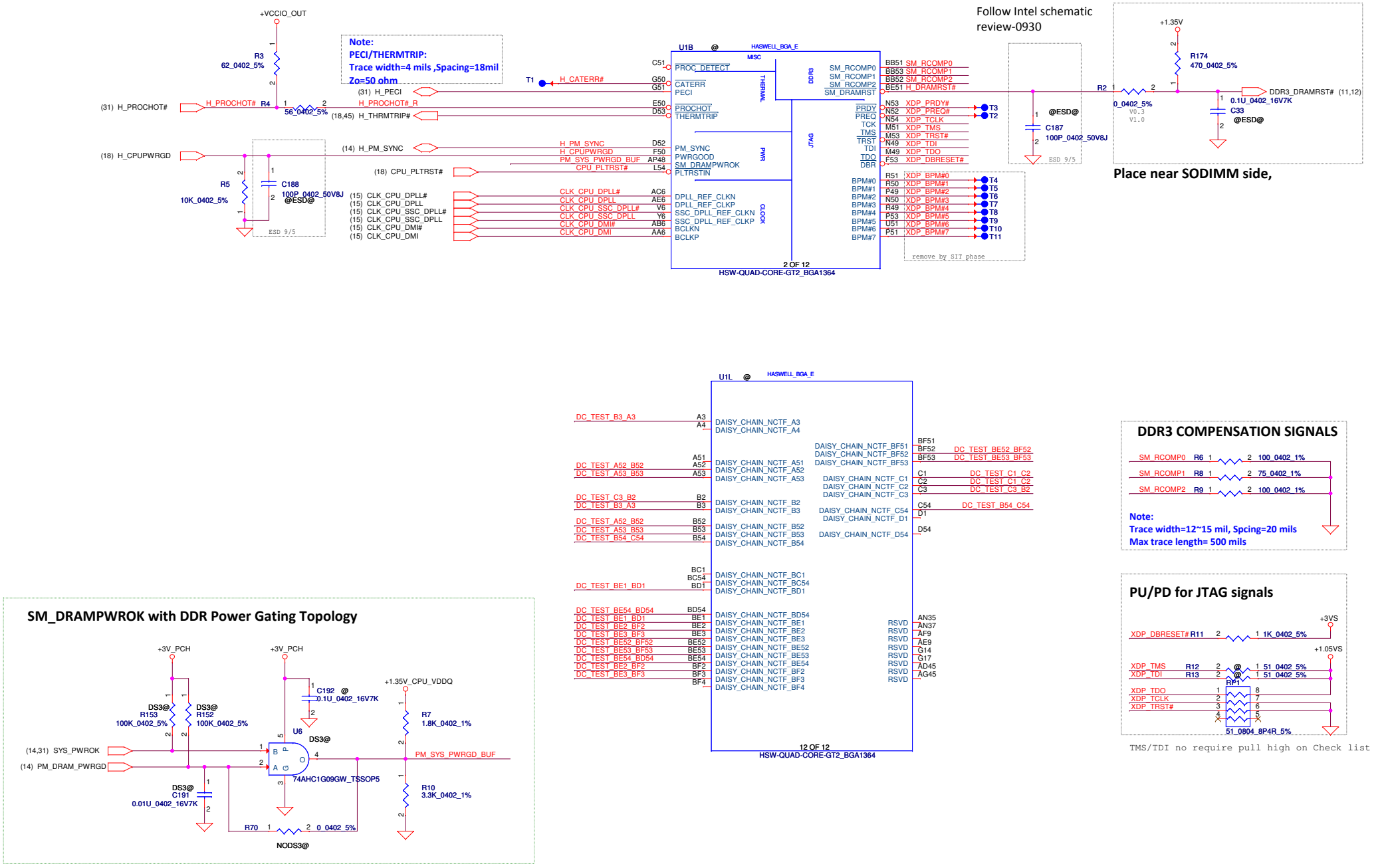

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Title: PROCESSOR(2/7) PM,XDP,CLK

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Date: Tuesday, February 25, 2014 | Sheet 5 of 59

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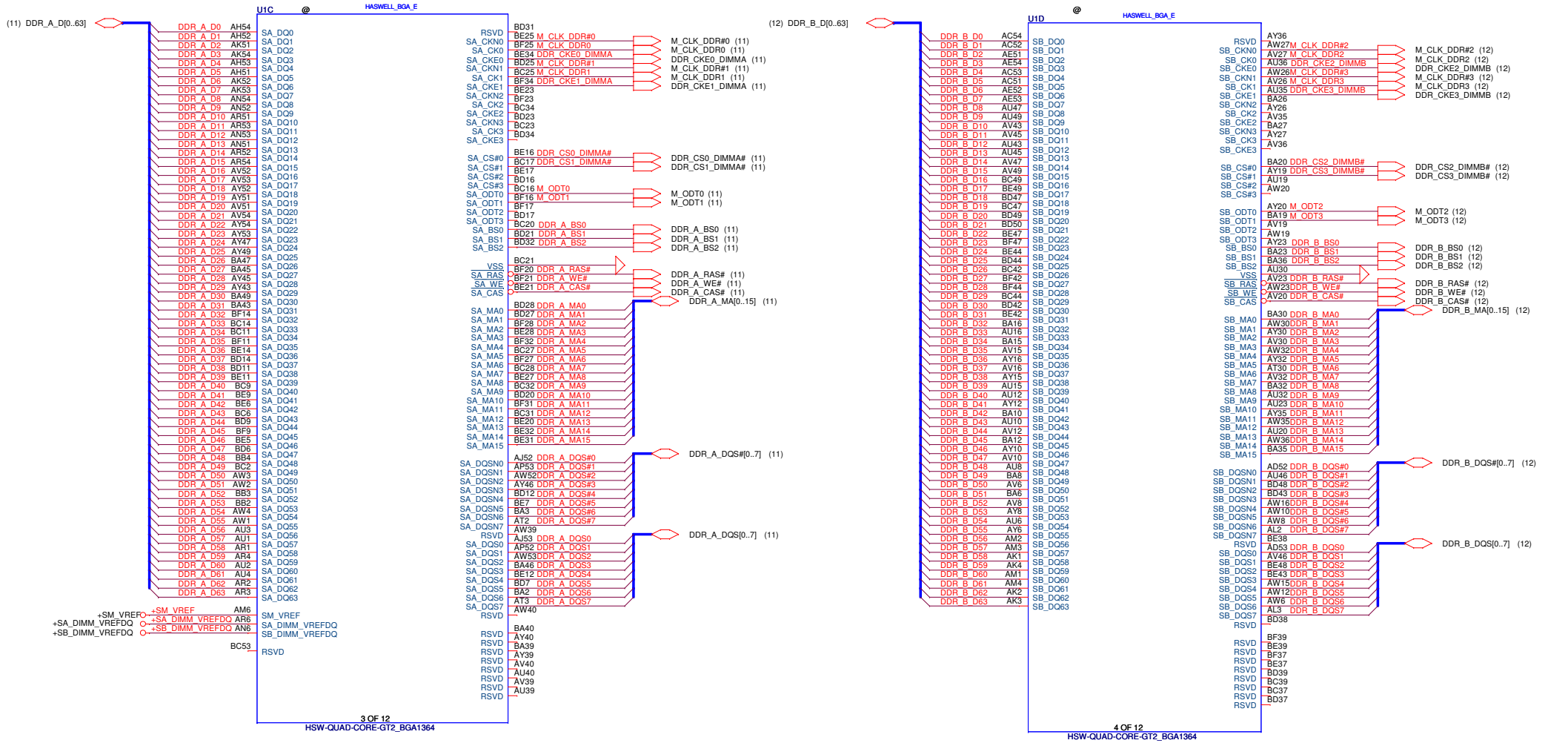

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Title: **PROCESSOR(3/7) DDRIII**

Size: Custom | Document Number: **LA-B111P** | Rev: 1.0

Date: Tuesday, February 25, 2014 | Sheet 6 of 59

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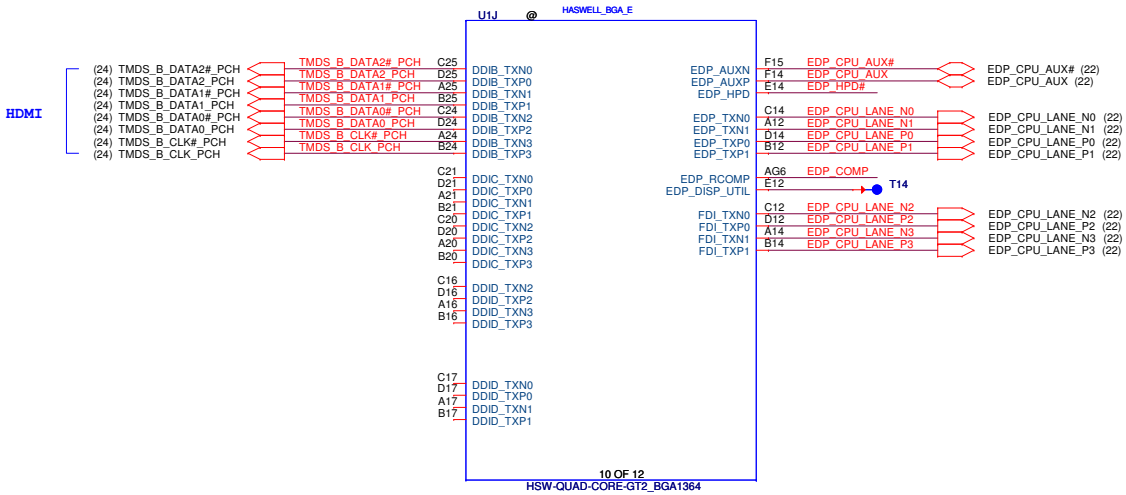
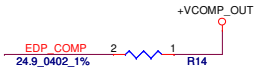
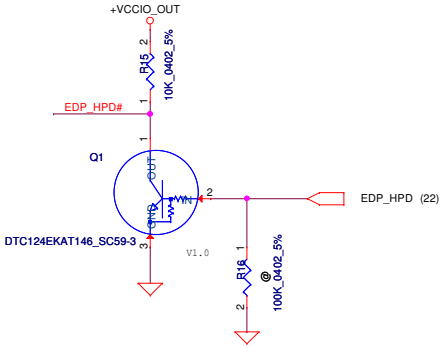


COMPENSATION PU FOR eDP



Note:
Trace width=20 mils ,Spacing=25mil,
Max length=100 mils.

HPD INVERSION FOR EDP



HPD is a active-high signal from device.
The HPD processor input is
active-low signal.

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Title: PROCESSOR(4/7) eDP,DP and HDMI

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Date: Tuesday, February 25, 2014 | Sheet 7 of 59

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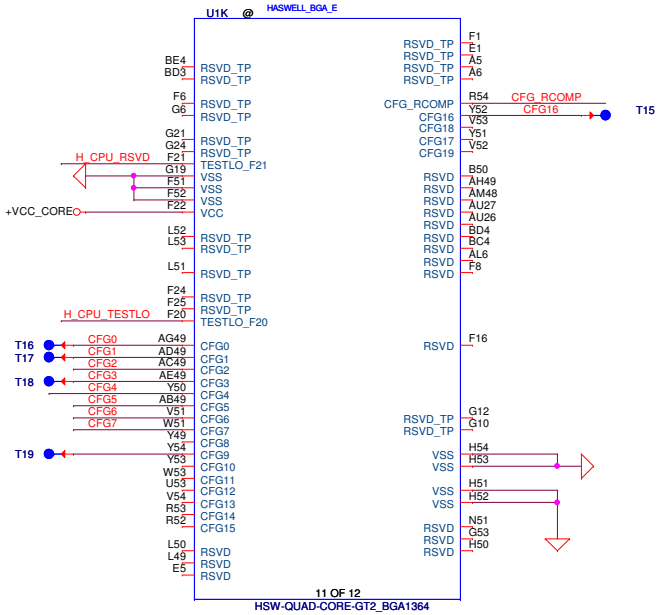
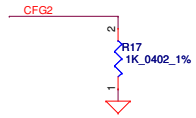
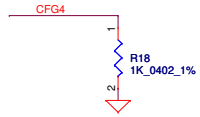
CFG Straps for Processor

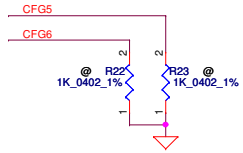




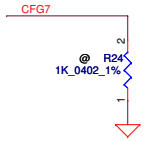
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



Embedded Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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Title: PROCESSOR(5/7) RSVD,CFG

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Date: Tuesday, February 25, 2014 | Sheet 8 of 59

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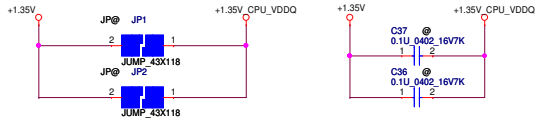
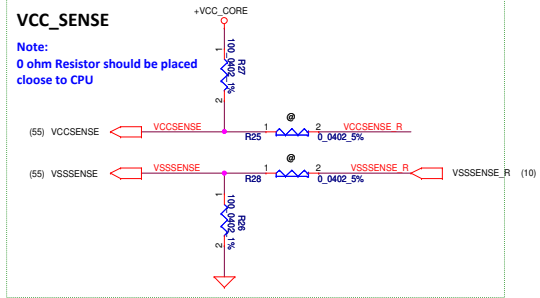
+1.35V_CPU_VDDQ Source

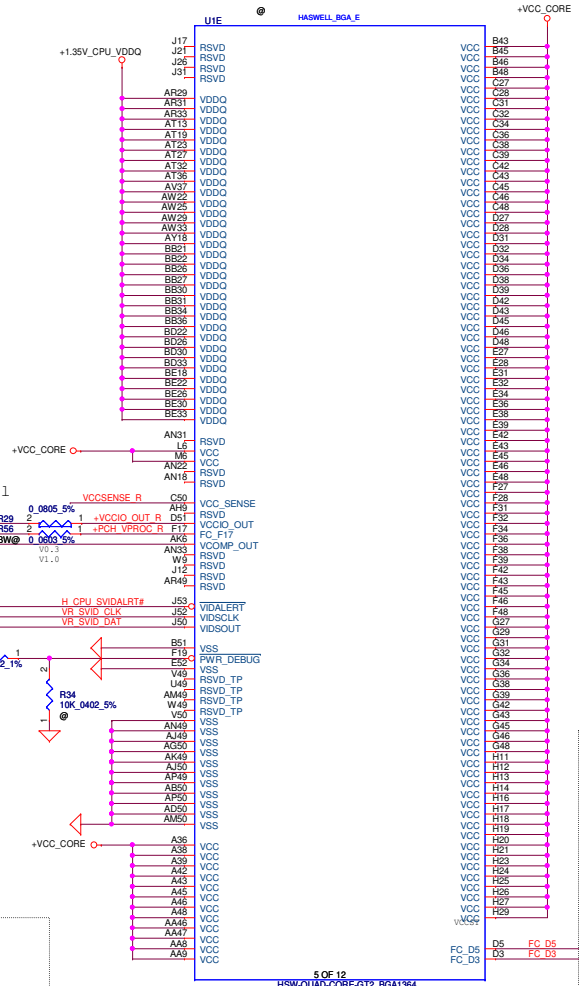
Note:
Intel Shark Bay
Removed the S3 power reduction circuit.

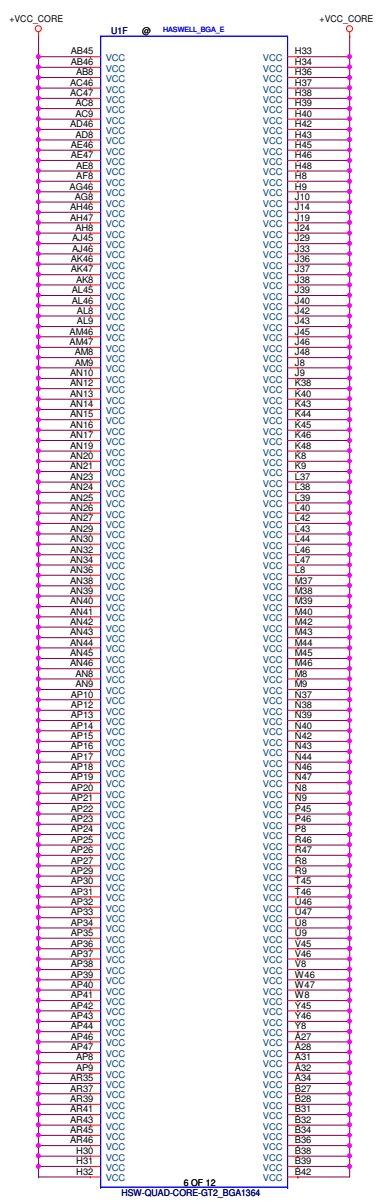


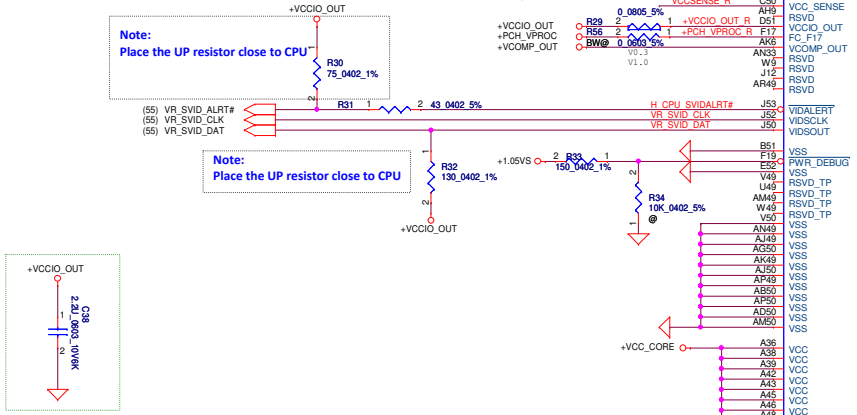
VCC_SENSE

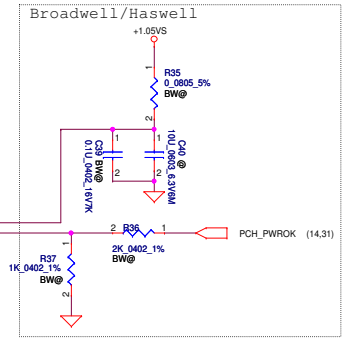
Note:
0 ohm Resistor should be placed cloose to CPU



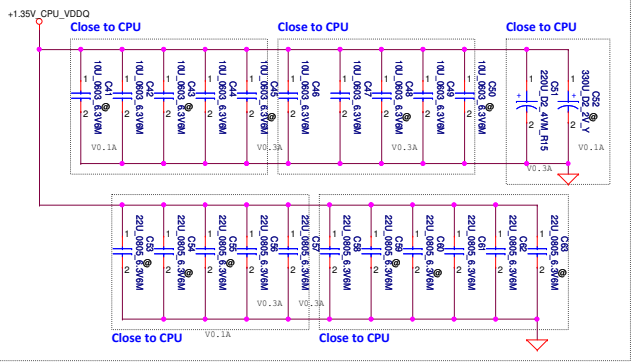








VDDQ DECOUPLING (Follow INTEL DG)



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Title: **PROCESSOR(6/7) PWR**

Size: C | Document Number: **LA-B111P** | Rev: 1.0

Date: Tuesday, February 25, 2014 | Sheet 9 of 59

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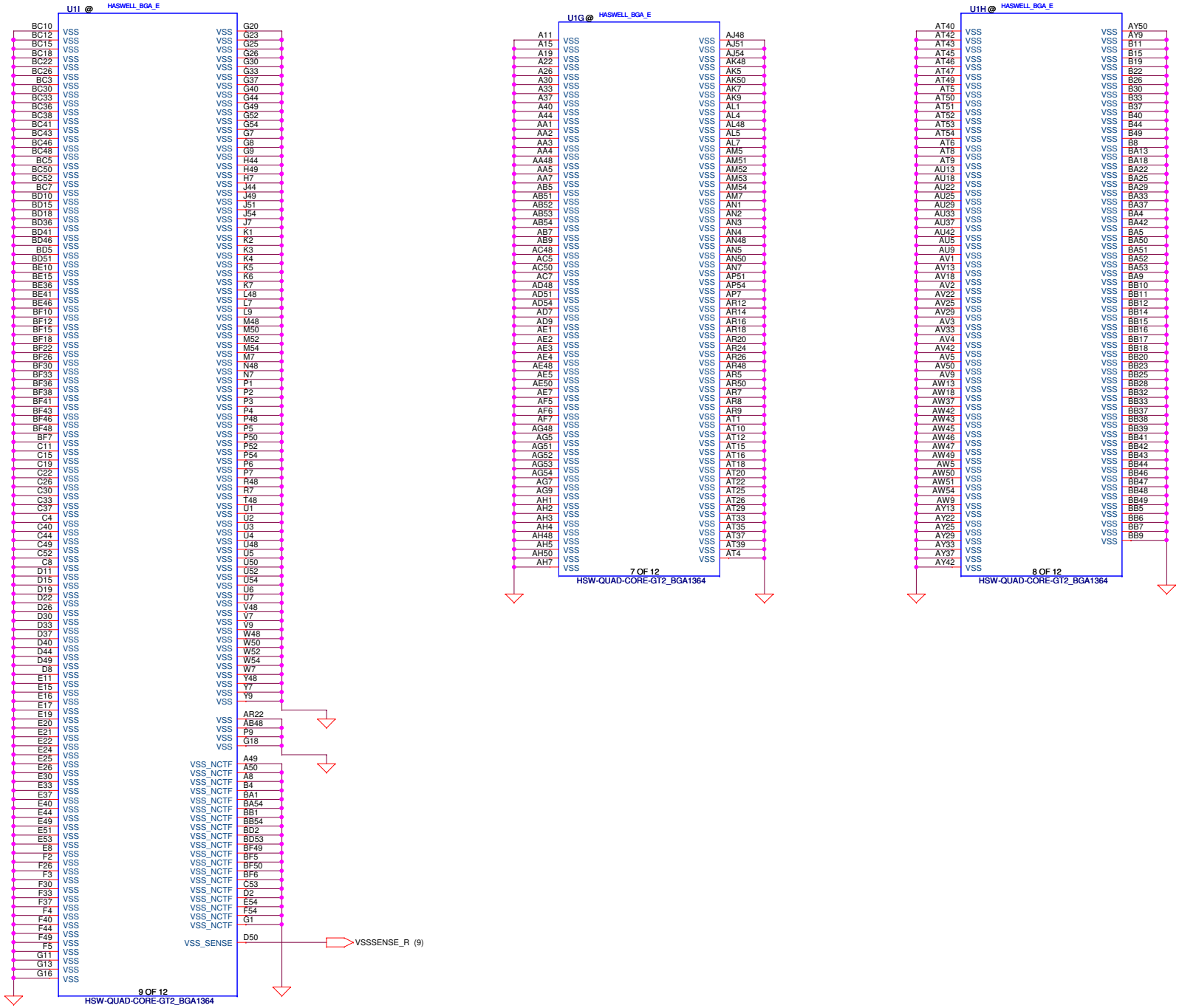

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Title: **PROCESSOR(7/7) VSS**

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Date: Tuesday, February 25, 2014 | Sheet 10 of 59

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DDR3 SO-DIMM A

JDIMM1 CONN@

LCN_DAN06-K4406-0103

SP07000LT00

(6) DDR_A_D[0..63]
(6) DDR_A_DQS[0..7]
(6) DDR_A_DQS#[0..7]
(6) DDR_A_MA[0..15]

Layout Note:
Place near JDIMM1

Place near JDIMM1 pin203 pin204

Layout Note:
Place near JDIMM1

CPU DRIVER VREF PATH IS DEFAULT

Note:
VREF trace width:20 mils at least
Spacing:20mils to other signal/planes

*M3+M1:Default Recommendation
M1:VREF_DQ driven by a voltage Divider Network during Processor power-off state.
M3:VREF_DQ driven by Processor.

Note:
VREF trace width:20 mils at least
Spacing:20mils to other signal/planes

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Title: DDRIII-SODIMM SLOT1

Size: Custom | Document Number: LA-B111P | Rev: 1.0

Date: Tuesday, February 25, 2014 | Sheet 11 of 59

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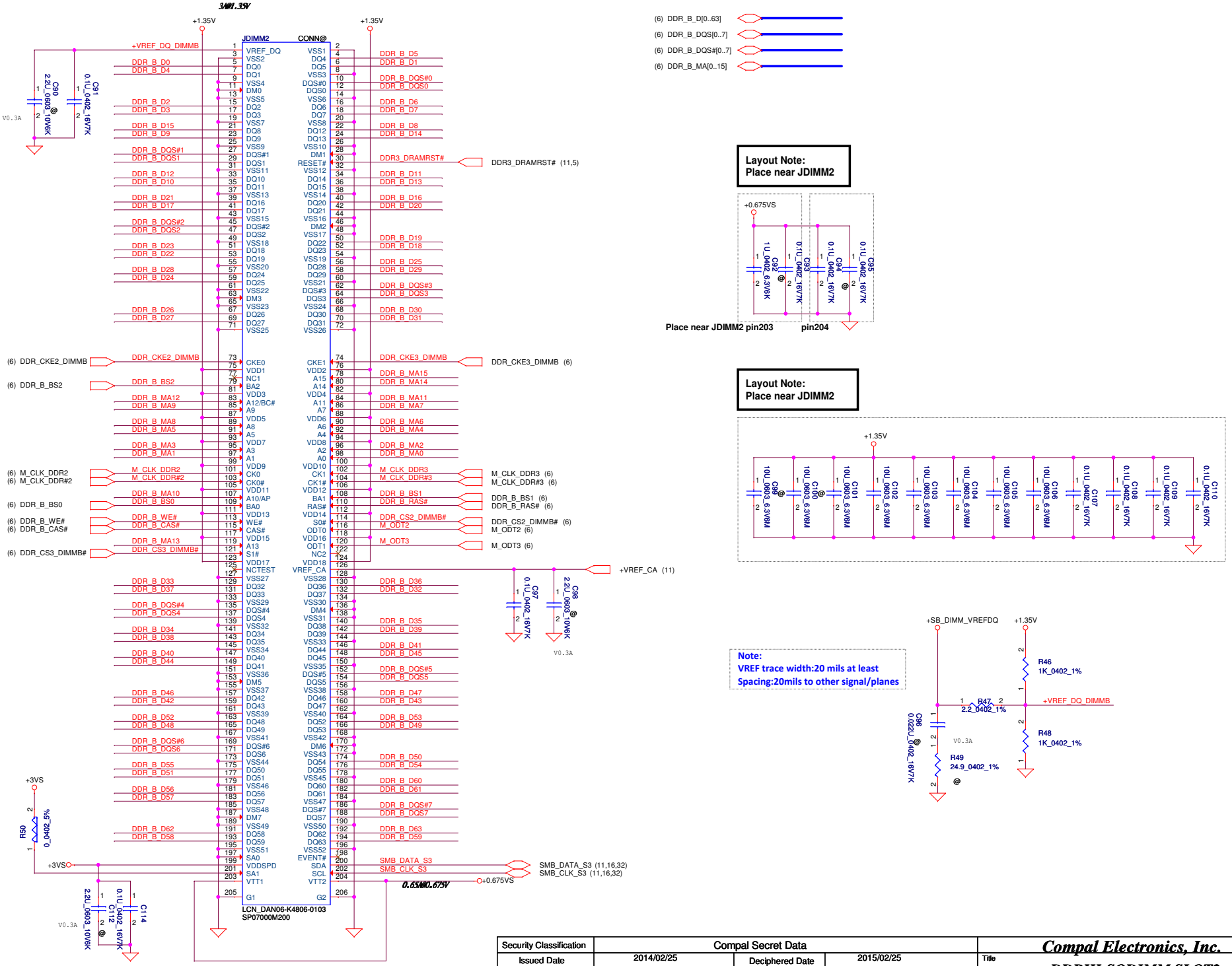

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Title: DDRIII-SODIMM SLOT2

Size: B/25 | Document Number: LA-B111P | Rev: 1.0

Date: Tuesday, February 25, 2014 | Sheet 12 of 59

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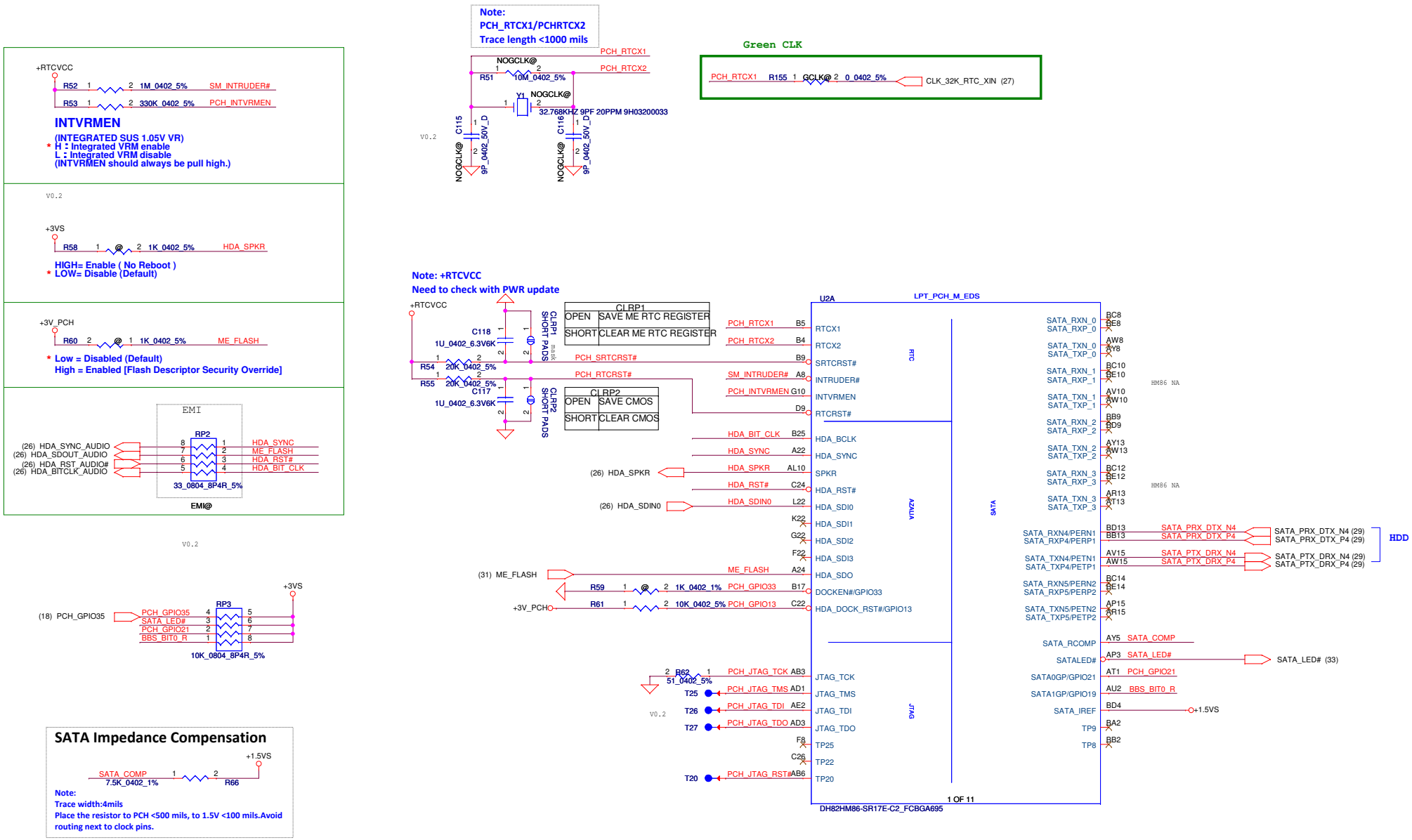

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Issued Date	2014/02/25	Deciphered Date	2015/02/25

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Compal Electronics, Inc.

Title: PCH (1/9) SATA,HDA,SPI, LPC, XDP

Size: B/26 Custom | Document Number: LA-B111P | Rev: 1.0

Date: Tuesday, February 25, 2014 | Sheet 13 of 59

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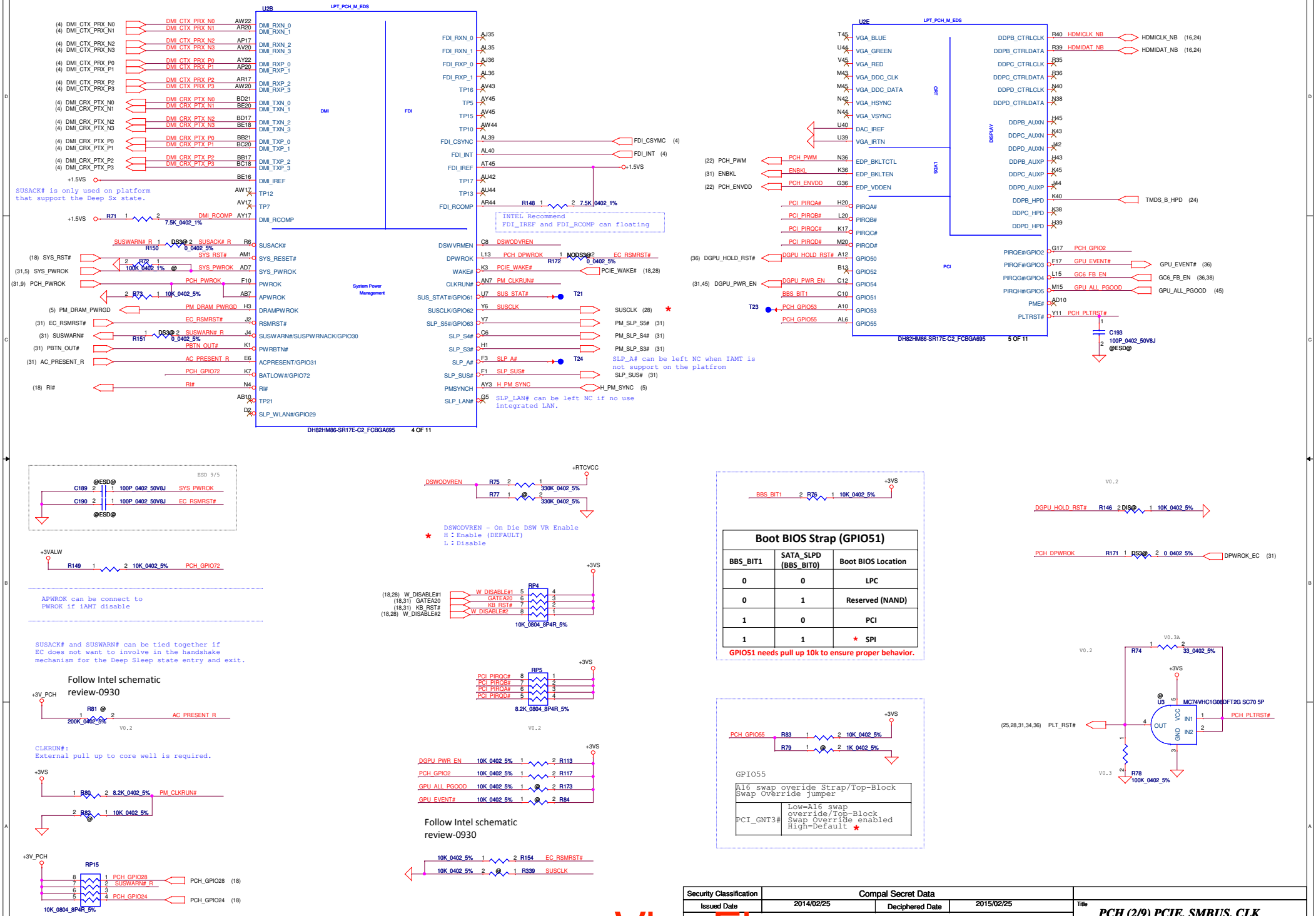

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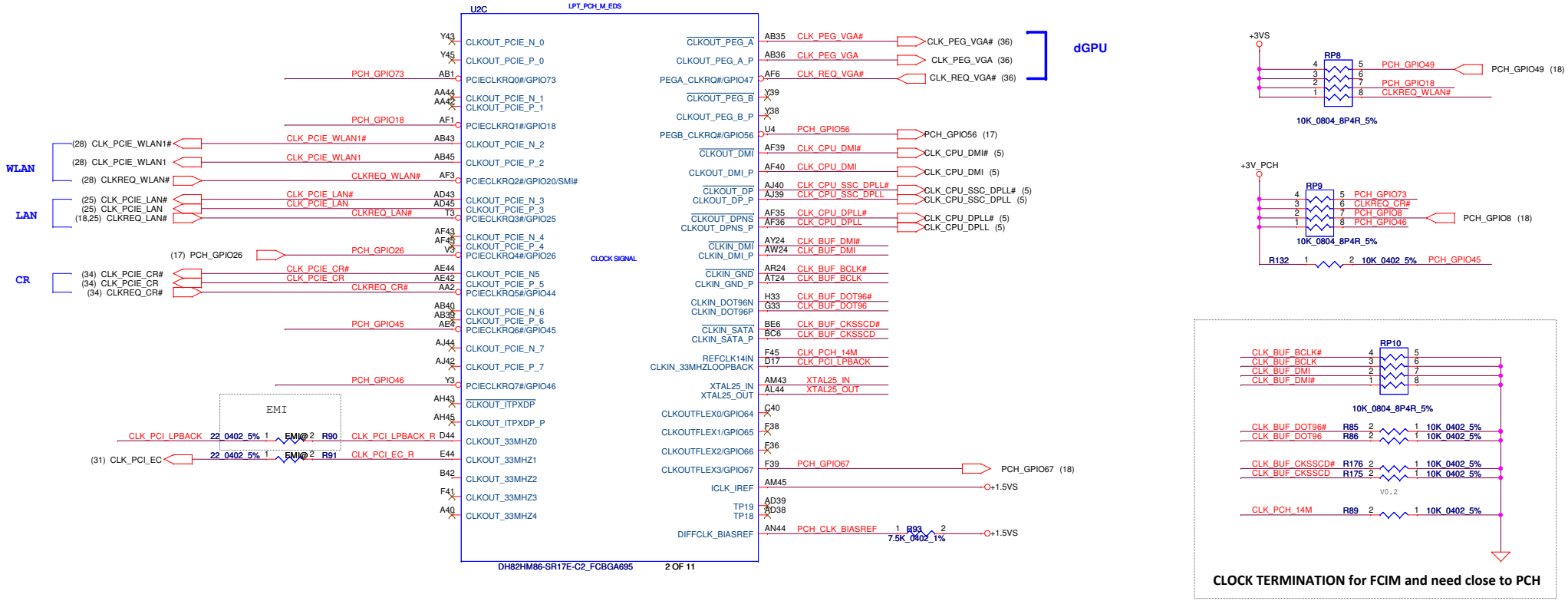

Security Classification	Compal Secret Data		
Issued Date	2014/02/25	Deciphered Date	2015/02/25

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Compal Electronics, Inc.

Title: PCH (3/9) DMI,FDI,PM,

Size: B | Document Number: LA-B111P | Rev: 1.0

Date: Tuesday, February 25, 2014 | Sheet 15 of 59

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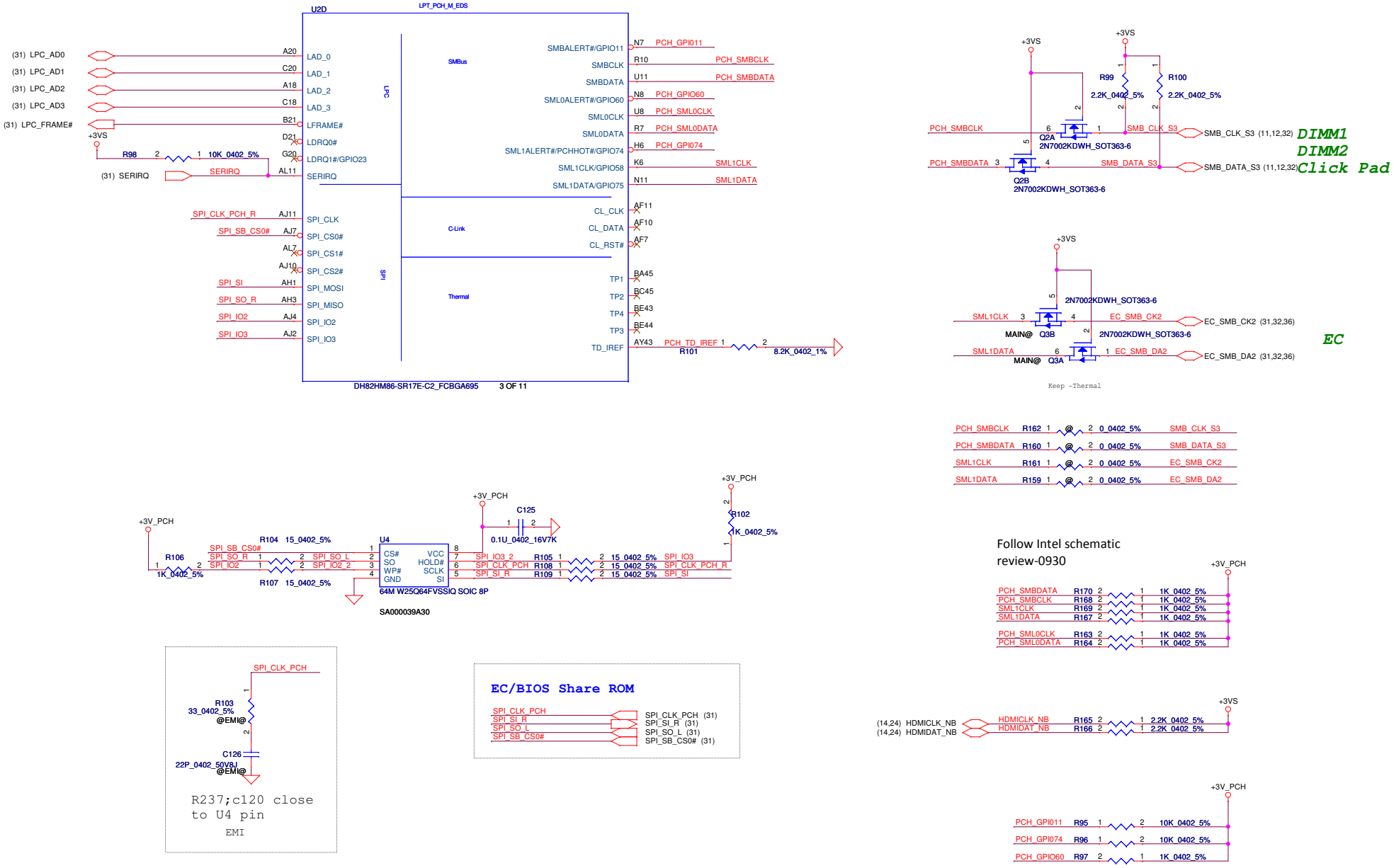

Security Classification	Compal Secret Data		
Issued Date	2014/02/25	Deciphered Date	2015/02/25

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Compal Electronics, Inc.

Title: PCH (4/9) LVDS,CRT,DP,HDMI

Document Number: LA-B111P

Rev: 1.0

Date: Tuesday, February 25, 2014 | Sheet 16 of 59

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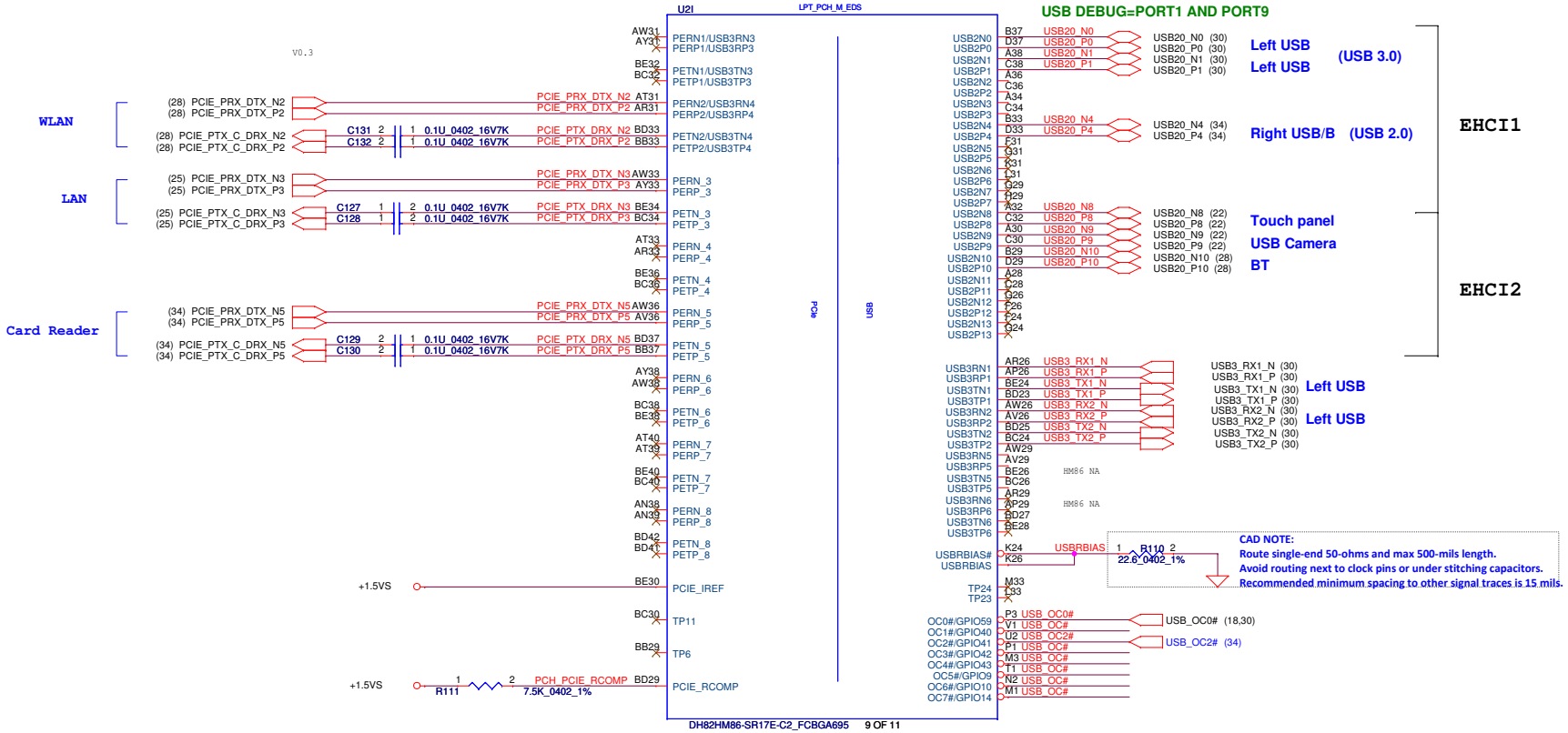

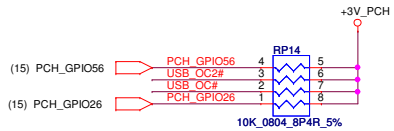

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Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB

Document Number: LA-B111P

Rev: 1.0

Date: Tuesday, February 25, 2014 | Sheet 17 of 59

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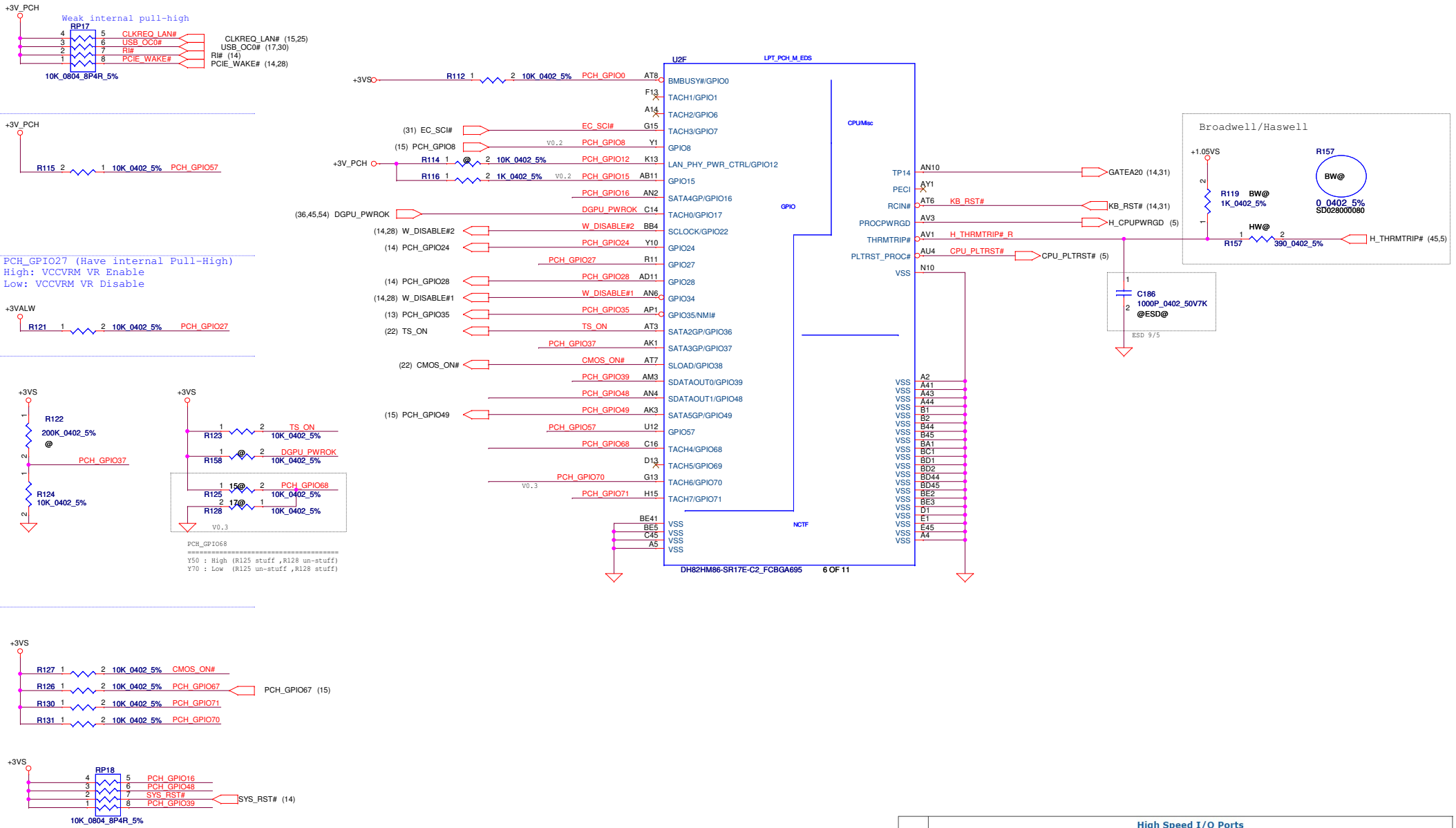

SKU	High Speed I/O Ports																	
	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8	Port 9	Port 10	Port 11	Port 12	Port 13	Port 14	Port 15	Port 16	Port 17	Port 18
HM86	USB 3.0 Port 1	USB 3.0 Port 2	NA	NA	USB 3.0 Port 3 / PCIe* Port 1	USB 3.0 Port 4 / PCIe* Port 2	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5	PCIe* Port 6	PCIe* Port 7	PCIe* Port 8	SATA 6Gb/s Port 4	SATA 6Gb/s Port 5	SATA 3Gb/s Port 0	NA	SATA 3Gb/s Port 2	NA

Security Classification	Compal Secret Data		
Issued Date	2014/02/25	Deciphered Date	2015/02/25

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Title: **PCH (6/9) GPIO, CPU, MISC**

Document Number: **LA-B111P** Rev 1.0

Date: Tuesday, February 25, 2014 Sheet 18 of 59

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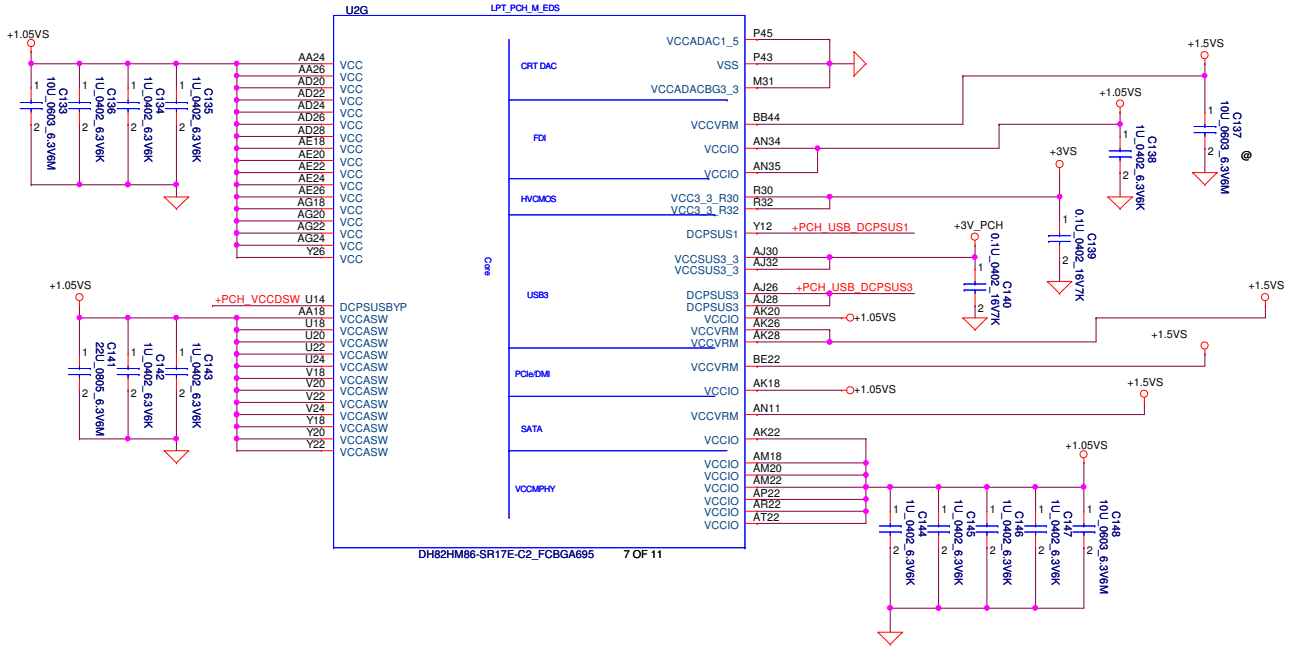
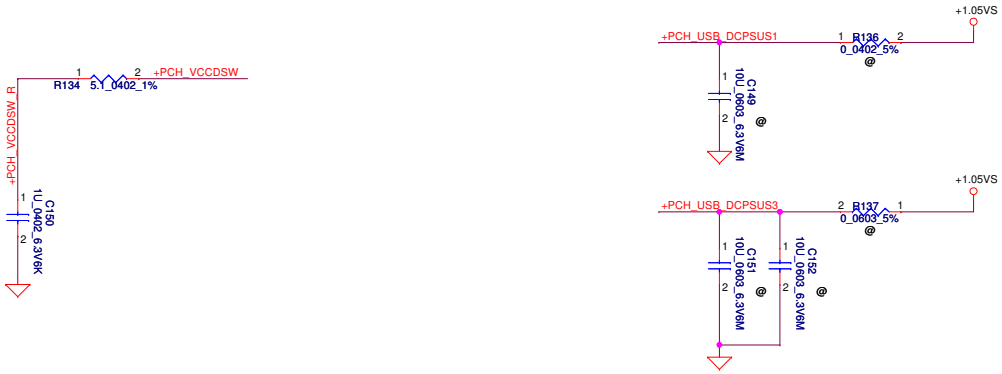


PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCADAC1_5	1.5V	0.070 A
VCCADAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A



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Compal Electronics, Inc.

Title: PCH (7/9) PWR

Document Number: LA-B111P

Rev: 1.0

Date: Tuesday, February 25, 2014 | Sheet 19 of 59

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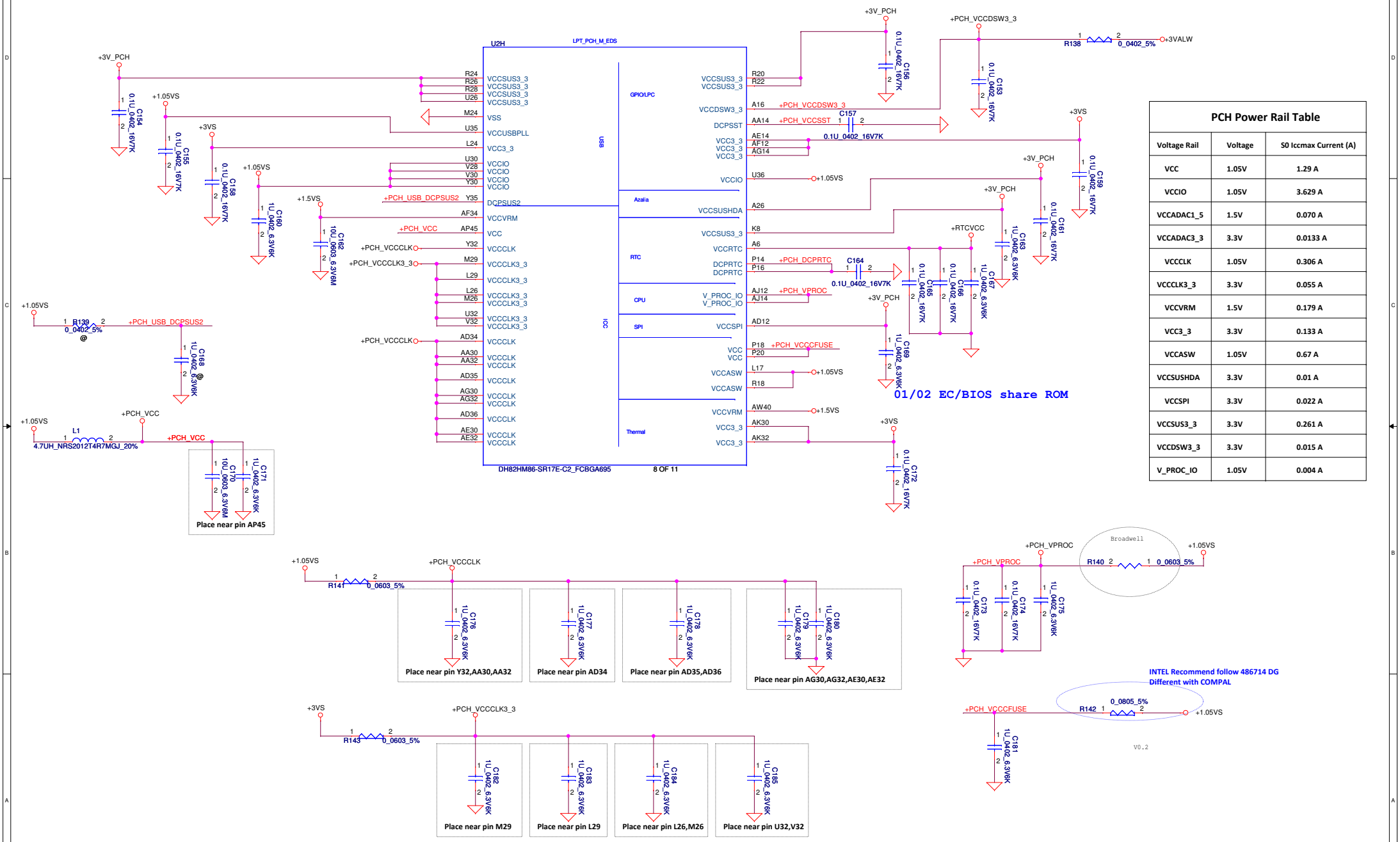

01/02 EC/BIOS share ROM

PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCADAC1_5	1.5V	0.070 A
VCCADAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A

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Title: **PCH (8/9) PWR**

Document Number: **LA-B111P**

Rev: 1.0

Date: Tuesday, February 25, 2014 | Sheet 20 of 59

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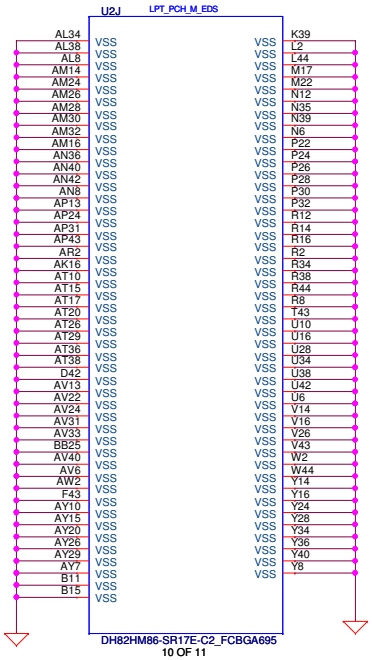

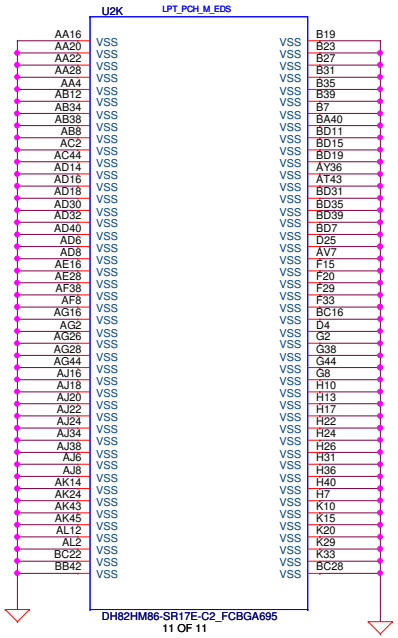

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Compal Electronics, Inc.

Title: PCH (9/9) VSS

Document Number: LA-B111P

Rev: 1.0

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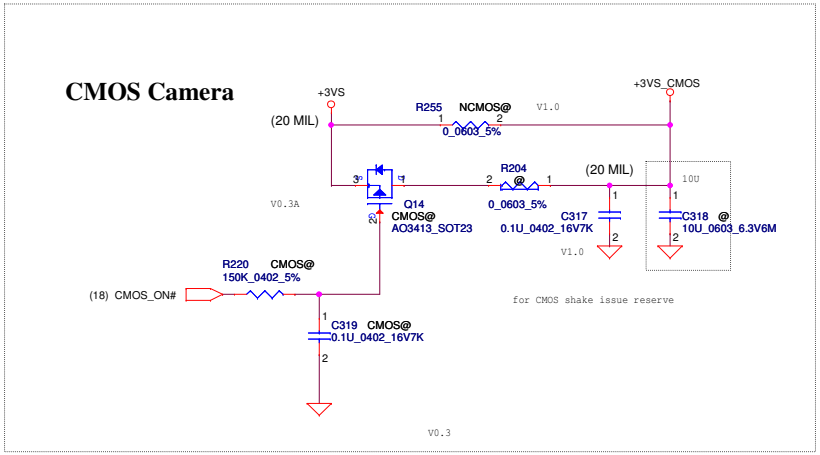
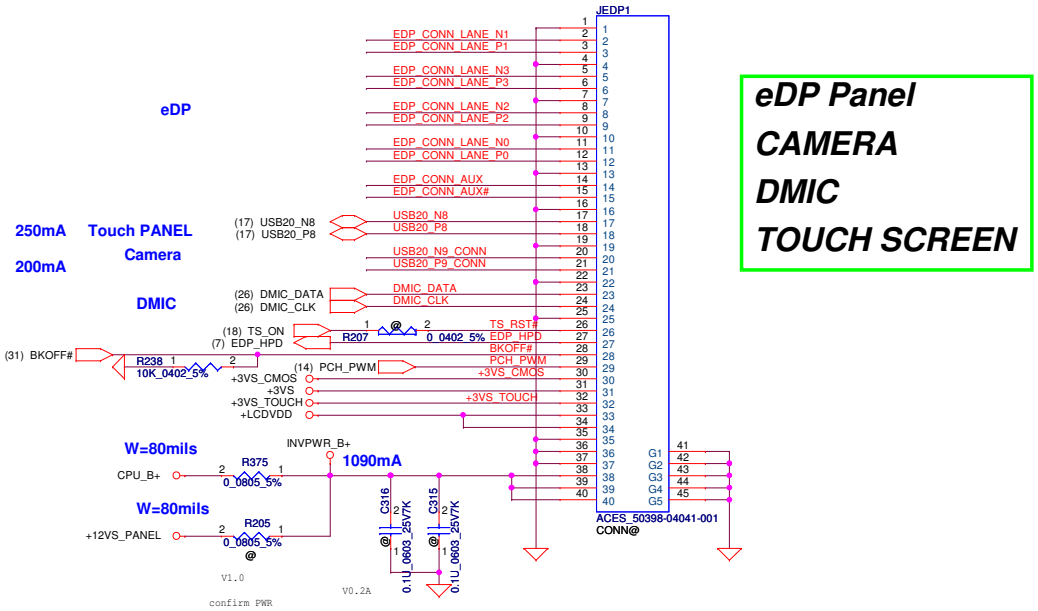
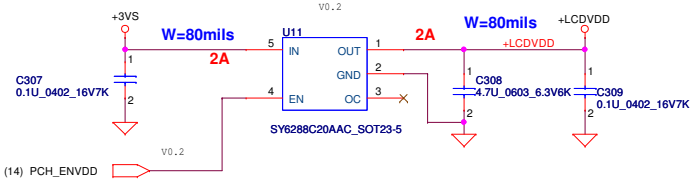
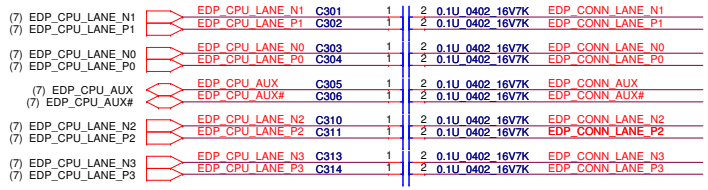




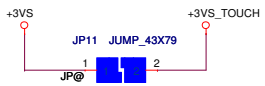
eDP Panel
CAMERA
DMIC
TOUCH SCREEN

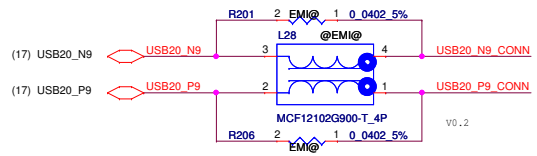
LCD POWER CIRCUIT





Touch Panel





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Compal Electronics, Inc.

Title: LCD Conn/Camera, Touch

Size: Custom | Document Number: LA-B111P | Rev: 1.0

Date: Tuesday, February 25, 2014 | Sheet 22 of 59

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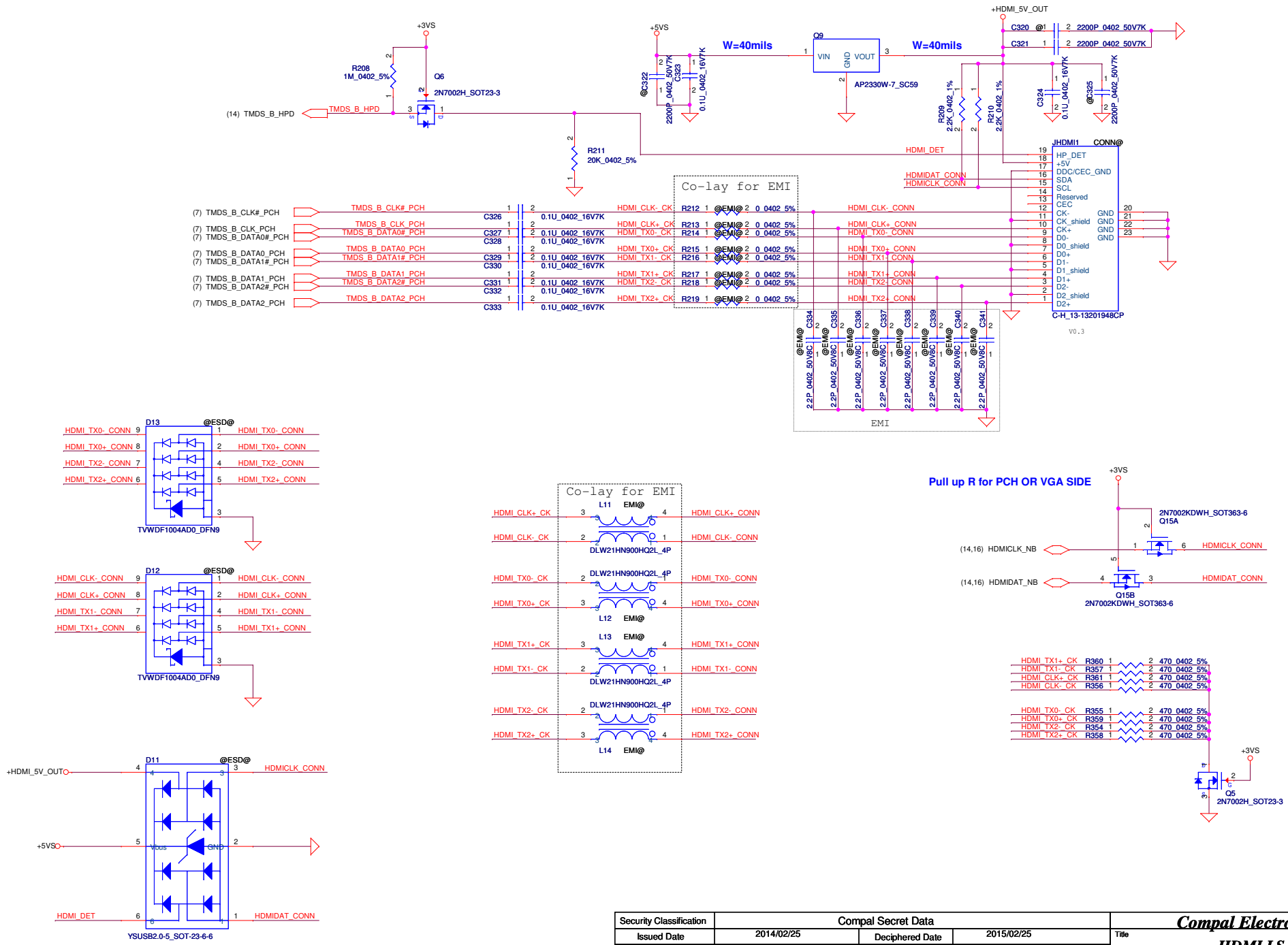
HDMI Connector



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Compal Electronics, Inc.

Title: **HDMI LS & Conn.**

Document Number: **LA-B111P** | Rev: 1.0

Date: Tuesday, February 25, 2014 | Sheet 24 of 59

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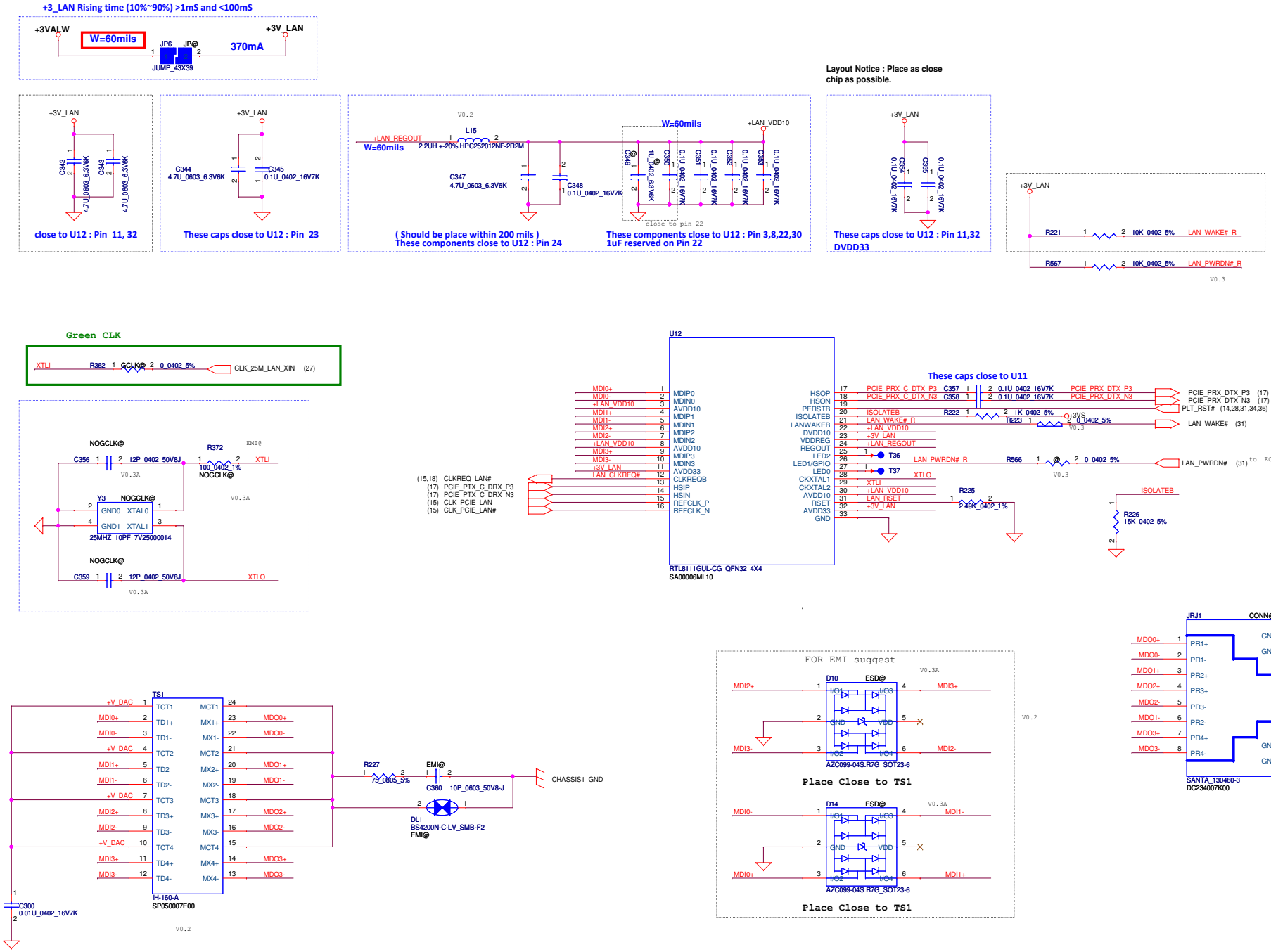

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Compal Electronics, Inc.

Title: LAN-RTL8111GUL

Size: Custom | Document Number: LA-B111P | Rev: 1.0

Date: Tuesday, February 25, 2014 | Sheet 25 of 59

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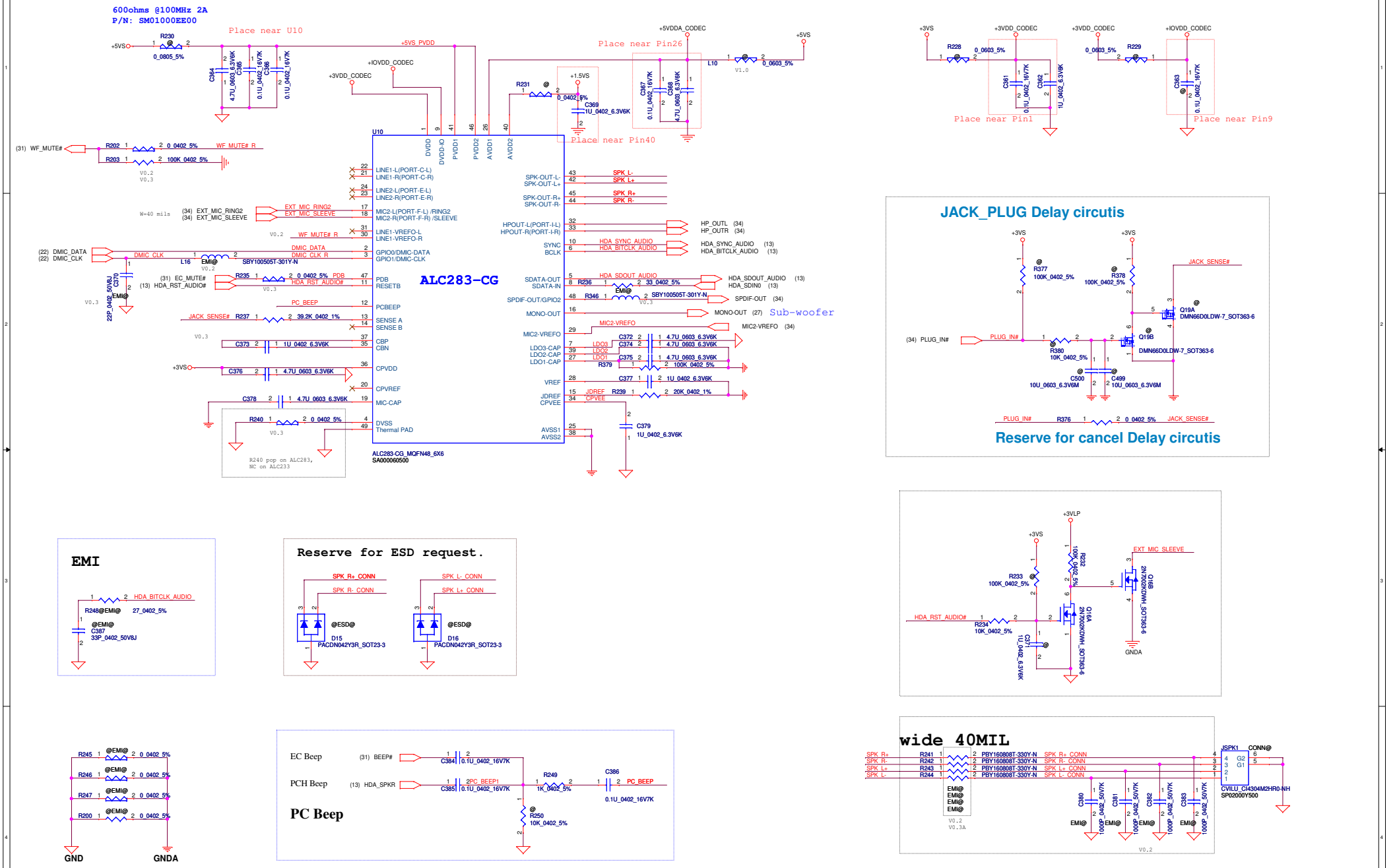

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Compal Electronics, Inc.

Title: **HD Audio ALC283**

Size: C | Document Number: LA-B111P | Rev: 1.0

Date: Tuesday, February 25, 2014 | Sheet 26 of 59

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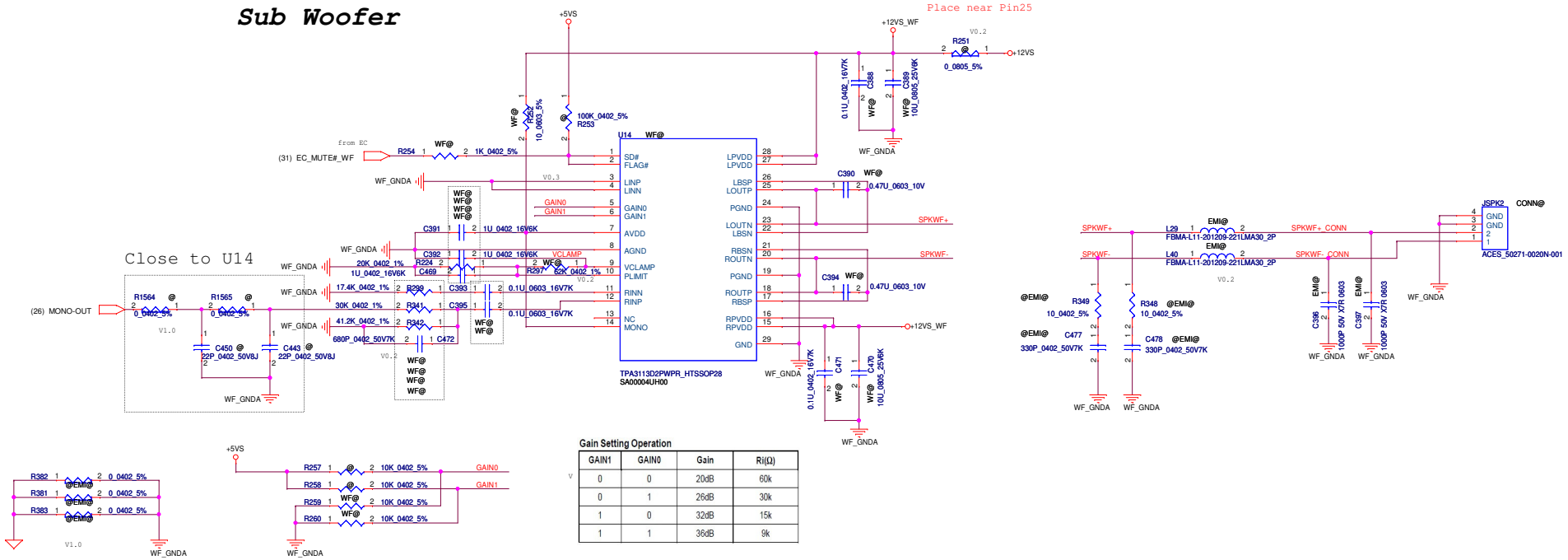
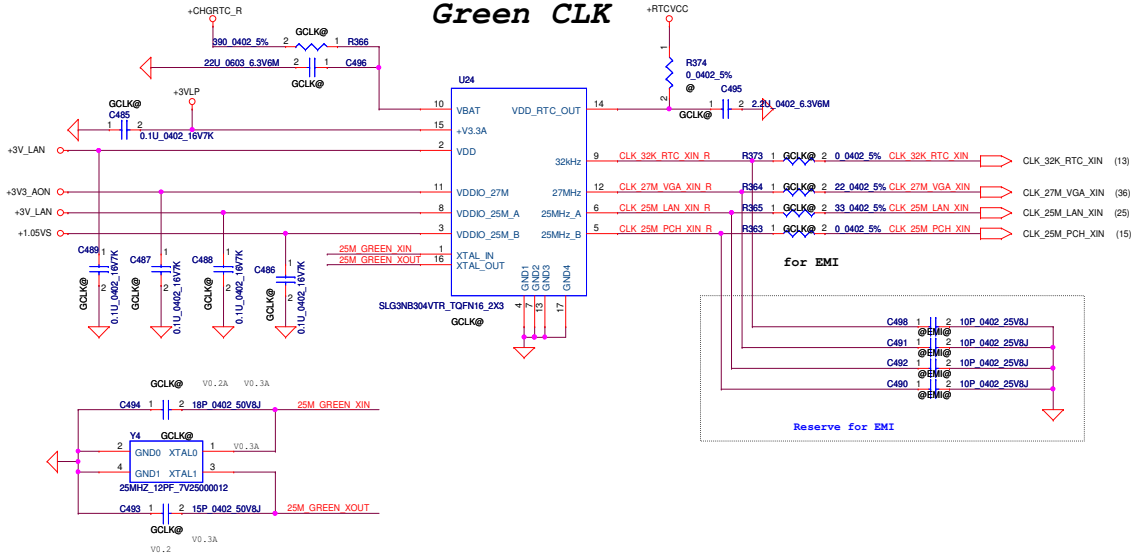
Sub Woofer



Gain Setting Operation

GAIN1	GAIN0	Gain	Ri(Ω)
0	0	20dB	60k
0	1	26dB	30k
1	0	32dB	15k
1	1	36dB	9k

Green CLK



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Compal Electronics, Inc.

Title: Sub-Woofer / Green CLK

Size: C | Document Number: LA-B111P | Rev: 1.0

Date: Tuesday, February 25, 2014 | Sheet 27 of 59

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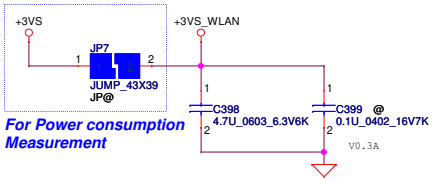
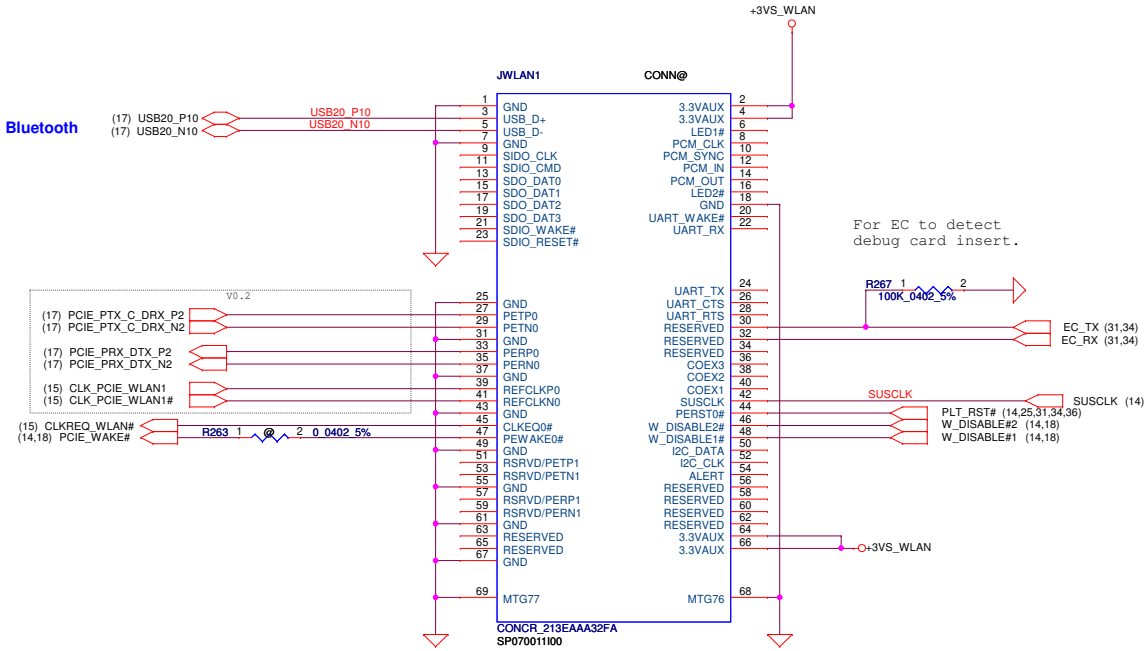
WLAN



NGFF for WLAN (TYPE 2230)



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Title	Compal Electronics, Inc.	
	NGFF (WLAN/BT)	
Size: Custom	Document Number: LA-B111P	Rev: 1.0
Date: Tuesday, February 25, 2014	Sheet 28 of 59	

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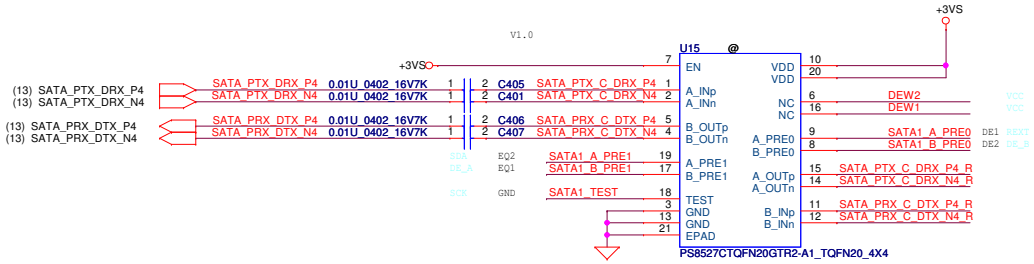
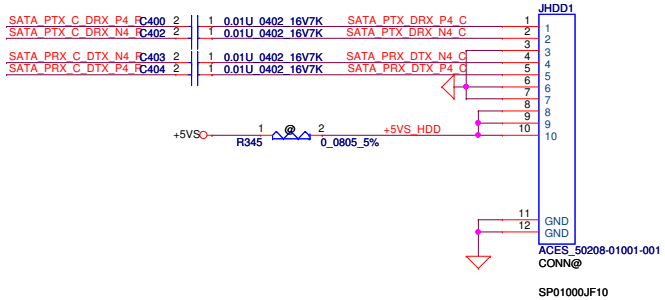
SATA HDD CONN.





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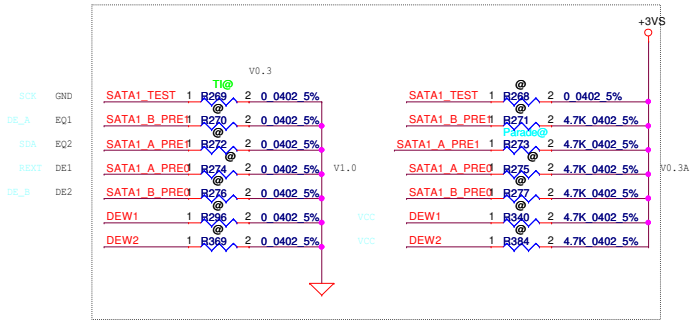
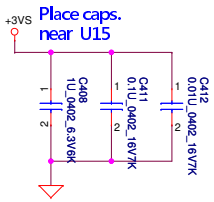
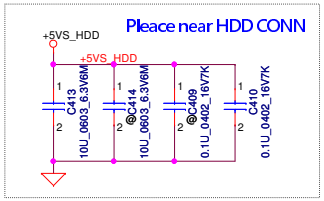
Add EQ pin for PI3EQX6741STZDEX







TI

DE1/DE2	dB
NC	-6
0	0
1	-3

EQ1/EQ2	dB
NC	0
0	7
1	14

V0.3

Asmidia

DE_X	dB
0	+1.5
1	+3.0

Security Classification	Compal Secret Data		
Issued Date	2014/02/25	Deciphered Date	2015/02/25

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Compal Electronics, Inc.

Title: HDD/SSD

Document Number: LA-B111P

Rev: 1.0

Date: Tuesday, February 25, 2014 | Sheet 29 of 59

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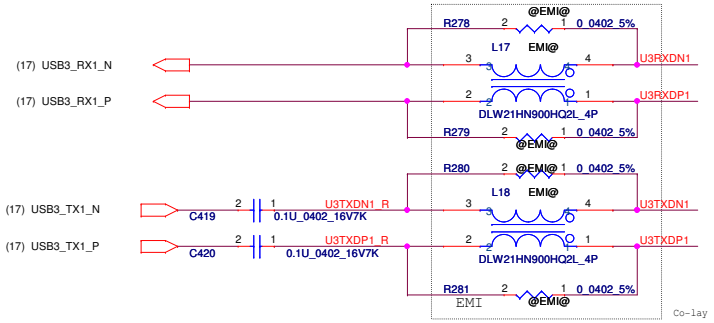

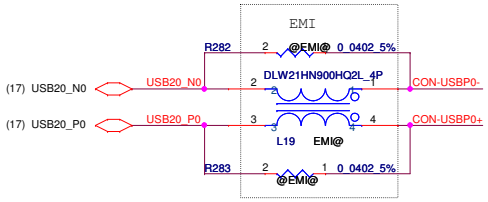

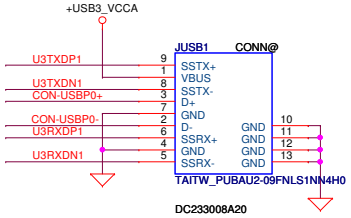

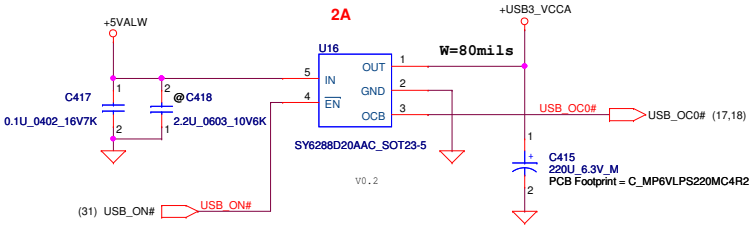

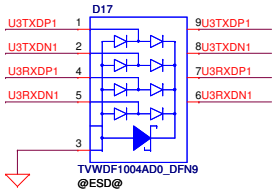

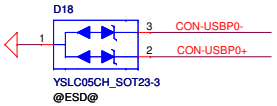

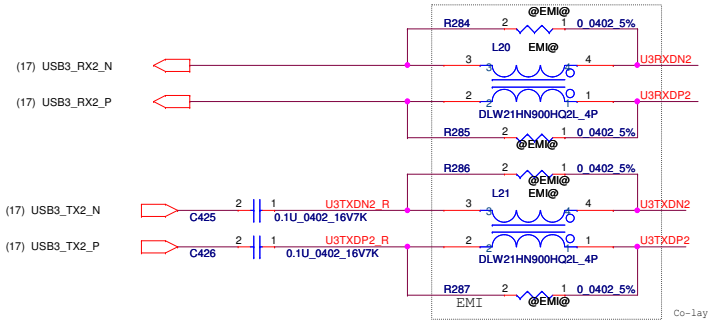

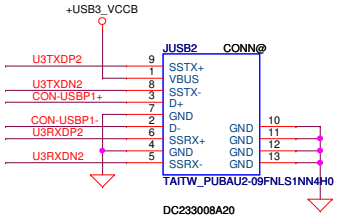

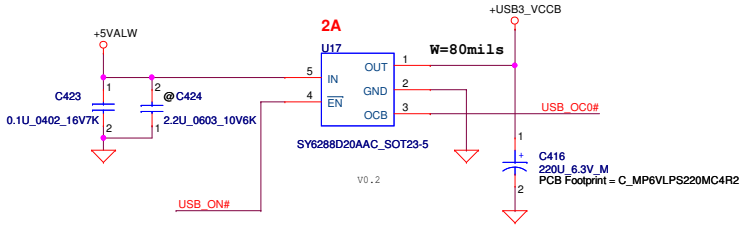

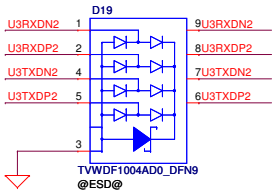

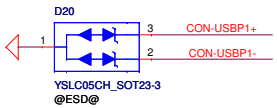

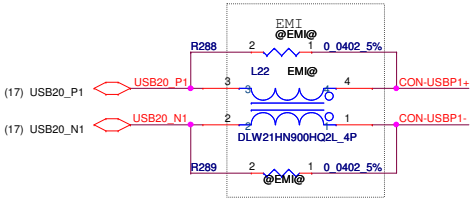

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Issued Date	2014/02/25	Deciphered Date	2015/02/25

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Compal Electronics, Inc.

Title: USB3.0 Port

Size: Custom | Document Number: LA-B111P | Rev: 1.0

Date: Tuesday, February 25, 2014 | Sheet 30 of 59

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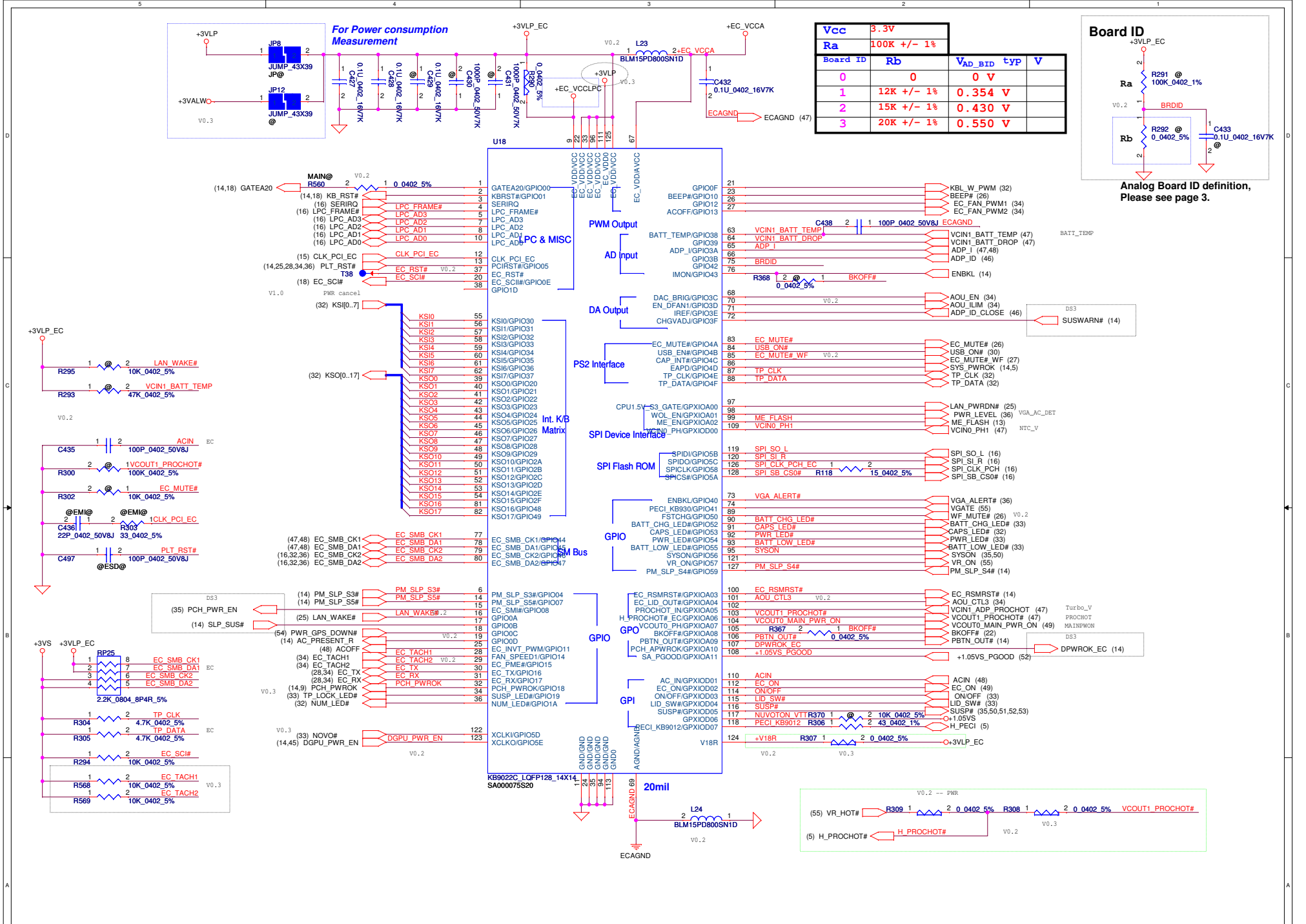

Security Classification	Compal Secret Data		
Issued Date	2014/02/25	Deciphered Date	2015/02/25

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Compal Electronics, Inc.

Title: EC ENE-KB9022 C

Size: Custom | Document Number: LA-B111P | Rev: 1.0

Date: Tuesday, February 25, 2014 | Sheet 31 of 59

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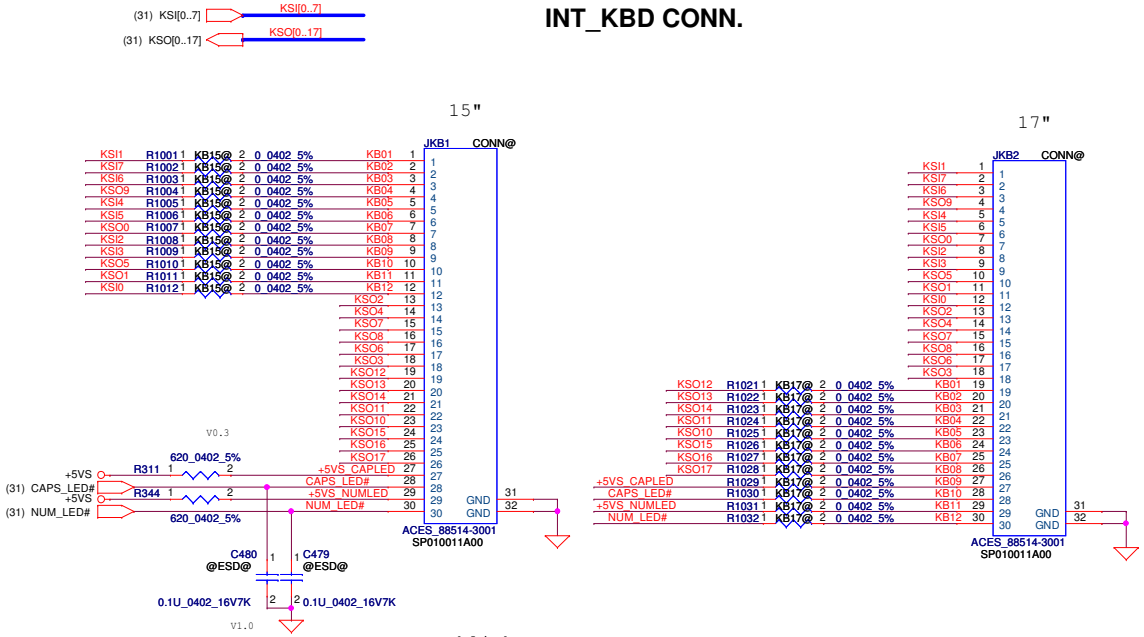
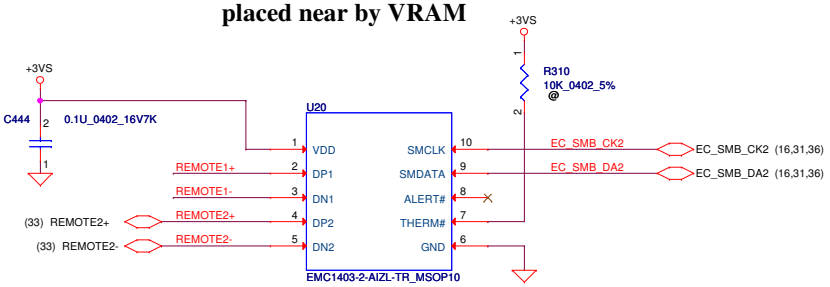
INT_KBD CONN.



KB BackLight Control

SMSC thermal sensor placed near by VRAM



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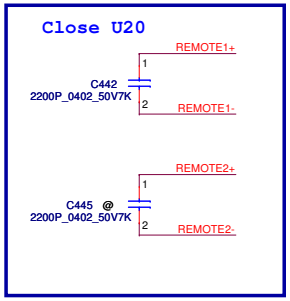

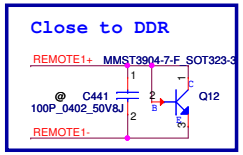

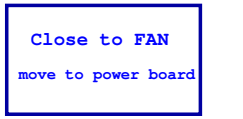

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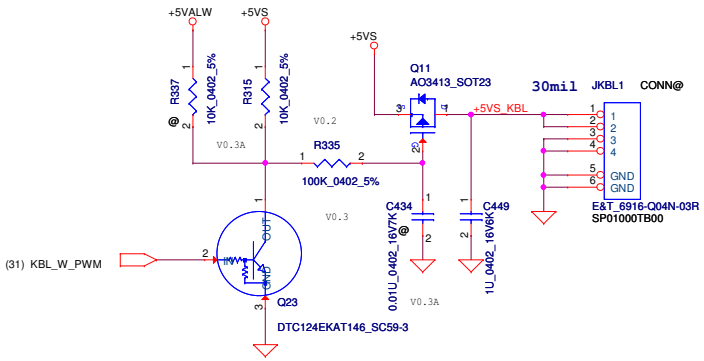

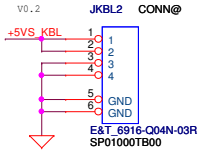

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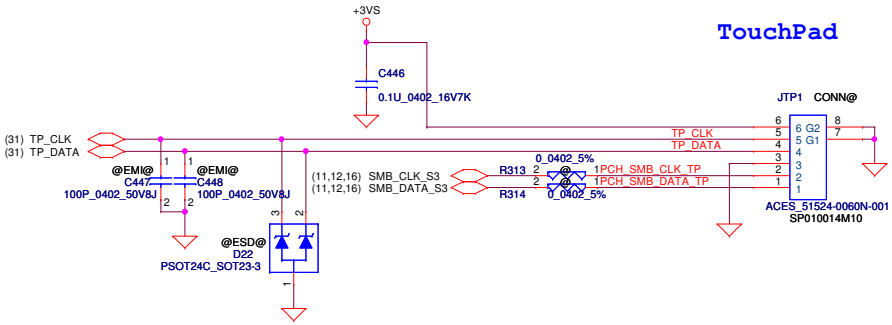

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Issued Date	2014/02/25	Deciphered Date	2015/02/25

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Compal Electronics, Inc.

Title: KB/TP/Thermal sensor

Size: B | Document Number: LA-B111P | Rev: 1.0

Date: Tuesday, February 25, 2014 | Sheet 32 of 59

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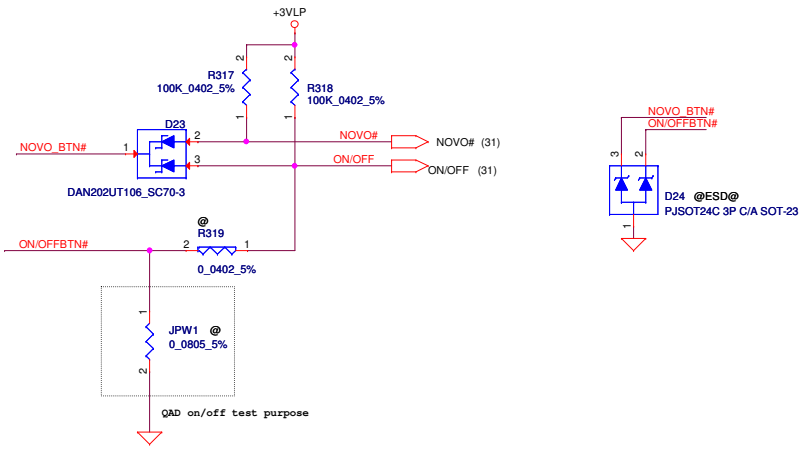
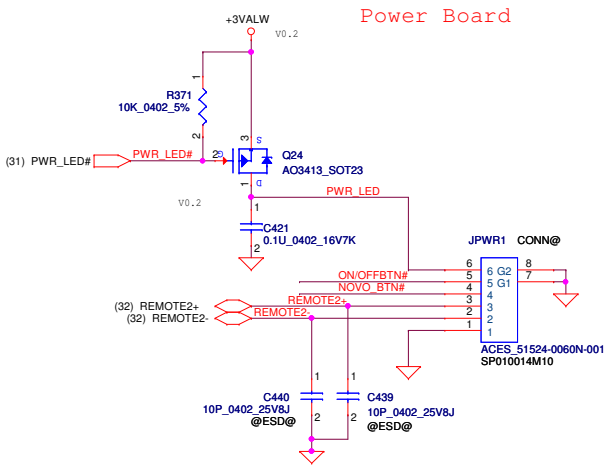
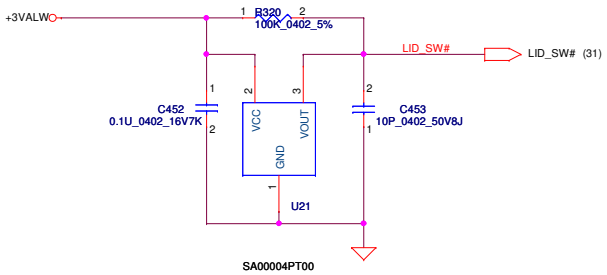


Connector: 0.3A / pin

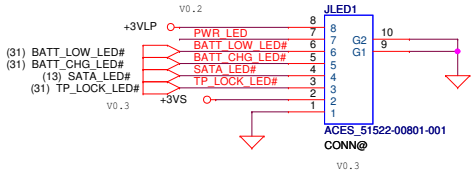
PWR Board CONN.



Lid switch



LED-B CONN



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Issued Date	2014/02/25	Deciphered Date	2015/02/25

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Compal Electronics, Inc.

Title: **PWR_BTN/PWR_B/LED_B/LID**

Document Number: *LA-B111P* | Rev 1.0

Date: Tuesday, February 25, 2014 | Sheet 33 of 59

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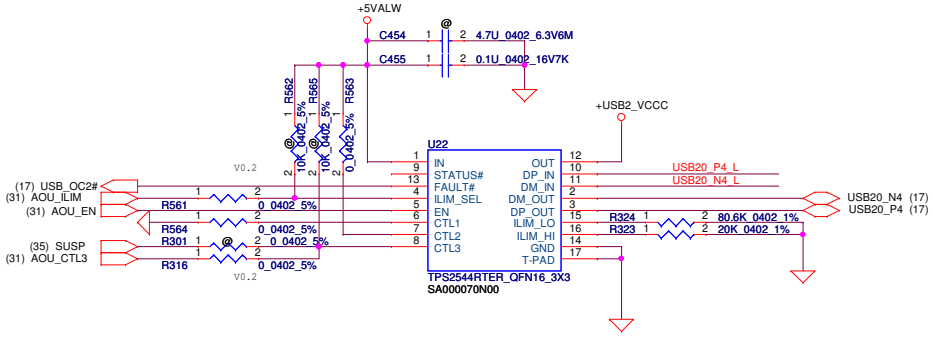
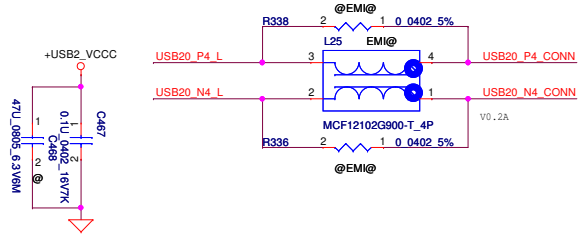
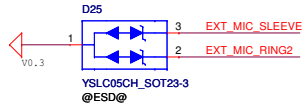


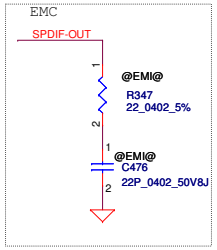


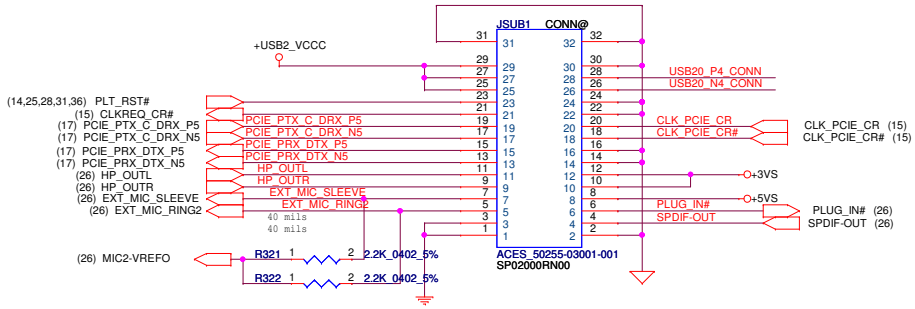


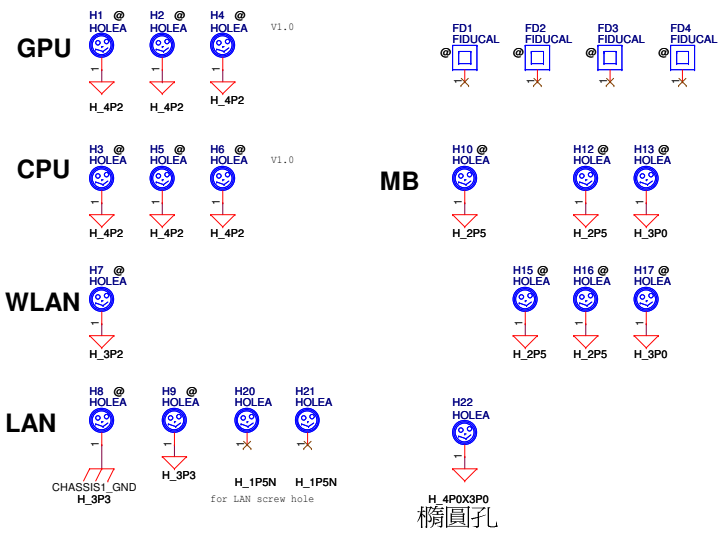
Alway on USB	Mode	CTL1~3,ILIM_SEL
Enable	S0	0 1 0 1
	S3/S4/S5	0 1 1 1
Disable	S0	0 1 0 1
	S3	0 1 0 0
	S4/S5	0 1 0 0

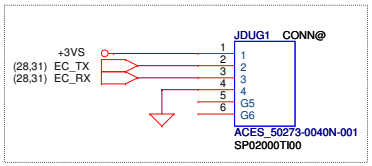
V0.2

USB Board CONN.

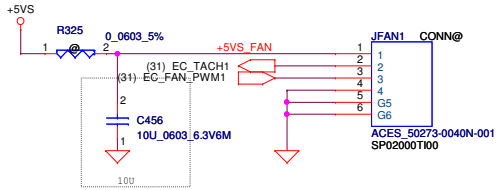




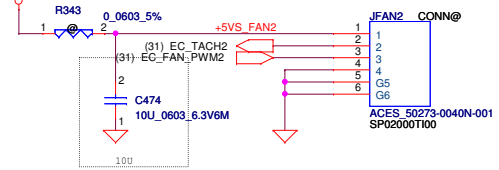




Fan1 Control Circuit



FAN2 Control Circuit



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Compal Electronics, Inc.

Title: USB charge/FAN/Screw holes

Document Number: LA-B111P

Rev: 1.0

Date: Tuesday, February 25, 2014 | Sheet 34 of 59

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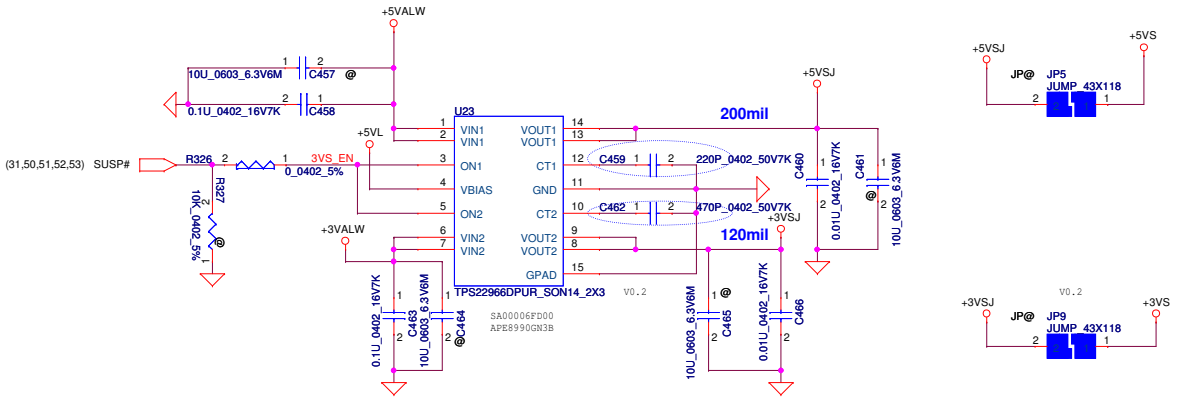
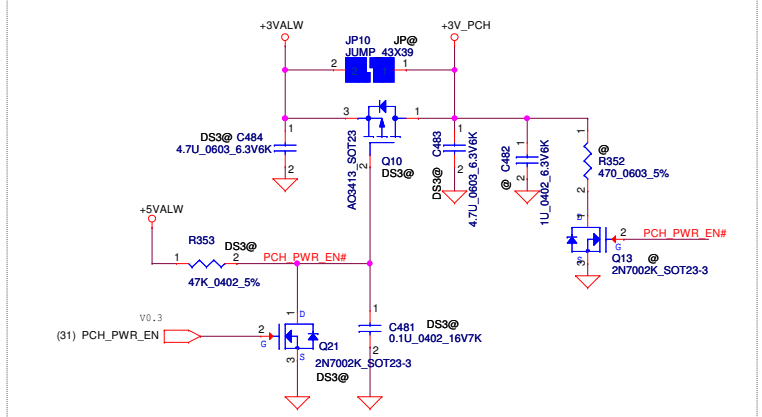
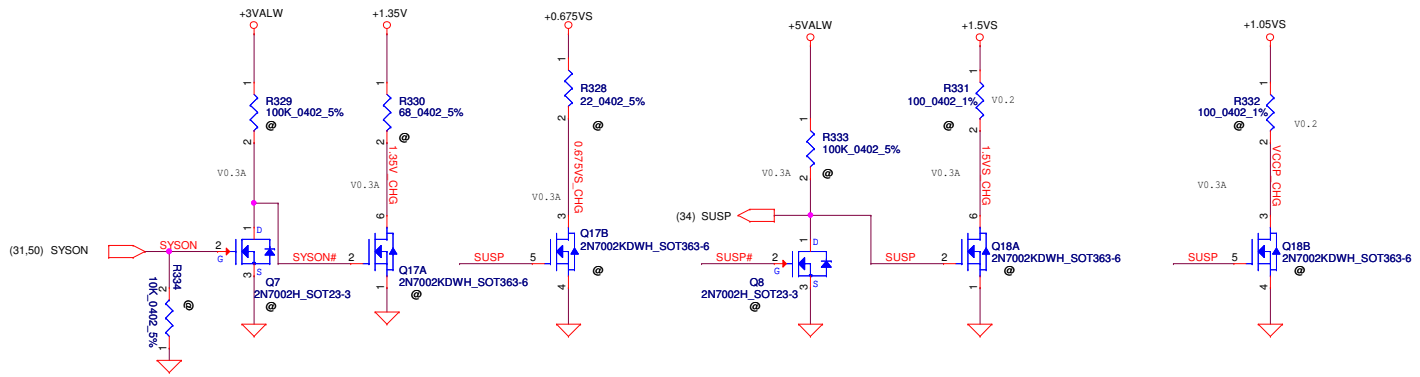
+5VALW to +5VS Transfer



+3VALW to +3VS Transfer



Discharge circuit-1



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Issued Date	2014/02/25	Deciphered Date	2015/02/25

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Compal Electronics, Inc.

Title: DC/DC Interface

Document Number: LA-B111P

Rev: 1.0

Date: Tuesday, February 25, 2014 | Sheet 35 of 59

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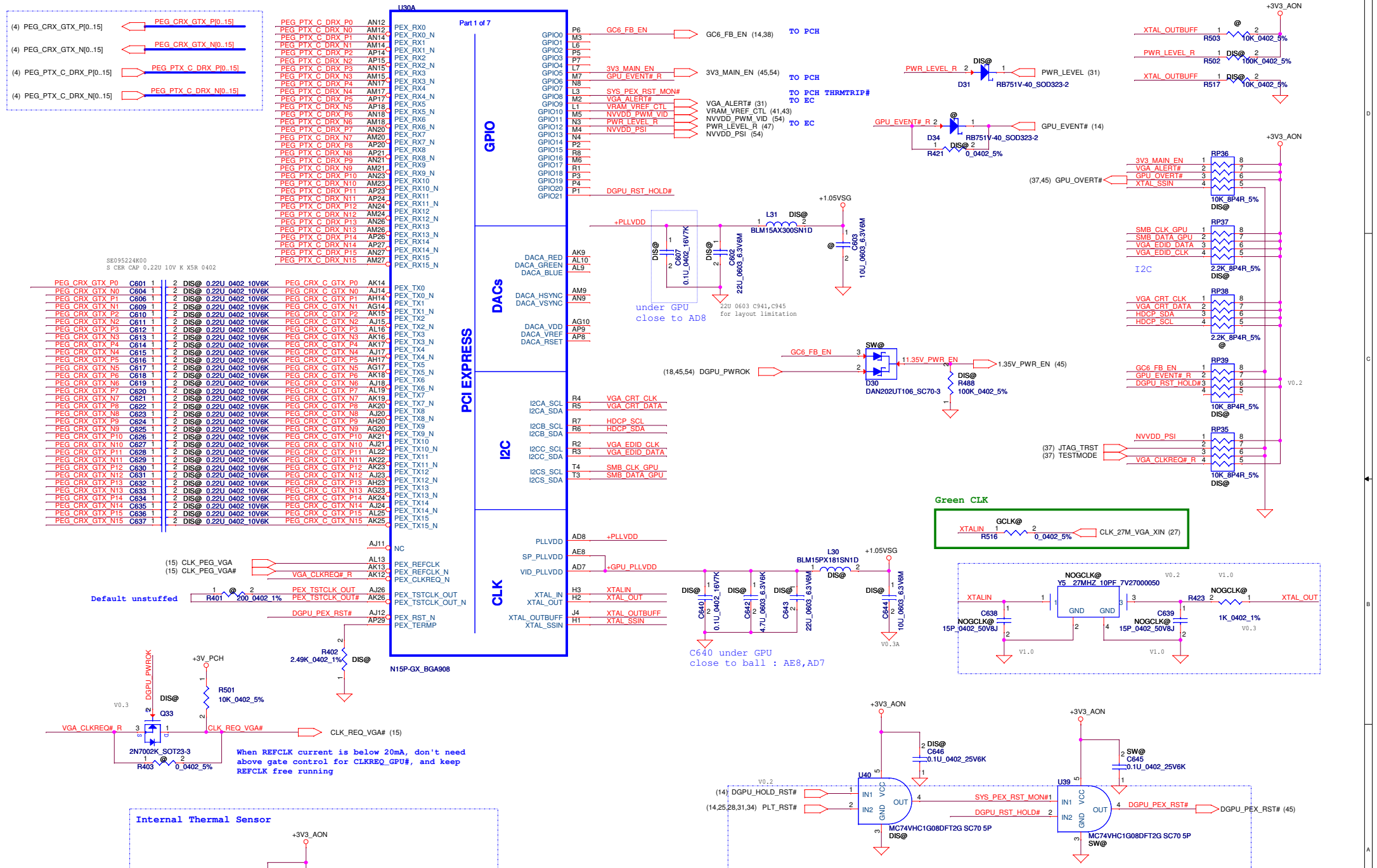

Security Classification	Compal Secret Data		
Issued Date	2014/02/25	Deciphered Date	2015/02/25

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Compal Electronics, Inc.

Title: N15P-GX (1/5) PEG & DAC

Size: Custom | Document Number: LA-B111P | Rev: 1.0

Date: Tuesday, February 25, 2014 | Sheet 36 of 59

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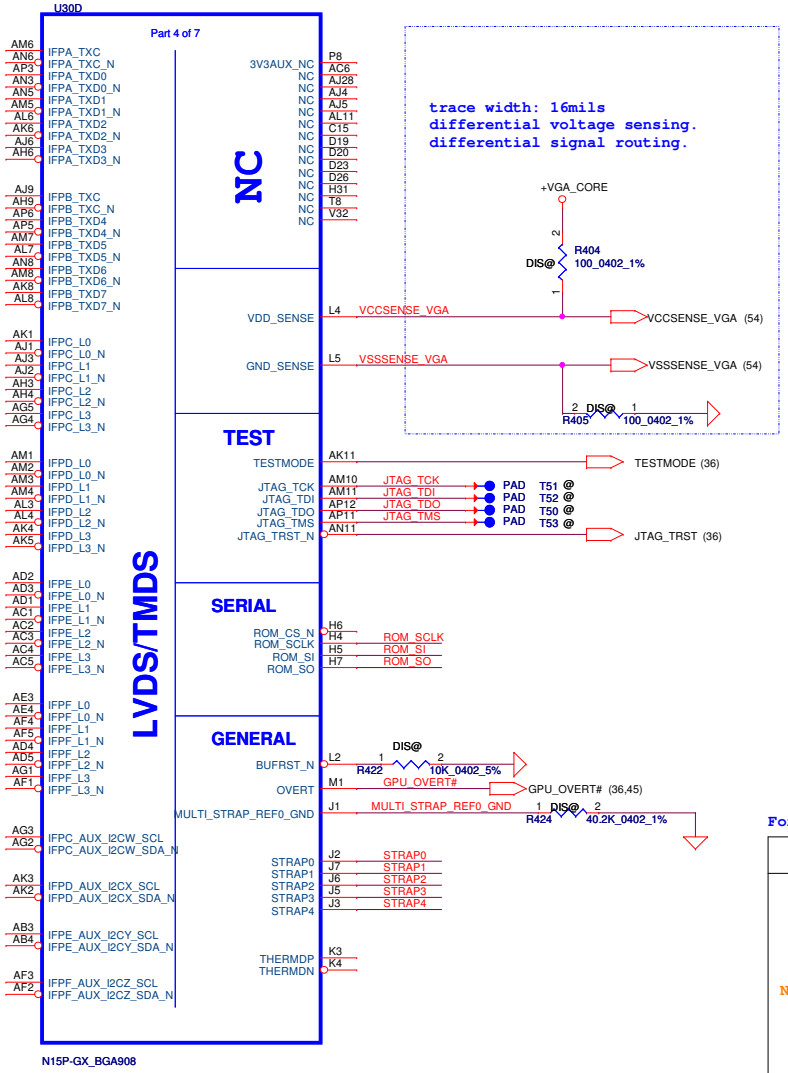
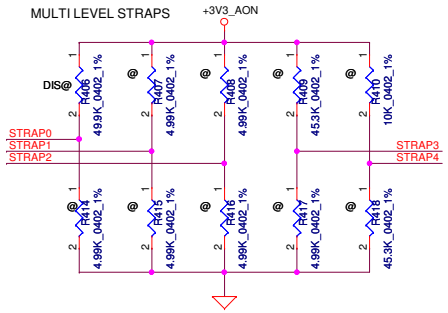
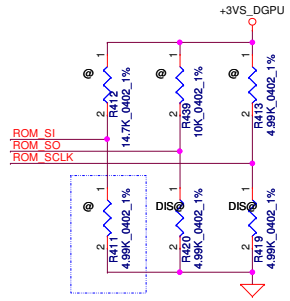


Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_DGPU	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SO	+3VS_DGPU	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SI	+3VS_DGPU	**DEVID_SEL**	**PCIE_CFG**	**SMB_ALT_ADDR**	VGA_DEVICE
STRAP0	Keep pull-up to 3V3_AON and pull-down to GND foot print and stuff 50K ohm pull-up				
STRAP1	RESERVED				
STRAP2					
STRAP3					
STRAP4					

SKU	Device ID	bit5 to bit0
N15P-GX	0x1392	

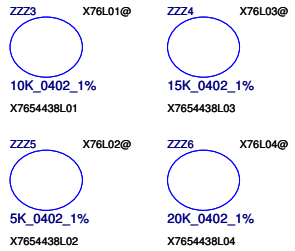
Resistor Values	Pull-up to +3VS _DGPU	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111





For X76 (N15P-GX)

GPU	FB Memory DDR5					ROM_SI
N15P-GX	128Mx16	X76L02@	Samsung	2G	K4G20325FD-FC03	PD 5K
		X76L01@	Hynix	2G	H5GC2H24BFR-T2C	PD 10K
	256Mx16	X76L03@	Hynix	4G	H5GC4H24MFR-T2C	PD 15K
		X76L04@	Samsung	4G	K4G41325FC-HC03	PD 20K



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Compal Electronics, Inc.

Title: N15P-GX (2/5) TMDS/LVDS

Size: B/25 Custom | Document Number: LA-B111P | Rev: 1.0

Date: Tuesday, February 25, 2014 | Sheet 37 of 59

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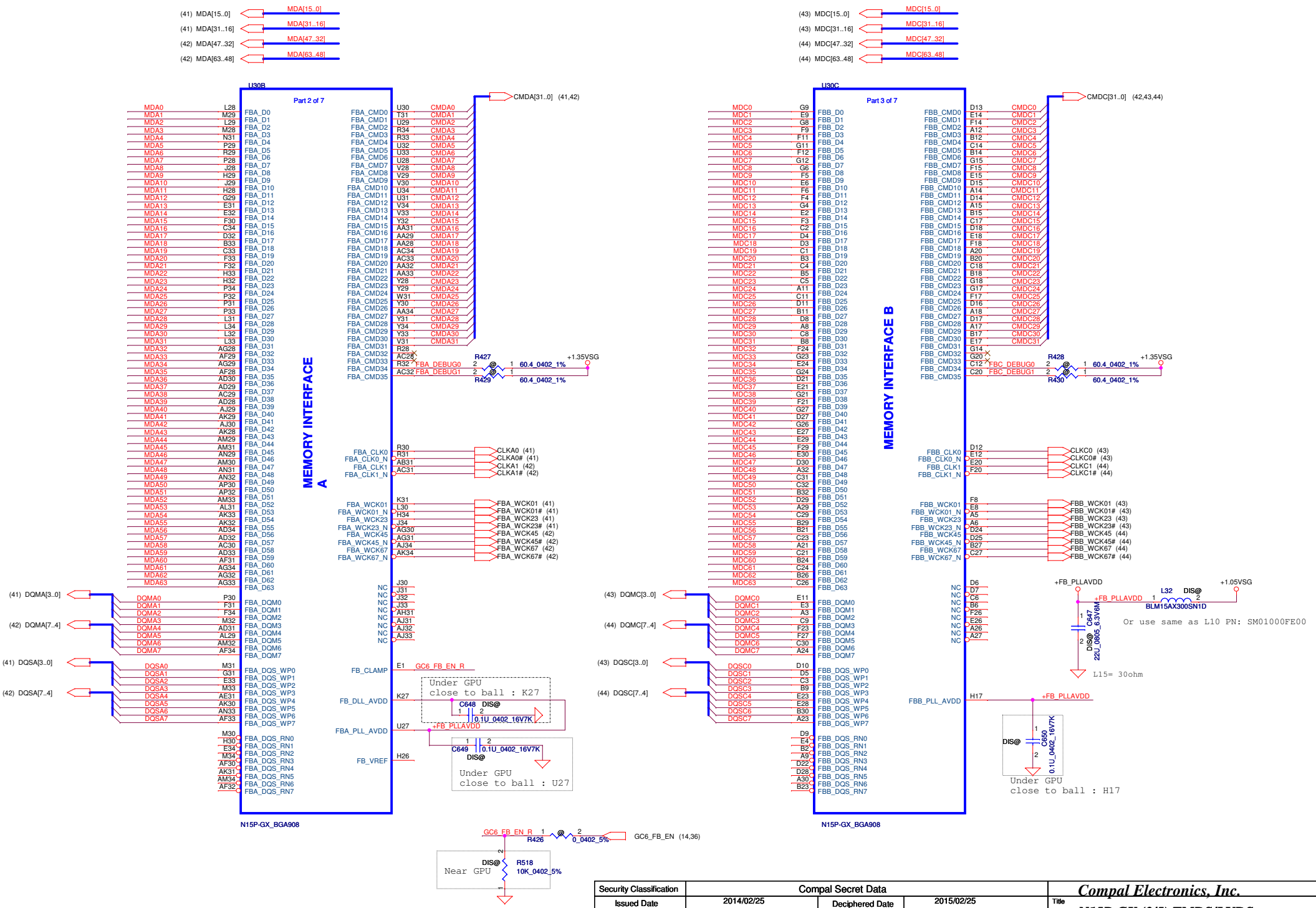

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Compal Electronics, Inc.

Title: N15P-GX (3/5) TMDS/LVDS

Size: B/25 Custom | Document Number: LA-B111P | Rev: 1.0

Date: Tuesday, February 25, 2014 | Sheet 38 of 59

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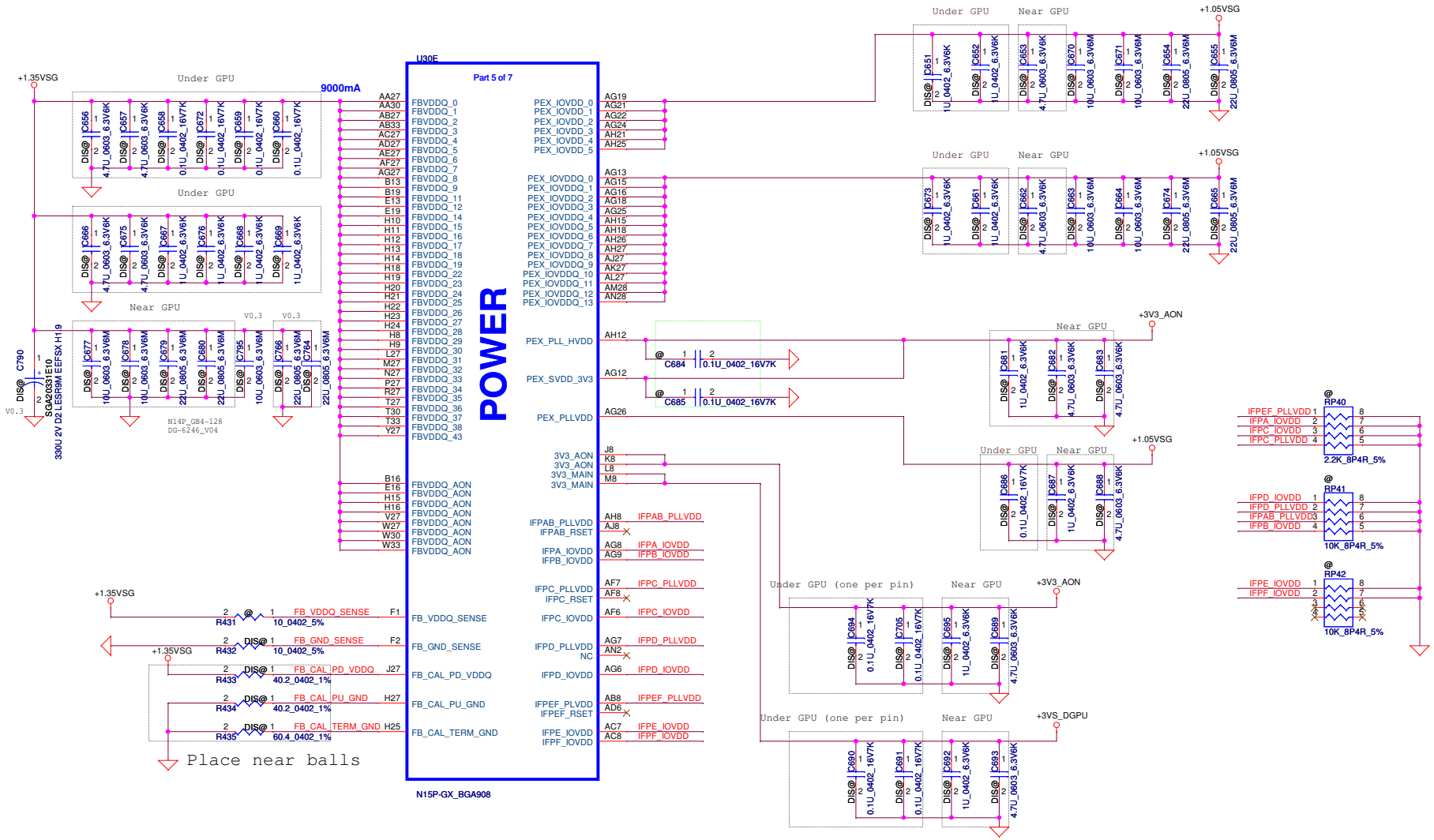

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Compal Electronics, Inc.

Title: N15P-GX (4/5) POWER

Size: B/26 Custom | Document Number: LA-B111P | Rev: 1.0

Date: Tuesday, February 25, 2014 | Sheet 39 of 59

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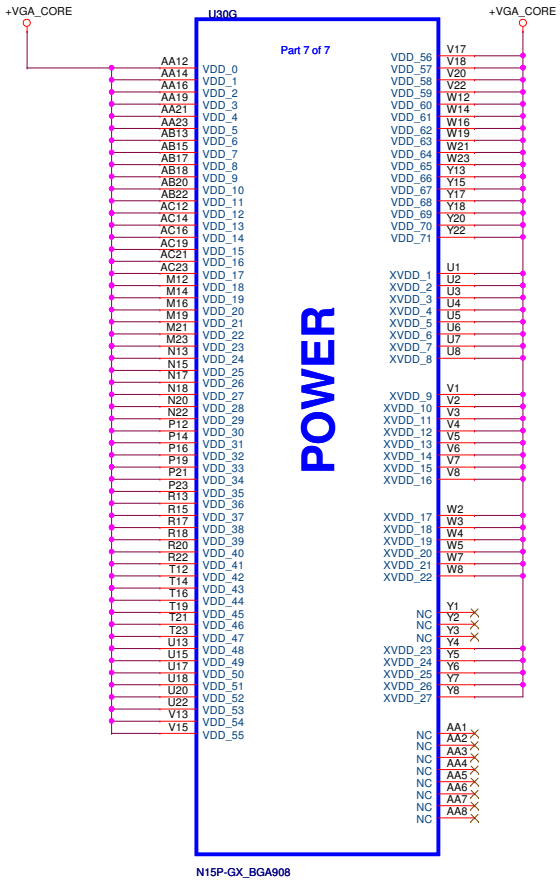

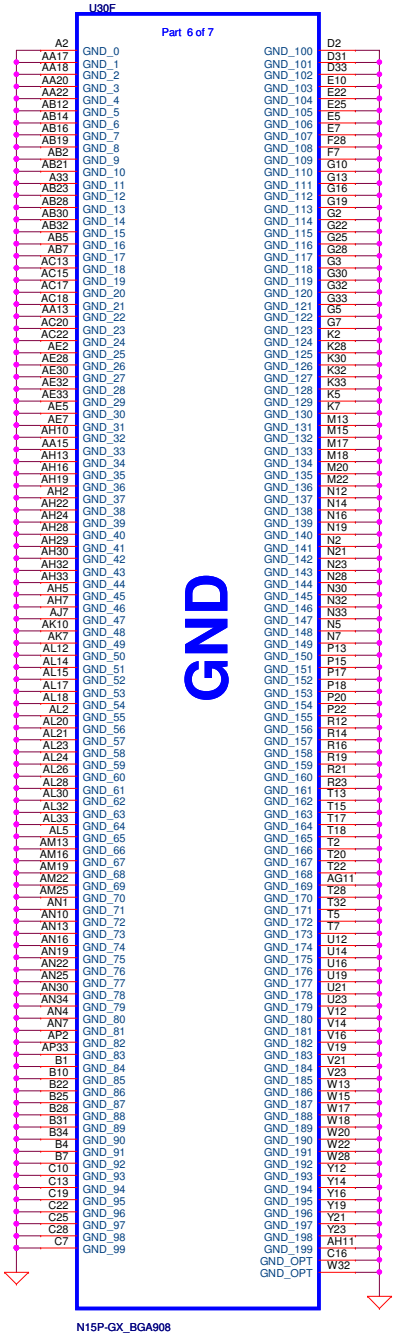

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Issued Date	2014/02/25	Deciphered Date	2015/02/25

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Compal Electronics, Inc.

Title: N15P-GX (5/5) POWER/ GND

Size: Custom | Document Number: LA-B111P | Rev: 1.0

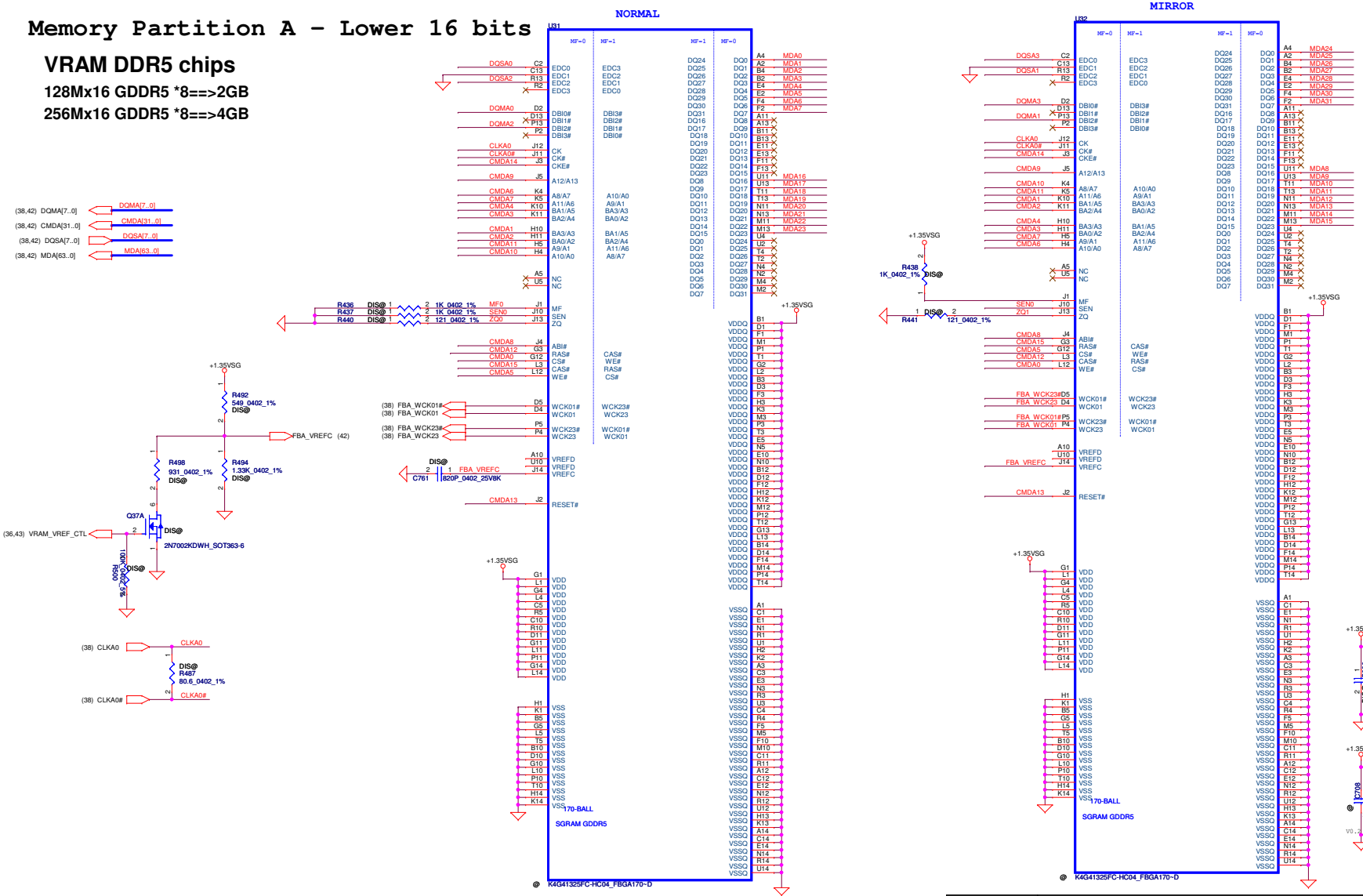
Date: Tuesday, February 25, 2014 | Sheet 40 of 59

Memory Partition A - Lower 16 bits

VRAM DDR5 chips

128Mx16 GDDR5 *8==>2GB

256Mx16 GDDR5 *8==>4GB



Mode H Address	0..31	Mode H Address	32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	ABI*	CMD24	ABI*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CK1*	CMD30	CK1*
CMD15	CAS*	CMD31	CAS*
CMD32	NO USED		
CMD33	NO USED		
CMD34	Debug0		
CMD35	Debug1		

Security Classification	Compal Secret Data		
Issued Date	2014/02/25	Deciphered Date	2015/02/25

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Compal Electronics, Inc.

Title: N15P-GX GDDR5 1/4

Size: A3 | Document Number: LA-B111P | Rev: 1.0

Date: Tuesday, February 25, 2014 | Sheet 41 of 59

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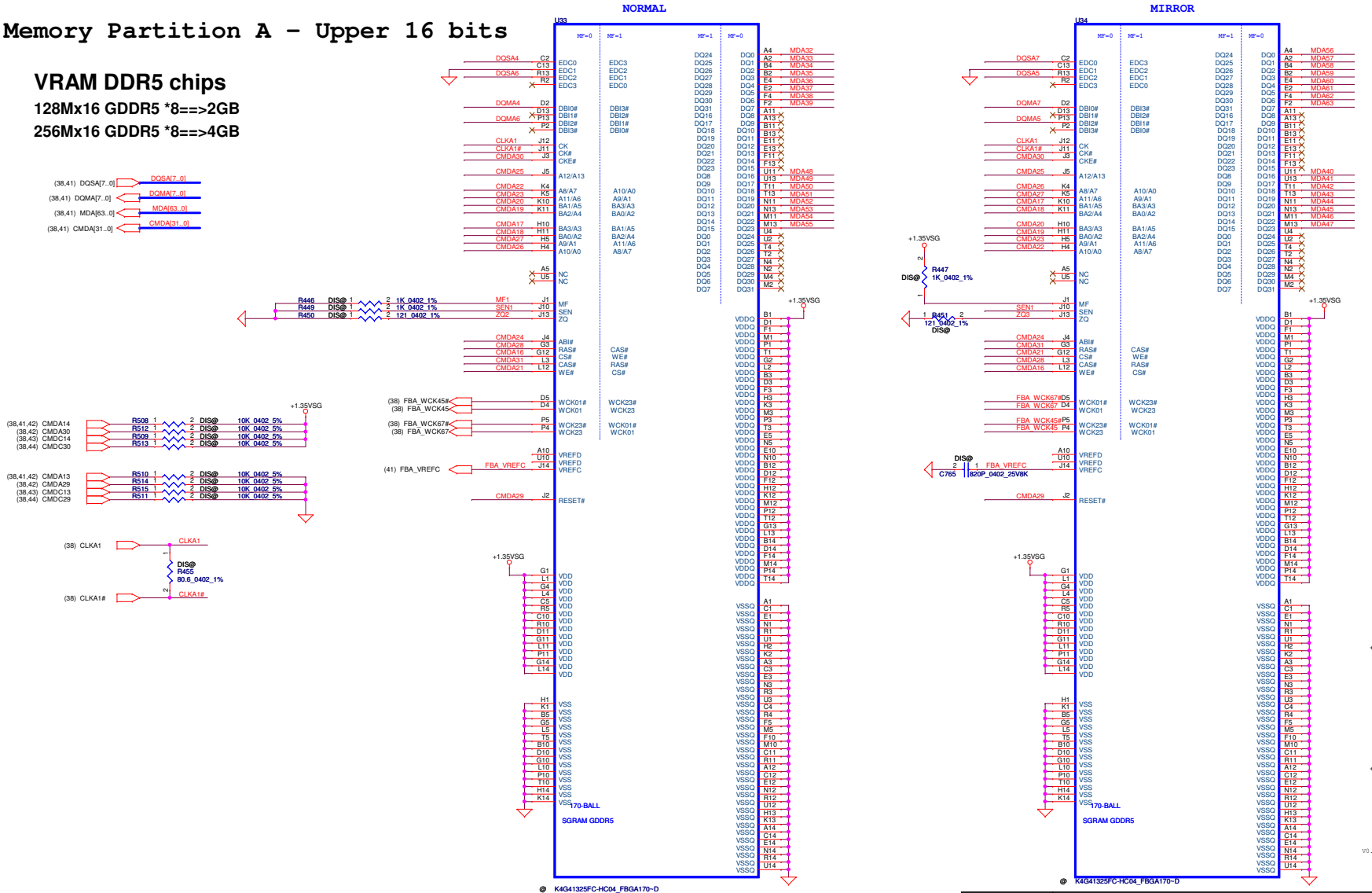
Memory Partition A - Upper 16 bits

VRAM DDR5 chips

128Mx16 GDDR5 *8==>2GB

256Mx16 GDDR5 *8==>4GB



Mode H Address	0..31	Mode H Address	32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	ABI*	CMD24	ABI*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CK1*	CMD30	CK1*
CMD15	CAS*	CMD31	CAS*
CMD32	NO USED		
CMD33	NO USED		
CMD34	Debug0		
CMD35	Debug1		

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: **N15P-GX GDDR5 2/4**

Document Number: **LA-B111P** Rev 1.0

Date: Tuesday, February 25, 2014 Sheet 42 of 59

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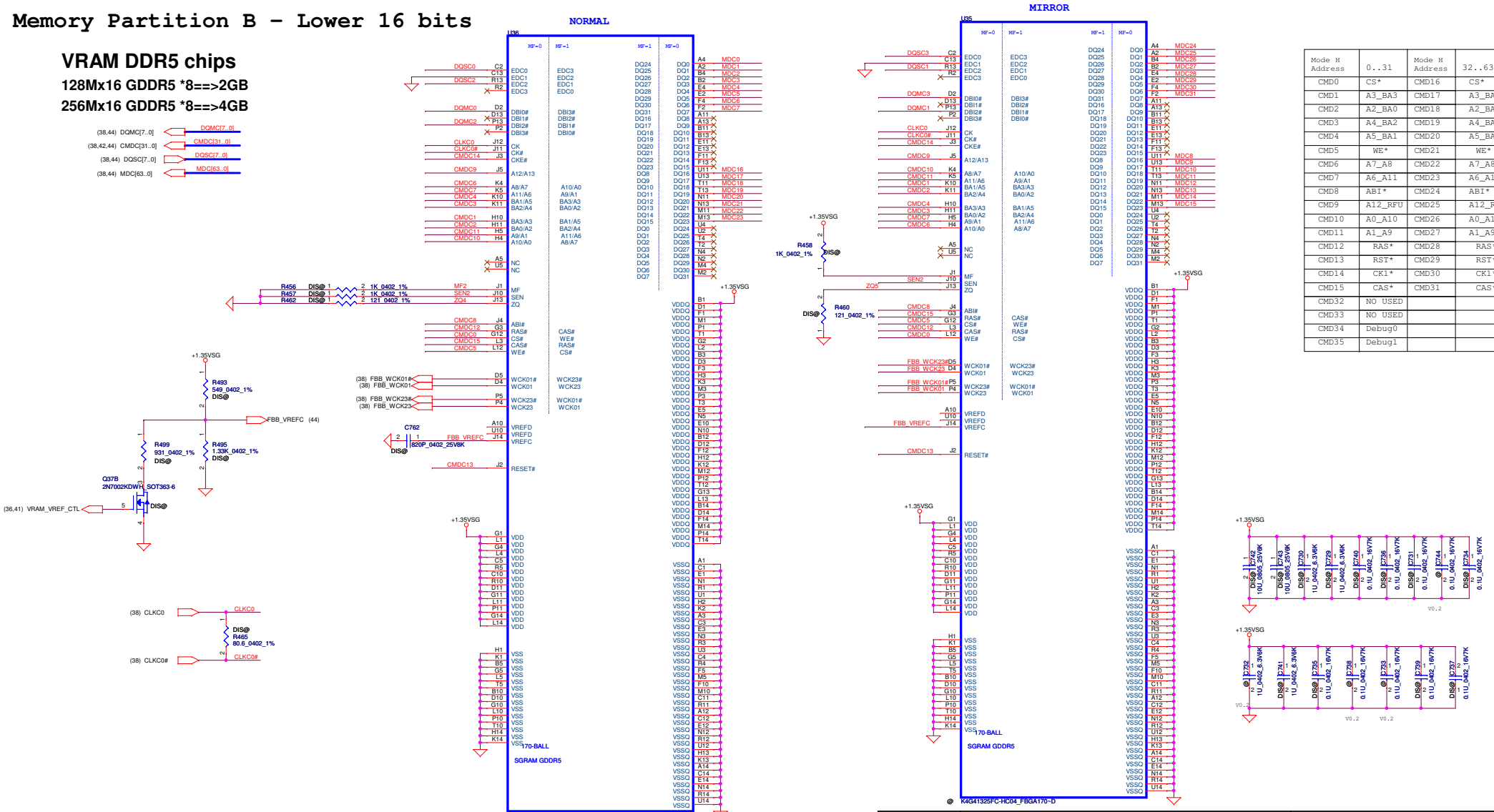
Memory Partition B - Lower 16 bits

VRAM DDR5 chips

128Mx16 GDDR5 *8==>2GB

256Mx16 GDDR5 *8==>4GB



Mode H Address	0..31	Mode H Address	32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	ABI*	CMD24	ABI*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CK1*	CMD30	CK1*
CMD15	CAS*	CMD31	CAS*
CMD32	NO USED		
CMD33	NO USED		
CMD34	Debug0		
CMD35	Debug1		

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: **N15P-GX GDDR5 3/4**

Size: Custom | Document Number: **LA-B111P** | Rev: 1.0

Date: Tuesday, February 25, 2014 | Sheet 43 of 59

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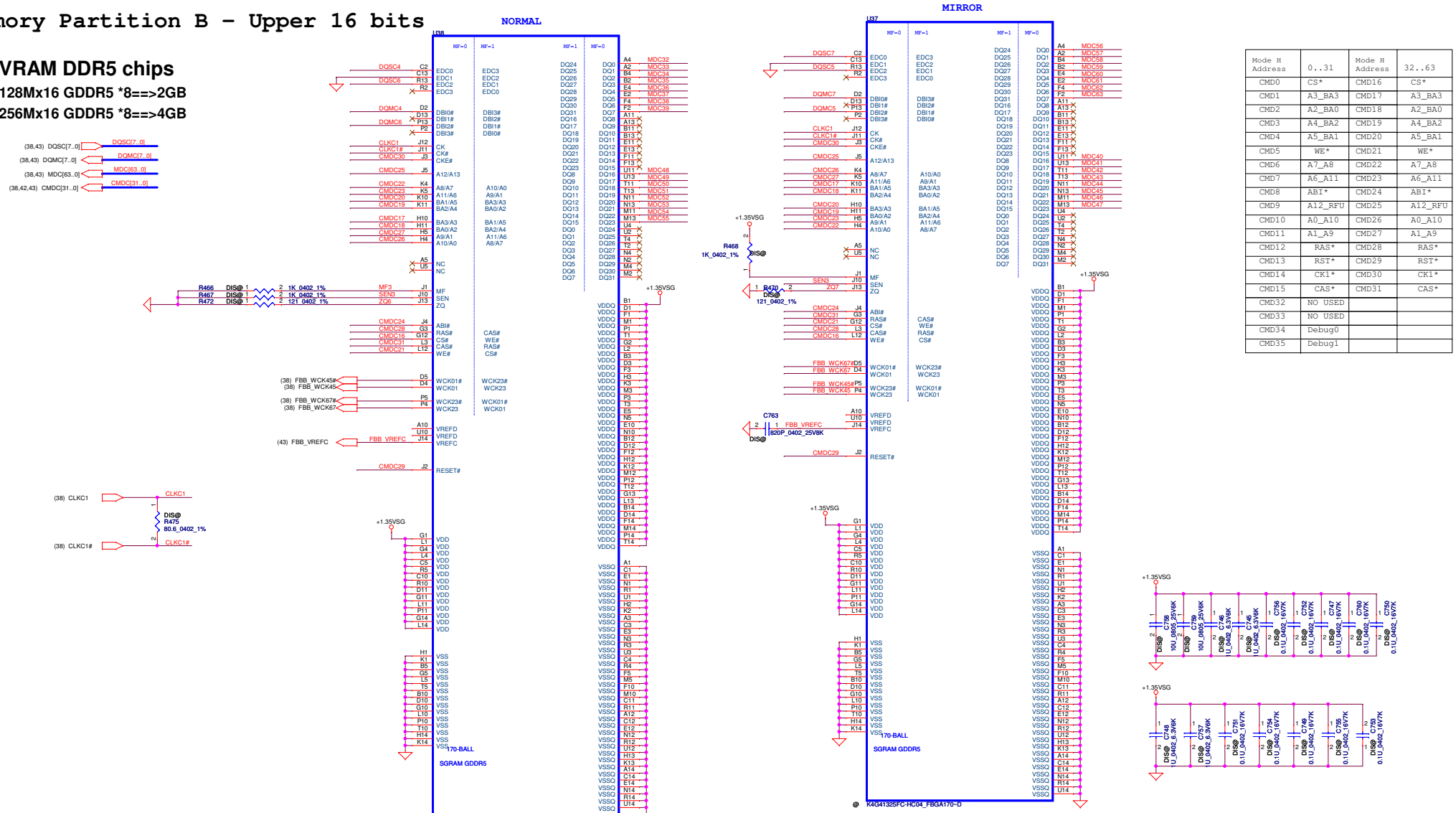
Memory Partition B - Upper 16 bits

VRAM DDR5 chips

128Mx16 GDDR5 *8==>2GB

256Mx16 GDDR5 *8==>4GB



Mode H Address	0..31	Mode H Address	32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	ABI*	CMD24	ABI*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CK1*	CMD30	CK1*
CMD15	CAS*	CMD31	CAS*
CMD32	NO USED		
CMD33	NO USED		
CMD34	Debug0		
CMD35	Debug1		

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Compal Electronics, Inc.

Title: **N15P-GX GDDR5 4/4**

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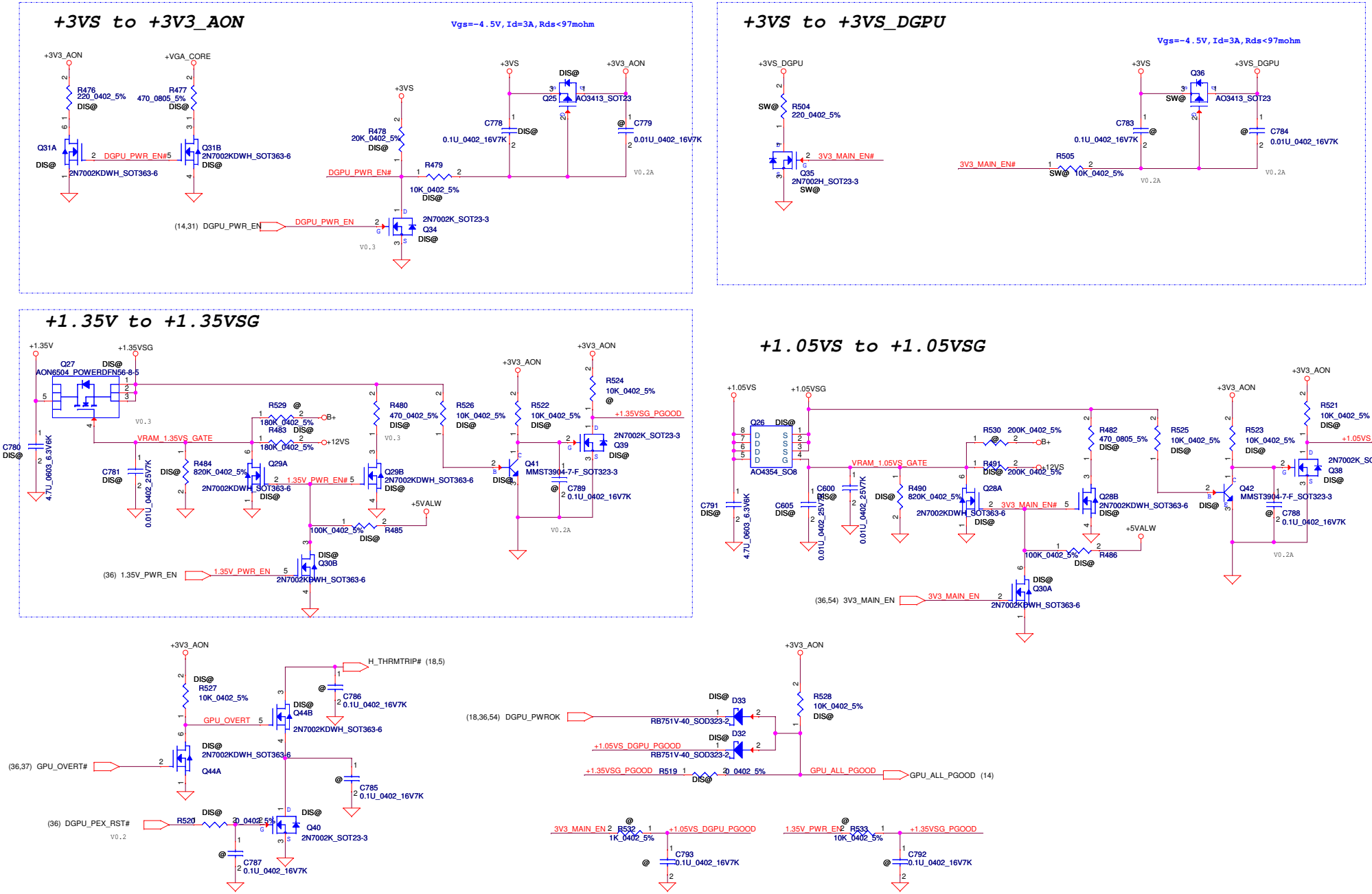

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Compal Electronics, Inc.

Title: **N15P-GX DC-DC**

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Date: Tuesday, February 25, 2014 | Sheet 45 of 59

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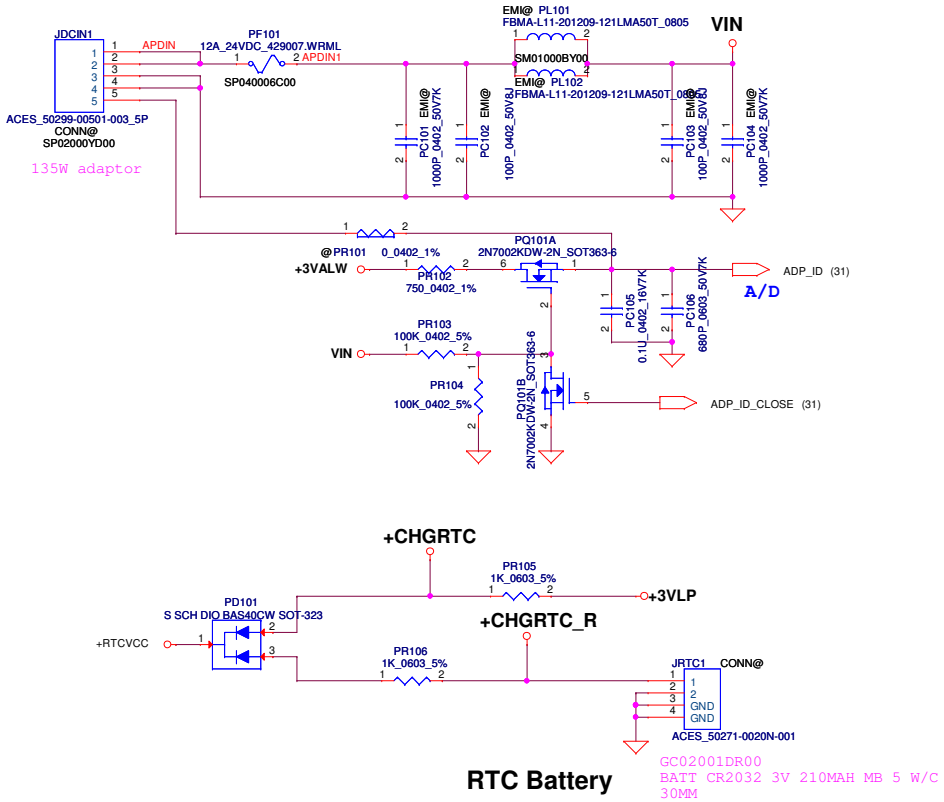

RTC Battery

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Compal Electronics, Inc.

Title: **PWR DCIN / RTC Battery**

Size: Custom | Document Number: **BE_BDW** | Rev: 1.0

Date: Tuesday, February 25, 2014 | Sheet 46 of 59

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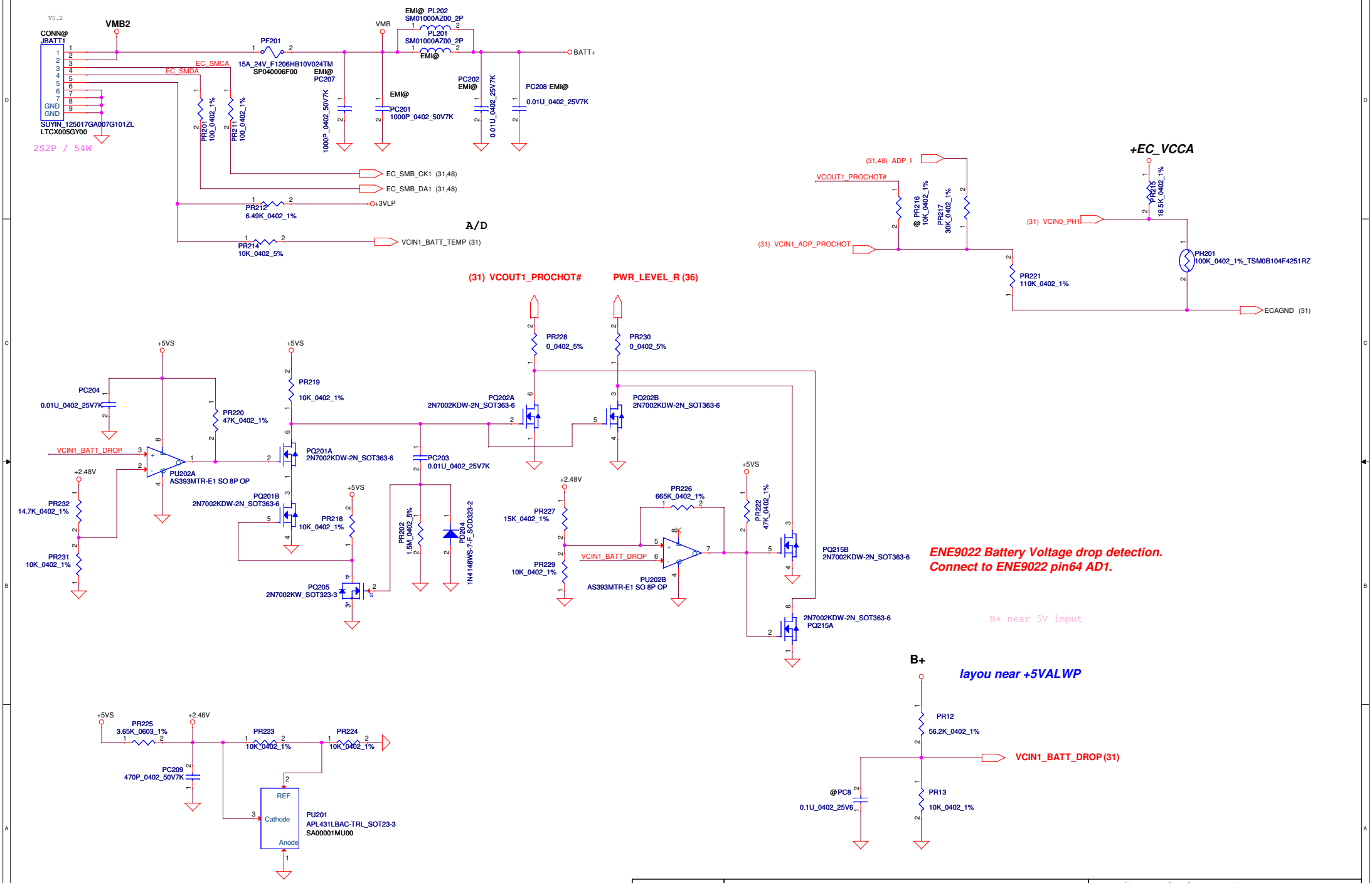

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Compal Electronics, Inc.

Title: PWR-BATTERY CONN/OTP

Size: Custom | Document Number: BE_BDW | Rev: 1.0

Date: Tuesday, February 25, 2014 | Sheet 47 of 59

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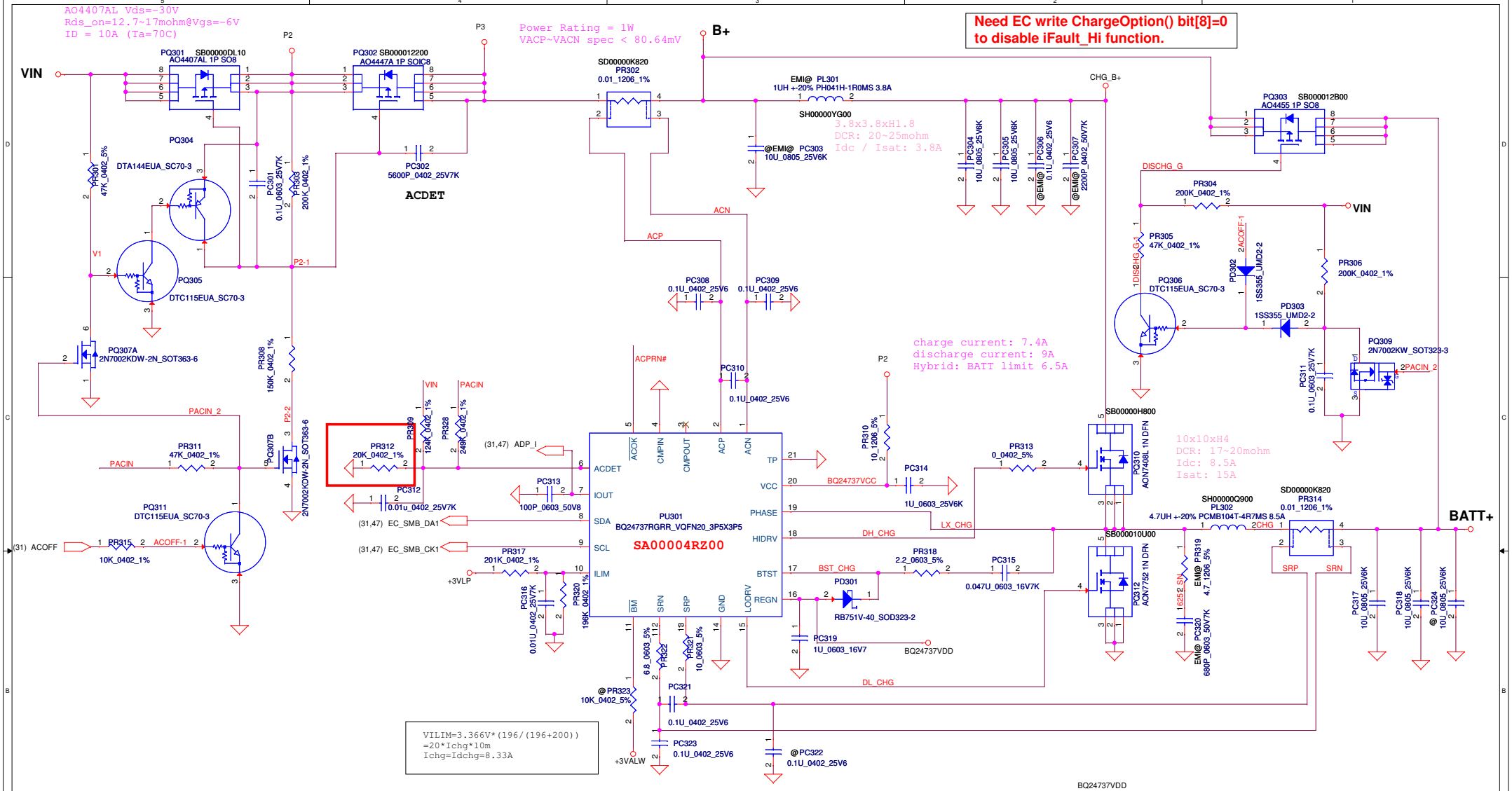

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Issued Date	2014/02/25	Deciphered Date	2015/02/25	Title: Charger_BQ24737
				Size: Document Number: BE_BDW Rev: 1.0
				Date: Tuesday, February 25, 2014 Sheet 48 of 59

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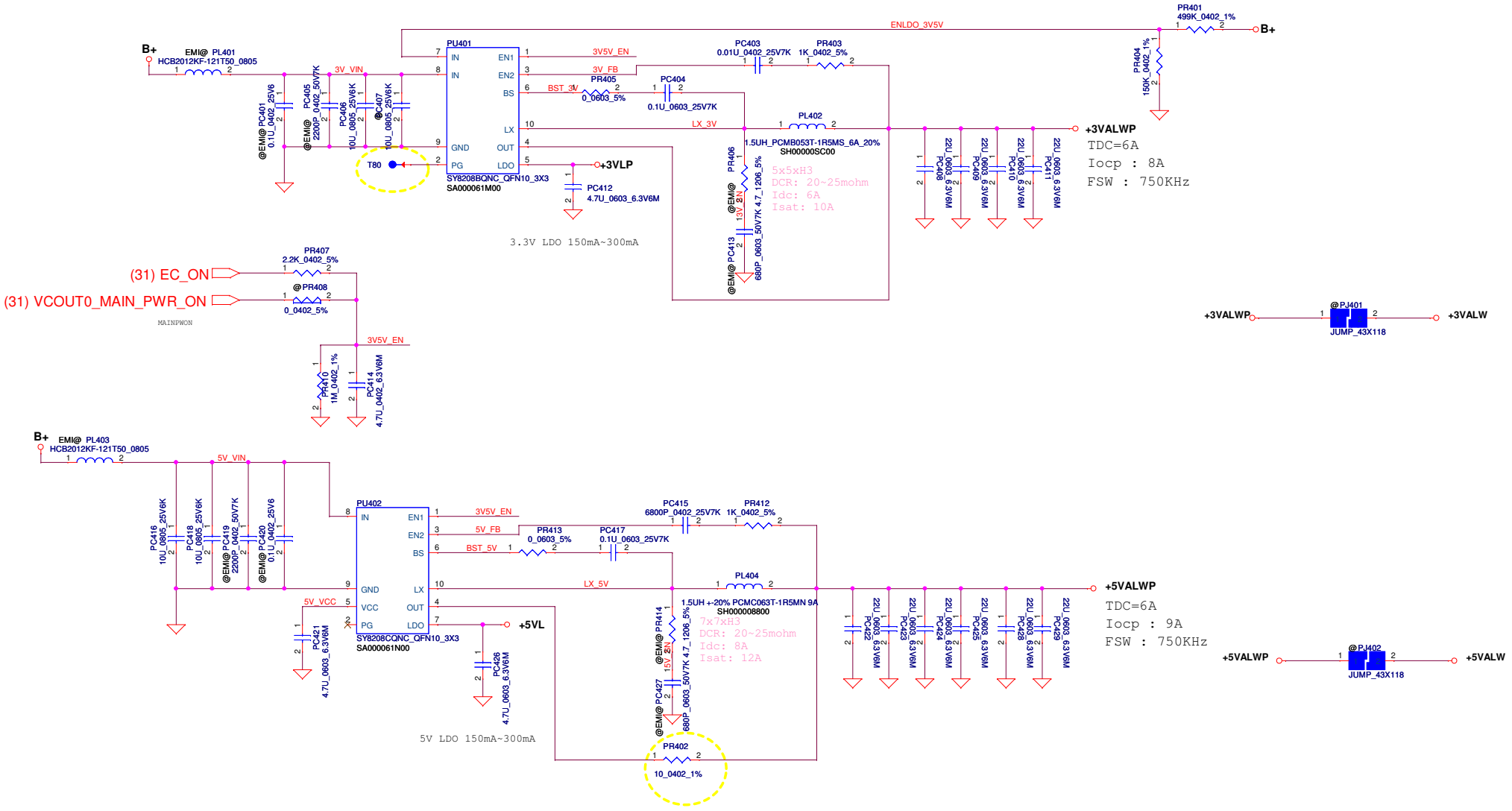

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Issued Date	2014/02/25	Deciphered Date	2015/02/25

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Compal Electronics, Inc.

Title: +3VALW/+5VALW

Size: Custom | Document Number: BE_BDW | Rev: 1.0

Date: Tuesday, February 25, 2014 | Sheet 49 of 59

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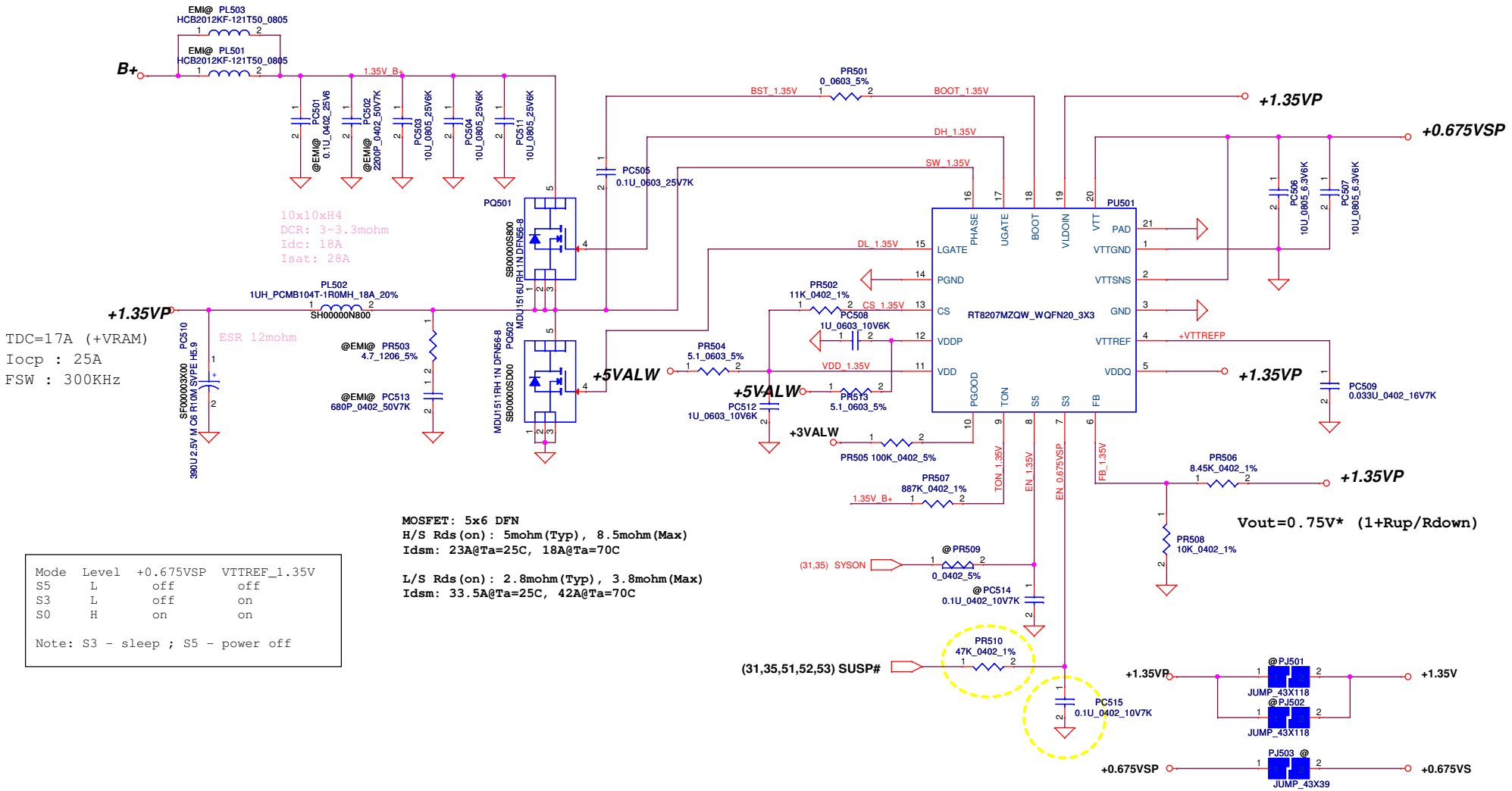

MOSFET: 5x6 DFN
H/S Rds(on): 5mohm(Typ), 8.5mohm(Max)
Idsm: 23A@Ta=25C, 18A@Ta=70C

L/S Rds(on): 2.8mohm(Typ), 3.8mohm(Max)
Idsm: 33.5A@Ta=25C, 42A@Ta=70C

Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

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Issued Date	2014/02/25	Deciphered Date	2015/02/25

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Compal Electronics, Inc.

Title: RT8207M

Size: Custom | Document Number: BE_BDW | Rev: 1.0

Date: Tuesday, February 25, 2014 | Sheet 50 of 59

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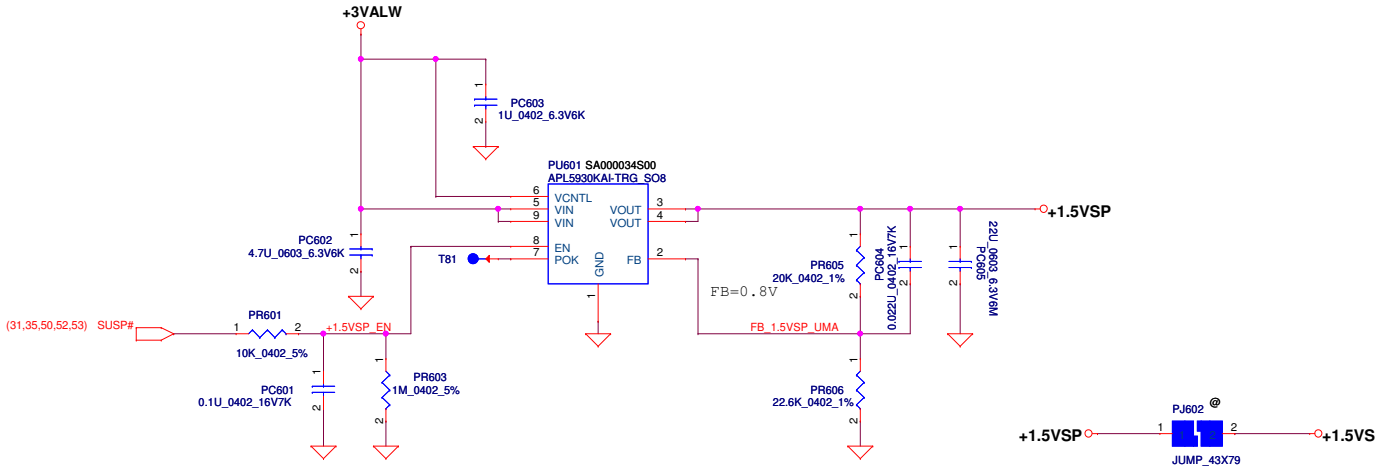

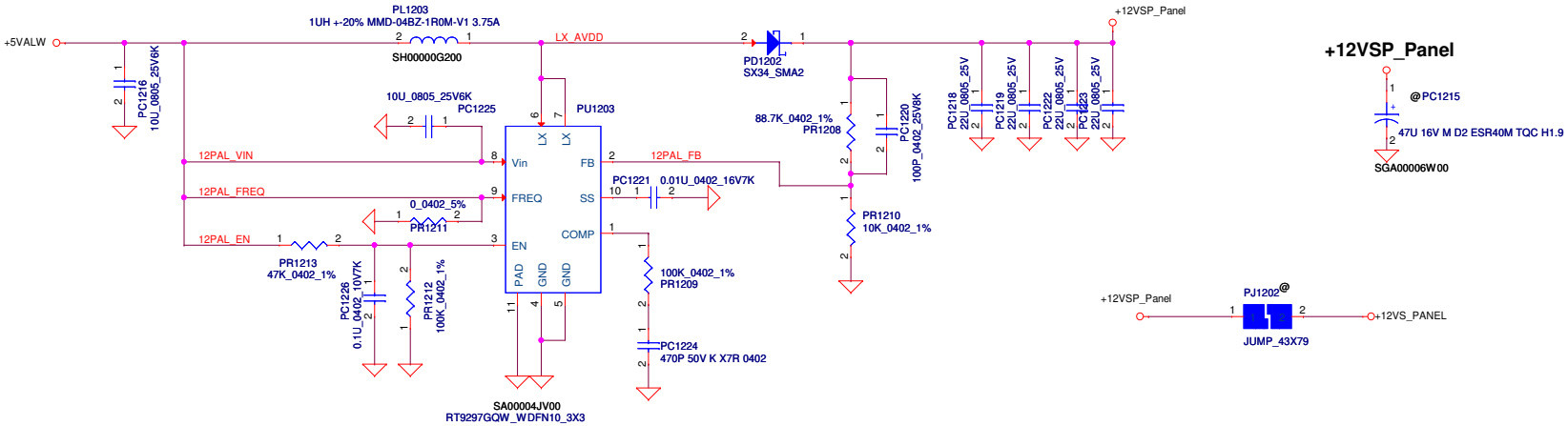

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2014/02/25	Deciphered Date	2015/02/25	Title: +1.5VS
				Size: Custom; Document Number: BE_BDW; Rev: 1.0
				Date: Tuesday, February 25, 2014; Sheet 51 of 59

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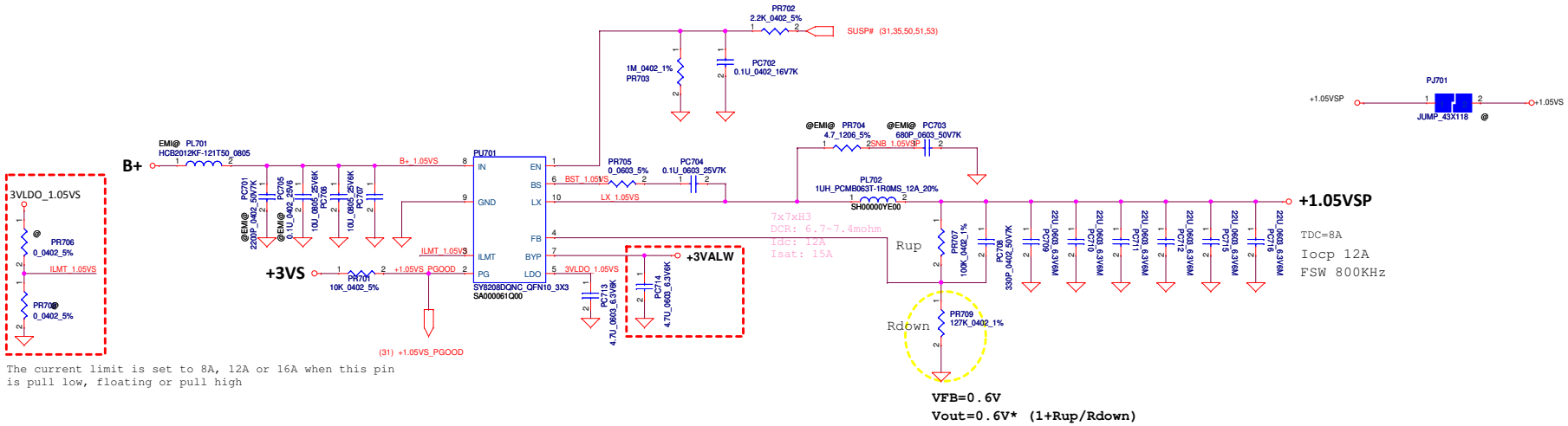

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Issued Date	2014/02/25	Deciphered Date	2015/02/25

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Compal Electronics, Inc.

Title: **+1.05VS**

Size: C | Document Number: BE_BDW | Rev: 1.0

Date: Tuesday, February 25, 2014 | Sheet 52 of 59

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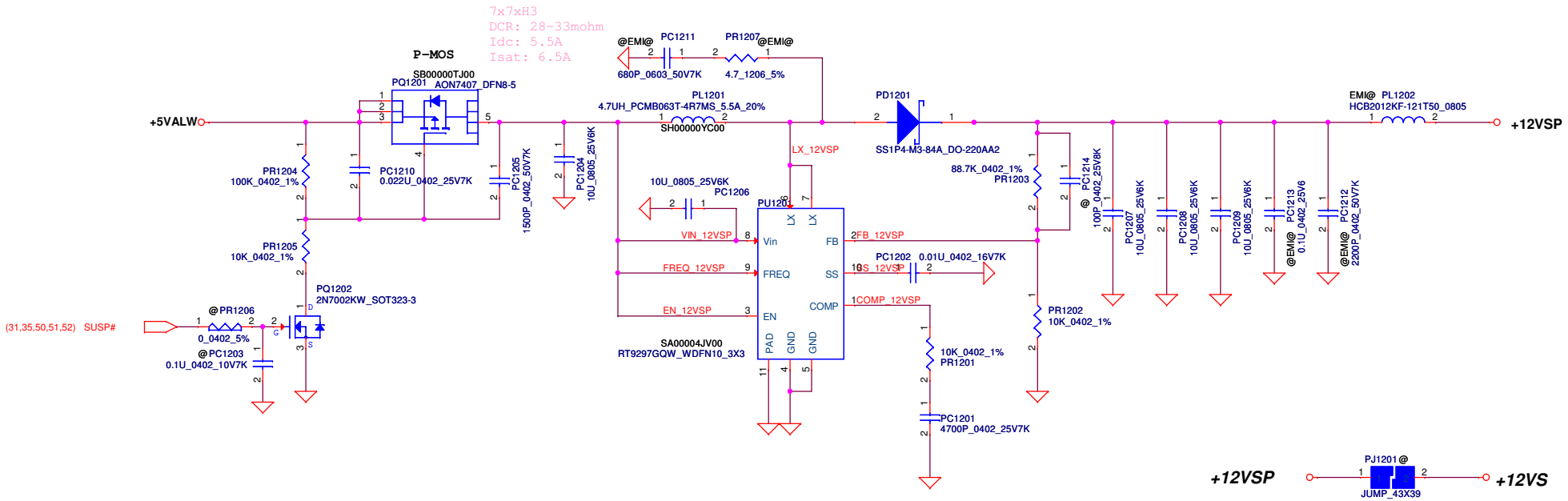

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Issued Date	2014/02/25	Deciphered Date	

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Compal Electronics, Inc.

Title: **+12V-Boost**

Size	Document Number	Rev
A3	VPUAE	1.0

Date: Tuesday, February 25, 2014 Sheet 53 of 59

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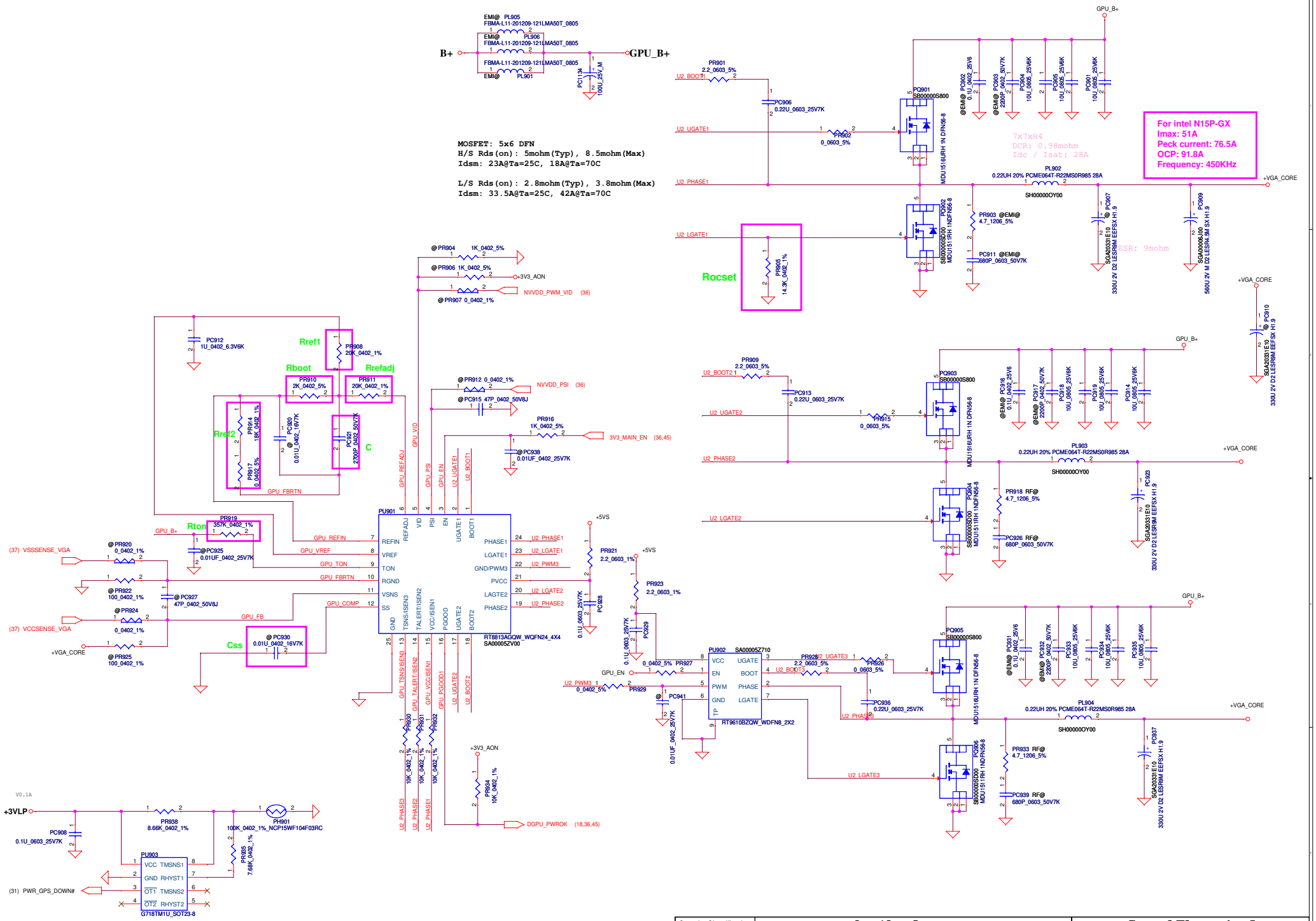

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Issued Date	2014/02/25	Deciphered Date	2015/02/25

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Compal Electronics, Inc.

Title: RT8813

Size | Document Number | Rev 1.0

Date: Tuesday, February 25, 2014 | Sheet 54 of 59

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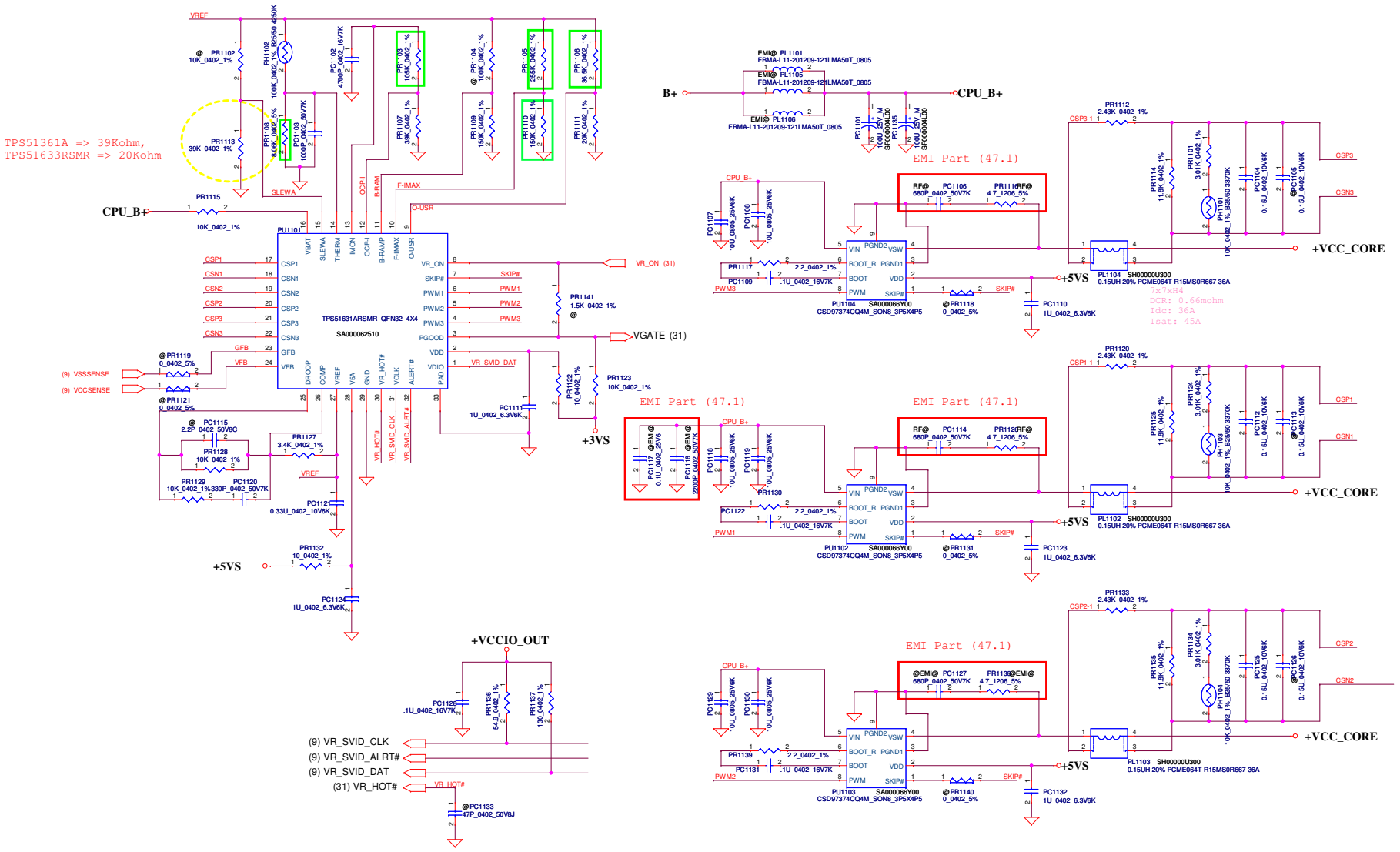

For intel SB 47W
TDC: 33A
Support Turbo: 95A
OCP setting: 114A
Frequency: 1MHz
DC_LL: -1.5mV/A

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2014/02/25	Deciphered Date	2015/02/25	Title: CPU_CORE-47W
				Size: Custom; Document Number: ; Rev: 1.0
				Date: ; Sheet 55 of 59

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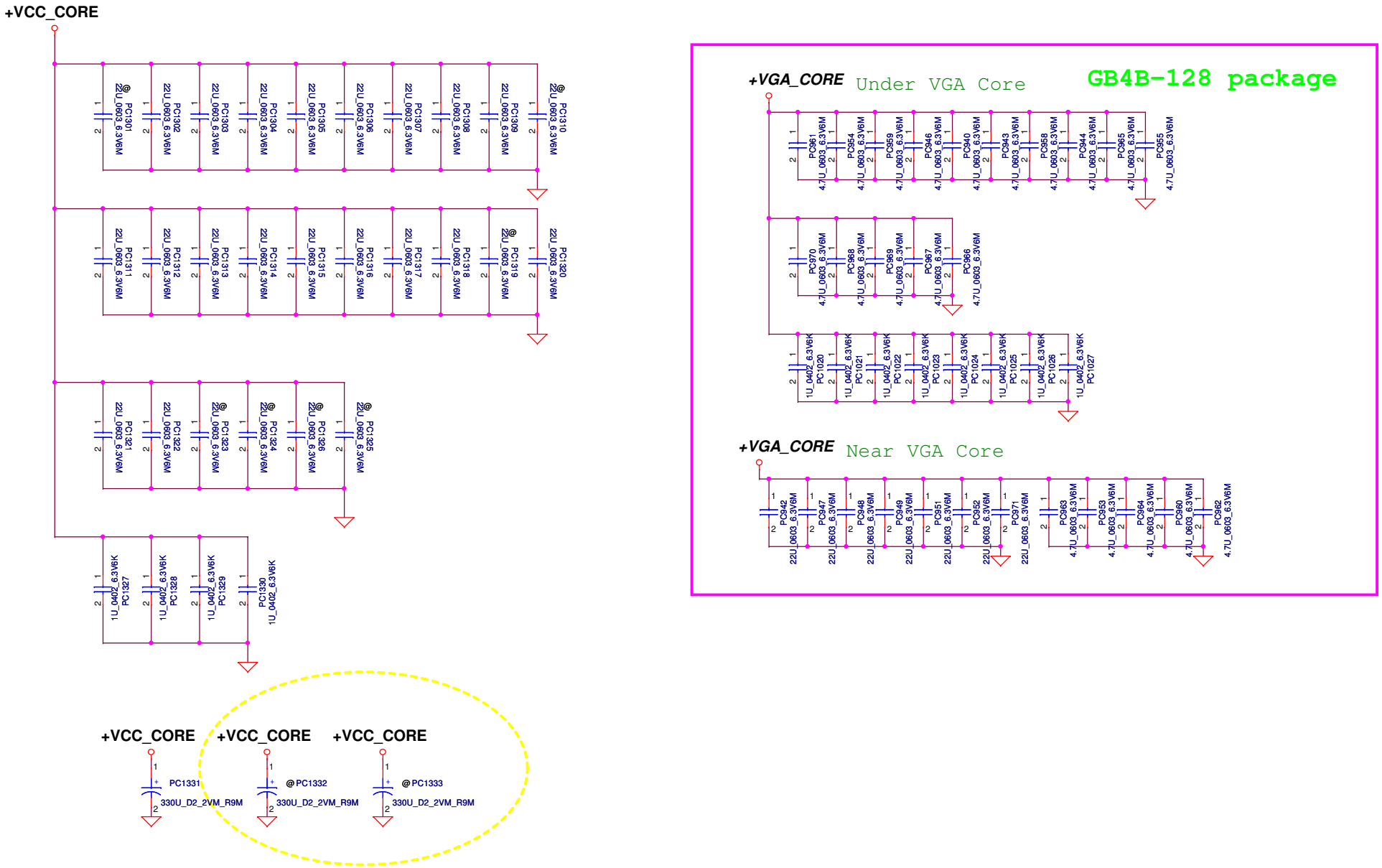

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Issued Date	2014/02/25	Deciphered Date	2015/02/25

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Compal Electronics, Inc.

Title: **PWR-PROCESSOR DECOUPLING**

Size: Custom | Document Number: **BE_BDW** | Rev: 1.0

Date: Tuesday, February 25, 2014 | Sheet 56 of 59

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Version change list (P.I.R. List)

for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1	for panel Vdrop	51	add boost solution	11/15	SIV
2	for EMI request	48	PR319, PC320 change to mount	11/15	SIV
3	for RF request	54	PR918, PC926, PR933, PC939 change to mount	11/18	SIV
4	for RF request	55	PC1114, PR1126, PC1106, PR1116 change to mount	11/18	SIV
6	battery can't be remove	47	del PR222, PR227, PC204, PR220, PU202, PC206, PR226, PD201, PC205, PR218, PR219, PQ201, PQ205, PR228	12/30	SIT
7	for acoustic noise	55, 56	add PC1135, 1332	12/30	SIT
8	SIV rework	48	PR309 is changed from 392K_0402_1% to 124K_0402_1% (SD034124380) PR312 is changed from 59K_0402_1% to 20K_0402_1% (SD034200280) Add a resistor 249K_0402_1% (SD034249380) between pin 6 of PU301 and PACIN. PC312 is changed from 2200pF_0402_25V_X7R to 0.01uF_0402_25V_X7R (SE075103K80) PQ302 change to AO4447A	12/30	SIT
9	SIV rework	47	PR217 change to 30K PR221 change to 110k	12/30	SIT
10	for HW request	50	PR506 change to SD000000680 8.45K 1%	12/30	SIT
11	accuracy modify	52	PR707 change to 100K +-1% PR709 change to 127K +-1%	1/20	SVT
15					
16					
17					

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Security Classification	Compal Secret Data		
Issued Date	2014/02/25	Deciphered Date	2015/02/25

Compal Electronics, Inc.

Title: PIR (PWR)

Size: Custom | Document Number: BE_BDW | Rev: 1.0

Date: Tuesday, February 25, 2014 | Sheet 57 of 59

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase	Verify

1		Add 3D Camera function	0.2	23
				22
					Add U25,C502~C511.
					Add R386~R400,R550~R559.
					Del Q14,R205,C319
					Add U13
						10/30	SIV	SIV Phase

2		Remove LPF for woofer amplifier	0.2	27	Change R224->20K,R297->62K Change R1564,R1565->0 ohm,R341->15K, Change R342->20.5K,R81->200K. un-stuff C450,C443	10/30	SIV	Verified by SDV rework.
3		AC/DC detect issue	0.2	14 31	Del D1 Add AC_PRESENT_R to U18 pin 19	11/03	SIV	Verified by SDV rework.
4		Change USB power switch (follow B/E series)	0.2	30	Change U16,U17->SY6288D20AAC	11/04	SIV	Verified by SDV rework.
5		Add resistor for 15"/17" K/B co-lay	0.2	31	Add R1001~R1012,R1021~R1032	11/04	SIV	SIV Phase
6		Cancel 3D Camera function	0.3	23 22	Del U25,C502~C508 Del R387~R400,R550~R557. Del R255,R256,R261,R262,L41,L42,D21. Del R204,R386,R558,R559	12/17	SIT	SIT Phase
7		TP lock LED function	0.3	31	TP_LOCK_LED# from U18_pin34 to LED	12/24	SIT	Verified by SIV rework.
8		KB Backight behavior	0.3	32	Add R337,R335,C434,Q23	12/24	SIT	Verified by SIV rework.
9		Improve VRAM +1.35V	0.3	39	C790 stuff 330uf	12/25	SIT	Verified by SIV rework.
10		Hole size change for Thermal bracket.	1.0	34	H1,H2,H3,H4,H5,H6 : change to 4.2 mm.	2/5	SVT	Verified by SIT rework.
11		ESD reserve	1.0	32	Reserve C479,C480.	2/5	SVT	SVT Phase
12								
13								
14								
15								
16								
17								
18								
19								
20								

Security Classification: Compal Secret Data
Issued Date: 2014/02/25 Deciphered Date: 2015/02/25
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Compal Electronics, Inc.
Title: PIR-HW
Size: Custom | Document Number: LA-B111P | Rev: 1.0
Date: Tuesday, February 25, 2014 | Sheet 58 of 59

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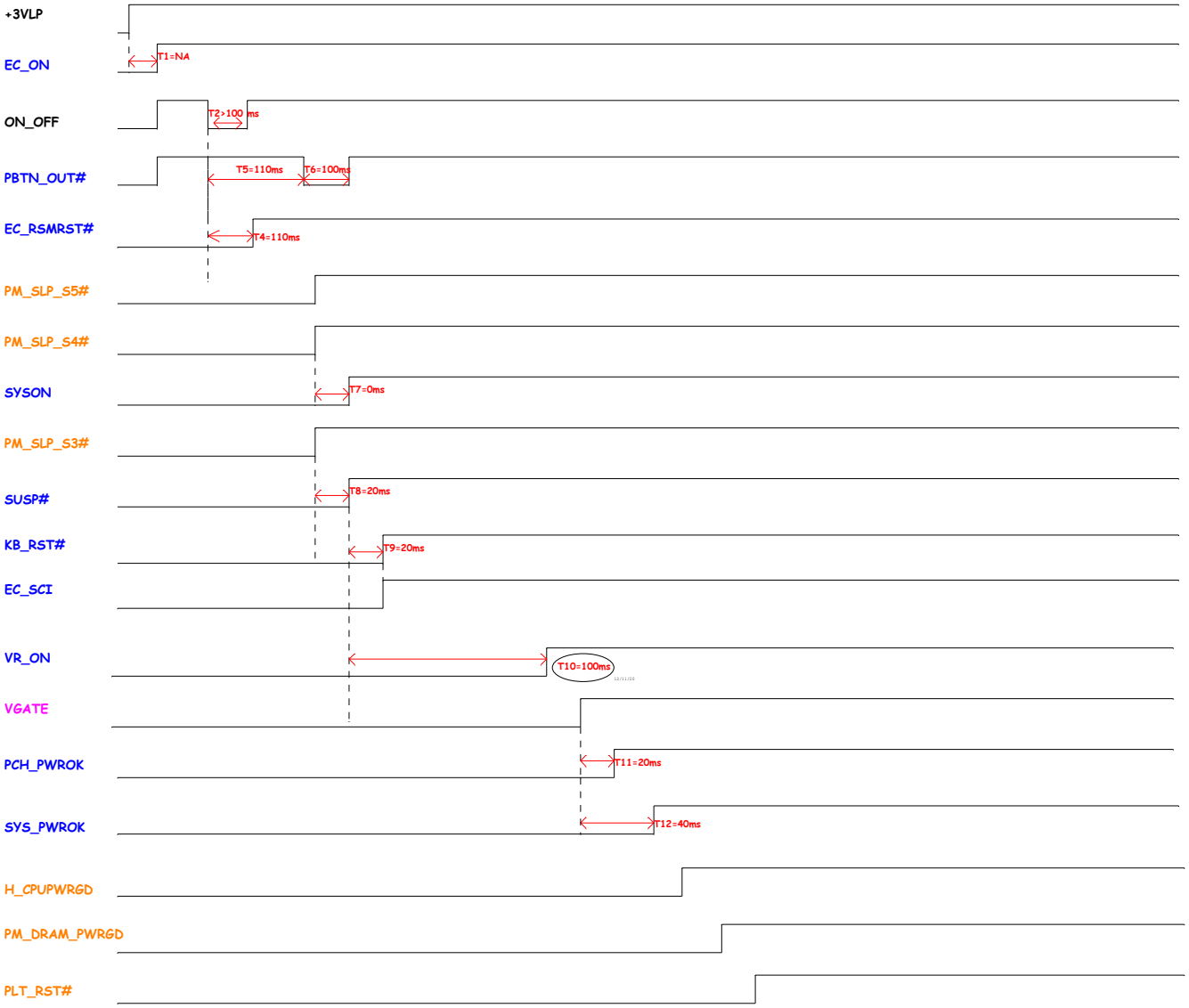
Timing Diagram for G3 or S4-5/M-off (Suspend Well Off) to S0/M0 [non Deep S4/S5 Platform]



Color	Command
Signal Names	Timing of these signals is set by PCH or processor
Signal Names	Timing of these signals should be met by the platform (EC)
Signal Names	Timing of these signals is set by IntelR MVP
Signal Names	Voltage rails or chip-to-chip buses

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Issued Date	2014/02/25	Deciphered Date	2015/02/25

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Compal Electronics, Inc.

Title: Power Sequence

Size: Custom | Document Number: LA-B11IP | Rev: 1.0

Date: Tuesday, February 25, 2014 | Sheet 38 of 58

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