

The diagram illustrates the system architecture for the Arrandale 35W processor. The central components are the CPU (Arrandale 35W) and the PCH (Ibex Peak-M). The CPU is connected to the PCH via a DMI LINK (32.768KHz, 25MHz). The PCH is connected to the CPU via a PEG (PCI Express Gen 1) interface. The PCH is also connected to the CPU via a Singel Link interface.

**Memory and Storage:**

- DDRIII-SODIMM1** (PAGE 14) and **DDRIII-SODIMM2** (PAGE 15) are connected to the CPU via DDRIII (1066/1333 MT/s).
- SATA0 150MB** (PAGE 31), **SATA1 150MB** (PAGE 31), and **SATA2 150MB** (PAGE 29) are connected to the PCH via SATA.
- ATA -HDD** (PAGE 31), **ATA - CD-ROM** (PAGE 31), and **ATA - SATA** (PAGE 29) are connected to the PCH via SATA.

**Peripherals and Expansion:**

- CLOCK GEN 9LRS3197** (PAGE 3) is connected to the PCH via a 14.318MHz clock signal.
- ESATA** (PAGE 29), **WLAN** (PAGE 33), **Epress Card** (PAGE 29), and **Card Reader** (PAGE 30) are connected to the PCH via PCI-E.
- USB2.0 Ports X3** (PAGE 29), **BlueTooth** (PAGE 32), **Fingerprint** (PAGE 32), and **Camera** (PAGE 23) are connected to the PCH via USB2.0.
- Mini PCI-E Card** (PAGE 33), **Epress Card** (PAGE 29), and **LAN** (PAGE 28) are connected to the PCH via PCI-E.
- RJ45** (PAGE 28) is connected to the PCH via LAN.
- MDC CONN** (PAGE 29) is connected to the PCH via Azalia.
- Audio Codec** (PAGE 25) is connected to the PCH via Azalia.
- EXT-MIC** (PAGE 26), **Speaker** (PAGE 26), **HeadPhone** (PAGE 26), and **D-MIC** (PAGE 23) are connected to the PCH via Azalia.

**Other Components:**

- Accelerometer Sensor** (PAGE 31) is connected to the PCH via SMBUS.
- SMSC KBC 1098** (PAGE 27) is connected to the PCH via LPC and SPI.
- PWM FAN** (PAGE 31) and **SPI ROM** (PAGE 27) are connected to the PCH via SMBUS.

32.768KHz

**Keyboard Conn.**  
PAGE 32

**Touch Pad**  
PAGE 32

**SMSC KBC**  
**1098**  
PAGE 27

**PWM FAN**  
PAGE 31

**SPI ROM**  
PAGE 27

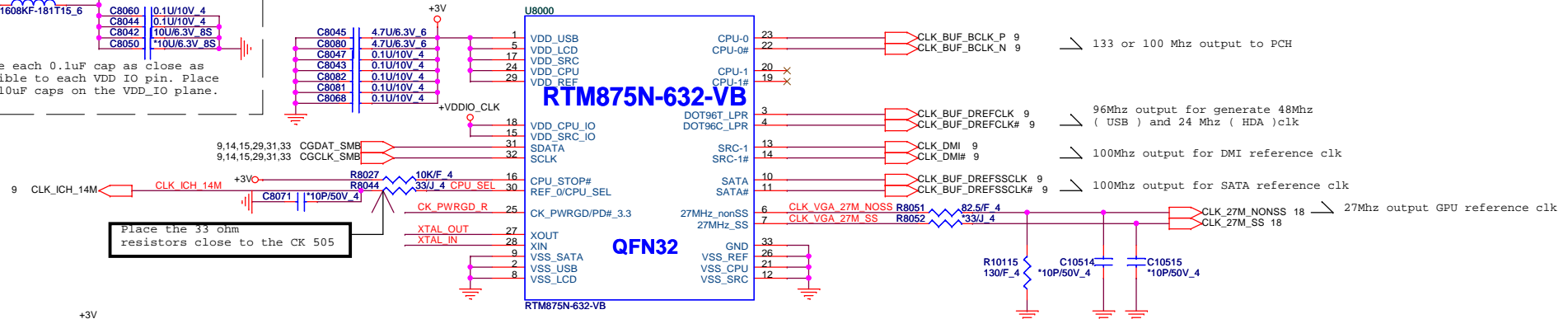
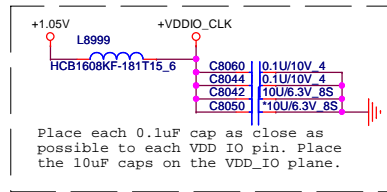
power State	+RTC_CELL	+VIN +3VPCU	+3VS5 +5VS5	+5VSUS +1.5VSUS	+5V +3V +1.8V_GFX +1.8V +1.5V +1.5V_CPU +1.1V_VTT +1.05V +1.0V_GFX +VGA_CORE +VCORE
S0	ON	ON	ON	ON	ON
S1	ON	ON	ON	ON	ON
S3	ON	ON	ON	ON	OFF
S4/S5 AC	ON	ON	ON	OFF	OFF
S4/S5 DC Only	ON	ON	OFF	OFF	OFF
AC/DC No Exist	ON	OFF	OFF	OFF	OFF

	SOURCE	BATTERY 0x16	CLK GEN 0xD2	Thermal IC 0x98(Write) / 0x99(Read)	G-SENSOR 0x3A(Write) /0x3B(Read)	WLAN	SO-DIMM DIMM0: 0xA0 DIMM1: 0xA2	SMSC 1098	GPU thermal sensor
SMBCLK SMBDATA	PCH	X	Y	Y	Y	Y	Y	X	X
SMB_CLK_ME1 SMB_DAT_ME1	PCH	X	X	X	X	X	X	Y	Y
AB1A_CLK AB1A_DATA	SMSC 1098	Y	X	X	X	X	X	X	X

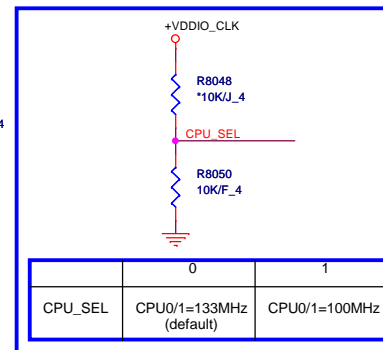
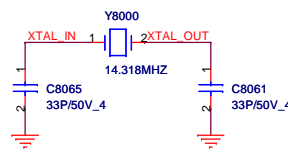
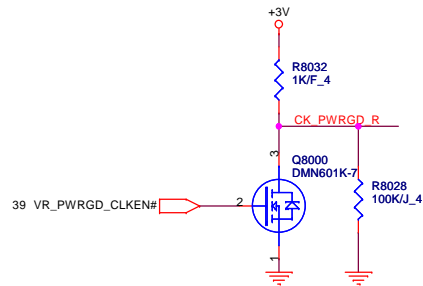


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Size Custom	Document Number <b>power rails</b>	Rev 2B
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AL000875002IC OTHER(32P) RTM875N-632-VB-GRT(QFN)Realtek  
 AL8SP585000IC OTHER(32P)SLG8SP585VTR(QFN)Silego

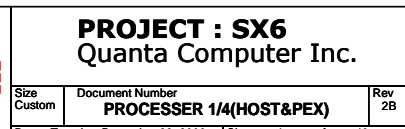


**PROJECT : SX6**  
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Size Custom	Document Number <b>CLOCK GEN (9LRS3197)</b>	Rev 2B
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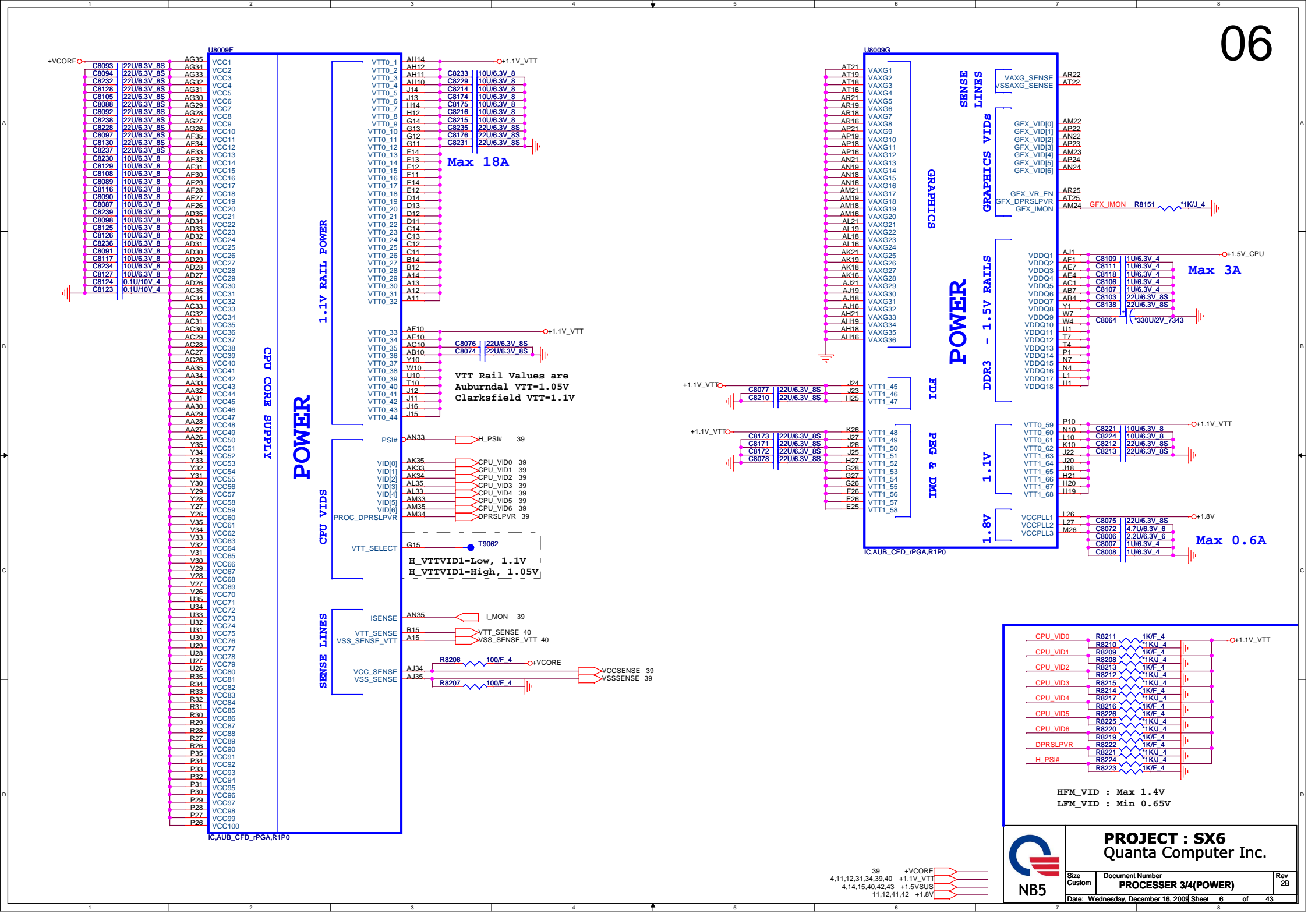
4,8,9,10,11,12,14,15,16,20,23,25,27,28,29,30,31,32,33,34,35,37,39,42

+3V



## AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



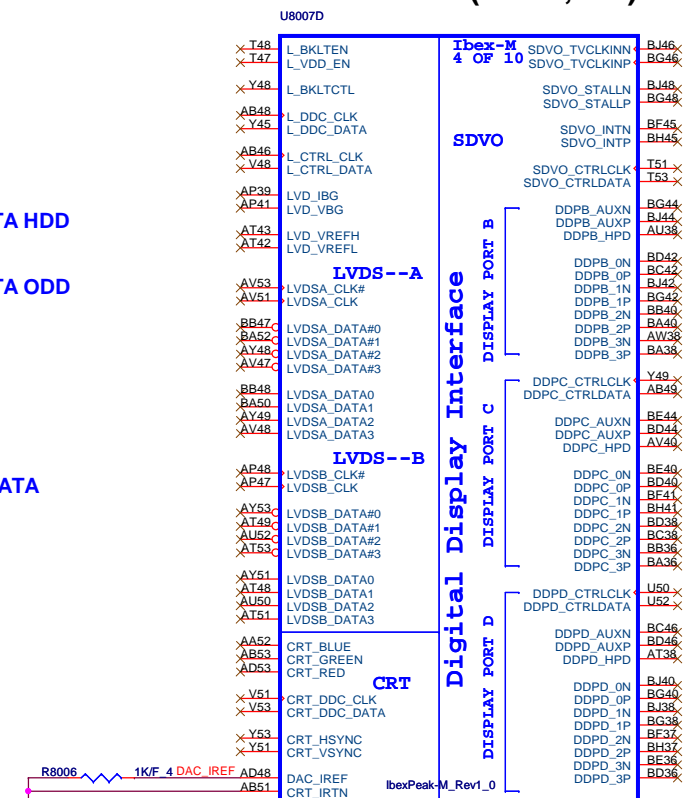
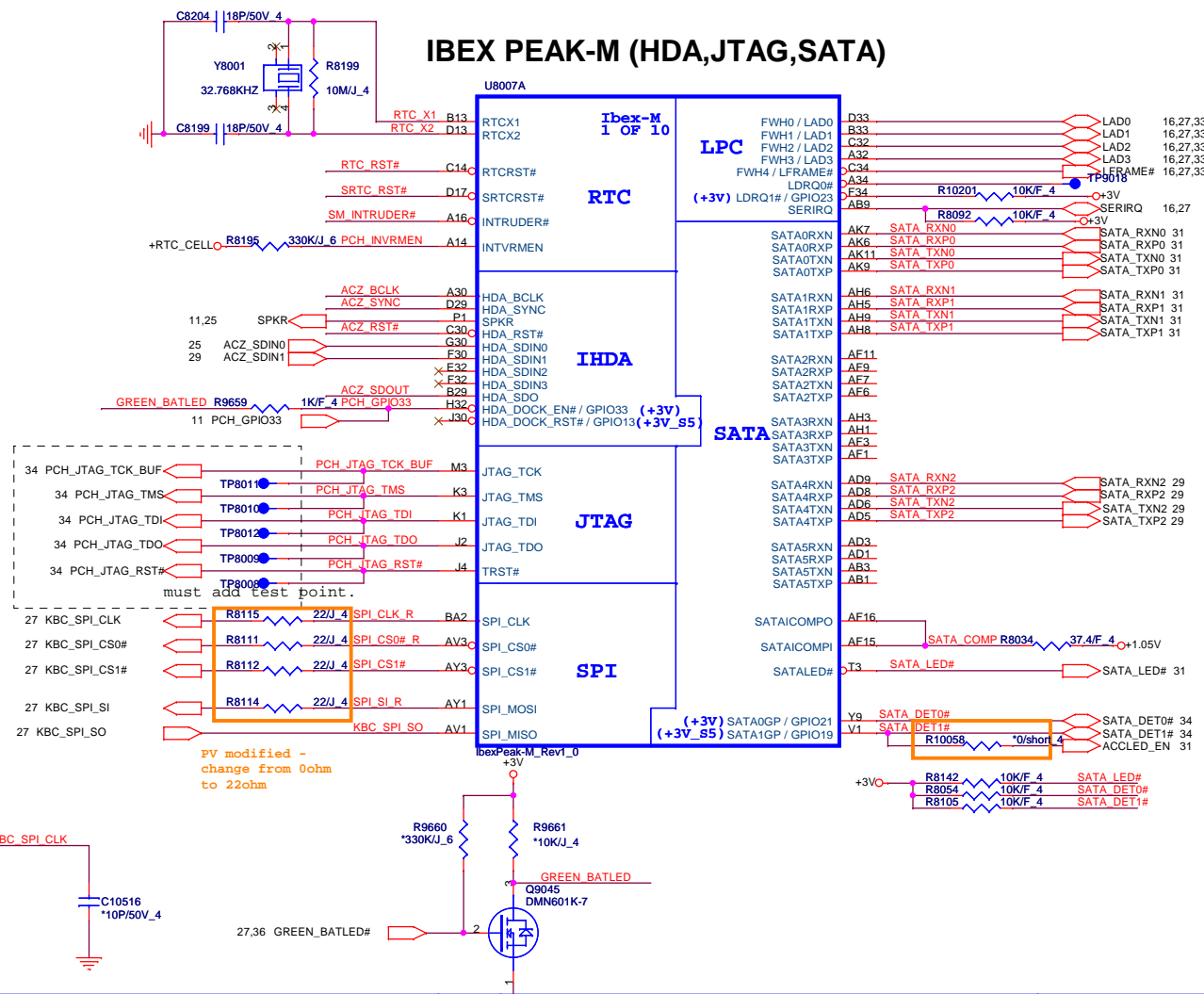




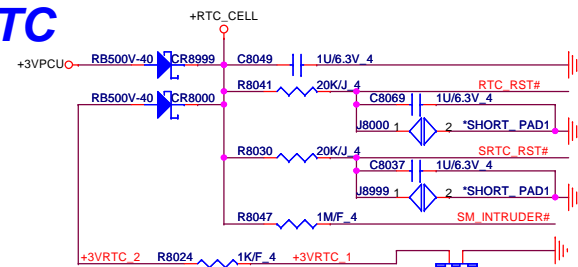


Size Custom	Document Number <b>PROCESSER 4/4(GND)</b>	Re 2
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## IBEX PEAK-M (LVDS,DDI)



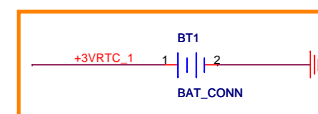
**RTC**

DFWF02MS022  
SI change p/n

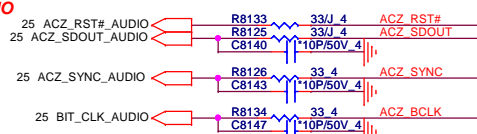
CN7042  
\*85205-0200L

change p/n 3,9,10,12,34,39,41 +1.05V  
3,4,9,10,11,12,14,15,16,20,23,25,27,28,29,30,31,32,33,34,35,37,39,42 +3V  
10,23,25,27,31,32,36,37,38 +3V/PC

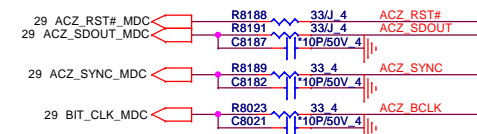
PV modified -



**For AUDIO**



**For MDC**



**PROJECT : SX6**  
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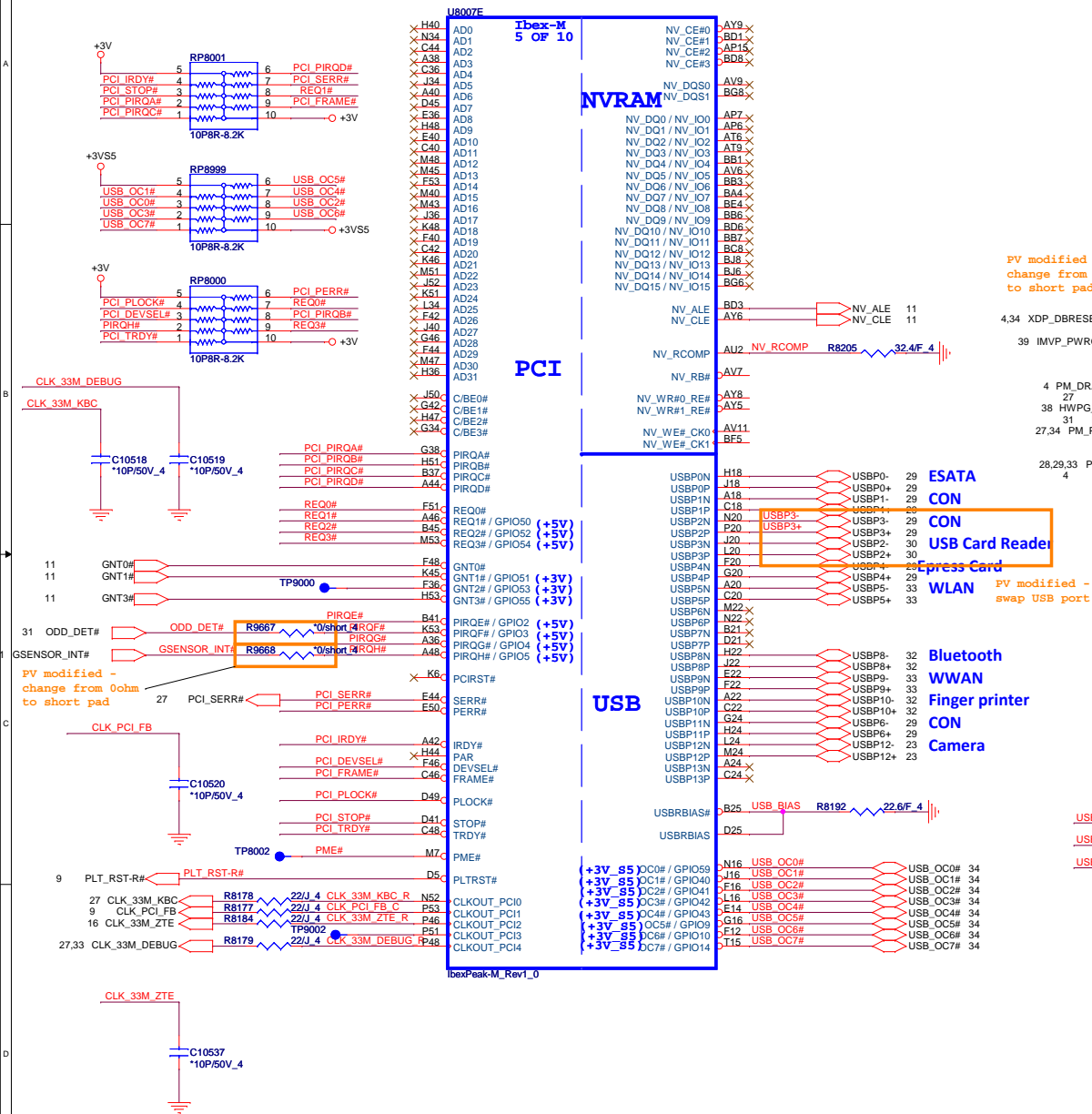
Size Custom	Document Number <b>PCH 2/6 (SATA,HDA,LPC)</b>	Rev 2B
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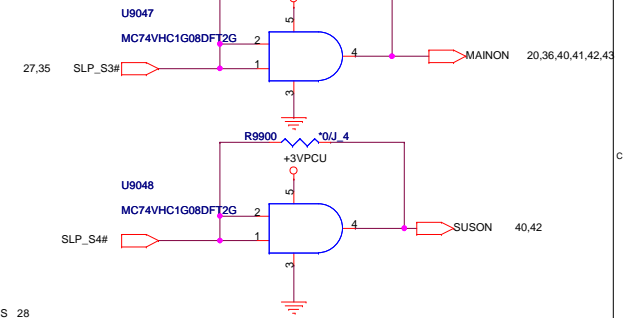
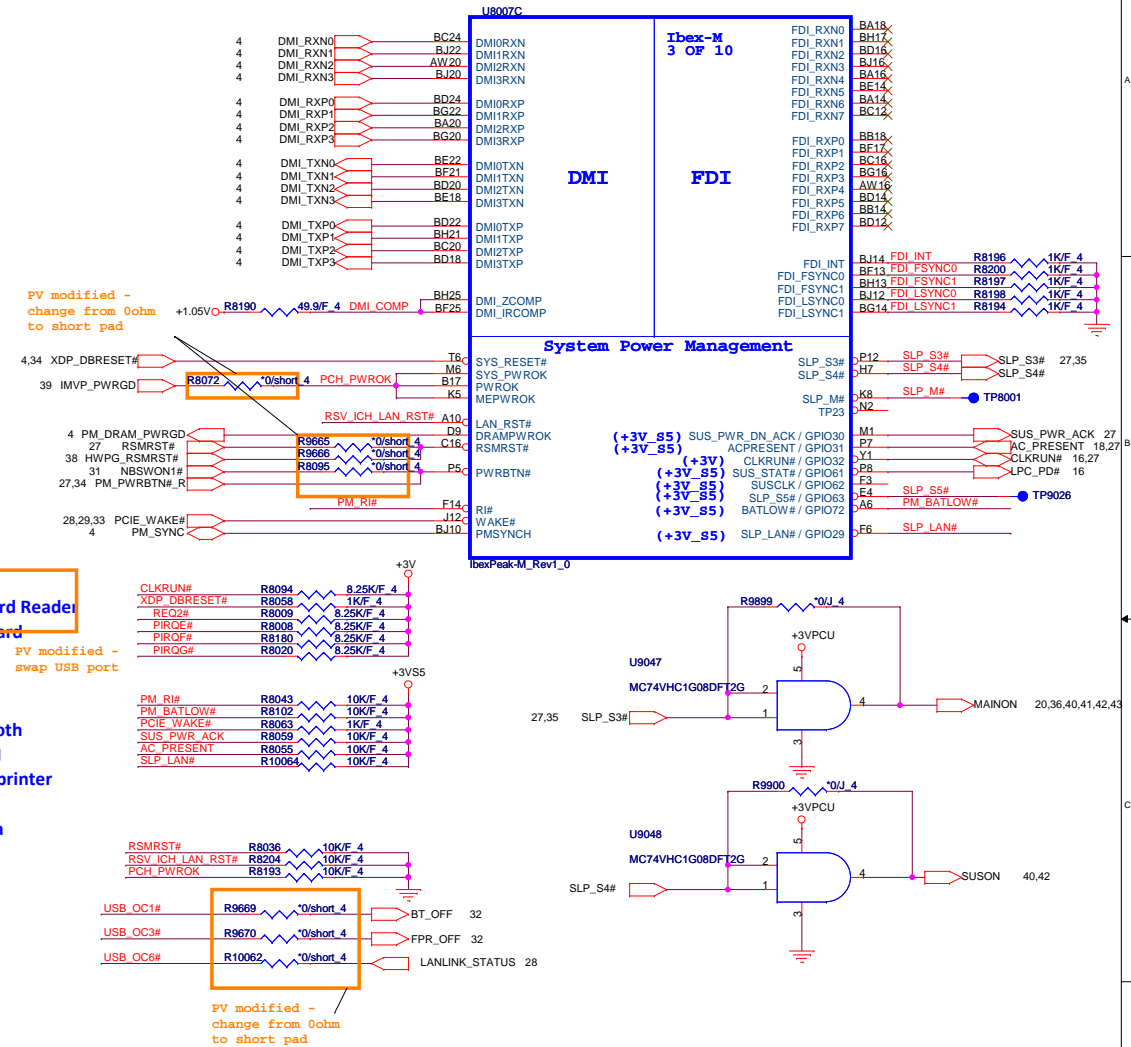
## 09



## IBEX PEAK-M (PCI,USB,NVRAM)

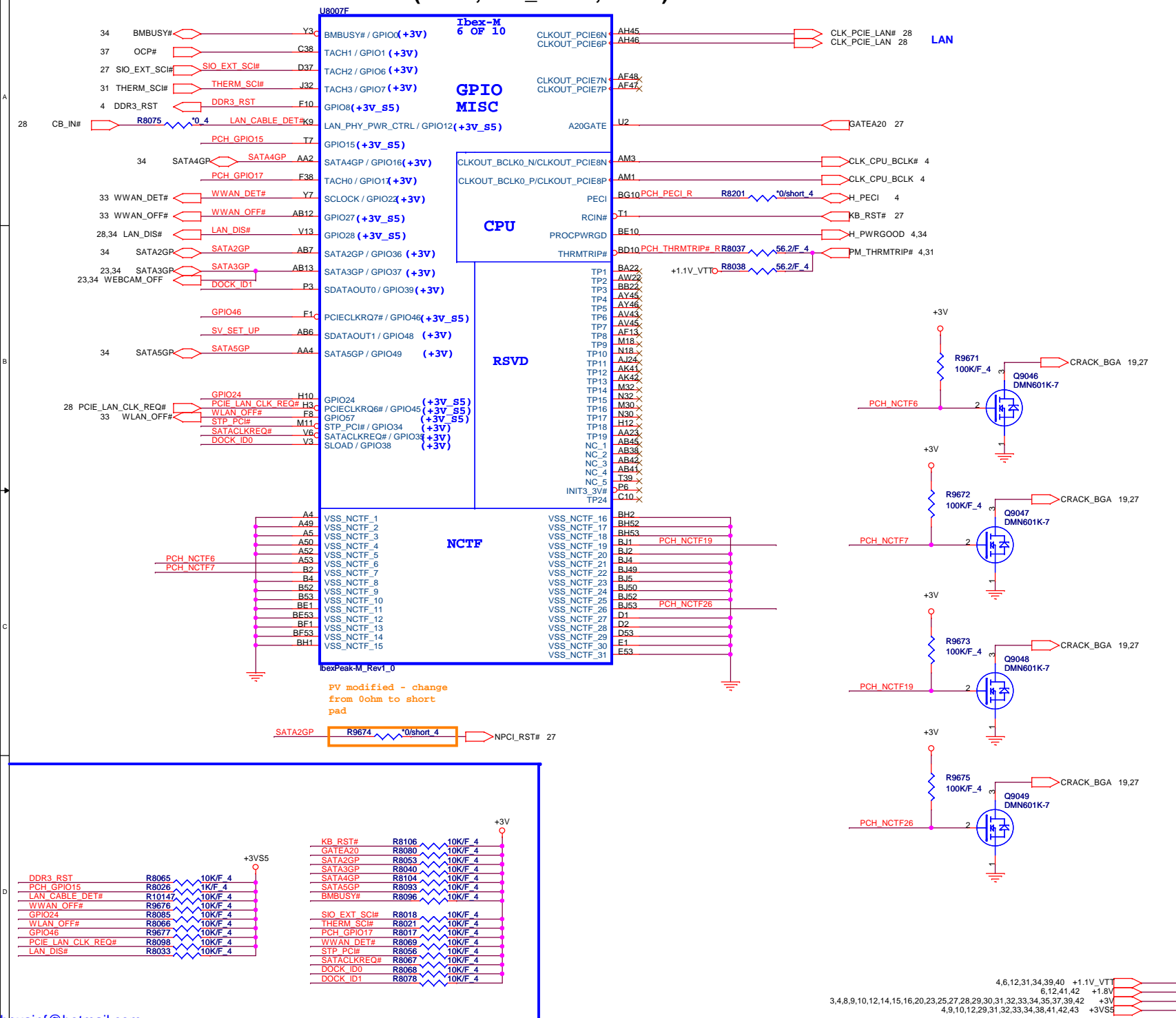


## IBEX PEAK-M (DMI,FDI,GPIO)



# IBEX PEAK-M (GPIO,VSS\_NCTF,RSVD)

11



**Al6 swap override Strap/Top-Block Swap Override jumper**

Low = Al6 swap override/Top-Block Swap Override enabled  
High = Default

**SV SET UP**

1-X High = Strong (Default)

**Boot BIOS Strap**

PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

**Danbury Technology Enabled**

NV\_ALE High = Enable  
Low = Disable

**DMI Termination Voltage**

NV\_CLE Set to Vcc when LOW  
Set to Vcc/2 when HIGH

**No Reboot Strap**

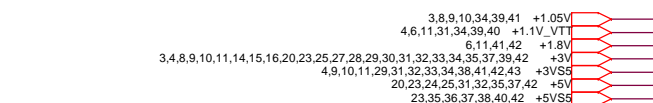
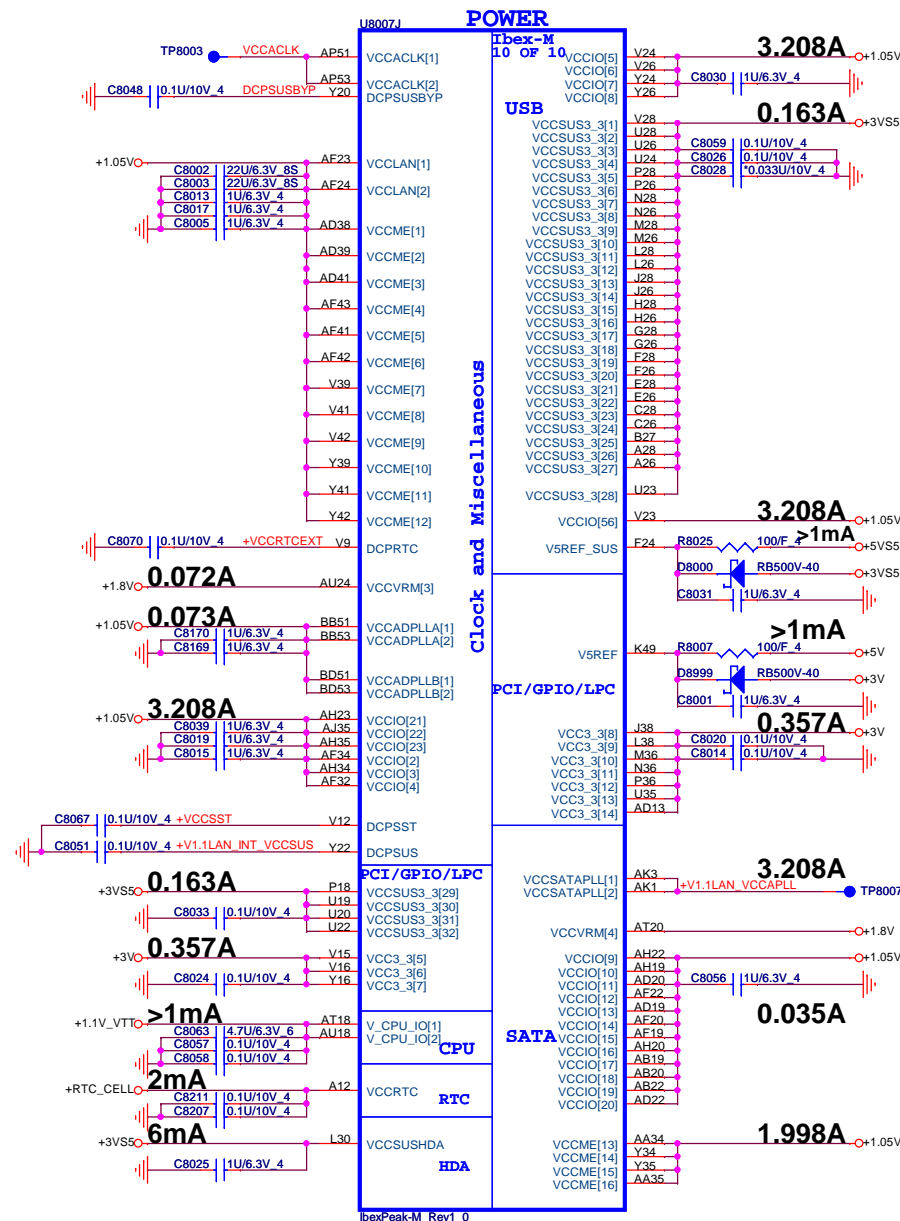
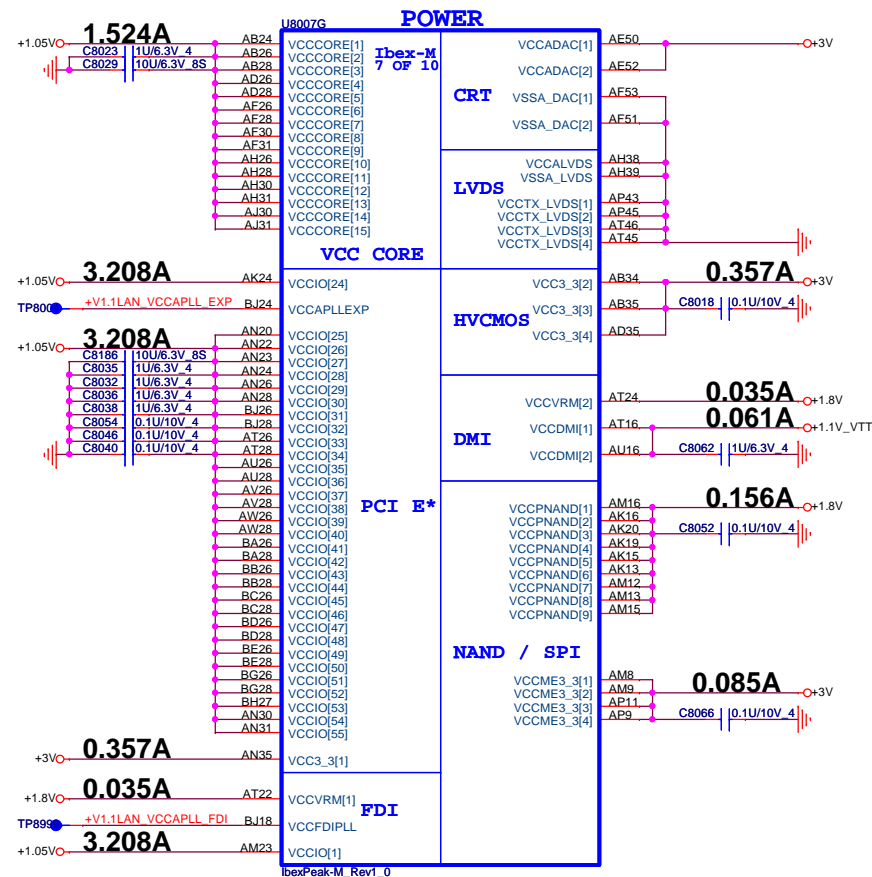
SPKR R8132 \*1K/J 4 +3V

PCH\_GPIO33 R8022 \*100K/J 4

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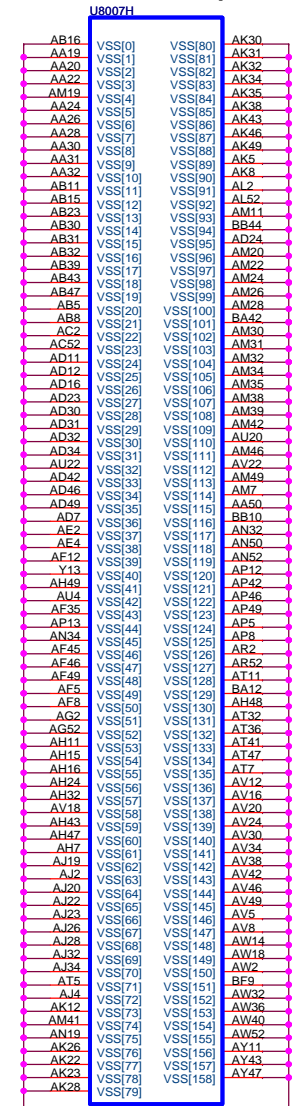
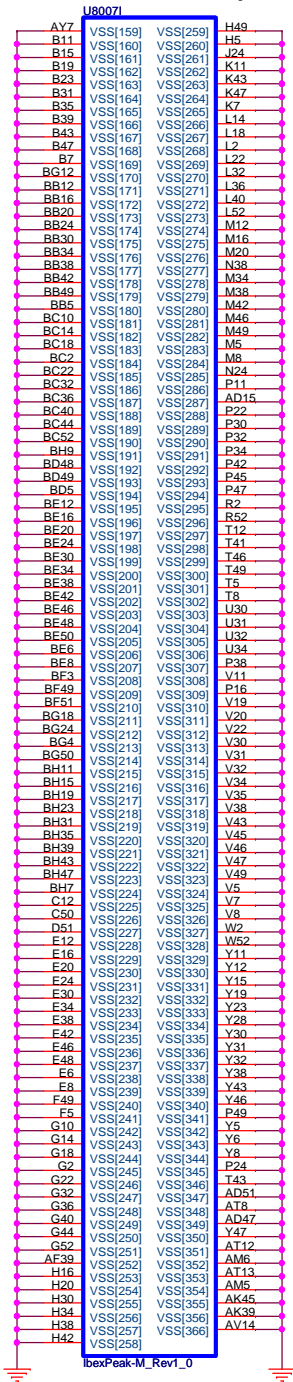
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Document Number  
**PCH 4/6 (GPIO & Strap)**  
Rev 2B

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# IBEX PEAK-M (GND)

# IBEX PEAK-M (GND)



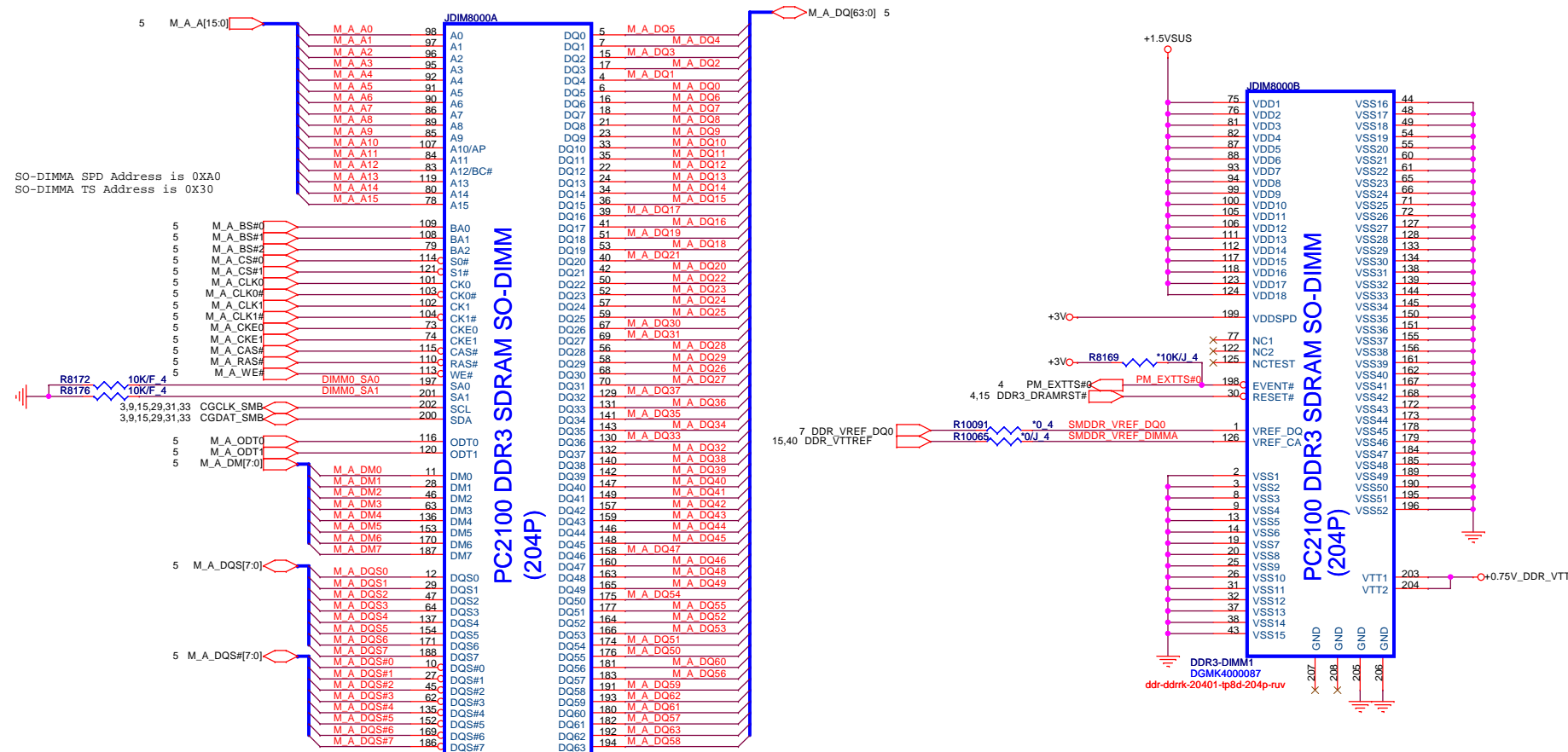
ibexPeak-M\_Rev1\_0



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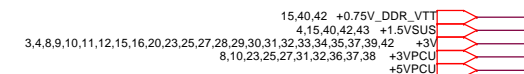
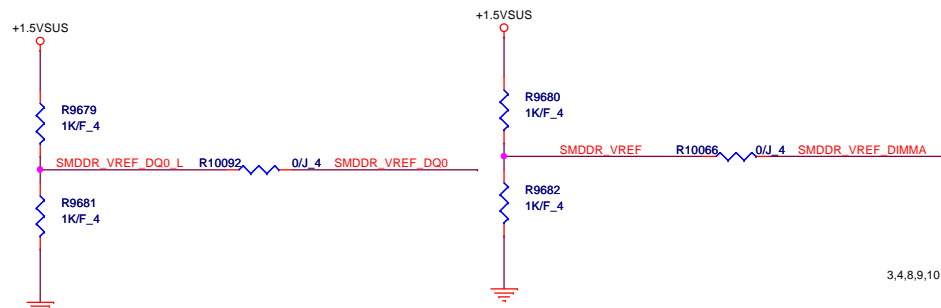
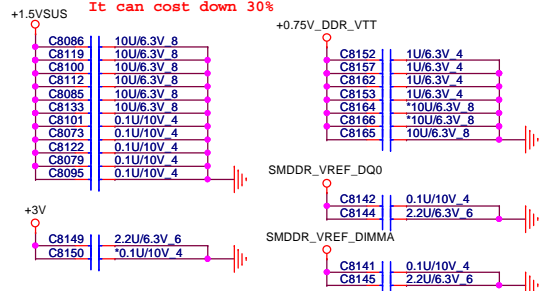
Size Custom	Document Number <b>PCH 6/6 (GND)</b>	Rev 2B
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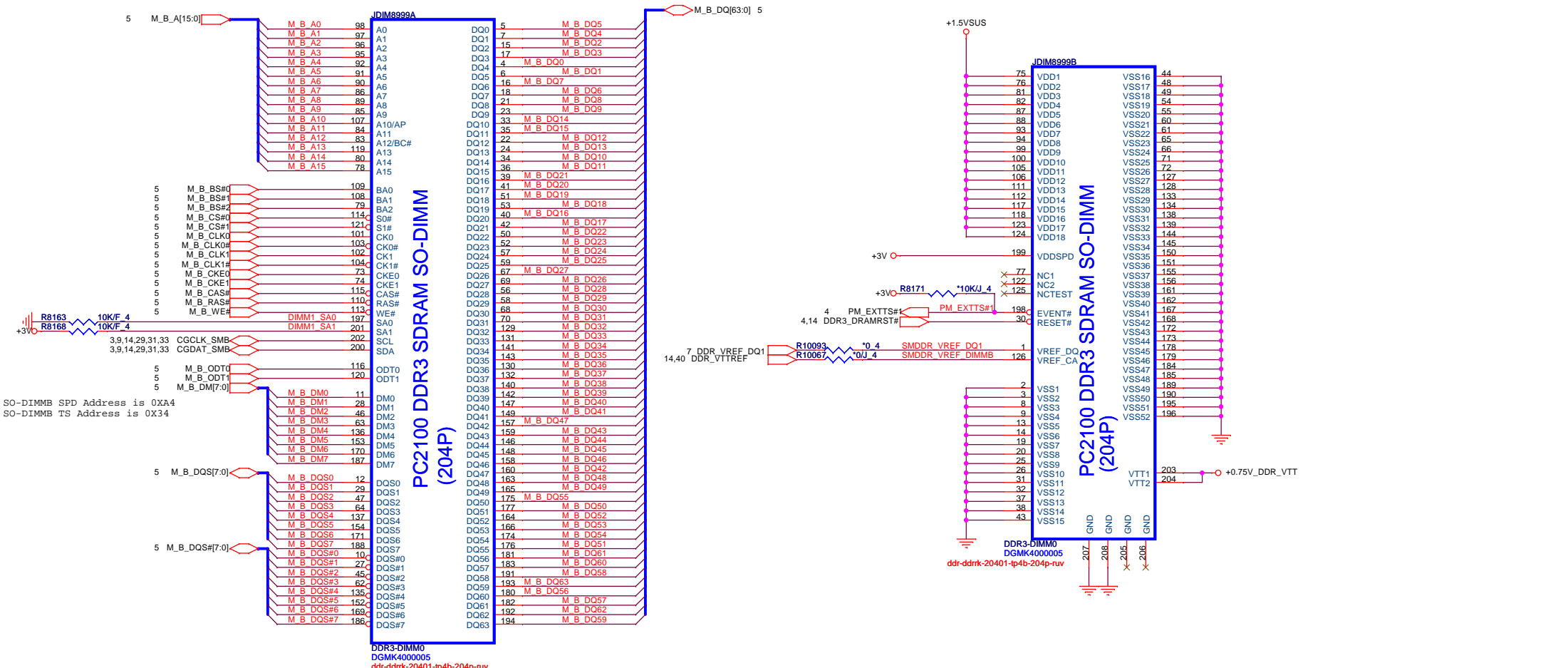


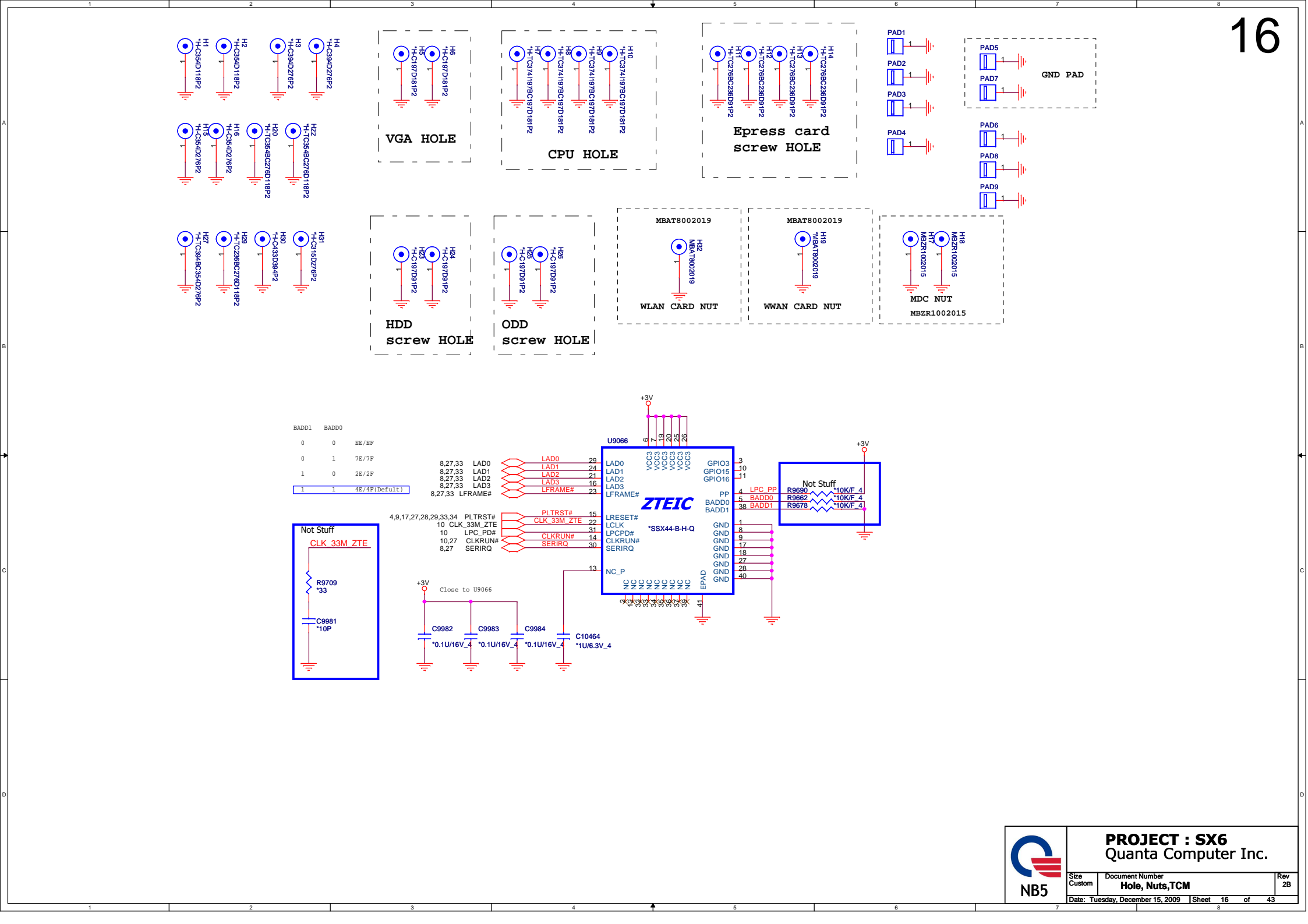
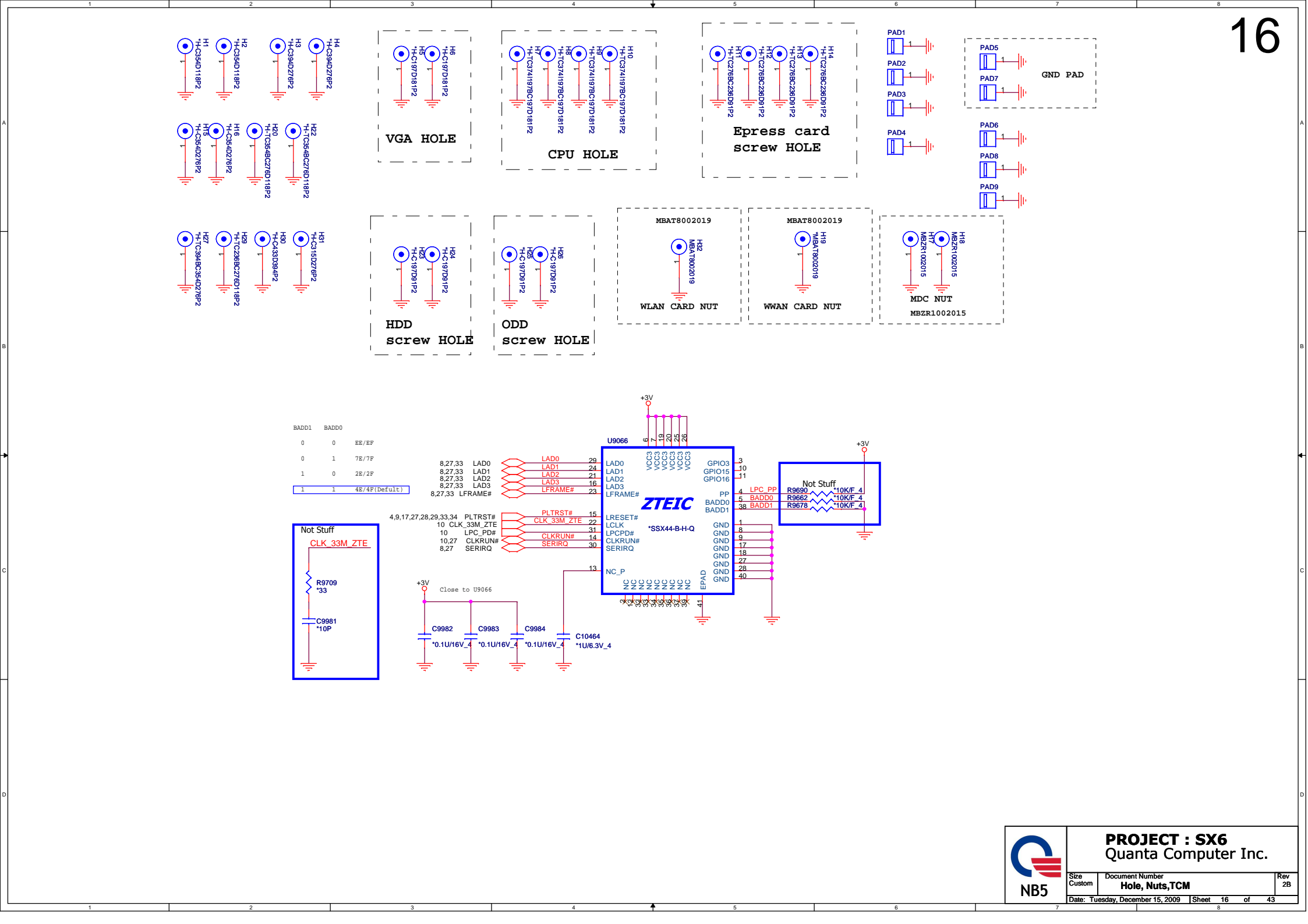
***Place these Caps near So-Dimm0.***

Some Projects replace 10UF 0805 by 4.7UF 0603 11/6  
It can cost down 30%

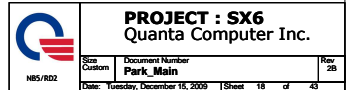


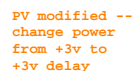








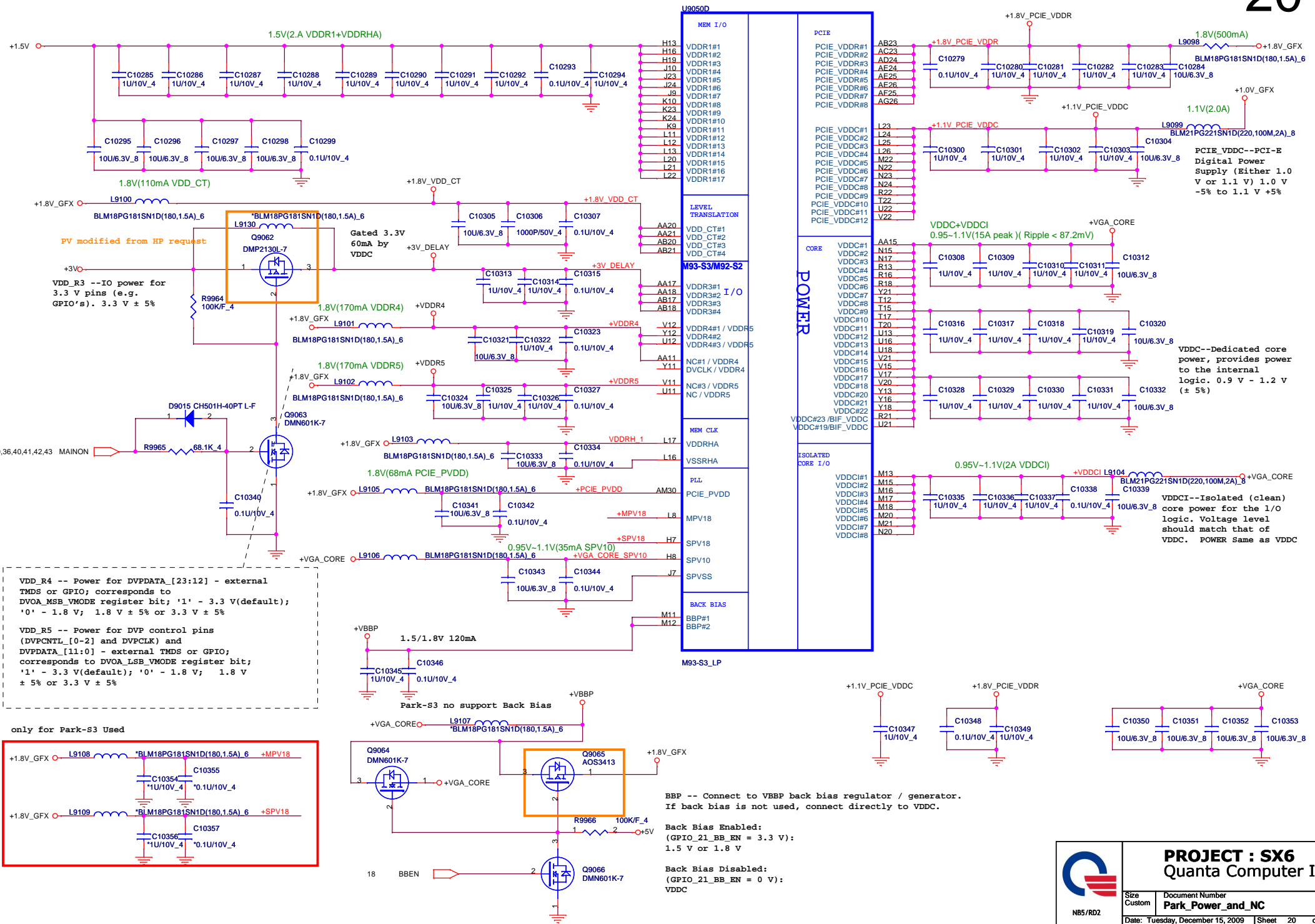




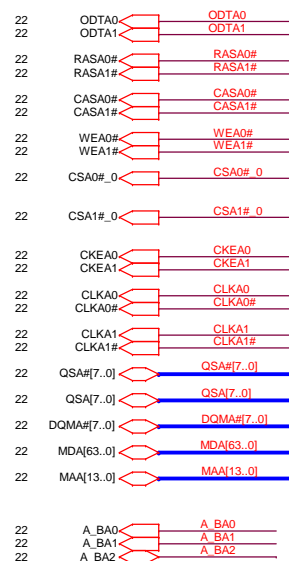
### Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

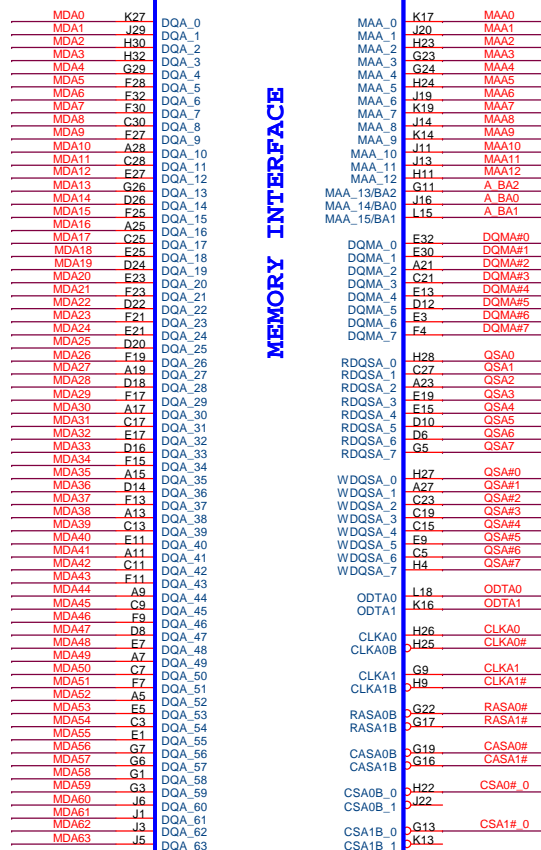
It is a shared pin strap with CONFIG[2:0] if BIOS ROM EN is set to 0.



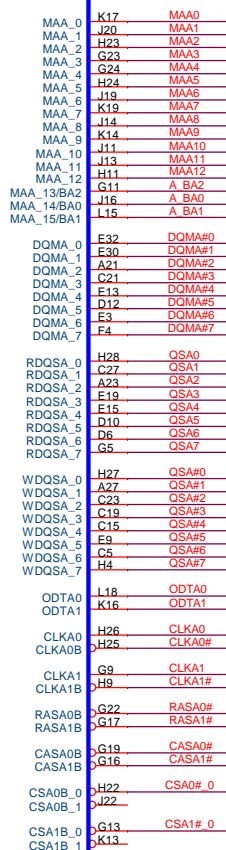




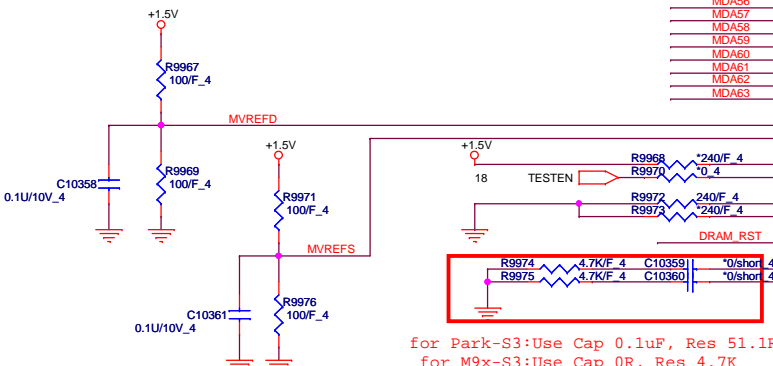
support 1Gbit  
VRAM ( 64M x 16 )



# MEMORY INTERFACE

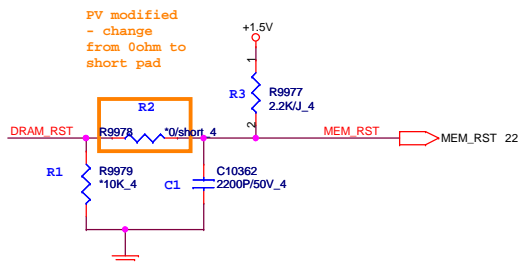


for Park-S3:Use only  
for M9x-S3: no support



	M9x-S2/S3	Park-S3
MEM_CALRN0 (J25)	NC	240R
MEM_CALRP0 (K25)	NC	240R
MEM_CALRP1 (J8)	240R	150R
TESTEN2#2 (K7)	NC	0R
R1	NC	10K
R2	0R	680R
R3	2.2K	NC
C1	2.2nF	68pF

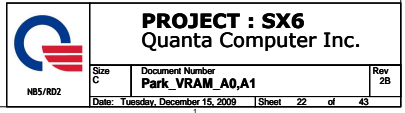
240R:CS12402FB03  
150R:CS11502FB21  
  
0R:CS00002JB38  
680R:CS16802JB27  
  
2.2nF:CH22206KB16  
68pF:CH06806JB01

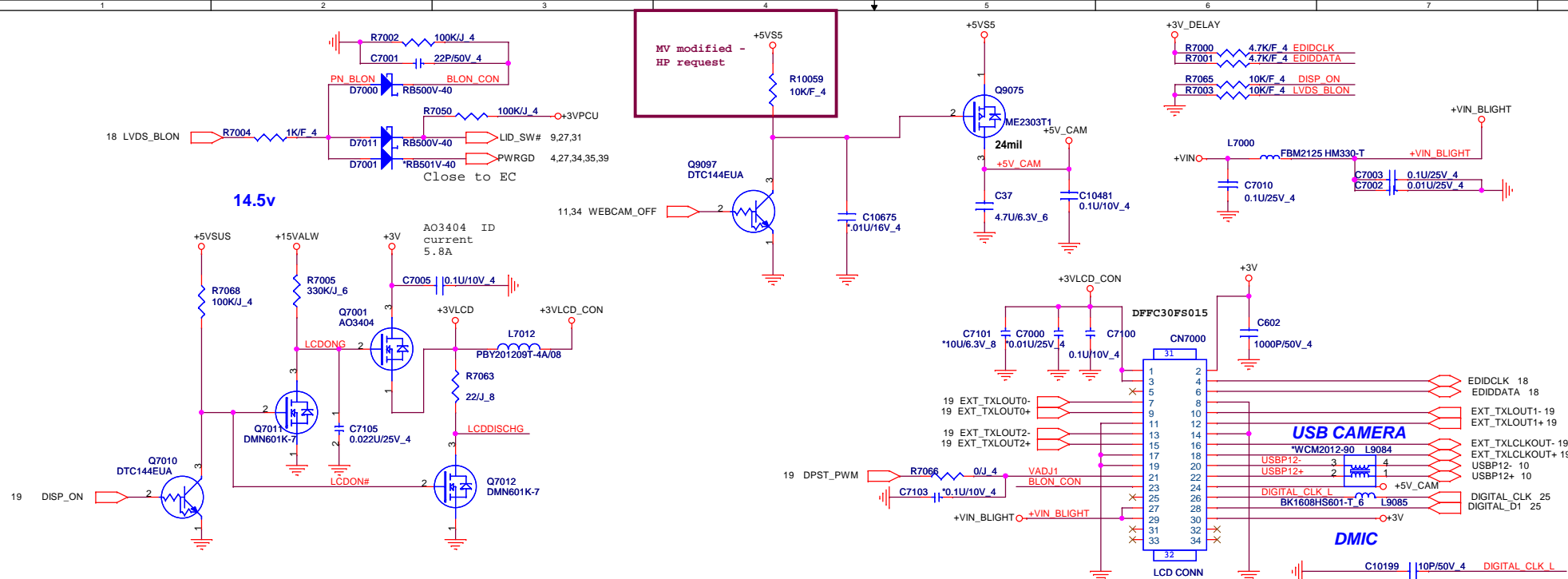


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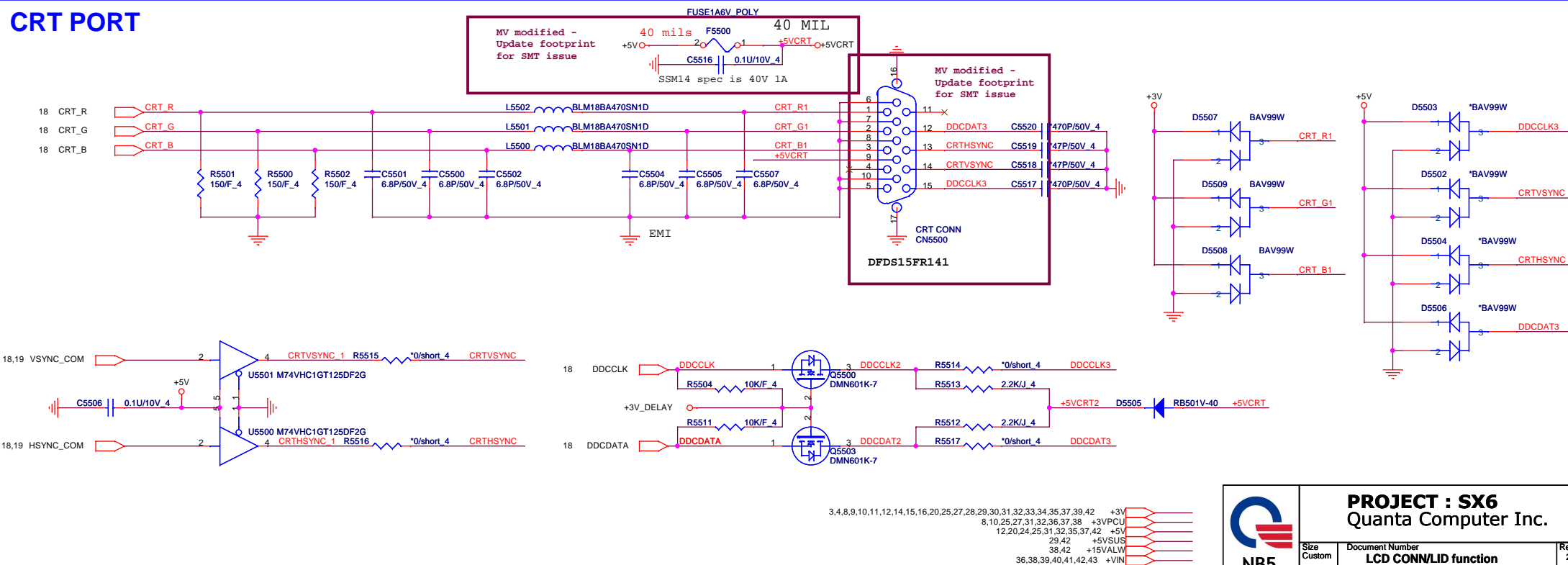
Size Custom	Document Number <b>Park_MEM_Interface</b>	Rev 2B
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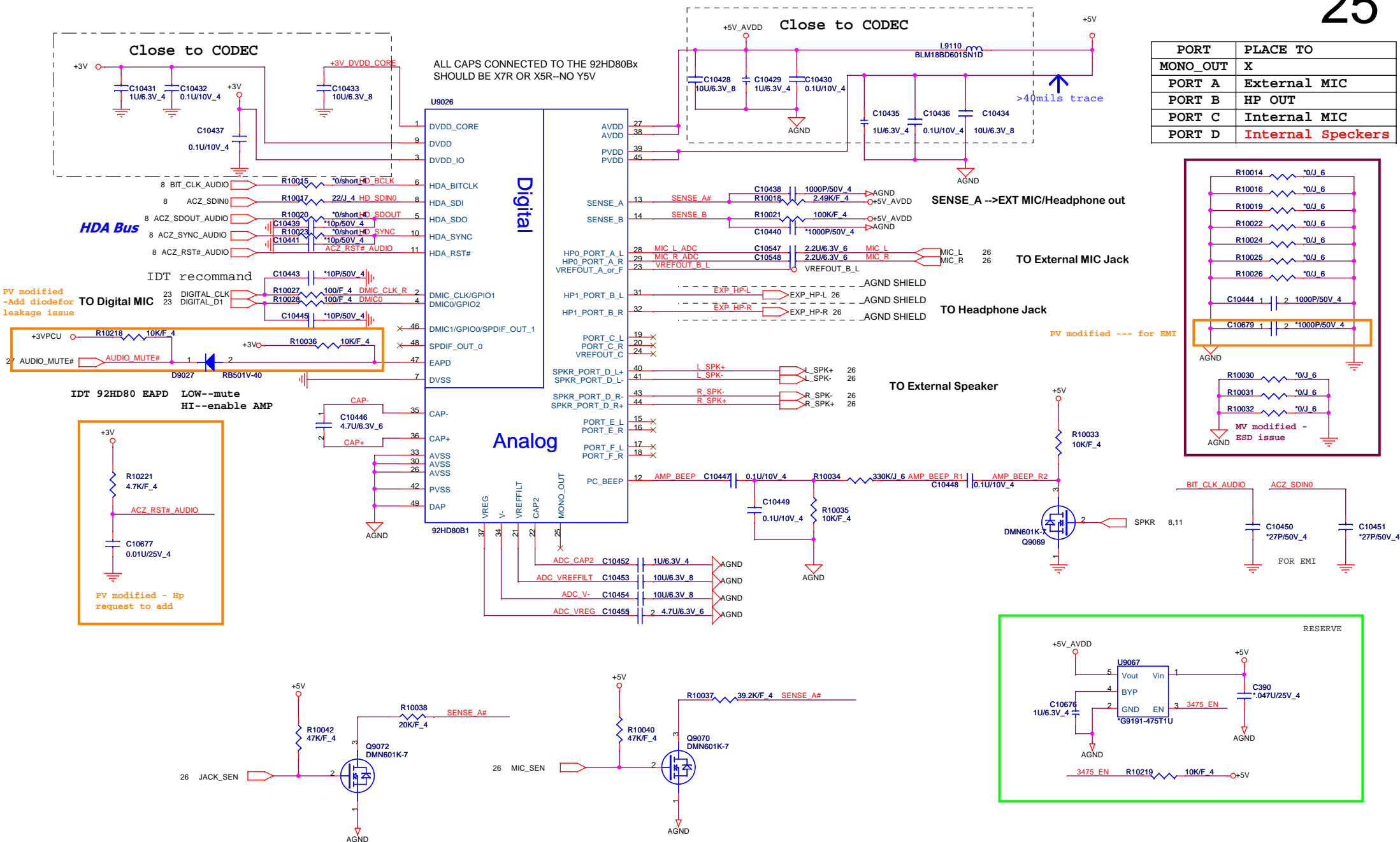


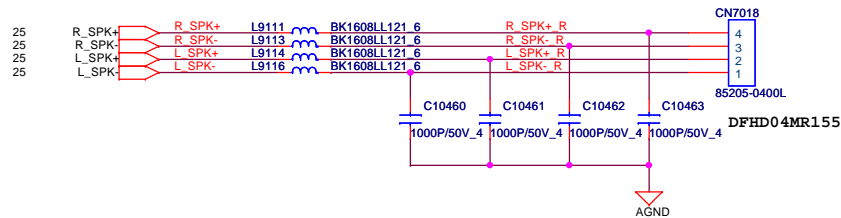
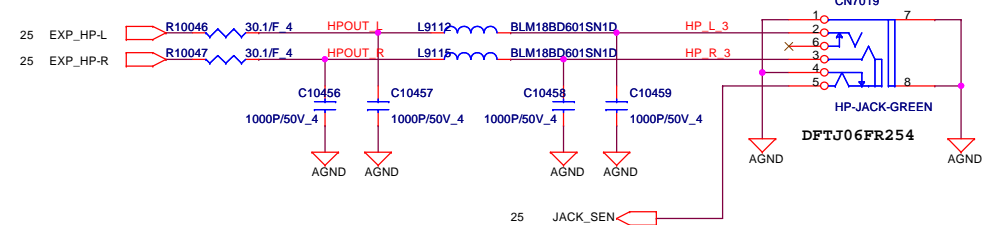
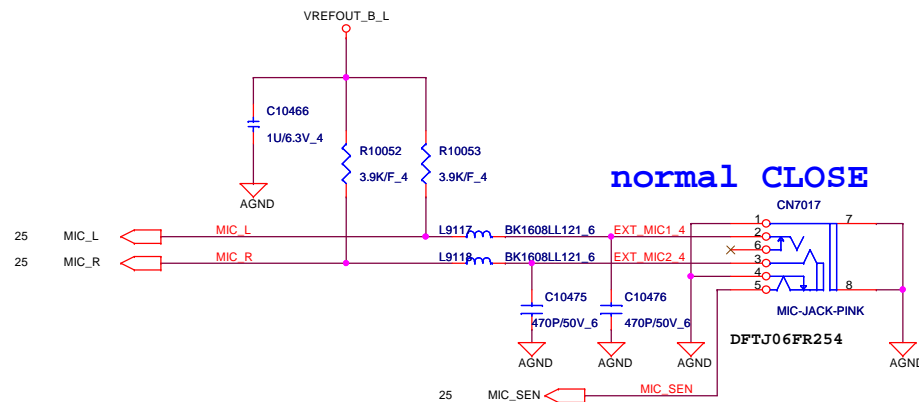


## CRT PORT





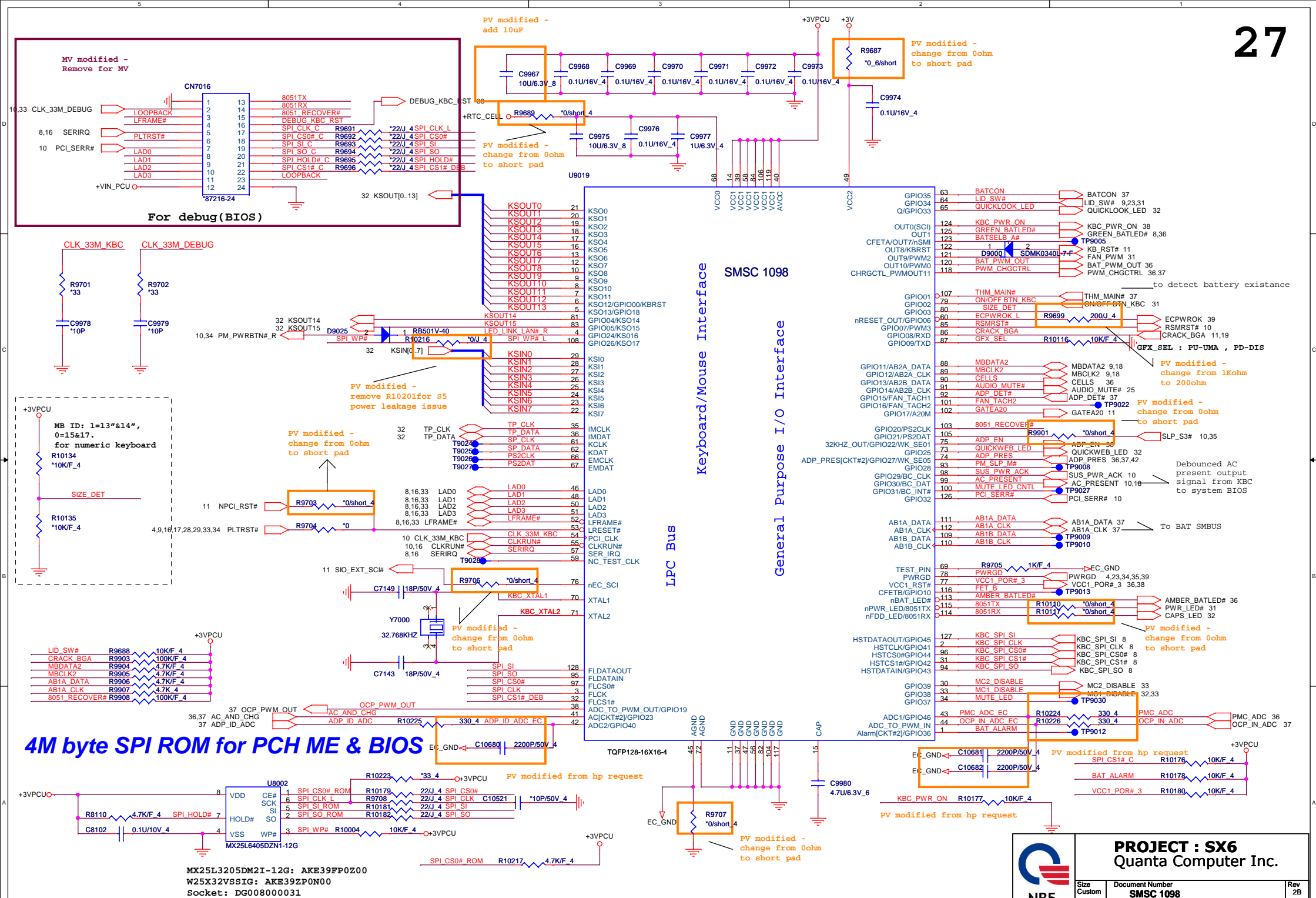


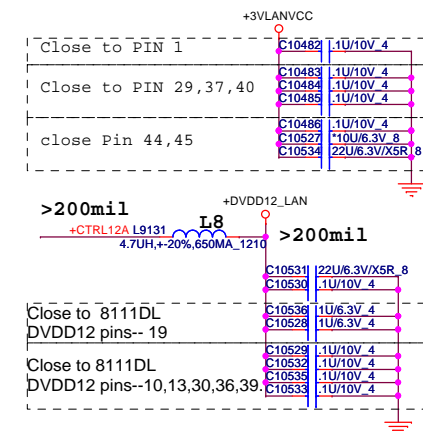
**INT. SPEAKER****Headphone Jack****normal CLOSE****EXT Mic Jack****normal CLOSE**

Note: MIC\_SEN# is electrically floating when no jack is inserted and shorted to ground when jack is present.

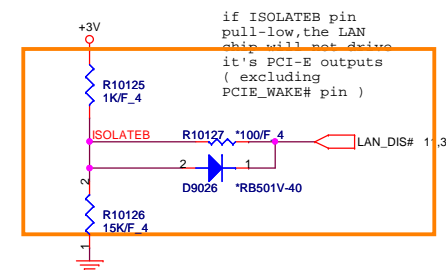
Note: JACK\_SEN# is electrically floating when no jack is inserted and shorted to ground when jack is present.



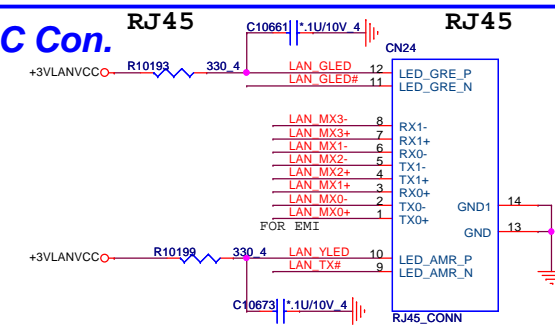




R461 and R463 are used in RTL8111DL, remove R463 if switching regulator is enable, Remove R461 external power is used.

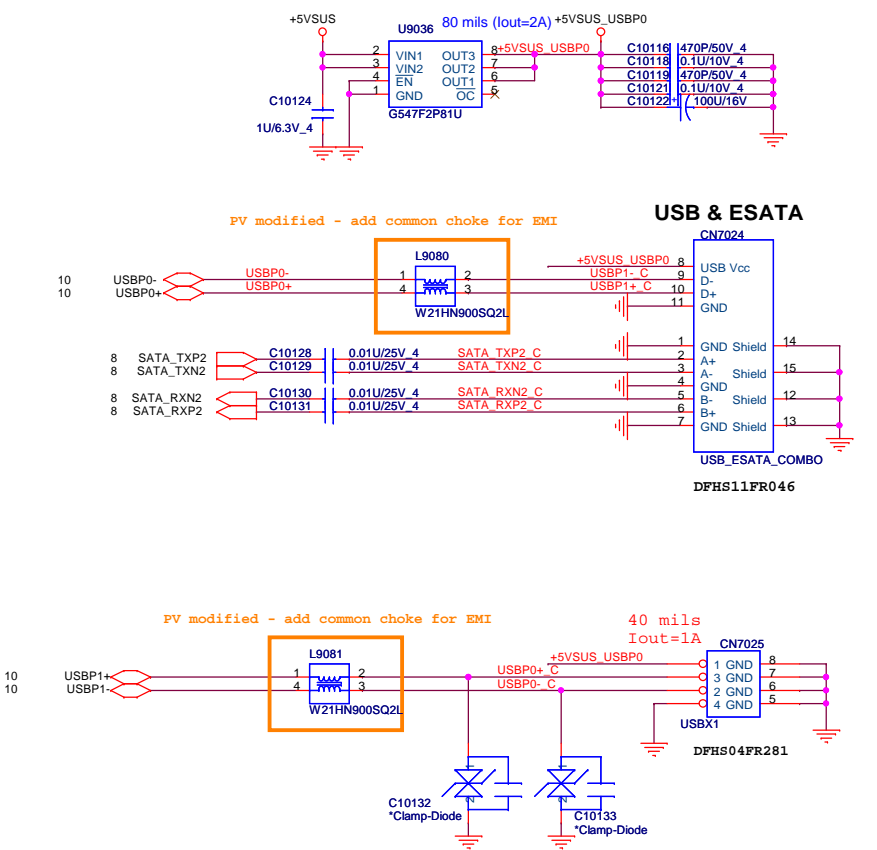


## RJ45

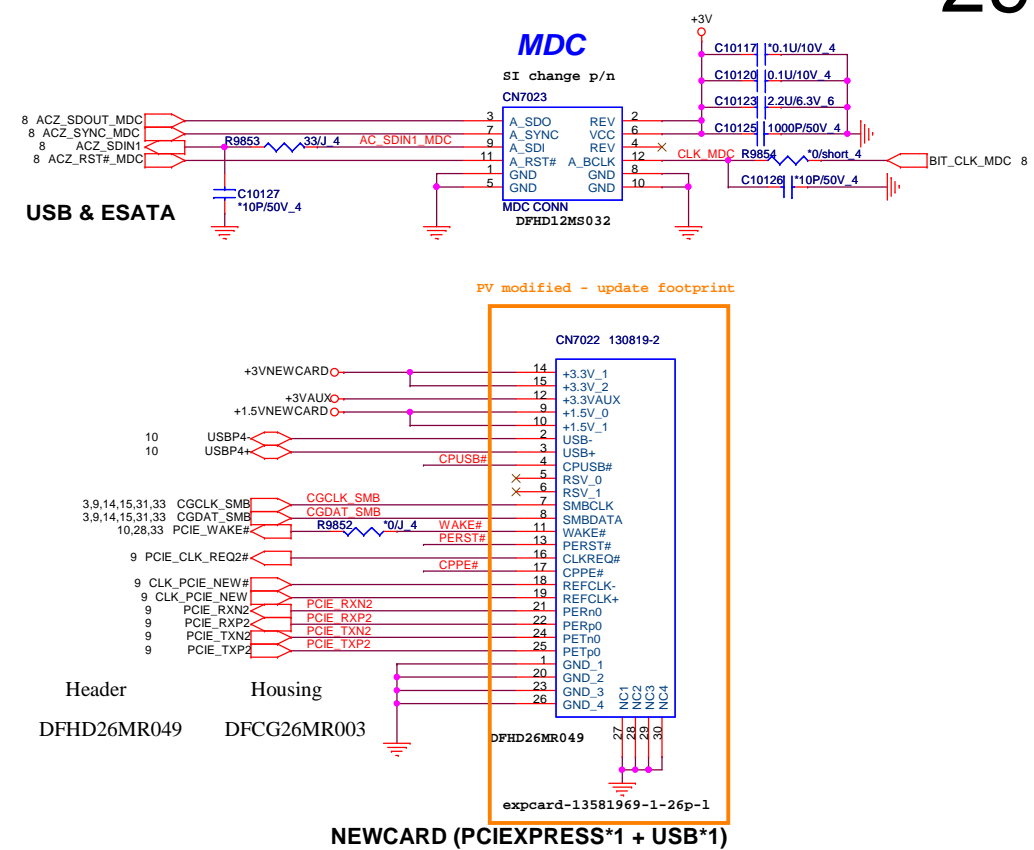


Size Custom	Document Number <b>RTL8151DH-GR</b>	Rev 2B
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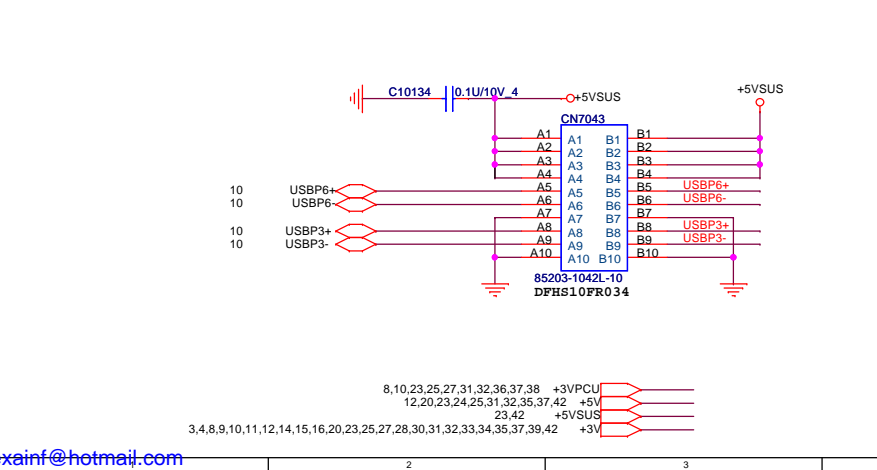
# LEFT SIDE USBX1 and E-SATA/USB COMBO



# Modem CONN

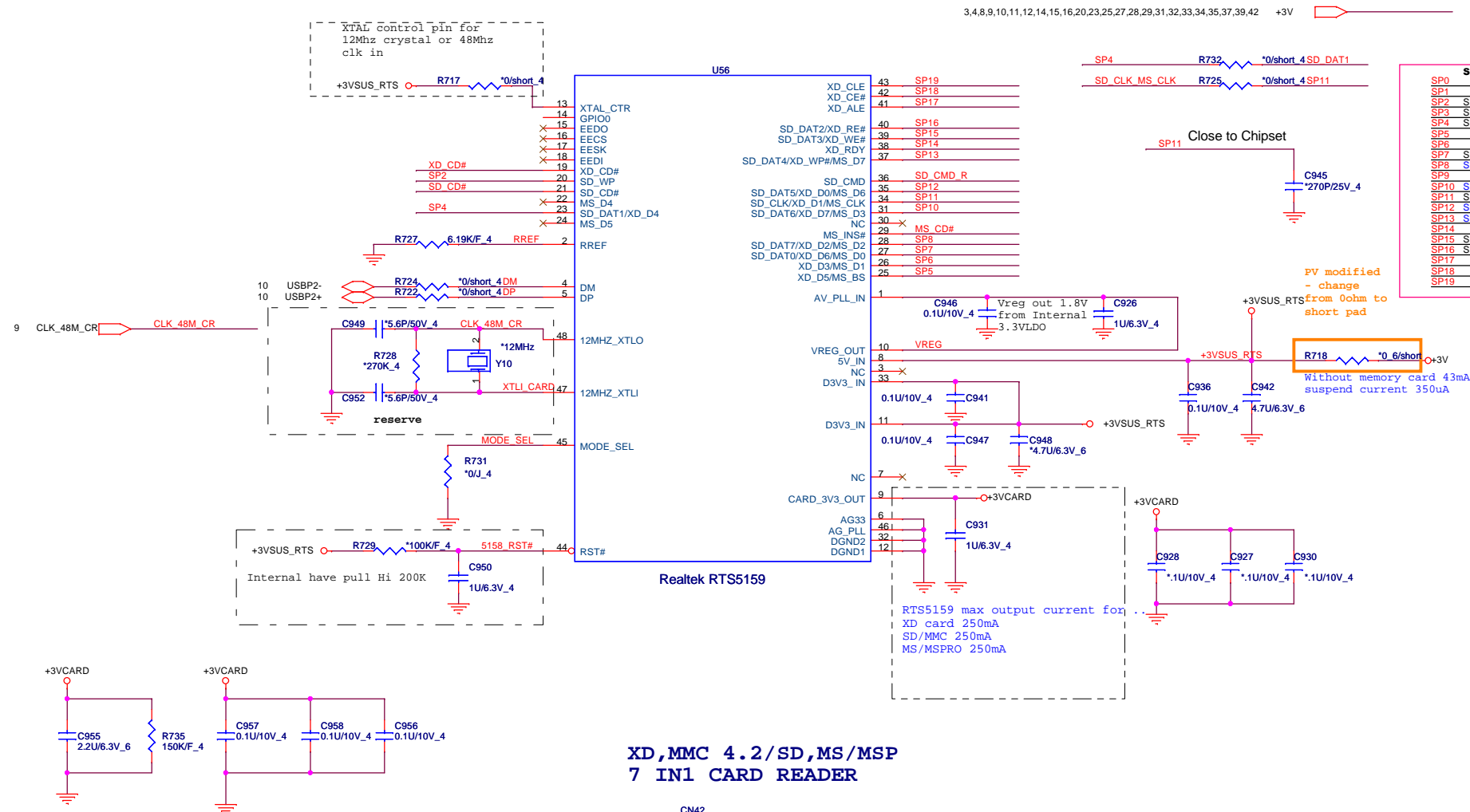


# RIGHT SIDE USBX2

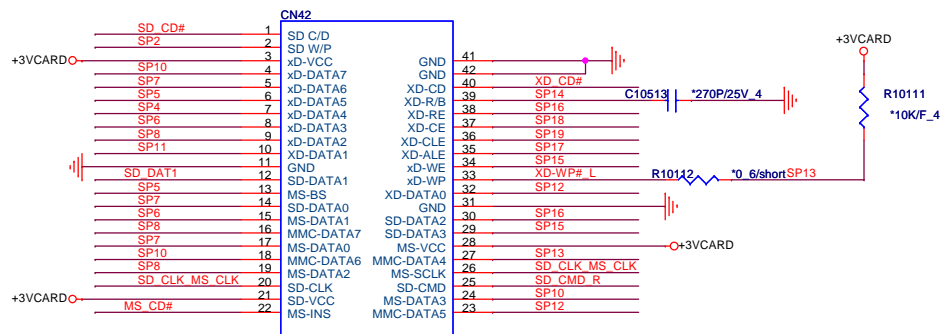


Note:


SP0	SD/MMC 4.2	MS	XD
SP1	SD WP		XD CD#
SP2	SD CD#		
SP3	SD DAT1		XD D4
SP4		MS BS	XD D5
SP5		MS D1	XD D3
SP6		MS D0	XD D6
SP7	SD DAT0	MS D2	XD D2
SP8	SD DAT7/MMC DAT7	MS INS#	
SP9	SD DAT6/MMC DAT6	MS D3	XD D7
SP10	SD CLK	MS SCLK	XD D1
SP11	SD DAT5/MMC DAT5		XD D0
SP12	SD DAT4/MMC DAT4		XD WP#
SP13			XD R/B#
SP14			XD WE#
SP15			XD RE#
SP16			XD ALE
SP17			XD CE#
SP18			XD CLE
SP19			



XD, MMC 4.2 / SD, MS / MSP  
7 IN1 CARD READER



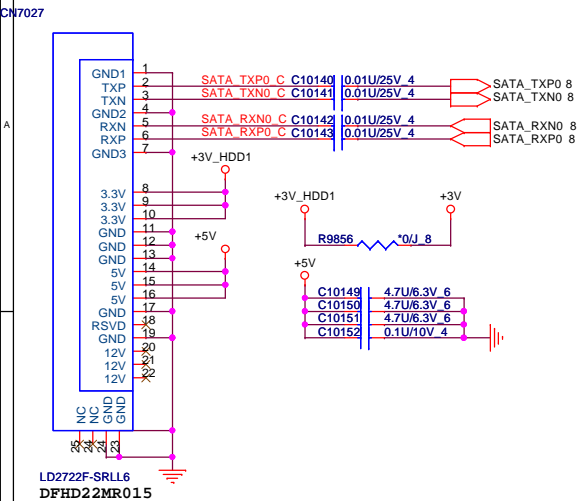
PLASTIC CM7S-02 CARD READER SOCKET  
DFHD42MR011



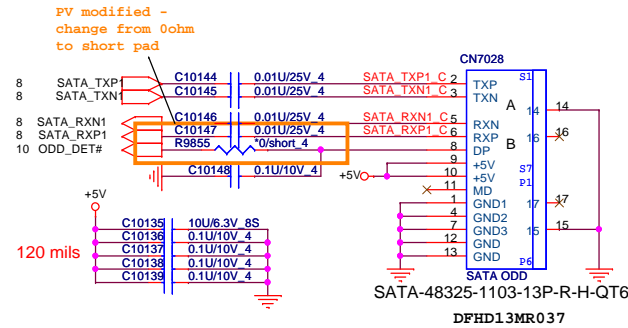
**PROJECT : SX6**  
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Size Custom	Document Number <b>RTS5159 &amp; CR SOCKET</b>	Rev 2B
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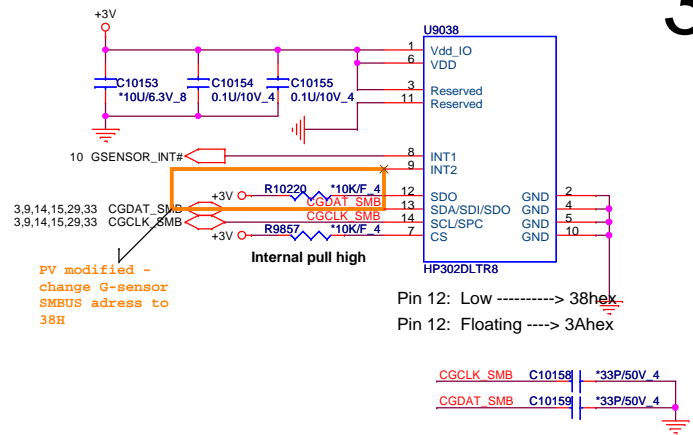
## SATA HDD CONNECTOR



## SATA CD-ROM

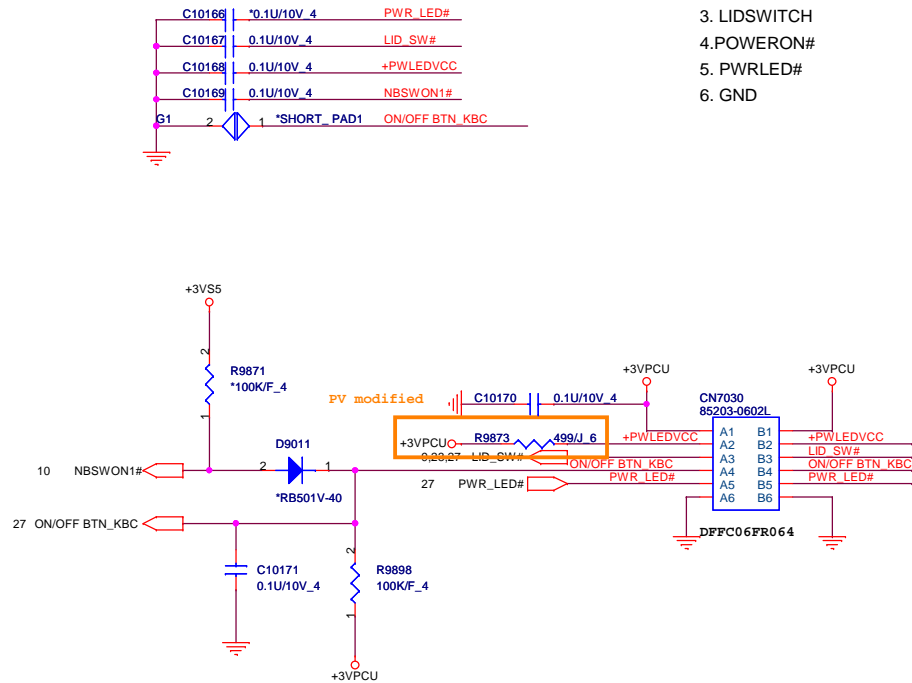


## Accelerometer Sensor

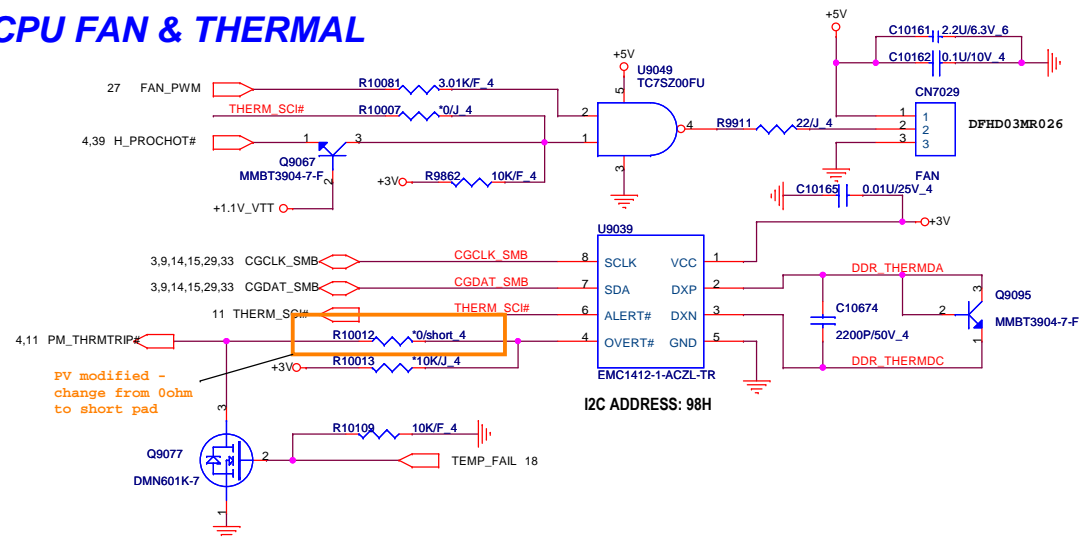


## POWER BOTTON CONNECT

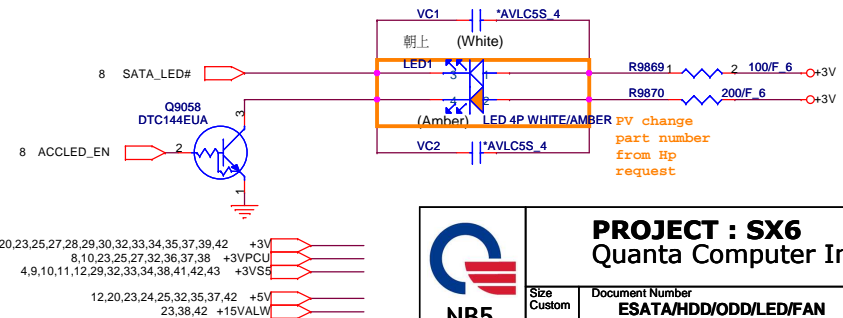
- 1.+3VPCU(LIDSWITCH PWR)
- 2.LEDVCC(+3VPCU)
- 3.LIDSWITCH
- 4.POWERON#
- 5.PWRLED#
- 6.GND



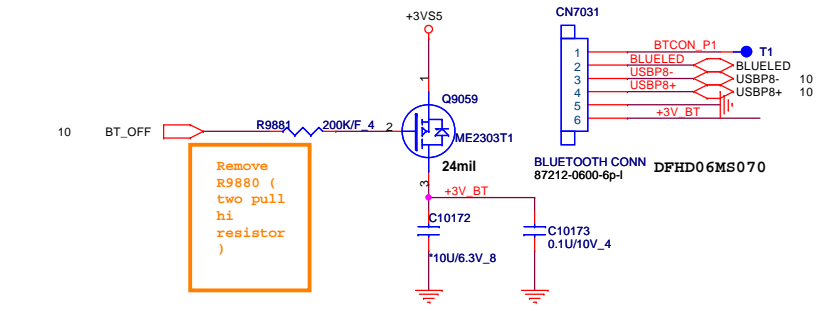
## CPU FAN &amp; THERMAL



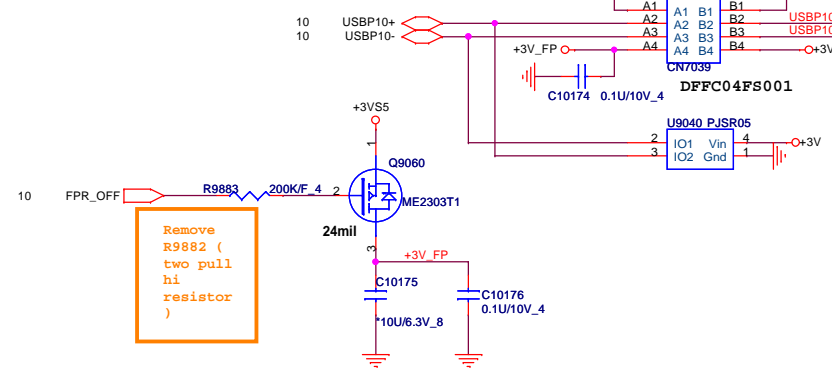
## LED



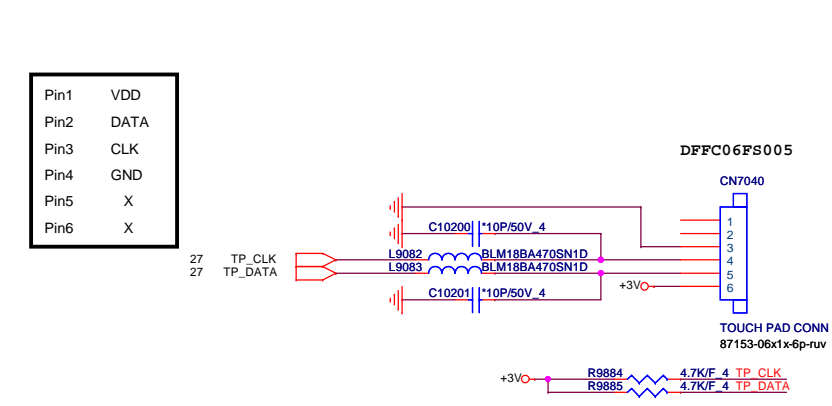
BLUETOOTH



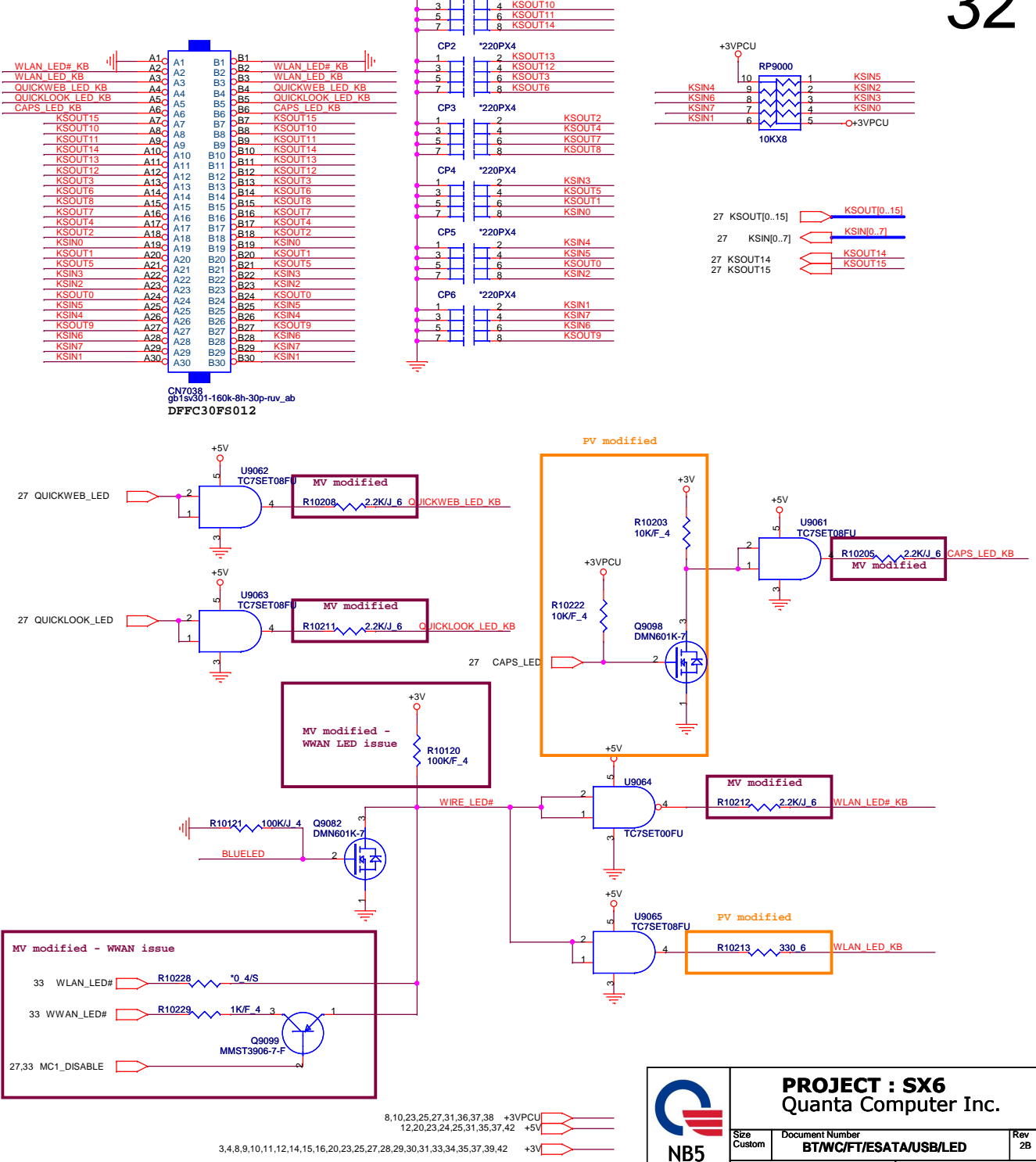
USB fingerprint CON



TOUCH PAD CONNECTOR

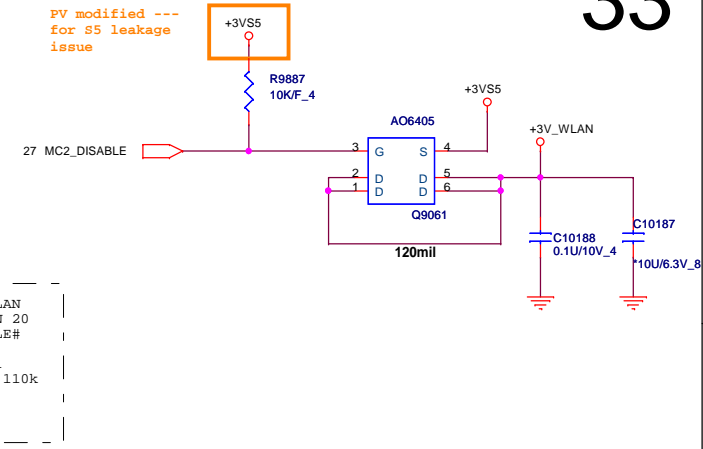
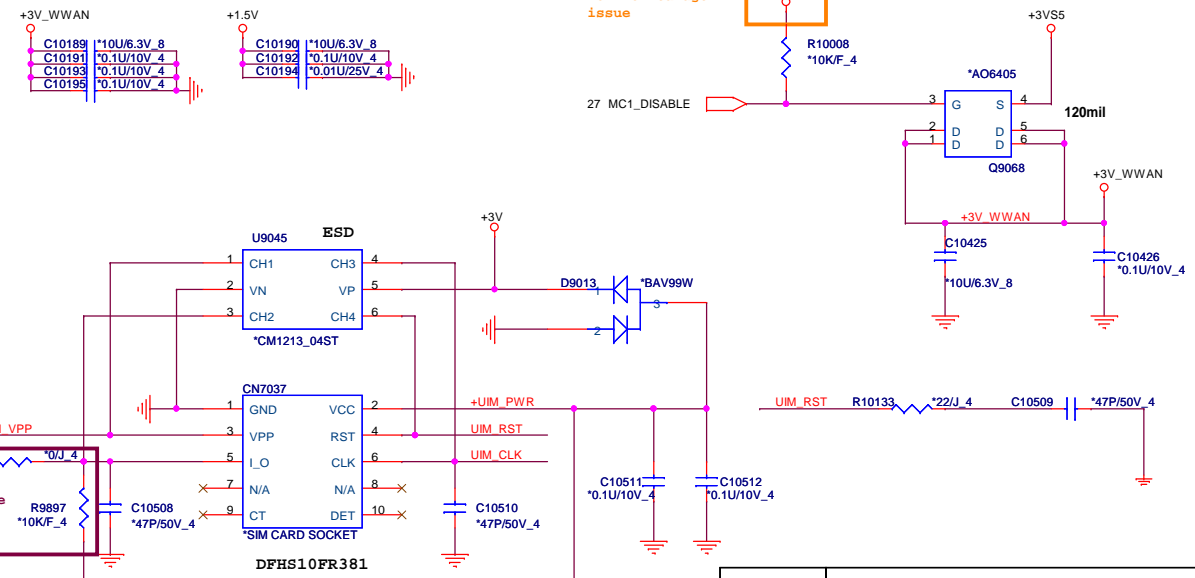


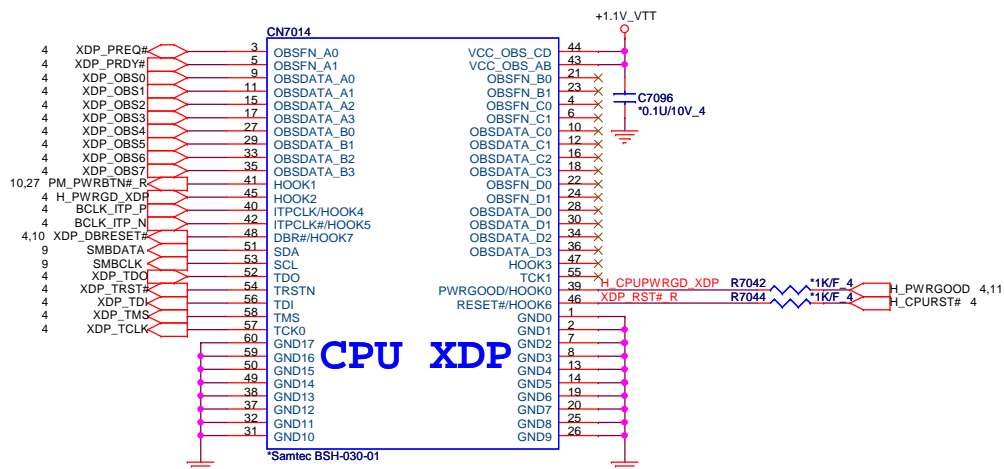
KEYBOARD CONNECTOR.



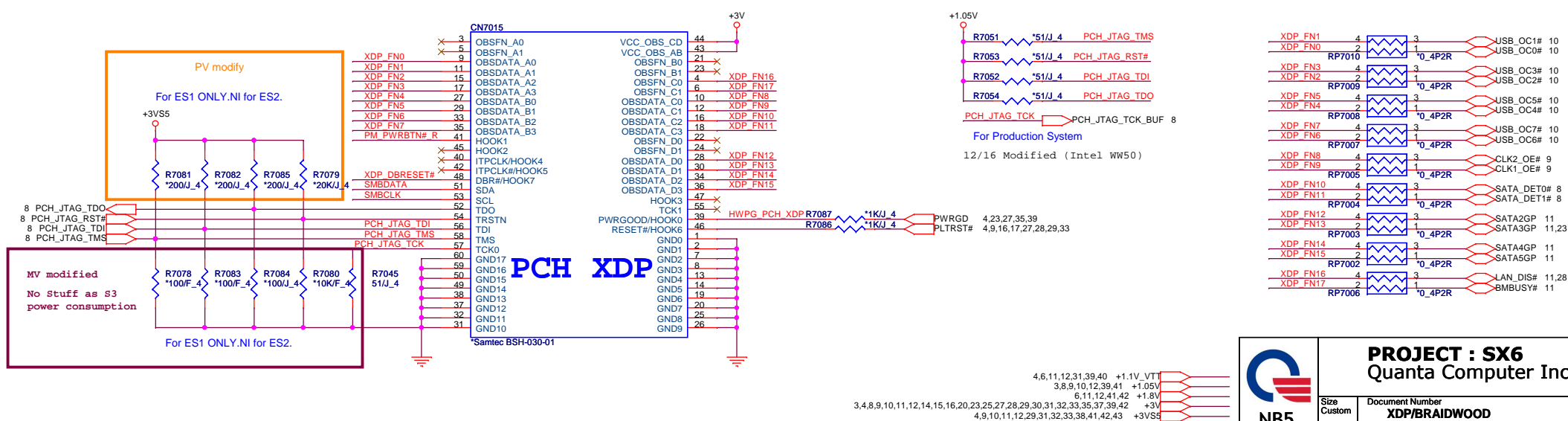
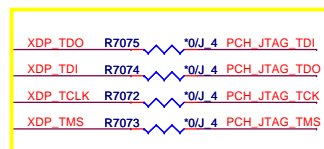


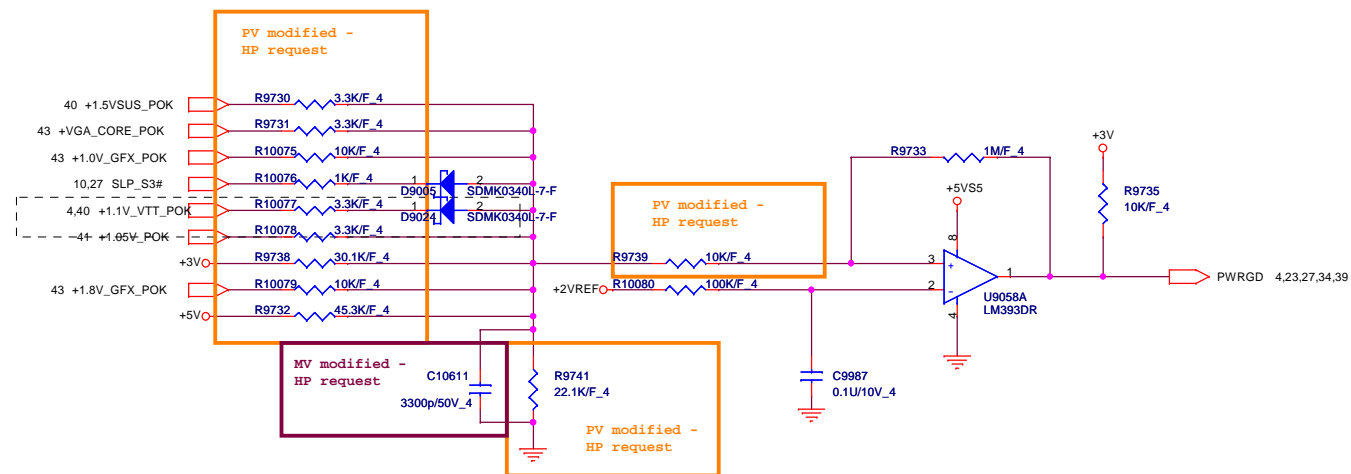
## 33

[illegible]

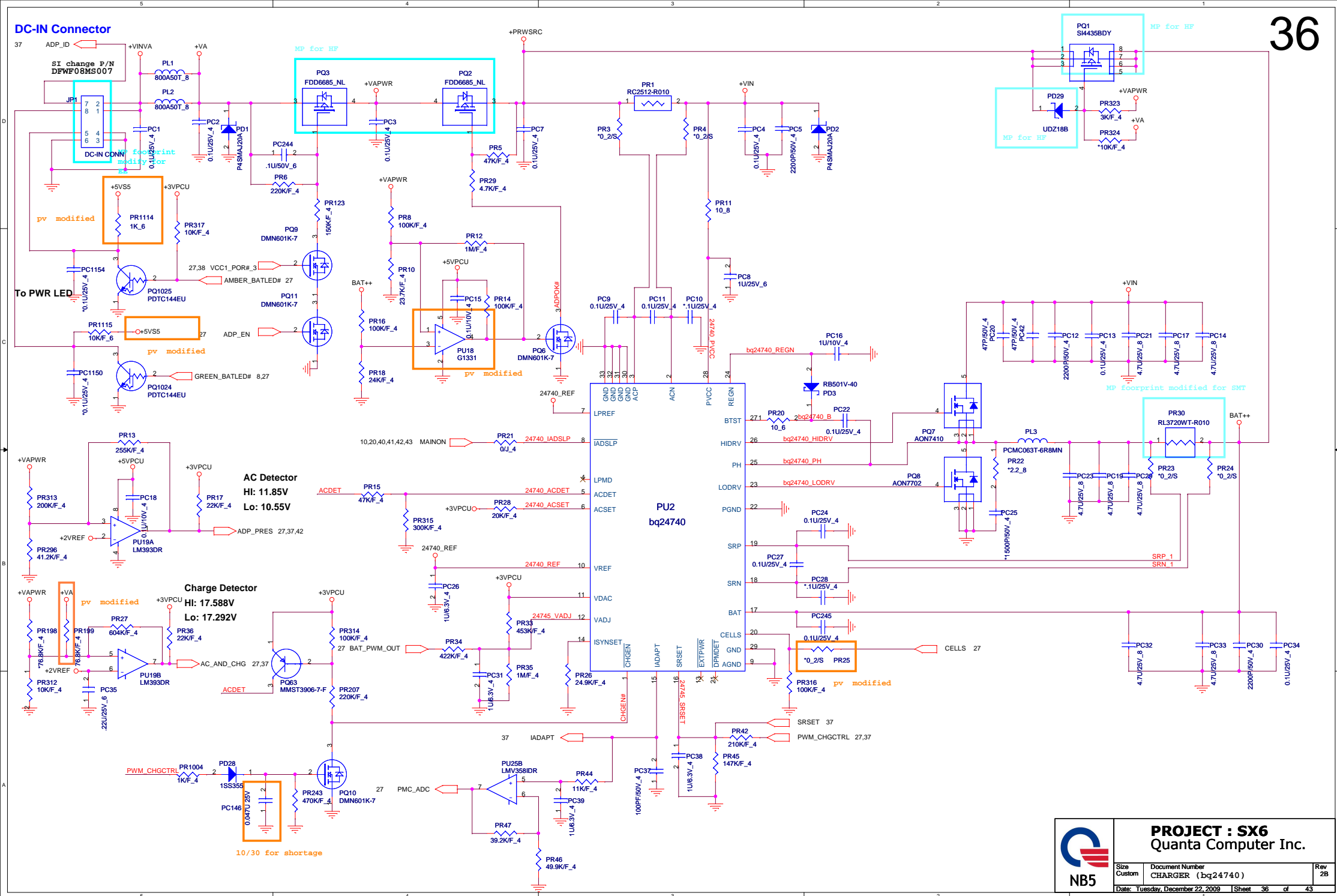


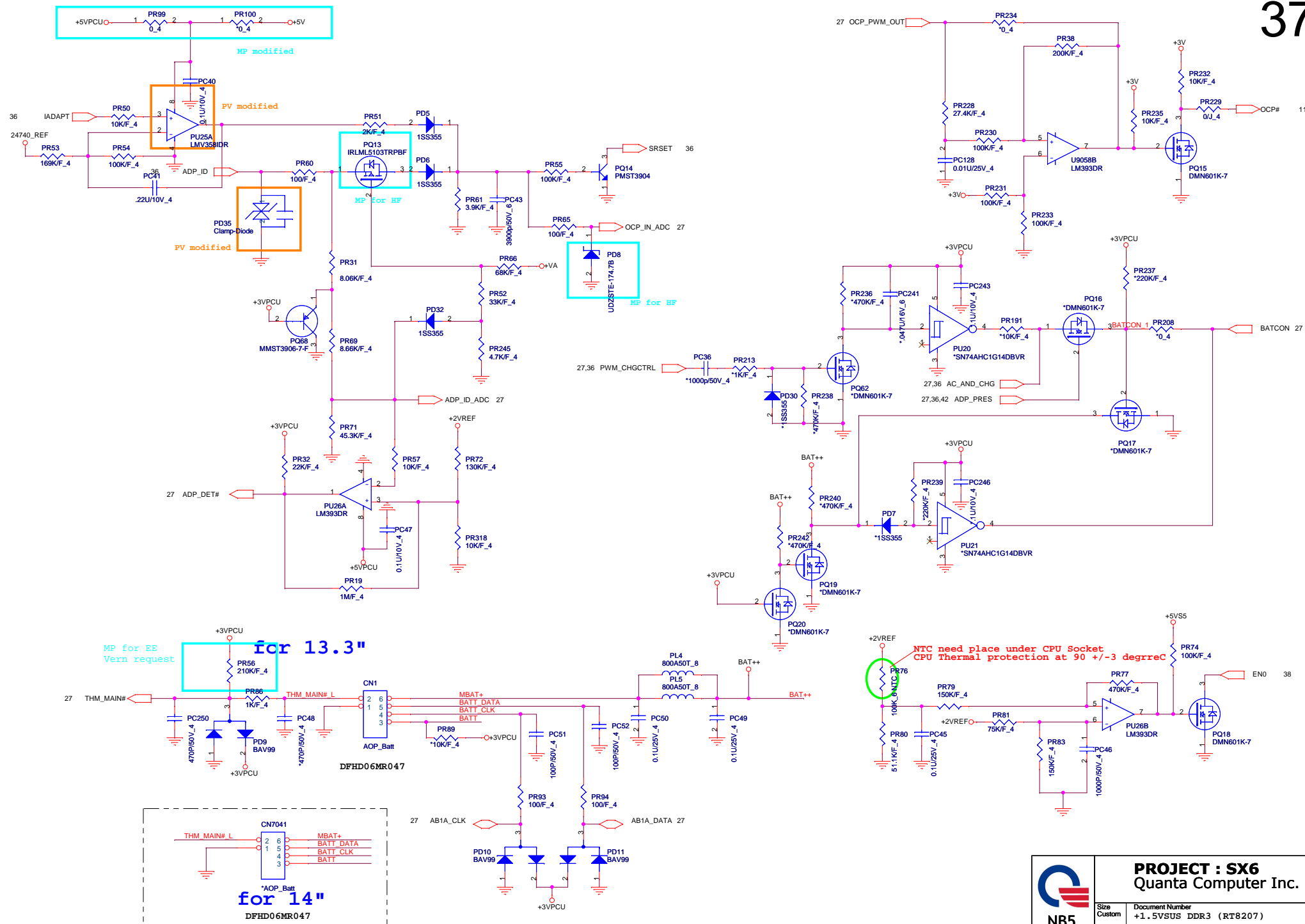
Reserve for BSDL

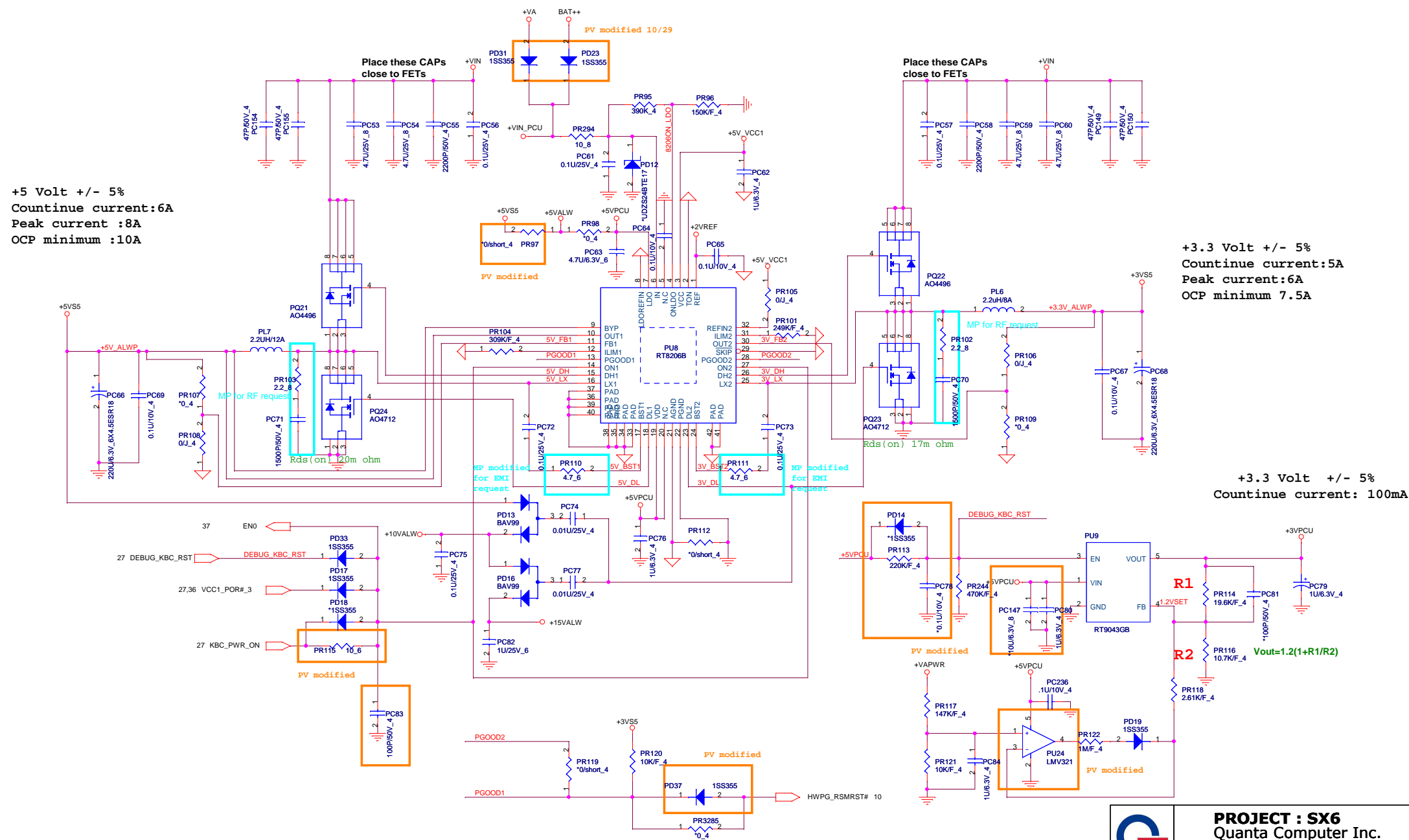




## DC-IN Connector



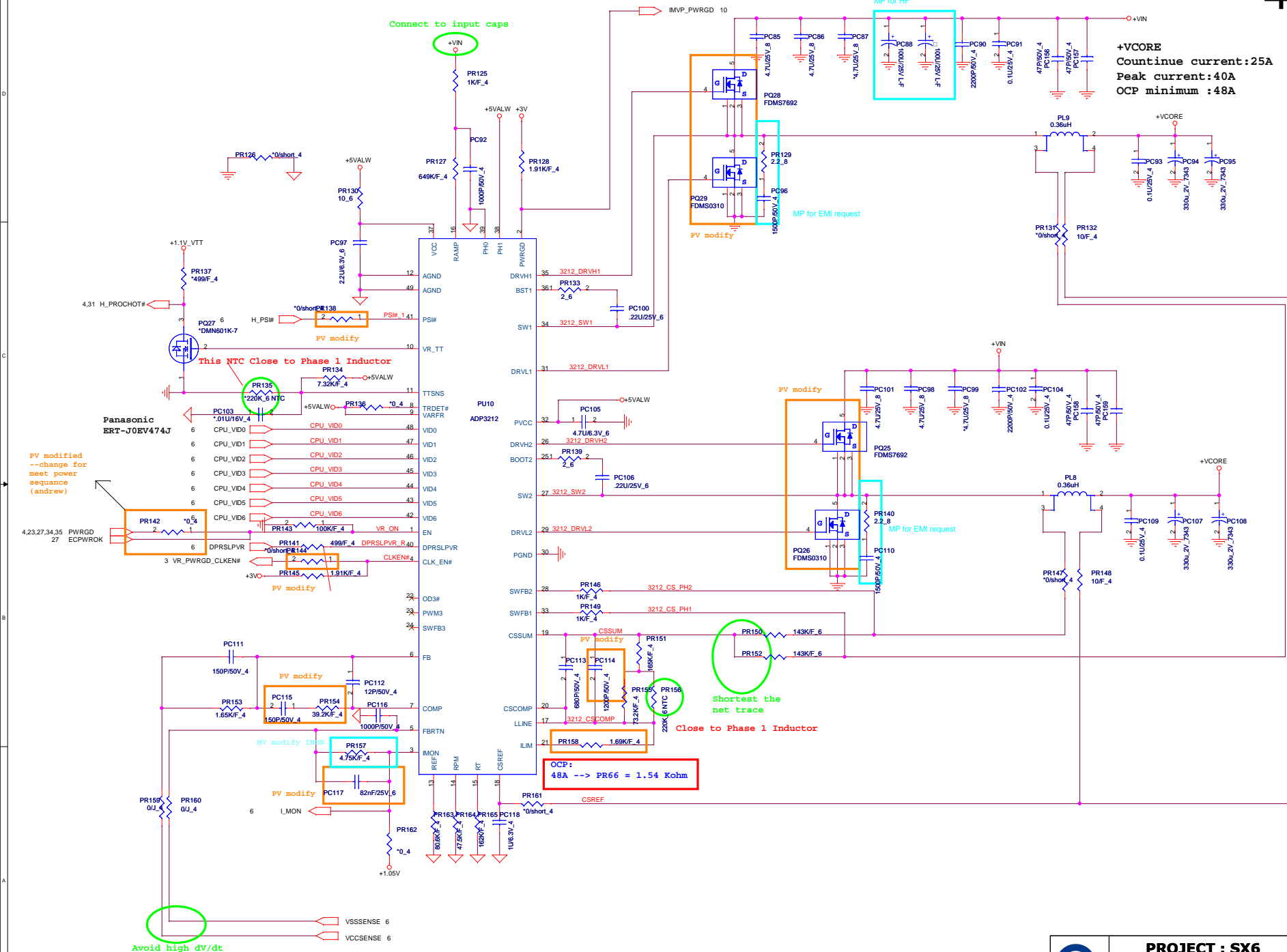


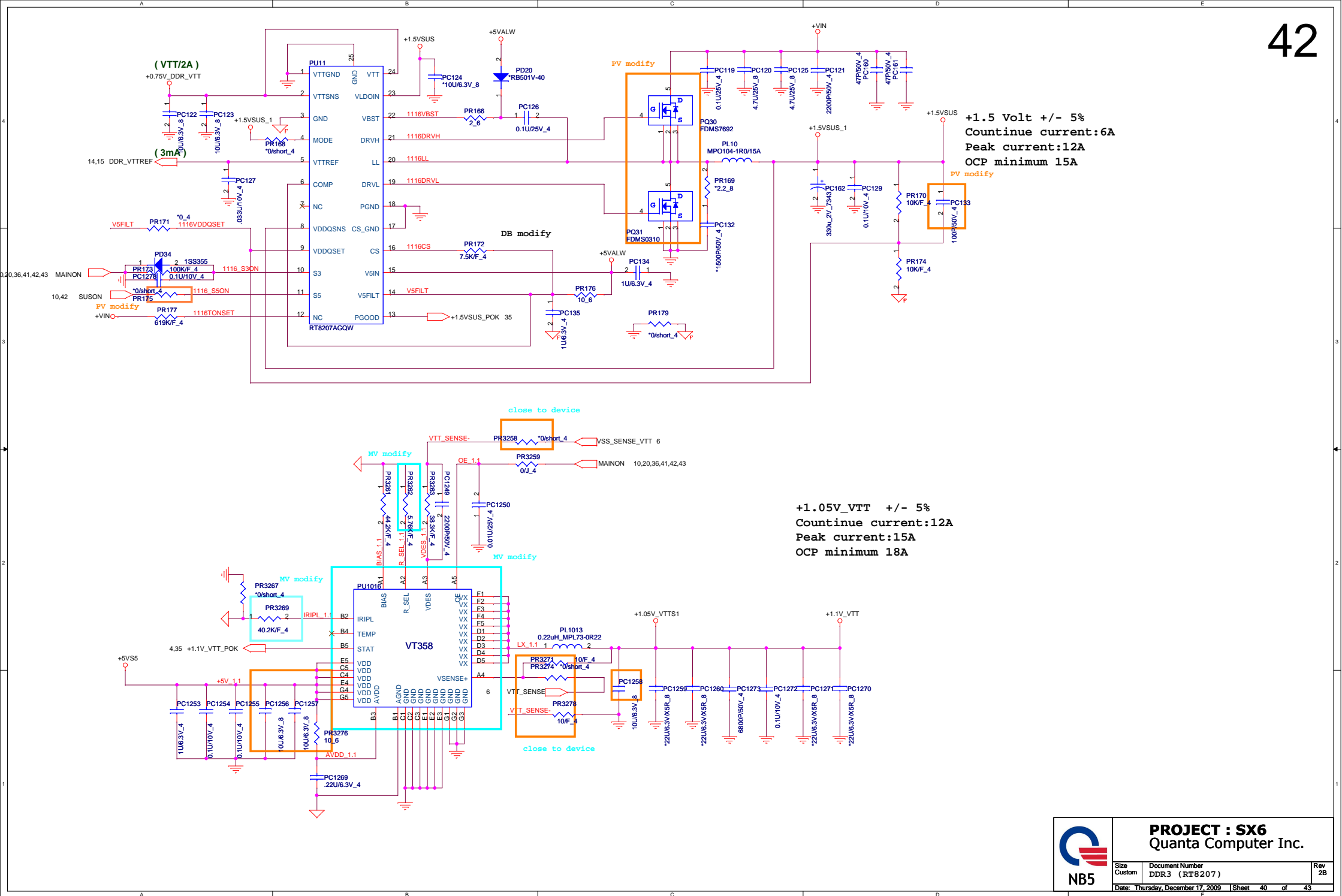


+3.3 Volt +/- 5%  
Continue current:5A  
Peak current:6A  
OCP minimum 7.5A

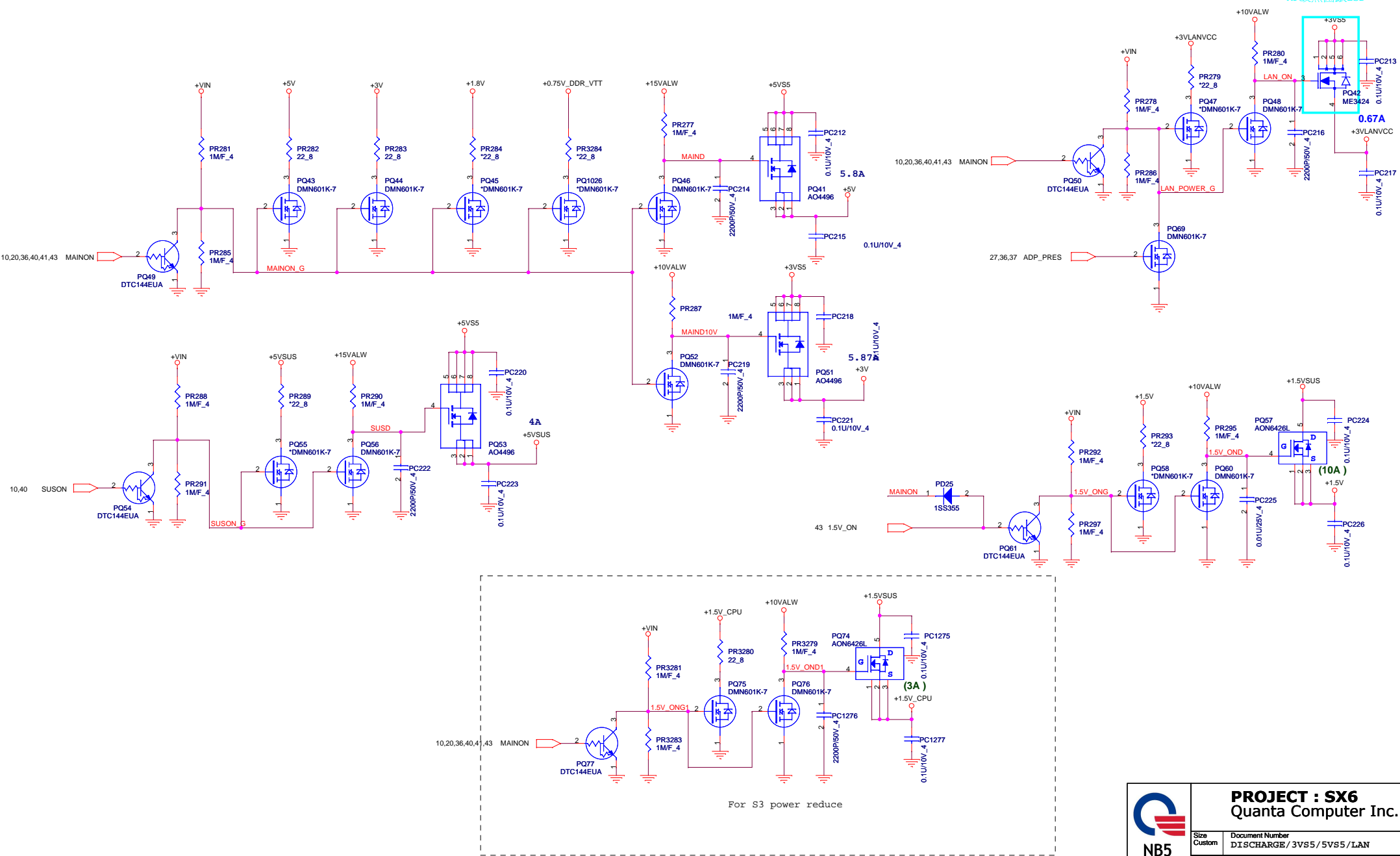
+3.3 Volt +/- 5%  
Continue current: 100mA












 <b>NB5</b>	<b>PROJECT : SX6</b> <b>Quanta Computer Inc.</b>		
	Size Custom	Document Number <b>DISCHARGE/3VS5/5VS5/LAN</b>	Rev <b>2B</b>
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