Touch PAD

GPIO

Skytake-U Strapping Table

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Strap Description</th>
<th>Sampled Configuration</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPP_B14 (SPKR)</td>
<td>Top-Block Swap only</td>
<td>PCH_PWROCK</td>
<td></td>
</tr>
<tr>
<td>GPP_B18 (CAPB. MOSO)</td>
<td>No Reboot</td>
<td>PCH_PWROCK</td>
<td></td>
</tr>
<tr>
<td>GPP_C2 (SMBALERT8)</td>
<td>TLS Confidential</td>
<td>RSMSRT8</td>
<td></td>
</tr>
<tr>
<td>GPP_C6 (SMBALERT9)</td>
<td>USB BIOS Swap Bit (SSBI)</td>
<td>PCH_PWROCK</td>
<td></td>
</tr>
<tr>
<td>GPP_B2 (CAPF1. MOSO)</td>
<td>Boot BIOS Swap Bit (SSBI)</td>
<td>PCH_PWROCK</td>
<td></td>
</tr>
<tr>
<td>GPP_C6 (SMBALERT9)</td>
<td>eSPI or LPC</td>
<td>RSMSRT8</td>
<td></td>
</tr>
<tr>
<td>GPP_MSO0</td>
<td>Reserved</td>
<td>RSMSRT8</td>
<td>(IPU 15 - 40K)</td>
</tr>
<tr>
<td>GPP_MSO1</td>
<td>Reserved</td>
<td>RSMSRT8</td>
<td>(IPU 15 - 40K)</td>
</tr>
<tr>
<td>GPP_C2 (SMBALERT9)</td>
<td>(PCHIOTD)</td>
<td>RSMSRT8</td>
<td>(IPU 20K)</td>
</tr>
<tr>
<td>GPP_ID0</td>
<td>Reserved</td>
<td>RSMSRT8</td>
<td>(IPU 15 - 40K)</td>
</tr>
<tr>
<td>GPP_ID2</td>
<td>Reserved</td>
<td>RSMSRT8</td>
<td>(IPU 15 - 40K)</td>
</tr>
<tr>
<td>HDA_SDO / USB_TXD</td>
<td>Flash Descriptor Security</td>
<td>PCH_PWROCK</td>
<td>(IPU 15 - 40K)</td>
</tr>
<tr>
<td>GPP_E1 (DDPF_CTRLDATA)</td>
<td>Display Port B Detected</td>
<td>PCH_PWROCK</td>
<td>(IPU 20K)</td>
</tr>
<tr>
<td>GPP_E2 (DDPF_CTRLDATA)</td>
<td>Display Port C Detected</td>
<td>PCH_PWROCK</td>
<td>(IPU 20K)</td>
</tr>
</tbody>
</table>

Strapping

Touchpad INT

Reserved UART FFC connector for Win 7 debug

UART2 for RMT

Add GPU Power Control Signals

GPU Control PU/PD

SPKR

Note: For GC6 NV DG GC6_FB_EN PD.

20131015

Rev:D change to eSPI or LPC

HDA_SDO / USB TXD

Flash-Descriptor Security

Overclock Intel ME Clock Mode

CPU_PWROCK

GPP_C7

GPP_CX

GPP_C6

GPP_B20 (CAPB. MOSO) | Boot BIOS Swap Bit (SSBI)         | PCH_PWROCK            | (IPU 15 - 40K) |
| GPP_B2 (CAPF1. MOSO) | Boot BIOS Swap Bit (SSBI)         | PCH_PWROCK            | (IPU 15 - 40K) |
| GPP_C6 (SMBALERT9) | eSPI or LPC                        | RSMSRT8               | (IPU 20K)  |
| GPP_MSO0       | Reserved                            | RSMSRT8               | (IPU 15 - 40K) |
| GPP_MSO1       | Reserved                            | RSMSRT8               | (IPU 15 - 40K) |
| GPP_C2 (SMBALERT9) | (PCHIOTD)                         | RSMSRT8               | (IPU 20K)  |
| GPP_ID0        | Reserved                            | RSMSRT8               | (IPU 15 - 40K) |
| GPP_ID2        | Reserved                            | RSMSRT8               | (IPU 15 - 40K) |
| HDA_SDO / USB_TXD | Flash Descriptor Security         | PCH_PWROCK            | (IPU 15 - 40K) |
| GPP_E1 (DDPF_CTRLDATA) | Display Port B Detected          | PCH_PWROCK            | (IPU 20K)  |
| GPP_E2 (DDPF_CTRLDATA) | Display Port C Detected          | PCH_PWROCK            | (IPU 20K)  |

Note: For GC6 NV DG GC6_FB_EN PD.

20131015

Rev:D change to eSPI or LPC

HDA_SDO / USB TXD

Flash-Descriptor Security

Overclock Intel ME Clock Mode

CPU_PWROCK

GPP_C7

GPP_CX

GPP_C6

GPP_B20 (CAPB. MOSO) | Boot BIOS Swap Bit (SSBI)         | PCH_PWROCK            | (IPU 15 - 40K) |
| GPP_B2 (CAPF1. MOSO) | Boot BIOS Swap Bit (SSBI)         | PCH_PWROCK            | (IPU 15 - 40K) |
| GPP_C6 (SMBALERT9) | eSPI or LPC                        | RSMSRT8               | (IPU 20K)  |
| GPP_MSO0       | Reserved                            | RSMSRT8               | (IPU 15 - 40K) |
| GPP_MSO1       | Reserved                            | RSMSRT8               | (IPU 15 - 40K) |
| GPP_C2 (SMBALERT9) | (PCHIOTD)                         | RSMSRT8               | (IPU 20K)  |
| GPP_ID0        | Reserved                            | RSMSRT8               | (IPU 15 - 40K) |
| GPP_ID2        | Reserved                            | RSMSRT8               | (IPU 15 - 40K) |
| HDA_SDO / USB_TXD | Flash Descriptor Security         | PCH_PWROCK            | (IPU 15 - 40K) |
| GPP_E1 (DDPF_CTRLDATA) | Display Port B Detected          | PCH_PWROCK            | (IPU 20K)  |
| GPP_E2 (DDPF_CTRLDATA) | Display Port C Detected          | PCH_PWROCK            | (IPU 20K)  |

Note: For GC6 NV DG GC6_FB_EN PD.

20131015

Rev:D change to eSPI or LPC

HDA_SDO / USB TXD

Flash-Descriptor Security

Overclock Intel ME Clock Mode

CPU_PWROCK

GPP_C7

GPP_CX

GPP_C6

GPP_B20 (CAPB. MOSO) | Boot BIOS Swap Bit (SSBI)         | PCH_PWROCK            | (IPU 15 - 40K) |
| GPP_B2 (CAPF1. MOSO) | Boot BIOS Swap Bit (SSBI)         | PCH_PWROCK            | (IPU 15 - 40K) |
| GPP_C6 (SMBALERT9) | eSPI or LPC                        | RSMSRT8               | (IPU 20K)  |
| GPP_MSO0       | Reserved                            | RSMSRT8               | (IPU 15 - 40K) |
| GPP_MSO1       | Reserved                            | RSMSRT8               | (IPU 15 - 40K) |
| GPP_C2 (SMBALERT9) | (PCHIOTD)                         | RSMSRT8               | (IPU 20K)  |
| GPP_ID0        | Reserved                            | RSMSRT8               | (IPU 15 - 40K) |
| GPP_ID2        | Reserved                            | RSMSRT8               | (IPU 15 - 40K) |
| HDA_SDO / USB_TXD | Flash Descriptor Security         | PCH_PWROCK            | (IPU 15 - 40K) |
| GPP_E1 (DDPF_CTRLDATA) | Display Port B Detected          | PCH_PWROCK            | (IPU 20K)  |
| GPP_E2 (DDPF_CTRLDATA) | Display Port C Detected          | PCH_PWROCK            | (IPU 20K)  |
SP@ socket P/N: DFHS08FS023 only for A-TEST

<table>
<thead>
<tr>
<th>SPIROM</th>
<th>Vendor</th>
<th>Size</th>
<th>Quanta P/N</th>
<th>Vender P/N</th>
</tr>
</thead>
<tbody>
<tr>
<td>Skylake 3.3V</td>
<td>WND</td>
<td>8M</td>
<td>AKE3EFP0N07</td>
<td>AK2EZN0Q00</td>
</tr>
<tr>
<td>W25Q64FVSSIQ</td>
<td>W25Q64FV  -- 8MB</td>
<td>3.3V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

PCH SPI ROM(8M+4M)
15ohm CS01502B12
33ohm CS03302B29

For M.2 wifi module must 

2/10 add C633 for EMI request , R748 no stuff from EC site

15ohm CS01502B12

Skylake 5 (SATA/HDA/SPI)
Friday, June 23, 2017
Sheet 7 47 of 5

Quanta Computer Inc.

PROJECT : ZAAR

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Project Rev. 3A

Date: Friday, June 23, 2017

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Quanta Computer Inc.
Intel APS Fixture use

CN1

1 APS1  R209  *0.6  +3V_S5  SUSB# [8,30,31]
2peating A                         PCH_SLP_S5# [8]
3 APS3  R207  *0.6  PCH_SLP_A# [8]
4 R684  *0.4  SUSC# [8,30]
5 R689  *0.4
6 R690  *0.4
7 R691  *0.4
8 APS7  R215  *0.6  +3VPCU  PCH_SLP_A# [8]
9 R688  *0.4  RTC_RST# [6]
10 R687  *0.4  NBSWON# [28,30]
11 R686  *0.4
12 R211  *0.4  SYS_RESET# [8]
13 R206  *0.6
14
15
16
17
18

+3V_S5 [2,3,4,6,7,8,9,20,23,26,27,28,30,31,33,39]
+3VPCU [8,9,22,25,26,27,28,30,31,37,40]
Close to CPU side of CAP.

Note:
1. C1, C3, C4, C5, C11, C16. C21 should be placed close to chip
2. C5 should be X5R material
3. R6, R7, R8 should be 75 ohm with +/-1%
4. Suggest to connect Pin 29 and Pin 30 to PCH SMBU for debug purpose.
5. This configuration is for internal ROM mode and using embedded LDO mode.
2013/10/18 Change CN21 Pin 8 for TP_PWR rail to S5
2013/10/29 Change CN21 power rail to S5
1A-5 2013/10/18 Change CN21 Pin 8 for
TPD_INT# change Q42 direction and net name,
reserve PS2 PU to +3V.

Prevent ESD/EOS
device

For 15"

Prevent ESD/EOS
device

TOUCHPAD BOARD CONN (TPD I2C/PS2 co-layer)

CPU FAN (THM)

KB_BL LED (KBC)

G-sensor(ACS)
USB Charger to 3.0 (UBC)

USB 3.0 Connector (UB3)

USB2.0 DB (UB2)

USB protection diodes for ESD, as close as possible to USB connector pins.
Double Check ADP-in Type

Double Check BATT-in Type

**V_{ILIM} - 20*(V_{SRP}-V_{SRN}) = 20*I_{chp}*R_{sr}

\[ \text{ILIM} = 0.793V \text{ for 3.965A current limit} \]**

**REGN MAX voltage 6.5V**

**Rsr = 0.01ohm**

**V_{ILIM} = 0.793V**

**War = 0.01ohms**
Power auto recovery

TDC : 3.38A
PEAK : 4.5A
Width : 140mI

TDC : 3.6A
PEAK : 4.8A
Width : 140mI

TDC : 1.65A
PEAK : 2.2A
Width : 80mI

TDC : 3.15A
PEAK : 4.2A
Width : 140mI

Soft-Start

Soft-Start

Rds(on)=4.9m ohm

R(Ilim)=(61.252mV*8)/10uA
~49K
TDC : 0.45A
PEAK : 0.6A
Width : 20mil

TDC : 0.38A
PEAK : 0.5A
Width : 20mil

Rds(on)=14.5mohm

Fsw=500KHz

OCP=9A
L ripple current
=19.1*(2.246/2)*14.5mohm
=114.202mA
Rlim=114.202mA/V5mA*10=228.4Kohm

remove +2.5VSUS Power circuit 5/2
VCORE

VCORE = 1 Phase for U22，不使
VCORE = 2 Phase for U42，使用

VCCGT

DCR=0.66mOhm

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Thermal protection

Vo = 0.6*(R1+R2)/R2 = 1.8V

Vo = 0.6*(1+R1/R2) = 1.5V

Need fine tune for thermal protect point

Note placement position

TEMP=85C

For EC control thermal protection (output 3.3V)
N16S-GTR (23W/GDDR5)
OpenVreg Config : B
Vboot : 0.9V
- EDP-C: 4.2A
- EDP-P: 6.8A
- OCP: 12A
- FSW: 400KHz

N17S-G1 (23W/GDDR5)
OpenVreg Config : Type2+
Vboot : 0.8V
- EDP-C: 4.6A
- EDP-P: TBD (預估TDC*1.5=7A)
- OCP: 12A
- FSW: 400KHz

Remove N16 controlled Pin 02/06

For N17 1.35VFX Sense (reference ZGL) page 15

Rds(on)=5mohm(MAX)
VGA power up sequence

All 3.3V includes all rails powered at 3.3V
-ProVDD 1.05V includes all rails that are shared

Notes: -All 3.3V includes all rails powered at 3.3V
-ProVDD 1.05V includes all rails that are shared

VGA Reset

I/O 3.3V
PEX_RST

PEX_RST timing

Quit >> bus

YFall <0.5mS
<table>
<thead>
<tr>
<th>Stage</th>
<th>Date</th>
<th>Change Description</th>
</tr>
</thead>
</table>
| A     | 02/06  | 1. change net LSP050 to T/P050 (reference E3) page 95:   page 95  
2. change 5nF value from 0.1u to 1uF: page 6  
3. change 85 value from 0.06 to 0.015: page 5  
4. Add Q030 to Q031: level shifter for LSP: page 17  
5. LFX CL1 is defined to FRB05 to N7/F0514 and P7/F0515: page 17  
6. Add D0316A to LFX0316: support to anti-backlash drive: page 17  
7. add 10uF, 10uF, 10uF for R1 and 15uF, 15uF for R5: page 5  
8. change Q8086 from D0314G0130 to P0010: page 36  
9. Reserve S04 controlled Pin NC and change PR0089 from 0.06 to 0.06, change PR0122 from 0.06 to 0.06: page 35  
10. Reserve R05 and last Revision page 17  
11. R076 & R078 change from 10K to 0.01: page 59  
12. reserve R059 page 13  
13. R05 change from 0.06 to 0.06: page 17  
14. Add RR0111 to LFX0111 for P50: page 17  
15. VFBV 1:4 from VCCR 8, VCCR 91 to LFX0125: page 17  
16. Change B880 from N7/F0816850H8526 to N7/F0816850H8526 and add R1120 from 0.06 to N01 POWER & R11221 from 0.06 to N01 POWER: page 16  
17. Change Q0817 from source to net page 14  
18. Change R0017 from 0.06 to 0.06: page 50  
19. Staff R046 page 4  |
| A     | 02/07  | 1. Change PR0095 from 0.06 to 0.06: page 57  
2. Add PR0096 at Pin (D030) page 56  
3. Change R207 from 0.06 to 0.06: page 17  
4. Change Q8087 from 0.06 to N01 POWER & R1100 page 16  
5. Change U170 to D00000: page 16  
6. Reserve R055 page 17  
7. Reserve P095 page 50  
8. Add R01117 and R01115 to Q030: Page 17  
9. RFBV 12 connect: 0V, VCCR 8, VCCR 91: all hant R1125: page 59  
10. Change B880 from N7/F0816850H8526 to N7/F0816850H8526 and add R1120 from 0.06 to N01 POWER & R11221 from 0.06 to N01 POWER: page 16  
11. Change Q0817 from source to net page 14  
12. Change PR0097, PR0098, PR0099, PR0100 from 0.06 to 0.06: page 53, 53  |
| A     | 02/08  | 1. Update S07 & S08 spare pin 0.069 page 17  |
| A     | 02/09  | 1. E09 S07 & S07 reserve a 0.00 pin pull-up to +0.01: power rail for N7/F095 page 16  
2. David D00000 for N7/F095 page 17  
3. Reserve PR035 for N135 and N130 page 51  
4. Reserve R034 for N135: page 51  
5. Connect R035 for N135: page 51  
6. Connect R034 for N135: page 51  
7. add GPIO1 (not sure +0.00, N8, N3, N0, N14, N15): page 57  
8. change D0012 page 17  
9. RFBV 12 from 0.00 to 0.00: Page 17  
10. Change L000 from +3V/0.00 to +3V/0.00 page 50, 53  |
| A     | 02/10  | 1. Add PR0010 page 50  
2. Reserve R0001: page 50  
3. Add PR0011 page 50  
4. Reserve R0012 page 15  |
| A     | 02/11  | 1. Add C9093 page 30  
2. Reserve D4016 page 22  
3. Double check R781 from 0.00 to 0.00: page 77 (keep 20K, -10%)  
4. Reserve C170 page 7  
5. David D00000 for N01 (N7*S7) page 17  
6. Staff R0001 page 06  
7. change pull-up [R0096] from 0.06 to 0.06: page 20  
8. Add 0001 and 0002 page 22  |

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PROJECT - ZAAR  

CHANGE LIST
<table>
<thead>
<tr>
<th>Stage</th>
<th>Date</th>
<th>Change List</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>02/14</td>
<td>1. Remove TP4392, TP4393, TP4394, TP4392 page 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2. Remove R762 and TP96 page 9</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3. Remove C9094 and PR67002 page 9</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4. Add VHF1 [Yellow B0C] page 9</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5. Change Q207, R2021, R2023, R2037 from N16@ to N16@ page 14</td>
</tr>
<tr>
<td></td>
<td></td>
<td>6. Change R9287 from N16@ to N16@ page 17</td>
</tr>
<tr>
<td></td>
<td></td>
<td>7. Install TP9300 page 9</td>
</tr>
<tr>
<td></td>
<td>02/15</td>
<td>1. Remove TP20 page 9</td>
</tr>
<tr>
<td></td>
<td>02/16</td>
<td>1. Remove TP16 page 5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2. Change U4509 from BC104308Z00 [AZ1043-08F.R7G(3.3V)] to BC104508Z00 [AZ1045-08F.R7G (5V)] page 19</td>
</tr>
<tr>
<td></td>
<td>02/17</td>
<td>1. Change SW4 footprint from sw-ds-a40e-4p to sw-ds-a40e-4p-smt page 19</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2. Add C9095 [Follow SPEC] page 9</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3. Change Q8027, R8204, R8223, R8220, C8327 from EV@ to N16@ page 16</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4. Change R8247 from N16@ to EV@ page 17</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5. Unstuff PR9018 page 9</td>
</tr>
<tr>
<td></td>
<td>05/08</td>
<td>1. Stuff R125 &amp; R69 &amp; R89 for power request</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2. Change R597 from 49.9k to 40.2k for N16</td>
</tr>
<tr>
<td>C</td>
<td>05/11</td>
<td>1. Change Vcore enable pin from 3V_MAIN_EN to 1.8_GFX_MAIN for matching N17 sequence</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2. Change PR289 to 1K and PC89 to 0.22uf for matching N16 sequence</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3. Change PQ89083 type from PQ89083 to PQ89084 type for VGA waveform 2 steps problem</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4. Stuff R255 for VGA waveform problem</td>
</tr>
<tr>
<td>RAMP</td>
<td>06/07</td>
<td>1. Change Vcore enable pin from 3V_MAIN_EN to 1.8_GFX_MAIN for matching N17 sequence</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2. Change PR289 to 1K and PC89 to 0.22uf for matching N16 sequence</td>
</tr>
</tbody>
</table>

**Notes:**
- Change list - 2/2
- Monday, June 19, 2017
- ZAAR
- Quanta Computer Inc.