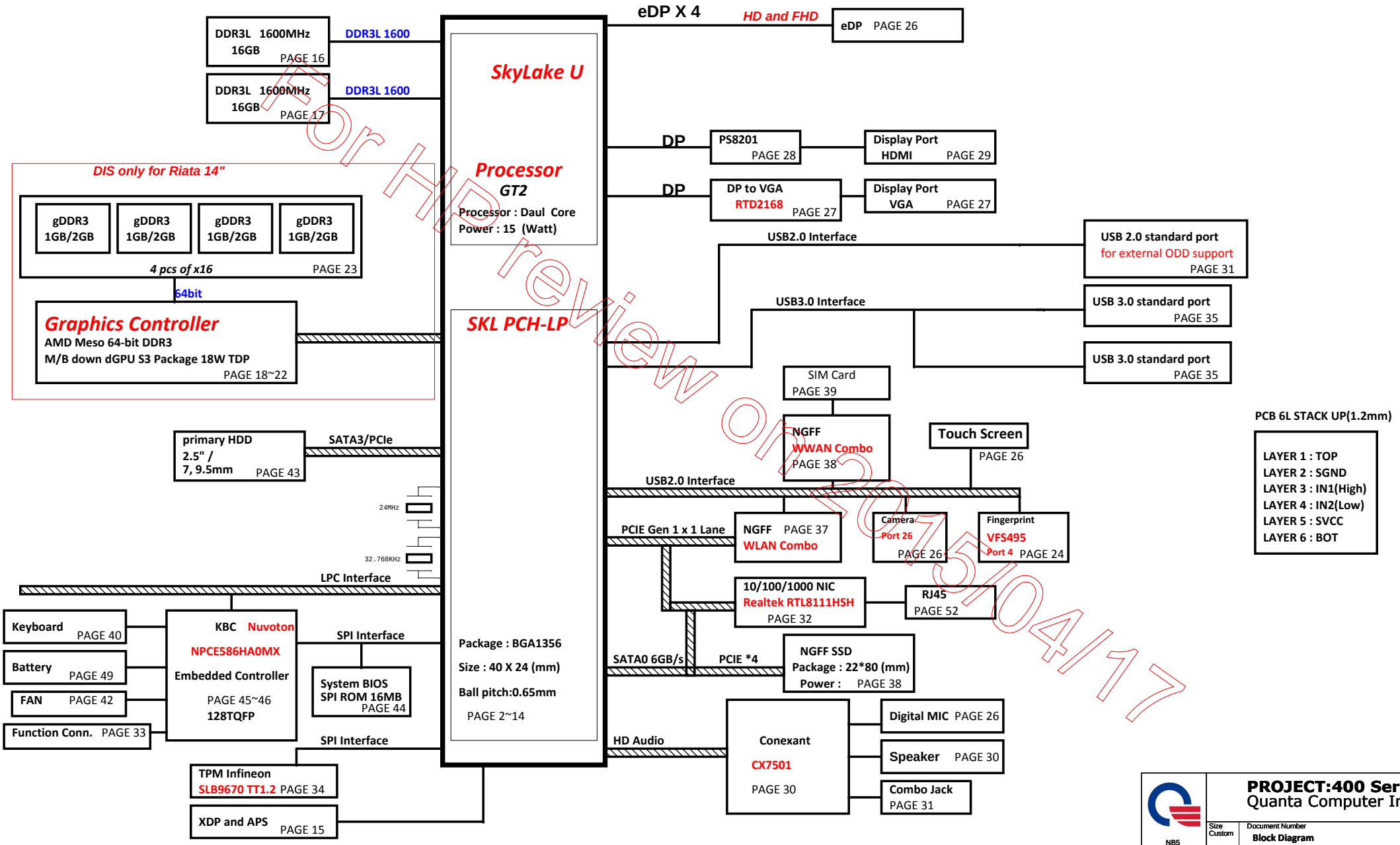
Royal 13"/Riata 14" SkyLake -U (UMA/DIS) Schematics

01



For Hp review on 2015/04/17

NB5

PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	1A

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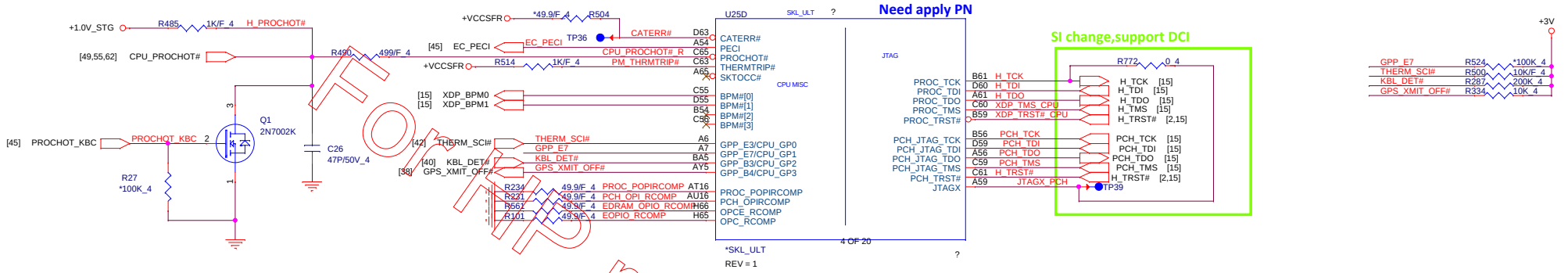
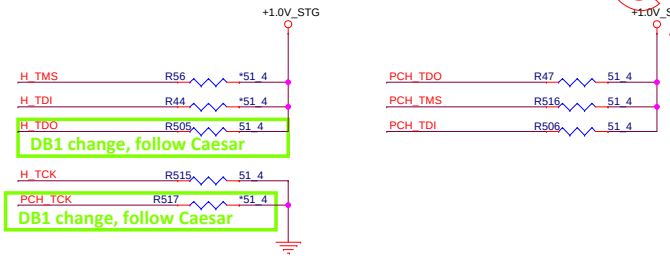


Processor pull-up (CPU)



+1.0V_STG [11,13]
+VCCSFR [3,9,11,13,45]
+3V [3,4,5,7,8,9,10,15,16,17,24,26,27,28,30,31,32,33,36,38,42,44,45,49,55,57,63]

TOP review on 2015/04/17

PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	02 -- SKYLAKE 2/20(MISC/ JTAG)	1A

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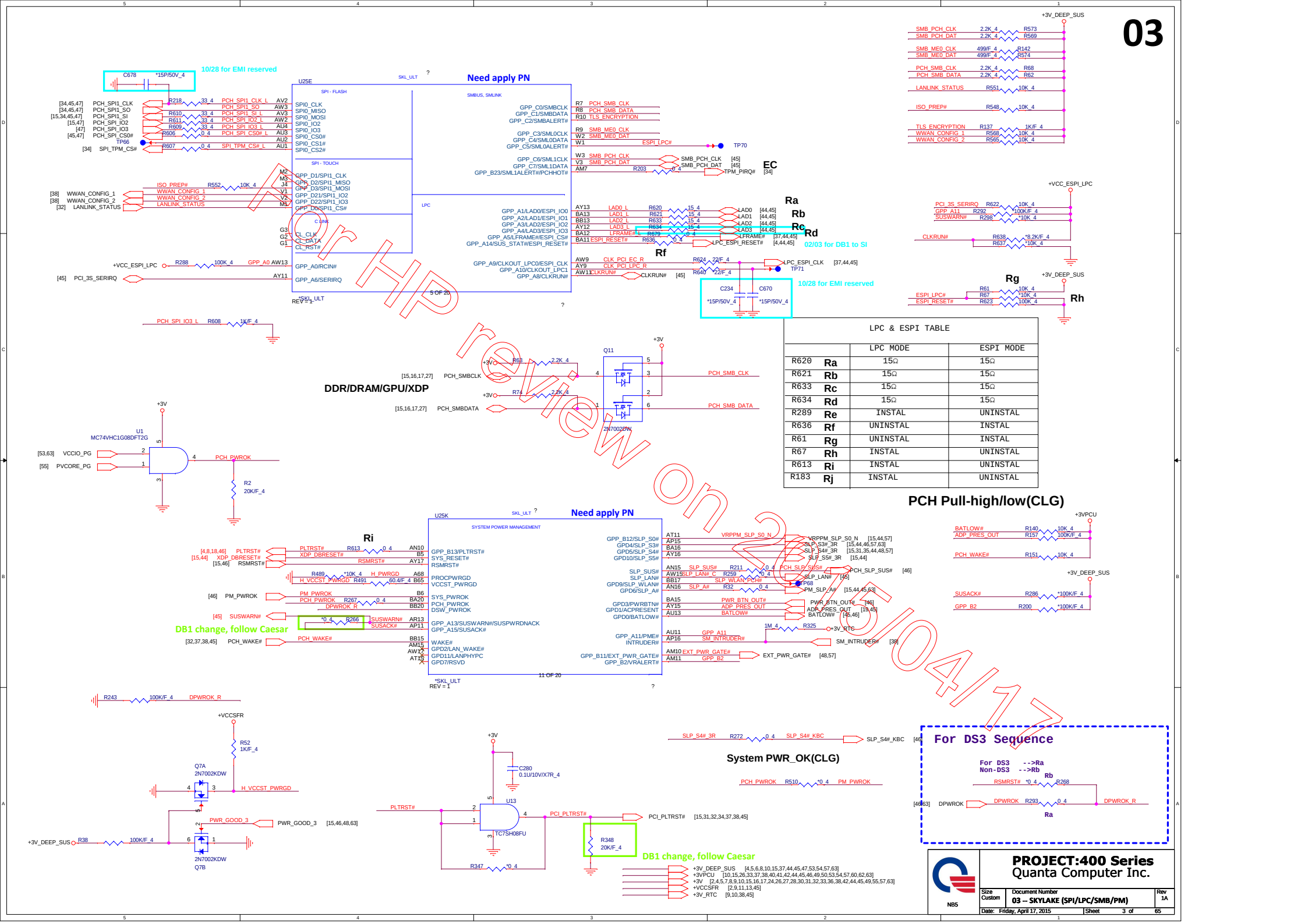
NB5



For Review on 2015/04/17

Skylake (GPIO)

04

Need apply PN

U25F — SKL_ULT ?

LPSS

NFC_DWL_REQ	AN8	GPP_B15/GSPI0_CS#
TP26 GPP_B16	AP7	GPP_B16/GSPI0_CLK
[31] CR_RST# CR_RST#	AP8	GPP_B17/GSPI0_MISO
NFC_FW_RESET	AR7	GPP_B18/GSPI0_MOSI
[26] CAMERA_ON CAMERA_ON	AM5	GPP_B19/GSPI1_CS#
[46] NMI_SMI_DBG# NMI_SMI_DBG#	AN7	GPP_B20/GSPI1_CLK
NFC_HOST_INT	AP5	GPP_B21/GSPI1_MISO
BOOT_SPI#	AN5	GPP_B22/GSPI1_MOSI
[44] UART0_RXD UART0_RXD	AB1	GPP_C8/UART0_RXD
[44] UART0_TXD UART0_TXD	AB2	GPP_C9/UART0_TXD
[24] FPR_LOCK# FPR_LOCK#	W4	GPP_C10/UART0_RTS#
TP19 UART0_CTS#	AB3	GPP_C11/UART0_CTS#
[24] FPR_OFF FPR_OFF	AD1	
[31] HDD_HALTLED HDD_HALTLED R167 1K/F_4	AD2	GPP_C20/UART2_RXD
[36] ACCEL_INT ACCEL_INT	AD3	GPP_C21/UART2_TXD
RUNSCI_EC#	AD4	GPP_C22/UART2_RTS#
		GPP_C23/UART2_CTS#
TP13 GPP_C16	U7	GPP_C16/I2C0_SDA
TP14 GPP_C17	U6	GPP_C17/I2C0_SCL
[3,44,45] LPC_ESPI_RESET# R289 *0_4	U8	
TP15 GPP_C19	U9	GPP_C18/I2C1_SDA
		GPP_C19/I2C1_SCL
	AH9	
	AH10	GPP_F5/I2C2_SCL
	AH11	
	AH12	GPP_F7/I2C3_SCL
GPP_F8	AF11	GPP_F8/I2C4_SDA
TP20 GPP_F9	AF12	GPP_F9/I2C4_SCL

ISH

P2 WWAN_TRANSMIT_OFF#		WWAN_TRANSMIT_OFF# [33,38]
GPP_D9 P3 GPP_D10		TP51
GPP_D10 P4 CR_PWREN#		CR_PWREN# [31]
GPP_D11 P1 BT_OFF		BT_OFF [37]
GPP_D12		
	M4	
GPP_D5/ISH_I2C0_SDA	N3	
GPP_D6/ISH_I2C0_SCL		
	N1	
GPP_D7/ISH_I2C1_SDA	N2	
GPP_D8/ISH_I2C1_SCL		
	AD11 GPP_F10	
GPP_F10/I2C5_SDA/ISH_I2C2_SDA	AD12 GPP_F11	TP18
GPP_F11/I2C5_SCL/ISH_I2C2_SCL		
	U1 GPP_D13	TP55
GPP_D13/ISH_UART0_RXD/SML0BDATA/I2C4B_SDA	U2 GPP_D14	
GPP_D14/ISH_UART0_TXD/SML0BCLK/I2C4B_SCL	U3 MPHY_PWREN	MPHY_PWREN [57]
GPP_D15/ISH_UART0_RTS#	U4 WWANSSD_M2	WWANSSD_M2 [38]
GPP_D16/ISH_UART0_CTS#/SML0BALERT#		
	AC1 PCH_LAN_RST#	
GPP_C12/UART1_RXD/ISH_UART1_RXD	AC2 PCH_WLAN_RST#	
GPP_C13/UART1_TXD/ISH_UART1_TXD	AC3 PCH_SLP_S0IX#	PCH_SLP_S0IX# [45]
GPP_C14/UART1_RTS#/ISH_UART1_RTS#	AB4 GPP_C15	TP60
GPP_C15/UART1_CTS#/ISH_UART1_CTS#		
	AY8 GPP_A18	
GPP_A18/ISH_GP0	BA8 GPP_A19	
GPP_A19/ISH_GP1	BB7 GPP_A20 R780 *100K/F_4	+3V
GPP_A20/ISH_GP2	BA7 R779 100K/F_4	
GPP_A21/ISH_GP3	AY7	
GPP_A22/ISH_GP4	AW7	
GPP_A23/ISH_GP5	AP13 ISH_GP6 R304 0_4	SX_EXIT_HOLDOFF# [45]
GPP_A12/BM_BUSY#/ISH_GP6		

6 OF 20

*SKL_ULT
REV = 1

?

Re

Ra

Rb

Rc

Rd

[3,8,18,46] PLTRST# — PLTRST# R204 *0_4 — R199 *0_4 RUNSCI_EC#

[45] RUNSCI_EC#_R

WWAN & TS TABLE		
	WWAN MODE	TS MODE
Rc	INSTAL	UNINSTAL
Rd	UNINSTAL	INSTAL

LPC & ESPI TABLE		
	LPC MODE	ESPI MODE
Ra	UNINSTAL	INSTAL
Rb	INSTAL	UNINSTAL

GPIO Pull-up/Pull-down(CLG)

11/05 for intel check list

+3V_DEEP_SUS

R285	10K_4	
BT_OFF	R555	*10K_4
WWAN_TRANSMIT_OFF#	R556	100K/F_4
CR_PWREN#	R284	*10K_4
GPP_D13	R563	100K/F_4
WWANSSD_M2	R566	10K_4
NFC_DWL_REQ	R206	*100K_4
PCH_LAN_RST#	R583	100K/F_4
PCH_WLAN_RST#	R582	100K/F_4
GPP_D14	R560	100K/F_4

+3V

RUNSCI_EC#	R183	*10K_4
CR_RST#	R282	10K_4
FPR_OFF	R184	10K_4
PCH_SLP_S0IX#	R581	100K_4
NFC_FW_RESET	R290	10K_4
CAMERA_ON	R14	10K_4
NMI_SMI_DBG#	R612	10K_4
MPHY_PWREN	R562	10K_4
ACCEL_INT	R359	8.2K/F_4
HDD_HALTLED	R350	10K_4

+VCC_ESPI_LPC

GPP_A18	R629	*100K/F_4
GPP_A19	R625	*100K/F_4
ISH_GP6	R305	*100K/F_4

+1.8V

GPP_F8	R191	*100K_4
GPP_F10	R190	*100K_4

BOOT_SPI#	R202	10K_4
NFC_DWL_REQ	R207	100K_4
NFC_HOST_INT	R201	10K_4
MPHY_PWREN	R480	*10K_4

[2,3,5,7,8,9,10,15,16,17,24,26,27,28,30,31,32,33,36,38,42,44,45,49,55,57,63] +3V

Quanta review on 2015/04/17

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PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	04 – SKYLAKE (GPIO)	1A
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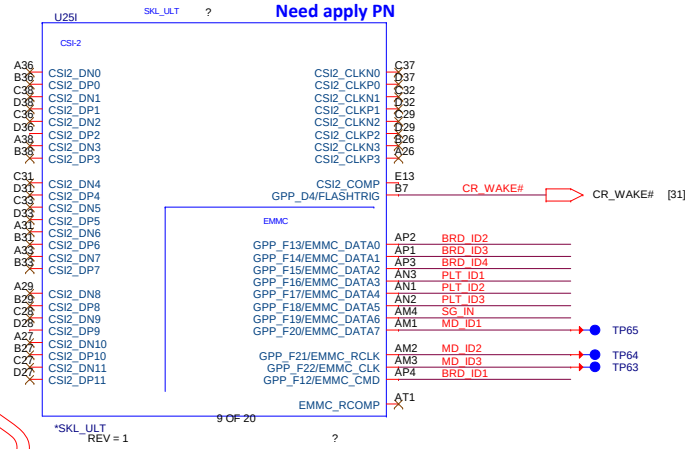
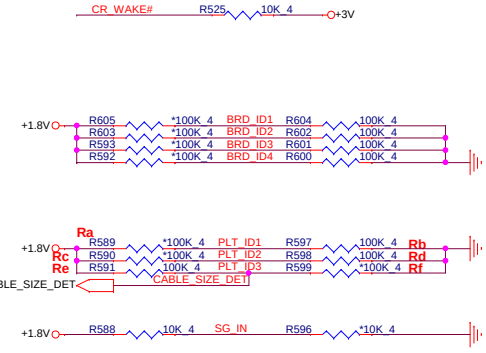
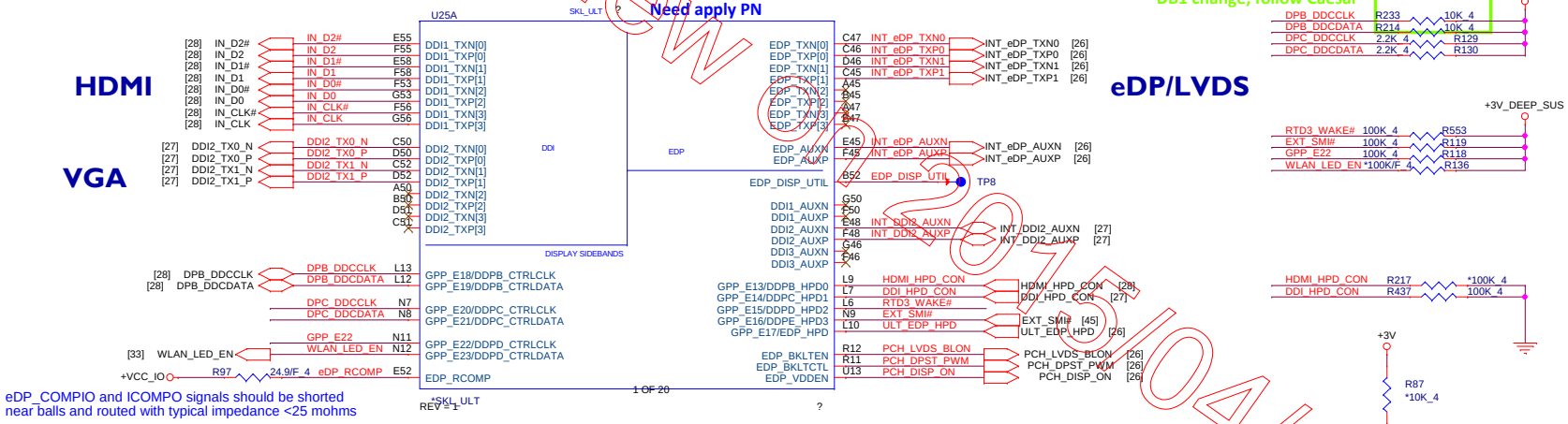
	BRD_ID1	BRD_ID2	BRD_ID3	BRD_ID4	
	GPIO201	GPIO202	GPIO203	GPIO204	AMD_FCH
	GPIO14	GPIO34	GPIO35	GPIO40	PPMT
	GPIO15	GPIO34	GPIO35	GPIO40	LPI-H
BOARD REVISION	GPIO76	GPIO77	GPIO78	GPIO79	LPT-LP
DB0	0	0	0	0	
DB1	0	0	0	1	
DB2	0	0	1	0	
	0	0	1	1	
SI1	0	1	0	0	
SIB	0	1	0	1	
SI2	0	1	1	0	
	0	1	1	1	
PV1	1	0	0	0	
	1	0	0	1	
	1	0	1	0	
	1	0	1	1	
MV1	1	1	0	0	
	1	1	0	1	
	1	1	1	0	
	1	1	1	1	



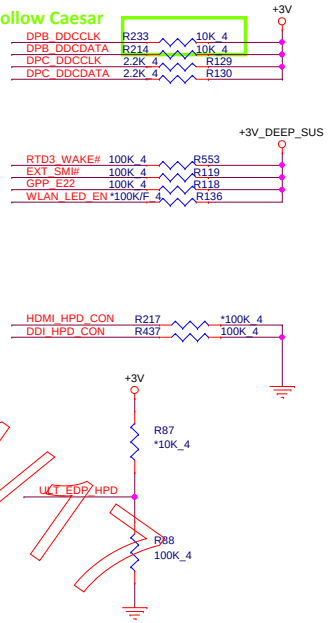


PLT_ID1	PLT_ID2	PLT_ID3	
Ra	Rc	Re	H
Rb	Rd	Rf	L
0	0	0	13.3"
0	0	1	14"
0	1	0	15.6"
0	1	1	17.3"

SG_IN	SG_IN
UNINSTAL	R588
UMA	DIS



eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms



For HP review only 2015/04/17

NB5

PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	05 -- SKYLAKE (eDP/DDI/Board ID)	1A
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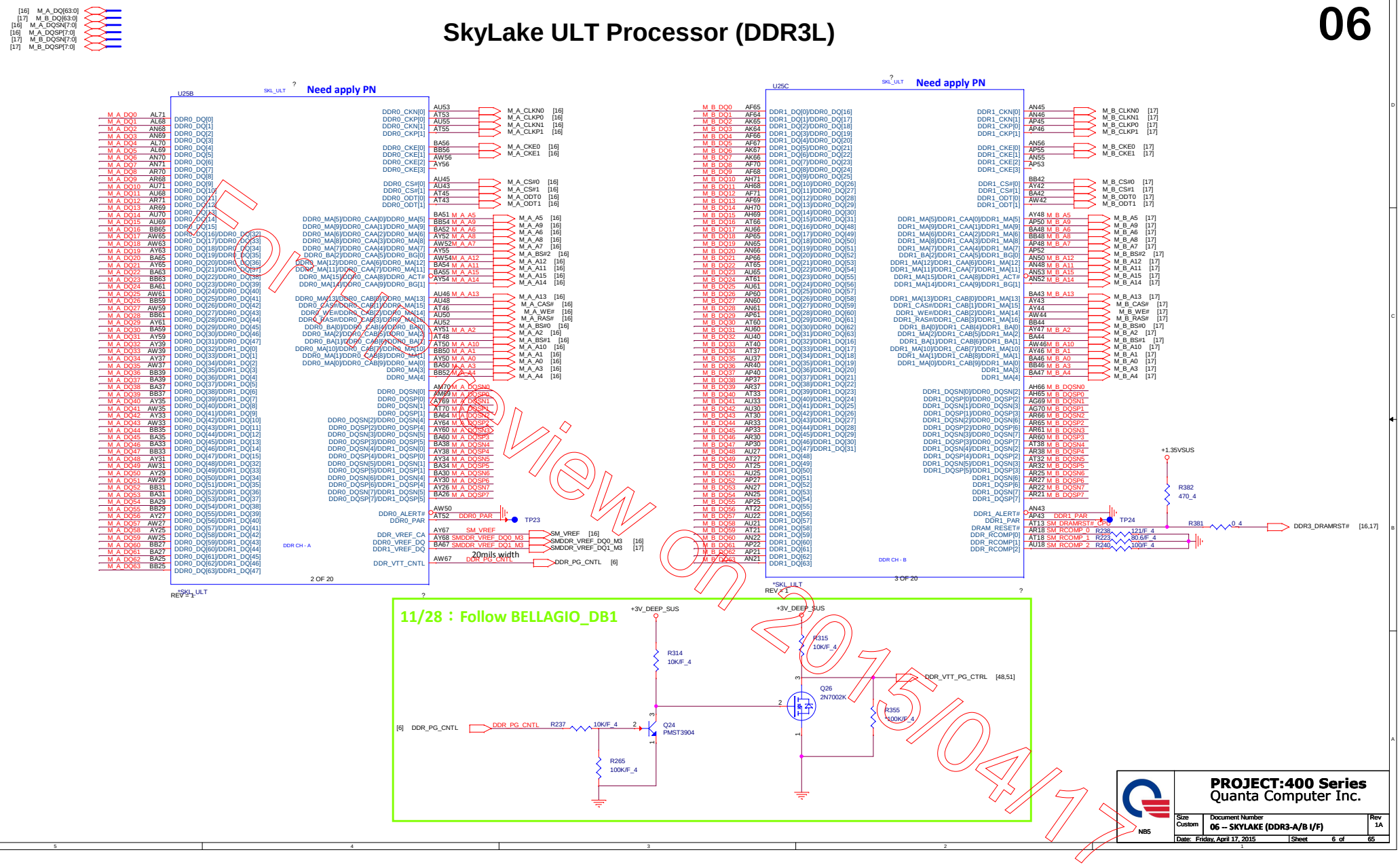
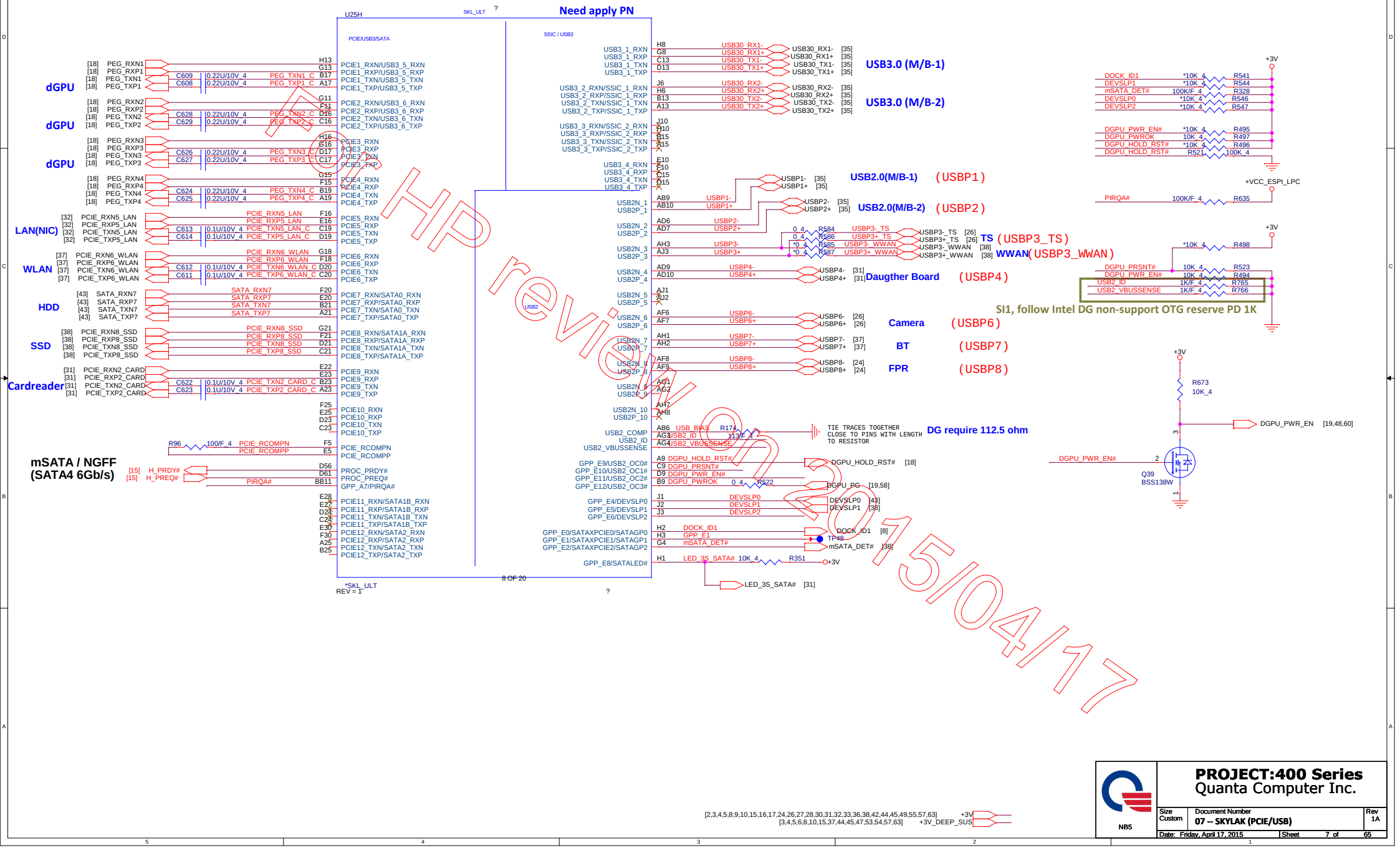
SkyLake ULT Processor (DDR3L)

06



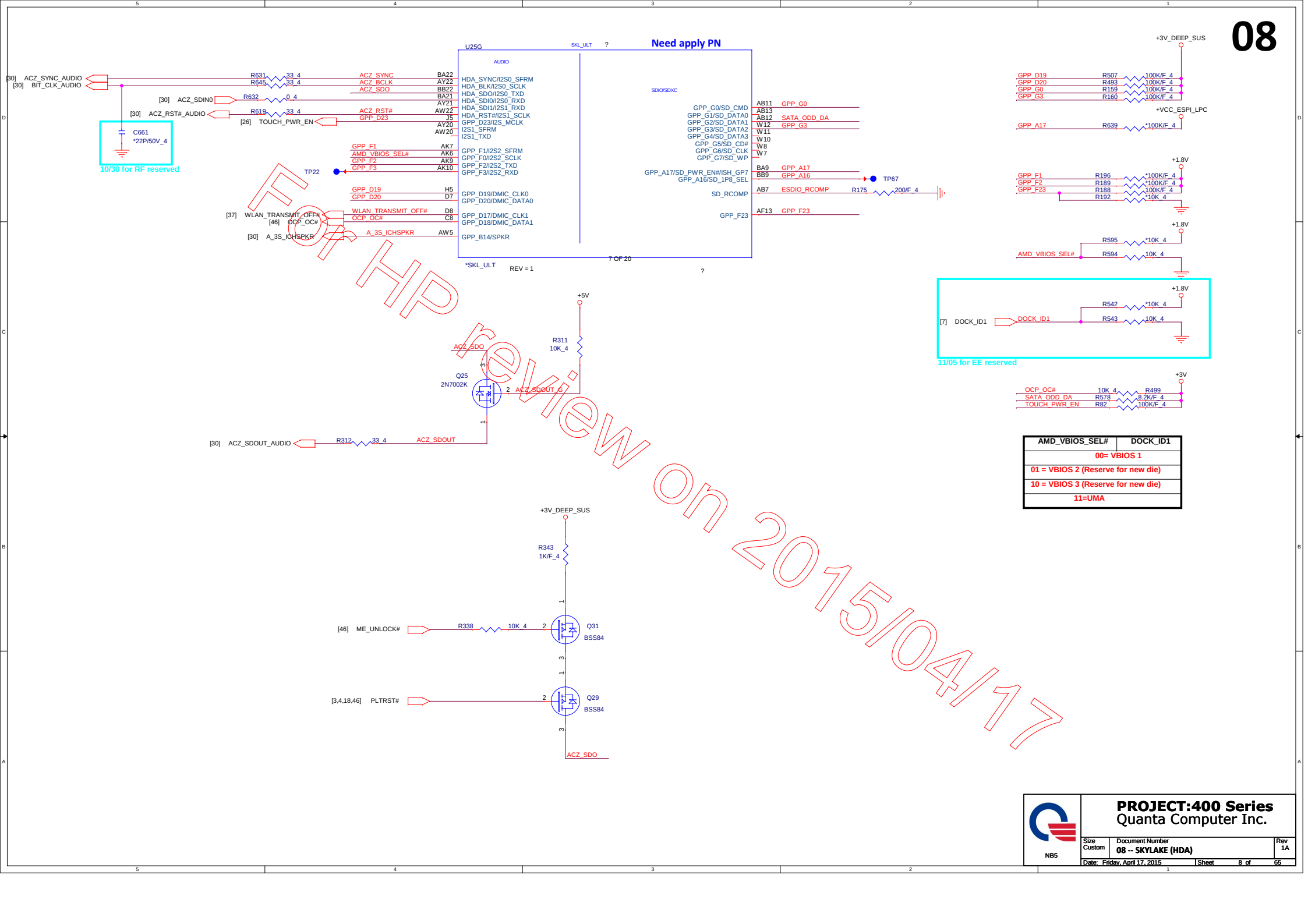
Review on 2015/04/17

NB5	**PROJECT:400 Series** Quanta Computer Inc.	
Size: Custom	Document Number: 06 -- SKYLAKE (DDR3-A/B I/F)	Rev: 1A
Date: Friday, April 17, 2015	Sheet 6 of 65	



HP review on 2015/04/17

PROJECT:	400 Series
Quanta Computer Inc.	
Size: Custom	Document Number: 07 -- SKYLAK (PCIE/USB)
Rev:	1A
NB5	
Date: Friday, April 17, 2015	Sheet 7 of 65



AMD_VBIOS_SEL#	DOCK_ID1
00= VBIOS 1	
01 = VBIOS 2 (Reserve for new die)	
10 = VBIOS 3 (Reserve for new die)	
11=UMA	

FOR HP review on 2015/04/17

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PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	08 -- SKYLAKE (HDA)	1A

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TBT

RTC Clock 32.768KHz

C402 8.2P/50V_4 — Y2 32.768KHz — C394 8.2P/50V_4

RTC_X1 — R319 10M_4 — RTC_X2

11/10 for 2nd reserved

TP41 — C631 10P/50V_4 — XTAL24_IN — R509 1M_4 — 24MHZ +-30PPM Y4 — XTAL24_OUT — C632 10P/50V_4 — TP42

SI Modify by vendor

RTC Circuitry(RTC)

PV, 0413 add R795, R794 to prevent RTC power over +3.2V

+3V_ALW — R795 1.5K/_4 — R794 47K/F_4

30mils

+3V_RTC_0 — R180 1K/F_4 — +3V_RTC_2 — D8 BAT54C — +3V_RTC

CN20 BAT_CONN DFHS02FS058 BAT-23_2-4_2

RTC Power trace width 20mils.

+3V_RTC — R228 20K/F_4 — RTC_RST# — RTC_RST# [15,44]

+3V_RTC — R661 20K/F_4 — SRTC_RST#

C328 1U/6.3V_4

C306 1U/6.3V_4

C673 1U/6.3V_4

CFG4 R550 1K/F_4

CFG9 R557 *1K/F_4

+VCCSFR [2,3,11,13,45]
+1.0V_DEEP_SUS [10,15,52,53,54,57]
+3V [2,3,4,5,7,8,10,15,16,17,24,26,27,28,30,31,32,33,36,38,42,44,45,49,55,57,63]

Cardreader: [31] CLK_PCIE_CRN, [31] CLK_PCIE_CRP, [31] PCIE_CLKREQ_CR# → CLK_PCIE_CRN, CLK_PCIE_CRP, PCIE_CLKREQ_CR#

LAN: [32] CLK_PCIE_LANN, [32] CLK_PCIE_LANP, [32] PCIE_CLKREQ_LAN# → CLK_PCIE_LANN, CLK_PCIE_LANP, PCIE_CLKREQ_LAN#

WLAN: [37] CLK_PCIE_WLANN, [37] CLK_PCIE_WLANP, [37] PCIE_CLKREQ_WLAN# → CLK_PCIE_WLANN, CLK_PCIE_WLANP, PCIE_CLKREQ_WLAN#

dGPU: [18] CLK_GFX_N, [18] CLK_GFX_P, [19] PCIE_REQ_GPU# → CLK_GFX_N, CLK_GFX_P, PCIE_REQ_GPU#

PCIE_CLKREQ_SSD# → PCIE_CLKREQ5#

11/06 for RF reserved

C25 *10P/50V_4 R10 *0_4 — CLK_PCIE_LANN, CLK_PCIE_LANP

11/06 for RF reserved

C23 *10P/50V_4 R9 *0_4

U25J SKL_ULT — Need apply PN

CLOCK SIGNALS

CLKOUT_PCIE_N0 (D42) / CLKOUT_PCIE_P0 (C42) / GPP_B5/SRCCLKREQ0# (AR10)
CLKOUT_PCIE_N1 (B42) / CLKOUT_PCIE_P1 (A42) / GPP_B6/SRCCLKREQ1# (AT7)
CLKOUT_PCIE_N2 (D41) / CLKOUT_PCIE_P2 (C41) / GPP_B7/SRCCLKREQ2# (AT8)
CLKOUT_PCIE_N3 (D40) / CLKOUT_PCIE_P3 (C40) / GPP_B8/SRCCLKREQ3# (AT10)
CLKOUT_PCIE_N4 (B40) / CLKOUT_PCIE_P4 (A40) / GPP_B9/SRCCLKREQ4# (AU8)
CLKOUT_PCIE_N5 (E40) / CLKOUT_PCIE_P5 (E39) / GPP_B10/SRCCLKREQ5# (AU7)

CLKOUT_ITPXDP_N (F43) CK_XDP_N_R
CLKOUT_ITPXDP_P (E43) CK_XDP_P_R
GPD8/SUSCLK (BA17) SUSCLK32_KBC [46] TO KBC
XTAL24_IN (E37) XTAL24_IN
XTAL24_OUT (E35) XTAL24_OUT
XCLK_BIASREF (E42) XCLK_BIASREF — R117 2.7K/F_4 — +1.0V_DEEP_SUS
RTCX1 (AM18) RTC_X1
RTCX2 (AM20) RTC_X2
SRTCRST# (AN18) SRTC_RST#
RTCRST# (AM16) RTC_RST# — RTC_RST# [15,44]

RP1 install for XDP

RP1 0_4P2R_4: 2/4 — 1/3 — CK_XDP_N [15], CK_XDP_P [15]

*SKL_ULT REV = 1

10 OF 20

CLK_REQ/Strap Pin(CLG)

+3V

PCIE_REQ_GPU# R241 10K_4
PCIE_CLKREQ5# R291 10K_4
PCIE_CLKREQ_WLAN# R229 10K_4
PCIE_CLKREQ_LAN# R260 10K_4
PCIE_CLKREQ_CR# R262 10K_4
PCIE_CLKREQ_SSD# R242 10K_4

CFG0-19 need Reserve TP

U25S SKL_ULT — Need apply PN

RESERVED SIGNALS-1

CFG[0] (E68) … CFG[19] (G70)
CFG_RCOMP (E60) — R86 49.9/F_4
ITP_PMODE (E8) — +1.0V_DEEP_SUS — R520 1.5K_4 — [15] ITP_PMODE

RSVD_AY2 (AY2) / RSVD_AY1 (AY1)
RSVD_D1 (D1) / RSVD_D3 (D3)
RSVD_K46 (K46) / RSVD_K45 (K45)
RSVD_AL25 (AL25) / RSVD_AL27 (AL27)
RSVD_C71 (C71) / RSVD_B70 (B70)
RSVD_F60 (F60)
RSVD_A52 (A52)
RSVD_TP_BA70 (BA70) / RSVD_TP_BA68 (BA68)
RSVD_J71 (J71) / RSVD_J68 (J68)
VSS_F65 (F65) / VSS_G65 (G65)
RSVD_F61 (F61) / RSVD_E61 (E61)

RSVD_TP_BB68 (BB68) / RSVD_TP_BB69 (BB69)
RSVD_TP_AK13 (AK13) / RSVD_TP_AK12 (AK12)
RSVD_BB2 (BB2) / RSVD_BA3 (BA3)
TP5 (AU5) / TP6 (AT5)
RSVD_D5 (D5) / RSVD_D4 (D4) / RSVD_B2 (B2) / RSVD_C2 (C2)
RSVD_B3 (B3) / RSVD_A3 (A3)
RSVD_AW1 (AW1)
RSVD_E1 (E1) / RSVD_E2 (E2)
RSVD_BA4 (BA4) / RSVD_BB4 (BB4)
RSVD_A4 (A4) / RSVD_C4 (C4)
TP4 (BB5)
RSVD_A69 (A69) / RSVD_B69 (B69)
RSVD_AY3 (AY3)
RSVD_D71 (D71) / RSVD_C70 (C70)
RSVD_C54 (C54) / RSVD_D54 (D54)
TP1 (AY4) / TP2 (BB3)
VSS_AY71 (AY71) / ZVM# (AR56)
RSVD_TP_AW71 (AW71) / RSVD_TP_AW70 (AW70)
MSM# (AP56) / PROC_SELECT# (C64) — R508 *100K_4 — +VCCSFR

*SKL_ULT REV = 1

19 OF 20

+1.8V_DEEP_SUS

U25T SKL_ULT — Need apply PN

SPARE

AW69 RSVD_AW69 — RSVD_F6 (F6)
AW68 RSVD_AW68 — RSVD_E3 (E3)
AU56 RSVD_AU56 — RSVD_C11 (C11)
AW48 RSVD_AW48 — RSVD_B11 (B11)
C7 RSVD_C7 — RSVD_A11 (A11)
U12 RSVD_U12 — RSVD_D12 (D12)
U11 RSVD_U11 — RSVD_C12 (C12)
H11 RSVD_H11 — RSVD_F52 (F52)

*SKL_ULT REV = 1

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For KBC on 20150417

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PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	09 -- SKYLAKE (CLK/RSV/RTC)	1A
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LPC & ESPI TABLE		
	LPC MODE	ESPI MODE
Ra	INSTAL	UNINSTAL
Rb	UNINSTAL	INSTAL

PCH Internal VRM

Need apply PN

U25O SKL_ULT CPU POWER 4 OF 4

+1.0V_DEEP_SUS +VCCPRIM C578 1U/6.3V_4
+VCC_PRIM C263 1U/6.3V_4 C224 0.1U/16V_4
+VCCDSW_1.0V +VCCDSW_1.0V C651 1U/6.3V_4
+1.0V_DEEP_SUS C198 1U/6.3V_4
+1.0V_MODPHY C604 1U/6.3V_4 C239 1U/6.3V_4 C251 0.1U/16V_4 C216 0.1U/16V_4
+1.0V_DEEP_SUS C233 22U/6.3V_6
+3VPCU R155 0_4 +VCCDSW C265 1U/6.3V_4
+3V C433 1U/6.3V_4
+3V_DEEP_SUS +1.8V_DEEP_SUS R173 0_4 R171 *0_4 +VCCSPI C290 *0.1U/16V_4
+1.0V_MODPHY C606 1U/6.3V_4
+3V_DEEP_SUS C57 1U/6.3V_4
+1.0V_DEEP_SUS C559 *1U/6.3V_6
+1.0V_MODPHY R124 0_6 +VCCAPLLEBB C262 1U/6.3V_4 C603 1U/6.3V_4 C238 0.1U/16V_4 C605 0.1U/16V_4

AB19 AB20 P18	VCCPRIM_1P0 VCCPRIM_1P0 VCCPRIM_1P0	0.696A
AF18 AF19 V20 V21	VCCPRIM_CORE VCCPRIM_CORE VCCPRIM_CORE VCCPRIM_CORE	2.574A
AL1	DCPDSW_1P0	75mA
K17 L1	VCCMPHYAON_1P0 VCCMPHYAON_1P0	22mA
N15 N16 N17 P15 P16	VCCMPHYGT_1P0_N15 VCCMPHYGT_1P0_N16 VCCMPHYGT_1P0_N17 VCCMPHYGT_1P0_P15 VCCMPHYGT_1P0_P16	22mA
K15 L15	VCCAMPHYPLL_1P0 VCCAMPHYPLL_1P0	88mA
V15	VCCAPLL_1P0	26mA
AB17 Y18	VCCPRIM_1P0_AB17 VCCPRIM_1P0_Y18	
AD17 AD18 AJ17	VCCDSW_3P3_AD17 VCCDSW_3P3_AD18 VCCDSW_3P3_AJ17	118mA
AJ19	VCCHDA	68mA
AJ16	VCCSPI	11mA
AF20 AF21 T19 T20	VCCSRAM_1P0 VCCSRAM_1P0 VCCSRAM_1P0 VCCSRAM_1P0	642mA
AJ21	VCCPRIM_3P3_AJ21	
AK20	VCCPRIM_1P0_AK20	
N18	VCCAPLLEBB	33mA

15 OF 20

	VCCPRIM_3P3_V19	20mA
AK15 AG15 Y16 Y15 T16 AF16 AD15	VCCPGPPA VCCPGPPB VCCPGPPC VCCPGPPD VCCPGPPE VCCPGPPF VCCPGPPG	4mA 6mA 8mA 6mA 161mA 41mA
V19	VCCPRIM_3P3_V19	
T1	VCCPRIM_1P0_T1	
AA1	VCCATS_1P8	6mA
AK17	VCCRTCPRIM_3P3	1mA
AK19 BB14	VCCRTC_AK19 VCCRTC_BB14	1mA
BB10	DCPRTC	
A14 K19 L21 N20 L19 A10	VCCCLK1 VCCCLK2 VCCCLK3 VCCCLK4 VCCCLK5 VCCCLK6	35mA 29mA 24mA 33mA 4mA 10mA
AN11 AN13	GPP_B0/CORE_VID0 GPP_B1/CORE_VID1	

*SKL_ULT REV = 1

+VCC_ESPI_LPC +VCC_ESPI_LPC +3V_DEEP_SUS Ra 0_4 R185 R172 Rb +3V_DEEP_SUS +1.8V_DEEP_SUS
+1.8V_DEEP_SUS
+1.0V_DEEP_SUS C558 22U/6.3V_6
+1.8V_DEEP_SUS
+3V_DEEP_SUS C368 1U/6.3V_4 +3V_RTC C401 0.1U/16V_4 C292 1U/6.3V_4
DCPRTC C657 0.1U/16V_4
+1.0V_DEEP_SUS
+VCCCLK1 +VCCCLK2 +VCCCLK3 +VCCCLK4 +VCCCLK5 +VCCCLK6
CORE_VID0 0_4 R409 CORE_VID1 0_4 R407
VID0_VCC_PRIM [54] VID1_VCC_PRIM [54]

DB1 CHANGE

11/05 for intel check list

+3V_DEEP_SUS C274 1U/6.3V_4 C266 0.1U/16V_4

LPC & ESPI TABLE		
	LPC MODE	ESPI MODE
Ra	INSTAL	UNINSTAL
Rb	UNINSTAL	INSTAL

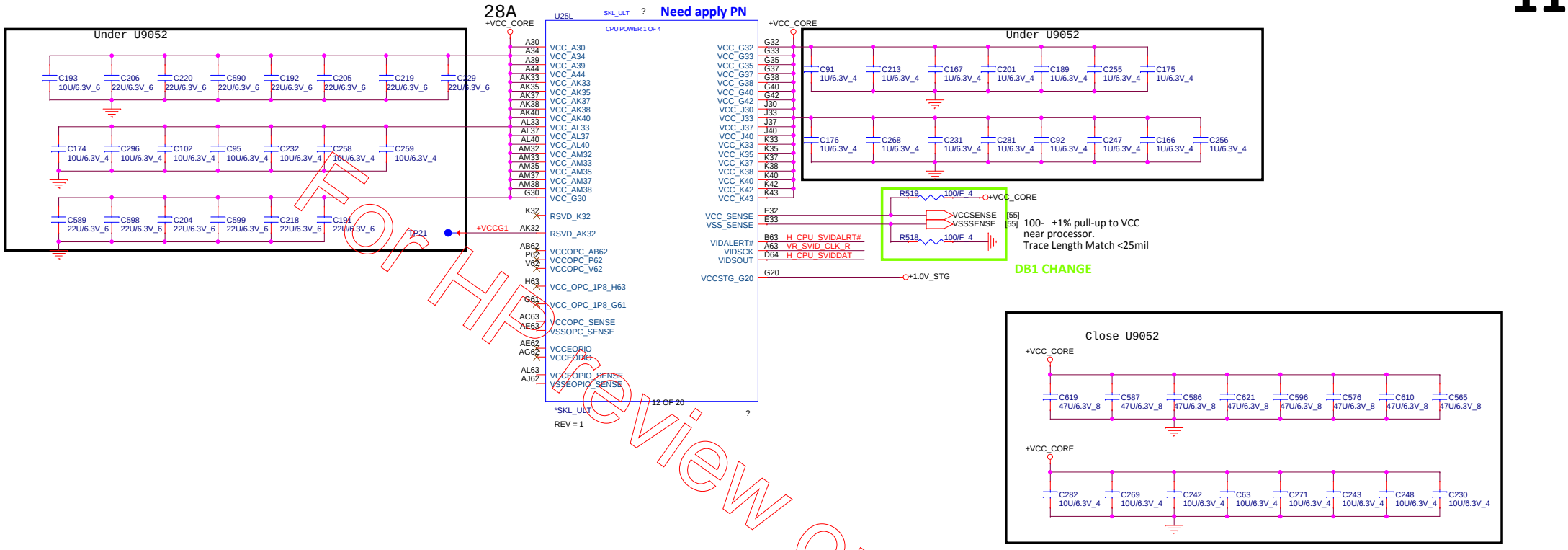
For Review on 2015/04/17

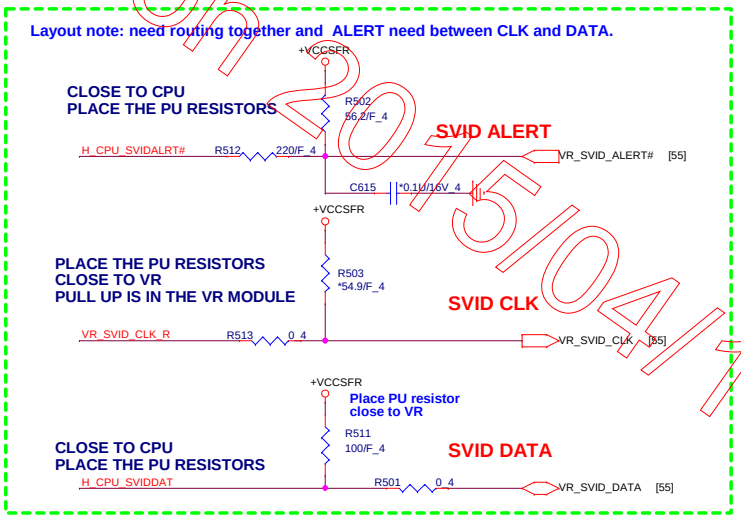
+3V_DEEP_SUS [3,4,5,6,8,15,37,44,45,47,53,54,57,63]
+3VPCU [3,15,26,33,37,38,40,41,42,44,45,46,49,50,53,54,57,60,62,63]
+1.0V_DEEP_SUS [9,15,52,53,54,57]
+VCC_PRIM [25,54]
+3V [2,3,4,5,7,8,9,15,16,17,24,26,27,28,30,31,32,33,36,38,42,44,45,49,55,57,63]
+1.8V_DEEP_SUS [9,45,47,52,63]

NB5

PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	10 -- SKYLAKE (PCH POWER)	1A
Date: Friday, April 17, 2015	Sheet 10 of 65	

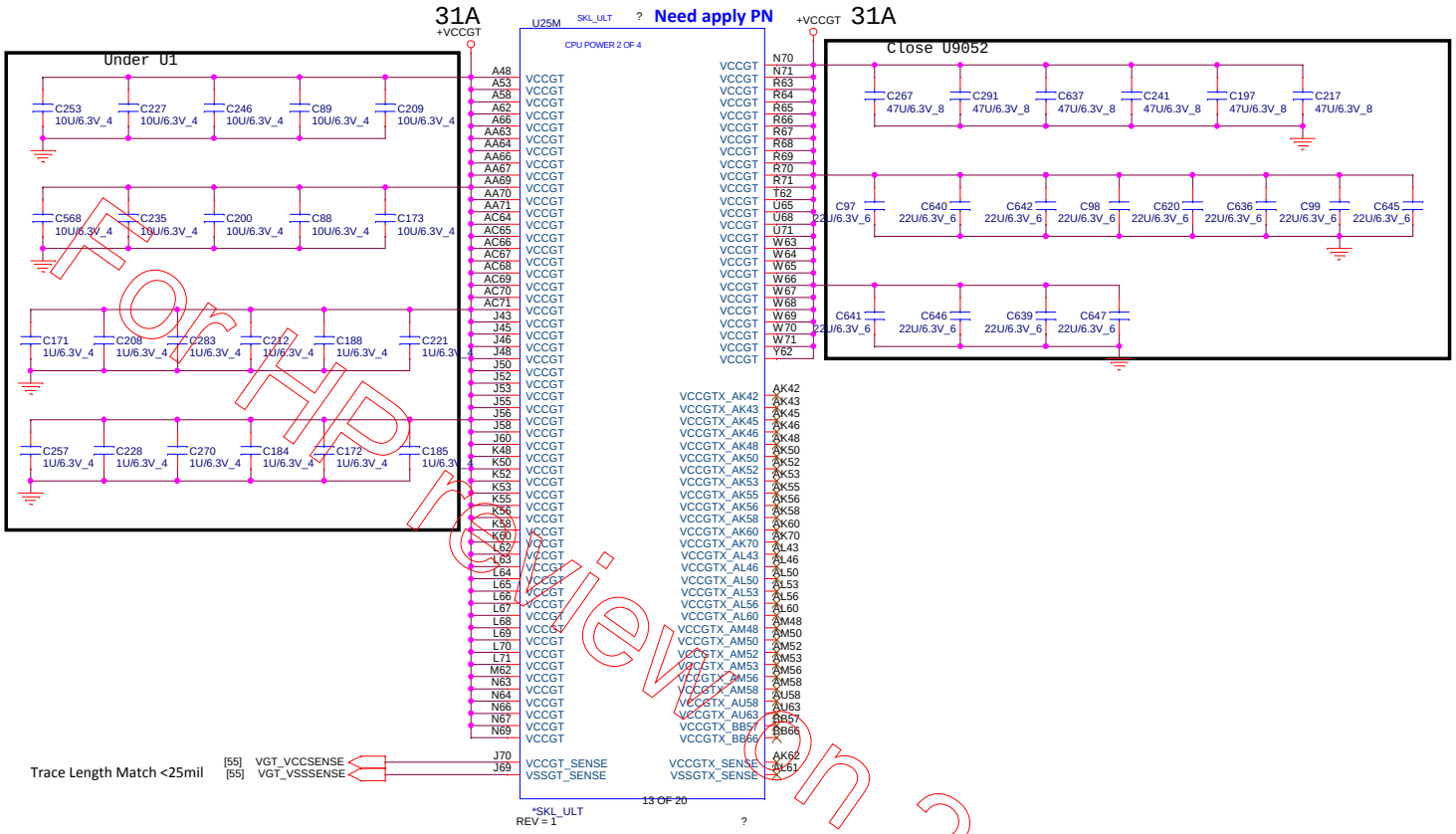




Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
$V_{CC_{GT}}$	Processor Graphics Power Rails	SVID
$V_{CC_{GTX}}$	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
$V_{CC_{SA}}$	System Agent Power Rail	SVID/Fixed (SKU dependent)
$V_{CC_{IO}}$	IO Power Rail	Fixed
$V_{CC_{ST}}$	Sustain Power Rail	Fixed
$V_{CC_{PLL}}$	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
$V_{CC_{OPC}}$	Processor OPC power rail (available only in SKU's with OPC)	Fixed
$V_{CC_{OPC\_1P8}}$	Processor OPC power rail (available only in SKU's with OPC)	Fixed
$V_{CC_{EOPIO}}$	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

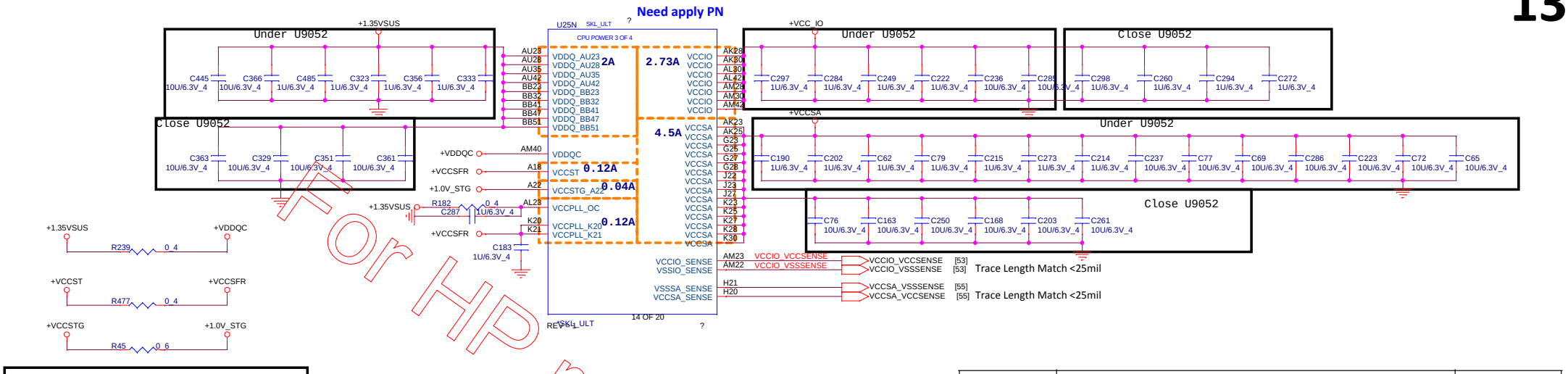
Top Review on 2015/04/17

+1.8V [4,5,8,30,52,60,63]
+VCC_CORE [55]
+VCCSFR [2,3,9,13,45]
+1.0V_STG [2,13]
+1.35VSUS [6,13,16,17,51]



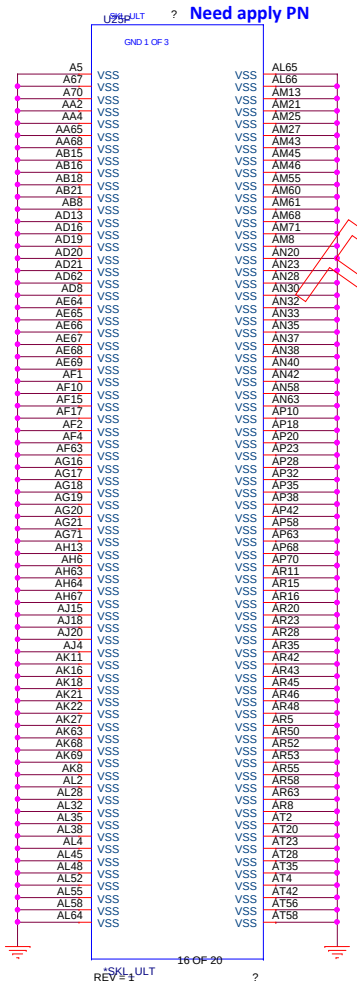
For Review 2015/04/17

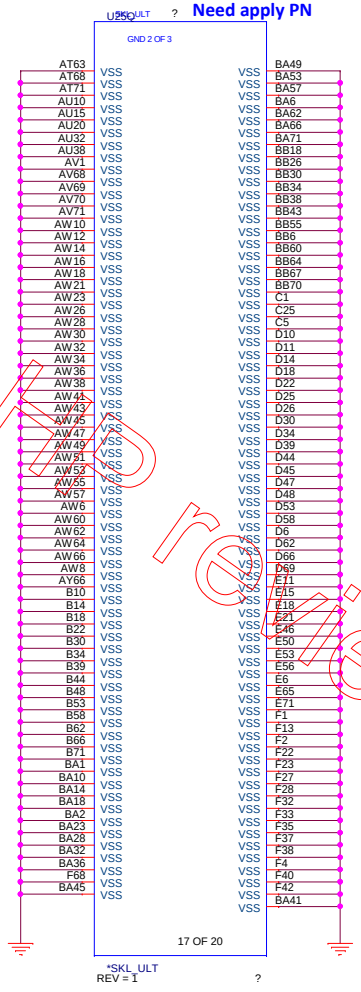
Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

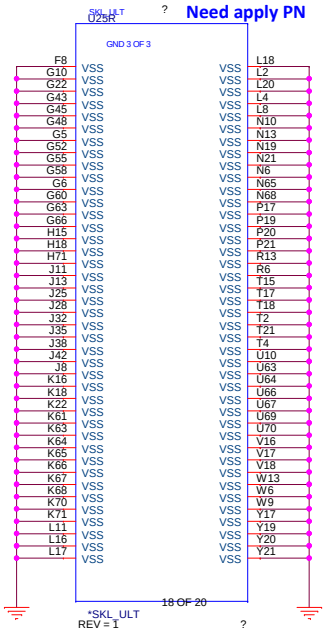


For HP review on 20150417

Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed







For Review on 2015/04/17

NB5	PROJECT:400 Series Quanta Computer Inc.	
Size: Custom	Document Number: 14 -- SKYLAKE (GND)	Rev: 1A
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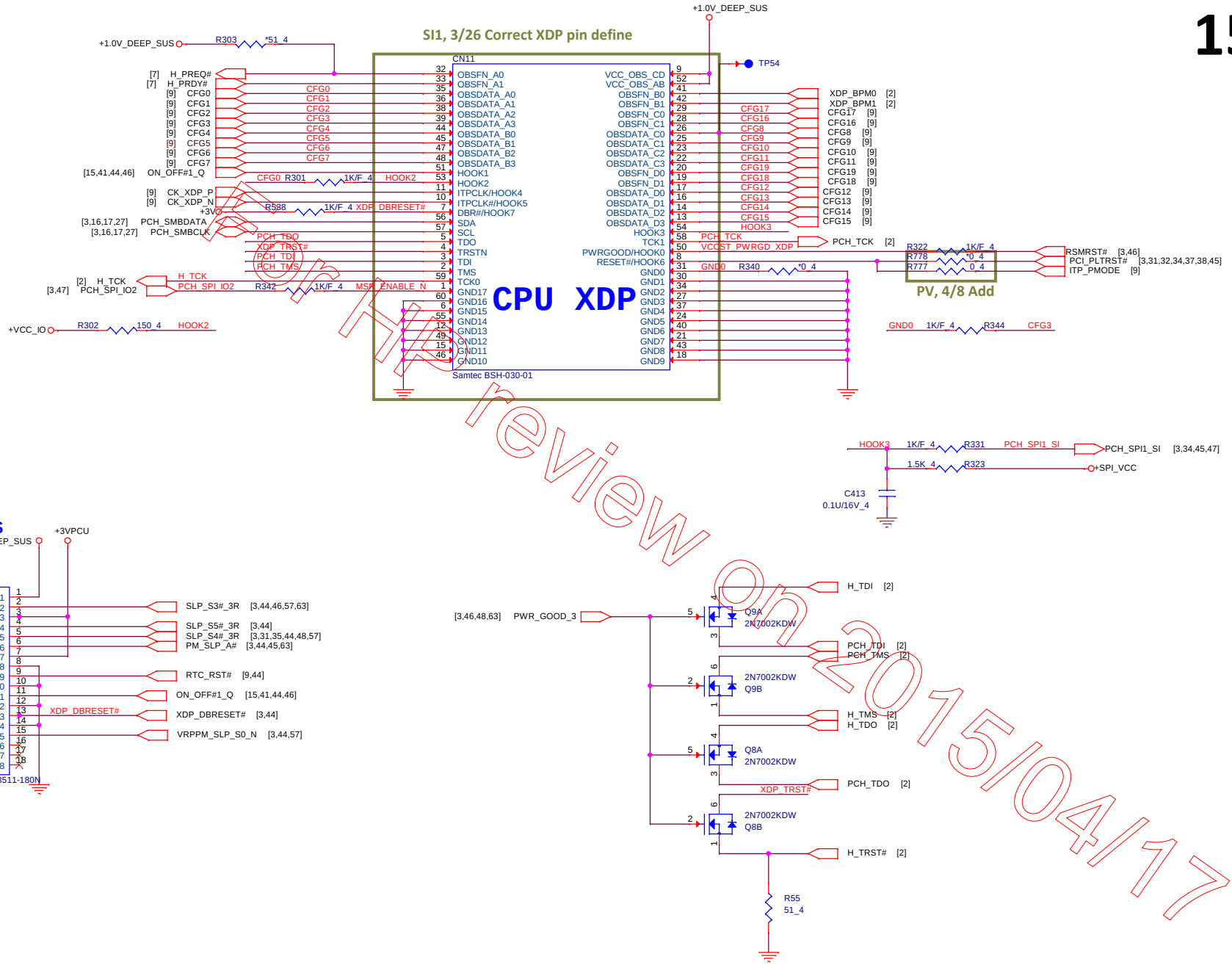
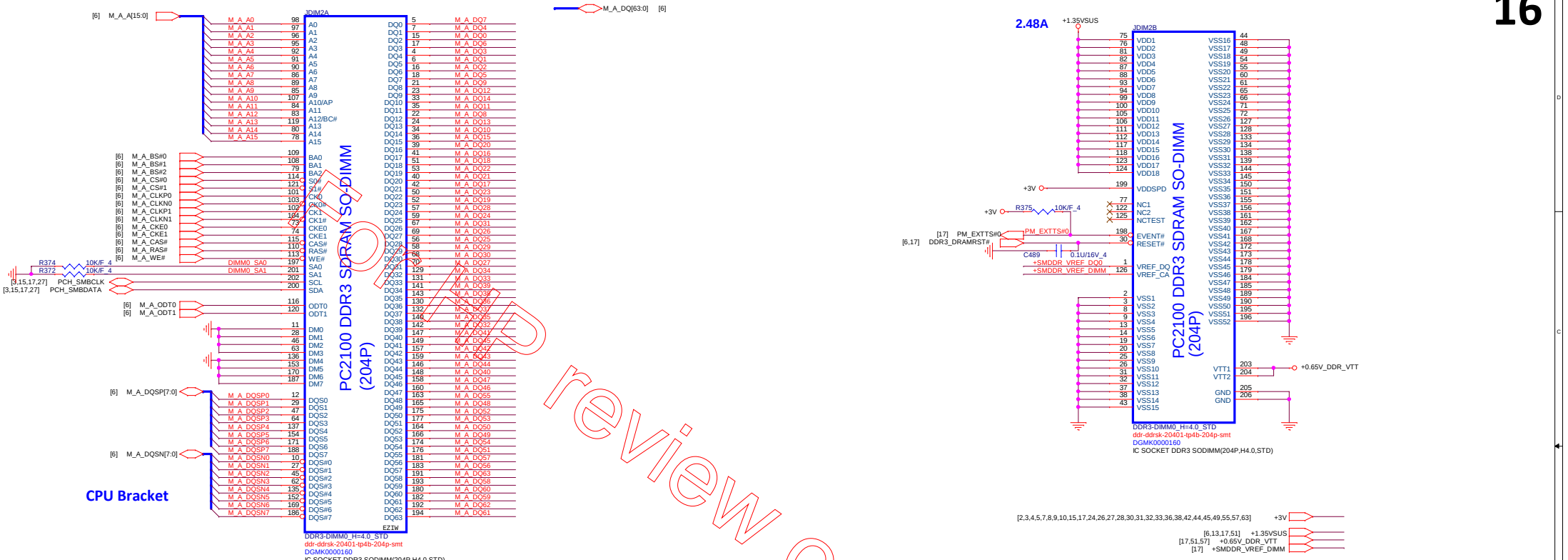


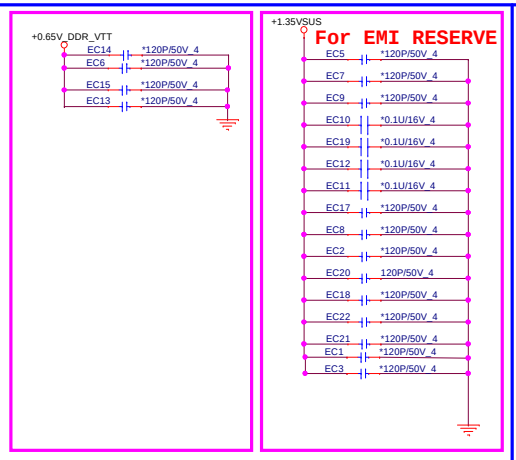
NB5	PROJECT:400 Series Quanta Computer Inc.	
Size	Document Number 15 -- HSW XDP & APS	Rev 1A
Date: Friday, April 17, 2015	Sheet 15 of 65	

DIMM & Footprint /同Joshua提供

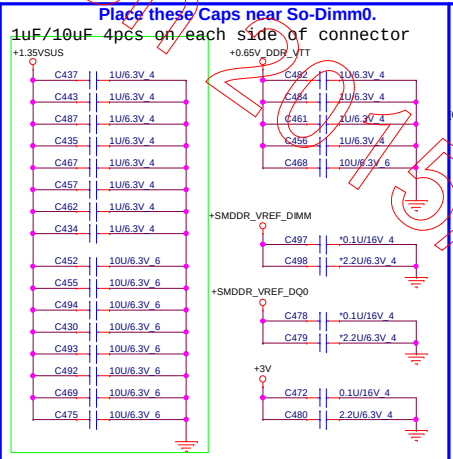


Review On 2015/04/17

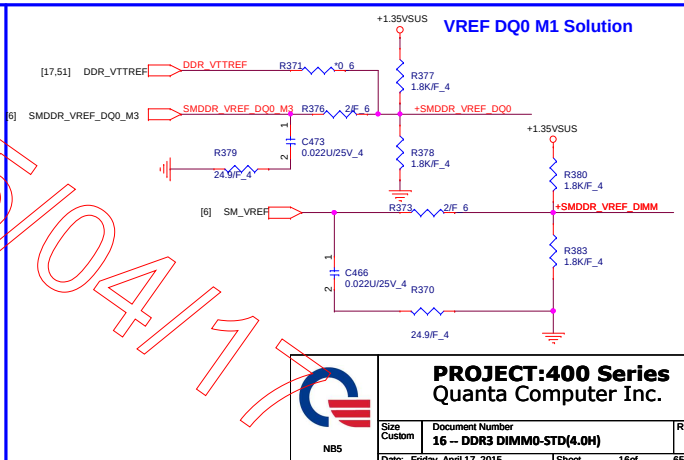
For EMI RESERVE



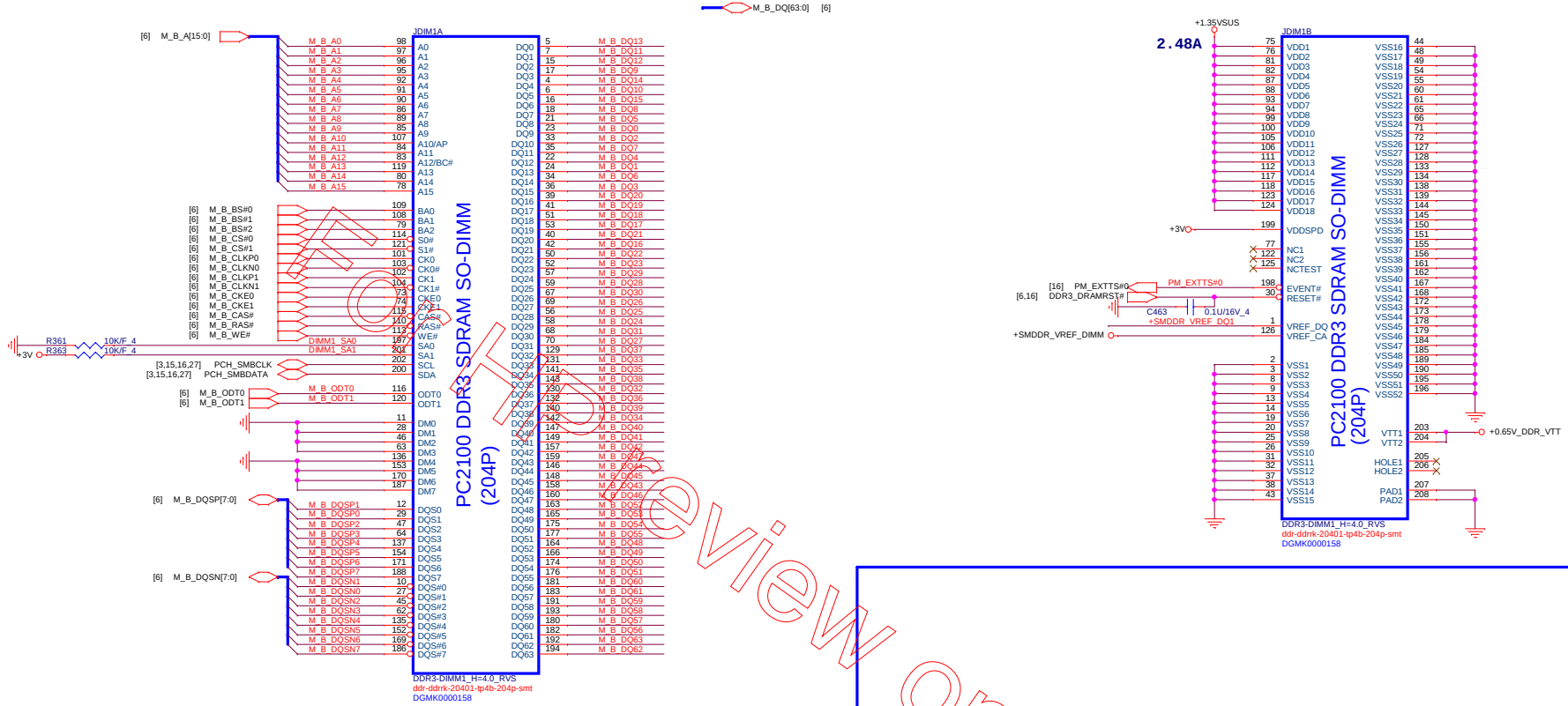
Place these Caps near So-Dimm0.
1uF/10uF 4pcs on each side of connector



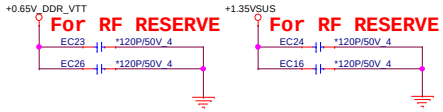
VREF DQ0 M1 Solution

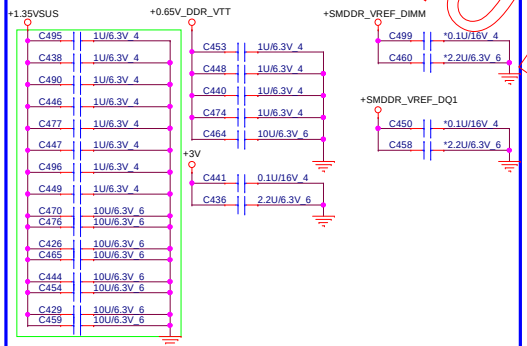


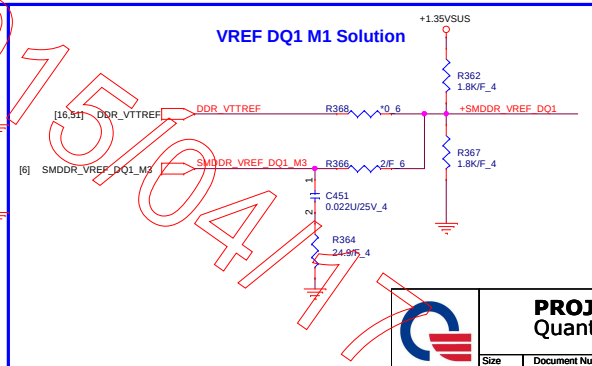
PROJECT:400 Series Quanta Computer Inc.		
Size: Custom	Document Number: 16 -- DDR3 DIMM0-STD(4.0H)	Rev: 1A
Date: Friday, April 17, 2015	Sheet: 16of	65



Review on 2015/04/17







[6,13,16,51] +1.35VSUS
[16,51,57] +0.65V_DDR_VTT
[2,3,4,5,7,8,9,10,15,16,24,26,27,28,30,31,32,33,36,38,42,44,45,49,55,57,63] +3V

NB5

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	17 -- DDR3 DIMM1-RVS(4.0H)	1A
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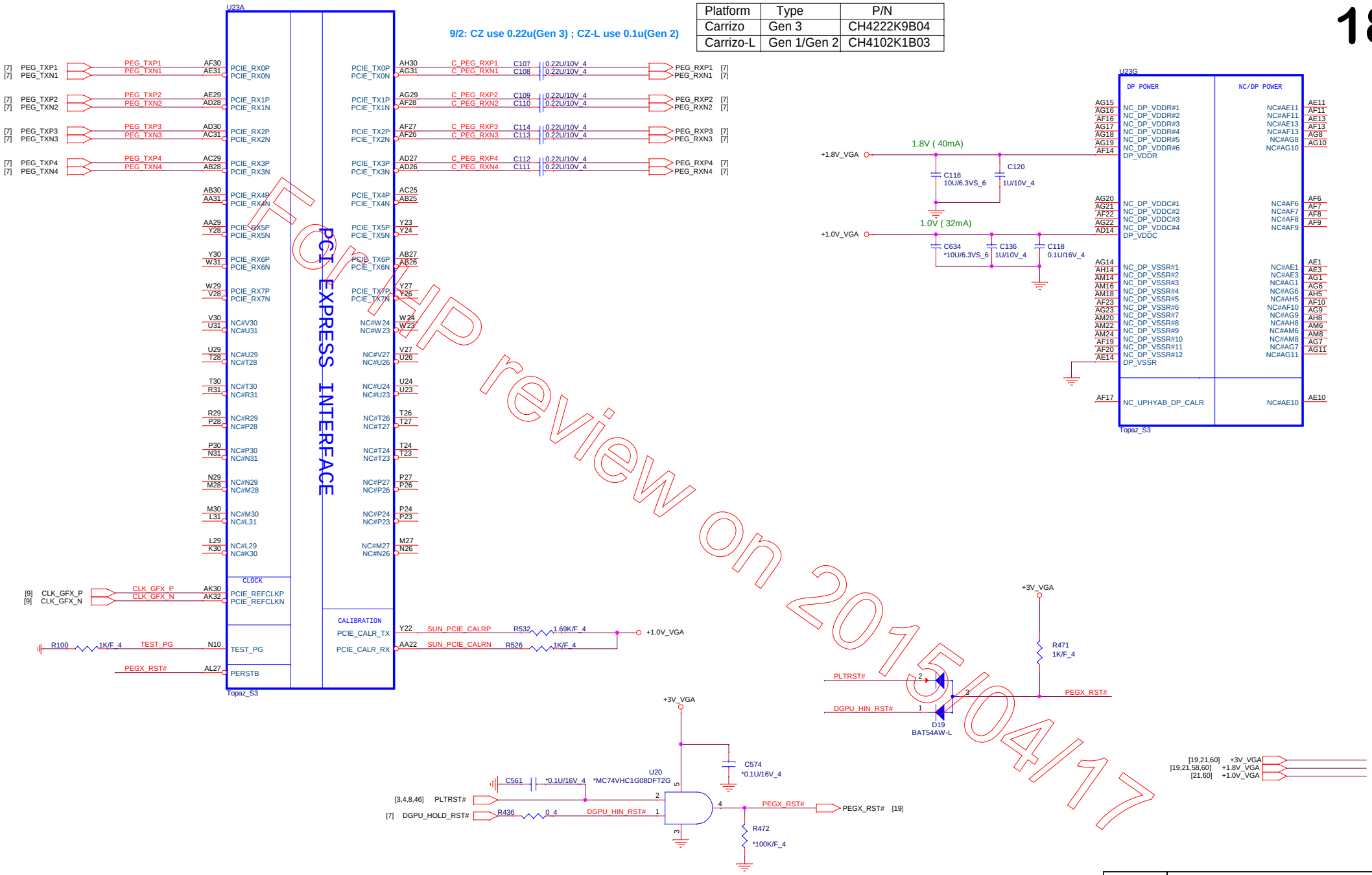
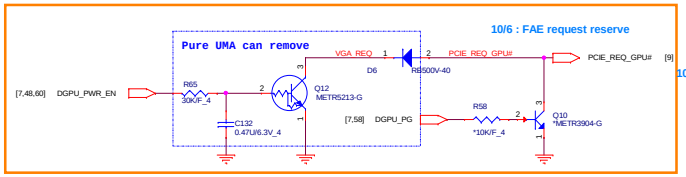
Platform	Type	P/N
Carrizo	Gen 3	CH4222K9B04
Carrizo-L	Gen 1/Gen 2	CH4102K1B03

9/2: CZ use 0.22u(Gen 3) ; CZ-L use 0.1u(Gen 2)

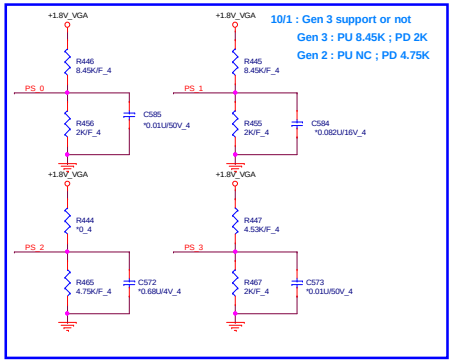


For ZIP review on 2015/04/17

NB5	PROJECT:400 Series Quanta Computer Inc.	
	Size:	Document Number: 18 -- Meso_S3_PCIE/DP POWER — Rev: 1A
	Date: Friday, April 17, 2015	Sheet 18 of 65

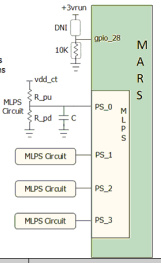


10/7 : remove TP for no use



MLPS Implementation

- Connect GPIO_28 to 10K pulldown to enable MLPS
- If any of PS_0/1/2/3 is not used, leave "no connect"
- R_pu, R_pd and C must be properly populated per tables below
- Place MLPS circuit components as close to the ASIC as possible
- Total DC resistance of trace between PS pin and C should be less than 2 ohms
- Total DC resistance of trace between C and ground should be less than 2 ohms
- Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance



Capacitor Lookup Table

C (nF)	Bits(5,4)
680	00
82	01
10	10
NC	11

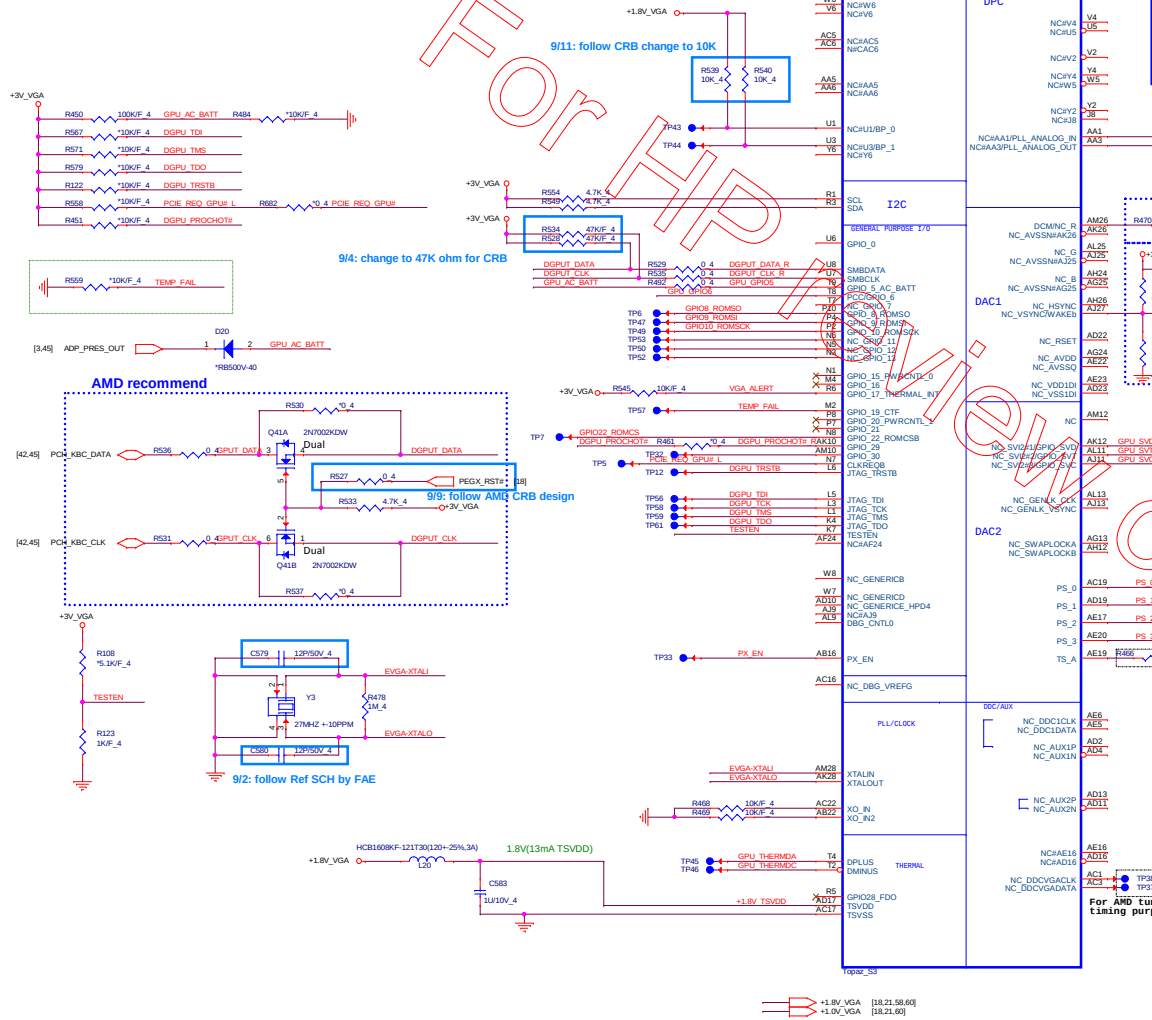
Resistor Divider Lookup Table

R_pu (Ohm)	R_pd (Ohm)	Bits(3,2,1)
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

BIT5 => BIT0

PS0 => 11001
PS1 => 11000
PS2 => 11000
PS3 => 11000

MLPS Bit	Strap Name	Description	Recommended Settings
PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	If STRAP_BIOS_ROM_EN = 1, ROM_CONFIG[2:0] define the ROM type. If STRAP_BIOS_ROM_EN = 0, ROM_CONFIG[2:0] define the primary memory-aperture size. See Primary Memory Aperture Size (p. 29).	Design dependent, see the description.
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	N/A	Reserved.	1
PS_1[1]	STRAP_BIF_GEN3_EN_A	PCIe GEN3 capability. 1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported.	Design dependent, see the description.
PS_1[2]	STRAP_BIF_CLK_PM_EN	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQB). 0 = The CLKREQB power management capability is disabled 1 = The CLKREQB power management capability is enabled	0
PS_1[3]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	Control the transmitter full-/half-swing mode 0 = The transmitter half-swing is enabled 1 = The transmitter full-swing is enabled	1
PS_1[5]	STRAP_TX_DEEMPH_EN	PCI EXPRESS® transmitter, de-emphasis enable. 0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled.	Design dependent, see the description.
PS_2[1]	N/A	Reserved.	0
PS_2[2]	N/A	Reserved.	0
PS_2[3]	STRAP_BIOS_ROM_EN	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	Design dependent, see the description.
PS_2[4]	N/A	Reserved.	1
PS_2[5]	N/A	Reserved	1
PS_3[1]	BOARD_CONFIG[0]	Board configuration related strapping, such as for memory ID	Design dependent, see the description.
PS_3[2]	BOARD_CONFIG[1]		
PS_3[3]	BOARD_CONFIG[2]		
PS_3[4]	N/A	Reserved.	1
PS_3[5]	N/A	Reserved.	1



PS_3[3:1]	Vendor	Type	Vendor P/N	QCI P/N	PU	PD
000	Samsung- Q die	128Mx16 *4, 1Ghz	K4W2G1646Q-BC1A	AKD5MGST508/AKD5MGST509	NC	4.75K
001	Samsung- E die	256Mx16 *4, 1Ghz	K4W4G1646E-BC1A	AKD5PGDT500/AKD5PGDT501	8.45K	2K
010	Hynix- Huma F die	128Mx16 *4, 1Ghz	H5TC2G63FFR-11C	AKD5MZDTW02/AKD5MZDTW03	4.53K	2K
011	Hynix- C(Polaris)	256Mx16 *4, 1Ghz	H5TC4G63CFR-N0C	AKD5PZDTW01/AKD5PZDTW02	6.98K	4.99K
100	Micron- K die	128Mx16 *4, 1Ghz	MT41J128M16JT-093G:K	AKD5MGSTL16/AKD5MGSTL17	4.53K	4.99K
101	Micron- E die	256Mx16 *4, 1Ghz	MT41J256M16HA-093G:E	AKD5PZSTL00/AKD5PZSTL01	3.24K	5.62K
110	Nanya- F die	128Mx16 *4, 1Ghz	NT5CB128M16FP-FL	AKD5MGDTF00/AKD5MGDTF01	3.4K	10K
111	Nanya- D die	256Mx16 *4, 1Ghz	NT5CB256M16DP-FL	AKD5PGDTF02/AKD5PGDTF03	4.75K	NC

Vendor ID

00 = Samsung
01 = Hynix
10 = Micron
11 = Nanya

VRAM density

0=128Mx16
1=256Mx16

Meso Multi-level Pin Straps

MLPS Bit: PS_3_
mappings between the bit values and resistor values

For Review Only

PROJECT:	400 Series
	Quanta Computer Inc.
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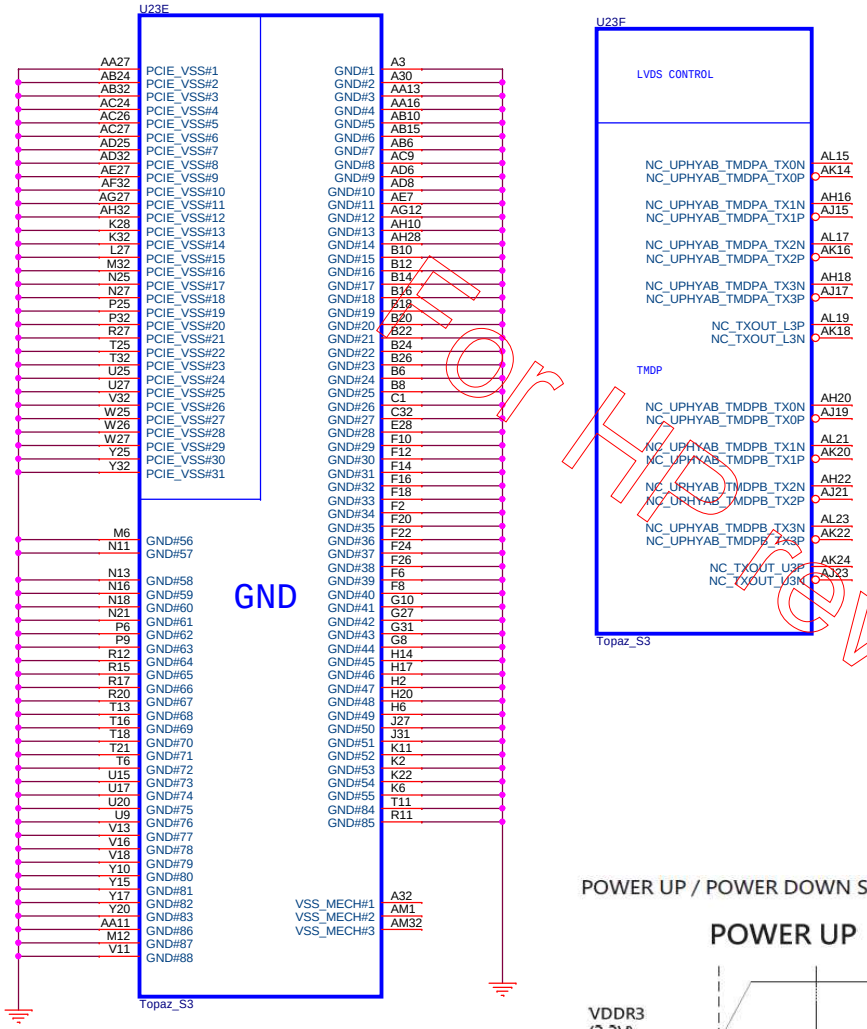


CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

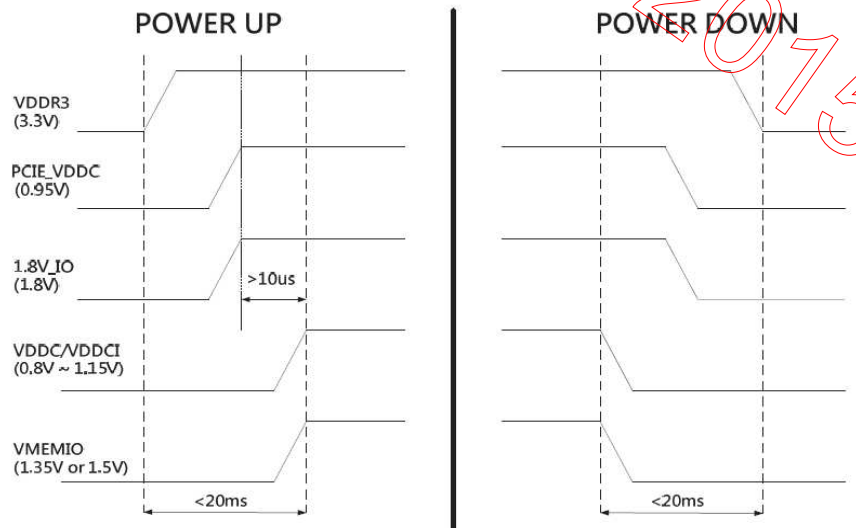
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSYNC	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21 H2SYNC GENERICC GPIO8 GPIO2

POWER UP / POWER DOWN SEQUENCE



For Review on 2015/04/17

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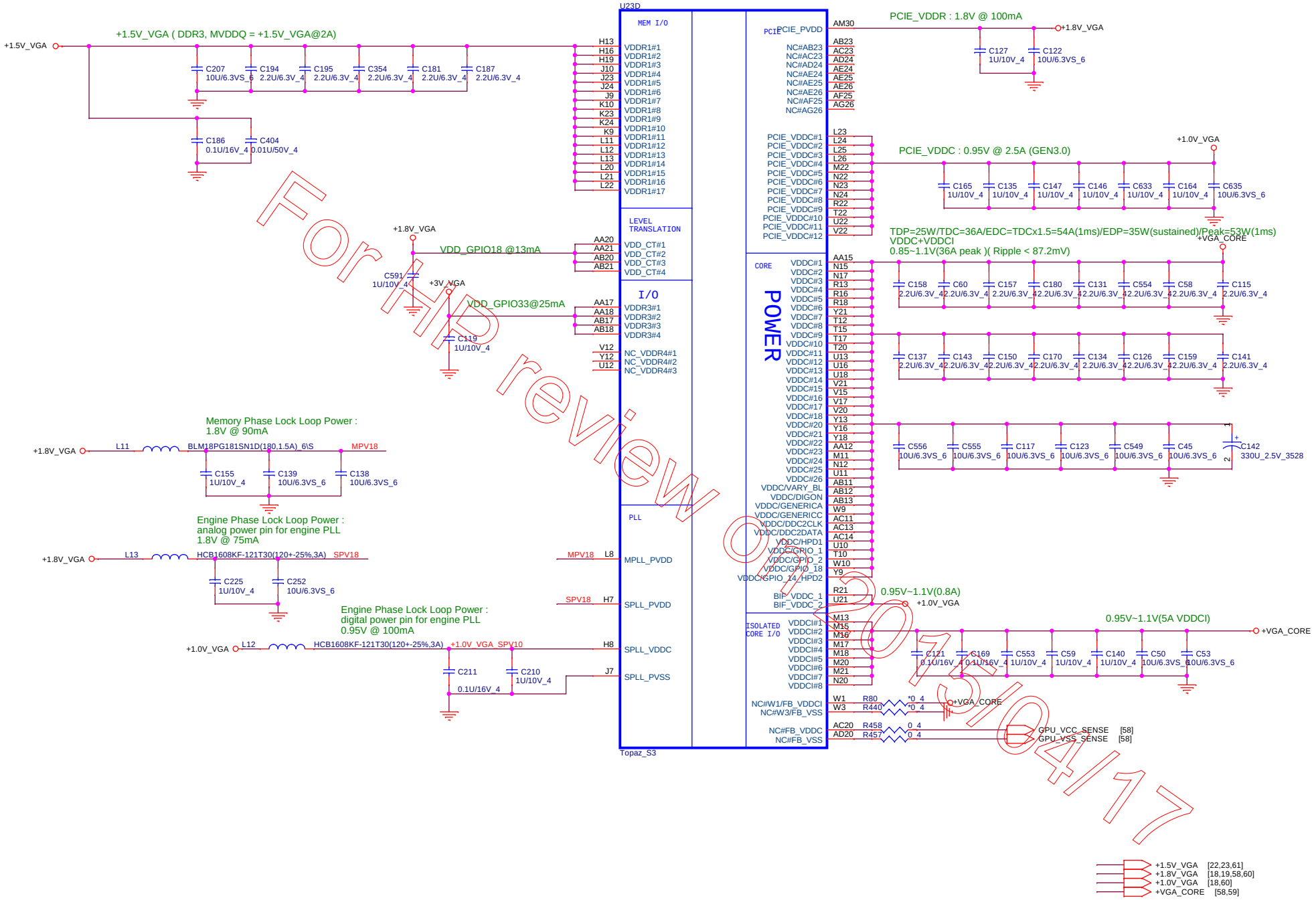
Size	Document Number 20 -- Meso_S3_GND/LVDS/Strap	Rev 1A
Date: Friday, April 17, 2015	Sheet 20 of 65	



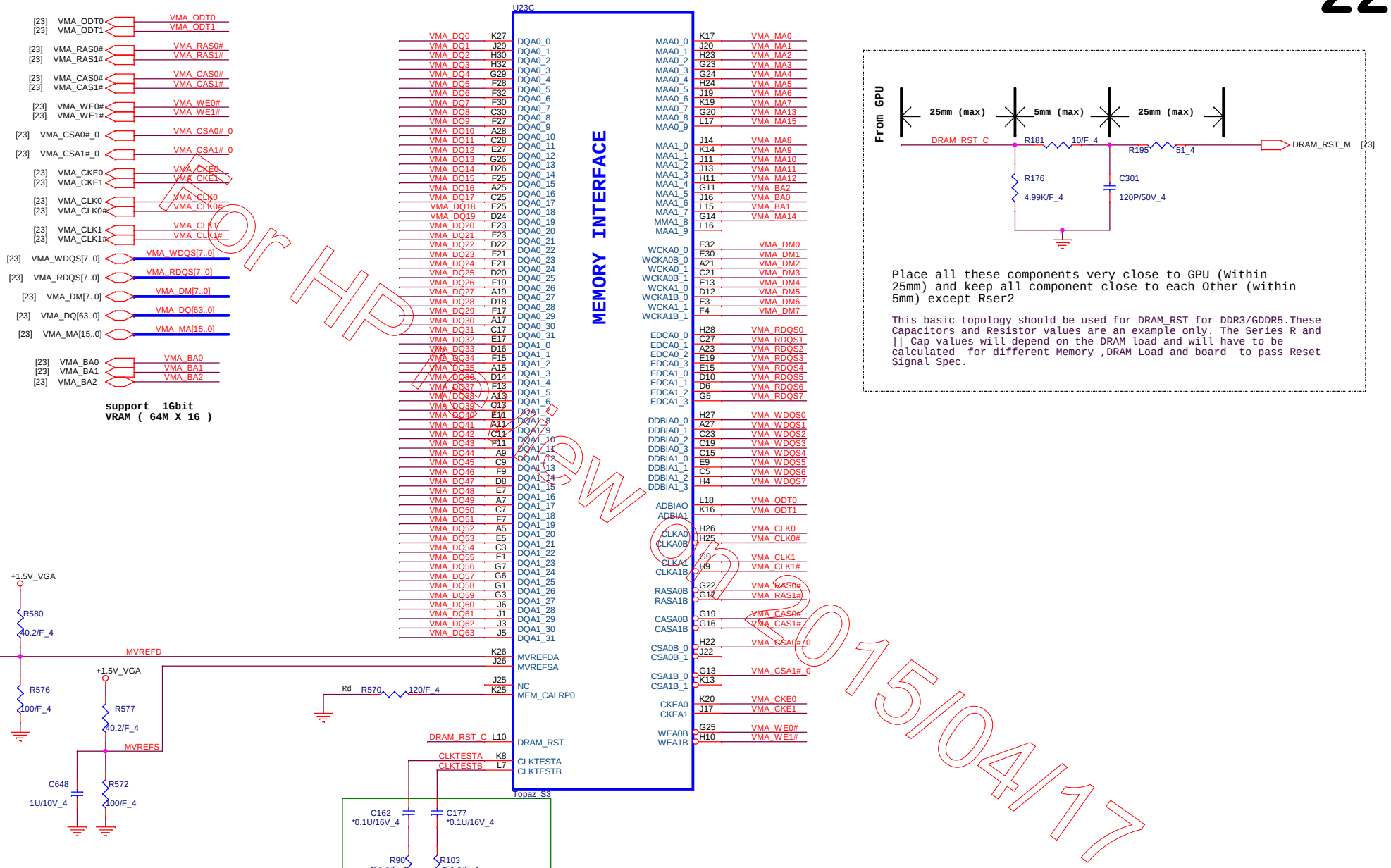
For HP review 01/30/2015/04/17

PROJECT:400 Series
Quanta Computer Inc.

NB5

Size	Document Number	Rev
	21 -- Meso_S3_Power	1A

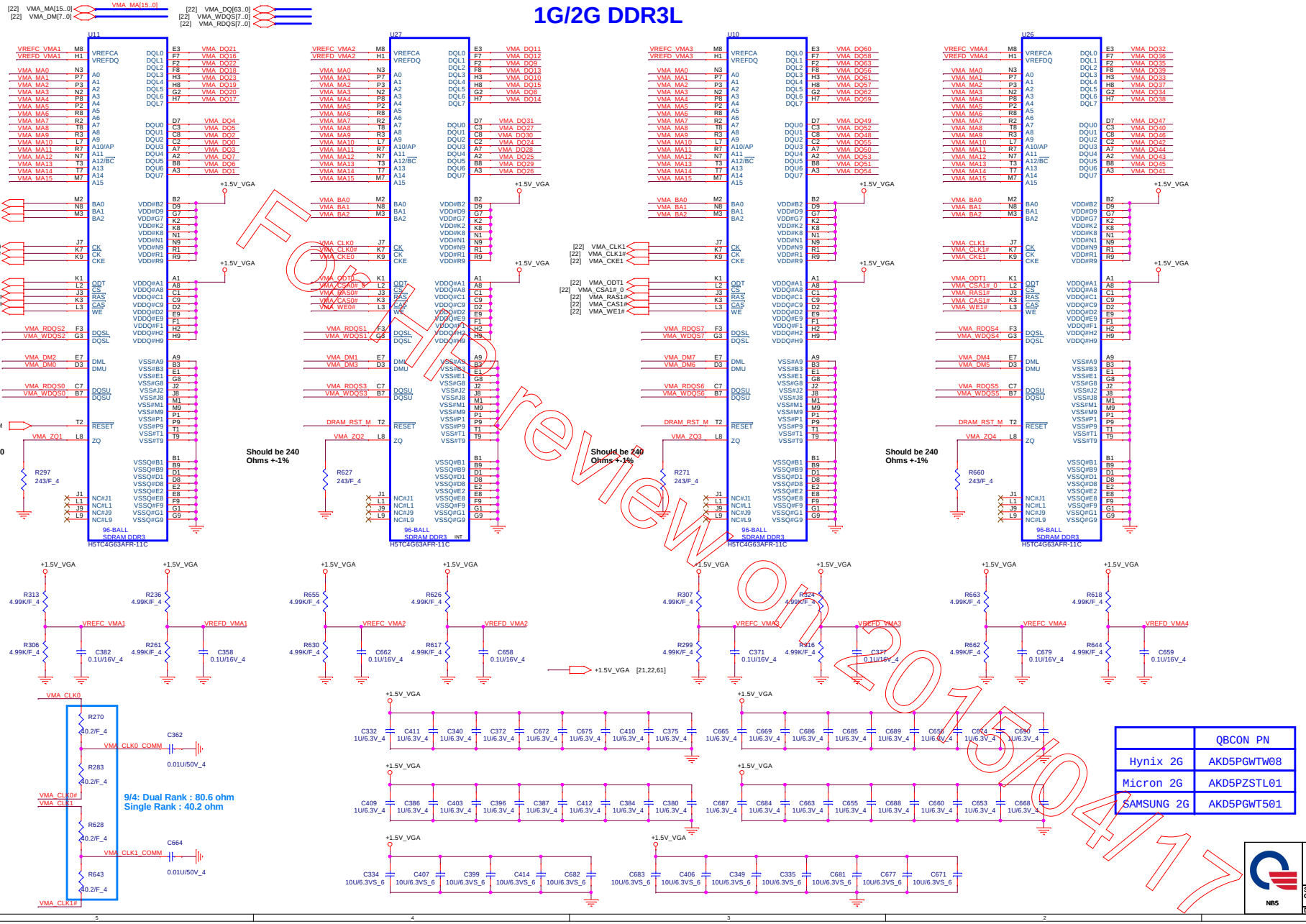
Date: Friday, April 17, 2015 Sheet 21 of 65



For HP Review 2015/04/17

NB5	PROJECT:400 Series Quanta Computer Inc.	
Size	Document Number 22 -- Meso_S3_MEM_Interface	Rev 1A
Date: Friday, April 17, 2015	Sheet 22 of 65	

1G/2G DDR3L



	QBCON PN
Hynix 2G	AKD5PGWTW08
Micron 2G	AKD5PZSTL01
SAMSUNG 2G	AKD5PGWT501

For Review on 2015/04/17

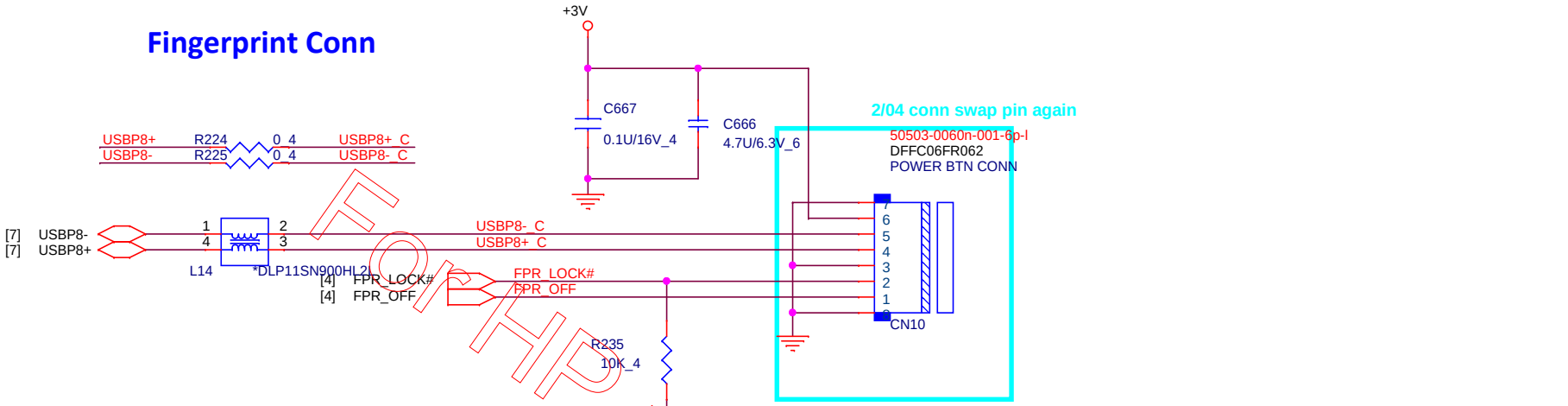
NB5

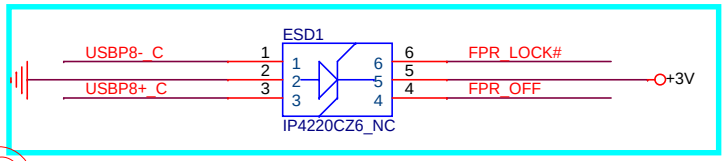
PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	23 -- Meso_S3_VRAM_DDR3L BGA96	1A

Date: Friday, April 17, 2015 | Sheet 23 of 65

Fingerprint Conn





FOR HP review on 2015/04/17

NB5

PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	**24 -- FPR**	1A
Date: Friday, April 17, 2015	Sheet 24 of 65	

Hole

H4 *H-TC295BC315D118P2
H10 *H-C315D236P2
H9 *H-C315I118D118P2
H25 *SPAD-RE236X276NP
H27 *H-C315D118P2
H12 *H-TC236BC150D142P2
H17 *H-TC236BC150D142P2
H13 *H-TC236BC150D142P2
H18 *H-TC236BC150D142P2
H8 *H-TC236BC150D142P2

H16 *H-TC236BC150D142P2
H21 *H-C315I118D118P2
H28 *H-C236D102P2
H14 *H-C315I118D118P2
H15 *H-C315I118D118P2
H2 * H-C315I118D118P2
H3 *H-C197D197N

02/03 DB1 to SI

H7 H-TC236BC197D102P2
H1 H-TC236BC197D102P2
H11 H-TC236BC197D102P2

H20 *H-C256D118P2
H5 *H-C315D118P2
H6 *H-C315D118P2
H19 *H-C205D118P2
H22 *H-C102D102N
H23 *H-0MBA-1
H29 *H-C102D102N

02/11 DB1 to SI

ESD_GND
ESD_GND
D14 Clamp-Diode
D15 Clamp-Diode
H26 *SHORT-ESD31_5X32
H24 *SHORT-ESD31_5X32
ESD_GND
ESD_GND
H30 *spad-s197np

02/04 DB1 to SI for RF

+VIN
EC54 2200P/50V_4
EC55 82P/50V_4
EC71 2200P/50V_4
+1.35VSUS_S
EC68 82P/50V_4
+1.05V_LAN_REGOUT
EC56 82P/50V_4
+VCC_PRIM
EC69 82P/50V_4
+VCCGT
EC70 82P/50V_4
C713 22U/6.3V_6
+VIN
C708 1U/6.3V_4
EC57 2200P/50V_4
EC58 82P/50V_4
+VIN
C709 1U/6.3V_4
EC59 2200P/50V_4
EC60 82P/50V_4
+VIN
C710 1U/6.3V_4
EC61 2200P/50V_4
EC62 82P/50V_4
+VIN
C711 1U/6.3V_4
EC63 2200P/50V_4
EC64 82P/50V_4
+VIN
C712 1U/6.3V_4
EC65 2200P/50V_4
EC66 82P/50V_4

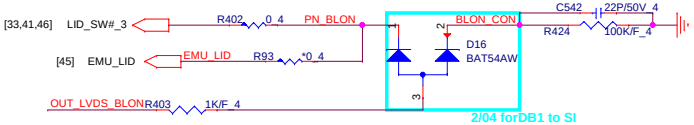
For HP review on 2015/04/17

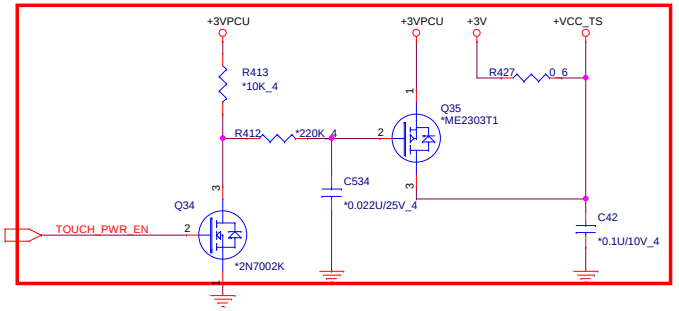
NB5

PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	25 -- LVDS converter RTD2136	1A
Date: Friday, April 17, 2015	Sheet 25of 65	

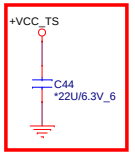
LID Switch





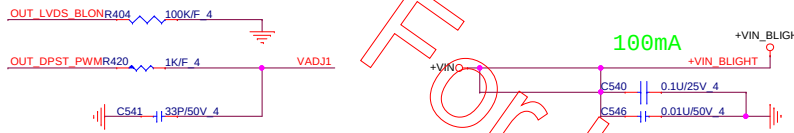
LVDS Conn.

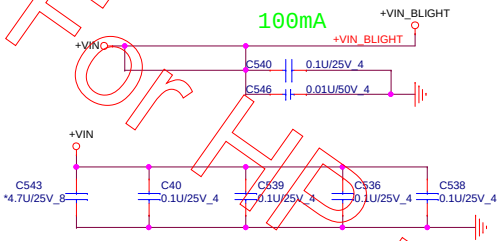
26

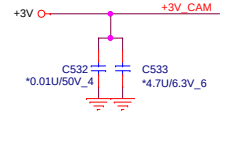


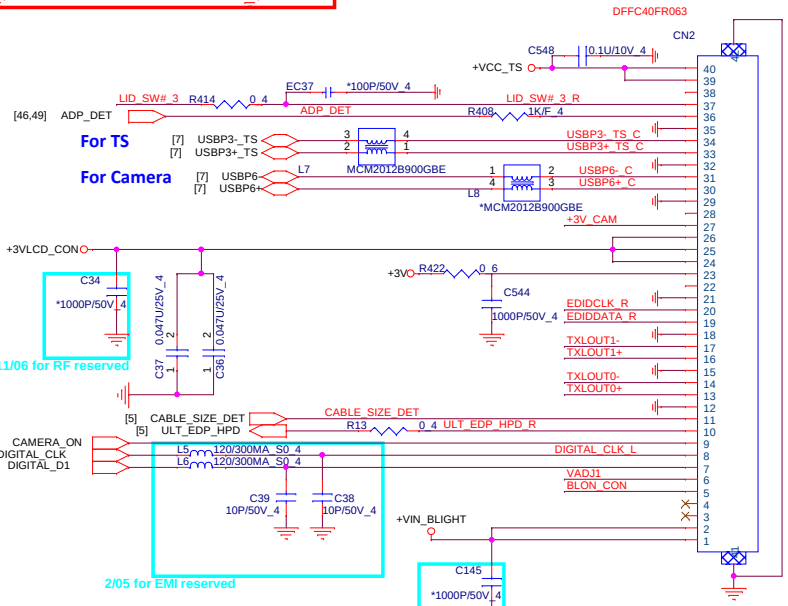
GS12401-1011-9H
lvds-50671-04041-001-40p-l

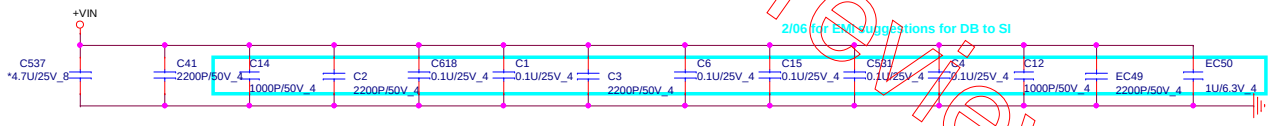
DFFC40FR063

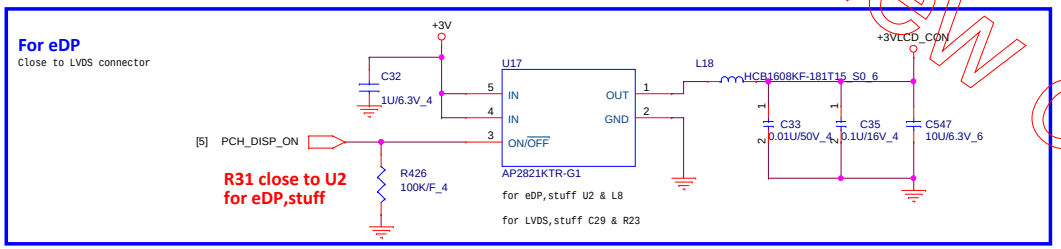


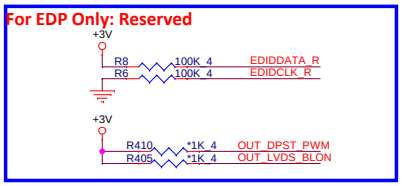


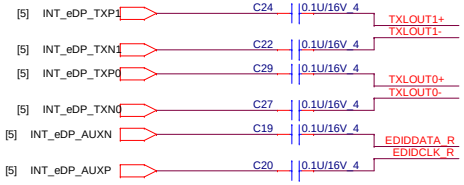












[2,3,4,5,7,8,9,10,15,16,17,24,27,28,30,31,32,33,36,38,42,44,45,49,55,57,63] +3V
[8,29,30,31,40,42,43,52,57,63] +5V
[25,44,49,50,51,52,53,54,55,56,57,59,61] +VIN

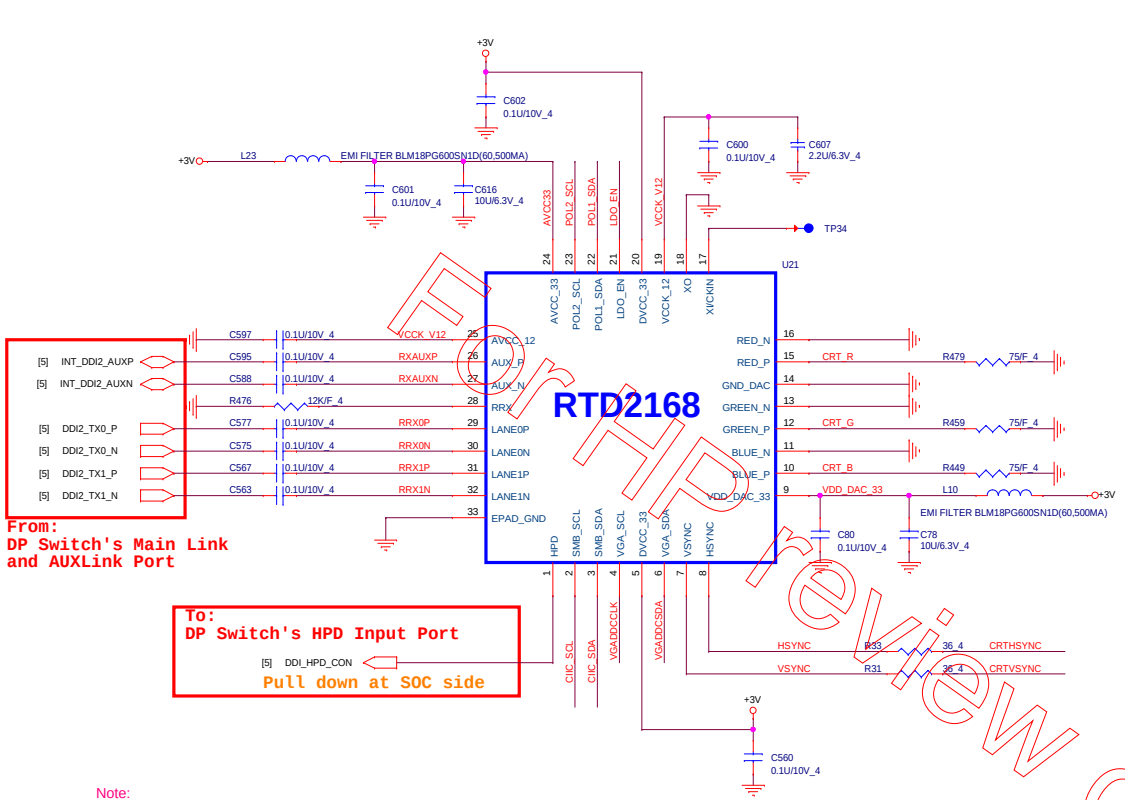
For Review on 2015/04/17

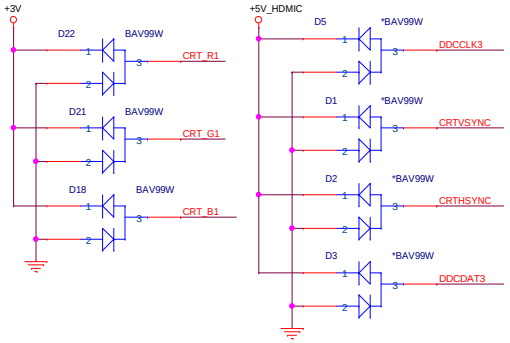
NB5

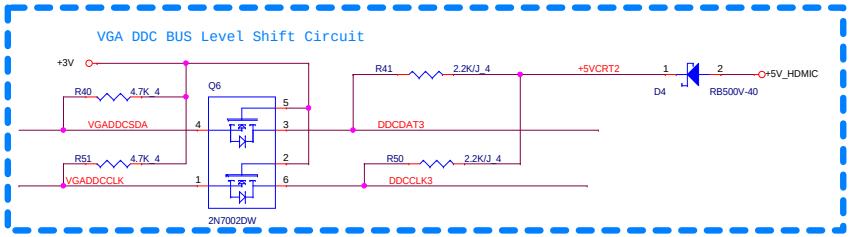
PROJECT:400 Series
Quanta Computer Inc.

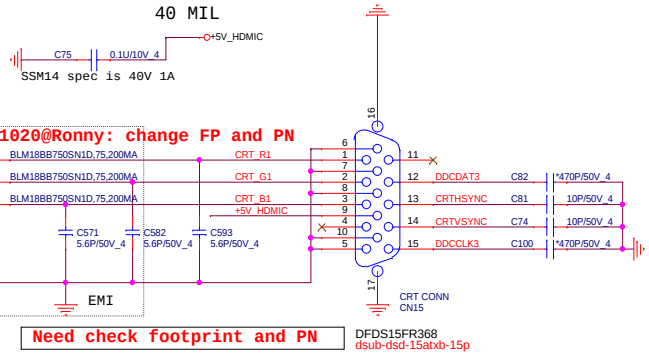
Size	Document Number	Rev
Custom	26 -- LCD CONN/LID/CAM/D-MIC	1A

Date: Friday, April 17, 2015 Sheet 26 of 65









Need check footprint and PN — DFDS15FR368 dsub-dsd-15atxb-15p

Note:
1- C1,C3,C6,C8,C9,C11,C12,C19,C20
Should be close to chip
2- C12 shold be X5R material
3- R1 should be 12K ohm with +/-1%
4- R8, R9, R10 should be 75 ohm with +/-1%

Mode Configure Table(Power On Latch)

POL2_SCL(PIN23) \ POL1_SDA(PIN22)	0	1
0	X	EP MODE
1	ROM ONLY MODE	EEPROM MODE

RTD2168 Supports three operation mode for system design.
Reserve 4.7K resistor pull high/low for mode selection

ROM ONLY Mode : PIN22 pull low, PIN23 pull high
EP Mode : PIN22 pull high, PIN23 pull low
EEPROM Mode : PIN22 pull high, PIN23 pull high

EEPROM MODE

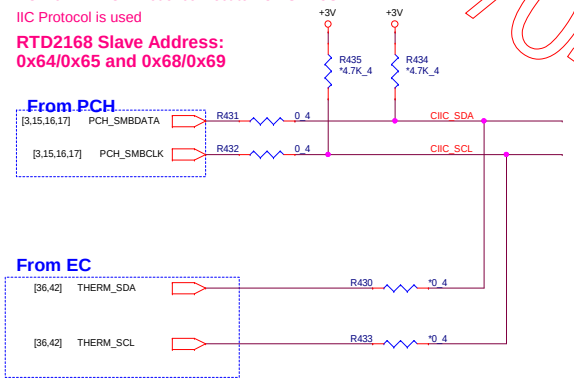
In EEPROM mode,an additional EEPROM is needed.
EEPROM should configure with following conditions.

1- EEPROM with a size of 16K-Byte
2- EEPROM device should be 2-byte addressing device
3- Slave address should configure as 0xA8

CIIC_SCL, CIIC_SDA Connection

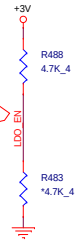
EP mode: Pin2, Pin3 connect to EC SMBUS
ROM or EEPROM mode: connect to PCH SMBUS
IIC Protocol is used

RTD2168 Slave Address:
0x64/0x65 and 0x68/0x69



Embedded LDO

Select VCCK_V12 source from external 1.2V or embedded LDO



LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO

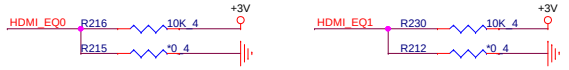
NB5

PROJECT : S Class-AMD
Quanta Computer Inc.

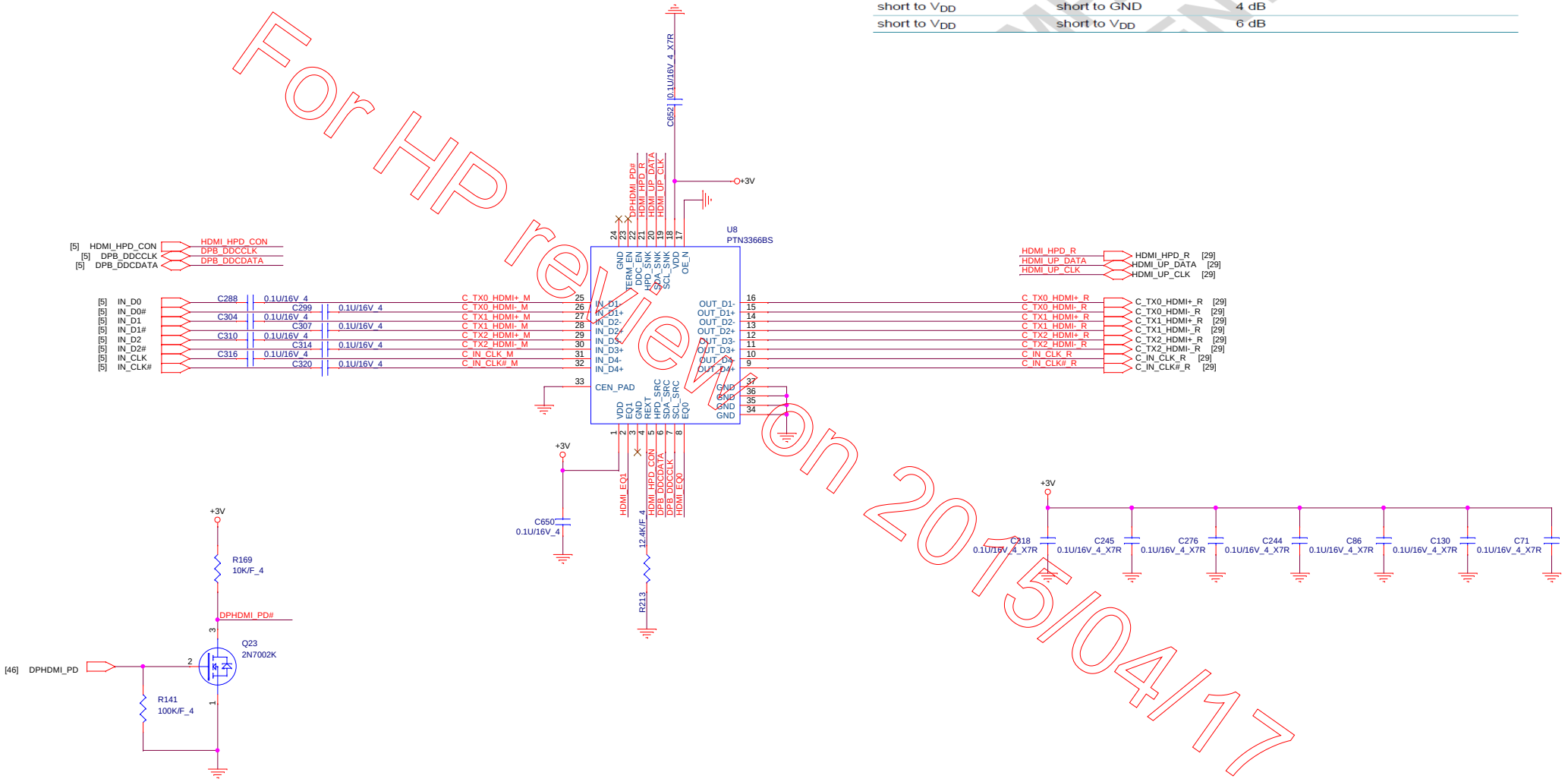
Size	Document Number	Rev
Custom	DP to VGA	1A

Date: Friday, April 17, 2015 Sheet 27 of 65

Under Review on 20150417



Inputs		Equalization for 3 Gbit/s
EQ1	EQ0	
short to GND	short to GND	0 dB
short to GND	short to V_{DD}	2 dB
short to V_{DD}	short to GND	4 dB
short to V_{DD}	short to V_{DD}	6 dB



OE_N	DDC_EN	HPD_SINK	Source output	PTN3366 power mode
LOW	HIGH	HIGH	source active	Active mode; DDC active
LOW	LOW	LOW	don't care	Standby mode
HIGH	LOW	don't care	don't care	Ultra low-power mode

For HP review on 2015/04/17

NB5

PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	28 – REPEATER PS8407A	1A

Date: Friday, April 17, 2015 Sheet 28 of 65

EMI Solution

C_TX2_HDMI+_R — R208 150/F_4 — C_TX2_HDMI-_R
C_TX1_HDMI+_R — R194 150/F_4 — C_TX1_HDMI-_R
C_TX0_HDMI+_R — R178 150/F_4 — C_TX0_HDMI-_R
C_IN_CLK_R — R221 150/F_4 — C_IN_CLK#_R

HDMI SMBus Isolation

[28] HDMI_UP_CLK — HDMI_UP_CLK
[28] HDMI_UP_DATA — HDMI_UP_DATA

11/06 for change new SW

+5V
U22
GND
IN
OUT
AP2331SA-7-01
C638 0.1U/16V_4
L24
0_6
+5V_HDMIC
C83 *0.01U/50V_4
C103 0.1U/16V_4
C617 *10U/6.3V_6

For Review on 2015/04/17

CN18
X_DP(PWR)
D2+
GND
D2-
D1+
GND
D1-
D0+ SHELL2
GND
D0-
CK+
GND
CK- SHELL2
CE Remote
NC
DDC CLK
DDC DATA
GND_DPAUX
+5V
HP DET
HD_DP_Option
DP/HDMI CONN
hdmi-c128g7-11913-l-19p

[28] C_TX2_HDMI+_R
[28] C_TX2_HDMI-_R
[28] C_TX1_HDMI+_R
[28] C_TX1_HDMI-_R
[28] C_TX0_HDMI+_R
[28] C_TX0_HDMI-_R
[28] C_IN_CLK+_R
[28] C_IN_CLK#_R
+5V_HDMIC
R616 2.2K_4 HDMI_UP_CLK
R615 2.2K_4 HDMI_UP_DATA
C331 *10P/50V_4
C342 *10P/50V_4
+5V_HDMIC
+5V_HDMIC
C654 *0.01U/50V_4
[28] HDMI_HPD_R
C279
VC1 *TVM0G5R5M220R
*220P/50V_4
for EMI request

ESD chip, reserve

U7
+5V_HDMIC
I/O-1 I/O-6
VDD GND
NC NC
I/O-2 I/O-5
I/O-3 I/O-4
C_TX1_HDMI-_R
C_TX1_HDMI+_R
C_TX0_HDMI-_R
C_TX0_HDMI+_R
*AZ1065-06F.R7G

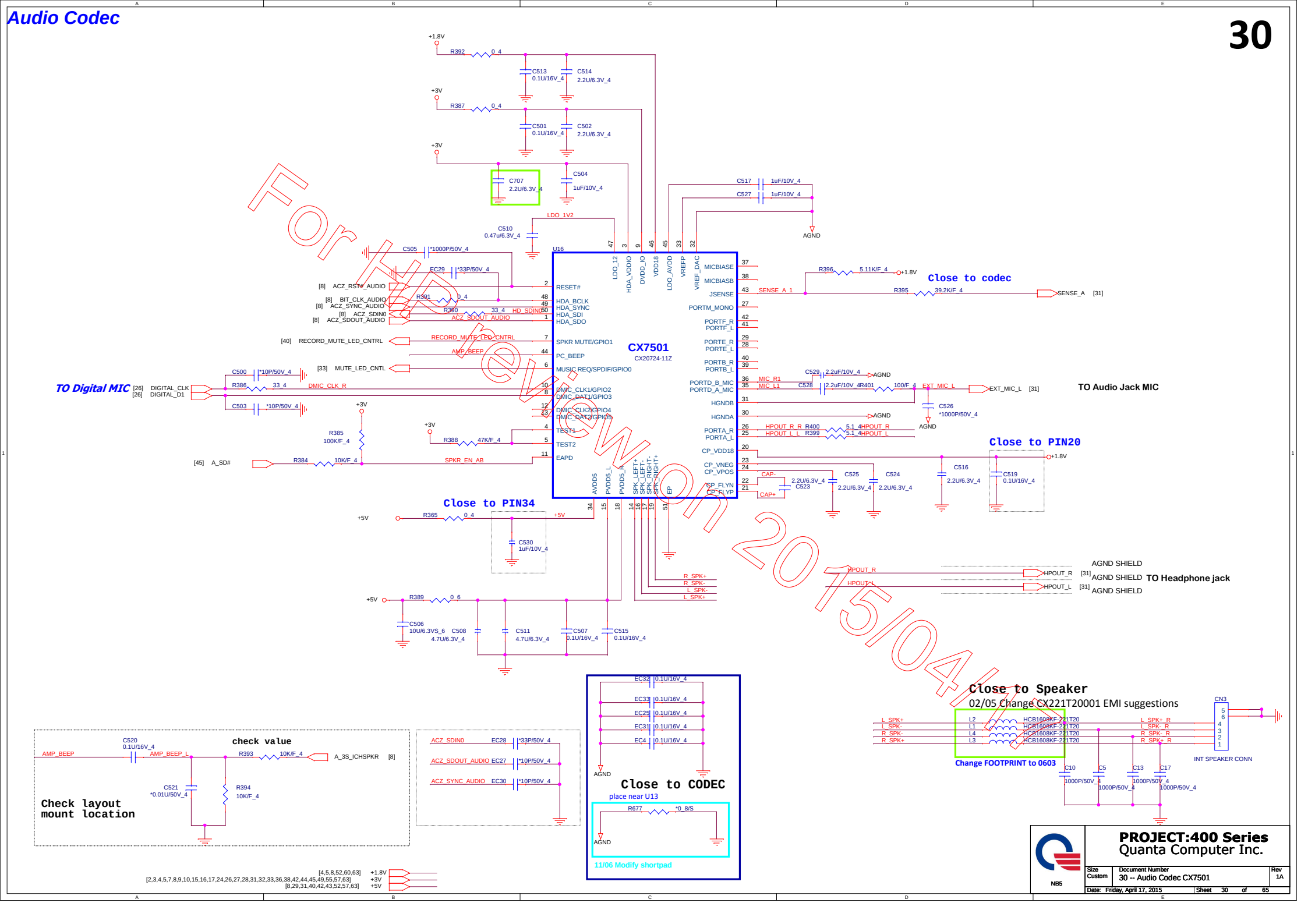
ESD chip, reserve

U9
+5V_HDMIC
I/O-1 I/O-6
VDD GND
NC NC
I/O-2 I/O-5
I/O-3 I/O-4
C_TX2_HDMI+_R
C_TX2_HDMI-_R
C_IN_CLK_R
C_IN_CLK#_R
*AZ1065-06F.R7G

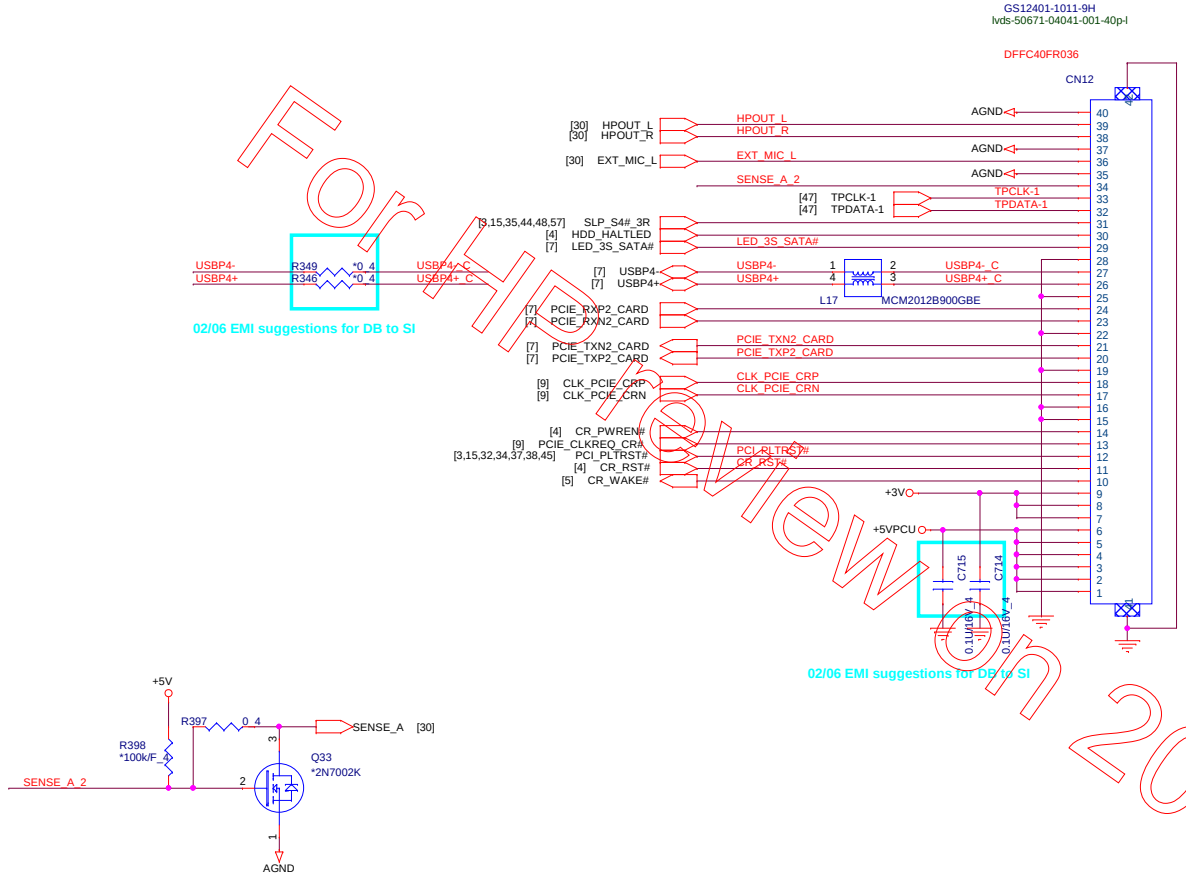
PROJECT:400 Series
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	29 -- HDMI CONNECTOR	1A
Date: Friday, April 17, 2015	Sheet 29 of 65	


Audio Codec
30
For HP review on 2015/04/17
CX7501
CX20724-11Z
U16
Close to codec
Close to PIN20
Close to PIN34
Close to CODEC
place near U13
11/06 Modify shortpad
TO Digital MIC
TO Audio Jack MIC
TO Headphone jack
AGND SHIELD
Close to Speaker
02/05 Change CX221T20001 EMI suggestions
Change FOOTPRINT to 0603
INT SPEAKER CONN
check value
Check layout
mount location
PROJECT:400 Series
Quanta Computer Inc.
Size Custom
Document Number 30 -- Audio Codec CX7501
Rev 1A
Date: Friday, April 17, 2015
Sheet 30 of 65
NB5

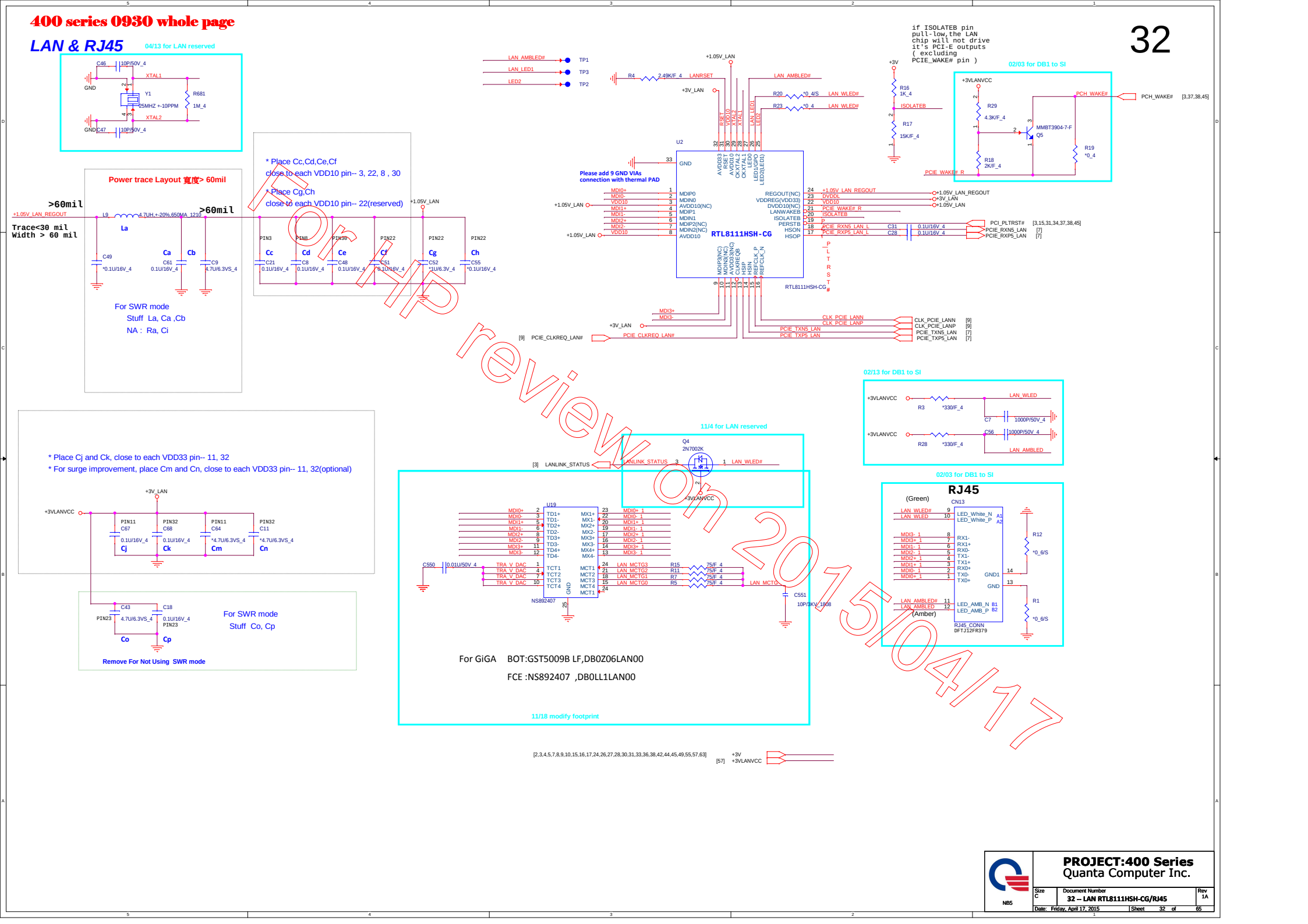
USB/Card Reader/Headphone_Mic Combo Jack Daugther Board Connector



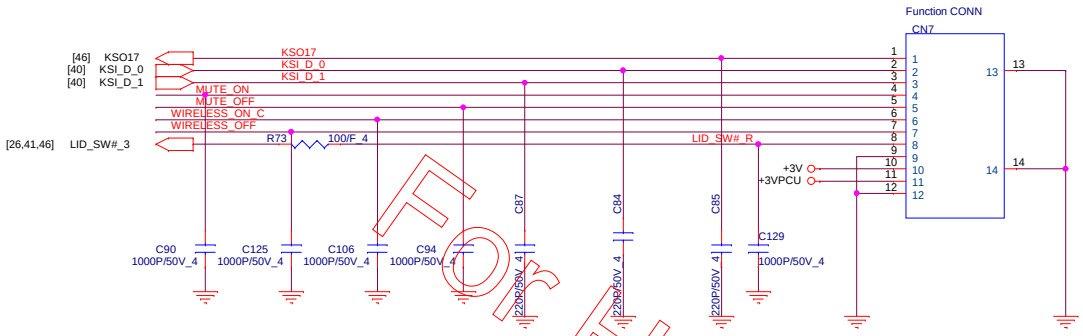
For Review on 2015/04/17

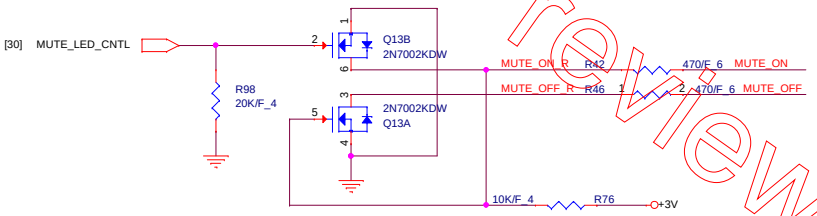
	PROJECT:400 Series Quanta Computer Inc.	
Size: Custom	Document Number: 31 -- DAUGTHER BOARD CONN.	Rev: 1A
Date: Friday, April 17, 2015	Sheet 31 of 65	

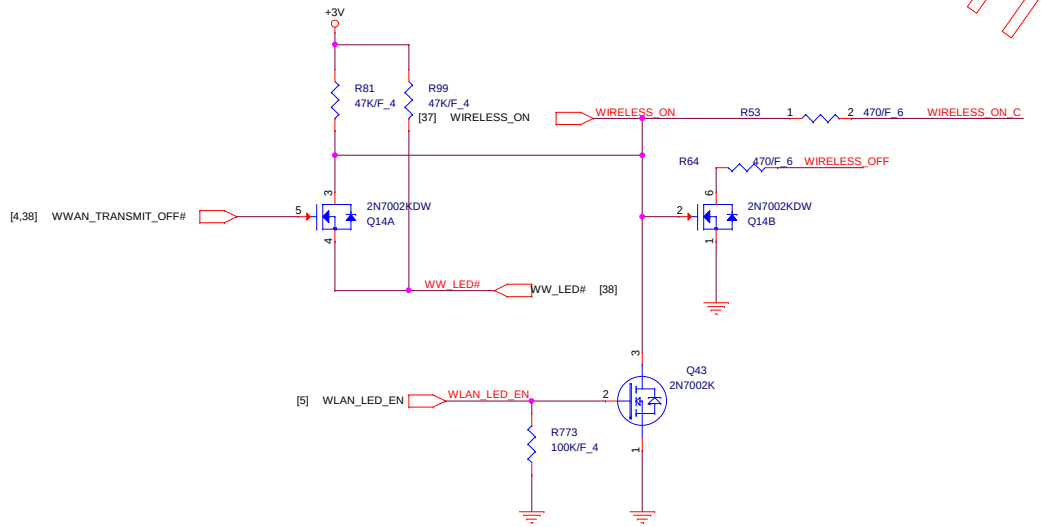
NB5



400 series 0930 whole page
LAN & RJ45
32
04/13 for LAN reserved
Power trace Layout 寬度> 60mil
>60mil
Trace<30 mil
Width > 60 mil
For SWR mode
Stuff La, Ca ,Cb
NA : Ra, Ci
* Place Cc,Cd,Ce,Cf
close to each VDD10 pin-- 3, 22, 8 , 30
* Place Cg,Ch
close to each VDD10 pin-- 22(reserved)
* Place Cj and Ck, close to each VDD33 pin-- 11, 32
* For surge improvement, place Cm and Cn, close to each VDD33 pin-- 11, 32(optional)
For SWR mode
Stuff Co, Cp
Remove For Not Using SWR mode
if ISOLATEB pin
pull-low,the LAN
chip will not drive
it's PCI-E outputs
(excluding
PCIE_WAKE# pin)
02/03 for DB1 to SI
Please add 9 GND VIAs
connection with thermal PAD
RTL8111HSH-CG
11/4 for LAN reserved
NS892407
For GiGA BOT:GST5009B LF,DB0Z06LAN00
FCE :NS892407 ,DB0LL1LAN00
11/18 modify footprint
RJ45
(Green)
(Amber)
RJ45_CONN
DFTJ12FR379
For MP review on 2015/04/17
PROJECT:400 Series
Quanta Computer Inc.
Size C
Document Number
32 -- LAN RTL8111HSH-CG/RJ45
Rev 1A
Date: Friday, April 17, 2015
Sheet 32 of 65







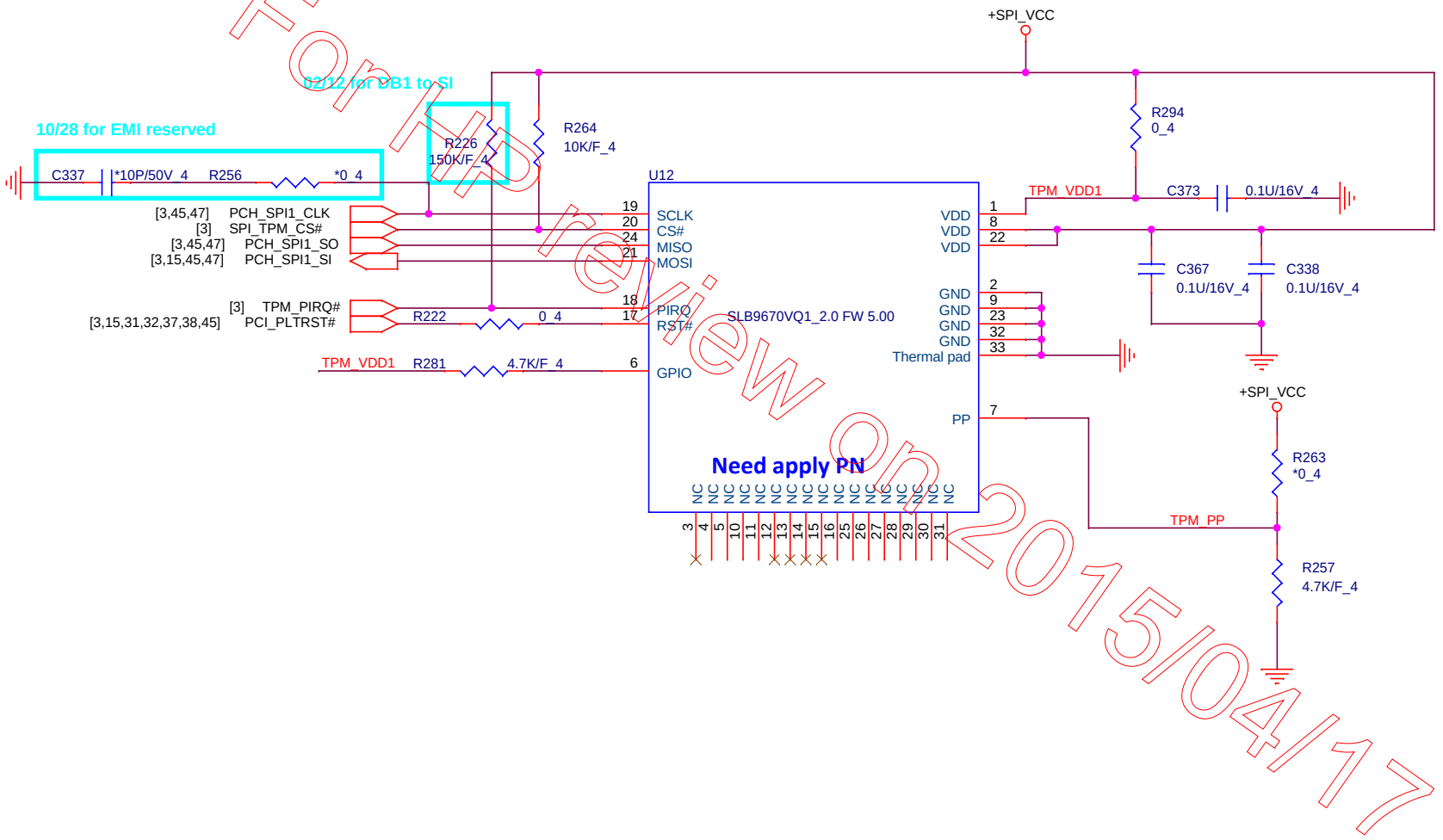
For HP review on 2015/04/17

NB5

PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	33 -- Function Conn.	1A
Date: Friday, April 17, 2015	Sheet 33 of 65	

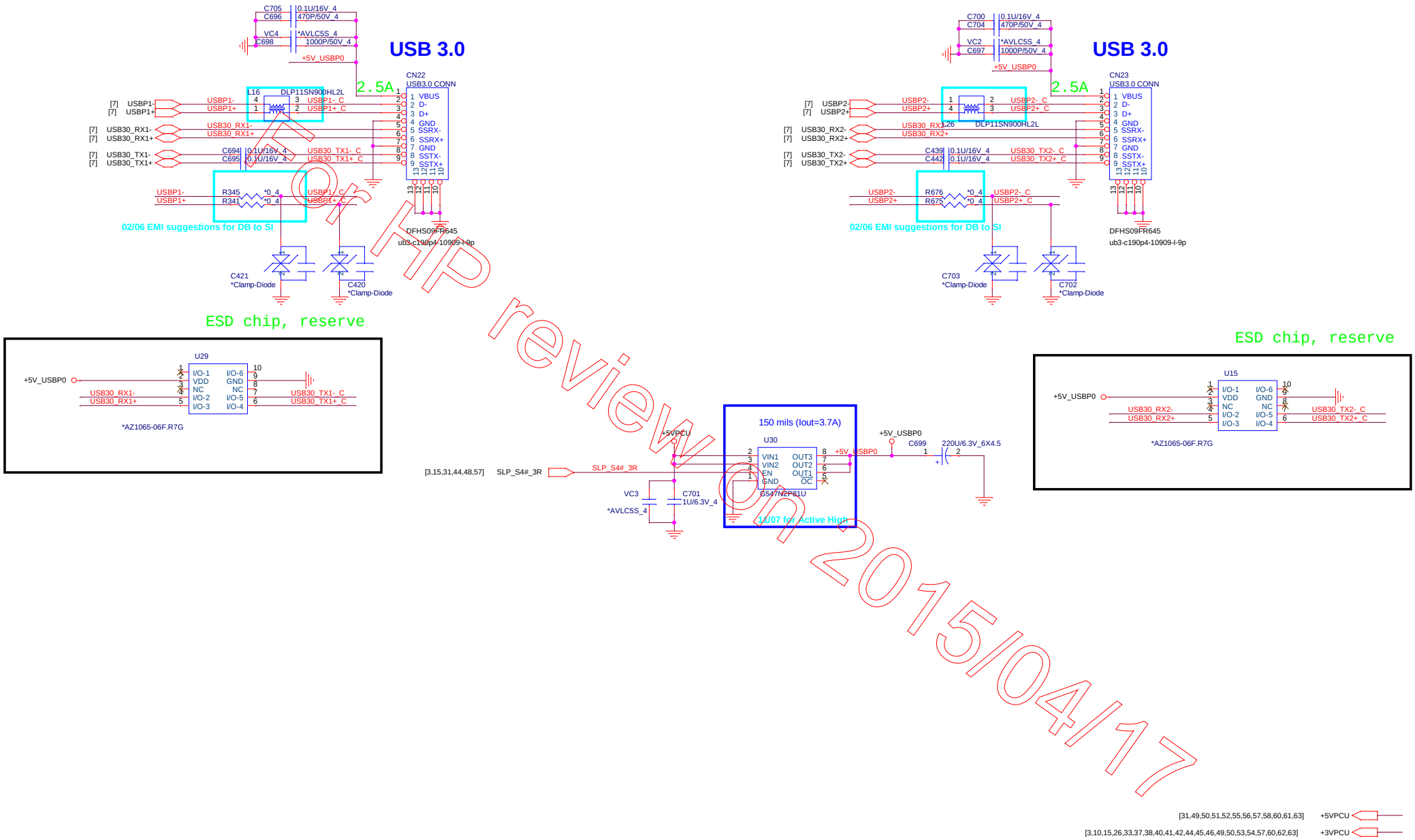
TPM (1.2 or 2.0)



For Review On 2015/04/17

NB5	PROJECT:400 Series Quanta Computer Inc.	
Size: Custom	Document Number: 34 -- TPM SLB9670_QFN	Rev: 1A
Date: Friday, April 17, 2015	Sheet: 34of 65	

USB 2.0/3.0 Combo



For HP review on 2015/04/17

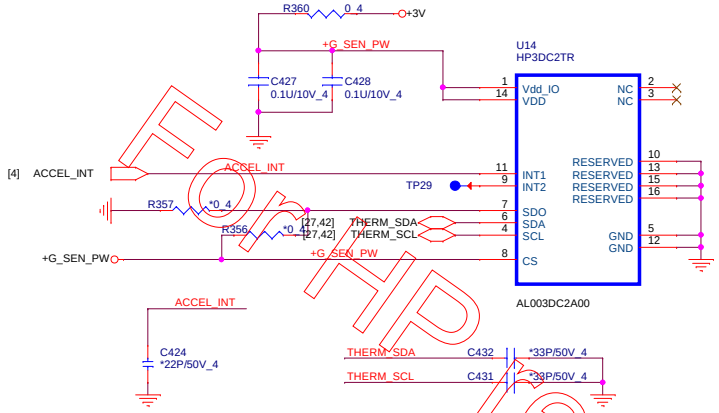
PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	35 -- USB3.0 x2	1A

NB5

Date: Friday, April 17, 2015 Sheet 35 of 65

Accelerometer Sensor



For HP Preview on 2015/04/17

[2,3,4,5,7,8,9,10,15,16,17,24,26,27,28,30,31,32,33,38,42,44,45,49,55,57,63] +3V

[3,10,15,26,33,37,38,40,41,42,44,45,46,49,50,53,54,57,60,62,63] +3VPCU

NB5

PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	36 -- TS and Accelerometer	1A

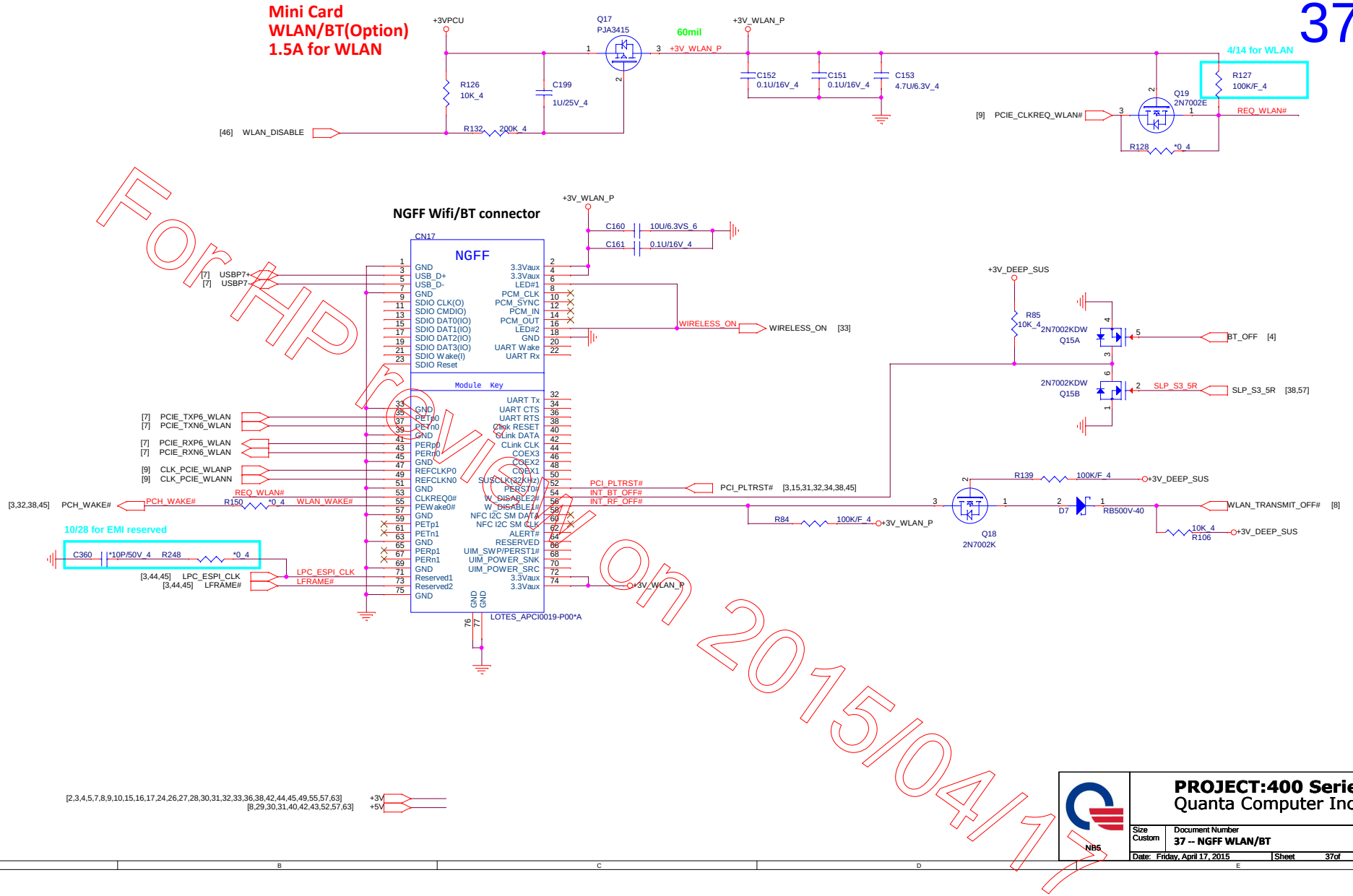
Date: Friday, April 17, 2015 Sheet 36of 65

NGFF WLAN/BT

EC-B-03

Mini Card
WLAN/BT(Option)
1.5A for WLAN

37

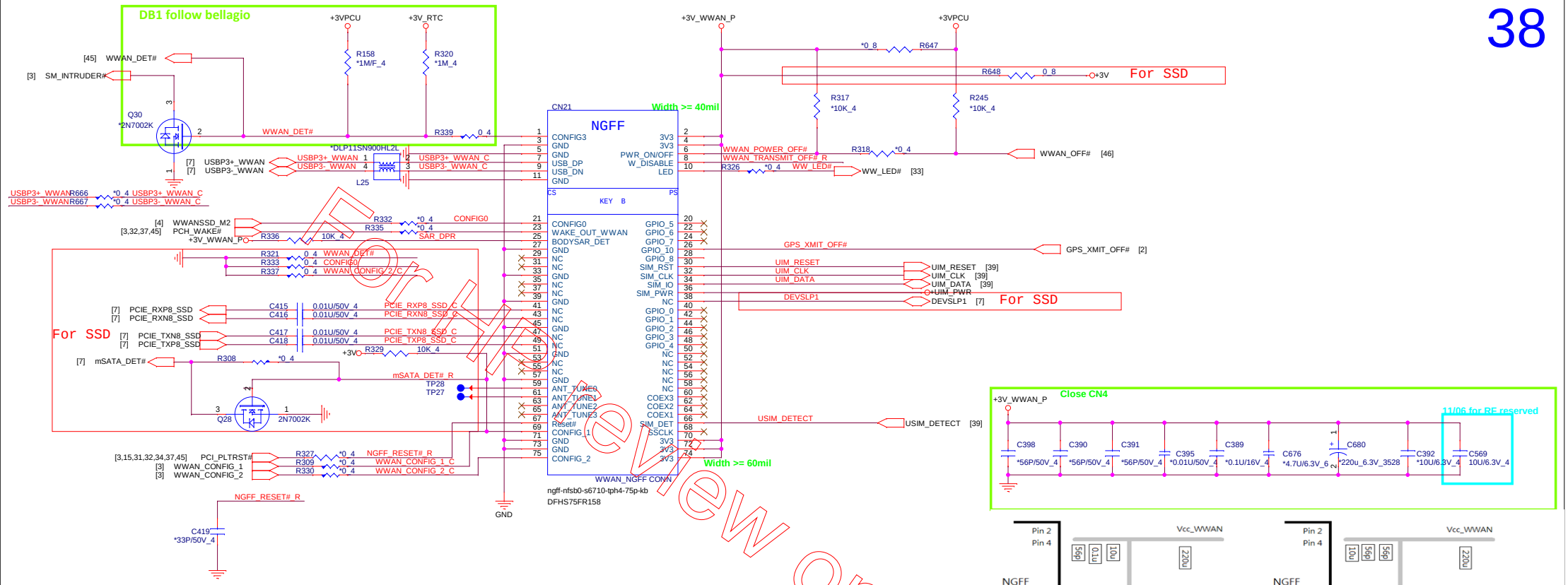


For HP Review on 2015/04/17

PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	37 -- NGFF WLAN/BT	1A

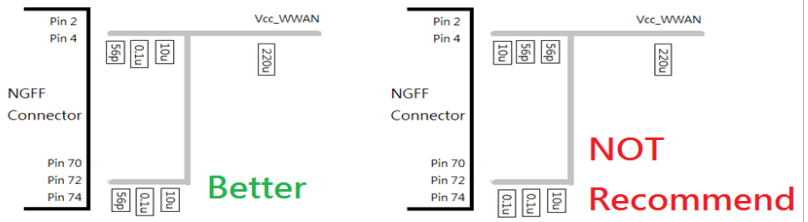
Date: Friday, April 17, 2015 | Sheet 37of 65



Review on 2015/04/17

WWAN(Option)
Control of power must be allowed in all S0, S3, S4 and S5 states.

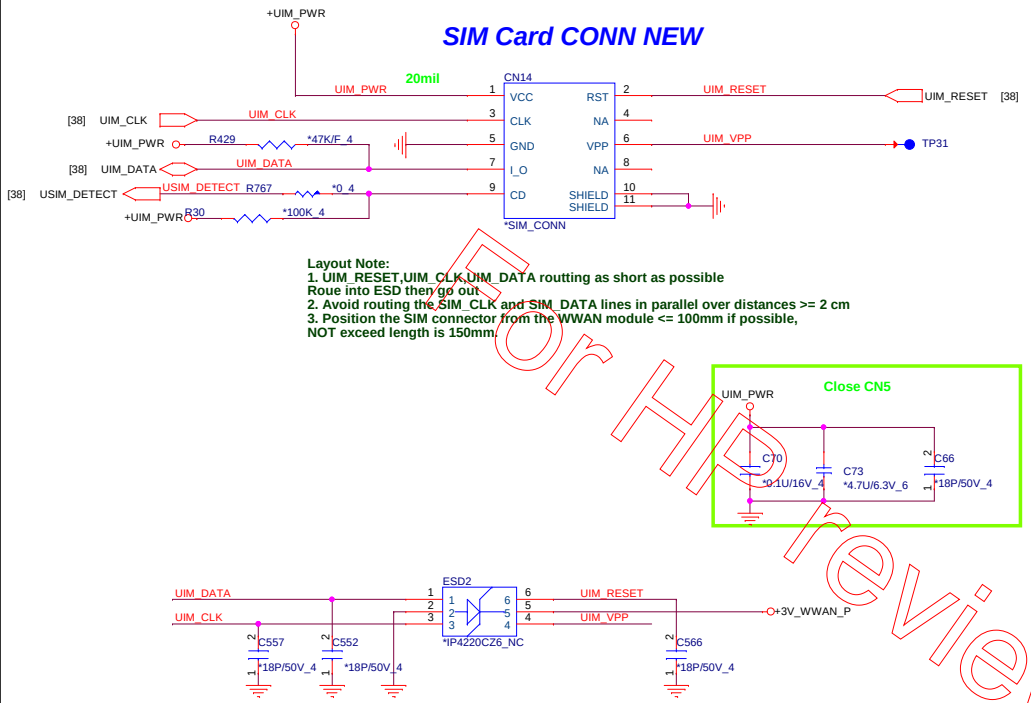
	M.2 Pinout	S0	S3 – S5
WWAN 3.3V	2, 4, 70, 72, 74	On	Off



+VCC	Power_On/Off (Pin6)	W_Disable (Pin8)	GPS_Disable (Pin26)
S0 ON	High	High	High
S3 ON	High	Low	Low
S4 ON	Low	Low	Low
S5 ON	Low	Low	Low

NB5	**PROJECT:400 Series** Quanta Computer Inc.
Size: Custom	Document Number: 38 -- WWAN NGFF/ SSD
Rev: 1A	
Date: Friday, April 17, 2015	Sheet 38 of 65

SIM Card CONN NEW



Trace Length and Routing

- Special attention should be paid to SIM traces (UIM_CLK, UIM_DATA and UIM_RST) to minimize the trace lengths between the SIM slot and the WAN NGFF slot. **Minimizing the signal lengths and traces will reduce possibility of SIM signal integrity issues.** Recommended maximum length is 100mm. Not to exceed length is 150mm.
- Minimum distance between UIM_CLK and UIM_DATA should be 20 mils. Static signals such as UIM_RST can be routed between UIM_CLK and UIM_DATA to conserve space if needed.
- It is recommended that SIM traces be isolated from other high-speed switching signals, as noise can couple into the SIM signals. Keep a minimum distance of 20 mils between UIM_CLK, UIM_DATA and any other high-speed switching signals.
- Placing the SIM card on a daughter card is also not recommended as the interconnect may impact SIM signal integrity.

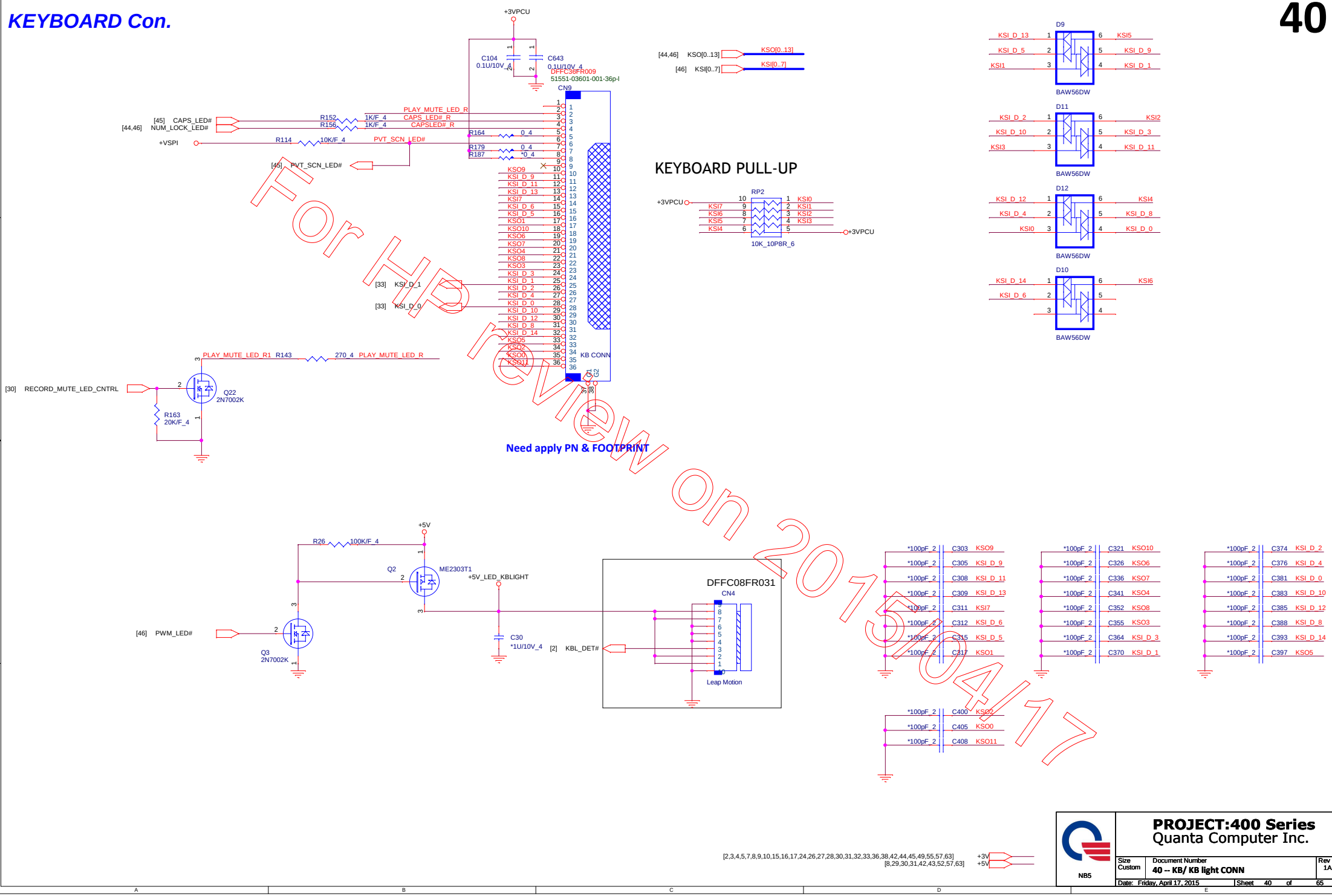
SIM Power

- The UIM_PWR trace width must be at least 20 mils. Sub-planar routing is recommended.
- Implement additional power filtering to SIM card power to ensure clean power is supplied to minimize any possible noise ripple effects. At a minimum, place a 0.1uF and a 4.7uF capacitor on the UIM_PWR supply and locate near the SIM connector.

For HDP review on 2015/04/17

RF cap

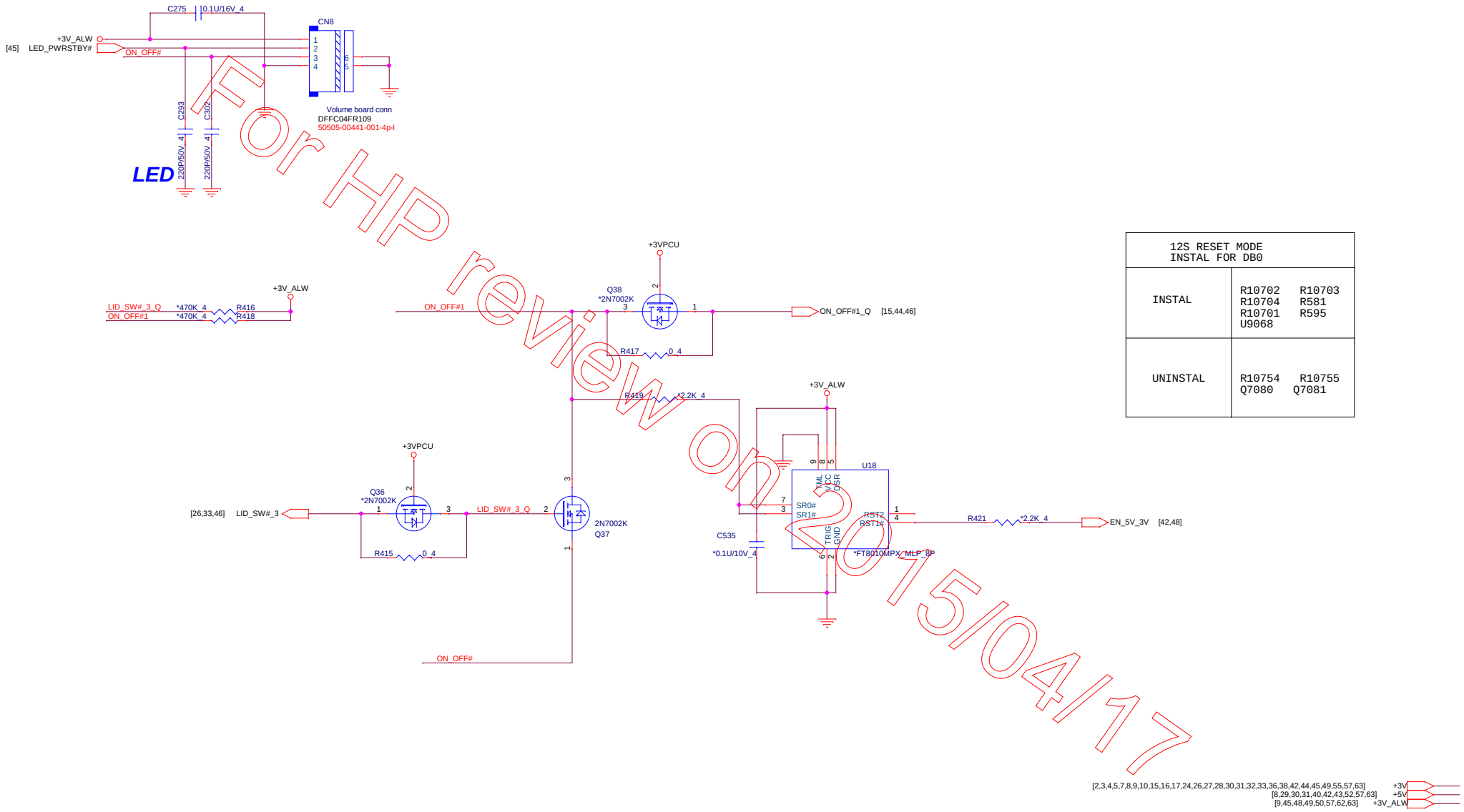
KEYBOARD Con.



For Review on 2015/04/17

NB5	PROJECT:400 Series Quanta Computer Inc.	
	Size: Custom	Document Number: 40 -- KB/ KB light CONN
	Rev: 1A	
	Date: Friday, April 17, 2015	Sheet 40 of 65

Power Botton Connector



12S RESET MODE INSTAL FOR DB0	
INSTAL	R10702 R10703 R10704 R581 R10701 R595 U9068
UNINSTAL	R10754 R10755 Q7080 Q7081

FOR HP review on 2015/04/17

[2,3,4,5,7,8,9,10,15,16,17,24,26,27,28,30,31,32,33,36,38,42,44,45,49,55,57,63] +3V
[8,29,30,31,40,42,43,52,57,63] +5V
[9,45,48,49,50,57,62,63] +3V_ALW

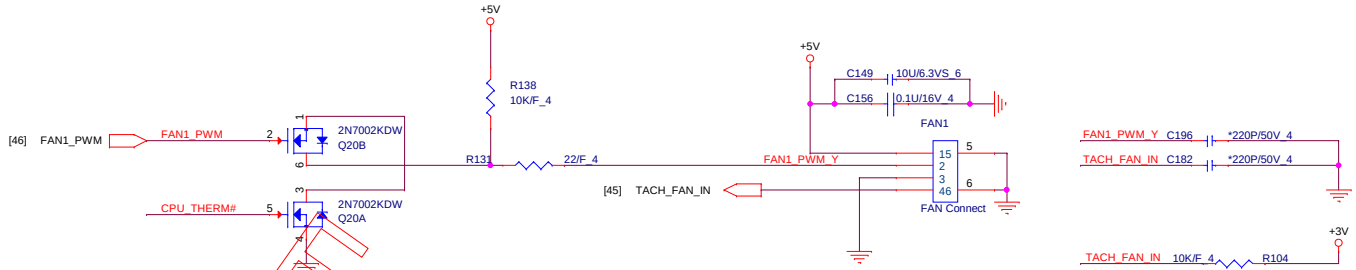
NB5

PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	41 -- Power Button/ HW Reset	1A

Date: Friday, April 17, 2015 Sheet 41 of 65

FAN

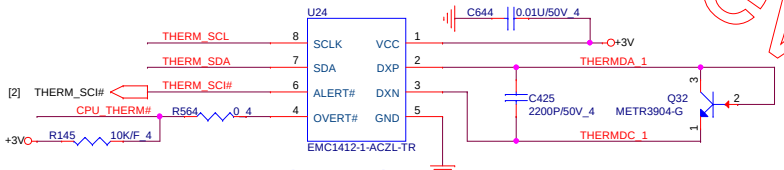


For HP review on 2015/04/17

Thermal sensor

PV, 0416, change HW thermal protect to +3VPCU

CPU Thermal Sensor

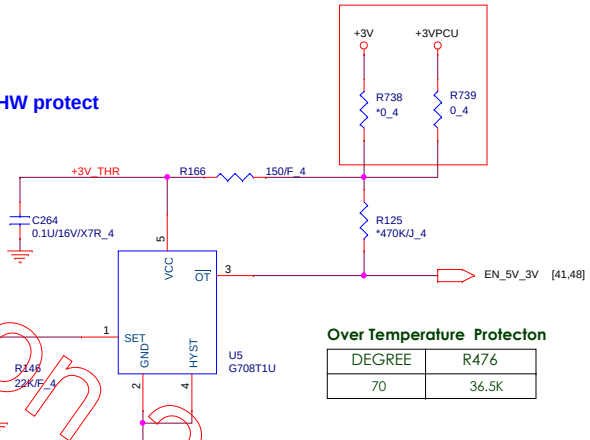


Under Heat Pipe

2nd:AL000431014 TMP431ADGKR

Main: AL000781012 G781P8(98h)

HW protect

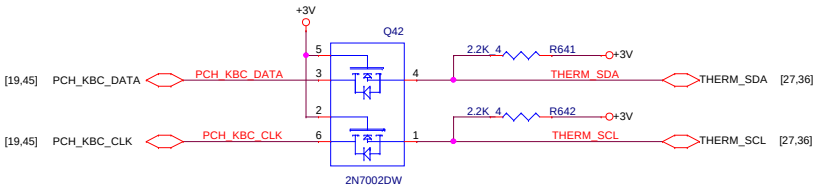


Over Temperature Protecton

DEGREE	R476
70	36.5K

Under CPU

RSET (K OHM) = 0.0012T^2 - 0.9308T + 96.147

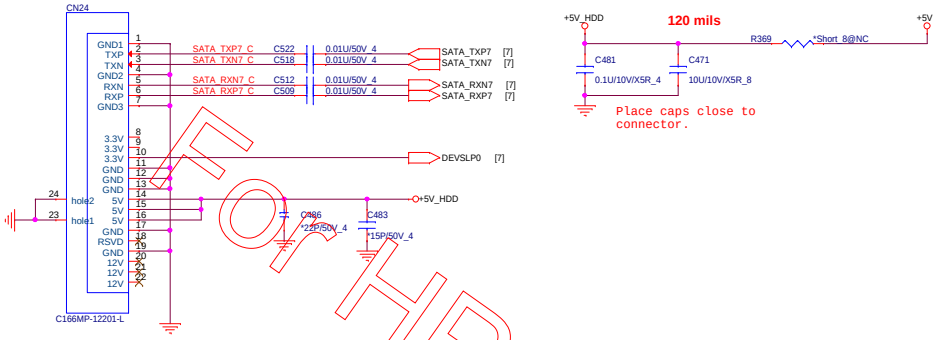


[2,3,4,5,7,8,9,10,15,16,17,24,26,27,28,30,31,32,33,36,38,44,45,49,55,57,63] +3V

[9,41,45,48,49,50,57,62,63] +3V_ALW

NB5	PROJECT:400 Series Quanta Computer Inc.	
Size: Custom	Document Number: 42-- FAN and Thermal IC	Rev: 1A
Date: Friday, April 17, 2015	Sheet 42 of 65	

SATA-HDD



For HP review on 2015/04/17

EMI cap

[2,3,4,5,7,8,9,10,15,16,17,24,26,27,28,30,31,32,33,36,38,42,44,45,49,55,57,63]
[8,29,30,31,40,42,52,57,63]
+3V
+5V

NB5

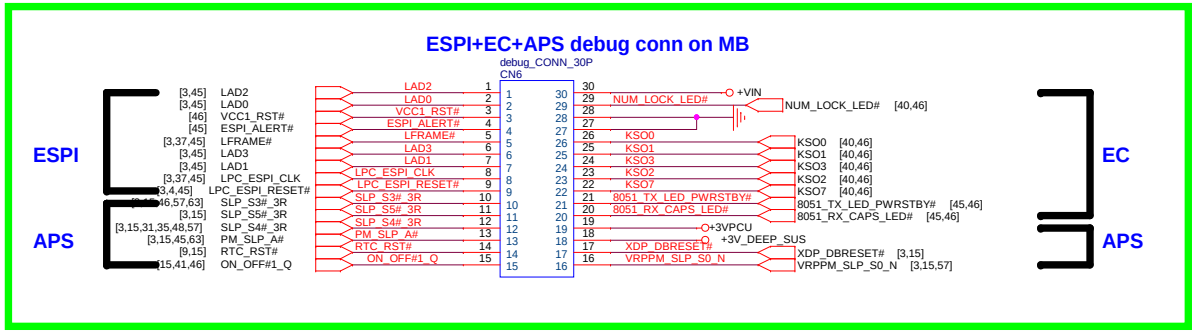
PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
C	43 -- HDD/ EMI cap	1A

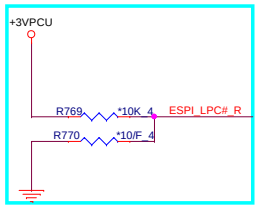
Date: Friday, April 17, 2015 | Sheet 43of 65

For HP review on 2015/04/17

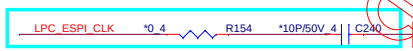
ESPI+EC+APS debug conn on MB



02/10 for Bellagio ESPI



10/28 for EMI reserved



11/04 for check list

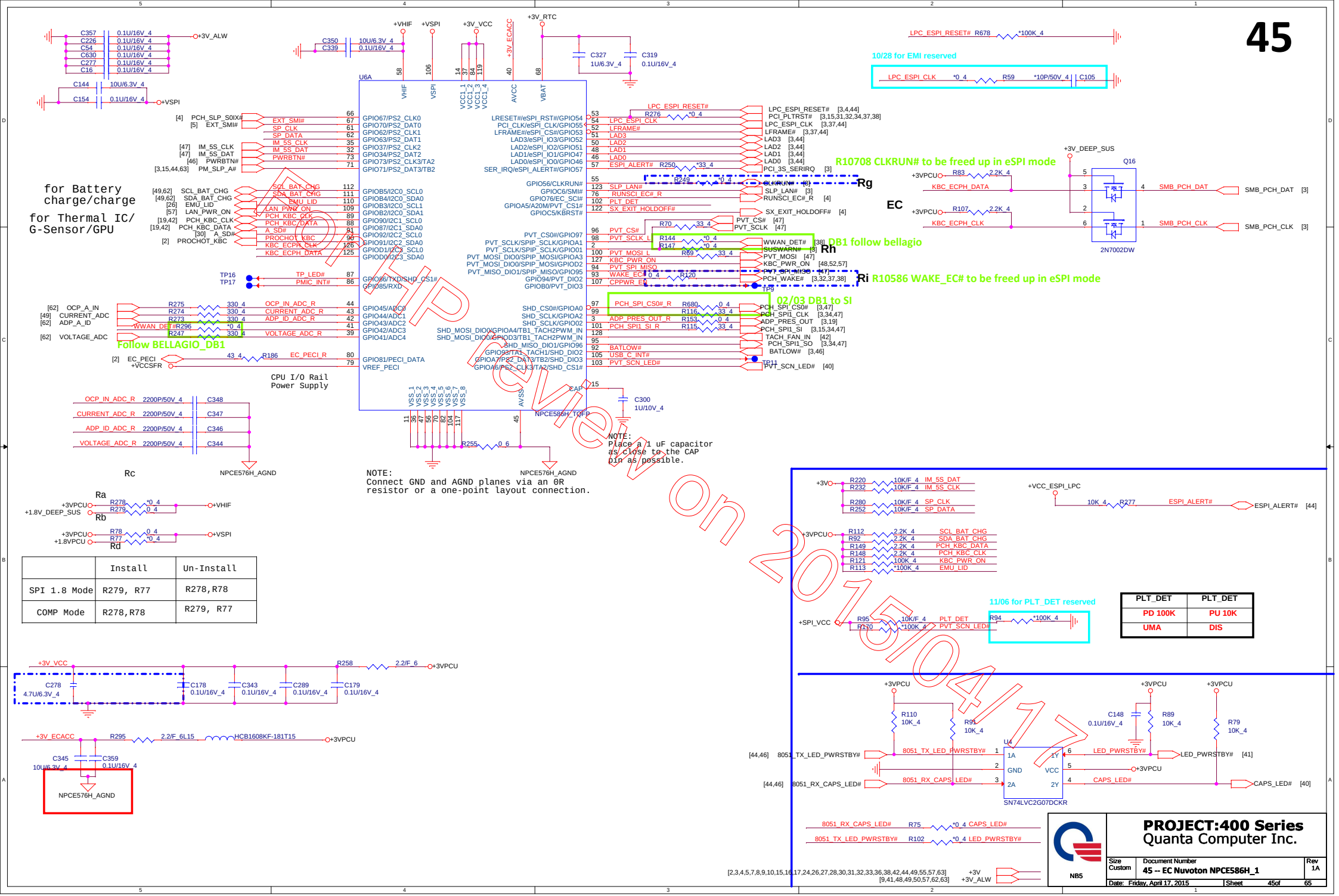
LPC & ESPI TABLE		
	LPC MODE	ESPI MODE
R771	INSTAL	UNINSTAL
R769	UNINSTAL	INSTAL
R770	INSTAL	UNINSTAL

LPC & ESPI TABLE			
		LPC MODE	ESPI MODE
R658	Ra	INSTAL	UNINSTAL
R646	Rb	INSTAL	UNINSTAL
R659	Rc	INSTAL	UNINSTAL
R656	Rd	INSTAL	UNINSTAL
R649	Re	INSTAL	UNINSTAL
R657	Rf	INSTAL	UNINSTAL
R249	Rg	INSTAL	UNINSTAL
R147	Rh	INSTAL	UNINSTAL
R120	Ri	INSTAL	UNINSTAL
R276	Rj	INSTAL	UNINSTAL
R678	Rk	UNINSTAL	INSTAL

NB5

PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	44 -- EC & eSPI/UART debug conn	1A
Date: Friday, April 17, 2015	Sheet 44 of 65	



	Install	Un-Install
SPI 1.8 Mode	R279, R77	R278,R78
COMP Mode	R278,R78	R279, R77

For HP Review on 2015/04/17

All the PWM outputs can directly drive the cathode of a LED connected to 3.3V power

LANPWR ENABLE

U6B

PWR_GOOD_3 72 PWRGD/GPIO72
VCC1_RST# 77 VCC1_RST#/GPO77
PM_PWROK 60 GPIO61/RESET_OUT#
SLP_S4#_KBC R246 1K/F_4 SLP_S4#_KBC_R 38 GPIO40/TA1_TACH1
BAT_GRNLED# 120 GPIOC3/PWM0
PWM_LED# 118 GPIOC2/PWM1
FAN1_PWM 121 GPIOC4/PWM2_TACH2PWM_OUT
ADP_ID_CHK 78 GPIO80/PWM3_LED3
AMBER_BATLED# 113 GP(I)OB6/PWM4_LED0/SPI_COMP#
8051_RX_CAPS_LED# 114 GPIOB7/PWM5_LED1
8051_TX_LED_PWRSTBY# 115 GPIOC0/PWM6_LED2
OCP_PWM_OUT 59 GPIO60/PWM7
DPWROK R135 0_4 1 GPIO00
WLAN_DISABLE 30 GPO32/TRIS#
TP_SCAN_DISABLE# 31 GPIO33
WWAN_OFF# 33 GPO35/TEST#
DPHDMI_PD 34 GPIO36
R786 *0_4 ADP_DET_R 49 GPIO50
ME_UNLOCK# 63 GPIO64
LID_SW#_3 64 GPIO65
MAIN_BAT_DET# 65 GPIO66
R797 *0_4 ADP_PRES_R 74 GPIO74
RSMRST# R151 1K/F_4 85 GPIO84
R768 10K_4 116 GPIOC1
124 GPIOC7
RSMRST_PG R109 0_4
DTR#_BOUT
NPCE586H_TQFP

KSO00/GPO21/JTAG_TCK0_SWCLK0 21 KSO0 KSO0 [40,44]
KSO01/GPO20/JTAG_TMS0_SWIO0 20 KSO1 KSO1 [40,44]
KSO02/GPO17/JTAG_TDI0 19 KSO2 KSO2 [40,44]
KSO03/GPO16/JTAG_TDO0_SWO0 18 KSO3 KSO3 [40,44]
KSO04/GPO15/XNOR 17 KSO4 KSO4 [40]
KSO05/GPO14 16 KSO5 KSO5 [40]
KSO06/GPO13 13 KSO6 KSO6 [40]
KSO07/GPO12/JEN0# 12 KSO7 KSO7 [40,44]
KSO08/GPO11/CR_SOUT 10 KSO8 KSO8 [40]
KSO09/GPO10/CR_SIN 9 KSO9 KSO9 [40]
KSO10&P80_CLK/GPIO07 8 KSO10 KSO10 [40]
KSO11&P80_DAT/GPIO06 7 KSO11 KSO11 [40]
KSO12/GPO05 6
KSO13/GPO04 5
KSO14/GPO82 81 SLP_S3#_3R_KBC 1K/F_4 R177 SLP_S3#_3R [3,15,44,57,63]
KSO15/GPO83 83 NUM_LOCK_LED# [40,44]
KSO16/GPO03 4 PWR_BTN_OUT# [3]
KSO17/GPOB1 108 KSO17 KSO17 [33]

KSI0/GPIO31/TRACEDATA3 29 KSI0 KSI0 [40]
KSI1/GPIO30/TRACEDATA2 28 KSI1 KSI1 [40]
KSI2/GPIO27/TRACEDATA1 27 KSI2 KSI2 [40]
KSI3/GPIO26/TRACEDATA0 26 KSI3 KSI3 [40]
KSI4/GPIO25/TRACECLK 25 KSI4 KSI4 [40]
KSI5/GPIO24 24 KSI5 KSI5 [40]
KSI6/GPIO23 23 KSI6 KSI6 [40]
KSI7/GPIO22 22 KSI7 KSI7 [40]

GPIO75/32KHZ_OUT 75 PCH_SLP_SUS# PCH_SLP_SUS# [3]
GPIOE7/32KCLIN 69 SUSCLK32_KBC SUSCLK32_KBC [9]

ME_UNLOCK# 100K/F_4 R253 +3VPCU
LID_SW#_3 470K_4 R254
VCC1_RST# 100K/F_4 R198
AMBER_BATLED# *10K/F_4 R111
NUM_LOCK_LED# 100K/F_4 R168

WWAN_OFF# *1K/F_4 R244
PM_PWROK 20K/F_4 R251
VCC1_RST# *10K/F_4 R197
WLAN_DISABLE *1K/F_4 R133
ADP_ID_CHK 100K/F_4 R193

ESD SOLUTION
KSO7 R165 *1K/F_4

02/09 for Ji-An suggestions for DB to SI

RSMRST# 2 1 RSMRST_PG
*RB500V-40 D23

ADP_DET R798 0_4 ADP_PRES_R

PV, 0415 add R798 connect ADP_DET and ADP_PRES_R

CPU Throttling

Q21A 2N7002KDW
Dual
OCP_OC# [8]
OCP_PWM_OUT
[3,4,8,18] PLTRST# PLTRST#
[4] NMI_SMI_DBG# NMI_SMI_DBG# BATLOW# BATLOW# [3,45]
Q21B 2N7002KDW

+3VPCU
R210 100K/F_4
+3VPCU
R219 100K/F_4
[15,41,44] ON_OFF#1_Q ON_OFF#1_Q R205 47_4 PWRBTN#
R209 *0_4 PWR_BTN_OUT#
PWRBTN# [45]
C313 1U/6.3V_4

NOTE : IF INSTALL R10603, PLEASE UNINSTALL R224

Intel review on 20150417

NB5

PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	46 -- EC Nuvoton NPCE586H_2	1A
Date: Friday, April 17, 2015	Sheet 46of 65	

SPI ROM

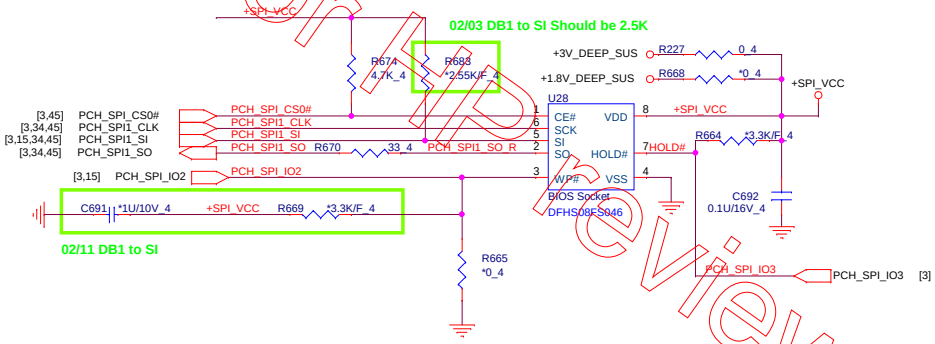
Vender	Size	P/N
Winbond	128MB	AKE3DZN0N01
Socket		DFHS08FS023

Vender	Size	P/N
Winbond	16MB	AKE38FP0N03
Socket		DFHS08FS023

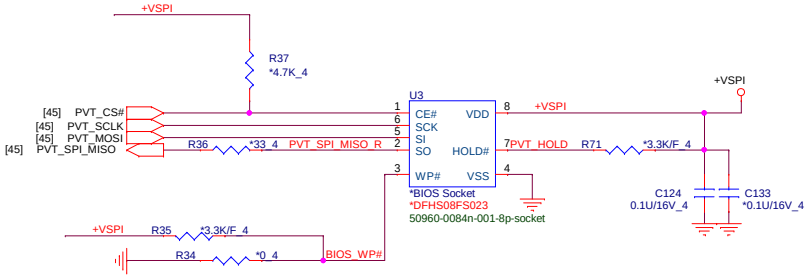
For AMD Review on 2015/04/17

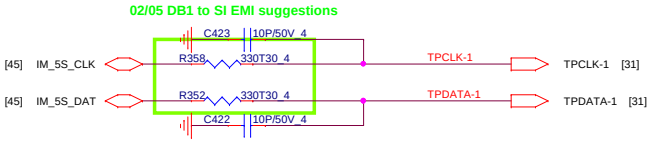
PCH SPI ROM(CLG)

PCH 6*5mm WSON 16M SPI ROM Socket



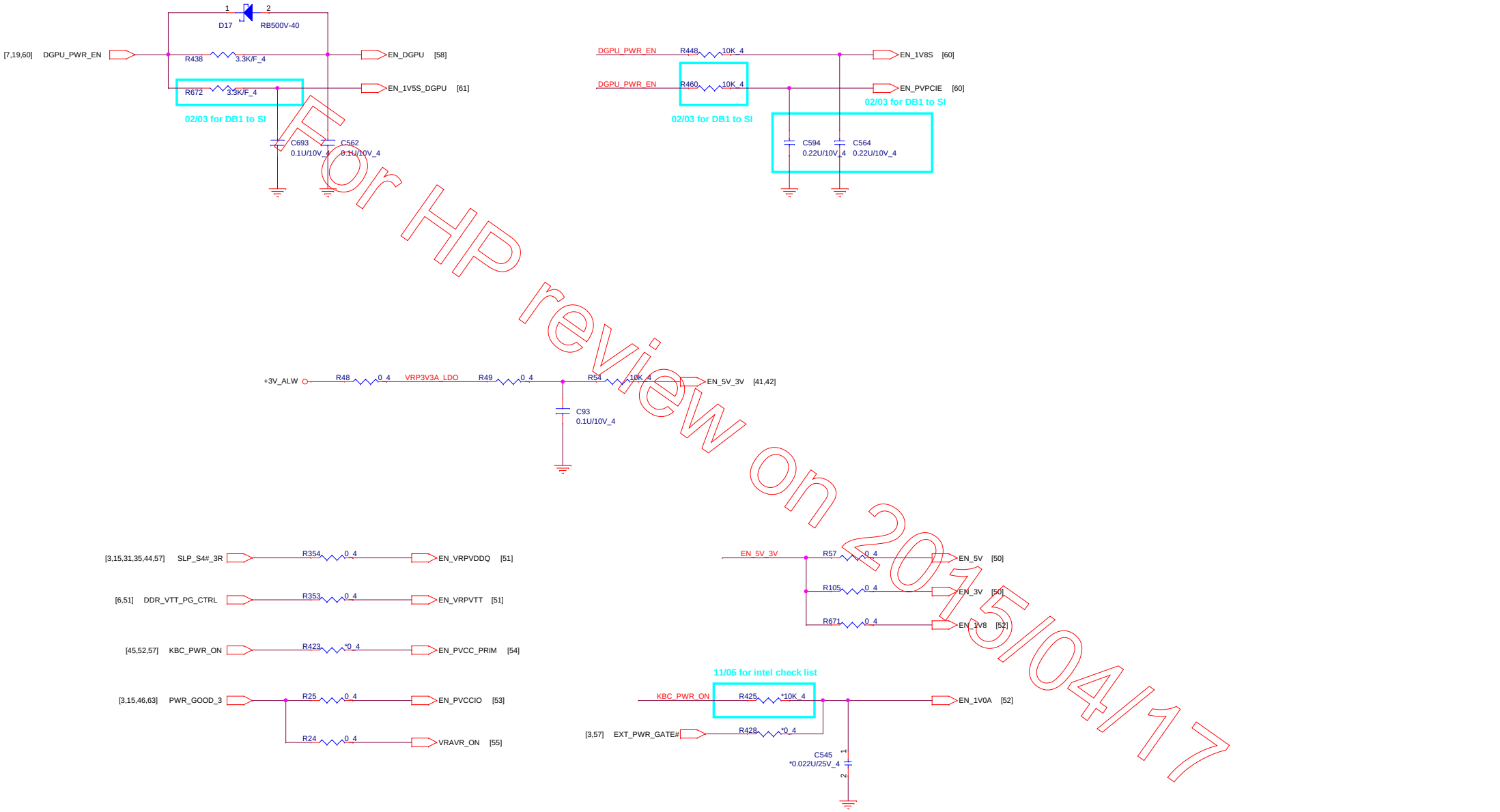
EC 6*5mm WSON 8M SPI ROM Socket





NB5	PROJECT:400 Series Quanta Computer Inc.		
	Size: Custom	Document Number: 47 -- Flash(KBC+PCH)	Rev: 1A
	Date: Friday, April 17, 2015	Sheet: 47of	65

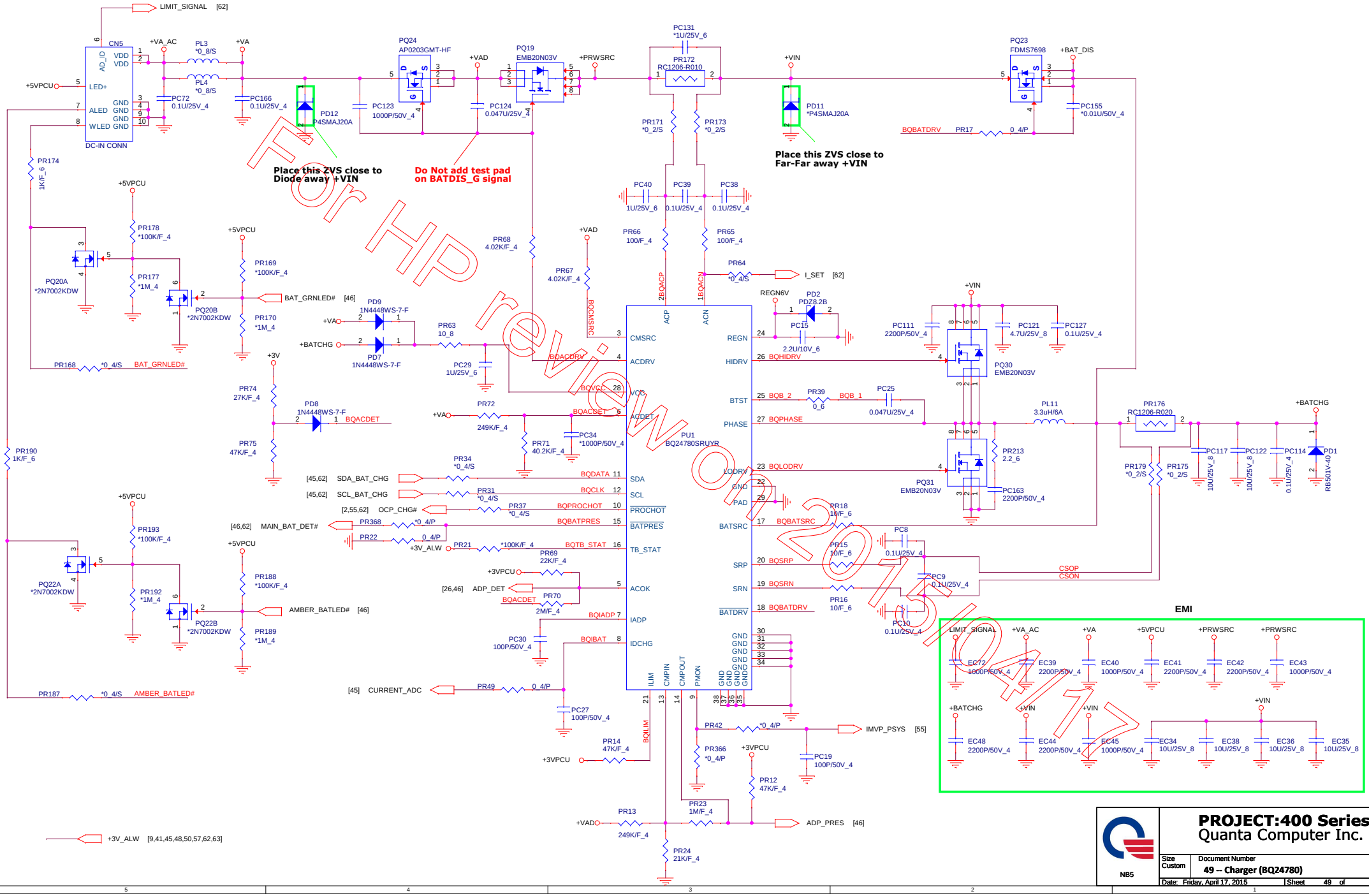
POWER TO EE NET NAME CONNECTION



For HP review on 2015/04/17

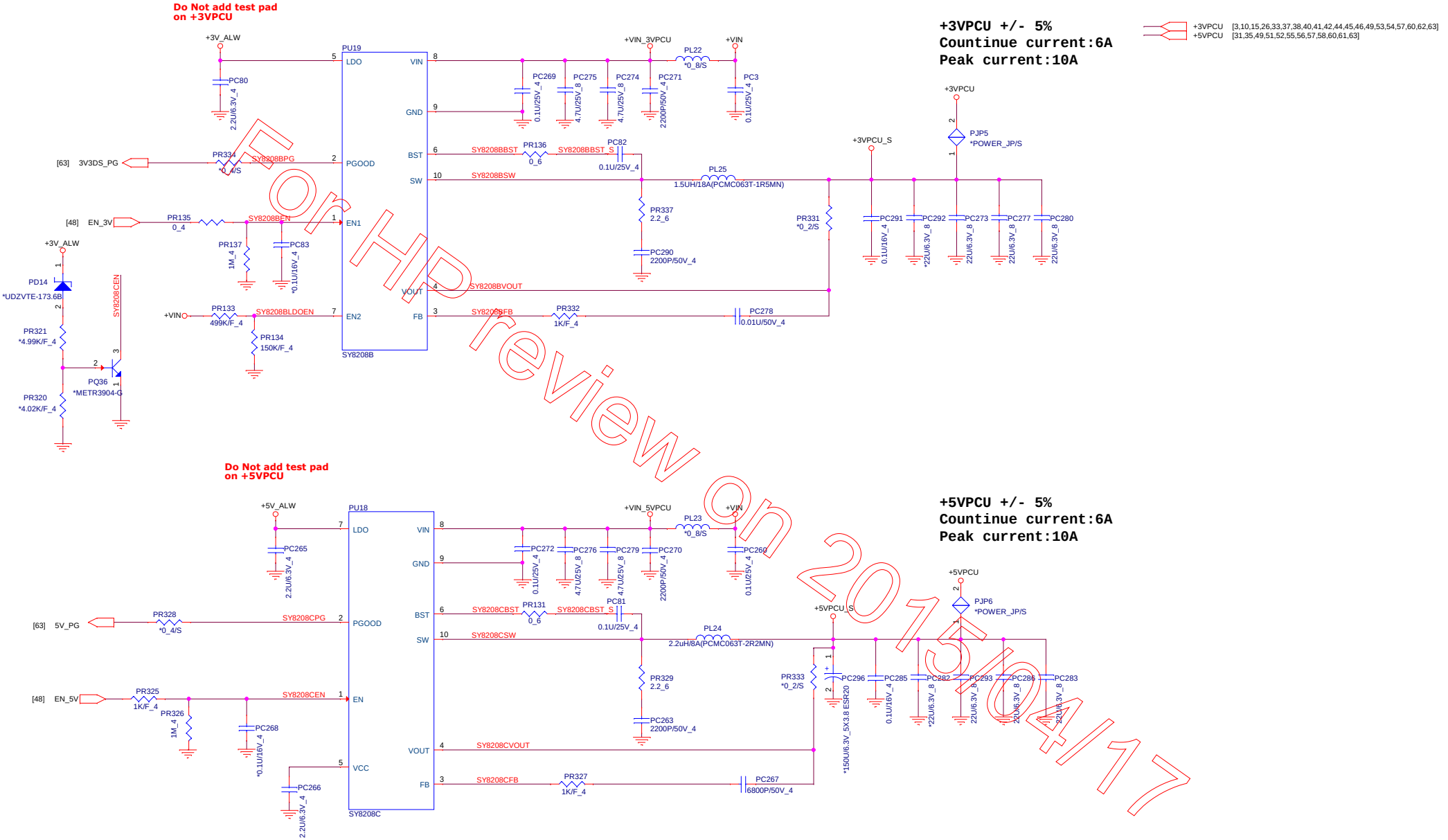
NB5	PROJECT:400 Series Quanta Computer Inc.	
Size: Custom	Document Number: 48 -- POWER ENABLE	Rev: 1A
Date: Friday, April 17, 2015	Sheet 48of 65	

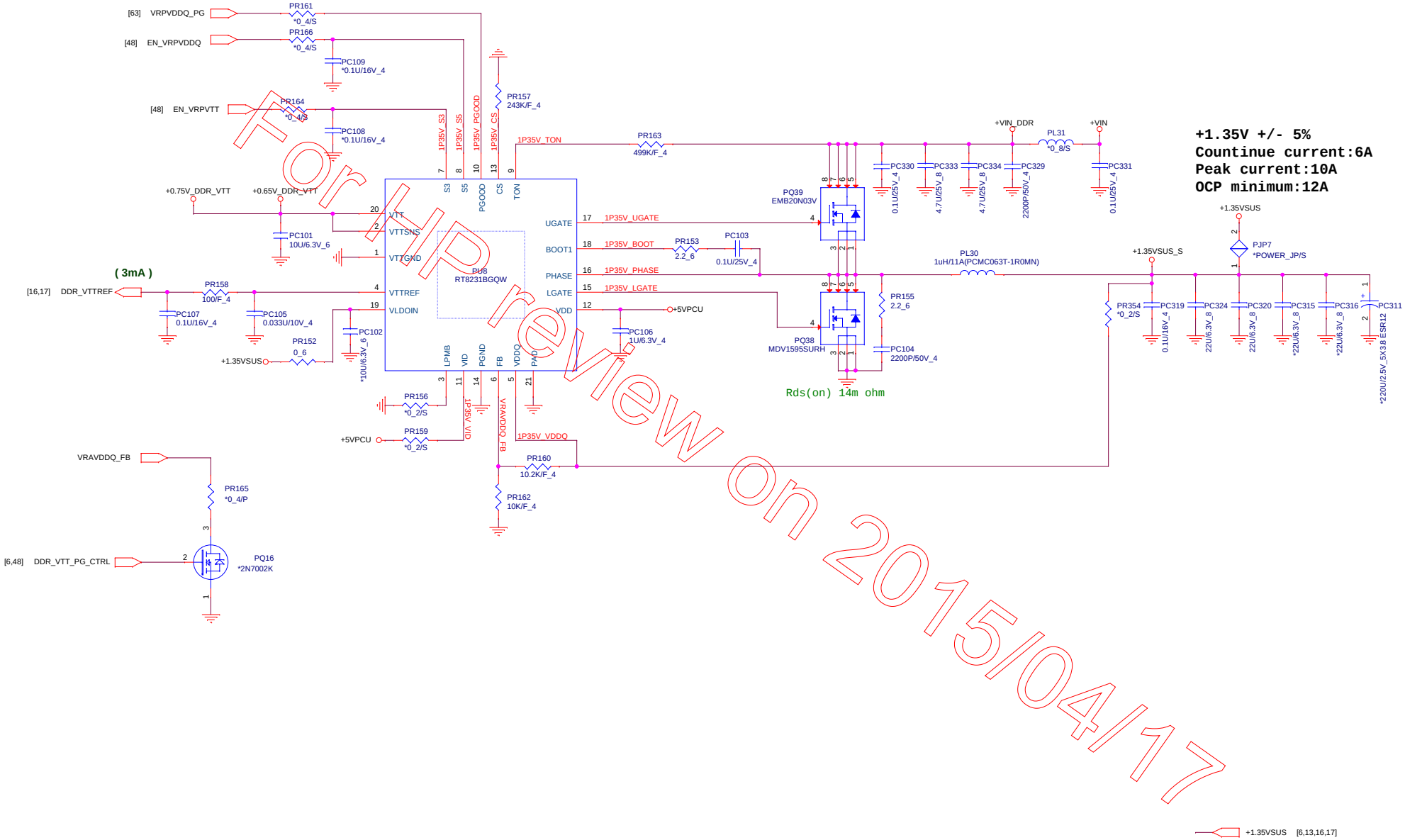
90W DC_JACK



For HP Review Only 2015

NB5	PROJECT:400 Series Quanta Computer Inc.	
Size: Custom	Document Number: 49 -- Charger (BQ24780)	Rev: 1A
Date: Friday, April 17, 2015	Sheet 49 of 65	


Do Not add test pad on +3VPCU
+3VPCU +/- 5%
Countinue current:6A
Peak current:10A
+3VPCU [3,10,15,26,33,37,38,40,41,42,44,45,46,49,53,54,57,60,62,63]
+5VPCU [31,35,49,51,52,55,56,57,58,60,61,63]
+3V_ALW
PU19
LDO
VIN
GND
BST
SW
EN1
PGOOD
EN2
VOUT
FB
SY8208B
+VIN_3VPCU
+VIN
PL22
*0_8/S
PC80
2.2U/6.3V_4
PC269
PC275
PC274
PC271
PC3
0.1U/25V_4
4.7U/25V_8
2200P/50V_4
[63] 3V3DS_PG
PR334
*0_4/S
SY8208BPG
SY8208BBST
PR136
0_6
PC82
SY8208BBST_S
SY8208BSW
PL25
1.5UH/18A(PCMC063T-1R5MN)
+3VPCU_S
PJP5
*POWER_JP/S
PR337
2.2_6
PC290
PR331
*0_2/S
PC291
PC292
PC273
PC277
PC280
22U/6.3V_8
*22U/6.3V_8
[48] EN_3V
PR135
SY8208BEN
PR137
1M_4
PC83
*0.1U/16V_4
PD14
*UDZVTE-173.6B
PR321
*4.99K/F_4
PQ36
*METR3904-G
PR320
*4.02K/F_4
SY8208CEN
+VIN
PR133
499K/F_4
SY8208BLDOEN
PR134
150K/F_4
SY8208BVOUT
SY8208BFB
PR332
1K/F_4
PC278
0.01U/50V_4
Do Not add test pad on +5VPCU
+5V_ALW
PU18
+VIN_5VPCU
PL23
PC265
PC272
PC276
PC279
PC270
PC260
[63] 5V_PG
PR328
SY8208CPG
PR131
PC81
SY8208CBST
SY8208CBST_S
SY8208CSW
PL24
2.2uH/8A(PCMC063T-2R2MN)
+5VPCU_S
PJP6
*POWER_JP/S
PR329
2.2_6
PC263
2200P/50V_4
PR333
*0_2/S
PC296
*150U/6.3V_5X3.8 ESR20
PC285
PC282
PC293
PC286
PC283
[48] EN_5V
PR325
1K/F_4
PR326
1M_4
SY8208CEN
PC268
*0.1U/16V_4
PC266
SY8208CVOUT
SY8208CFB
PR327
1K/F_4
PC267
6800P/50V_4
SY8208C
For Hp review on 2015/04/17
PROJECT:400 Series
Quanta Computer Inc.
NB5
Size
Document Number
50 -- 3/5VS5 (SY8208B/SY8208C)
Rev
1A
Date: Friday, April 17, 2015
Sheet 50 of 65

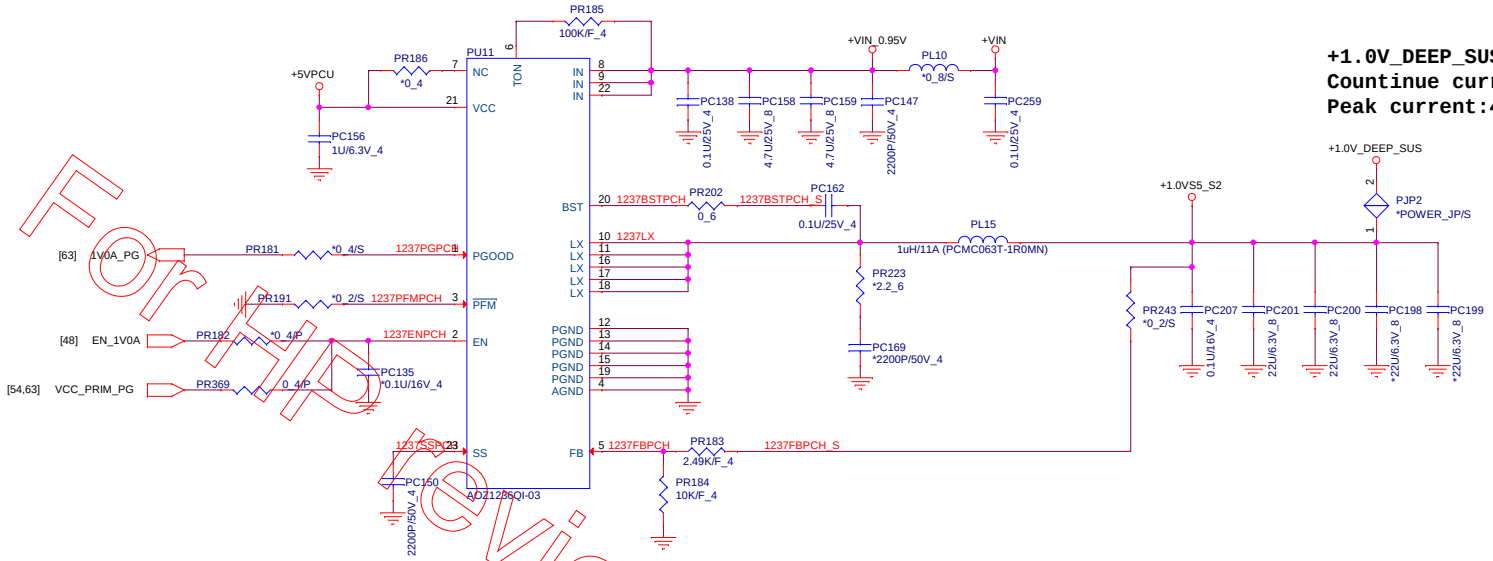


For Review on 2015/04/17

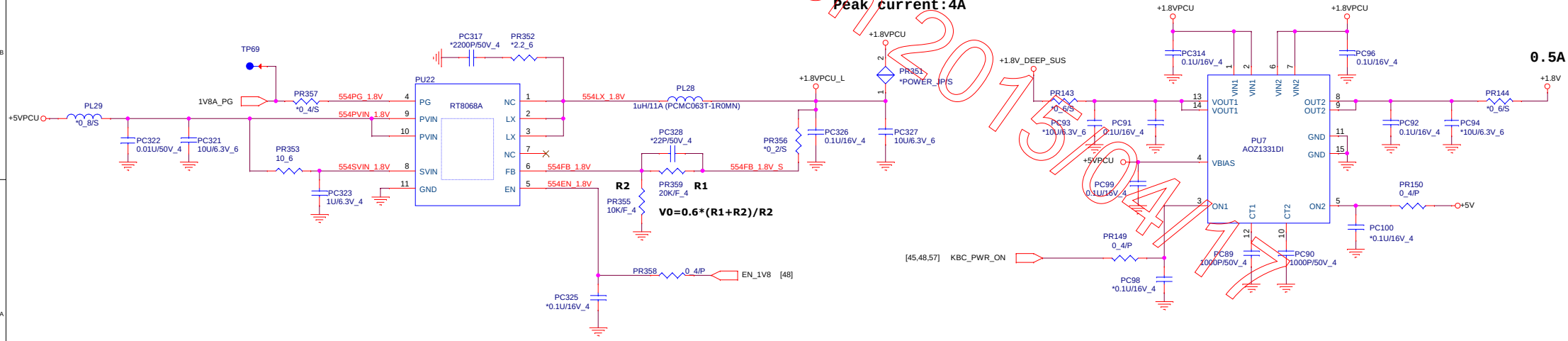
NB5	PROJECT:400 Series Quanta Computer Inc.	
Size	Document Number 51 -- DDR3 (RT8231B)	Rev 1A
Date: Friday, April 17, 2015	Sheet 51 of 65	

For Review Only

+1.0V_DEEP_SUS +/- 5%
Countinue current:2A
Peak current:4A



+1.8VPCU +/- 5%
Countinue current:2A
Peak current:4A

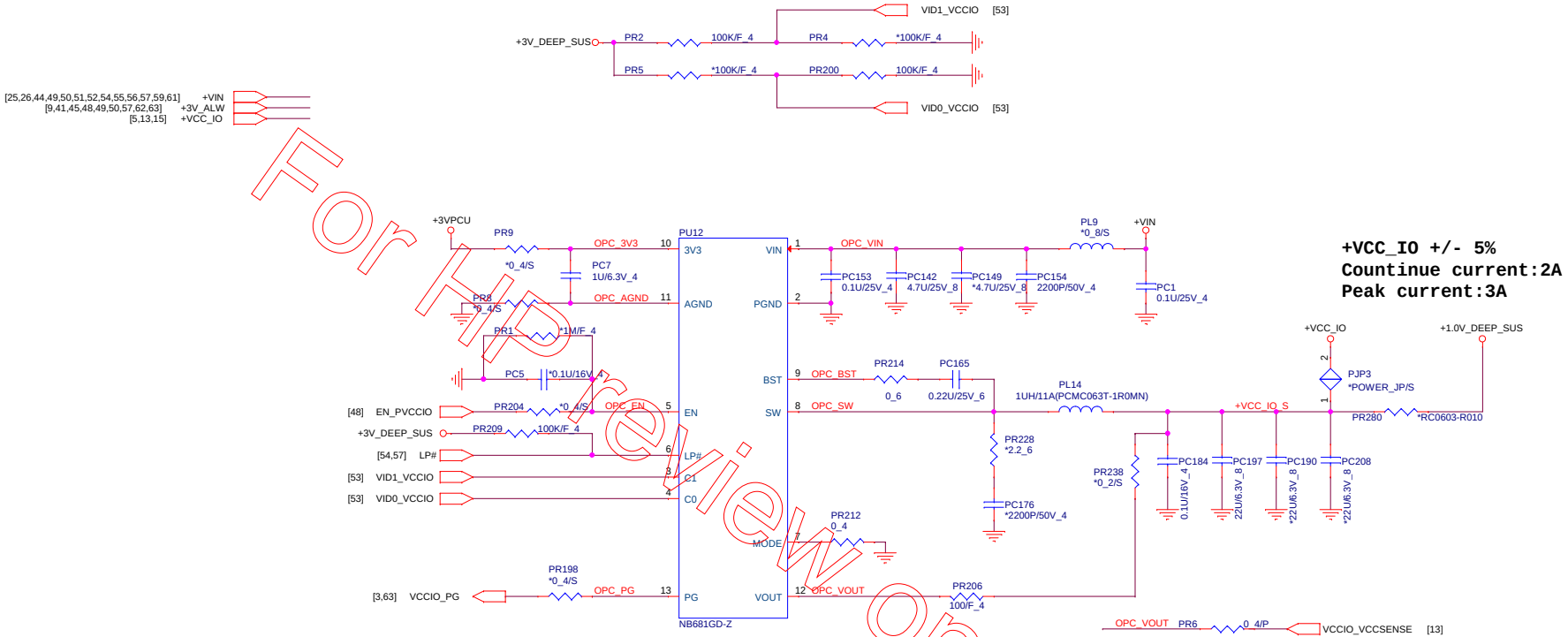


+VIN [25,26,44,49,50,51,53,54,55,56,57,59,61]
+3VPCU [3,10,15,26,33,37,38,40,41,42,44,45,46,49,50,53,54,57,60,62,63]
+5VPCU [31,35,49,50,51,55,56,57,58,60,61,63]

NB5

PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
	52 -- +1.0VS5/1.8VS5	1A
Date: Friday, April 17, 2015	Sheet 52 of 65	



+VCC_IO +/- 5%
Countinue current:2A
Peak current:3A

VCCIO

LP#	C1	C0	Vout
0	X	X	0
1	0	0	0.85
1	0	1	0.875
1	1	0	0.95
1	1	1	0.975

MODE

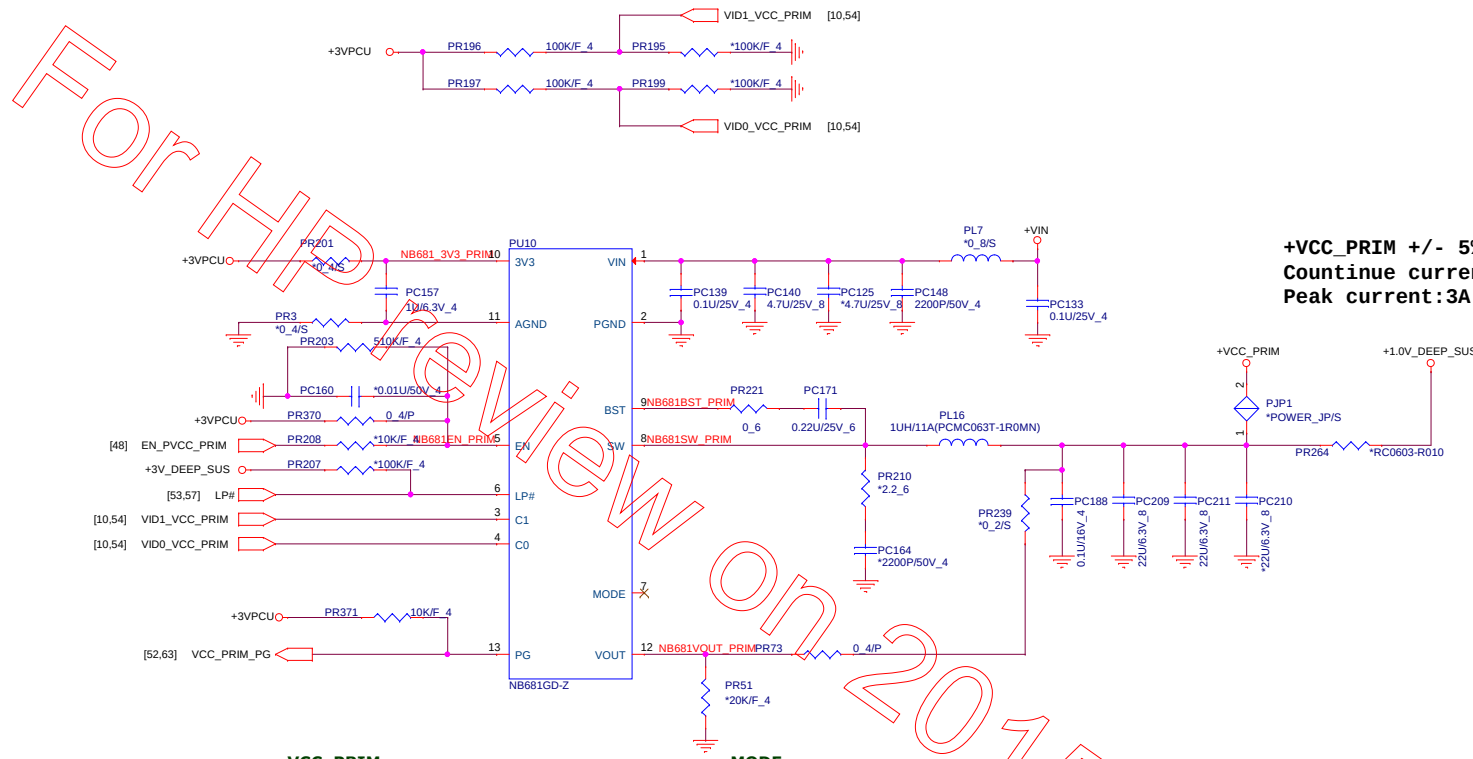
	VR rail	Resistor
M1	VCCIO	0
M2	PRIMCORE	Float
M3	EDRAM/EOPIO	100K
M4	other	150K

For Review on 2015/04/17

PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
	53 -- +VCC_IO (NB681)	1A
Date: Friday, April 17, 2015	Sheet 53 of 65	

NB5



+VCC_PRIM +/- 5%
Countinue current:2A
Peak current:3A

For HP Review on 2015/04/17

VCC_PRIM

LP#	C1	C0	Vout
0	X	X	0.7
1	0	0	0.8
1	0	1	0.9
1	1	0	0.95
1	1	1	1.0

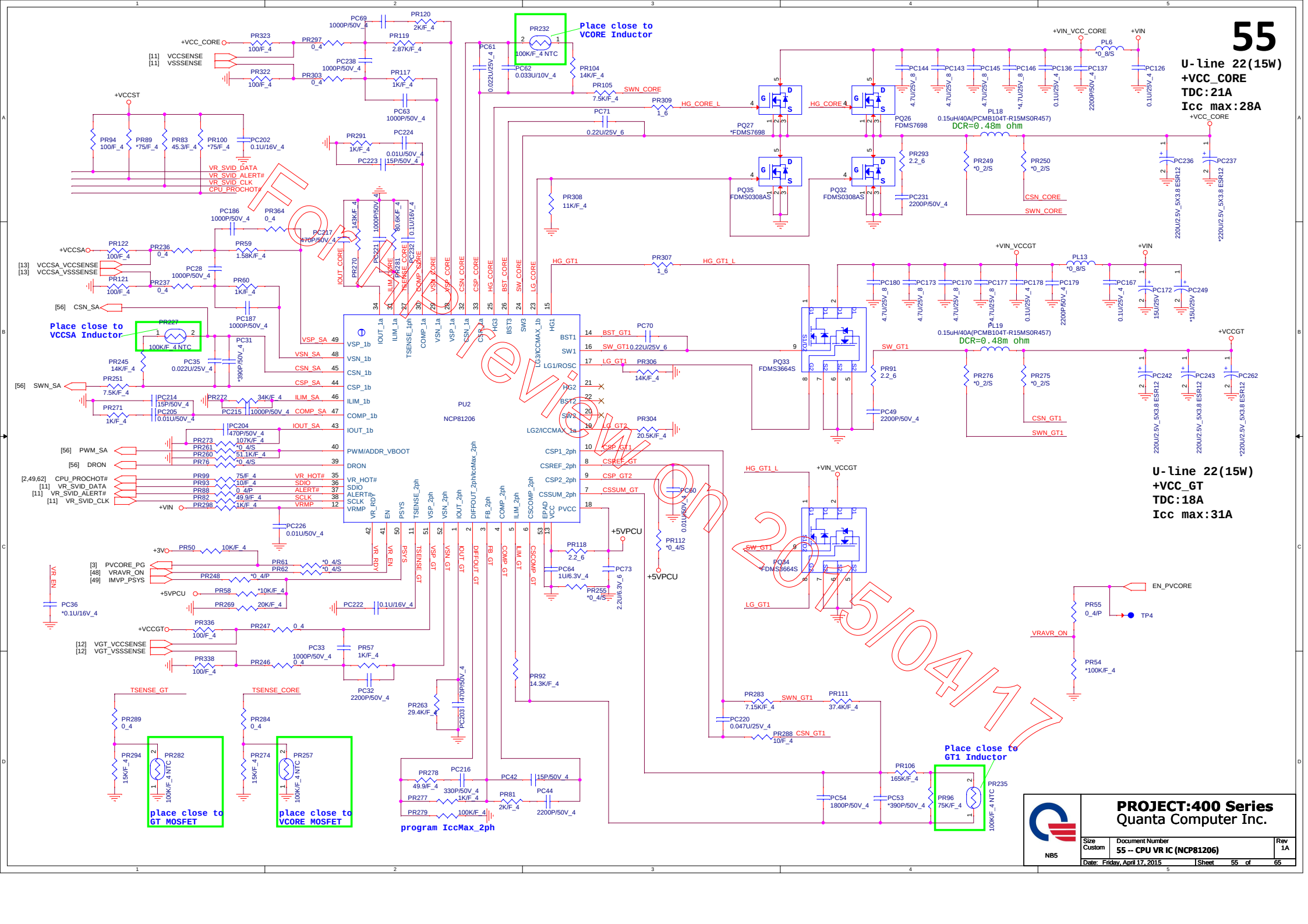
MODE

	VR rail	Resistor
M1	VCCIO	0
M2	PRIMCORE	Float
M3	EDRAM/EOPIO	100K
M4	other	150K

PROJECT:400 Series
Quanta Computer Inc.

NB5

Size	Document Number	Rev
	54 -- +VCC_PRIM (NB681)	1A
Date: Friday, April 17, 2015	Sheet 54 of 65	


55
U-line 22(15W)
+VCC_CORE
TDC:21A
Icc max:28A
U-line 22(15W)
+VCC_GT
TDC:18A
Icc max:31A
Place close to VCORE Inductor
Place close to VCCSA Inductor
Place close to GT1 Inductor
place close to GT MOSFET
place close to VCORE MOSFET
program IccMax_2ph
PU2
NCP81206
DCR=0.48m ohm
DCR=0.48m ohm
PROJECT:400 Series
Quanta Computer Inc.
NB5
Size Custom
Document Number
55 -- CPU VR IC (NCP81206)
Rev 1A
Date: Friday, April 17, 2015
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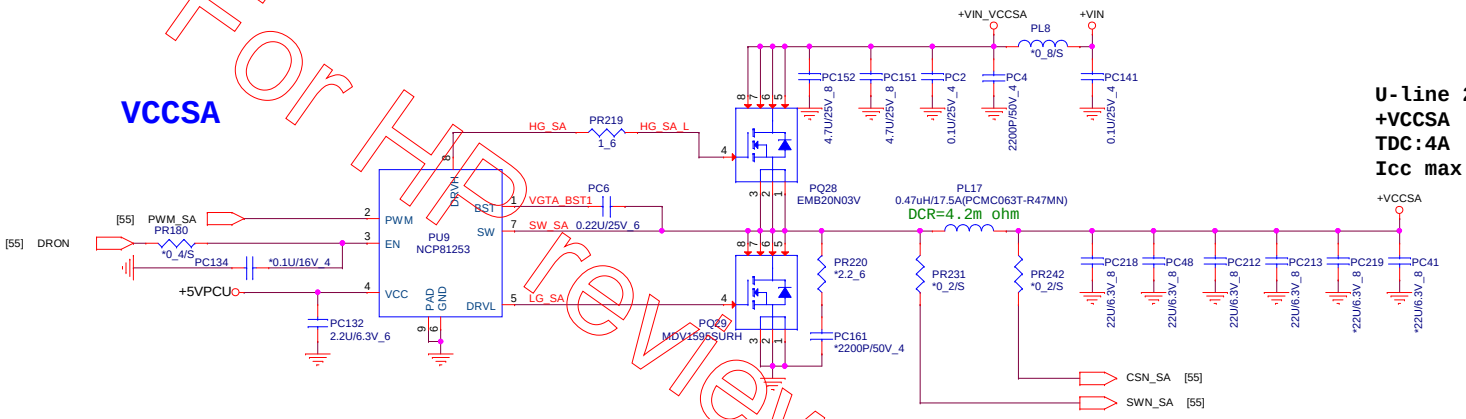
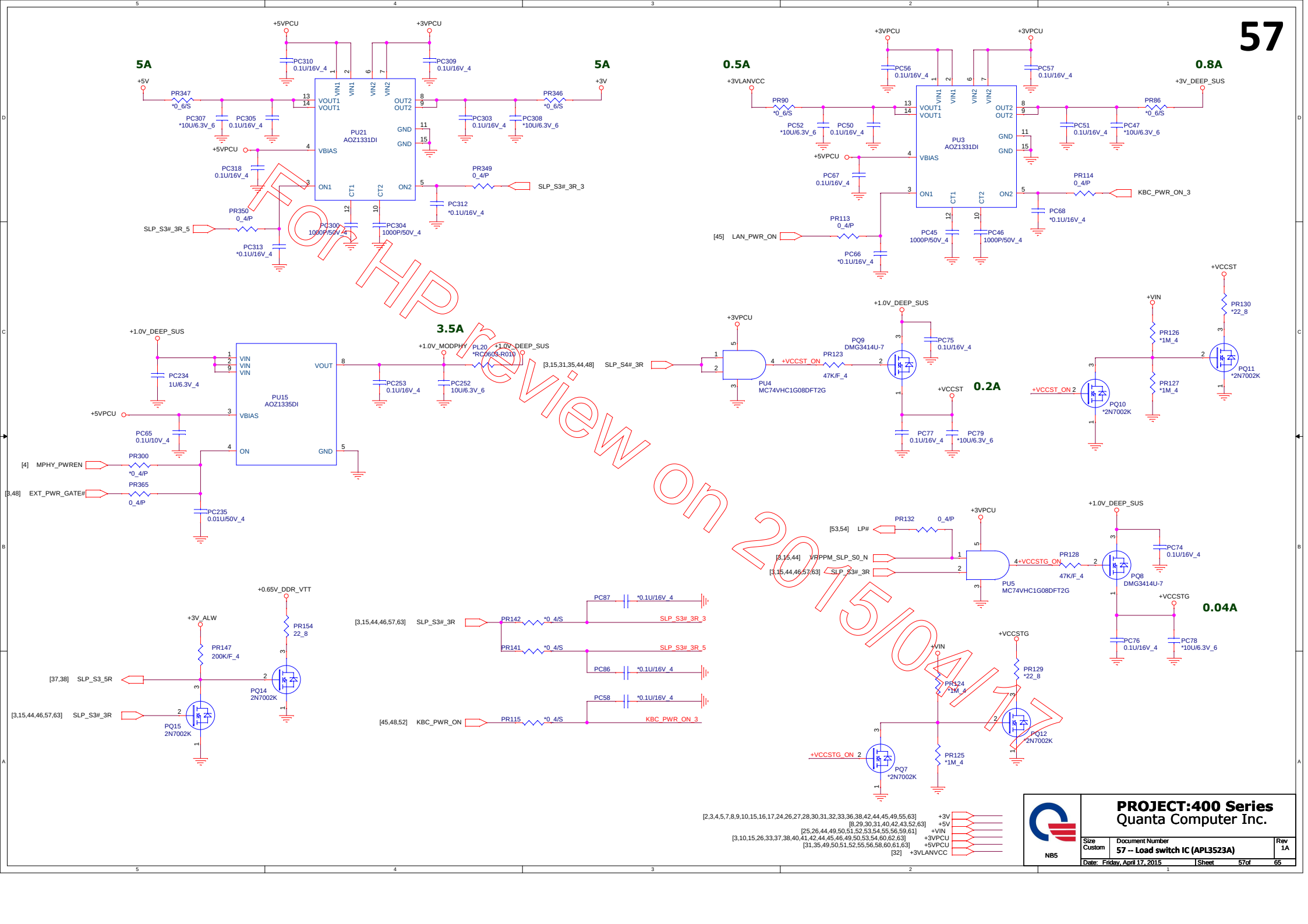
For HP review on 2015/04/17

VCCSA



U-line 22(15W)
+VCCSA
TDC:4A
Icc max:5A

NB5	**PROJECT:400 Series** Quanta Computer Inc.		
	Size: Custom	Document Number: **56 -- +VCCSA (NCP81253)**	Rev: 1A
	Date: Friday, April 17, 2015	Sheet: 56of 65	



For HP review on 2015/04/17

NB5

PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	57 -- Load switch IC (APL3523A)	1A
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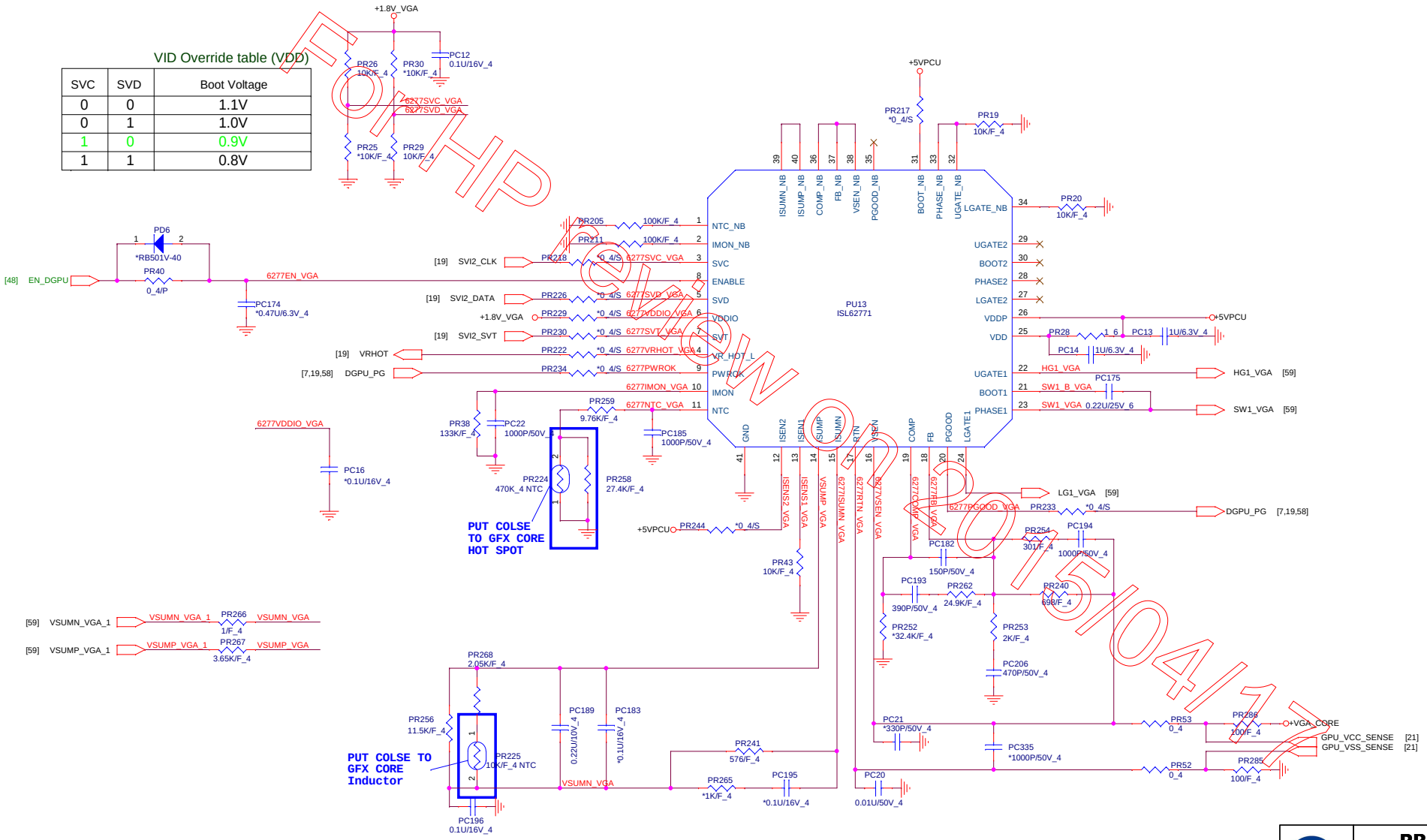
VID Override table (VDD)

SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V



FOR HP review 2015/04/17

PROJECT:400 Series
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	58 -- VGA Core1 (ISL62771)	1A

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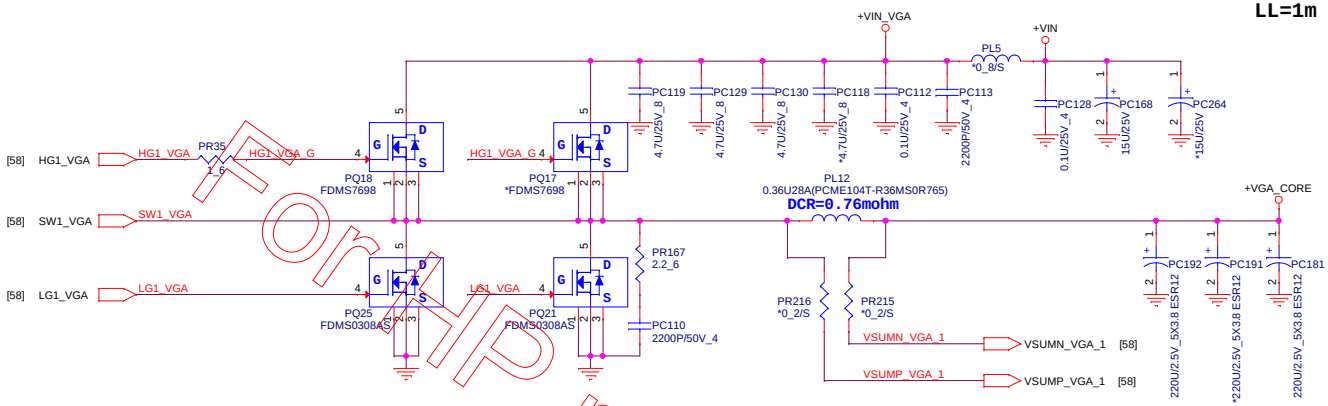
VGACORE (Meso PRO (DDR3)_ 25W/38W(1ms))
Countinue current:28A
OCP_SPIKE=47A(1ms)
LL=1m V/A



For HP review on 2015/04/17

NB5	**PROJECT:400 Series** Quanta Computer Inc.	
Size: Custom	Document Number: **59 -- VGA Core2**	Rev: 1A
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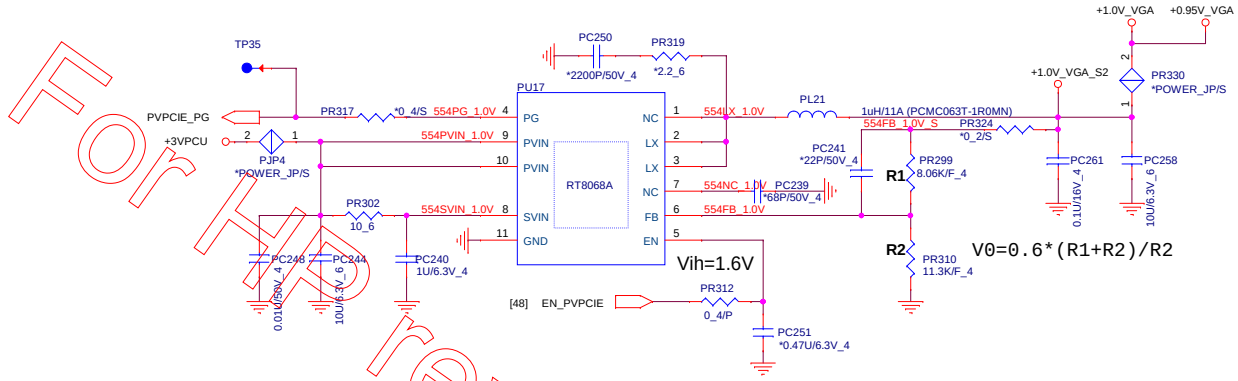
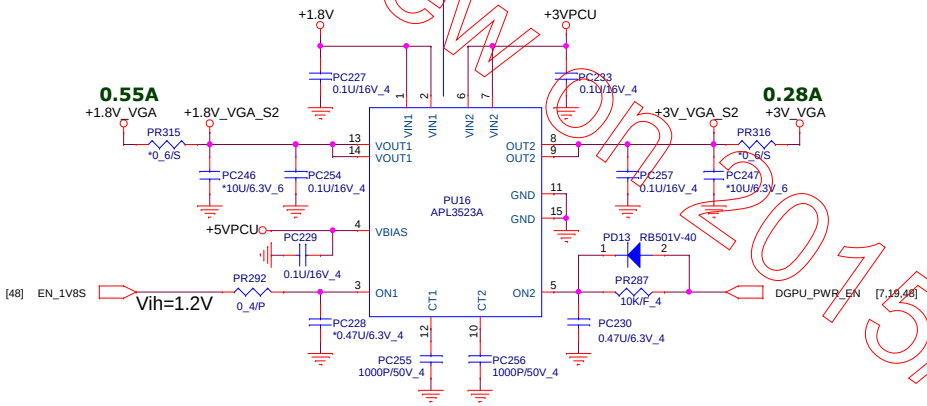
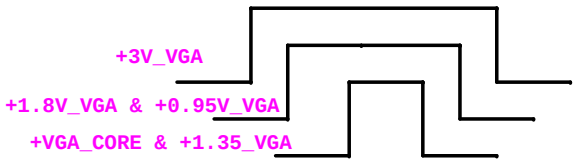
+1.0V_VGA +/- 3%
Countinue current:2A
Peak current:3A



PUT COLSE TO +1.8V power.





For Review on 2015/04/17

NB5	**PROJECT:400 Series** Quanta Computer Inc.	
Size: Custom	Document Number: **60 -- +1.0V_VGA/1.8V_VGA/3V_VGA**	Rev: 1A
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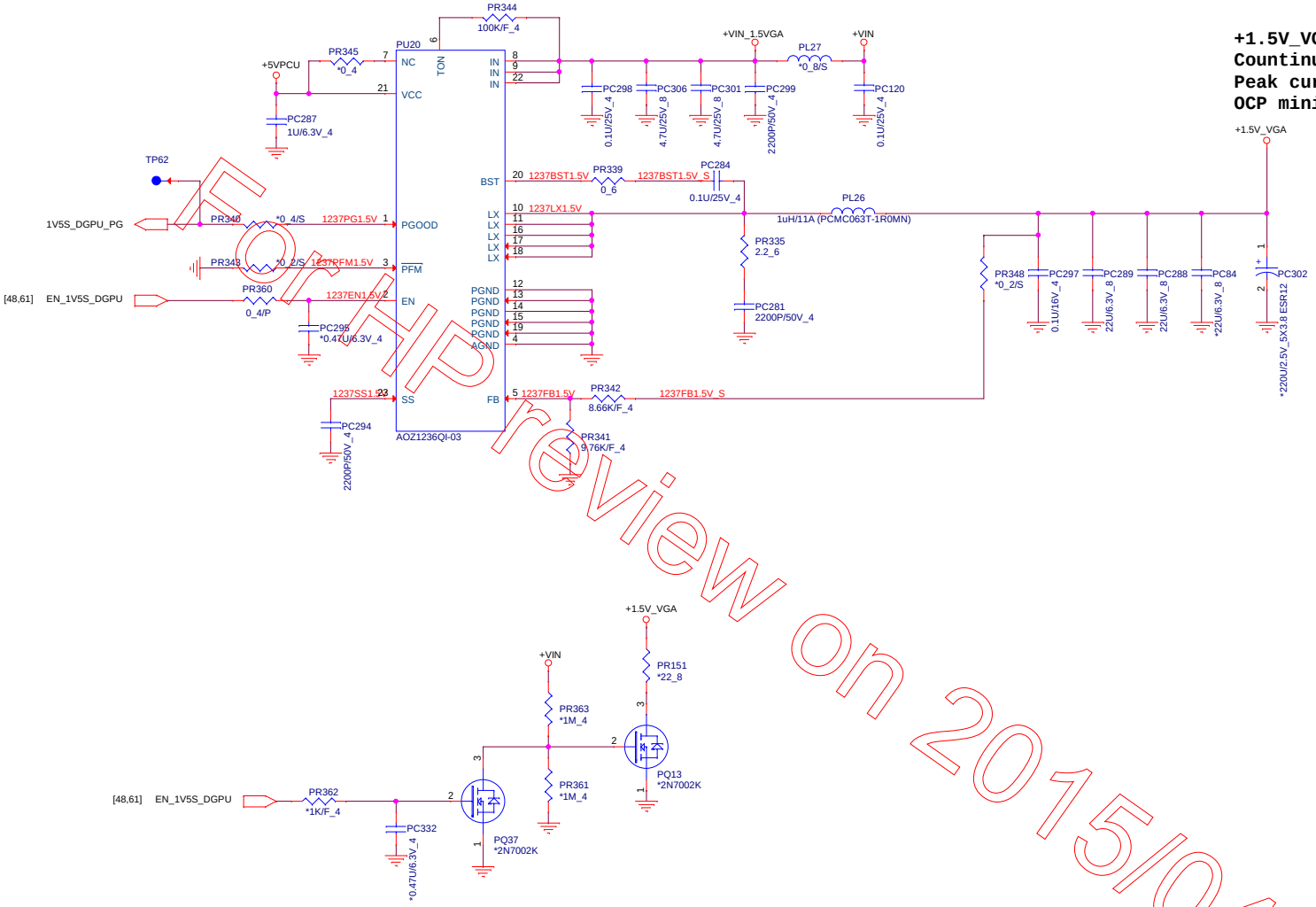
+1.5V_VGA Volt +/- 5%
Countinue current:4A
Peak current:5A
OCP minimum:8A



For Review on 2015/04/17

NB5	**PROJECT:400 Series** Quanta Computer Inc.	
Size: Custom	Document Number: **61 -- +1.35V_GFX (AOZ1267)**	Rev: 1A
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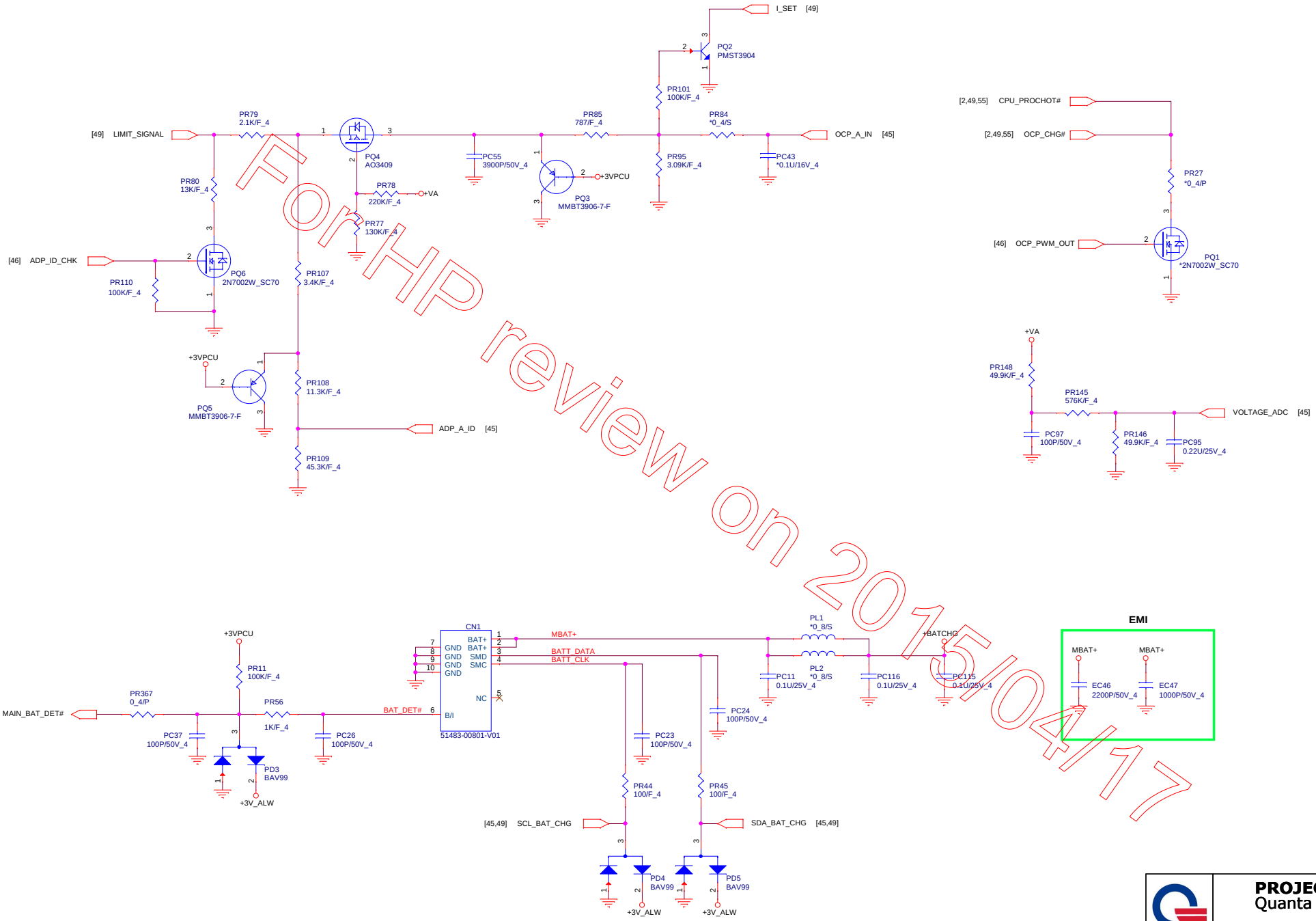
Adapter OCP



For HP review on 2015/04/17

NB5	**PROJECT:400 Series** Quanta Computer Inc.	
	Size: Document Number: 62 -- CHARGER II	Rev: 1A
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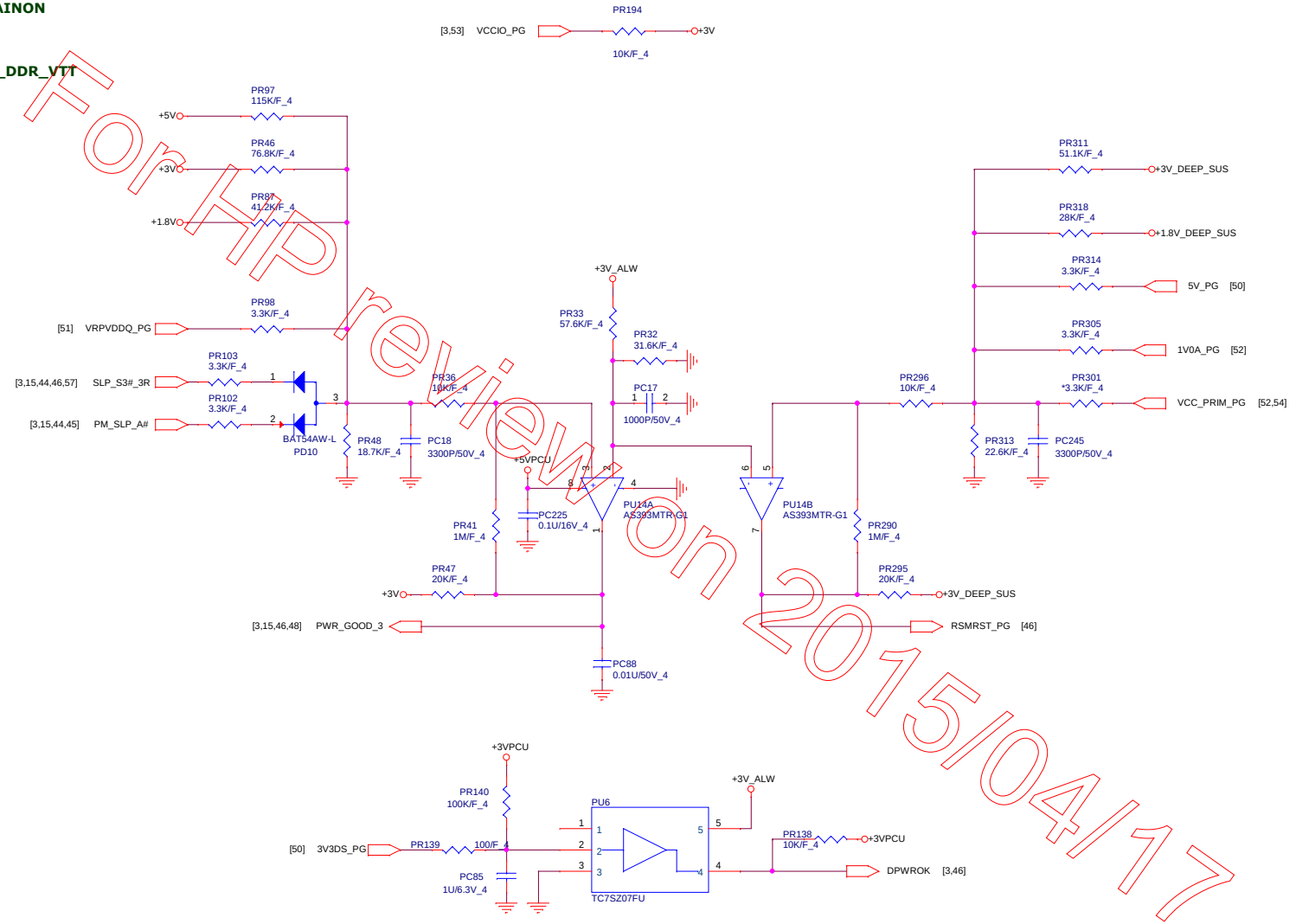
POK CKT

PM_SLP_S4# = SUSON
PM_SLP_S3# = MAINON
+V5S = +5V
+V3S = +3V
+V0.75S =+0.75V_DDR_VTT

For Review on 2015/04/17



[2,3,4,5,7,8,9,10,15,16,17,24,26,27,28,30,31,32,33,36,38,42,44,45,49,55,57] +3V
[8,29,30,31,40,42,43,52,57] +5V
[9,41,45,48,49,50,57,62] +3V_ALW

NB5

PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	**63 -- PWROK**	1A
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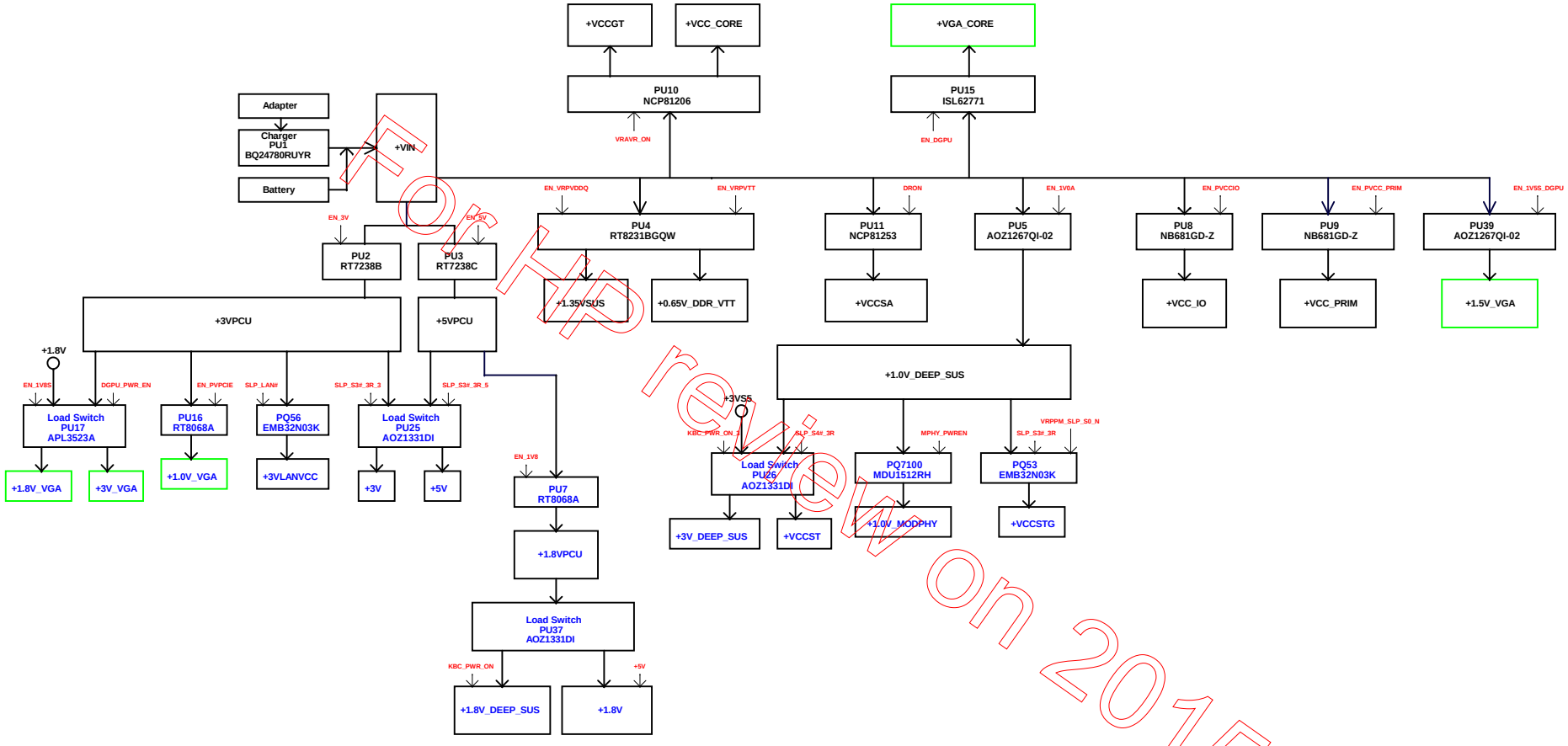
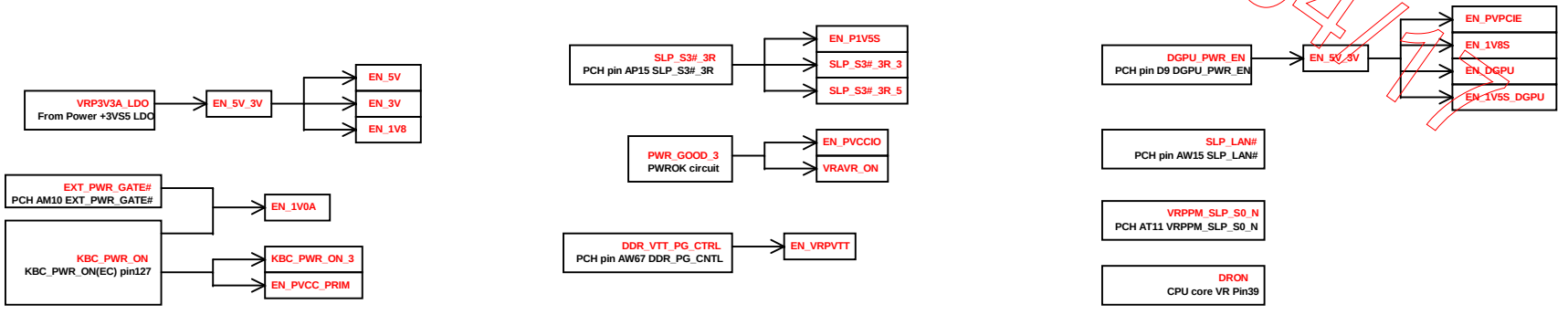
POWER BLOCK DIAGRAM



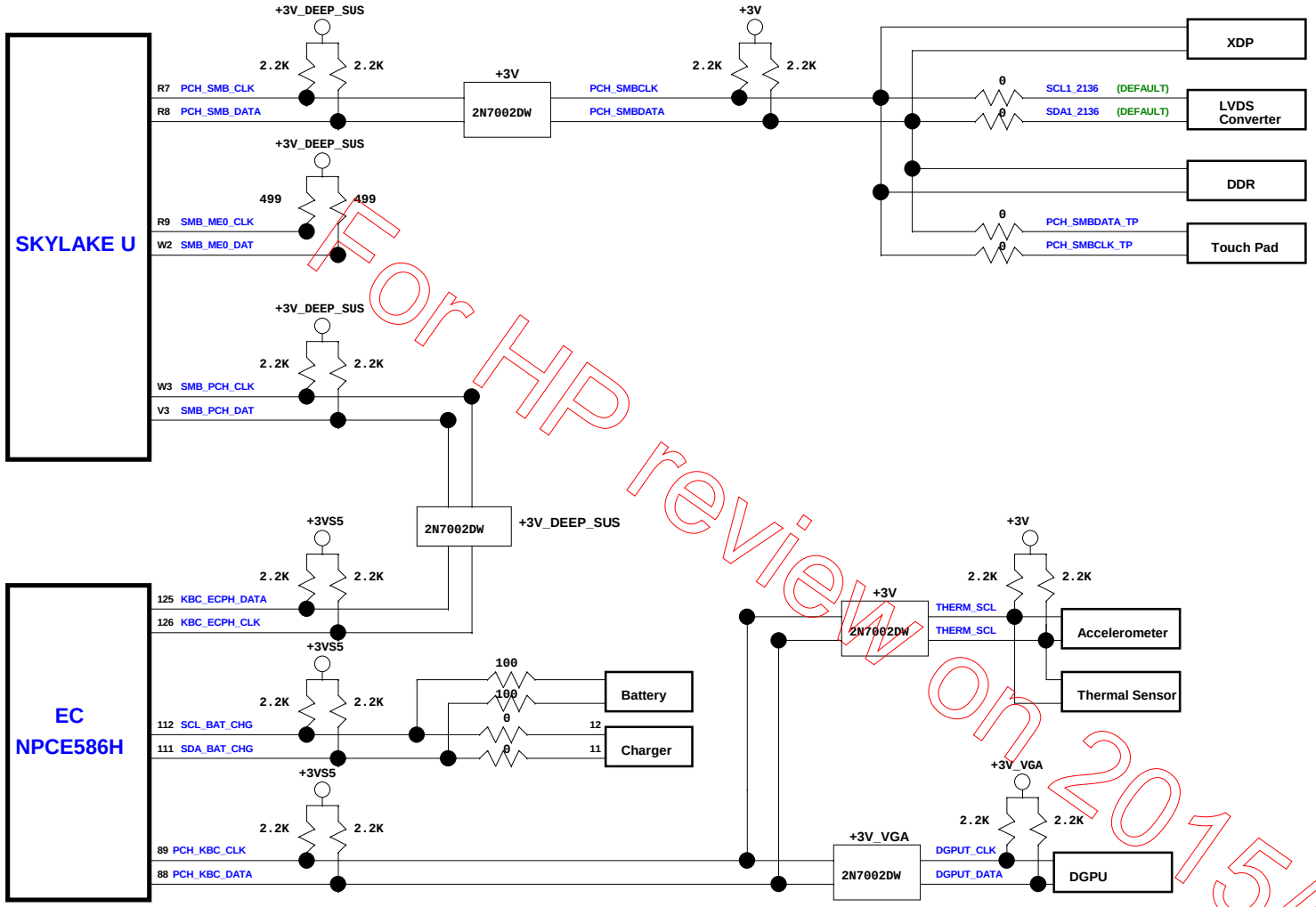
Not for review on 2015/04/17

POWER ENABLE PIN



PROJECT:400 Series
Quanta Computer Inc.

Size: Custom | Document Number: 64 – Power Block Diagram | Rev: 1A
Date: Friday, April 17, 2015 | Sheet: 64of | 93



Example: *499/F_4 and *0_6/S
* means none-installed
499 means value
F means 1%
_4 means 0402 size
/S means short pad

Multiplexed HSIO Lane	Port Assignment
USB3 #1	USB2.0/USB3.0 Combo Jack(Left side down)
USB3 #2 / SSIC #1	USB2.0/USB3.0 Combo Jack(Left side up)
USB3 #3 / SSIC #2	NC
USB3 #4	NC
PCIE1 / USB3 #5	dGPU
PCIE2 / USB3 #6	dGPU
PCIE3	dGPU
PCIE4	dGPU
PCIE5	LAN
PCIE6	WLAN
PCIE7 / SATA #0	HDD (SATA)
PCIE8 / SATA #1	ODD (SATA)
PCIE9	Cardreader (PCIE)
PCIE10	NC
PCIE11 / SATA #1*	NC
PCIE12 / SATA #2	SSD (SATA)

USB2.0	Port Assignment
USB2 #1	USB2.0/USB3.0 Combo Jack(Left side down)
USB2 #2	USB2.0/USB3.0 Combo Jack(Left side up)
USB2 #3	WWAN
USB2 #4	USB2.0(Right side on USB Board)
USB2 #5	USB2.0(Right side on USB Board)
USB2 #6	Touch Screen
USB2 #7	Bluetooth
USB2 #8	Finger Print
USB2 #9	Camera
USB2 #10	NC

For HP review on 2015/04/17

PROJECT:400 Series
Quanta Computer Inc.
Size: Custom | Document Number: 65 -- SMBus/Port Assignment | Rev: 1A
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